HP 3000 Series III Computer System

HP 30417A Upgrade Kit

Installation Guide

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LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. Changes are marked with a vertical bar in the margin. If an update is incorporated when an edition is reprinted, these bars are removed but the dates remain.

PRINTING HISTORY

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The date of the title page of the manual changes only when a new edition is published. When an edition is reprinted, all the prior updates to the edition are incorporated.

First Edition. . . . . .Sept 1978
Change 1 . . . . . Feb 1980

UPGRADE PROCEDURE OVERVIEW

This upgrade is completed in three steps.

1. First the HP 30311A Power Supplies are removed, modified, and replaced.

2. The CPU PCAs are removed; the CPU backplane is removed; and a new backplane is installed. Then updated PCAs replace Series II PCAs in the original PCA location.

3. The Series II Nameplate in the top of the CPU bay front dcor is replaced with a Series III Nameplate.

SERIES II TO SERIES III UPGRADE PROCEDURE

1. Ensure that the Series II is operational and runs all Series II microdiagnostics before proceeding.

2. Calculate memory size at 128K words per array PCA. Be sure to count the 256K supplied in this kit and any other memory ordered separately that is to be installed concurrent with the kit. Enter final memory size here:

   Memory size is _____K words.

3. At this time do a :SYSDUMP using a future date (for example 9/9/99) changing the memory size to the amount calculated. The tape will contain MPE and all accounting structure but no user files.

4. Proceed with an orderly shutdown of the operating system and equipment turn off as described in Appendix A.

POWER SUPPLY MODIFICATION

This modification replaces the mother board and control board in an HP 30311A Power Supply if date code if less than 1822. If no modification is necessary, return both the mother boards and the control boards shipped in the kit and skip this procedure. Repeat the procedure for systems having two HP 30311A Power Supplies. If system has but one HP 30311A, return one each Mother board and control board furnished in the HP 30417A Upgrade kit as well as the mother board and control board replaced in these steps. Figure 1 is provided as reference.

1. Disconnect plugs P2, P3, P4, and P5 on the rear panel of the power supply.

2. Remove four screws on the front of the cabinet securing the Power supply to the cabinet frame and the two screws on the right rear of the power supply and remove the power supply by sliding it forward.

3. Remove top and bottom covers from the power supply.

4. Free the mother board by removing four screws, two from the top and two from the bottom edges of the rear panel frame.

5. Remove two screws holdind the control board to the metal spacers on the top right side of the frame.

6. Disconnect plug P6 on the mother board and plug P2 on the front of the control board.

7. Slide the two boards out of the rear of the power supply frame.

8. Remove the heat sink from the mother board.

9. Remove the control board from J1 on the mother board. Set both boards aside in an area reserved for components to be returned to the factory.

10. Rebuild and reinstall power supply using new mother board and control board date coded 1822 or later.

11. Replace the heatsink.

12. Install date code tag furnished with the kit over old serial tag at rear of power supply.

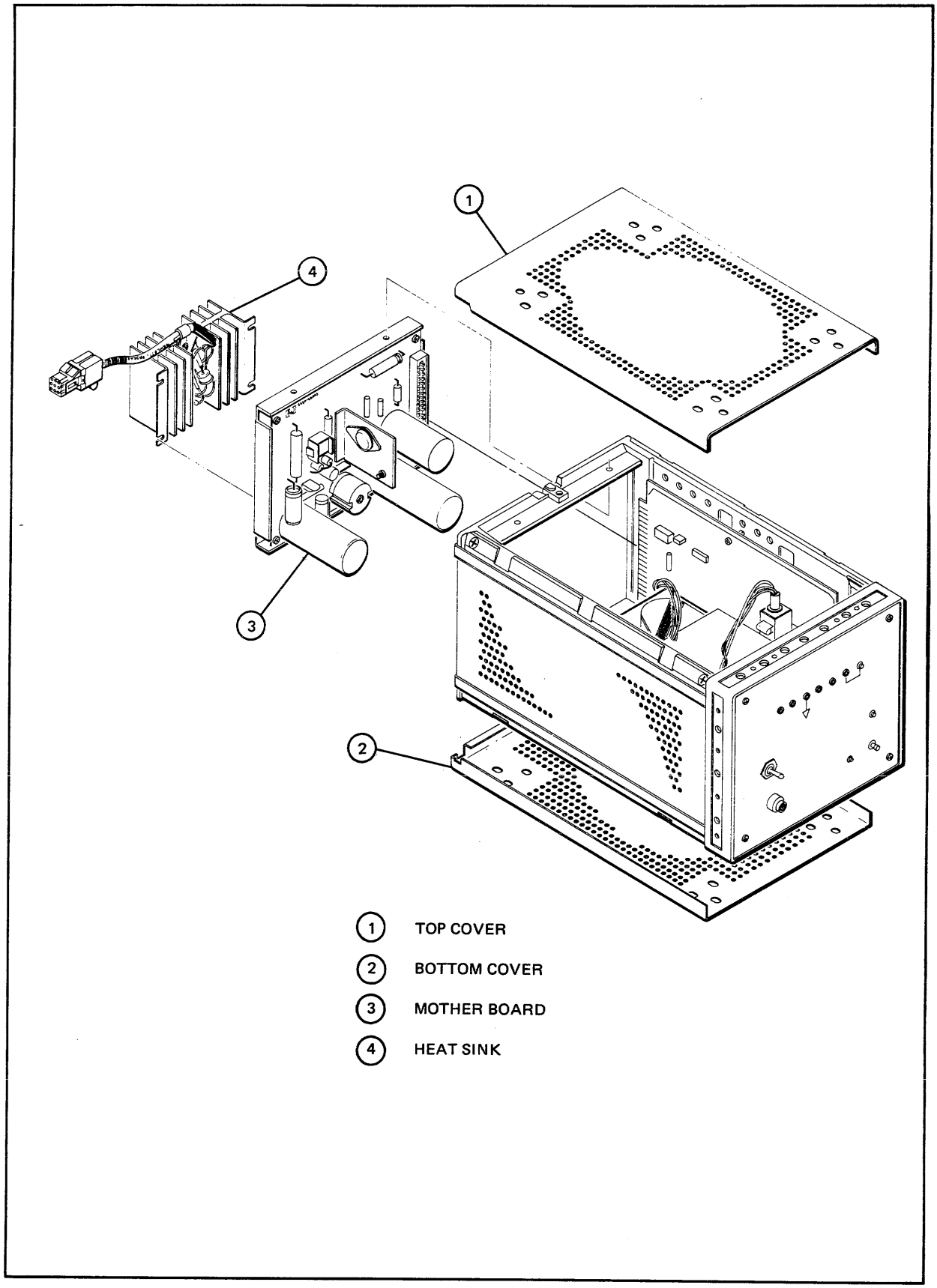


Figure 1. Power Supply Modification

PCA REPLACEMENT

1. Remove the following PCAs and set aside in area reserved for components to be returned to the factory.

   1 30003-60001 ROM PCA
   1 30003-60002 Skip and Special Field PCA
   1 30003-60005 S-Bus PCA
   1 30003-60008 IOP PCA
     30007-60002 Memory Control and Logging PCA
                 (Return 1 or 2)
     30008-60002 SMA PCAs (Return all)
     30009-60001 Fault Correction Array PCAs (Return 1 or 2)
   1 30030-60016 Port Controller PCA
   1 30030-60018 Selector Channel Register PCA
   1 30036-60001 Multiplexer Channel PCA

2. Remove all PCAs remaining in the CPU card cage and set aside for re-installation.

3. Disconnect cables at the CPU card cage backplane. This includes the IOP bus, CTL data bus, power bus, interrupt poll, data poll, and all MCUCLKs. Disconnect power harness. Remove the CPU backplane PCA 30003-60009. Retain small hardware. Set aside for return to the factory.

4. Install new CPU backplane PCA 30003-60029 using hardware saved. Restore power harness connections. See figure 1. DO NOT TIGHTEN BACKPLANE HARDWARE. CARD CAGE BACKPLANE HARDWARE MUST BE SNUG BUT MOVABLE FOR ALIGNMENT.

5. On the MCU PCA, remove jumper W4 (ENABLE 5) if it is installed. The Series III will not run if this jumper is installed. Appendix C summarizes switch settings for switches whose settings vary with the size of memory.

6. Install PCAs in the CPU card cage in the following order:

Slot	PCA
1A2	30012-60001 Expanded Instruction Set PCA
1A10	30003-60028 IOP PCA
1A5	30003-60003 ALU PCA
1A3	30003-60021 ROM PCA
1A4	30003-60022 Skip and Special Field PCA
1A6	30003-60004 R-Bus PCA
1A7	30003-60025 S-Bus PCA
1A8	30003-60006 CIR PCA
1A9	30003-60007 MCU PCA

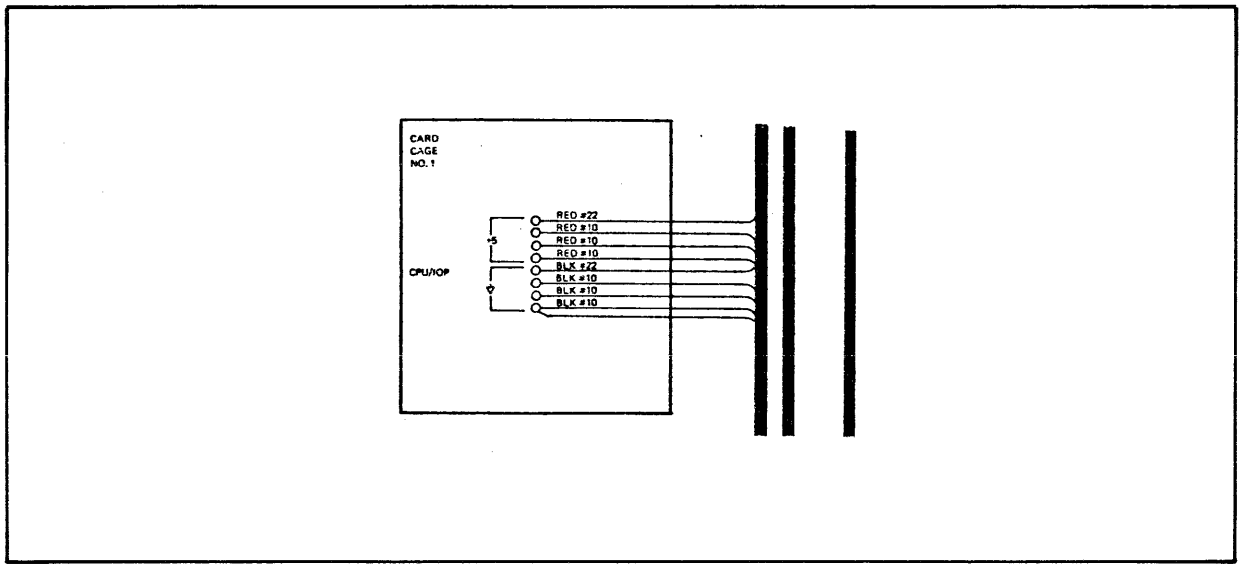


Figure 2. +5 Volt Connections

7. Tighten all CPU backplane mounting hardware.

8. Except for the 30009-60002 Fault Logging Interface PCA, empty card cages 2 and 3 of memory PCAs. Put all PCAs in the area being used for components to be returned to the factory. This includes all 30007-60002 Memory Control and Logging PCAs, 30008-60002 SMAs, and all 30009-60001 Fault Correction Arrays.

9. Set the READY/ENABLE switch on the 30007-60005 MCL PCA furnished with kit to position A and install it in slot A10 of card cage No. 2. If necessary, see Appendix C for the function of this switch.

   If a second 30007-60005 MCL PCA is on hand and is to be installed concurrently with this upgrade, set its READY/ENABLE switch to position B and install it in slot A1 of card cage No. 3.

10. Set the BOARD SELECT switch on one of the SMA PCAs furnished with this kit to 0 and install it in slot A6 of card cage No. 2. The BOARD SELECT switch on the second SMA PCA is set to 1 and installed in slot A7 of card cage No. 2.

    If other 30008-60003 SMA PCAs are to be installed, see Appendix C for switch settings and figure 3 for flat cable connections.

11. Install the following PCAs in locations previously made available by PCA removable:

    30030-60020 Port Controller
    30030-60021 Selector Channel Register
    30036-60002 Multiplexer Channel Register
    30036-60002 Multiplexer Channel

    Re-install flat cables on selector channel in their original configuration.

12. If a second selector channel exists within this system, see Appendix E.

13. Noting orientation of each CTL data bus terminator, remove and replace with kit furnished 30003-60030 terminators.

14. Re-install cabling at the CPU backplane that was disconnected earlier. This includes the IOP bus, CTL data bus, power bus, interrupt poll, data poll, and MCUCLKs.

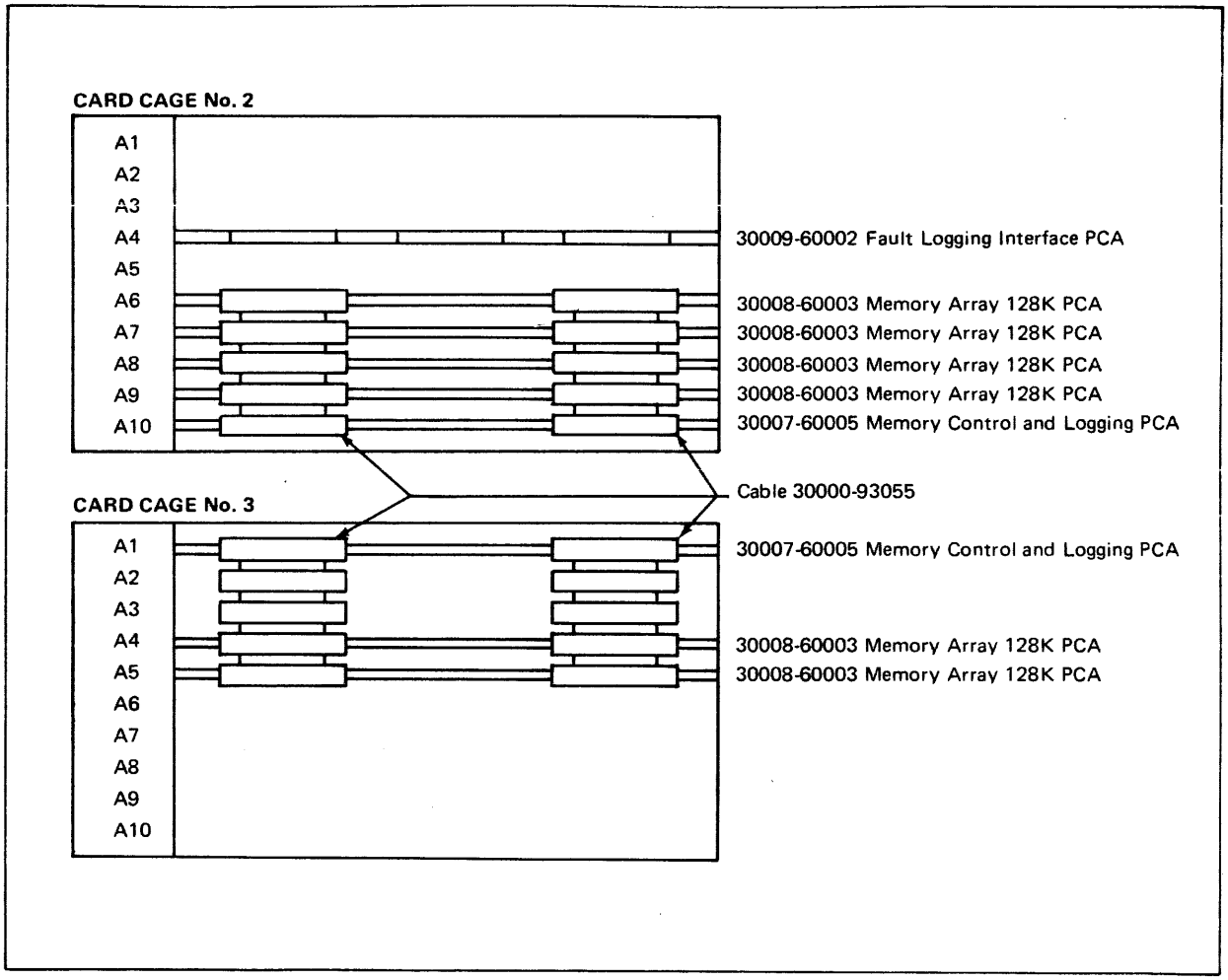


Figure 3. Memory Configuration

SERIES III NAMEPLATE INSTALLATION

The following hardware is provided for items which may be used up or broken during installation of the Series III nameplate.

1. RING-RETAINER. This is a "C" shaped retainer for the ferrule at the EMERGENCY OFF switch.

2. PUSH-ON RETAINER. This is a round washer for retaining the ferrule at the EMERGENCY OFF switch.

3. CLIP/HOLDER COMPONENT. These "black rings" are used to secure the LED holder and LEDS.

4. CABLE TIES.

Proceed as follows.

1. At the DC Control Panel, unplug the cable to the System Control Panel. At the System Control Panel, disconnect at two terminals; then disconnect at the two LEDs. Cut two cable ties and remove cable. See figure 4.

2. Remove three screws that attach bottom of the System Control Panel to a trim strip.

NOTE

In the step which follows, the System Control Panel and the trim strip beneath it will be freed from the front door. BE CAREFUL NOT TO DROP THEM.

3. Remove four screws holding the top of the System Control Panel to the front door. Remove the System Control Panel and the trim strip. The trim strip is easily removed; the System Control Panel may be hindered by front door hardware and require some lateral and downward movement.

4. Remove three screws and cable tie support at top of door that fasten the nameplate holder to the door and remove.

5. At the back of the nameplate holder, remove the retaining ring on the translucent EMERGENCY OFF switch extension tube. Remove the tube.

6. Remove the push on retainer holding the metal ferrule in place and remove the ferrule. (Two spare push on retainers are included in the kit in case one breaks.)

7. Remove the black rings holding the LED holders in place. Remove the LEDs and the LED holders.

8. Slide the Series II nameplate out of the holder and slide the Series III nameplate in.

9. Insert the two LED holders, replace the LEDs, and fasten with the black rings.

10. Insert the metal ferrule and secure with a push on retainer. Insert switch extension tube and secure with retaining ring.

11. Use the three screws and cable tie support removed in step 4 to fasten nameplate and nameplate holder to the door.

12. Put the trim strip in place and mount the System Control Panel using 7 each lock washers and screws removed in steps 2 and 3.

13. Use cable ties to fasten cable 30003-60014 (removed in step 1) to the top and side of door. See figure 4.

14. Connect orange wire to the long pin and the yellow wire to the short pin at the first LED from the edge of door. The green wire goes on the long pin and the blue wire goes on the short pin of the remaining LED. Connect the red wire to the top terminal (+5) of the System Control Panel and the brown wire on the bottom. Plug the cable to the System Control Panel to the DC Control Panel.

15. On DC Control Panel, install UPPER MEMORY label over UPPER 128K MEMORY silkscreen and LOWER MEMORY label over LOWER 128K MEMORY silkscreen.

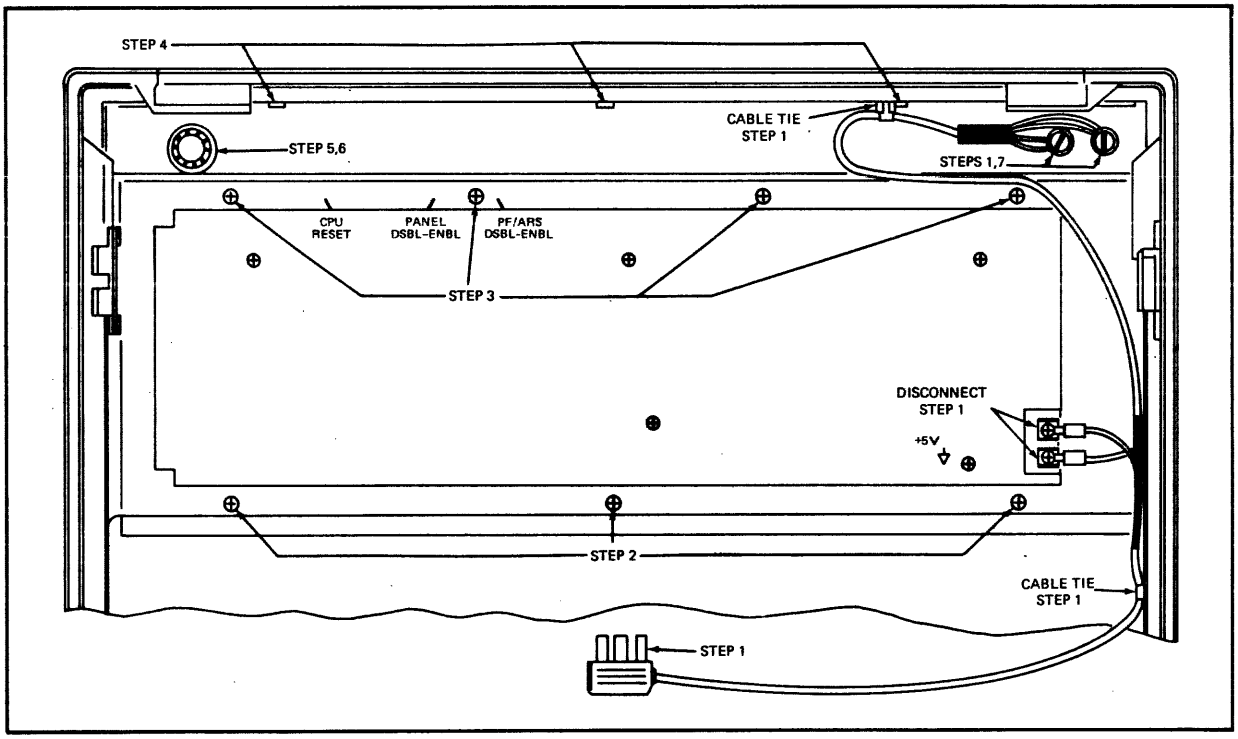


Figure 4. Hardware Installation at Top of CPU Front Door

SYSTEM TURN ON

Restore power to the system as follows:

1. At the Power Control Module, throw the circuit breaker on.

2. On the DC Control Panel, set the SYSTEM, UPPER MEMORY, and LOWER MEMORY toggle switches to ON.

3. Turn on and adjust all power supplies as described in Appendix B.

4. Run the microdiagnostics as described in Appendix D.

5. Reload the future-dated SYSDUMP tape that was created in step 3 on page 1. Refer to the System Manager/System Supervisor Reference Manual.

The upgrade is now complete. Have the customer use his Date 0 backup tape to restore all files using the "Keep" option of the "Restore" command. The customer should then perform a SYSDUMP Date 0 to configure a magnetic tape backup for the new memory size.

SYSTEM SHUT-DOWN

APPENDIX A

This appendix contains a procedure for an orderly shut down of an HP 3000 Series III Computer System.

IMPORTANT

> The installation of the upgrade kit destroys the existing accounting and file structure. It will be necessary for the customer to re-create and/or restore his accounts and files after the upgrade is complete.

Prior to shut down of the system, ensure that the customer's System Supervisor has backed up his entire system with a :SYSDUMP Date 0. The System Supervisor should also be advised while that his account, group, user, and directory information is preserved on the magnetic tape produced by the :SYSDUMP, experience has shown that it is also a good idea to keep all created account structures on some offline medium such as a magnetic tape stream file or a job card deck.

If the customer has not shut down the system, request his console operator or some other responsible person to do so. The command =SHUTDOWN is a system operator's capability.

With the system shut down, turn off system power as follows:

a. On the DC Control Panel, set the SYSTEM, UPPER MEMORY, and LOWER MEMORY switches to STANDBY.

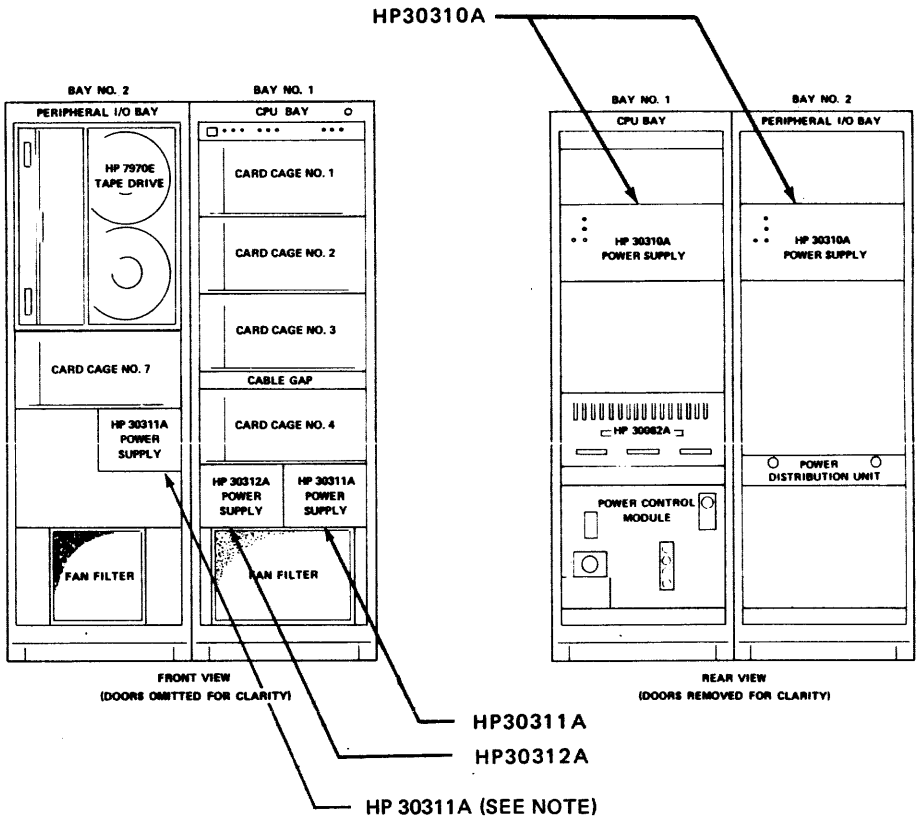
b. On the HP 30310A Power Supplies, set the POWER toggle switches to OFF.

c. On any 30311A Power Supplies, set the power switch to off (down).

d. On any 30312A Power Supplies, set the POWER switch to OFF.

e. If the system has an HP 2888A Disc File, set the circuit breaker on the Power Control Unit to OFF.

f. Set the circuit breaker on the Power Control Module to OFF.



NOTE: MODEL 6 WITH 160K WORDS OR GREATER, OR SERIES III WITH 768K WORDS OR GREATER.

Figure A-1. Power Supply Locations, HP 3000 Series III

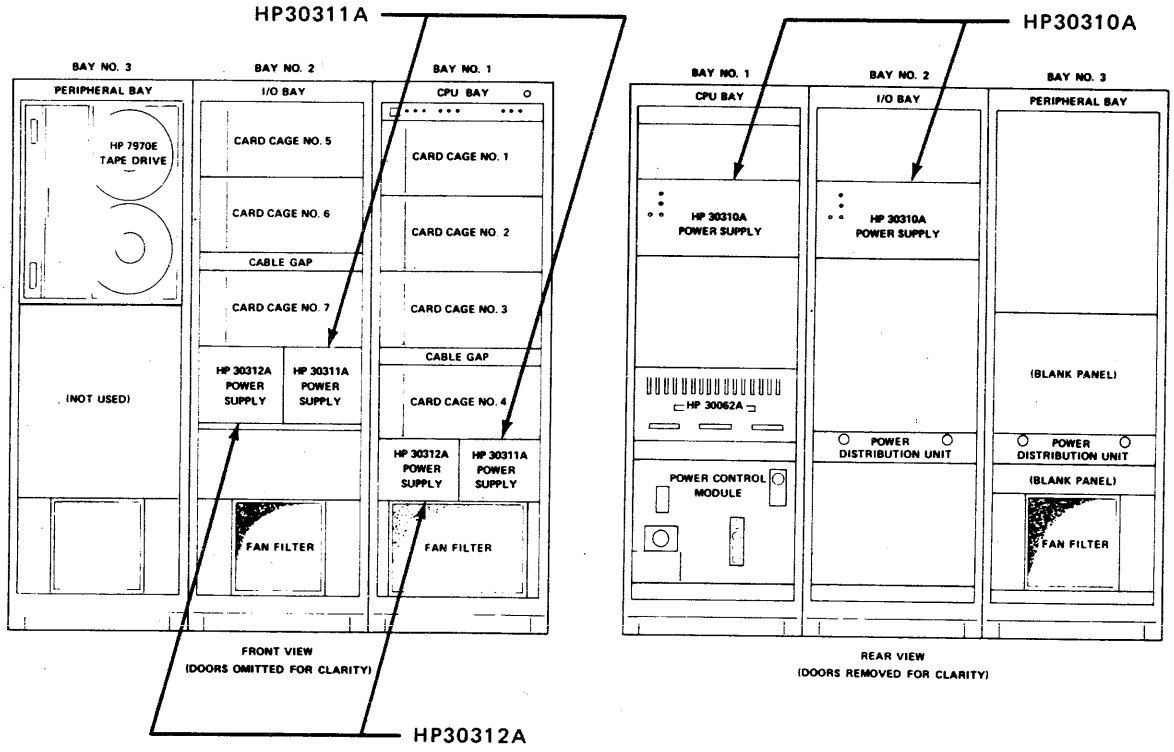


Figure A-2. Power Supply Locations, HP 3000 Series III - Option 200

POWER SUPPLY ADJUSTMENTS

APPENDIX B

IMPORTANT**** The HP 30310A Power Supply must be operating with an approximate 100-watt load while its output voltages are being checked or adjusted. Such a load may be attained by installing 5 PCAs in the card cage it is supplying power. It may be necessary to rearrange PCAs in the I/O bay or PIO bay before attempting these adjustments.

After the system hardware has been configured with all PCAs in place and all associated hardware installed, DC power may be returned from STANDBY to ON at the DC Control Panel. Power supplies will now be turned on and adjusted here. Perform the steps once for the CPU bay and once for the second bay of a two-bay system.

A digital voltmeter (HP 970 or equivalent) and an oscilloscope (HP 180 or equivalent) are required.

CPU Bay I/O Bay

[1] [1] At the HP 30310A Power Supply, turn power ON and check the lighted +5 indicator. Adjust the + 20V ADJ A3R2 fully clockwise in the CPU bay and in the I/O bay.

[2] [2] Monitor the 5V output at any P1-20(+) and P1-40(-) at the CPU backplane or P1-1(+) and P1-10(-) at card cage No.5 (top card cage of bay 2). If necessary use +5,+15 ADJ control to produce reading of 5.17 volts (CPU card cage) or 5.11 volts (top card cage of bay 2).

[3] [3] Check that -5, +15, and -15 test points are within limits as follows:

VOLTAGE TEST POINT	MINIMUM READING	MAXIMUM READING	RIPPLE VOLTAGE TOLERANCE
+15	+14.2	+16.7	0.4V P-P
+5	+ 5.11	+ 5.17	0.4V P-P
-5	- 4.4	- 5.7	0.4V P-P
-15	-14.2	-16.7	0.4V P-P

4 4 With oscilloscope, check ripple voltages against table values.

5 5 At the HP 30311A Power Supply, turn power on and check the lighted +5 indicator. Check that the BATTERY STATUS indicator is flashing at a 0.5 Hz rate or on continuously. At the front panel, connect the voltmeter between +12 and "common" test jacks. If necessary, use +12V ADJ to produce reading of 12.0 plus or minus 0.12.

6 6 Check that +5B, +12.7B, -3B, and -5B test points are within limits as follows:

TEST JACK	INDICATION
+ 5B	+5.1 + or - 0.1
+12B	+12.0 + or - 0.1
+12.7B	Voltage measured at +12B test jack plus 0.7 + or - 0.2 volts.
- 3B	-3.0 + or - 0.25
- 5B	-5.0 + 0r - 0.20

NOTE

If all voltages are out of tolerance, adjust the +5 Internal Reference of the HP30311A Power Supply first. This adjustment is described in the HP 3000 System Service manual.

7 7 At each 30312A Power Supply, set the ADJ R32 potentiometer fully clockwise. Press and hold toggle switch S2 and turn ADJ R32 counterclockwise until the LED in the upper right corner of the front panel just lights indicating "over current". Back off slightly until the LED goes out. Release toggle switch S2 and chek that the "over current" LED is off and the +5 LED is on.

MEMORY CONFIGURATION

APPENDIX C

GENERAL

This appendix provides PCA switch data for switches that are subject to change with a change in memory size. The positions and functions of other switches on the affected PCAs are also included. Figure C-1 shows approximate location of the switches.

PORT SELECTOR PLUG

The Selector Channel Register PCA in slot A8 of card cage No. 3 must have its port selector plug in socket XW1 if the system has only one selector channel. If the system has a second Selector Channel Register in slot A1 of card cage No. 4, the plug is installed in socket XW1 and the plug in the Selector Channel Register in slot A8 of card cage No. 3 is installed in XW3. Flat Cable 30000-93052 is installed on connector J3 of the Port Controller and Register in slots A7 and A8 of card cage No. 3 when this channel is configured as XW3.

MEMORY SIZE

Memory size affects switch S3 on the S-Bus PCA, IOP PCA, and Selector Channel Register PCA. Switch S3 is positioned according to memory size in words as follows:

1	128K	3	384K	5	768K
2	256K	4	512K	6	1024K

MEMORY INTERLEAVING

Switches S1 and S2 on the S-Bus PCA, IOP PCA, and Selector Channel Register PCA are configured as follows:

Mode	S1						S2					
	1	2	3	4	5	6	1	2	3	4	5	6
Non-Interleaving	C	C	C	C								C *
*Applies to IOP PCA only.												

On each PCA, open all switch positions of S1 and S2, then close switch positions according to mode where a C appears in the above table.

NOTE

On initial release of the Series III, memory interleaving is not supported. All systems are presently configured by switches S1 and S2 for the non-interleaving mode.

ERROR LOGGING ARRAY CLEAR

The error logging array on the Memory Control and Logging PCA can be cleared by using the momentary switch S1 on the front edge of the PCA. The array is normally cleared by software or at system turn on.

READY/ENABLE SELECT

This switch S2 is set to position A on the Memory Control and Logging PCA in card cage No. 2 and to position B of the Memory Control and Logging PCA in card cage No. 3.

NOTE

This is a convention used in the factory; one switch must be set to A and one to B.

BOARD SELECT

Each Semiconductor Memory Array PCA has a four-position switch S1 that is set according to its location in the card cage as follows:

Card Cage No. 2		Card Cage No. 3	
SLOT	POSITION	SLOT	POSITION
A6	0	A2	3
A7	1	A3	2
A8	2	A4	1
A9	3	A5	0

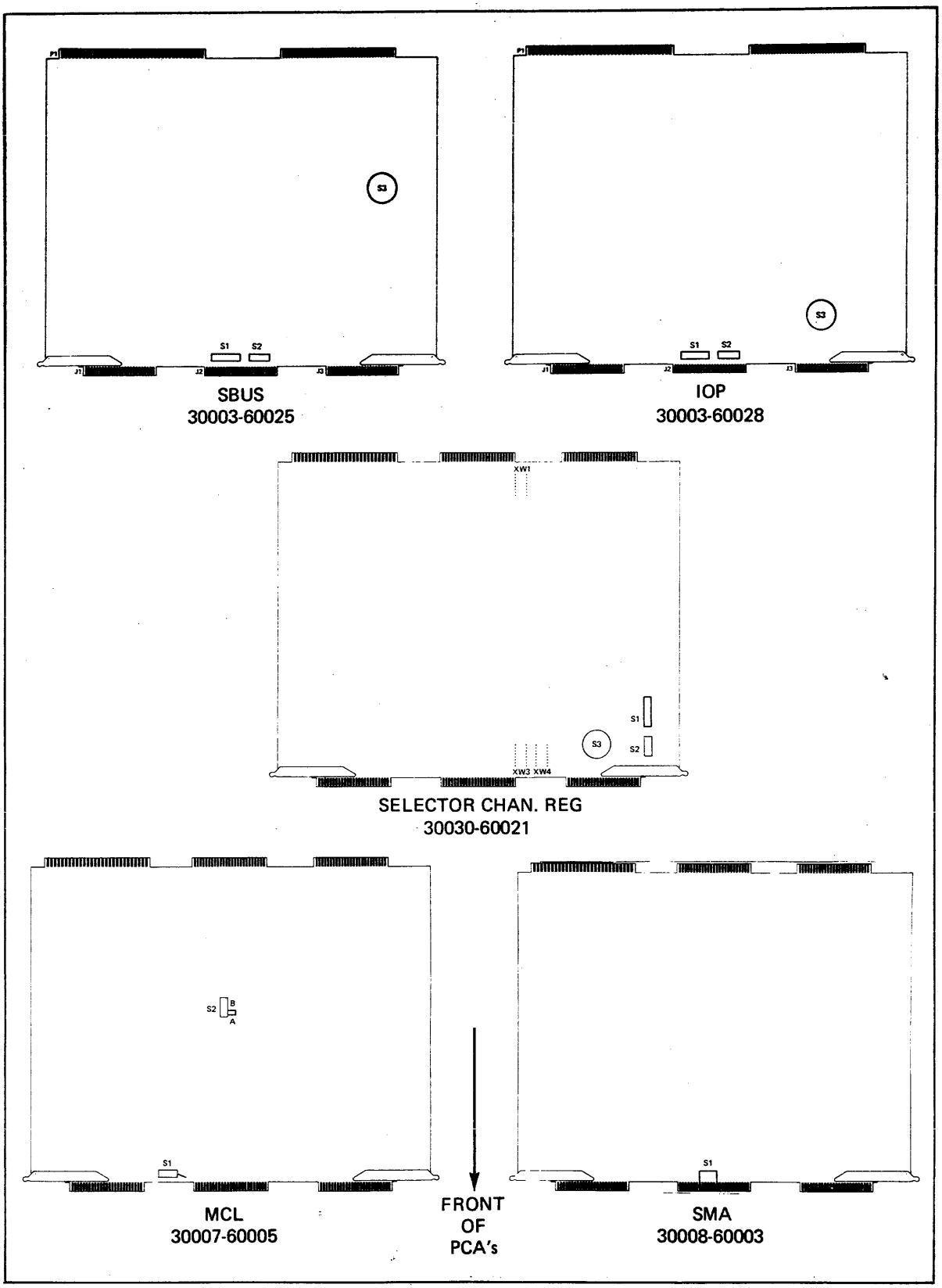


Figure C-1. Memory Associated PCAs

SERIES III MICRODIAGNOSTICS

APPENDIX D

D-1. CONTROL PANEL TESTS AND FUNCTIONS

Stored in the microcode are diagnostics to test the CPU registers, memory, I/O channels, magnetic tape subsystem, and the asynchronous terminal data PCAs. Diagnostics are executed from the system's control panel. The microcode also provides the following functions:

a. Display Memory Logging Errors

b. Read/Write Memory

c. Display Register Contents

D-2. CPU REGISTER TEST

Proceed as follows to test the various CPU registers.

a. Set the SYSTEM SWITCH REGISTER to %000001.

b. Press the ENABLE and LOAD switches.

c. The program runs continuously until the HALT switch is pressed or until an error occurs.

Upon detection of an error, the test pauses in the run mode with the CURRENT INSTRUCTION REGISTER (CIR) displaying "bad bits". Press the RUN/HALT switch to obtain a code designating the failing register. Decode the display using table D-1.

Table D-1. CPU Register Codes

CIR	REGISTER	LOCATED ON
00	SP1 (Note)	R-Bus PCA
01	PL	R-Bus PCA
02	Z	R-Bus PCA
03	X	R-Bus PCA
04	RD (R-Bus)	R-Bus PCA
05	RC (R-Bus)	R-Bus PCA
06	RB (R-Bus)	R-Bus PCA
07	RA (R-Bus)	R-Bus PCA
10	SPO	R-Bus PCA
11	CRTL	S-bus PCA
12	P	S-Bus PCA
13	Q	S-Bus PCA
14	DB	S-Bus PCA
15	SM	S-Bus PCA
16	STA	SSF and S-Bus PCA's
17	SP3	S-Bus PCA
20	OPND	CIR PCA
21	DL	S-Bus PCA
22	SP2	S-Bus PCA
23	PB	S-Bus PCA
24	PCLK	S-Bus PCA
25	RD (S-Bus)	S-Bus PCA
26	RC (S-Bus)	S-Bus PCA
27	RB (S-Bus)	S-Bus PCA
30	RA (S-Bus)	S-Bus PCA
31	CTRH	S-Bus PCA
32	ABS BANK	SSF PCA
33	PB BANK	SSF PCA
34	DB BANK	SSF PCA
35	S BANK	SSF PCA

NOTE

SP1 is the first register tested and the problem may not necessarily be in SP1 but somewhere previous in the data path (Store logic, Shifter, ALU, etc.)

D-3. MEMORY PATTERN TEST

This test writes then immediately reads back any bit pattern entered into the SYSTEM SWITCH REGISTER. The pattern pervades all of memory. The initial pattern is 100000. The current pattern is displayed in the CIR. Invoke the test as follows:

a. Set the SYSTEM SWITCH REGISTER to %100000.

b. Press the ENABLE and LOAD switches.

c. The test runs continuously until an error occurs or if the RUN/HALT switch is pressed until the end of a pass.

If an error is detected, the test halts and the CIR displays the error type as follows:

```
CIR = 0      Data Compare Error
CIR(4) = 1   System Parity Error
CIR(5) = 1   Address Parity Error
CIR(6) = 1   Multiple-Bit Error
```

Press the RUN/HALT switch for a CIR display of memory bank number, press again for address, and press again for expected data XOR actual data (bad bits).

D-4. MEMORY ADDRESS TEST

This test loads the memory with address dependent data then checks it while reading it back. Perform this test as follows:

a. Set the SYSTEM SWITCH REGISTER to %000000.

b. Press the ENABLE and LOAD switches.

c. The test runs continuously until an error occurs or if the RUN/HALT switch is pressed until the end of a pass.

If an error is detected, the test halts and the CIR displays the error type as follows:

```
CIR = 0      Data Compare Error
CIR(4) = 1   System Parity Error
CIR(5) = 1   Address/Data Bus Parity Error
CIR(6) = 1   Multiple-Bit Error
```

Press the RUN/HALT switch for a CIR display of memory bank number,press again for address, press again for actual data, and press again for expected data.

D-5. I/O TEST (TIO)

This test sends a TIO command to device numbers octal 2 through 177 in turn, then pauses with the TIO status of each responding device in the CIR. Pressing the RUN/HALT switch advances to the next device. Perform the test as follows:

a. Set the SYSTEM SWITCH REGISTER to %000002.

b. Press the ENABLE and LOAD switches. The test pauses with 000002 in the CIR. This is the device number of the FLI PCA.

c. Press the RUN/HALT switch to display TIO status of that device.

d. Press the RUN/HALT switch for the device number of the next responding device, then once more for TIO status of that device.

e. Repeat step "d" until the CIR displays %000200 and the SYSTEM HALT light is lit.

D-6. I/O TEST (SIO)

This test executes an SIO program consisting of only an END-ORDER for all devices in turn that have the SIO OK bit set in the TIO status word. It pauses for each with the END-ORDER status in the CIR. Press the RUN/HALT switch to advance to the next device. Perform the test as follows:

a. Set the SYSTEM SWITCH REGISTER to %100002.

b. Press the ENABLE and LOAD switches.

c. The CIR displays the device number of the first responding device that has the SIO OK bit set in its TIO status. Press RUN/HALT to display SIO END-ORDER status for that device.

d. Press the RUN/HALT switch for the device number of the next responding device, then once more for SIO status of that device.

e. Repeat step d until the CIR displays %000200 and the SYSTEM HALT light is lit.

D-7. START I/O TEST

This function issues a start I/O (SIO) command to a device then waits for an interrupt from that device. A RIL is sent to any other interrupting devices. Ater receiving the interrupt, the function system-halts with the CIR displaying TIO status from the device if the command succeeded or 030370 if the command failed.

This function assumes that an SIO program is already in memory and that the DRT pointer at DEVNO*4 has been initialized.

Use the function as follows:

a. Set the SYSTEM SWITCH REGISTER to %005000.

b. Press the ENABLE and LOAD switches. The system pauses with 005000 in the CIR.

c. Set the SYSTEM SWITCH REGISTER bits 9 through 15 to the device number.

d. Press the RUN/HALT switch to send the SIO command to the device.

D-8. MAG-TAPE TEST

This test writes a 4K-word record to tape from each memory bank correcting for tape errors by issuing a backspace record followed by a write gap and then retrying. After this writing operation, the tape is rewound and each 4K-word record is read into another area of its source memory bank. The data written is compared with the data read and the test halts if an error is detected. The test runs continuously if no error is found. If the SIO command to the tape unit fails, the test halts with 030370 in the CIR. Invoke the test as follows:

a. Set the SYSTEM SWITCH REGISTER to 006000.

b. Press the ENABLE and LOAD switches. The test pauses with 006000 in the CIR.

c. Set bits 7 through 15 of the SYSTEM SWITCH REGISTER to the device number of the tape drive to be tested.

d. Press the RUN/HALT switch to start the test.

On a halt, the CIR displays the current bank in bits 0 through 3 and the mag tape command in bits 12 through 15. The test halts if an error is detected or if the RUN/HALT switch is pressed until a pass is completed. If the test halts on an error, subsequent pressing of the RUN/HALT switch causes the following sequence of displays.

1	STATUS	Privileged mode, enable interupt, CST #1*
2	SP1	Data word written
3	SP2	Data word read
4	TOS	Not used
5	PB-BNK	Current I/O bank address
6	PB	SP1 XOR SP2 (failing bit)
7	P	Write buffer address
8	PL	Read buffer offset
9	DB-BNK	Not used
10	DB	Device number under test
11	S-BNK	Always 0
12	DL	CCPX parameter word
13	Q	Device number times 4 (DRT)
14	SM	Used as address pointer to build SIO program.
15	Z	I/O bank in bits 0, 1, and 2
16	INDEX(X)	Interrupting device number

* 14001

D-9. ASYNCHRONOUS TERMINAL CONTROLLER SUBSYSTEM

This test causes characters typed on a selected terminal to be echoed and the ASCII code of the character to appear in bits 7 through 15 of the CIR. A non-responding device halts the test with 030370 in the CIR. Run the test as follows:

a. Set the SYSTEM SWITCH REGISTER to %007000.

b. Press the ENABLE and LOAD switches. The test pauses with 007000 in the CIR.

c. Enter the device number of the asynchronous terminal controller in bits 7 through 15 and the port number in bits 3, 4, 5, and 6.

d. Press the RUN/HALT switch. The test pauses with the CIR equal to the switch register.

e. Enter the character size parameter into bits 5, 6, and 7 and the baud rate parameter into bits 8 through 15.

f. Press the RUN/HALT switch. The test pauses with the CIR equal to the switch register.

g. Press the RUN/HALT switch.

h. Strike keys on the terminal's keyboard and observe that that the characters are echoed correctly and the ASCII code for each character is displayed in bits 7 through 15 of the CIR.

The character size parameter is the three least significant bits of the sum of the number of start, parity, data, and stop bits in a transmitted character less one.

To calculate the baud rate parameter divide decimal 14400 by the device bit rate, round off to the nearest integer, and subtract one. Convert the decimal answer to octal.

Some octal examples of character size and baud rate parameters are as follows:

DEVICE	CHARACTER PARAMETER	BAUD PARAMETER	OVERALL() SETTING
ASR 33 Teletype	2	202	1202
30-CPS Terminal	1	057	457
60-CPS Terminal	1	027	427
120-CPS Terminal	1	013	413
240-CPS Terminal	1	005	405

D-10. DISPLAY MEMORY LOGGING ERRORS FUNCTION

This function transfers the contents of the error logging arrays (one error logging array is on each of up to two MCL PCAs) to the I/O logging array on the fault logging interface (FLI) PCA. It then interrogates the FLI PCA and displays the diagnostic status word in the CIR for each error logged. The diagnostic status word, figure D-1, contains the information needed to find failing RAMs. Use this function as follows:

a. Set the SYSTEM SWITCH REGISTER to %001000.

b. Press the ENABLE and LOAD switches. The test pauses with 001000 in the CIR.

c. Press the RUN/HALT switch to observe the RIO status word for the first error logged. If no errors are logged, the CIR display is %000000 and the SYSTEM HALT light is lit.

d. Press the RUN/HALT switch again for the next and subsequent errors. When the CIR display is 000000 and the SYSTEM HALT light is lit, all errors have been observed.

The function system halts with 030370 in the CIR if the FLI PCA does not respond. When an error is detected, use the flowchart, figure D-2, to isolate the error to a single bit error, a double bit error, or more than a double bit error. Table D-2 is used with Figure D-2.

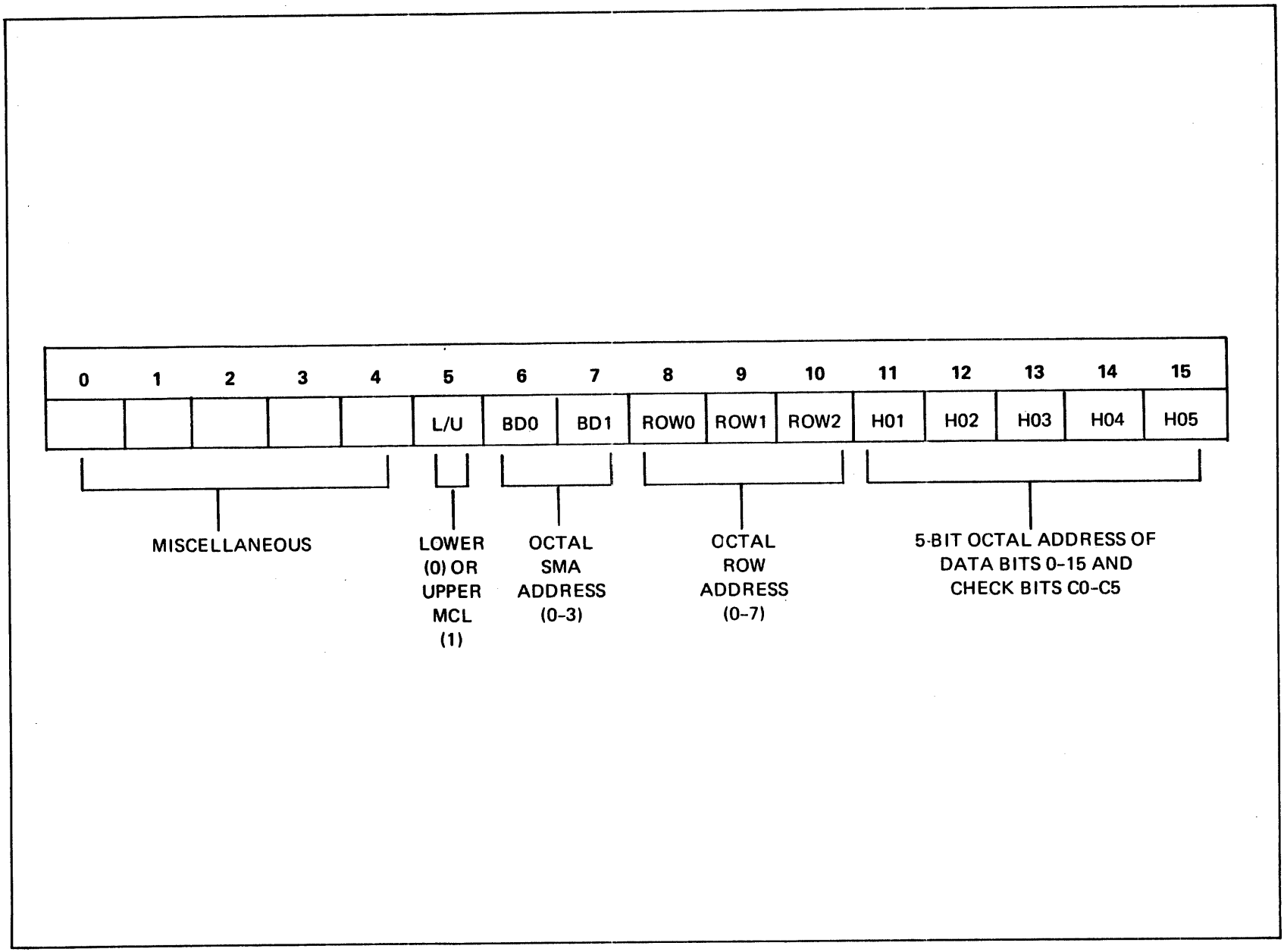


Figure D-1. Diagnostic Status Word

Table D-2. 5-Bit Octal ELAD to Data or Check Bits Conversion (More than Single Bit Errors)

H01-H05	A	B	
	BIT	BITS	
00	C0		
01	C5	D0, 2, 3, 4, 5, 6, 7	–
02	C4	D1, 2, 3, 8, 9, 10, 11	–
03	D3	D0, 1, 2, 4, 7	C5
04	C3	D0, 4, 5, 9, 12, 13, 14	–
05	*Note 1	D0, 1, 3, 4, 5, 6, 7	C5
06	D9	D0, 1, 2, 8, 10, 11	C4
07	D0	D1, 2, 3, 5, 6, 9	–
10	C2	D1, 6, 8, 10, 12, 13, 15	–
11	D6	D0, 1, 2, 4, 5, 7	C5
12	*Note 2	D0, 1, 3, 8, 9, 10, 11	C4
13	D1	D0, 2, 3, 4, 6, 7	–
14	D13	D0, 4, 8, 12, 14	C3
15	D4	D1, 3, 5, 6, 13	–
16	D8	D0, 3, 9, 10, 11, 13	–
17	*	D0, 1, 2, 3, 4, 5, 6, 8	–
20	C1	D2, 7, 11, 12, 14, 15	–
21	D7	D1, 2, 3, 4, 5, 6	C1
22	D11	D0, 2, 3, 8, 9, 10	C1
23	D2	D0, 1, 3, 5, 6, 7, 11	–
24	D14	D0, 5, 8, 9, 12, 13	C1
25	D5	D0, 2, 4, 6, 7, 14	–
26	*	D0, 3, 8, 9, 10, 11, 14	–
27	*	D0, 1, 2, 3, 4, 5, 7	–
30	D15	D1, 4, 6, 10, 12, 13	C1
31	*	D1, 3, 4, 5, 6, 7, 15	–
32	D10	D1, 2, 8, 9, 11, 15	–
33	*	D0, 1, 2, 3, 5, 6, 10	–
34	D12	D4, 5, 8, 9, 13, 14, 15	–
35	*	D0, 2, 4, 5, 6, 7, 12	–
36	*	D1, 2, 8, 9, 10, 11, 12	–
37	*	D1, 2, 3, 4, 7	–

COLUMN A IS FOR SINGLE CHECK OR DATA BIT ERRORS.
COLUMN B IS FOR MULTIPLE DATA OR CHECK BIT ERRORS.

Notes: 1. Forced Double Error Write.
2. Missing Array Board.

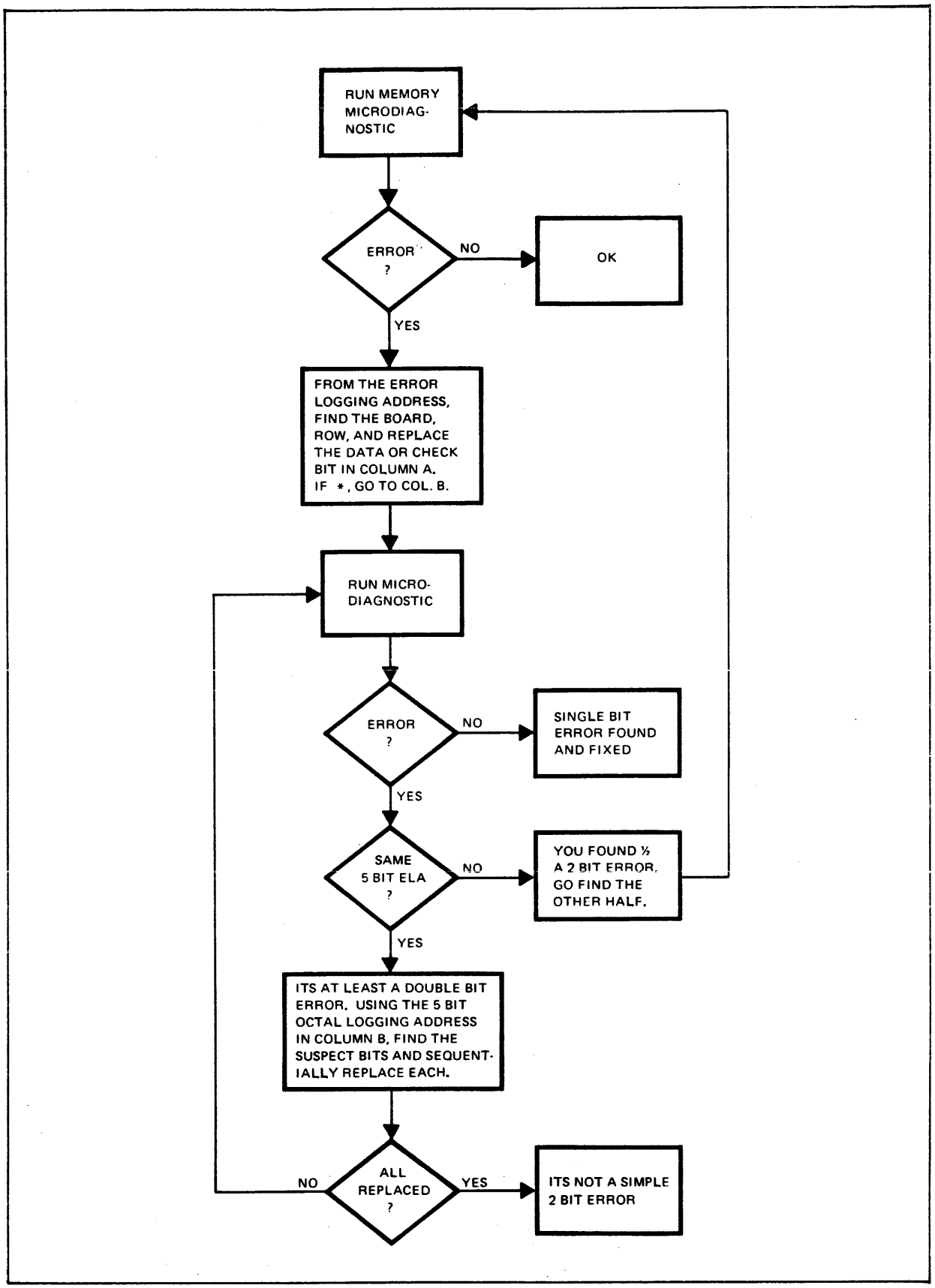


Figure D-2. Faulty Chip Locating Flowchart

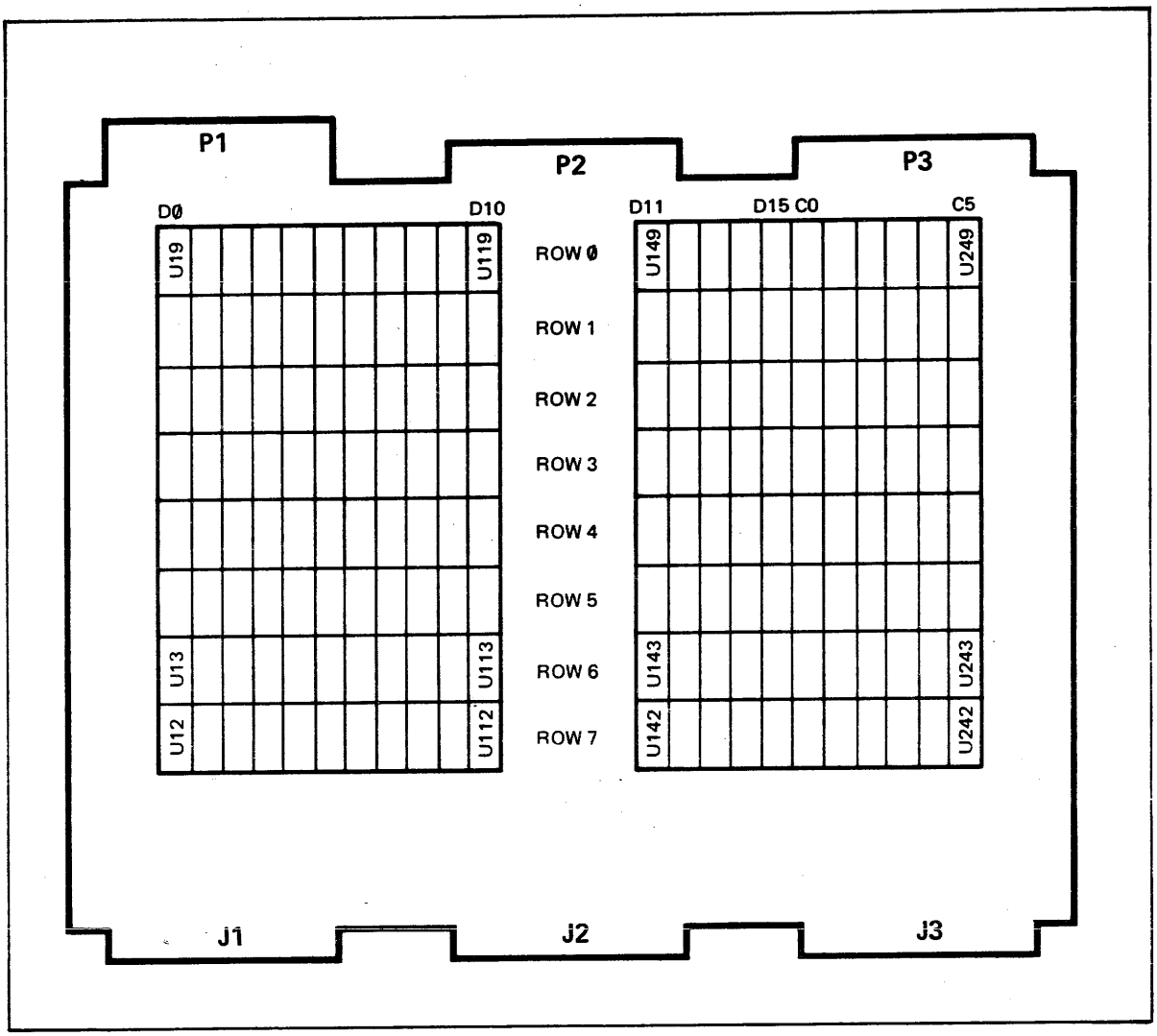


Figure D-3. Row and Chip Locator

D-11. CONTROL PANEL READ/WRITE MEMORY FUNCTION

This function allows memory to be written or read from the system control panel on a word-by-word basis. The function allows reading and writing while incrementing memory addresses or decrementing memory addresses.

To use this function, set one of the following bit patterns into the SYSTEM SWITCH REGISTER.

1. To write while incrementing memory: 002000
2. To read while incrementing memory: 003000
3. To write while decrementing memory: 102000
4. To read while decrementing memory: 103000

Then proceed as follows:

a. Press the ENABLE and LOAD switches. The system pauses with the CIR equal to the switch register.

b Enter the selected bank address (%0 -%17) in bits 12 through 15 of the SYSTEM SWITCH REGISTER.

c. Press the RUN/HALT switch. The system pauses with the bank number in the CIR.

d. Enter the starting address (%0 - %177777) in the SYSTEM SWITCH REGISTER.

e. Press the RUN/HALT switch. The system pauses with the starting address of the read or write operation in the SYSTEM SWITCH REGISTER.

For a memory write, set the data word to be written into the SYSTEM SWITCH REGISTER. Press the RUN/HALT switch to write the first data word at the starting address. If required, change the data word in the SYSTEM SWITCH REGISTER and press the RUN/HALT switch to write the data word at the incremented or decremented memory address. The data word is displayed in the CIR after it is written into memory.

For a memory read, press the RUN/HALT switch to read the data word at the starting address. The data word is displayed in the CIR. Press the RUN/HALT switch again to read the data word at the incremented or decremented address.

Addresses do not cross bank boundaries, address 000000 follows address 177777.

A SYSTEM/HALT occurs if an attempt is made to read or write non-existent memory.

D-12. DISPLAY REGISTER FUNCTION

This function displays the contents of most of the CPU registers and also the contents of the top-of-stack in memory. Pressing the RUN/HALT switch causes the CIR to display the contents of the following registers in the order shown below:

00 - STATUS	10 - DB bank
01 - SP1	11 - DB
02 - SP2	12 - S bank
03 - TOS = MEM(SM)	13 - DL
04 - PB bank	14 - Q
05 - PB	15 - SM
06 - P	16 - Z
07 - PL	17 - X

To use this function, proceed as follows:

a. Set the SYSTEM SWITCH REGISTER to 004000.

b. Press the ENABLE and LOAD switches. The system pauses with 004000 in the CIR.

c. Press the RUN/HALT switch as needed to observe register contents.

The function will SYSTEM HALT when the index register (X) has been displayed.

SYSTEM WITH TWO SELECTOR CHANNELS

APPENDIX E

NOTE

There is no Selector Channel number two in a Series III System.

Designate the Selector Channel nearest the Port Controller as No. 3 and install the configuring jumper plug of its Selector Channel Register PCA in socket XW3.

Designate the second Selector Channel as No. 1 and install the configuring jumper plug of its Selector Channel Register PCA in socket XW1.

Install the short flat cable 30000-93052 supplied with the upgrade kit on J3 of the upper Selector Channel Register PCA (new channel No. 3) and J3 of the Port Controller PCA. No cabling is required for the lower Selector Channel other than original flat cables.