OPERATING AND SERVICE MANUAL

12920A

ASYNCHRONOUS MULTIPLEXER INTERFACE KITS

(FOR 2100 SERIES COMPUTERS)

Printed-Circuit Assemblies:

12921-60001, Series 1222
12921-60002, Series 1203, 1215, 1229
12922-60001, Series 1220

Options Covered

This manual applies to option 001 as well as the standard version of the HP 12920A Asynchronous Multiplexer Interface Kit.

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LIST OF ILLUSTRATIONS

TERMINAL CONTROLLER/MULTIPLEXER
CONNECTOR PANEL

*ASYNCHRONOUS
MULTIPLEXER
CONTROL
ASSEMBLY
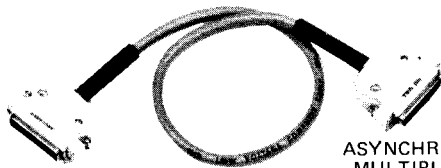
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MULTIPLEXER
TEST CABLE
ASSEMBLY
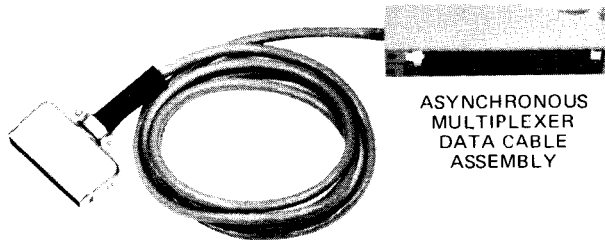
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DATA CABLE
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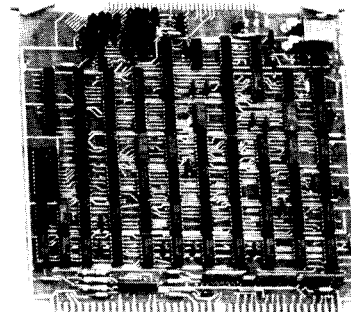
ASYNCHRONOUS MULTIPLEXER
DATA ASSEMBLIES
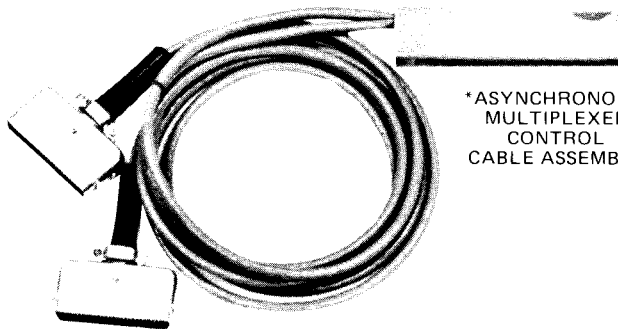
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MULTIPLEXER
CONTROL
CABLE ASSEMBLY
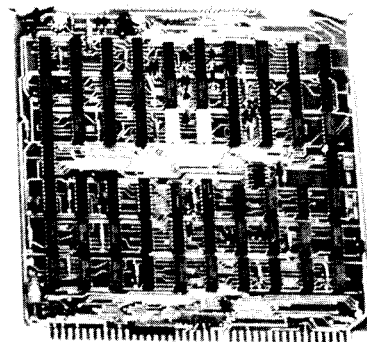
NOTE: THE HP 12920A-001 INCLUDES ONLY THOSE ITEMS MARKED WITH AN ASTERISK (*).

2176-17A

Figure 1-1. HP 12920A and HP 12920A-001 Asynchronous Multiplexer Interface Kits

1-1. INTRODUCTION.

1-2. This manual provides general information, installation, programming, theory of operation, maintenance, and replacement parts information for the HP 12920A and HP 12920A-001 Asynchronous Multiplexer Interface Kits (see figure 1-1). The HP 12920A Interface Kit provides multiplexed I/O capability for up to 16 type-103 data sets or bit serial, EIA RS232C compatible terminals such as teleprinters, card readers, or similar devices. With the optional HP 12920A-001 Interface Kit added, the combined kits provide multiplexed I/O capability for up to sixteen 202-type data sets or up to eight 801 computer-controlled, automatic dialers (see figure 1-2). Information in this manual applies to both interface kits unless otherwise noted.

1-3. DESCRIPTION.

1-4. The asynchronous multiplexer interface kit (multiplexer) provides 16 input and 16 output channels and the necessary control signals to exchange data between a Hewlett-Packard computer and up to 16 remote data sets or terminals. The input and output channels are independent so that full duplex and splitspeed devices may be interfaced. Five additional channels are available internally for diagnostic purposes. The HP 12920A Multiplexer contains all of the items listed in table 1-1, while the optional HP 12920A-001 Multiplexer contains only those items designated with an asterisk in table 1-1. Common names listed in table 1-1 are used throughout this text.

1-5. Each of the 16 input/output channels provides a path for transfer of control, status, and bit-serial data signals between the computer and an asynchronous device. This device can be a data set, data set compatible CRT,

teleprinter, card reader, or a similar device. Selection of the channel number, input or output operation, data-bit transfer (baud) rate, character format, and terminal control are all programmable. This allows the computer to service any mix of asynchronous, bit-serial devices on the 16 input/output channels. The multiplexer input/output signal levels are compatible with Electronic Industries Association (EIA) Standard RS-232-C specification.

1-6. The multiplexer connector panel provides 16 input/output connectors designated J0 through J15. These connector designations correspond to the assigned input/output channel numbers 0 through 15. All even numbered connectors carry data, control, and status lines for their assigned channel and also carry some control and status lines for the next odd numbered channel. For example, connector J0 carries all lines for channel 0 and also some of the control and status lines for channel 1. Connector J1 carries data, control, and status lines for channel 1 only. This arrangement allows 801-type automatic dialers to be connected and operated through the connector panel.

1-7. For data set applications, the multiplexer provides the signals necessary to operate up to sixteen 103- and/or 202-type data sets. The 103-type data sets, including the 103A, E, F, G, and 113A are full duplex, 300 baud asynchronous modems (modulator/demodulators). The 202-type data sets, including the 202C, D, and E, are half duplex, 1200 baud asynchronous modems with optional reverse channels. A HP 12920A Multiplexer operates up to sixteen 103-type data sets and/or terminals. Any combination of data sets and terminals can be connected and operated simultaneously. With the optional HP 12920A-001 Multiplexer added, 202-type data sets can also be connected and operated.

Table 1-1. Asynchronous Multiplexer Interface Kit Contents

DESCRIPTION	COMMON NAME	PART NUMBER
Asynchronous Multiplexer Data PCA, Upper Select Code	Upper Data PCA	12921-60001
Asynchronous Multiplexer Data PCA, Lower Select Code	Lower Data PCA	12921-60002
Asynchronous Multiplexer Data Cable Assembly	Data Cable	12921-60003
*Asynchronous Multiplexer Control PCA	Control PCA	12922-60001
*Asynchronous Multiplexer Control Cable Assembly	Control Cable	12922-60003
Asynchronous Multiplexer Connector Panel	Connector Panel	30062-60002
Asynchronous Multiplexer Test Cable Assembly	Test Cable	30062-60003
*Indicates items contained in optional HP 12920A-001 Multiplexer Kit.		
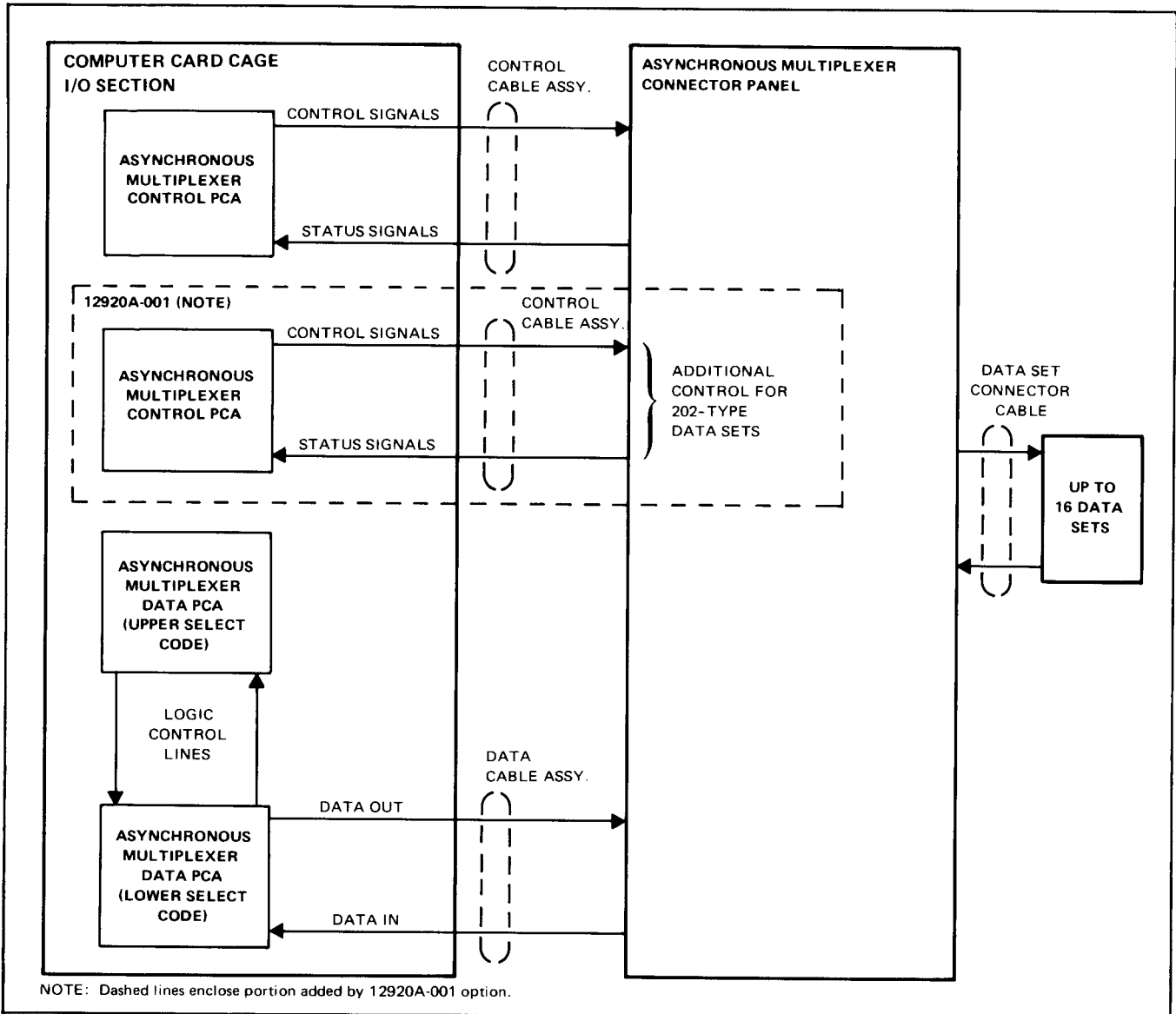
Figure 1-2. Interface Kit Block Diagram

1-8.   The multiplexer provides the signals necessary to operate up to eight 801-type automatic dialers. Since the automatic dialers require more control lines than are provided with one channel, two channels are used. An automatic dialer is connected to an even numbered connector on the multiplexer connector panel; the dialer uses both the corresponding even numbered channel and the next higher odd numbered channel.

1-9.   IDENTIFICATION.

1-10.   This manual is identified on the title page by interface kit designation and nomenclature, printed-circuit assembly part numbers and series numbers, and publication date. Refer to the information presented in the following

paragraphs and ensure that this manual applies to the equipment being serviced.

1-11.   Hewlett-Packard uses five digits and a letter (00000A) for standard interface kit designations. Options to an interface kit are identified by a three digit suffix following the model designations (00000A-000). If the designation and the option suffix of your kit do not agree with those on the title page of this manual, there are differences between your kit and the kit described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-12.   Printed-circuit assemblies are identified by a letter, a series number, and a division code stamped on the card (e.g., A-1135-22). The letter identifies the version of the

etched trace pattern on the unloaded board. The series number (middle digits) refers to the electrical characteristics and component locations of the loaded assembly. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the card. If the series numbers stamped on the printed-circuit assemblies do not agree with the series numbers shown on the title page of this manual, there are differences between your PCA and the PCA's described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-13. SPECIFICATIONS.

1-14. Specifications for the multiplexers are given in table 1-2. Current requirements listed in the table are for operation of one interface PCA of each type used. When the optional HP 12920A-001 Multiplexer is added, the current requirements for an additional control PCA, part number 12922-60001, must be added to the totals. Also, current may be drawn from the +12-volt and –12-volt power supplies through the 16 data set connectors. Current drawn through the data set connectors must be limited to 50 milliamperes per power supply and the amount added to the totals in table 1-2.

1-15. For installation, the HP 12920A Multiplexer requires three input/output (I/O) slots (select codes) in the computer and space to mount the connector panel at the rear of the cabinet. I/O slots for the upper and lower data assemblies must be side-by-side. The control PCA does not have to be adjacent. However, if the multiplexer is used with DMA in the 2114, 2115, or 2116 computers, the cards must be installed in the computer card cage and not in the 2151A or 2150B extender because DMA is not available in the extender. The optional HP 12920A-001 Multiplexer requires one additional control PCA slot.

Table 1-2. Multiplexer Specifications

PARAMETERS	REQUIREMENTS			
	Lower Data PCA (Part No. 12921-60002) Amperes	Upper Data PCA (Part No. 12921-60001) Amperes	Control PCA (Part No. 12922-60001) Amperes	Total (Paragraph 1-13)
CURRENT REQUIRED FROM COMPUTER:				
+12 Volt Supply	0.085	0.0	0.156	0.241
-12 Volt Supply	0.120	0.121	0.236	0.477
+4.5 Volt Supply	2.04	2.05	1.44	5.53
-2 Volt Supply	0.125	0.031	0.102	0.258

LOGIC VOLTAGE LEVELS: Between Interface PCA and Computer:	
Logic 1 (High): Logic 0 (Low):	+2.4V dc (minimum) +0.4V dc (maximum)
At Data Set Connectors: Command and Status Lines:	
Logic 1 (High): Logic 0 (Low):	more positive than +3V (ON) more negative than -3V (OFF)⎫ ⎬ Refer to EIA ⎨ Standard ⎬ RS-232-C
Data Lines:	
Logic 1 (Low): Logic 0 (High):	more negative than -3V (MARK) more positive than +3V (SPACE)⎭
BIT TRANSFER RATE (BAUD):	57 to 2400 bits per second (programmable).
CHARACTER LENGTH:	5 to 12 bits per character (programmable). Character size is the total number of bits (start plus data plus stop bits).
MODE OF COMMUNICATION:	Asynchronous bit-serial.
INTERRUPT TRIGGER:	Leading, trailing, or both edges of the status line signal (programmable).
DATA LINES:	Two data lines to each of 16 channels.
Data In: Data Out:	Received data (BB) Transmitted data (BA)
CONTROL LINES:	Two control lines from each control PCA for each of 16 channels.
Command 1 (C1) Command 2 (C2)	Data Terminal Ready (CD) ⎫ First Control Request to Send (CA) ⎬ PCA
Command 1 (C1) Command 2 (C2)	Supervisory Transmit (SA) ⎫ Second Control Data Signal Rate Selector (CH/CI) ⎬ PCA
STATUS LINES:	Two status lines from each control PCA for each of 16 channels.
Status 1 (S1) Status 2 (S2)	Data Set Ready (CC) ⎫ First Control Received Line Signal Detector (CF) ⎬ PCA
Status 1 (S1) Status 2 (S2)	Supervisory Receive (SB) ⎫ Second Control Clear to Send (CB) ⎬ PCA
NUMBER OF CHANNELS: (paragraph 1-6)	16 channels for transmit and 16 channels for receive with external data sets or terminals. 5 channels for receive-only are internal to interface for diagnostic purposes.

INSTALLATION   SECTION II

2-1. INTRODUCTION.

2-2. This section provides information on unpacking and inspection, installation, and reshipment for the interface kits.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the items comprising the kit for damage (cracks, broken parts, etc.). If any of the items are damaged and fail to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged items without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. Before installing a multiplexer, interconnecting cables must be supplied by the user to connect data sets or terminals to the connector panel. These interconnecting cable requirements are described in paragraph 2-8. The connector panel installation is described in paragraph 2-10, and the interface PCA and cable installation is described in paragraph 2-12.

2-7. INTERCONNECTING CABLES.

2-8. The interconnecting cables required to connect data sets or terminals to the multiplexer connector panel are determined by the number and type of data sets or terminals to be connected. Tables 2-1, 2-2 and 2-3 contain information describing the cables used to connect the multiplexer with 103- and 202-type data sets, and 801-type dialers. This same information applies to connecting other data sets and terminals except that a suitable mating connector must be selected for the terminal end of the cable. Commonly used cables in several lengths may be ordered from any HP Sales and Service Office. The following cables are available:

a. For 103- and 202-type data sets, part no. 30062-60004 (25 ft), part no. 30062-60007 (50 ft), or part no. 30062-60010 (100 ft).

b. For 801-type automatic dialers, part no. 30062-60005 (25 ft), part no. 30062-60008 (50 ft), or part no. 30062-60011 (100 ft).

c. Extender cables for increasing the length of the above cables, part no. 30062-60006 (25 ft), part no. 30062-60009 (50 ft), or part no. 30062-60012 (100 ft). Extender cables are also used for connecting directly to a data terminal device.

2-9. CONNECTOR PANEL INSTALLATION.

2-10. The connector panel is normally installed at the rear of the computer system cabinet, on the rear vertical channels, and in a position convenient for interconnections. Figures 2-1 and 2-2 show typical methods for mounting the connector panel in different types of cabinets. After mounting, connectors J0 through J15 are used for connecting the panel to data sets and/or terminals, while connectors J16 through J20 are used to connect the panel to interface PCAs in the computer.

2-11. INTERFACE PCA AND CABLE INSTALLATION.

2-12. Install the interface printed-circuit assemblies (PCAs) and cable assemblies as follows (see figure 2-3):

a. Determine if the computer power supplies will provide the additional current required for operation of the interface PCAs. Current requirements for the interface PCAs are listed in table 1-2. Refer to the Hewlett-Packard computer documentation (I/O System Operation) for instructions on how to determine the current available from the computer power supplies.

b. Turn off power at the computer and on all external devices to be connected.

CAUTION

Computer power must be off before installing the interface PCAs. Failure to turn off power may cause damage to the computer or interface PCAs.

c. Open computer for access to the I/O PCA slots.

d. Check the lower data PCA, part no. 12921-60002, to determine if jumper wire W1 is in position "A" (refer to the parts location diagram in section V of this manual). Position "B" of W1 is reserved for future applications.

Note: If programs have been prepared prior to installation, determine the appropriate card slots (select codes) from the software.

Table 2-1. Interconnecting Cable Information for 103- and 202-Type Data Sets

MULTIPLEXER PANEL CONNECTOR			DATA SET CONNECTOR		
PIN NO.	MULTIPLEXER DESIGNATION	EIA DESIGNATION		PIN NO.	EIA DESIGNATION	
2	Data In	Received Data	(BB)	3	Received Data	(BB)
3	Data Out	Transmitted Data	(BA)	2	★Transmitted Data	(BA)
4	Status 2	Signal Detector	(CF)	8	Signal Detector	(CF)
6	Command 1	Data Terminal Ready	(CD)	20	★Data Terminal Ready	(CD)
7	Common Return	Common Return	(AB)	7	Common Return	(AB)
8	Command 2	Request to Send	(CA)	4	★Request to Send	(CA)
11	Status 1*	Supervisory Receive	(SB)	12	Supervisory Receive	(SB)
12	Command 1*	Supervisory Transmit	(SA)	11	★Supervisory Transmit	(SA)
20	Status 1	Data Set Ready	(CC)	6	Data Set Ready	(CC)
22	Status 2*	Clear to Send	(CB)	5	Clear to Send	(CB)
23	Command 2*	Frequency Select	(CH)	23	★Frequency Select	(CH)

NOTES: 1. One cable required for each input/output channel.
2. The asterisk indicates signals required for 202-type data sets connected to the second (optional) control card only.
3. ★ Indicates signals from multiplexer to data set. Others are from data set to multiplexer.

Table 2-2. Interconnecting Cable Information for 801-Type Automatic Calling Unit

MULTIPLEXER PANEL CONNECTOR			801-TYPE ACU CONNECTOR		
PIN NO.	MULTIPLEXER DESIGNATION	EIA DESIGNATION		PIN NO.	EIA DESIGNATION	
4	Status 2	Abandon Call and Retry (ACR)		3	Abandon Call and Retry	(ACR)
6	Command 1	Digit Lead	(NB1)	14	Digit Lead	(NB1)
7	Common Return	Signal Ground	(SGD)	7	Signal Ground	(SGD)
8	Command 2	Digit Lead	(NB2)	15	Digit Lead	(NB2)
11	Status 1*	Data Line Occupied	(DLO)	22	Data Line Occupied	(DLO)
12	Command 1*	Digit Lead	(NB4)	16	Digit Lead	(NB4)
14	Status 1**	Power Indication	(PWI)	6	Power Indication	(PWI)
15	Command 2**	Call Request	(CRQ)	4	Call Request	(CRQ)
16	Command 1*,**	Digit Present	(DPR)	2	Digit Present	(DPR)
20	Status 1	Present Next Digit	(PND)	5	Present Next Digit	(PND)
22	Status 2*	Data Set Status	(DSS)	13	Data Set Status	(DSS)
23	Command 2*	Digit Lead	(NB8)	17	Digit Lead	(NB8)

NOTES: 1. Single asterisk indicates signals associated with the second (optional) control card.
2. Double asterisk indicates signals connected to the next higher channel.

Table 2-3. Extender Cable Information

MULTIPLEXER PANEL CONNECTOR			DATA TERMINAL CONNECTOR		
PIN NO.	MULTIPLEXER DESIGNATION	EIA DESIGNATION	PIN NO.	EIA DESIGNATION	
1	[Not Used]		1	Protective Ground	(AA)
2	Data In	Received Data (BB)	2	Transmitted Data	(BA)
3	Data Out	Transmitted Data (BA)	3	Received Data	(BB)
4	Status 2	Signal Detector (CF)	4	Request to Send	(CA)
5	Status 2	Signal Detector (CF)	5	Clear to Send	(CB)
6	Command 1	Data Terminal Ready (CD)	6	Data Set Ready	(CC)
7	Common Return	Signal Ground (AB)	7	Signal Ground	(AB)
8	Command 2	Request to Send (CA)	8	Signal Detector	(CF)
9	+12 Volts		9	Not Used	
10			10	Not Used	
11	Status 1*	Supervisory Receive (SB)	11	Supervisory Transmit	(SA)
12	Command 1*	Supervisory Transmit (SA)	12	Supervisory Receive	(SB)
13			13	Not Used	
14			14	Not Used	
15			15	Not Used	
16			16	Not Used	
17	–12 Volts		17	Not Used	
18			18	Not Used	
19			19	Not Used	
20	Status 1	Data Set Ready (CC)	20	Data Terminal Ready	(CD)
21			21	Not Used	
22	Status 2*	Clear to Send (CB)	22	Ring Indicator	(CE)
23	Command 2*	Frequency Select (CH)	23	Frequency Select	(CI)
24			24	Not Used	
25			25	Not Used	

NOTES: 1. This table applies to extender cables used to connect a data terminal to a multiplexer. When used to connect a data terminal to a modem, EIA designations are the same at both connectors.
2. The asterisk indicates signals connected to the second (optional) control card.

e. Install interface PCAs as required in the computer I/O slots as follows:

(1) Plug the lower data PCA, part no. 12921-60002, and the upper data PCA, part no. 12921-60001 into adjacent card slots. The lower data PCA must be installed in the higher numbered slot (lower select code).

(2) Plug a control PCA into a slot (not necessarily adjacent to the data PCA). If a second control PCA is used, it may be plugged into any slot and does not require a position near the first control PCA or data PCAs.

(3) Make certain that all higher priority slots have either another I/O PCA or a priority PCA installed.

Note: If the interface kit is used in conjunction with DMA in the 2114, 2115, or 2116 computer, the interface PCAs must be installed in the computer, not in the 2151A or 2150B extender.

(4) Perform the diagnostic tests described in section V of this manual to verify operation of the interface kit.

f. Pass the double-hooded connector end of the data cable through the opening at the rear of the computer. Slide the connector onto the upper and lower data PCAs so that the cable extends from the lower data PCA side of the connector.

g. Pass the hooded connector end of the control cable through the opening at the rear of the computer and slide the connector onto the control PCA.

Note: Perform step h if two control PCAs are installed.

h. Mark the two connectors on the connector panel end of the second control cable so that they are identified as coming from the second control PCA. Install the cable as described in step g.

i. Close computer and carefully route cables to connector panel.

j. Connect the cable assemblies to the connector panel as follows:

(1) Connect data cable to connector J18.

(2) Connect control cable connectors P1 and P2 to connectors J16 and J20 respectively. If a second control cable is used, its connectors P1 and P2 must be connected to connectors J17 and J19 respectively.

k. Connect interconnecting cables (refer to paragraph 2-8) between connector panel and data sets or terminals.

2-13. RESHIPMENT.

2-14. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-15. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-16. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corporation, Hawthorne, New Jersey, and place in a 200-pound-test corrugated carton. Seal the shipping carton securely and mark it "FRAGILE" to assure careful handling.

Note: In any correspondence, identify the kit by interface kit number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.
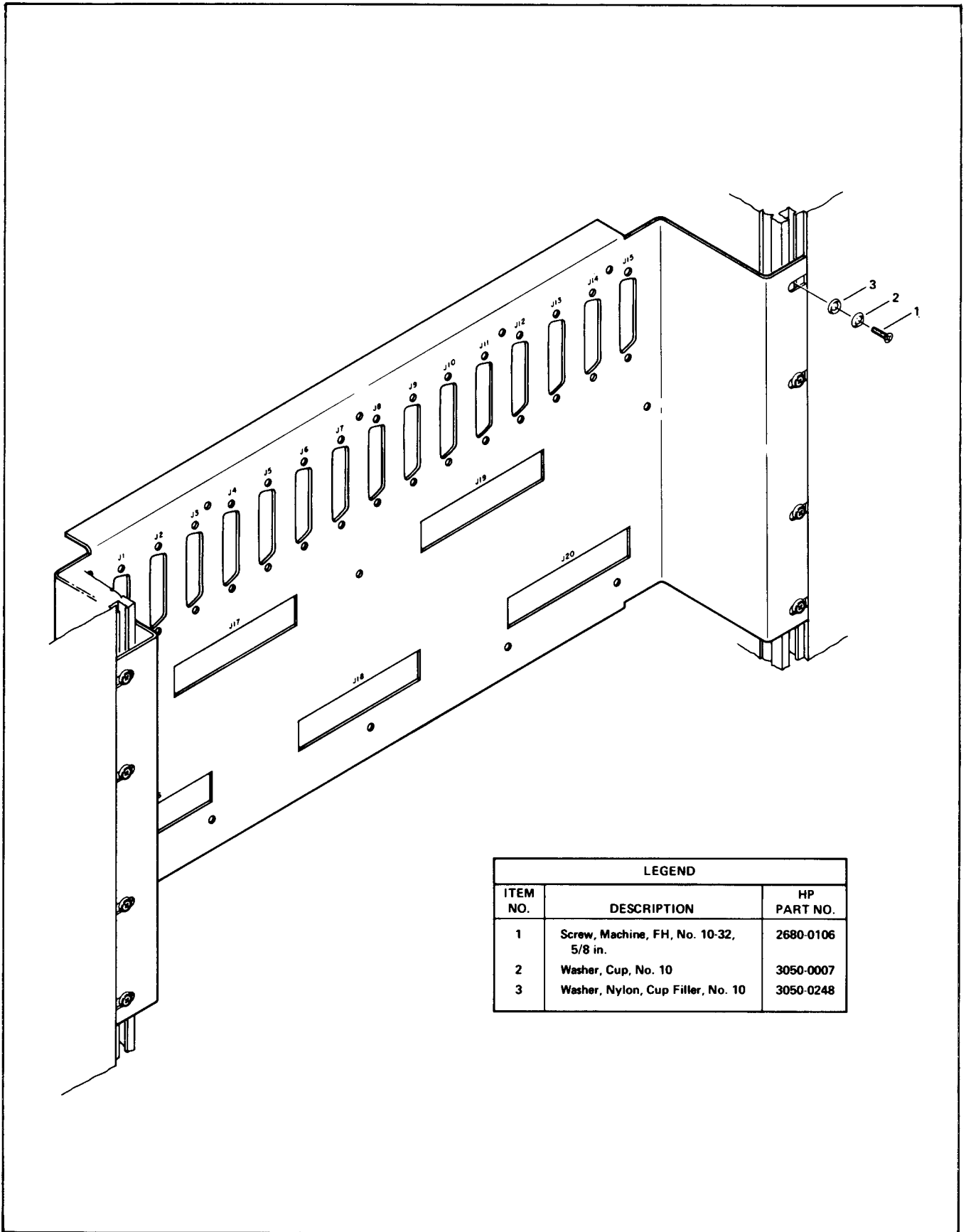
LEGEND		
ITEM NO.	DESCRIPTION	HP PART NO.
1	Screw, Machine, FH, No. 10-32, 5/8 in.	2680-0106
2	Washer, Cup, No. 10	3050-0007
3	Washer, Nylon, Cup Filler, No. 10	3050-0248

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Figure 2-1. Connector Panel Mounting, Standard
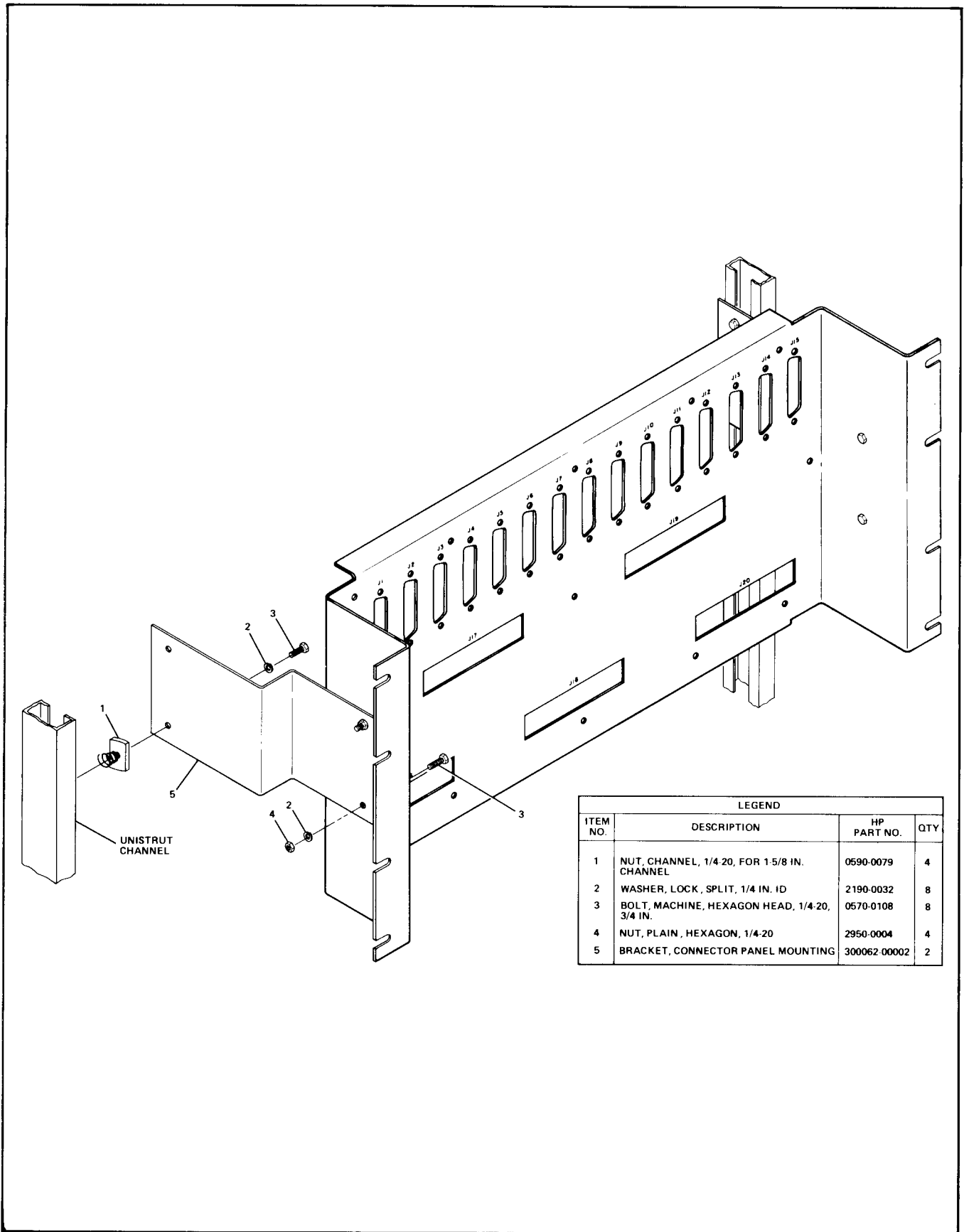
ITEM NO.	DESCRIPTION	HP PART NO.	QTY
1	NUT, CHANNEL, 1/4-20, FOR 1-5/8 IN. CHANNEL	0590-0079	4
2	WASHER, LOCK, SPLIT, 1/4 IN. ID	2190-0032	8
3	BOLT, MACHINE, HEXAGON HEAD, 1/4-20, 3/4 IN.	0570-0108	8
4	NUT, PLAIN, HEXAGON, 1/4-20	2950-0004	4
5	BRACKET, CONNECTOR PANEL MOUNTING	300062-00002	2

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Figure 2-2. Connector Panel Mounting Using Special Brackets
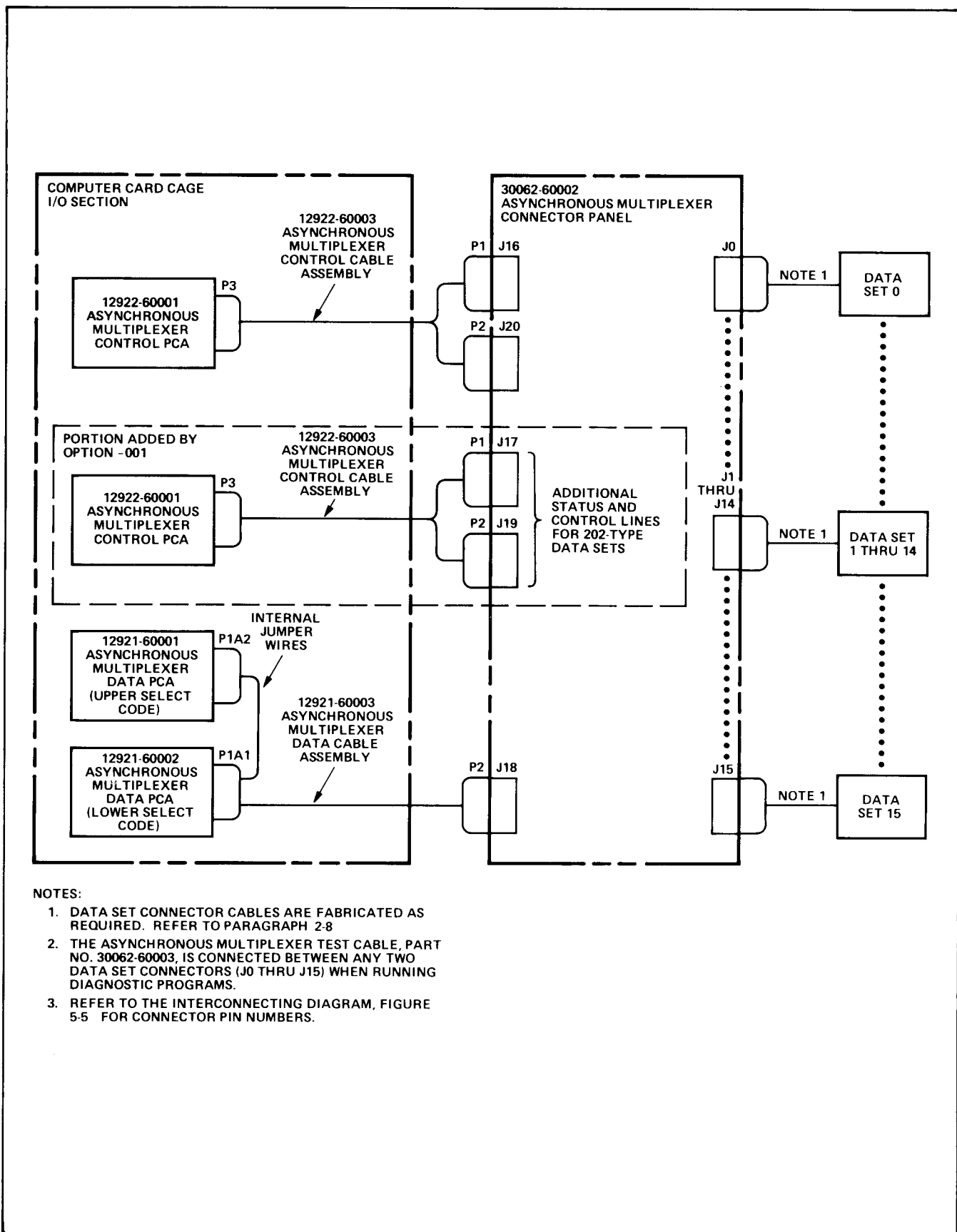
NOTES:

1. DATA SET CONNECTOR CABLES ARE FABRICATED AS REQUIRED. REFER TO PARAGRAPH 2-8

2. THE ASYNCHRONOUS MULTIPLEXER TEST CABLE, PART NO. 30062-60003, IS CONNECTED BETWEEN ANY TWO DATA SET CONNECTORS (J0 THRU J15) WHEN RUNNING DIAGNOSTIC PROGRAMS.

3. REFER TO THE INTERCONNECTING DIAGRAM, FIGURE 5-5 FOR CONNECTOR PIN NUMBERS.

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Figure 2-3. Multiplexer Simplified Connection Diagram

3-1. INTRODUCTION.

3-2.   This section provides general programming and other information necessary for operation of the asynchronous multiplexer. The multiplexer contains two programmable interfaces; the data interface and the control interface. The data interface consists of two interface printed-circuit assemblies (PCAs) with sequential select codes, while the control interface consists of one or two interface PCAs with one select code per PCA. Control PCA select codes are not necessarily sequential to the data PCA or to a second control PCA.

3-3. DATA PROGRAMMING TECHNIQUE.

3-4.   Table 3-1 shows the word formats and how they are configured for programming the data interface. The terms, parameters, and status bits shown in the word formats are defined in the following paragraphs. A sample program is given in table 3-4 to show how the data interface is used.

3-5.   DEFINITION OF TERMS.

3-6.   The following terms, parameters, and status bit definitions are presented in alphabetical order to provide ease in locating a desired definition. Locations of the parameter and status bits in the word formats are shown in table 3-1.

3-7.   BAUD RATE. Baud rate refers to the speed of character transfer and is programmable on the data interface from 57 to 2400 bits per second. The baud rate parameter is given by the following formula:

Parameter = (14,400/baud rate) - 1

For example, for a 2400 baud CRT:

Parameter = (14,400/2400) - 1 = 5

For a 110 baud teletype,

Parameter = (14,400/110) - 1 $\cong$ 130.

The baud rate parameter is programmed in octal so the parameter 130 is programmed as octal 202. Refer to table 3-2 for some commonly used baud rate parameters.

3-8.   BREAK. Break is a status bit that is set (logic 1) if the incoming data line remains a logic 0 for the duration of transmission or reception of a character, i.e., one continuous space. This character is generated in most terminals by a manual key. The data interface interprets this as a

normal character but sets the break status bit if a mark (logic 1) is not detected during the character transfer. One character interrupt is generated and the data interface will not receive another character until the line goes back to mark. If the interface kit is echoing bits to the I/O device, one character duration of spaces will be echoed; the transmit data line will then return to a mark. This prevents the teletype printer from jumping while the break key is depressed, and prevents the terminal data set from disconnecting due to reception of a long space. Figure 3-1 illustrates multiplexer break reception with echo on.

3-9.   CHANNEL NUMBER. The data interface has 20 programmable channels. Channels 0 through 15 can be connected through the connector panel to external data sets or terminals. Channels 16 through 20 are auxiliary channels contained on the data interface and are used for diagnostic purposes. All communication between the data interface and computer memory is addressed by the channel number to designate which channel is transferring a character. The channel number bits are 10 through 14 because this positions the channel number above the data in the input data word. An OTA with the upper select code is used to load the channel number in the data interface channel number register. This register is not changed until another output is programmed. Bits 0 through 9 and 15 of the channel number output word are not used.

3-10.   CHARACTER LENGTH. Character length refers to the number of bits contained in a character. This length is programmable on the data interface from 5 to 12 bits. For programming, the character length parameter is contained in bits 8 through 10. These three bits are the least significant bits of the binary number which indicates the number of bits, including stop bits, contained in a character. For example, a teletype transmits 8 data bits and 2 stop bits per character. The character length parameter is 010 which is a binary 1010 with the most significant bit removed. For a device with 7 bits of data and 1 stop bit, the character size parameter is 000 which is a binary 1000 with the most significant bit removed. Table 3-3 lists typical character sizes and character size parameters.

3-11.   CHARACTER LOST. Character lost is a status bit that is set (logic 1) if the data interface receives two or more characters without generating an interrupt. Each channel has a one-character buffer that allows the computer at least one complete character time for interrupt processing. When two characters are received without being serviced, the first character received is lost and the character lost status bit is set.

3-12.   CLC SC COMMAND. A CLC command with the data interface select code clears the Control FF and thus disarms interrupts from the interface. It does not reset the

Table 3-1. Data Interface Programming
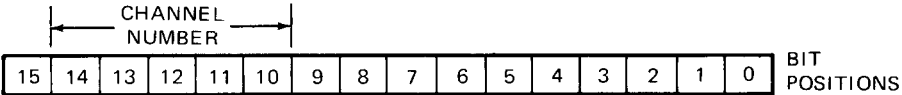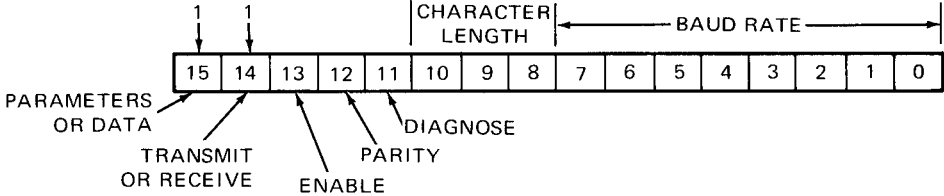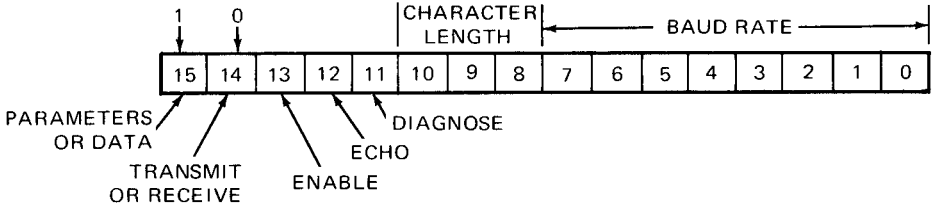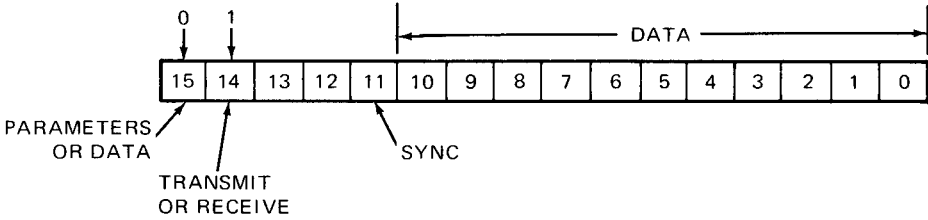
OPERATION MNEMONIC	DESCRIPTION AND WORD FORMAT
OTA (Upper Select Code)	**COMMANDS** Note: All communication between the data interface and computer memory must contain a channel number to designate which of 16 devices is making an input or output transfer. Output channel number to interface.
CLF (Lower Select Code)	Acknowledge interrupt. (Data interface provides an interrupt per character and must be primed with parameters before channel will transmit or receive.)
STC (Lower Select Code)	Initiate output of parameters or data to the data interface.
OTA (Lower Select Code)	**INFORMATION OUTPUT** Output parameters for transmit to channel.
OTA (Lower Select Code)	Output parameters for receive from channel.
OTA (Lower Select Code)	Output data to a transmit channel.

Table 3-1. Data Interface Programming (Continued)

OPERATION MNEMONIC	DESCRIPTION AND WORD FORMAT

OTA (Lower Select Code)	**INFORMATION OUTPUT (Continued)**
	
	Output data to a receive channel.
	Illegal. May alter received data.
	
	`0    0`
	`15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0`
	PARAMETERS OR DATA
	TRANSMIT OR RECEIVE

LIA (Lower Select Code) LIA (Upper Select Code)	**RECEIVE DATA AND STATUS** Receive data from channel. PARITY CHECK — CHANNEL NUMBER — DATA `15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0` Receive status from channel. SEEKING — CHANNEL NUMBER — DIAGNOSE — CHARACTER LOST `15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0` BREAK — SEND/RECEIVE

interface to its initial conditions but leaves all control words and data intact.

3-13.   CLC 0 COMMAND. A CLC command with a select code of zero clears the Control FF and may alter parameters and data in the interface. To correctly simulate preset, at least 100 milliseconds of CLC 0's must be programmed. This sets the interface to its initial conditions, i.e., all output lines in mark condition, no interrupts pending, all send and receive channels disabled, and echo off.

3-14.   CLF COMMAND. The CLF command is used to acknowledge interrupt to the data interface and must be executed in every device service program. This command prepares the data interface for the next interrupt. Until the CLF command is executed, data and status can be loaded repeatedly by LIA commands without the input information changing. After the CLF command is executed, another channel may interrupt and change the input registers.

3-15.   DATA. To output data, the data must be right justified and packed to the left, through bit 10, with trailing "ones". For an eight bit character, the data bits are bits 0 through 7 and bits 8, 9, and 10 are each logic 1. When the output command (OTA with lower select code followed by the STC command) is executed, the data interface clocks out the number of bits specified when the parameters were output. The output of data and parameters is identical except for bit 15 of the output word. Bit 15 is a logic 0 when data is output and a logic 1 when parameters are output. The channel number may be output before or after the data as long as both are output prior to the STC command. Data and status are input by LIA commands and no special procedures are required.

3-16.   DIAGNOSE. The diagnose bit, when set (logic 1), creates a data path between a main channel, one of the 16 send or 16 receive channels going to the device, and the five receive-only channels. For a send channel, this allows output of data on a main channel and reception on the

Table 3-2. Parameters for Common Devices

DEVICE	BAUD RATE PARAMETER (OCTAL)
OUTPUT	
TTY ASR 33 (11 bit format, ASCII) (110 baud)	161202
IBM 2741 Selectric (9 bit format, PTTC/BCD) (134.5 baud)	160157
30 cps terminal (10 bit format)	160457
60 cps terminal	160427
120 cps terminal	160413
240 cps terminal	160405
150 baud Baudot code terminal	163537
TTY with parity (110 baud)	171202
TTY with diagnose (data is routed to auxiliary channels)	165202
INPUT	
TTY ASR 33 (with echo) (110 baud)	131202
IBM 2741 Selectric (134.5 baud)	120157
30 cps terminal (with echo)	130457
60 cps terminal (without echo)	120427
120 cps terminal	120413
240 cps terminal	120405
TTY with diagnose (input data routed to auxiliary channels) (110 baud)	135202
150 baud terminal (Baudot code)	133537
STOP BIT FORMATS (to be inclusive or'd with the character before output)	
TTY (ASCII) (without parity or with odd parity)	43600
TTY with even parity	43400
Selectric	43600
Baudot code	43740
Time delay character on channel configured without parity	47777
Time delay character on channel configured with parity	47577

extra channel, an attribute useful for on-line diagnostics or monitoring of output. For a receive channel, this routes input data to the extra channels so that data can be received at six speeds simultaneously. This aids in selecting device type and device speed algorithms. Figure 3-2 shows diagnose parameters.

3-17. ECHO. Echo is a receive parameter and when the bit is set (logic 1) it enables the received data bits to be echoed back to the device bit-by-bit. When the data interface is transmitting data, the echo bit on the corresponding receive channel must be turned off (logic 0) to avoid interference between transmitted data and echoed data.

3-18. ENABLE. The data interface interrupt system allows each channel to request an interrupt. When the channel enable bit is turned off (logic 0), the channel can transmit and receive characters but will not interrupt the computer. With the enable bit set (logic 1) the channel can request an interrupt.

3-19. INTERRUPT. The data interface interrupts the computer when each character is received or on completing the transmission of each character. Interrupts are held off until a CLF command is programmed. There is no priority scheme between channels. When a CLF is programmed, the first channel with its internal buffer flag bit set will be

Table 3-3. Typical Character Lengths and Parameters

DEVICE	CHARACTER LENGTH	CHARACTER LENGTH PARAMETER (OCTAL)
HP 2749 Teleprinter	11 bits = 1 start, 7 data, 1 parity, 2 stops.	010
IBM 2741	9 bits = 1 start, 6 data, 1 parity, 1 stop.	000
HP 2605, HP 2761, HP 2600	10 bits = 1 start, 7 data, 1 parity, 1 stop.	001
Baudot code	7½ bits = 1 start, 5 data, 1½ stop (send 2; receive 1).	111 send 110 receive
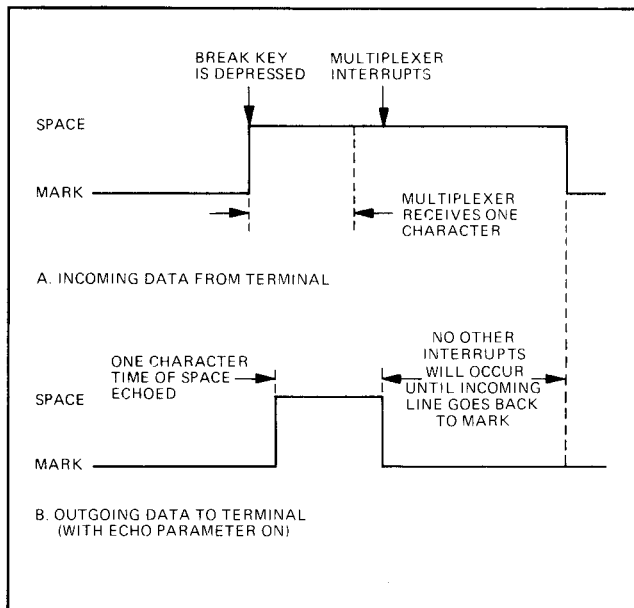
2176-23

Figure 3-1. Break Reception with Echo On

serviced. The interrupt system should be turned off during outputs to avoid the possibility of an interrupt between the parameter and data outputs.

3-20. LIA COMMAND. Input of data and status is by LIA commands. Data is input with the lower select code and status is input with the upper select code. Following the last LIA command, a CLF command is executed to indicate that the data interface input registers are ready to be loaded by the next interrupting channel.

3-21. OTA COMMAND. The OTA command is used with the upper select code to output channel numbers to the channel number register and with the lower select code to output parameters and data to the data interface buffer register. Formats for these output words are shown in table 3-1.

3-22. PARAMETERS. The output of parameters and data is identical except for bit 15 of the output word. Bit 15 is set (logic 1) to output parameters and is turned off (logic 0) to output data.
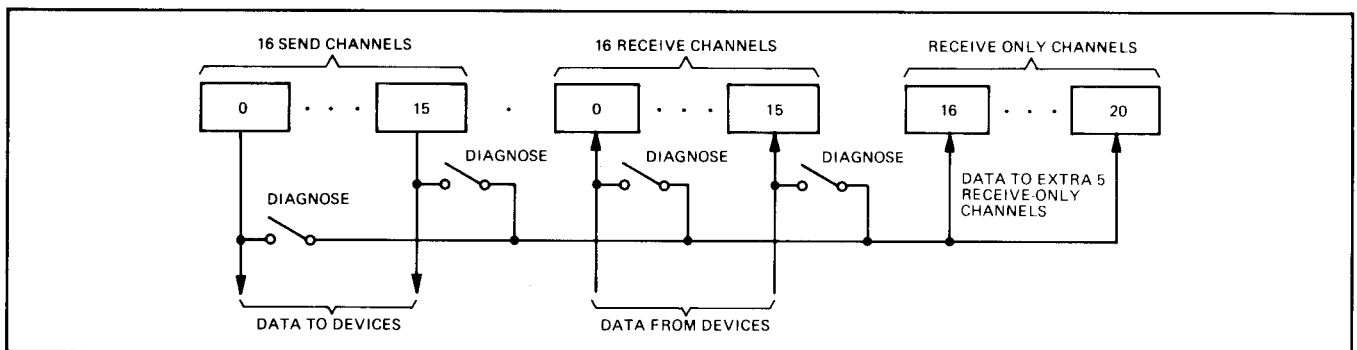
2176-24

Figure 3-2. Diagnose Parameters

3-23. PARITY. There is a parity bit in the received data word and also in the output parameter word. In either case the parity bit is set (logic 1) for odd parity and is turned off (logic 0) for even parity. To determine the parity parameter, ASCII parity is computed on bits 0 through 7 of the data word. The modulo two sum of bits 0 through 7 is the parity check bit. A parity bit in the parameter word does not effect the parity check bit in the input word. Parity is not generated for character sizes other than 8-bit ASCII.

3-24. RECEIVE. Bit 14 in the parameter word is the transmit or receive bit. When the bit is set (logic 1), the data word will be transmitted to a channel. To receive data, bit 14 of the parameter word is turned off (logic 0). Turning off bits 14 and 15 of the parameter word is illegal and may alter received data.

3-25. SEEKING. Seeking is a status bit on the input status word. This bit is set (logic 1) for an average of 35 microseconds and a maximum of 70 microseconds after each STC command. When the bit is set, a previously output character is seeking for a location in the data interface circulating register. New data must not be output until the bit is turned off (logic 0). If a nonexistent channel number was previously output, the logic will continue indefinately to seek for a memory field to put the data into. Therefore, care must be used to prevent sending data or parameters to nonexistent channels.

3-26. SEND/RECEIVE. Send/Receive is a status bit on the input status word. If the bit is set (logic 1) it indicates an interrupt was generated by completing a character transmission. When the bit is turned off (logic 0) it indicates an interrupt was generated by a received character.

3-27. STC COMMAND. An STC command with the lower select code initiates the output of parameters or data to the data interface. The data interface contains a 16-bit buffer register that is loaded by an OTA command with the lower select code. Each channel on the data interface also has a memory. These channel memories are 56-bits each and circulate data in a continuous, repeating cycle through the quad 256-bit shift registers (main memories) on the upper select code PCA. When the STC command is given with the lower select code, the data interface seeks the programmed channel and transfers the data from the 16-bit buffer register to the channel memory. If the buffer register contained parameters, the channel is configured with the parameters. If the buffer register contained data, the command starts transmission of the data.

3-28. STOP BITS. Stop bits are added by the program to each character before it is output. For an example, refer to table 3-2.

3-29. SYNC. The sync bit is transmitted with a data word and is used to synchronize operations of the terminals with the data interface. If the bit is set (logic 1), the character start bit is replaced by a mark. Output of 47777 for a transmit channel configured without parity or output

of 47577 for a transmit channel configured with parity generates a one character delay. Either output can be repeated as required to allow time for carriage returns, line feeds, or other terminal operations. Since only marks (the normal line-idle condition) are sent, the transmission of this delay character will not affect the distant terminal.

3-30. TRANSMIT. Bit 14 in the parameter word is a transmit or receive bit. The bit must be set (logic 1) to transmit data.

3-31. SAMPLE PROGRAM.

3-32. Table 3-4 shows a sample program for the data interface that demonstrates the programming of stop bits and checking of the seeking bit.

3-33. CONTROL PROGRAMMING TECHNIQUE.

3-34. Table 3-5 shows the word formats and how they are configured for programming the control interface. The terms and status bits shown in the word formats are defined in the following paragraphs. A sample program is given in table 3-8 to show how the control interface is used. Figure 3-3 is a schematic illustration of the control board logic. Some typical programming commands are shown in table 3-6.

3-35. DEFINITION OF TERMS.

3-36. The following terms and status bit definitions are presented in alphabetical order to provide ease in locating a desired definition. Locations of the status bits in the word formats are shown in table 3-5.

3-37. C1, C2. C1 and C2 are command bits and are set (logic 1) to turn on their associated command line. For the first control PCA used, the command line for C1 is Data Terminal Ready (CD) and for C2 is Request to Send (CA). For the second control PCA used, the command line for C1 is Supervisory Transmit (SA) and for C2 is Frequency Select (CH). Refer to table 3-7.

3-38. CHANNEL NUMBER. The channel number is four bits (10 through 13) of every output or input word. This number is an address that indicates which of the 16 input/output channels is being serviced. If the scan bit is set (logic 1) during an OTA/B command, the channel number in memory is continuously sequenced while the comparison logic checks the input status lines for cause to interrupt. When the scan bit is cleared (logic 0) during an OTA/B command, the channel number does not change and the status of the same channel is loaded by the next LIA/B command. After each LIA/B command the channel number in memory is incremented by one.

3-39. EC1, EC2. Bits EC1 and EC2 are enable command bits. If EC1 and/or EC2 are set (logic 1) when the update bit is set (logic 1) then the inputs to command bits (C1 and C2 respectively) are enabled.

Table 3-4. Sample Program for Data Interface

LABEL	OPERATION	COMMENTS
	CLF SC	Clear flag set by power on
	LDA CWS	Output send
	JSB OUT	Channel parameters
LOOP	LDA CHAR	Get ASCII character to be output
	IOR STOP	Include the stop bits
	JSB OUT	Send the character
	SFS SC	Wait for end of transmission
	JMP *−1	
	CLF SC	Acknowledge interrupt
	JMP LOOP	Repeat transmission
OUT	NOP	Subroutine to output information in A-register
	LIB SC+1	Check seeking bit
	SSB	Skip next instruction if bit 15=0
	JMP *−2	Wait until bit 15=0
	OTA SC	Output data
	LDA UNIT	Load channel number
	ALF, ALF	Rotate by 8
	RAL, RAL	Rotate by 2
	OTA SC+1	Output channel number in bits 10 thru 14
	STC SC	Initiate transmission
	JMP OUT, I	
CWS	OCT 161202	Send parameter for teletype
CHAR	OCT 101	Octal representation of ASCII character "A"
SC	EQU 13B	Select code number of 12921-60002 PCA
UNIT	OCT 2	Unit number of channel to be output to
STOP	OCT 43600	Stop bits for teletype

3-40.   ES1, ES2. Bits ES1 and ES2 are enable bits for comparison logic. The bits are stored in random-access-memory and enable the comparison logic when set (logic 1). If an enable bit is set when the comparison logic detects a difference between an input status bit (S1, S2) and a stored status bit (SS1, SS2), scanning is stopped and a flag bit (I1 or I2) is set.
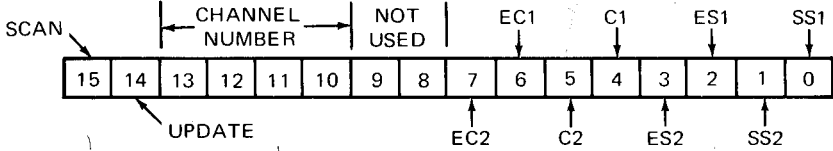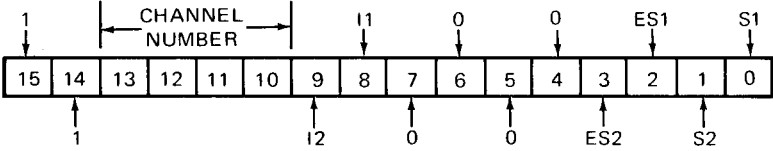
3-41.   I1, I2. Bits I1 and I2 are flag indicator bits. When a bit is set (logic 1) it indicates the comparison logic detected a difference in status that caused an interrupt. I1 corresponds to a change in S1 and I2 corresponds to a change in S2.

3-42.   LDA/B COMMAND. The LDA or LDB command loads the contents of an addressed location into computer memory (A or B register).

3-43.   LIA/B COMMAND. The LIA or LIB command with the control PCA select code is used to load the status word. When the status word is loaded following an interrupt, it contains the channel number of the channel that caused the interrupt. After the status word is loaded, the channel number is incremented by one so that subsequent LIA/B commands load status words from sequential channels. All input status words have the scan and update bits set (logic 1) so that an LIA/B command followed by an OTA/B command will input a status word and then update and output the stored status bits for the same channel.

3-44.   OTA/B COMMAND. The OTA or OTB command with the control PCA select code outputs a control word to the control PCA registers. The channel number in the control word directs the word to a particular location where it configures the channel memory.

Table 3-5. Control Interface Programming

OPERATION MNEMONIC	DESCRIPTION AND WORD FORMAT
OTA/B (Select Code)	Output control word.
STC (Select Code)	Enables computer I/O interrupt.
LIA/B (Select Code)	Receive status word.

3-45.   S1, S2. Bits S1 and S2 are input status bits selected by the channel number and indicate the states of S1 and S2 for that channel when the receive status word is input by an LIA/B command. For the first control PCA used, the status line for S1 is Data Set Ready (CC) and for S2 is Signal Detector (CF). For the second control PCA used, the status line for S1 is Supervisory Receive (SB) and for S2 is Clear to Send (CB).

3-46.   SCAN. When the scan bit is set (logic 1) by any OTA/B command, the channel number in memory is continuously stepped through each channel number. At each channel number, the comparison logic compares the input status bits with the stored status bits. If a difference is detected and the associated ES bit is set (logic 1), scanning halts and an interrupt occurs. The interrupt must be serviced before scanning can continue.

3-47.   SS1, SS2. Bits SS1 and SS2 are stored status bits that are stored in the random-access-memory to be compared with input status bits during a scan.

3-48.   STC COMMAND. The STC command with the control PCA select code enables the computer I/O interrupt.

3-49.   UPDATE. When the update bit is set (logic 1) the output latches are enabled for storing command bits C1 and C2, and the enable bits ES1 and ES2 are stored with the stored status bits SS1 and SS2 in the random-access-memory. It is necessary to output an update command so that a second interrupt does not occur from the same status bit change. An update command is output by outputting the same bit pattern that was read in. When this occurs, the control and enable bits are not changed but the stored status bits are updated to the current value.

3-50.   SAMPLE PROGRAM.

3-51.   Table 3-8 shows a sample program for the control interface that demonstrates the programming to detect changes in one status bit for one channel. Many other programming combinations are possible.
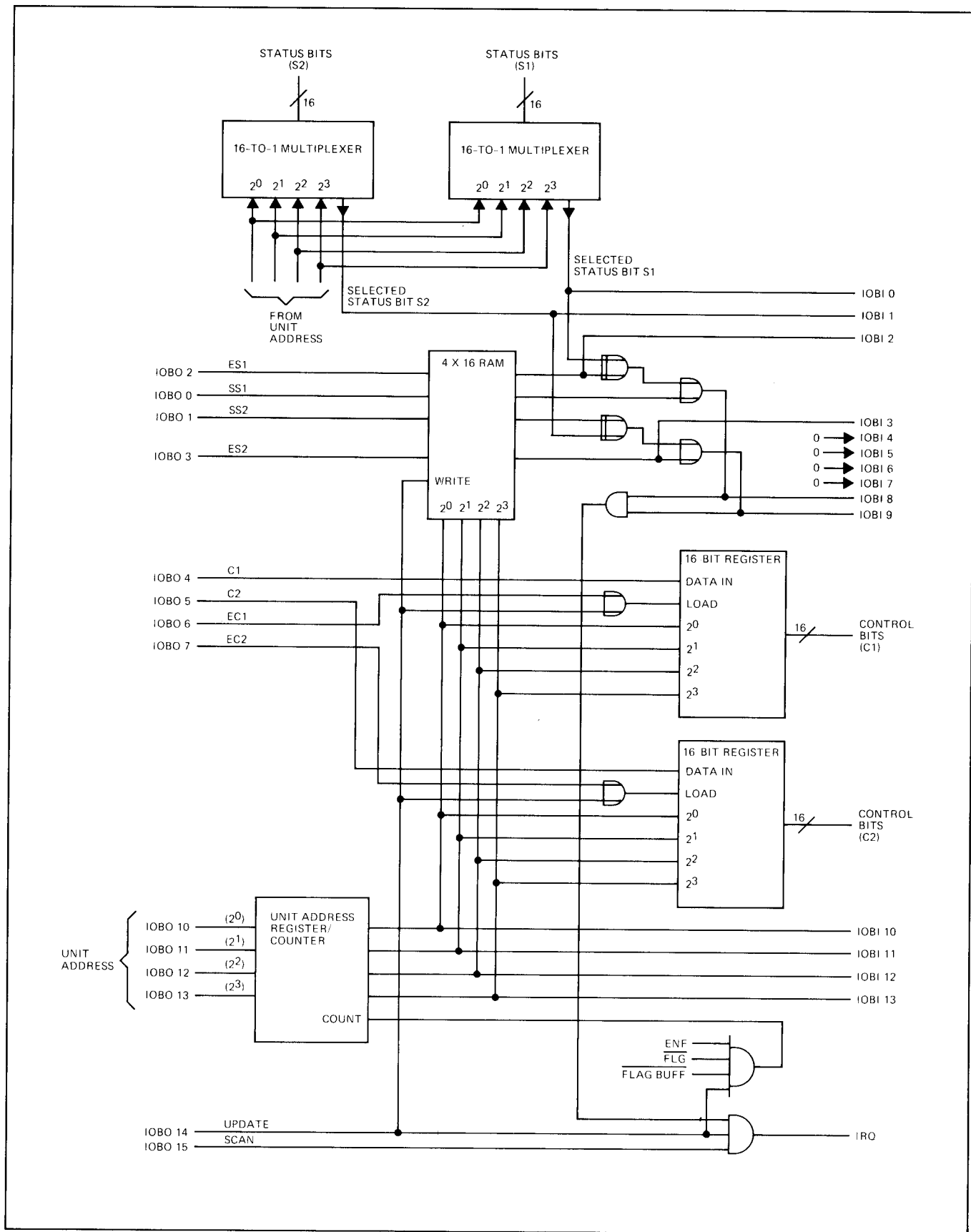
Figure 3-3. Control PCA, Simplified Schematic Diagram

Table 3-6. Typical Programming Commands Used With the Multiplexer

ACTION DESIRED	ACTION REQUIRED	EXPLANATION
Clear flags set by power on	CLF CNTL CLF MPX CLF REV	Interrupt will occur on the first STC if flags are not clear. CNTL is the select code of the control PCA. MPX is the data board. REV is the 12920-001 option control PCA.
Detect a status bit change	LDA UNIT ALF, ALF RAL, RAL IOR CWS OTA CNTL STC CNTL	UNIT is the port 0-15 of the device. CWS is the control word requesting an interrupt upon a status bit value.
Generate a 100 millisecond timeout	LDA =B161202 JSB OUT LDA =B47777 JSB OUT	Set up the channel to send all marks at teletype speed. Interrupt will occur in 100 ms.
Configure a channel	LDA CW JSB OUT	CW configures either a send or a receive channel with bit rate, character size, etc.
Send a character	LDA CHAR IOR =B43600 JSB OUT	The 7 bit character is or'd with stop bits and is sent. An interrupt occurs at the end of transmission.
Send a long space	LDA =B40000 JSB OUT	The output remains at a space until changed by another output.

Output data or parameters	OUT NOP
	    LIB MPX
	    SSB
	    JMP *−2
	    OTA MPX
	    LDA UNIT
	    ALF, ALF
	    RAL, RAL
	    OTA MPX+1
	    STC MPX
	    JMP OUT, I
		Enter with data in A.
		Check seeking bit.
		
		Output data.
		Position and output the unit number.
		
		Initiate the operation.

Acknowledge an interrupt from data transmission or reception	CLF MPX	The multiplexer will not interrupt again until it has received a Clear Flag.
Acknowledge an interrupt from status lines	CLF CNTL CLF REV	

Table 3-7. Control Interface to Data Set Signal Reference

CONTROL PCA USED	CONTROL INTERFACE SIGNAL NAME	CONNECTOR PANEL PIN NO.	103-TYPE DATA SET SIGNAL NAME	202-TYPE DATA SET SIGNAL NAME	DATA SET CONNECTOR PIN NO.
First	Command 1 (C1)	6	Data Terminal Ready (CD)	Data Terminal Ready (CD)	20
First	Command 2 (C2)	8	Request to Send (CA)	Request to Send (CA)	4
First	Status 1 (S1)	20	Data Set Ready (CC)	Data Set Ready (CC)	6
First	Status 2 (S2)	4	Signal Detector (CF)	Signal Detector (CF)	8
Second	Command 1 (C1)	12		Supervisory Transmit (SA)	11
Second	Command 2 (C2)	23	Not used for 103-type Data Sets	Frequency Select (CH)	23
Second	Status 1 (S1)	11		Supervisory Receive (SB)	12
Second	Status 2 (S2)	22		Clear to Send (CB)	5

Table 3-8. Sample Program for Control Interface

LABEL	OPERATION	OPERAND	COMMENTS
*This program commands an interrupt each time the data set ready line changes states.			
	LDA	CW3	Request for interrupt on condition
	OTA	CTL	Output control word
	STC	CTL	Enable I/O interrupt
*	. . .		Interrupt occurs
	LIA	CTL	Received status word is 164405
	OTA	CTL	Output conditions to interrupt if data set ready line is 0.
	STC	CTL,C	Enable I/O interrupt
*	. . .		Interrupt occurs
	LIA	CTL	Received status word is 164404
	OTA	CTL	Output conditions to interrupt if data set ready line is 1.
	STC	CTL,C	Enable I/O interrupt
	. . .		
CW3	OCT	164004	Scan, update, and enable status 1 to interrupt channel 10 when data set ready line is 1.
CTL	EQU	15B	Control card select code

4-1. INTRODUCTION.

4-2. This section contains a general and a detailed theory of operation for the HP 12920A and the HP 12920A-001 Asynchronous Multiplexer Interface Kits.

4-3. GENERAL THEORY OF OPERATION.

4-4. The HP 12920A Multiplexer provides 16 input/output channels for bit serial transfer of data, control, and status signals between an HP computer and an asynchronous device such as a data set, teleprinter, card reader, or a similar device. The optional HP 12920A-001 Multiplexer, added to the Hp 12920A, allows up to 16 of the 202-type data sets or up to eight 801-type automatic dialers to be connected and operated.

4-5. The multiplexer allows the computer to service any mix of asynchronous, bit-serial devices through programmed control of the data transfer (baud) rate, character format and terminal control.

4-6. The interface kit provides an interface between the fast, parallel operations of a computer and the relatively slow, serial, and somewhat random operations of mechanical input or output devices. To accomplish this the interface kit must be capable of converting data from parallel format to serial format for an output operation, of converting data from serial format to parallel format for an input operation, and of providing temporary storage of the data during both input and output operations.

4-7. A data character from an I/O device consists of a start bit, a variable number of data bits, and a stop bit. The start bit (a space) "tells" the receiving device (interface PCA or I/O device) that a character transmission has commenced. The data bits are supplied one after another, and the stop bit (a mark) signifies the end of the character.

4-8. The following paragraphs describe the circuits necessary to interface 16 full duplex, asynchronous channels. The block diagrams in figures 4-1 and 4-3, the timing diagram in figure 4-2, and the flowchart in figure 4-4 support the textual information. Figures 4-5 and 4-6 show additional timing information.

4-9. DATA INTERFACE THEORY OF OPERATION.

4-10. The data interface has two interface printed-circuit assemblies (PCAs) called the lower select code PCA and the upper select code PCA. These two assemblies share adjoining select codes. Data and parameters are output and data is input with the lower select code. Unit numbers are output and unit numbers and status are input with the upper select code. Interrupts, flags, and other control operations use only the lower select code.

4-11. The data interface provides single data otuput line and a single data input line with a common return to each of 16 channels. Communication over these lines is bit-serial with each character being made up from a timed sequence of bits, where each bit represents either a mark (logic 1) or a space (logic 0). The beginning of each character is indicated by one bit time of space (logic 0) and the end of each character is indicated by one or more bit times of mark (logic 1). Since each character can be transmitted with variable amounts of time between characters, the mode of communication is asynchronous, bit-serial.

4-12. The 16 channels connected to the data output and data input lines are full duplex so that data can be transmitted to and received from any channel simultaneously. Channels are also independently programmed with parameters such as baud rate, character length, parity, diagnose, and bit-by-bit echo. The data interface must be primed with these parameters before a channel can transmit or receive. Also, any communication with the computer must contain the channel number to indicate which device is being serviced.

4-13. All outputs of parameters or data to the interface are followed by an STC command that initiates the operation. The data interface then interrupts the computer upon reception of each character or upon completion of transmission of each character. A CLF must be issued after each interrupt to acknowledge the interrupt to the interface.

4-14. In addition to the 16 full duplex channels (designated 0 through 15), there are five auxiliary channels designated 16 through 20. These auxiliary channels are receive-only channels and are used for diagnostic purposes. A diagnose bit in the transmitted or received parameters controls access to the auxiliary channels. If the diagnose bit is set (logic 1) while transmitting, the transmitted data is looped back as input to all of the auxiliary channels. When the transmitting channel and an auxiliary channel are configured with the same baud rate and character length, data is transferred between the two channels as if they were two independent devices. Similarly, received data can be routed to the auxiliary channels. Auxiliary channels can each be configured with different parameters. Thus, data received at different speeds can be analyzed to determine the type of terminal being used.

4-15. The lower and upper select code assemblies use adjacent select codes and connect to the computer through the I/O backplane lines. There are 37 channels (16 send and 21 receive) which may be independently programmed with

baud rate, character size, parity, diagnose, and enable. The data interface PCA circuits are shown in functional block form in figure 4-1.

4-16. DATA OUTPUT.

4-17. Data and parameters are transferred from the computer to a 16-bit holding register on the upper select code PCA by executing an OTA/B instruction to the lower select code. An OTA/B instruction to the upper select code transfers the unit number to 5-bit holding register on the lower select code PCA. An STC instruction results in the information being transferred to the circulating shift registers. Information consisting of 56 bits for each of the 37 channels is transferred from the quad 256-bit shift registers (main memory) to the respective circulating register loops. When the channel corresponding to a specific unit number rotates into the circulating shift registers, the 16 bits of information are transferred from the holding registers to the circulating shift registers.

4-18. The information is captured in the main memory registers and rotated through the circulating register loop each 69.4 microseconds. The main memory (composed of shift registers) is rotated by pulses PH1 or PH2 from the oscillator circuit on the lower select code PCA. At this scanning frequency, the parallel to serial/serial to parallel operations are executed to clock data to and from the I/O devices. An illustration of the timing relationship between a single transmitted character and the circulating memory is shown in figure 4-5.

4-19. DATA INPUT.

4-20. Each bit coming from a device is scanned once every 69.4 microseconds as described in the preceding paragraphs. The circulating shift registers take a sample in the middle of each bit and retain it as part of the channel's memory field in the main memory. When a full character has been assembled it is transferred to input holding registers on the lower select code PCA. The computer may fetch the data in these registers by executing an LIA/B or MIA/B instruction.

4-21. PARALLEL TO SERIAL CONVERSION.

4-22. When the circulating register receives data output from the computer, it activates a send operation. A "mark" condition is clocked onto the transmitted data line for one bit time. This time serves as a stop bit for the preceding character. By placing a stop bit at the beginning of the character instead of at the end, it acts as a guard bit to allow the distant receiving device time to finish any preceding character reception.

4-23. The first bit to be clocked onto the transmitted data line is the synchronizing bit. This bit is normally a logic 0 or "space" and serves as a start bit. In a timed sequence, the data bits, least significant bit first, are placed on the transmitted data line. The last bit is normally a logic 1 stop bit. The channel then causes an interrupt to the computer. If parity was specified, the ASCII parity bit

position is replaced by the even parity of the eight least significant data bits before transmission. At the beginning of the transmit operation, the Break flag is set. If during the transmission the incoming data line is a "mark," the break bit clears.

4-24. SERIAL TO PARALLEL CONVERSION.

4-25. When the input line to a receive channel goes to a "space", a one-half bit timer starts in the circulating registers. If the input line goes back to a "mark" condition before the timeout, the circuit is cleared thus guarding against short noise pulses that would trigger a receive operation. The start bit and all subsequent data bits are shifted into the interface until the number of bits equals the character size parameter. At this time, the character must be right justified which takes 69.4 microseconds for each shift needed until the start bit reaches the end of the shift register. This justification takes about 70 microseconds for an 11-bit character format and 140 microseconds for a 10-bit format. This time requirement restricts operation at speeds above 2,400 bits per second.

4-26. When the entire character has been received, it is placed in a one character buffer register which rotates through the circulating register. Each channel has its own buffer register so there can be up to 16 characters in the interface awaiting service by the computer. If the buffer register for a given channel already contains a character at the completion of a reception, then this character is over-written. Then, when the interrupt from that channel occurs, the Character Lost status bit will be set, indicating that data has been destroyed in the interface process. The Break bit operation is the same during transmission or reception, being set at the beginning of the operation and being cleared when the line returns to a "mark" condition.

4-27. CLOCK SECTION.

4-28. The clock section generates all timing pulses needed to shift the quad 256-bit shift registers (main memories) and to clock the circulating registers. It consists of a 4.32 MHz crystal oscillator, timing signal generation logic, a shift counter, an address counter, and an address comparator.

4-29. A timing diagram for the signals from the clock section is shown in figure 4-2. The functions of the signals are as follows:

a. DECISION PULSE (DP). A 250-nanosecond pulse which informs the logic circuits that a new data field is in position to be operated upon.

b. LOGIC CLOCK (LC). A 100-nanosecond pulse which clocks the logic circuits.

c. PHI 1. A 150-nanosecond pulse that shifts the quad 256-bit shift registers (main memories).

d. PHI 2. A 150-nanosecond pulse that shifts the quad 256-bit shift registers (main memories).
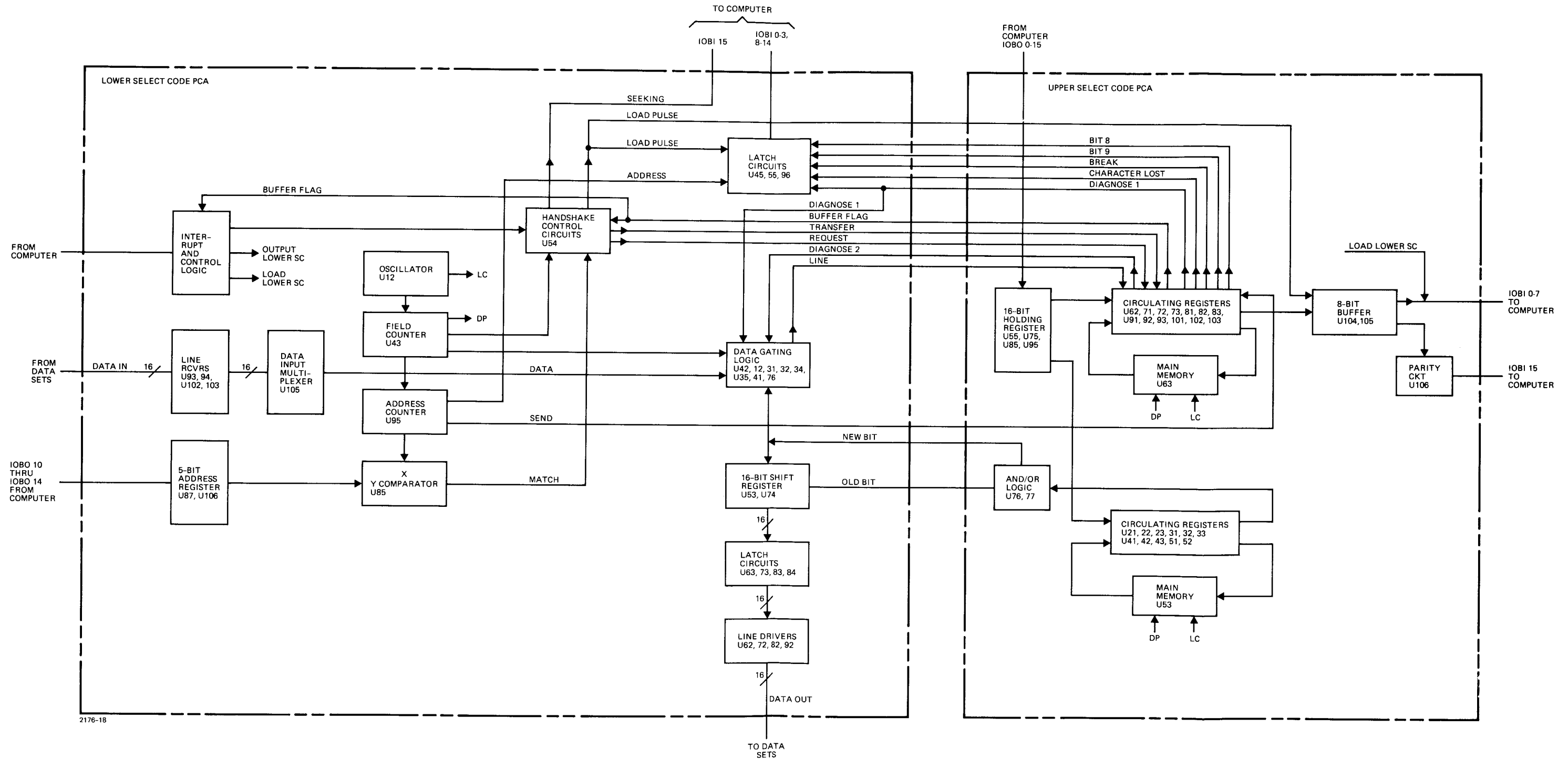
Figure 4-1. Functional Block Diagram, Asynchronous
Multiplexer Data Assemblies
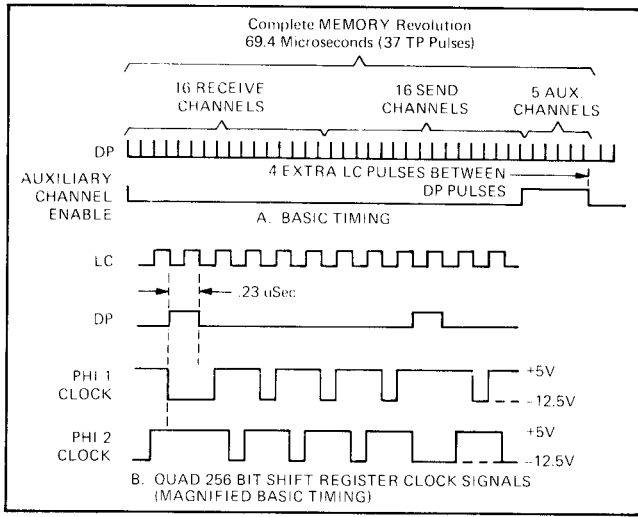
Figure 4-2. Basic Timing Diagram

crystal. Inverter U12C shapes the signal and isolates the oscillator from the pulse forming circuits that follow. With jumper W1 in position "A" the output frequency is 4.32 MHz. The 100 nanosecond one-shot, U22, provides the Logic Clock (LC) pulse. All states change on the trailing edge of this pulse.

4-31.   MAIN MEMORY CLOCKING. The main memory shift registers, U53 and U63, on the upper select code assembly are clocked by PHI 1 and PHI 2 clock signals to shift (or rotate) parameters and data through the circulating registers. The PHI 1 and PHI 2 signals are in the "1" state for 150 nanoseconds, are quiescent for 50 nanoseconds, and occur alternately as shown in figure 4-2. The PHI 1 and PHI 2 signals are provided by flip-flop U66A which is clocked by the combination of the Decision Pulse (DP) and the Logic Clock (LC) through "nand" gate U57C.

4-32. Every seven PHI pulses, a new field of a channel's parameters and data are aligned in the circulating registers, and an extra pulse time is taken to process the data. During this time, PHI 1 or PHI 2, whichever happens to be in the "1" state, is kept in the "1" state by stopping the clock to U66A. Thus the PHI 1 and PHI 2 sequence is halted for about a quarter microsecond. The information clocked into

4-30.   OSCILLATOR. The oscillator is mounted on the lower select code PCA. Resistors R3 and R4 connected across inverters U12A and U12B, respectively, cause the inverters to operate as linear amplifiers and oscillate the

Figure 4-3. Functional Block Diagram, Asynchronous Multiplexer Control PCA

the main memory shift register at the end of this cycle is the modified parameters and data.

4-33. FIELD COUNTER U43.

4-34.   The Field Counter is on the lower select code PCA and is a 4-bit synchronous binary counter which counts the shifts for positioning data fields in the circulating registers on the upper select code PCA. There are 37 fields of seven shifts plus one decision pulse with four additional shifts necessary to complete the cycle. This gives 300 Logic Clock (LC) pulses for each revolution of the circulating registers.

4-35. ADDRESS COUNTER U95.

4-36.   The Address Counter is also a 4-bit synchronous binary counter. The address counter is incremented each time a data field passes and makes a comparison with the last address output by the computer through Address Compare U85. The counter starts counting with the first receive channel, counts 16 receive channels, 16 send channels, and then the five receive-only auxiliary channels. When the addresses in the two counters compare, the Match signal is sent from Address Compare U85. The Match signal combines with the set-side output of the STC Flag FF in nand gate U86C to produce a Transfer signal.

4-37. INTERRUPT AND CONTROL CIRCUITS.

4-38.   The interrupt and control circuits on the lower select code PCA are similar to the standard circuits described in the computer documentation. The CLF Buffer FF and the STC Buffer FF prevent the possibility of interference that could occur when the interface tries to make a decision at the same time the computer issues a CLF or STC command. Interface decisions are made upon computer IOBO signals as the circulating registers revolve. Interference is prevented by storing the CLF and STC signals in the buffer flip-flops and then transferring these signals to the Transfer Up Flag (T Flag) FF and STC Flag FF, respectively.

4-39.   TRANSFER UP FLAG (T FLAG) FF. The clear-side output of the T Flag FF indicates that characters may be sent from the circulating registers to the IOBI buffers to await input to the computer. The sequence of events is as follows:

a. A character is received or a character transmission is completed.

b. The Buffer Flag (part of U71) for the channel sets.
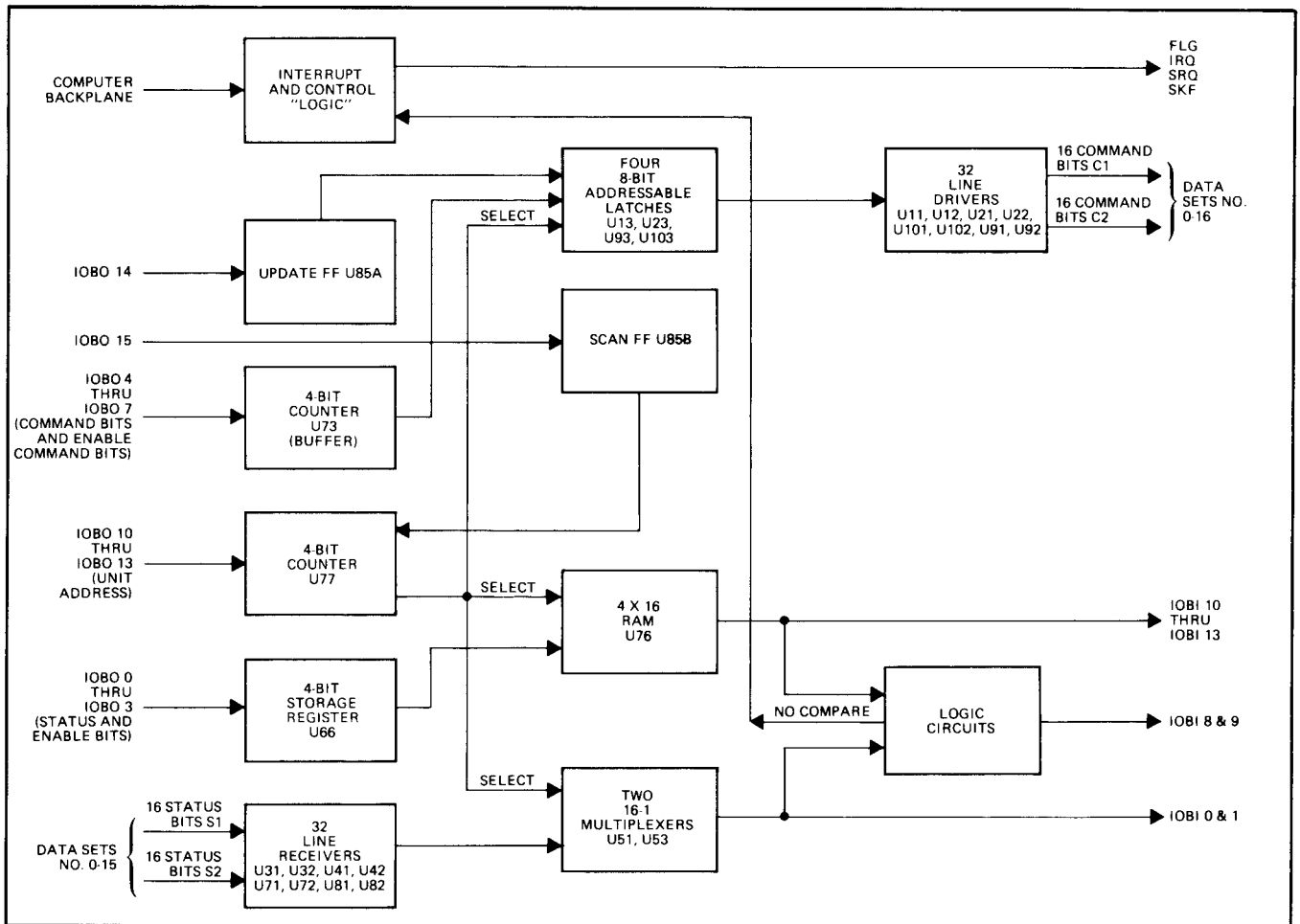
c. When the T Flag FF clears, the information is taken from the circulating registers and the T Flag FF sets.

d. T Flag being set causes an interrupt in computer operation.

e. The computer program responds with a Clear Flag (CLF) signal which clears the T Flag FF upon receipt of the next Logic Clock (LC) pulse.

4-40.   SET CONTROL FLAG (STC FLAG) FF. When the computer is sending information to the interface, the sequence of events is as follows:

a. The computer outputs information which is stored in buffer flip-flops on the upper select code PCA and outputs an address which is stored in buffer flip-flops on the lower select code PCA.

b. The computer issues an STC command which sets the STC Buffer FF. Synchronized with the circulating registers, the STC Flag FF sets.

c. When the address counter matches the address output of the computer through the address compare circuits, the Match signal combines with the set-side output of the STC Flag FF to send the Transfer signal to the circulating registers.

4-41. SELECT CODE DECODING.

4-42.   Decoding for both the upper and the lower select code outputs is performed by circuits on the lower select PCA. Buffer storage elements are contained on both upper and lower select code assemblies. For example, the data or parameters outputs to the lower select code are clocked into buffer flip-flops U55, U75, U85, and U95 on the upper select code PCA. The Output Lower SC signal, which is sent through the interconnecting cable, clocks the buffer flip-flops on the upper select code PCA.

4-43.   Data and status being transferred from the interface circulating registers to the computer are stored in buffer flip-flops U45, U55, and U96 on the lower select code PCA and U104 and U105 on the upper select code PCA. An LIA/B, MIA/B instruction to the lower select code will retrieve data from both locations.

4-44. DATA SET RECEIVERS AND TRANSMITTERS.

4-45.   Data from the data sets comes into the lower select code PCA through line receivers U93, U94, U102 and U103 to 16-to-1 multiplexer U105. One of the 16 input data lines is selected by the address number present on the select lines to the multiplexer; this data is output to flip-flop U32A. The set-side output of U32A is switched by "and-or" inverter gates U42 to either the auxiliary channel memory U32B or to the line that sends the Line signal to the upper select code PCA.

4-46.   There are 16 output transmitters contained in four integrated circuits, U62, U72, U82, and U92. The transmitters send signals from 16 output buffers in U63, U73, U83, and U84 to the data sets. Once every revolution of the circulating registers, a short pulse is sent from U116A to load the buffers. The signals then pass through the transmitters to the data sets. The input to the buffers is from two 8-bit shift registers, U53 and U74, which shift along with the circulating registers and collect bits from the individual channels.

START

A

Increment channel address.
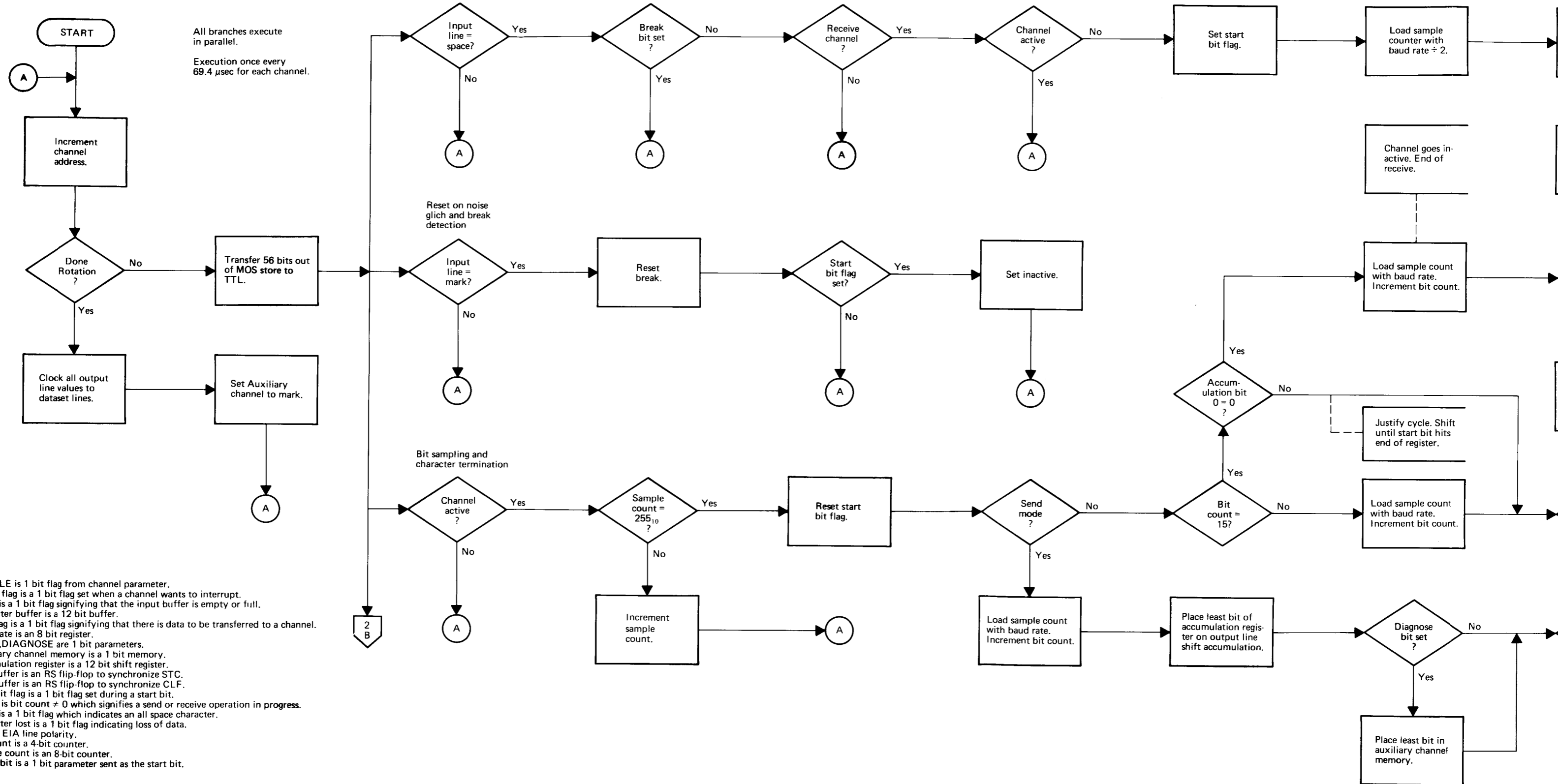
All branches execute in parallel.

Execution once every 69.4 μsec for each channel.

Character reception start

Input line = space? — Yes → Break bit set ? — No → Receive channel ? — Yes → Channel active ? — No → Set start bit flag. → Load sample counter with baud rate ÷ 2.

Input line = space? — No → A

Break bit set ? — Yes → A

Receive channel ? — No → A

Channel active ? — Yes → A

Done Rotation ? — No → Transfer 56 bits out of MOS store to TTL.

Done Rotation ? — Yes

Clock all output line values to dataset lines. → Set Auxiliary channel to mark. → A

Reset on noise glich and break detection

Input line = mark? — Yes → Reset break. → Start bit flag set? — Yes → Set inactive.

Input line = mark? — No → A

Start bit flag set? — No → A

Set inactive. → A

Channel goes in-active. End of receive.

Load sample count with baud rate. Increment bit count.

Accumulation bit 0 = 0 — No

Accumulation bit 0 = 0 — Yes

Justify cycle. Shift until start bit hits end of register.

Bit sampling and character termination

Channel active ? — Yes → Sample count = 255₁₀ ? — Yes → Reset start bit flag. → Send mode ? — No → Bit count = 15? — No → Load sample count with baud rate. Increment bit count.

Channel active ? — No → A

2 B

Sample count = 255₁₀ ? — No → Increment sample count. → A

Send mode ? — Yes → Load sample count with baud rate. Increment bit count.

Bit count = 15? — Yes

Load sample count with baud rate. Increment bit count. → Place least bit of accumulation register on output line shift accumulation. → Diagnose bit set ? — No

Diagnose bit set ? — Yes → Place least bit in auxiliary channel memory.

ENABLE is 1 bit flag from channel parameter.
Buffer flag is a 1 bit flag set when a channel wants to interrupt.
T flag is a 1 bit flag signifying that the input buffer is empty or full.
Character buffer is a 12 bit buffer.
STC flag is a 1 bit flag signifying that there is data to be transferred to a channel.
Baud rate is an 8 bit register.
ECHO,DIAGNOSE are 1 bit parameters.
Auxiliary channel memory is a 1 bit memory.
Accumulation register is a 12 bit shift register.
STC buffer is an RS flip-flop to synchronize STC.
CLF buffer is an RS flip-flop to synchronize CLF.
Start bit flag is a 1 bit flag set during a start bit.
Active is bit count ≠ 0 which signifies a send or receive operation in progress.
Break is a 1 bit flag which indicates an all space character.
Character lost is a 1 bit flag indicating loss of data.
Line is EIA line polarity.
Bit count is a 4-bit counter.
Sample count is an 8-bit counter.
Synch bit is a 1 bit parameter sent as the start bit.

2176-21

Figure 4-4. Operational Flowchart (Sheet 1 of 2)

Figure 4-4.

2176-28

Figure 4-4. Operational Flowchart (Sheet 2 of 2)

2176-26

Figure 4-5. Timing Relationship of Single Transmitted
Character and the Circulating Memory

4-47. CIRCULATING REGISTERS.

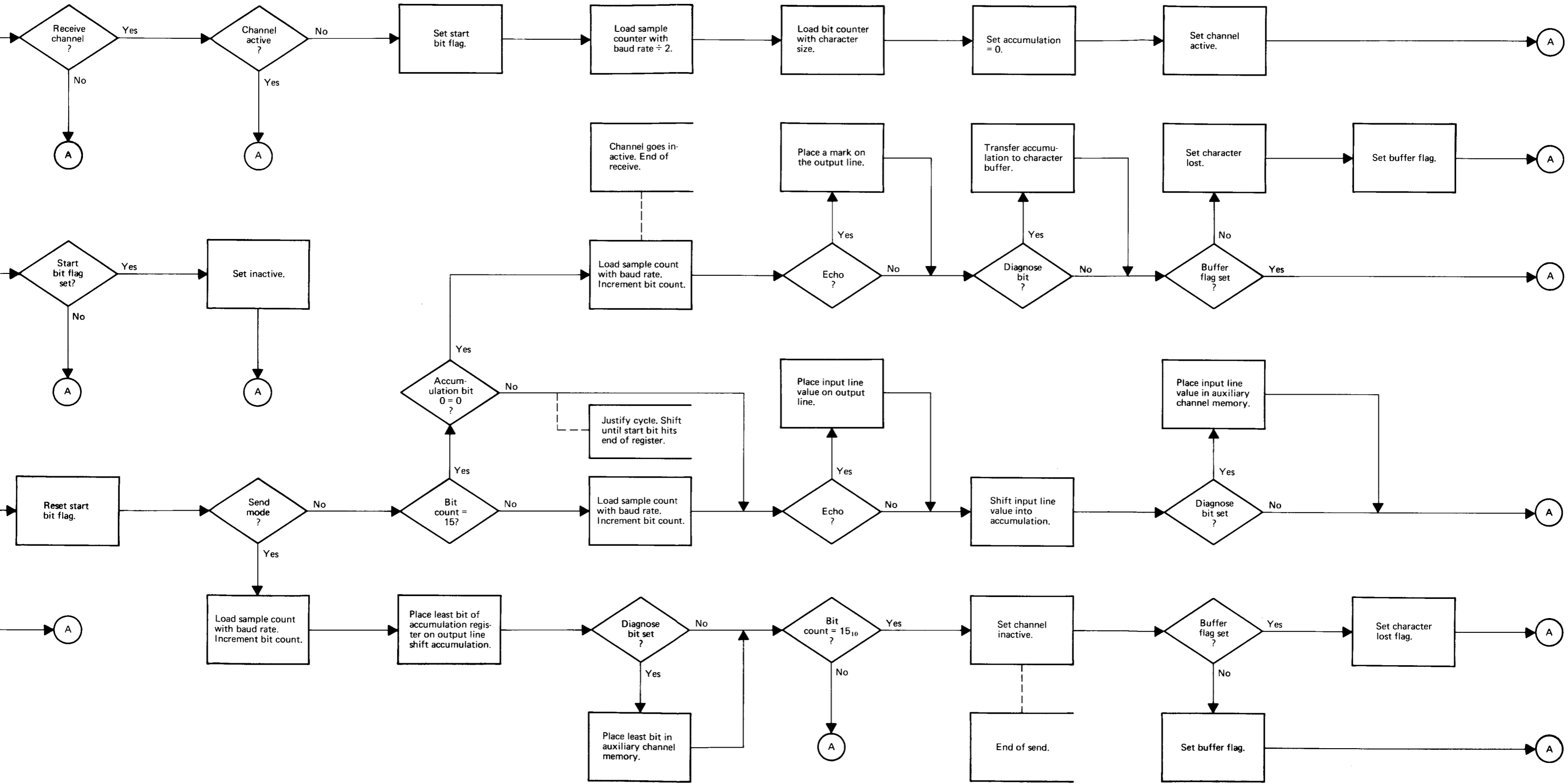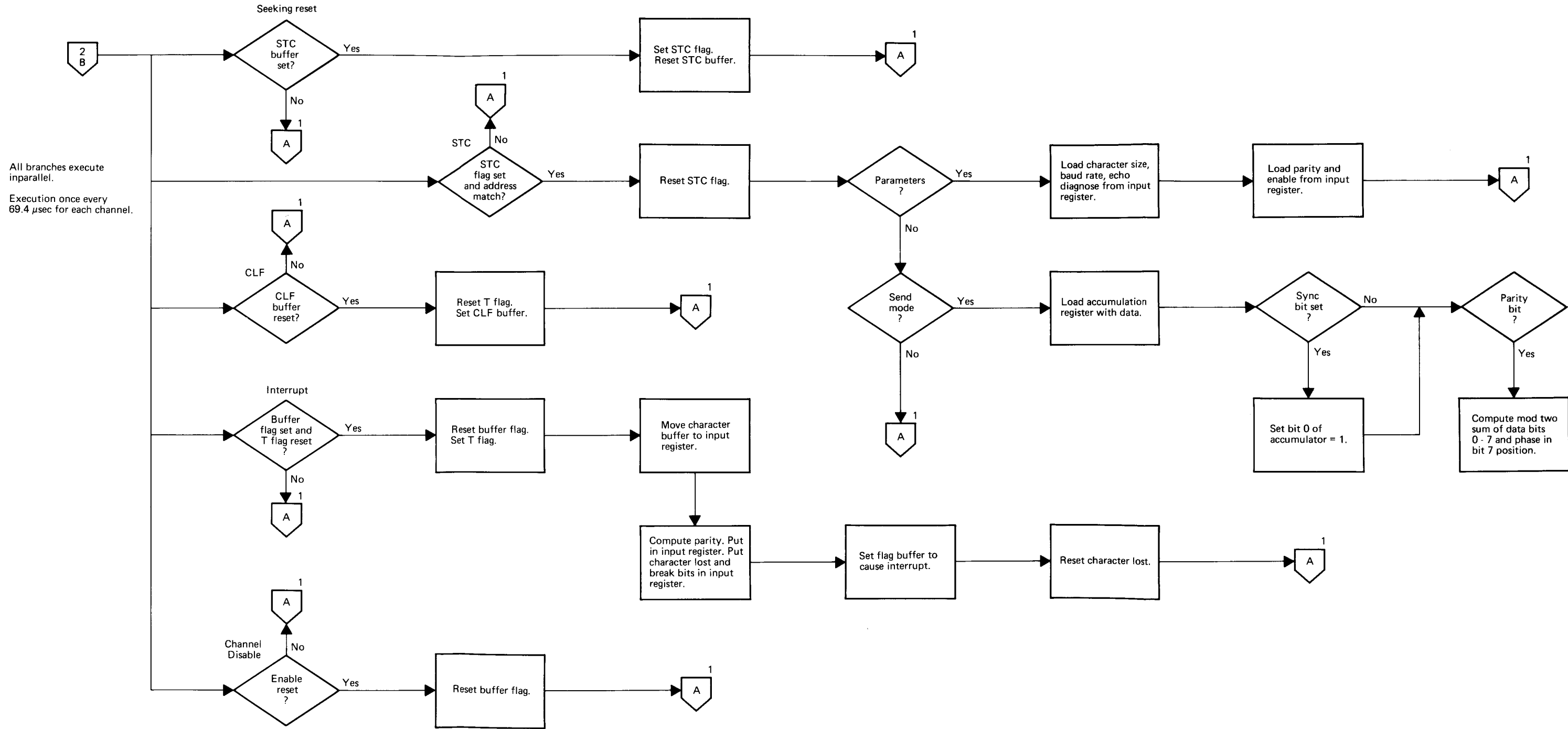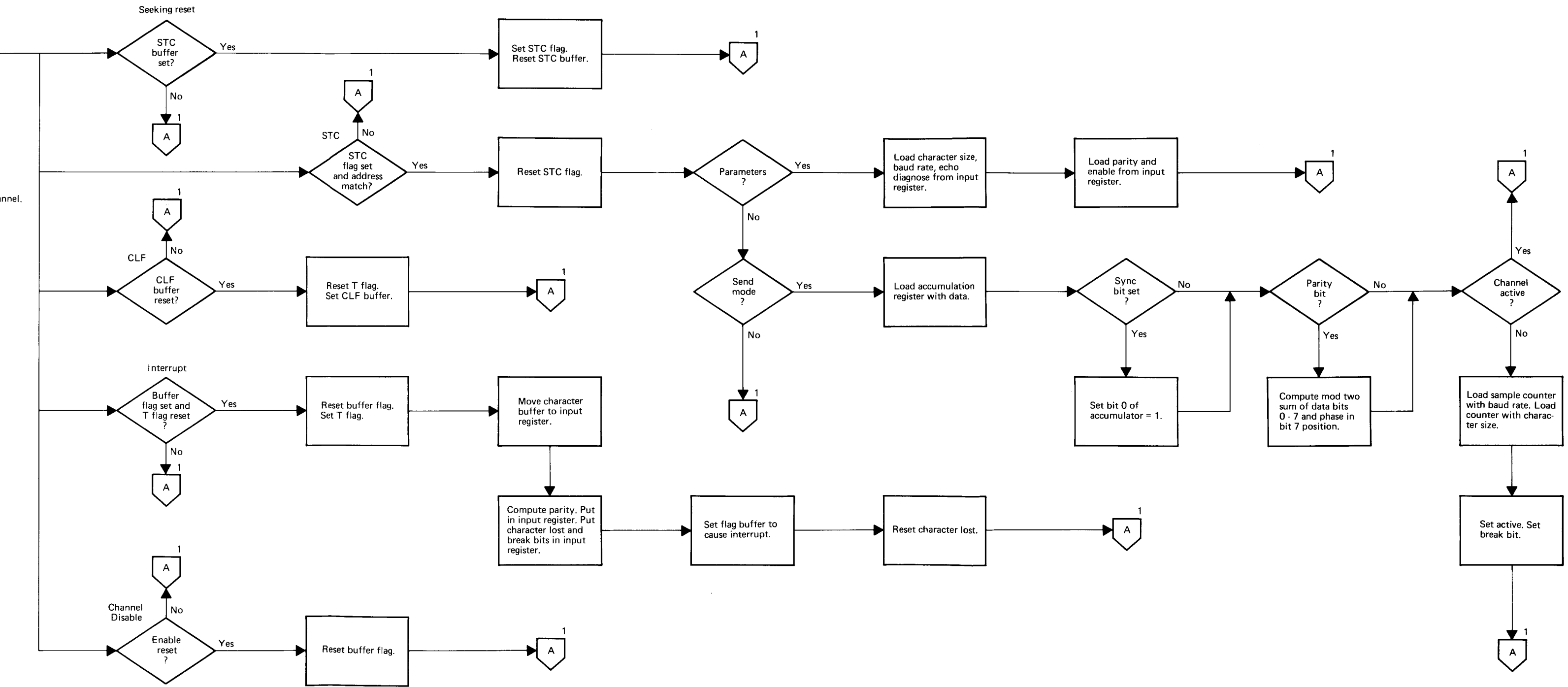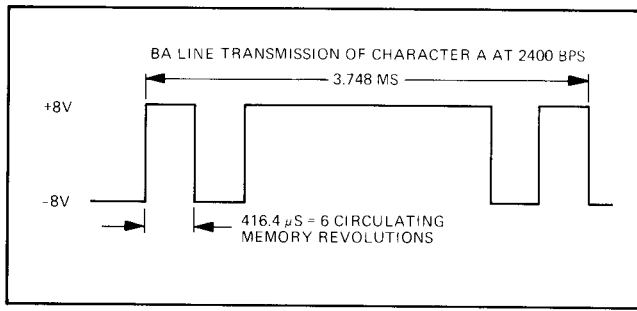4-48.   There are two loop circuits made up of registers through which data and parameters circulate on the upper select code PCA. One loop consists of circulating registers U62, U71, U72, U81, U82, U92, U91, U101, U102, U103, U93, U83, and U73 which receive information from main memory shift register U63. The other loop consists of circulating registers U52, U51, U41, U42, U32, U31, U21, U22, U23, U33, and U43 which receive information from main memory shift register U53. The circulating registers receive 56 bits of information, 8-bits at a time, at 1.86 microsecond intervals from the main memory shift registers. The field of information consists of status and parameters bits as defined in the following paragraphs.

4-49.   BREAK. A break is defined as the absence of a mark condition on the input data line during the reception or transmission of a character. At the beginning of the start bit the break bit (in U71 of the circulating registers) will be set. This is a result of the Line signal going to logic 1 when the Active signal is a logic 0 or when data and an STC command is output in the send mode. Break remains high as long as the Line signal remains high and will be cleared if the input line goes to a "mark." The Break bit indicates to the computer upon reception that the character (including stop bits) was all zeroes. Upon transmission of characters, the Break bit indicates that the input data line was all zeroes for the duration of one character transmission.

4-50.   BUFFER FLAG. When the multiplexer interface is finished receiving or transmitting a character, the Buffer Flag (in U71) sets. This flag indicates "buffer-full" in the receive mode and "buffer empty" in the send mode. The Buffer Flag signal controls the movement of data to the computer and the generation of interrupts. When the T Flag FF is clear (indicating that it is permissable to send data and address through the IOBI buffers to the computer) and when the Buffer Flag is set, a transfer to the computer is made. The T Flag FF is set and the Buffer Flag is cleared. The T Flag FF, in turn, sets the interrupt logic Flag Buffer FF and an interrupt occurs. Since the Buffer Flag is cleared, the channel does not request another interrupt, and interrupts from other channels are inhibited due to the T Flag FF being set. A CLF signal clears the T Flag FF and allows further interrupt requests.

4-51.   ECHO. Some asynchronous devices, such as teletypes, will only print received characters, so send characters must be echoed back from the receiving end to be printed. With the echo parameter on (Echo bit set in U51) all characters received for a channel are returned bit-by-bit to the source. This provides an echo with only ½-bit time delay. This delay is shown in figure 4-6. When the multiplexer interface is transmitting data the echo parameter must be off, allowing only the transmitted characters on the line.

4-52.   DIAGNOSE. The Diagnose bit (U51) can be set (logic 1) in either the transmitted or received parameters. When set, the diagnose bit enables data to go to the five auxiliary channels. This bit is connected to the lower select code PCA and if the channel is a receive channel, the Line value is clocked into Auxiliary Channel Memory FF, U32B. If the channel is a send channel, the new Bit value is clocked into U32B. During transmit, the five auxiliary channels can be configured to receive the same input. During receive, the five auxiliary channels can be configured to different baud rates and the incoming data would be examined as received by each channel to determine the baud rate and thus the type of terminal that is sending data.

4-53.   BAUD RATE. The Baud Rate parameter is an eight-bit number that initializes an eight-bit counter which measures the time between bits. A programmable divide-by-n counter for each channel allows operation of each channel at any one of 256 frequencies. The eight-bit number is output as the baud rate parameter and is used as the divisor. During transmit or receive, each time the channel field rotates into position, the sample counter is incremented. When the counter reaches all ones, the baud rate parameter is reloaded into the sample counter. The number of counts required for the sample counter to increment up from the preset number to all ones determines the time between bit samples.

4-54.   PARITY. The Parity bit occupies the same position in U51 as the Echo bit and applies to a transmit channel. This causes the set-side output of the IOBO 7 FF to U76 to be replaced by the output of Parity Checker/ Generator U65. Thus, when data to be output is clocked
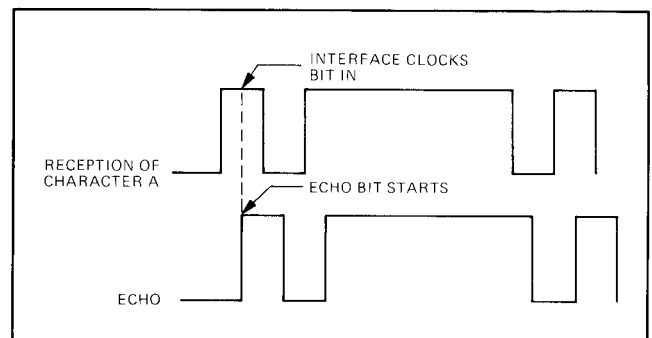
2176-27

Figure 4-6. Timing Relationship of Received Character
and Echo Bit Transmission

into the accumulate register it can have parity affixed to it. Parity Check, a status bit, is not affected by the parity parameter bit.

4-55.   ENABLE. The Enable bit (U51) is set (logic 1) to allow a channel to request an interrupt. When turned off (logic 0) the Enable bit acts as an interrupt disarm, and the channel can transmit and receive characters but will not interrupt the computer program. The Enable bit combines with the Buffer Flag bit in "and" gate U67 and disables the Buffer Flag bit when the enable bit is a logical 0.

4-56.   CHARACTER LOST. The Buffer Flag (U71) is set at the end of a receive or transmit operation. If another operation occurs, the Stop signal goes high to indicate completion. When both the Stop signal and Buffer Flag go high, the computer is not servicing the interface fast enough. When two characters are received without being serviced, the first character received is written over by the second and the Character Lost status bit is set. The Stop signal and Buffer Lost signal combine in "and" gate U27A to set the Character Lost bit in register U71.

4-57.   START BIT. At the beginning of a receive cycle, the Start Bit (U71) is set by the Receive Start signal to guard against a receive cycle being triggered by noise voltage pulses. If the input line goes back to a "mark" before the middle of the start bit, the output of "nand" gate U56A clears the Bit Count register U73. This causes the Active signal to be low, indicating that no operation is in progress or that the receive operation is aborted. However, if the start bit does not change through the middle of the bit, the Carry Out pulse from Sample Count counter U103 clears the Start Bit (U71).

4-58.   ACCUMULATE. The Accumulate register U42, U21, and U33 transfers data bits from the multiplexers to the buffer registers. At the beginning of a receive operation, it is loaded with zeroes because multiplexers U41, U31, and U23 are disabled. This zero load is necessary because the justify cycle requires zeroes in front of the start bit at the end of a receive operation. When data is being output from the computer, shift pulses from the Sample Count counter serially shift the data through the accumulate register. During a send operation the first bit in U33 (pin 5) is loaded with the Synch bit from the data output word. Since the first shift occurs one bit time after the output, the start bit does not get shifted out (pin 10) until one bit-time has elapsed. Registers U42, U21, and U33 shift as one unit when data is input to Serial In of each register.

4-59.   At the end of a receive operation the data is not right-justified. At this time both the Sample Count and Bit Count are logic 1's and shifts occur once every 69.4 microseconds. The counters cannot count because the count enable is held off by the Right Justify signal from "nand" gate U47A. When the start bit gets to the end of the register and is output from U33 (pin 10) the Right Justify signal goes high, the counters roll over to zero, and the data is loaded into the buffer register to complete the operation.

4-60.   SAMPLE COUNT. The Sample Count counter U92 and U103 functions as a divide-by-n counter to determine the bit (baud) rate. At the beginning of a send or receive operation and after each bit has been shifted, the counter is loaded with a predetermined number, the baud rate parameter. The bit rate is determined by the number of counts required to fill the counter to capacity and cause it to "roll over" to zero. At the beginning of a receive operation, U82 and U102 quad multiplexers shift the complement of the programmed baud rate parameter to the right one place, dividing the parameter by two. Thus, when the start bit occurs, only half the normal number of counts causes the counter to "roll over," and the start bit is sampled in the middle of its time period. All other data bits are sampled at the specified baud rate and, consequently, at a point near the middle of the time that each bit is available.

4-61.   BIT COUNT. When the sample counter increments to all ones, the output at U103, pin 15 increments the Bit Count counter. At the beginning of a send or receive operation the bit counter is loaded with the character size parameter. When the counter "rolls over" to zero, the specified number of bits have been sent or received.

4-62.   CONTROL INTERFACE THEORY OF OPER-ATION.

4-63.   The control interface can be either one or two control PCAs. Only one control PCA is needed when interfacing with 103-type data sets and terminals. For 202-type data sets, two control PCAs are used. Each PCA is independent of the other, programmed through its distinct select code, and routes signals through different pins in the control panel output connectors. The first control PCA is connected to connector panel receptacles J16 and J20. When a second control PCA is used, it must be connected to connector panel receptacles J17 and J19. These connections ensure that each signal is properly routed to multiplexer input/output channels.

4-64.   The control PCAs each provide two programmable command signals (C1 and C2) and monitor two status signals (S1 and S2) for each of the 16 input/output channels. Table 3-7 lists the command and status signals for each control PCA and the associated signal name at the data set. The signals shown in table 3-7 are available for each of the 16 input/output channels.

4-65.   The program controls the output of command signals to a data set and the input of status signals from a data set by straightforward output and input commands. Also, status conditions can be stored on the control PCA and an interrupt initiated if a change in status is detected. This allows the control PCA to operate as an input line monitor and to provide an interrupt when the programmed conditions occur. A typical condition that may be programmed is, "interrupt when the signal detector line for channel 5 is 0". The request for interrupt can be enabled, changed, or disabled only by the program.

4-66. When a condition for interrupt is programmed, a status condition that is opposite the desired status condition is stored in a random-access-memory. A scanning process is then initiated and the memory spins through all 16 input/output channels seeking the input status condition that is different from the stored status condition. An interrupt will occur when the desired status condition is present at the programmed channel. In practice, every channel may be primed with stored status conditions and any channel can then interrupt when the desired status conditions occur. Therefore, many interrupts for other channels may occur between the time that conditions are output for a particular channel and the time that the desired conditions for that same channel cause an interrupt.

4-67. CONTROL PCA INITIALIZATION.

4-68. When power is initially applied by the computer POWER switch, the POPIO and CRS signals are received simultaneously by the control PCA from the computer. These signals establish initial conditions for operation of the control PCA. The POPIO signal sets the Flag Buffer FF and the Master Reset FF. At time T2, the ENF signal clears the Interrupt Request (IRQ) FF and sets the Flag FF. Refer to figure 4-3 for a functional block diagram of the control PCA.

4-69. When power is first applied, the CRS signal clears the Control FF. Therefore, the PCA is always in the initial state after power turn-on or whenever the computer PRESET switch is pressed. In this state all output lines are set to an off condition (negative voltage) and no interrupts will occur on status line changes.

4-70. FLAG AND CONTROL LOGIC.

4-71. A programmed STC instruction with the address of the control PCA provides STC, LSCL, LSCM, and IOG signals to set the Control FF. At time T5 of the computer machine cycle, the IRQ FF is set by the true set-side output signals of the Flag Buffer FF, the Flag FF, and the Control FF, and by the high IEN, PRH and SIR signals. The high set-side output signal of the IRQ FF is then applied to the computer as the FLG and IRQ signals to request an interrupt of the computer program. The IRQ FF is cleared at the next time T2 (ENF) to allow devices of higher priority to interrupt. If no higher priority device requests an interrupt, the IRQ FF sets again and interrupts the computer program. The IAK signal, with the high set-side output signal of the IRQ FF, clears the Flag Buffer FF to permit recognition of the next interrupt.

4-72. UNIT ADDRESS.

4-73. The bits that determine the unit address, IOBI bits 10 through 13, are applied to the inputs of presettable binary counter/latch U77. When an OTA/B instruction is executed, the IOO signal is applied to "nand" gate U26C. The negative output of gate U26C strobes counter U77 and allows its four latch circuits to assume the state of the unit address number being transferred from the A- or B-register of the computer.

4-74. COUNTER U77.

4-75. During the time period when the MR signal is high, counter U77 will advance one count with each ENF signal. The MR signal is high after POPIO goes high and remains high until the select code and IOG signals become high. The purpose of the counting is to count through each address in 64-bit random access memory (RAM) U76 to clear the memory of the stored status bits SS1 and SS2 and enable bits ES1 and ES2. Counter U77 advances one count at each negative-going transition of the pulse at the clock 1 input; this occurs with each ENF signal when the MR signal is true.

4-76. Counter U77 will also count when the Scan FF is set by executing an OTA/B instruction with IOBO 15 (scan bit) high. The high set-side output of the Scan FF is applied to "nand" gate U25B. If the Flag Buffer and Flag FFs are clear, the output of "nand" gate U65A will be high. When an ENF signal occurs (T2) the high output of U25A is applied to the clock 1 input of counter U77. At the trailing edge of the ENF signal, the counter will advance by one count. The counting will continue each time the ENF signal occurs if the Scan FF is set and the Flag Buffer and Flag FFs are clear.

4-77. Each time an input instruction (LIA/B, MIA/B) is executed, the IOI, select code, and IOG signals applied to "nand" gate U37B will be high. This will cause a high output from gate U25A to be applied to the clock input of counter U77 when IOI is high. At the trailing edge of the IOI signal, the counter will advance by one count. Therefore, each input instruction will advance the counter by one count after the information is transferred to the A- or B-register. If the Scan FF is clear, any number of successive units can be read into the A- or B-registers by executing repeated load instructions.

4-78. The state of the latch circuits in counter U77 determines the address selected within the 64-bit memory of RAM U76 (4 by 16 bits) and two of the bits in addressable latches U13, U23, U103, and U93. The latch circuits of counter U77 also enable one input line to each data selector, U51 and U53.

4-79. The states of the latch circuits in counter U77 are transferred to the computer A- or B-register when an LIA/B instruction is executed. The outputs of counter U77 are connected through "and" gates U67B, U87B, U97A and U97B to IOBI lines 10 through 13, respectively. Therefore, any information transferred from the PCA to the computer A- or B-register is accompanied by the unit number.

4-80. RANDOM ACCESS MEMORY U76.

4-81. Random access memory (RAM) U76 is a 64-bit memory of which 4 bits are selected for each state (0 through 15) of the count in counter U77. Inputs to the RAM are enabled when the Write line is low. Before being transferred to RAM U76, information is temporarily stored in 4-bit binary counter/latch U66, which is utilized as a storage register only. Information is input from IOBO lines

0 through 3 when the strobe pulse on pin 1 goes low. If IOBO bit 14 of the information being transferred from the computer A- or B-register is high, the Update FF (U85) will be set. The set-side output of the Update FF combines with the next SIR signal through "nand" gate U75D to enable the input lines of RAM U76. The information in storage register U66 is transferred into the four bits of memory in RAM U76 selected by the unit address specified in the OTA/B instruction. The latch circuits in storage register U66 are cleared by the "not" MR signal during the master reset period.

4-82.   BUFFER U73.

4-83.   Buffer U73 is a presettable binary counter/latch utilized as a storage register for command bits C1 and C2 (IOBO lines 4 and 5) and enable command bits EC1 and EC2 (IOBO lines 6 and 7). When an OTA/B instruction is executed, the IOO signal applied to "nand" gate U26C results in a negative output which strobes buffer U73. This allows the U73 latch circuits to assume the state of the IOBO line 4 and 5 inputs and the line 6 and 7 inverted inputs. The latch circuits are cleared by the "not" MR signal during the master reset period.

4-84.   ADDRESSABLE LATCHES U13, U23, U93, AND U103.

4-85.   Each of the identical integrated circuits (U13, U23, U93, and U103) contains eight addressable storage latch circuits. Each latch circuit has a separate output with one input common to all eight. Information may be input to any latch circuit by addressing that latch circuit with the binary address on the A_0, A_1, and A_2 leads. When the enable input goes low, the information on the D input will be set in the addressed latch circuit.

4-86.   The three least significant binary bits of the unit number are connected from A, B, and C of counter/latch U77 to the address inputs of addressable latches U13, U23, U93, and U103. The fourth bit (8's bit) is connected from D of counter/latch U77 to the enable inputs of the same addressable latches through "or" gate U33A, B, C, and D. This fourth bit will be a logic 0 when the unit address is a number from 0 through 7, and the low outputs of "or" gates U33A and U33B will enable addressable latches U13 and U23. The outputs of U33C and U33D will be high and the addressable latches U103 and U93 will not be enabled, although they are addressed. If the unit address is a number from 8 through 15, the conditions are reversed and address-able latches U93 and U103 would be addressed and enabled and U13 and U23 would be addressed but not enabled.

4-87.   When the enable command bit EC1 is true, the output level from A of storage register U73 prevents the output of U43C from going low. This prevents enabling of addressable latches U13 and U103, which store all of the C1 command bits. In the same manner, when the enable command bit EC2 is high, the output level from C of storage register U73 prevents the output of U43A from going low. This prevents enabling of addressable latches U23 and U93 which store all of the C2 command bits.

4-88.   None of the addressable latches (U13, U23, U93, and U103) can be enabled unless the output of U75D goes low. This can only happen when the Update FF is set and the SIR signal occurs. At that time, the information stored in the C1 and C2 command bit latch circuits in U73 can be transferred into the addressed latch circuits in U13, U23, U103, or U93.

4-89.   In summary, information is transferred into the latch circuits of the addressable latches as follows:

a.   The address of the individual latch circuit will be in the three least significant bits of the unit address in counter/latch U77.

b.   Two of the four addressable latches (U13, U23, U103, and U93) will be selected by the "8's" bit of the unit address in counter/latch U77.

c.   The enable command bits EC1 and EC2 from storage register U73 must be low.

d.   The Update FF must be set and the SIR pulse must be high for the C1 and C2 command bits (inverted) to be transferred to the addressed latch circuit.

4-90.   QUAD LINE DRIVERS U11, U12, U21, U22, U101, U102, U91, and U92.

4-91.   The quad line driver integrated circuits contain drivers for each of the lines from the addressable latch. The driver inverts the signal and provides an output that swings both positive and negative. A capacitor is connected to each of the output lines to slow the switching time.

4-92.   QUAD LINE RECEIVERS U32, U31, U81, U82, U42, U41, U71, and U72.

4-93.   The quad line receiver integrated circuits receive signals from external devices through the control panel. The levels of the incoming signals are positive and negative with respect to ground. The outputs are inverted with respect to the inputs, and are positive. A capacitor connected to each receiver reduces the sensitivity to noise pulses.

4-94.   MULTIPLEXERS U51 AND U53.

4-95.   Each multiplexer integrated circuit has 16 input lines for status bits S1 or S2 from the quad line receivers. The unit address number from counter/latch U77 is connected to the A, B, C, and D inputs of the multiplexers and selects one of the 16 inputs to be transferred to the output line. The output signal is inverted with respect to the input. For every unit address number, one status bit S1 and one status bit S2 will be selected. The selected S1 and S2 bits are transferred to the computer A- or B-register through "and" gates U47A and U47B when an LIA/B instruction is executed.

4-96.   The selected status bits S1 and S2 are compared to the stored status bits SS1 and SS2, for that unit address number, in exclusive "or" gate U95. Status bit S1 and

stored status bit SS1 are compared in U95C. If SS1 is a binary one it will provide a low input to U95. If, at the same time S1 is a binary one, it will provide a high input to U95, and the output of U95 will be high. Thus, whenever the status bits and stored status bits transferred into the PCA are both the same (binary ones or zeroes) the output of exclusive "or" gate U95 will be high, if not, it will be low.

4-97.   If a comparison of status and stored status is to be made, the appropriate enable status bit (ES1 or ES2) will be set in the corresponding unit address in RAM U76. As a result, when the status bit S1 and the stored status bit SS1 do not compare (as binary ones or zeros) and enable status bit ES1 is set high, a binary one is transferred to the A- or B-register of the computer with an LIA/B instruction. The binary one is transferred through "and" gate U96C, inverter U86F, and U57A. If the S1 and SS1 bits compare or if the ES1 bit is low, a binary zero will be transferred to the computer A- or B-register with the LIA/B instruction. The

logic circuits that process status bit S2, stored status bit SS2, and enable status bit ES2 are identical.

4-98.   When the Scan FF is set by executing an OTA/B instruction (bit 15 high), the unit address number stored in counter/latch U77 is counted from 15 through 0 and over again until it is stopped. During this scan, any status bits that have their enable bits set high will be compared to their stored status bits. If a no-compare condition exists with the associated enable status bit set high, the output of "nand" gate U75C will go high. This will make all inputs to "nand" gate U65B high if the Flag and Flag Buffer FFs are clear. When the SIR signal goes high (T5), the output of U65B goes low to set the Flag Buffer FF and cause counter/latch U77 to stop counting. Executing an LIA/B instruction will load the status information into the computer A- or B-register. This information will include the unit address number where the no-compare condition took place, the stored status, the status and the appropriate interrupt bit in word format position 8 or 9.

5-1. INTRODUCTION.

5-2. This section provides maintenance information for the interface kit. Preventive maintenance procedures, corrective maintenance, and diagnostic test information are included. This information is supported by schematic diagrams, parts location diagrams, and replaceable parts lists.

5-3. PREVENTIVE MAINTENANCE.

5-4. Perform preventive maintenance for the interface kit at the same intervals as for the computer system.

5-5. Inspect the interface PCAs for burned or broken components and for the presence of foreign material. Check the cables and connectors included with the kit for damaged insulation and bent or broken pins. After any damage has been repaired, perform the diagnostic tests as described in paragraph 5-9.

5-6. CORRECTIVE MAINTENANCE.

5-7. Most malfunctions of the interface kit can be traced by analyzing the results of the diagnostic tests described in paragraph 5-9. Oscilloscope checks help to localize a fault to a single component.

5-8. Voltages of the signals that are transferred between the interface PCAs and the I/O devices are given in the table of specifications in section I of this manual. Refer to the computer documentation for characteristics of the signals transferred between the interface PCAs and the computer.

5-9. DIAGNOSTIC TESTS.

5-10. Perform the Asynchronous Channel Multiplexer Test and Asynchronous Multiplexer Control Test to verify proper operation of the data interface PCAs and the control interface PCA, respectively. The Diagnostic Program Procedures, part number 12921-90001 for the Asynchronous Channel Multiplexer Test and part number 12922-90001 for the Asynchronous Multiplexer Control Test, are located in the *Manual of Diagnostics* and give operating procedures for performing the diagnostic tests if the interface kit is installed in an HP 2100A Computer. If the kit is installed in an HP 2114, 2115, or 2116 Computer, the following additional documents will be useful for describing differences in computer front-panel operations.

a. HP 2114 *Front Panel Procedures*, part number 5951-1372.

b. HP 2115/2116 *Front Panel Procedures*, part number 5951-1370.

5-11. REPLACEABLE PARTS.

5-12. A replaceable parts list for each interface PCA is provided in tables 5-1, 5-2 and 5-3. The parts lists are in reference designation order and are used in conjunction with the parts location diagrams. The replaceable parts are referenced to the parts location diagrams by reference designations, which correspond to the interface schematic diagrams.

5-13. The parts lists provide the following information for each part:

a. REFERENCE DESIGNATION. The complete reference designation for each replaceable part.

b. HP PART NUMBER. The HP part number for each replaceable part.

c. DESCRIPTION. The description of each replaceable part. Refer to table 6-5 for an explanation of abbreviations used in the DESCRIPTION column.

d. MFR CODE. A five digit code that denotes a typical manufacturer of a part. Refer to table 6-6 for a list of manufacturers.

e. MFR PART NUMBER. The manufacturer's part number for each replaceable part.

5-14. DIAGRAMS.

5-15. The maintenance diagrams in this section consist of a parts location and schematic diagram for each PCA and an interconnecting diagram for the interface kit. These diagrams are supplemented by the integrated circuit diagrams of figure 5-1.

5-16. PARTS LOCATION AND SCHEMATIC DIAGRAMS.

5-17. Figures 5-2, 5-3, and 5-4 are parts locations and schematic diagrams for the interface PCAs. The parts location diagram for each PCA is located adjacent to the schematic diagram and shows the location and appearance of the electrical parts on each PCA. The parts are identified by the reference designations used on the schematic

diagrams. The PCA part number and identification code is shown on the parts location diagram as it is marked on the PCA itself.

5-18.   INTERCONNECTING DIAGRAM.

5-19.   Figure 5-5 is an interconnecting diagram that shows the output pin connections on the interface PCAs, cable connections to the connector panel, and connector panel routing to the data set connectors. Signal names are provided at both ends of the connecting strings with intermediate references from pin to pin so that each signal may be easily traced in either direction. For connections from the connector panel to the data sets, refer to tables 2-1 through 2-3. For connections between the interface PCAs and the computer, refer to the schematic diagrams.

Figure 5-1. Integrated Circuit Diagrams (Sheet 1 of 3)
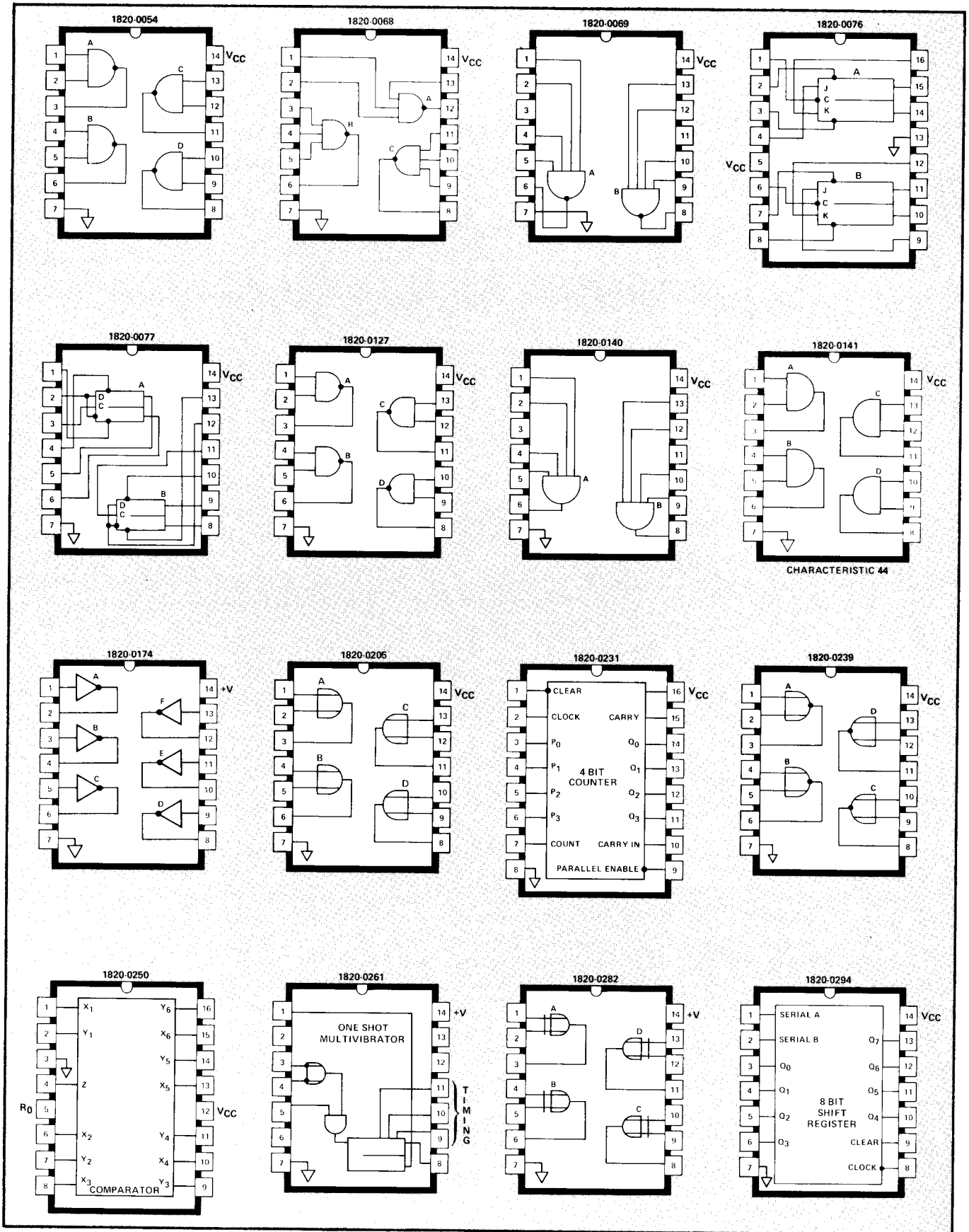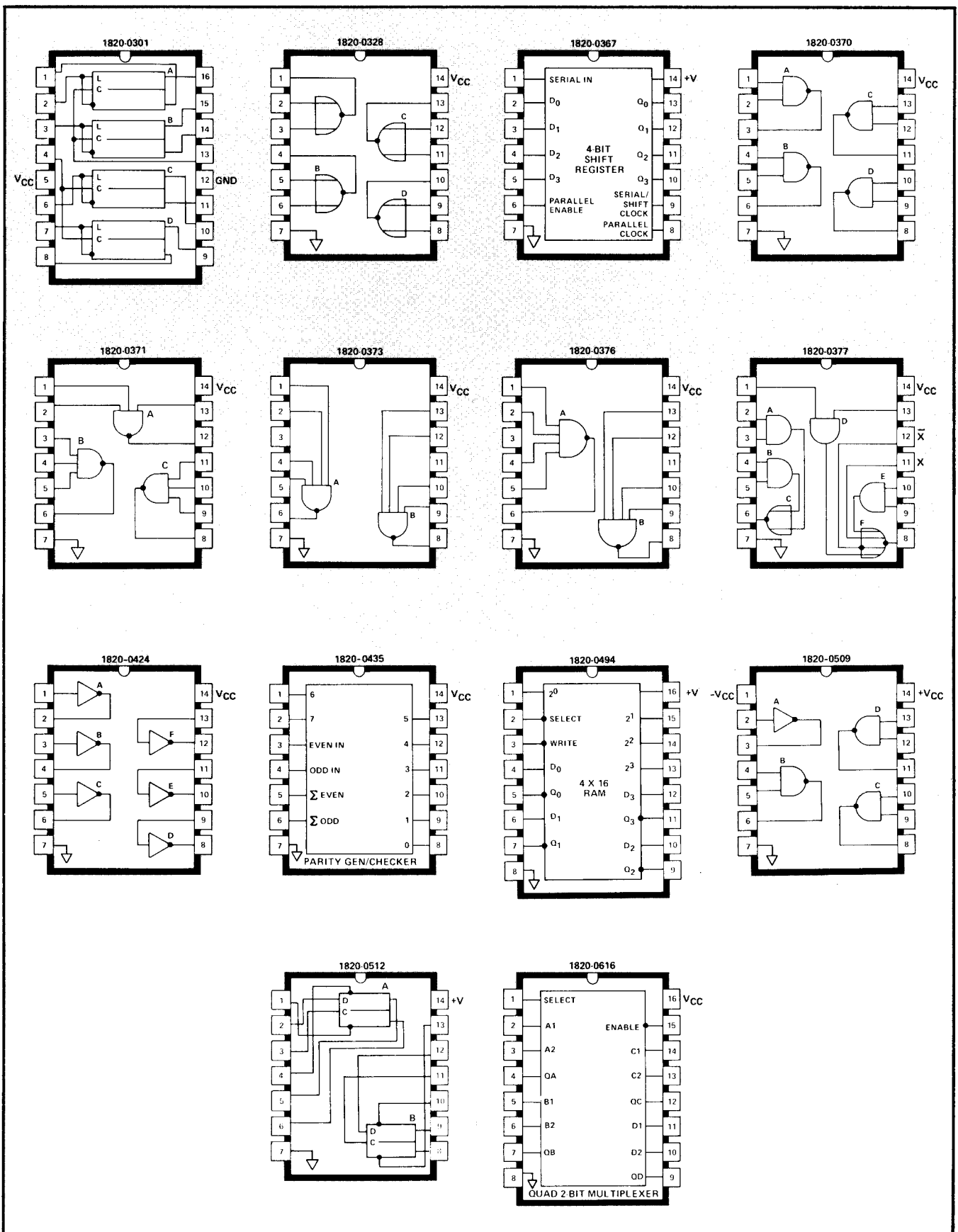
2176-22(1)

Figure 5-1. Integrated Circuit Diagrams (Sheet 2 of 3)
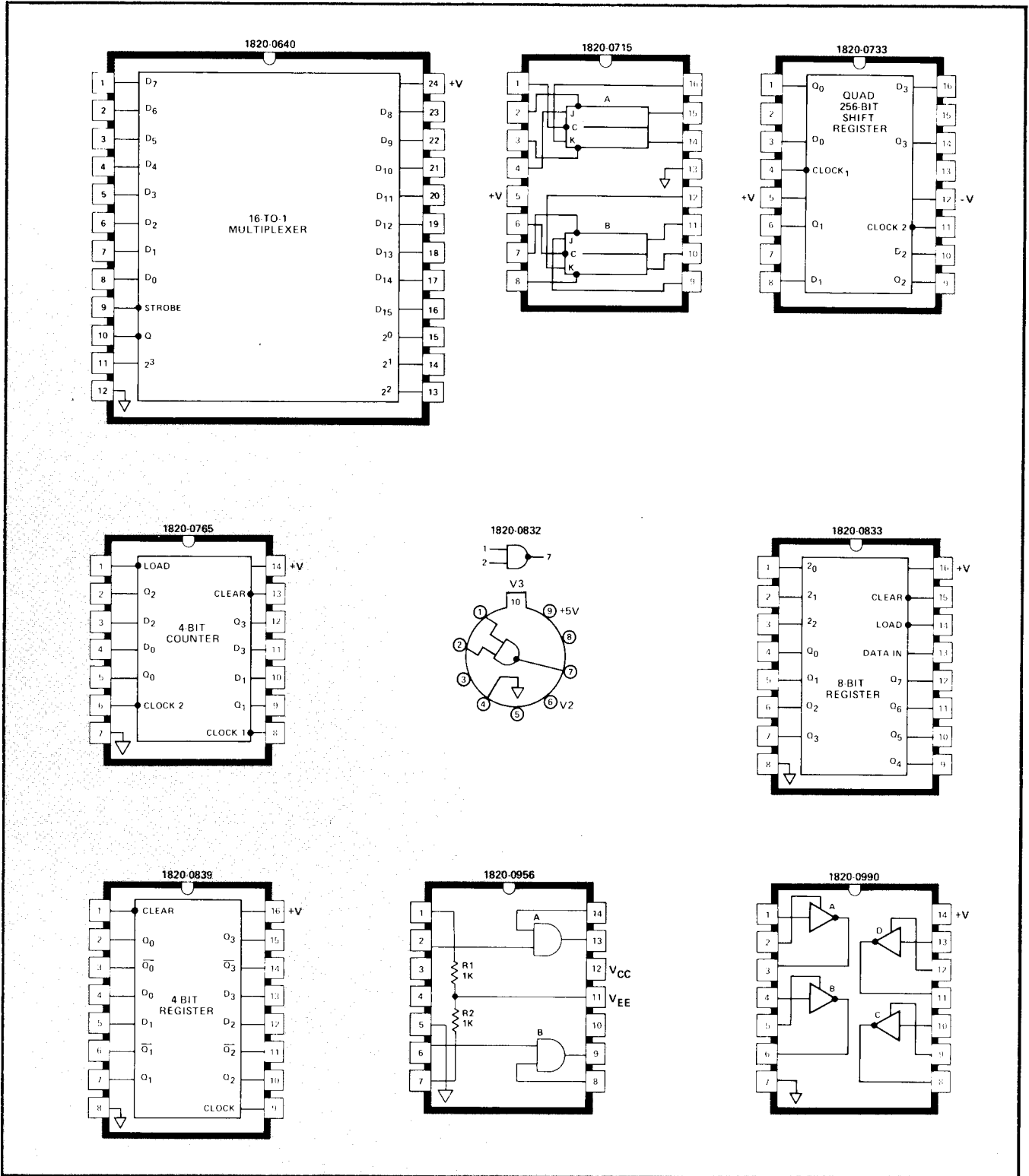
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Figure 5-1. Integrated Circuit Diagrams (Sheet 3 of 3)

Table 5-1. Asynchronous Multiplexer Data PCA, Upper Select Code (12921-60001), Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C14, C16 thru C20, C22 thru C25	12921-60001 0180-0291	Asynchronous Multiplexer Data PCA, Upper Select Code Capacitor, Fxd, Elect, 1.0 uF, 10%, 35 VDCW	28480 56289	12921-60001 150D105X9035A2-DYS
C15,21	0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192
C26 thru C35	0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 –20%, 100 VDCW	56289	C023F101F103ZS22-CDH
CR5,6	1902-0041	Diode, Breakdown, 5.11V, 5%	07910	CD 35622
R1	0683-1525	Resistor, Fxd, Comp, 1500 ohms, 5%, 1/4W	01121	CB1525
R2 thru R11, R14 thru R17,21,22	0757-0279	Resistor, Fxd, Met Flm, 3.16k ohms, 5%, 2W	28480	0698-3622
R12,13	0757-1094	Resistor, Fxd, Met Flm, 1.47k ohms, 1%, 1/8W	28480	0757-1094
R18,19,29,31	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R20,23	1810-0020	Resistor Network, Flm (7 resistor)	28480	1810-0020
R24,25	0757-0180	Resistor, Fxd, Met Flm, 3.16 ohms, 1%, 1/8W	28480	0757-0180
R26,27	0698-3407	Resistor, Fxd, Met Flm, 1.96k ohms, 1%, 1/2W	28480	0698-3407
R28,30	0757-0416	Resistor, Fxd, Met Flm, 511 ohms, 1%, 1/8W	28480	0757-0416
R32	0764-0013	Resistor, Fxd, Met Ox, 56 ohms, 5%, 2W	28480	0764-0013
U11,12,47,61	1820-0376	Integrated Circuit, TTL	01295	SN74H40N
U13,15,36,46,57	1820-0370	Integrated Circuit, TTL	01295	SN74H00N
U14,45	1820-0239	Integrated Circuit, TTL	04713	SC7527PK
U16,27,35,67	1820-0141	Integrated Circuit, TTL	04713	SC7514PK
U17,26	1820-0424	Integrated Circuit, TTL	04713	SN14751
U21,33,42	1820-0367	Integrated Circuit, TTL	01295	SN74H40N
U22,32,43,51,71, 81,83,101	1820-0839	Integrated Circuit, TTL	01295	SN35872
U23,31,41,52,62, 72,82,93,102	1820-0616	Integrated Circuit, TTL	07263	U78932259X
U25	1820-0205	Integrated Circuit, TTL	04713	SC7528PK
U37,56	1820-0371	Integrated Circuit, TTL	01295	SN74H10N
U53,63	1820-0733	Integrated Circuit, TTL	28480	1820-0733
U55,75,85,95, 104,105	1820-0301	Integrated Circuit, TTL	02195	SN74754
U65,106	1820-0435	Integrated Circuit, TTL	01295	SN74180N
U66	1820-0715	Integrated Circuit, Digital	01295	SN33S10
U73,92,103	1820-0231	Integrated Circuit, TTL	07263	U6B931659X
U76,77	1820-0377	Integrated Circuit, TTL	01295	SN74H50N
U86,87,96,97,107	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U108,109	1820-0832	Integrated Circuit, TTL	12040	SH15994

C28   + C1   hp 12921-60001   C27   C26   E1
                   A-1222-22

U11   U12   U13   U14   U15   U16   U17   C3
              E2   C2 +   C4 +

U21   U22   U23   U25   U26   U27   +
                                                    C7
                    + C5   R1
                    C29

U31   U32   U33   U35   U36   U37
                    R4
                    R5
E3   C8   R2   R6   C30   C10 +
      R3   R7
U41   U42   U43   R8   U45   U46   U47
                   R9
                         C31
R10   R11

U51   U52   U53   U55   U56   U57   R12
R14   R15   R13   R20
R16   R17   C33   C11 +
U61   U62   U63   R18   U65   U66   U67
                   R19
R21   E4   C12 +
R22
U71   U72   U73   U75   U76   U77
C13 +   C14 +
C15
R24   U81   U82   U83   U85   U86   U87
R30
R26   C16 +   C33   C17 +   R23
R27   C34
R28
U108
C25 + U91   U92   U93   U95   U96   U97
C18 +   C19 +   R29   C20 +
U109
C21   U101 U102 U103 U104 U105 U106 U107   + CR5 CR6
R25   R31   C22
            C23 +   C35   C24 +   E5   R32
                                          E5
                                          R32

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2176-12

U73 4-BIT COUNTER (BIT COUNT)
CARRY OUT CARRY IN
Q_3 Q_2 Q_1 Q_0 P_3 P_2 P_1 P_0
PARALLEL ENABLE CLEAR CLOCK LC

U83 4-BIT REGISTER (CHARACTER SIZE)
CLEAR CLOCK

U93 QUAD 2-BIT MULTIPLEXER (NEW CHARACTER SIZE)
Q_D Q_C Q_B Q_A D_2 D_3 D_0 D_1
C_1 C_2 B_1 B_2 A_2 A_1
SELECT ENABLE
IOBO 10 FF
IOBO 10 FF
IOBO 9 FF
IOBO 8 FF
CRS2

U103 4-BIT COUNTER (SAMPLE COUNT)
CARRY OUT CARRY IN
Q_3 Q_2 Q_1 Q_0 P_3 P_2 P_1 P_0
PARALLEL ENABLE COUNT CLEAR CLOCK
LC CRS 2

U102 QUAD 2-BIT MULTIPLEXER (DIVIDE BY 2)
Q_D Q_C Q_B Q_A D_1 D_2 C_1 C_2 B_1 B_2 A_1 A_2
SELECT ENABLE
R31 1K +4.85V

U101 4-BIT REGISTER (BAUD RATE)
Q_3 Q_2 Q_1 Q_0 D_2 D_3 D_0 D_1
CLEAR CLOCK
CRS2

U91 QUAD 2-BIT MULTIPLEXER (NEW BAUD RATE)
Q_D Q_C Q_B Q_A D_1 C_1 C_2 B_1 B_2 A_2 A_1
SELECT ENABLE
IOBO 7 FF
IOBO 6 FF
IOBO 5 FF
IOBO 4 FF

U92 4-BIT COUNTER (SAMPLE COUNT)
CARRY OUT CARRY IN
Q_3 Q_2 Q_1 Q_0 P_3 P_2 P_1 P_0
PARALLEL ENABLE COUNT CLEAR CLOCK
LC CRS 2

U82 QUAD 2-BIT MULTIPLEXER (DIVIDE BY 2)
Q_D Q_C Q_B Q_A D_1 C_1 C_2 B_1 B_2 A_2 A_1
SELECT ENABLE
CRS 3

U81 4-BIT REGISTER (BAUD RATE)
Q_3 Q_2 Q_1 Q_0 D_3 D_2 D_0 D_1
CLEAR CLOCK
CRS 3

U72 QUAD 2-BIT MULTIPLEXER (NEW BAUD RATE)
Q_D Q_C Q_B Q_A D_2 C_1 C_2 B_2 A_1
SELECT ENABLE
IOBO 3
IOBO 1
IOBO 0

U26C
ACTIVE

U32 4-BIT REGISTER (BUFFER)
Q_0 Q_1 Q_2 Q_3 D_3 D_2 D_1 D_0
SERIAL/SHIFT CLOCK CLEAR CLOCK
CRS 1

U31 QUAD 2-BIT MULTIPLEXER (NEW DATA OR ZERO)
Q_D Q_C Q_B Q_A D_2 D_0
C_2 C_1 B_2 B_1 A_1 A_2
SELECT ENABLE
IOBO 6 FF
IOBO 5 FF
IOBO 4 FF
IOBO 3 FF

U21 SERIAL IN 4-BIT SHIFT REGISTER (ACCUMULATE)
Q_0 Q_1 Q_2 Q_3 D_0 D_1
PARALLEL ENABLE PARALLEL CLOCK SERIAL/SHIFT CLOCK
CRS 1

U22 4-BIT REGISTER (BUFFER)
Q_3 Q_2 Q_1 Q_0 D_3 D_2 D_1 D_0
CLEAR CLOCK

U11A U13A DP LC
U27C LC U37B DP
U13C DP E2

RECEIVE START START
U56C DP
U45C DP
U16C
U57B
U16B U25D
U56A LC
U27D U26D
STOP

SHIFT
RIGHT JUSTIFY
U47A U17D U46A SHIFT BIT 0
U57A NOT JUSTIFIED U36D U17A
RECE

D_2 D_1 C_2 C_1 B_2 B_1 A_2 A_1
IOBO 2 FF
IOBO 1 FF
IOBO 0 FF
IOBO 11 FF
ENABLE

U14C DP
U13D DP E3

U36A DP U26F
PARAMETER
U12A U13B DP LC
PARAMETER LOAD

DATA U37A IOBO 15 FF
U36B IOBO 15 FF
PARAMETER

E4

TRANSFER

9A* 8A*
BIT 9 BIT 8

14B*
TRANSFER

10A*
SEND

Figure 5-2. Asynchronous Multiplexer Data PCA, Upper Select Code (12921-60001), Parts Location and Schematic Diagrams
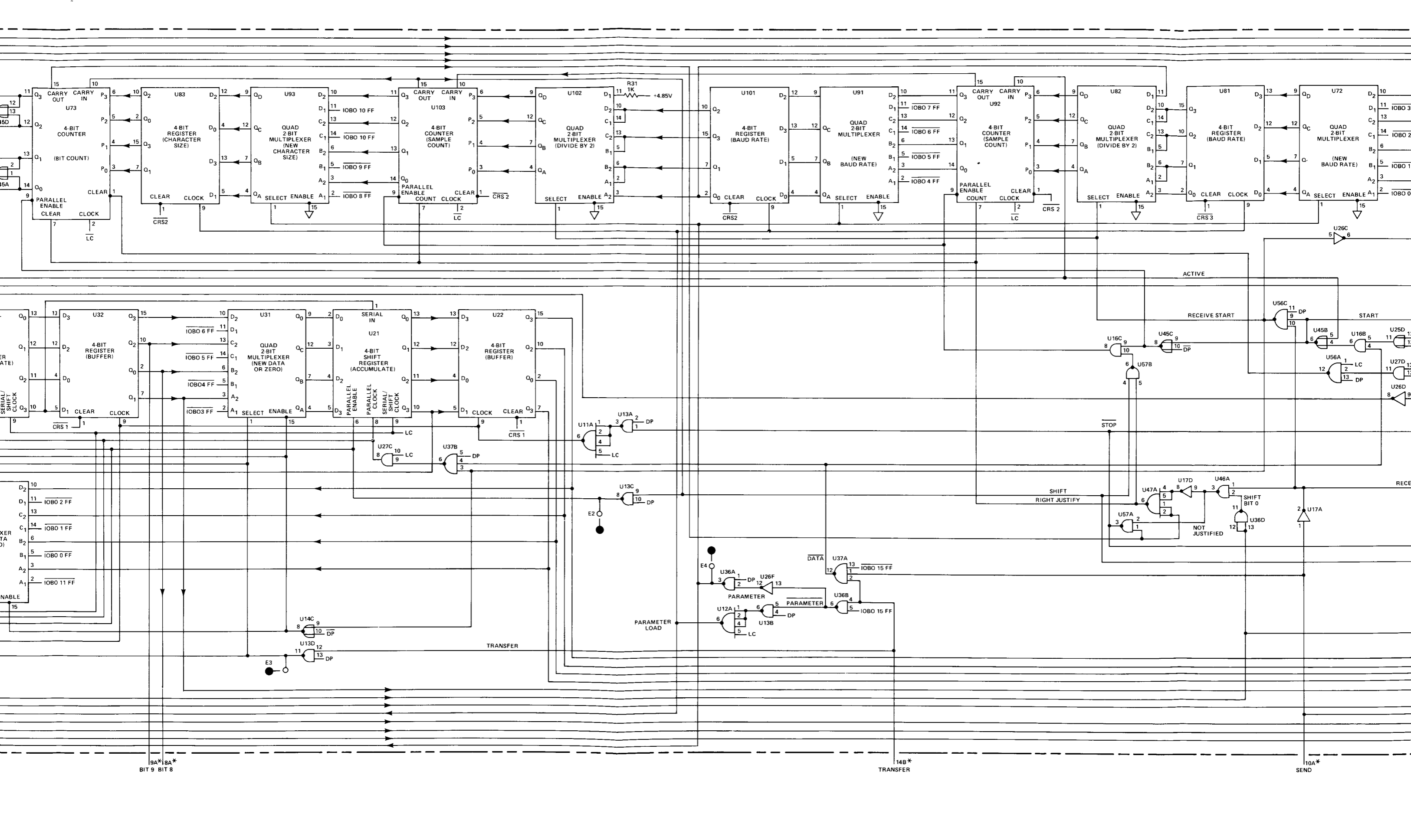
Table 5-2. Asynchronous Multiplexer Data PCA, Lower Select Code (12921-60002), Replaceable Parts

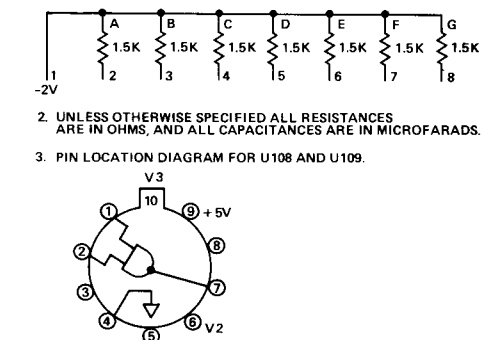| REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
	12921-60002	Asynchronous Multiplexer Data PCA, Lower Select Code	28480	12921-60002
C1★	0140-0198	Capacitor, Fxd, Mica, 200 pF, 5%	72136	RDM15F201J3C
C1■	0160-0939	Capacitor, Fxd, Mica, 430 pF, 5%	28480	0160-0939
C2 thru C5, C7 thru C10,18, C28 thru C30	0180-0291	Capacitor, Fxd, Elect, 1.0 uF, 10%, 35 VDCW	56289	150D105X9035A2-DYS
C6	0160-2307	Capacitor, Fxd, Mica, 47 pF, 5%	28480	0160-2307
C11 thru C17, C19 thru C27,C48■	0160-0938	Capacitor, Fxd, Mica, 1000 pF, 5%	72136	RDM15E102J1C
C31 thru C47	0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 –20%, 100 VDCW	56289	C023F101F103ZS22-CDH
CR1 thru CR6	1901-0159	Diode, Si, 0.75A, 400 PIV	04713	SR1358-4
R1,2	0683-1825	Resistor, Fxd, Comp, 1800 ohms, 5%, 1/4W	01121	CB1825
R3,4	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025
R5	0698-3445	Resistor, Fxd, Met Flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R6	0698-3440	Resistor, Fxd, Met Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R7,9,10,14	1810-0020	Resistor Network, Flm, (7 resistor)	28480	1810-0020
R8	0757-0279	Resistor, Fxd, Met Flm, 3.16k ohms, 1%, 1/8W	28480	0757-0279
R11	0683-1215	Resistor, Fxd, Comp, 120 ohms, 5%, 1/4W	01121	CB1215
R12,13	0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4W	01121	CB1015
R15,17	0757-0799	Resistor, Fxd, Met Flm, 121 ohms, 1%, 1/2W	28480	0757-0799
R16	0698-3102	Resistor, Fxd, Met Flm, 237 ohms, 1%, 1/2W	28480	0698-3102
U12	1820-0127	Integrated Circuit, TTL	02763	U6A900259X
U13,14,16,34, 36,64,117	1820-0370	Integrated Circuit, TTL	01295	SN74H00N
U15,26,44	1820-0371	Integrated Circuit, TTL	01295	SN74H10N
U17,27,37,47,57, 66,67,75,77, 97,107	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U22	1820-0261	Integrated Circuit, TTL	01295	SN7412N
U23*	1820-0076	Integrated Circuit, Digital	01295	SN7476N
U24	1820-0373	Integrated Circuit, TTL	01295	SN74H20N
U25,61	1820-0376	Integrated Circuit, TTL	01295	SN74H40N
U31,35,86	1820-0141	Integrated Circuit, TTL	04713	SC7514PK
U32,106	1820-0077	Integrated Circuit, TTL	01295	SN7474N
U41,46,65	1820-0424	Integrated Circuit, TTL	04713	SN14751
U42	1820-0377	Integrated Circuit, TTL	01295	SN74H50N
U43,95	1820-0231	Integrated Circuit, TTL	07263	U6B931659X
U45,55,63,73, 83,84,87,96	1820-0301	Integrated Circuit, TTL	01295	SN74754
U51,56	1820-0140	Integrated Circuit, TTL	04713	SC7513PK
U53,74	1820-0294	Integrated Circuit, TTL	12040	SD9935
U54	1820-0715	Integrated Circuit, Digital	01295	SN74H106N
U62,72,82,92	1820-0509	Integrated Circuit, DTL	04713	MC1488L
U76	1820-0328	Integrated Circuit, TTL	04713	SN7402N
U85	1820-0250	Integrated Circuit, TTL	28480	1820-0250
U93,94,102,103	1820-0990	Integrated Circuit, DTL	04713	SC24504LK
U105	1820-0640	Integrated Circuit, TTL	01295	SN74150N
U116**	1820-0069	Integrated Circuit, TTL	01295	SN7420N
W1	8159-0005	Jumper Wire	28480	8159-0005
XY1	1200-0199	Socket Crystal	20940	R7-100
Y1	0410-0459	Crystal, 4.320 MHz, ±0.002%, 25°C	28480	0410-0459

* On series 1203 assemblies, same as U54 (1820-0715)   ★ 0140-0198 used on series 1203 and 1215 assemblies.
** On series 1203 assemblies, same as U24 (1820-0373)   ■ C1 part no. 0160-0939 and C48 first used on series 1229 assemblies.

12921-60002
C-1229-22

NOTE: C48 NOT USED ON A-1203-22 AND B-1215-22 ASSEMBLIES.
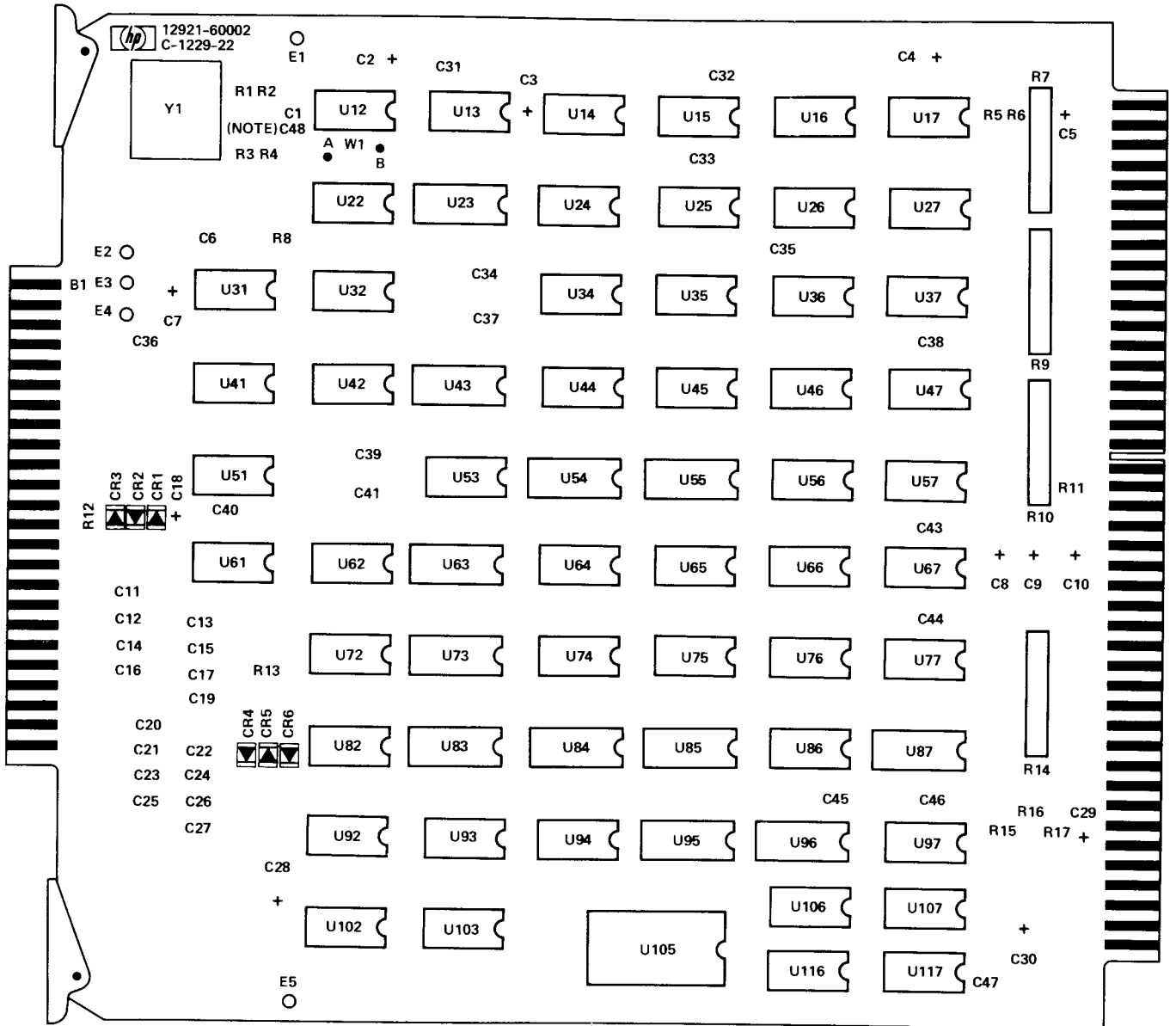
ASYNCHRONOUS MULTIPLEXER DATA · LOWER SELECT CODE (12921-60002, SERIES 1203, 1215, 1229)

Figure 5-3. Asynchronous Multiplexer Data PCA,
Lower Select Code (12921-60002), Parts Location
and Schematic Diagrams

Table 5-3. Asynchronous Multiplexer Control PCA (12922-60001), Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C101	0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 -20%, 100 VDCW	56289	C023F101F103ZS22-CDH
CR1 thru CR6	1901-0159	Diode, Si, 0.75A, 400 PIV	04713	SZ10939-122
R1,17	0698-3440	Resistor, Fxd, Met Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R2,R11 thru R16, 18,19	0757-0280	Resistor, Fxd, Flm, 1k ohm, 1%, 1/8W	28480	0757-0280
R3	0698-3445	Resistor, Fxd, Met Flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R4	0698-3440	Resistor, Fxd, Met Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R5,6,9,10	1810-0020	Resistor, Network, Flm (7 resistor)	28480	1810-0020
R7,8	0757-1094	Resistor, Fxd, Met Flm, 1.47k ohms, 1%, 1/8W	28480	0757-1094
U11,12,21,22, 91,92,101,102	1820-0509	Integrated Circuit, DTL	04713	MC1488L
U13,23,93,103	1820-0833	Integrated Circuit, TTL	07263	SL18556
U15,25,35	1820-0068	Integrated Circuit, TTL	12040	SN7410N
U16,26,36,46,75	1820-0054	Integrated Circuit, TTL	01295	SN74004
U17,27,37,47,57, 67,87,97,107	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U31,32,41,42, 71,72,81,82	1820-0990	Integrated Circuit, DTL	04713	SC24504LK
U33,43,96	1820-0205	Integrated Circuit, TTL	04713	SC7528PK
U45,65	1820-0069	Integrated Circuit, TTL	01295	SN7420N
U51,53	1820-0640	Integrated Circuit, TTL	01295	SN74150N
U56,83,86	1820-0174	Integrated Circuit, TTL	01295	SN7404N
U66,73,77	1820-0765	Integrated Circuit, TTL	01295	SN74197N
U76	1820-0628	Integrated Circuit, TTL	28480	1820-0628
U85	1820-0512	Integrated Circuit, TTL	01295	SN74H74N
U95	1820-0282	Integrated Circuit, TTL	01295	SN7486N

E1

C3 C4 C5 C6 C7   C8 C9   C10 C11 C12

C1 C2

+ C13

CR2

C14 +   C15 +   C16 +

U11   U12   U13   C18   R1   U15   U16   U17

C17

CR3

R5 R6

C19   C20   C21   R2   C22   R3   C23   R4

U21   U22   U23   C24   U25   U26   U27

C25   C26   C27   C28   C29 C30 C31 C34 C35   C32   C33

U31   U32   U33   U35   U36   U37

C36   C37   C38   C41 C42 C43   C39   C40

U41   U42   U43   U45   U46   U47   R7

C44   C45   C46   C47   C48

U56   U57

U51   U53   C50   C51

C49   U65   U66   U67   R8

C54

C52   C53   C55   C56   C57

C58   U71   U72   U73   C59   U75   U76   U77

C60   C61   C62   C63   C64 C65 C66   C67   C68   R11   R9 R10

U81   U82   U83   U85   U86   U87

C69   C70   C71   C72   C73 +   C74   C75   + C101

U91   U92   U93   C77   U95   U96   U97

C76

R12   + C78   C79   C80

C81 C82   U101   U102   U103   C83   CR4   R13 R15 R18   R14 R16 R19   U107

CR5

C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96   C97 +   CR6

R17

C98 +   C99 +   C100 +

E2

12922-60001
A-1220-22

DWG. REV. C
2176-13

ASYNCHRONOUS MULTIPLEXER CONTROL (12922-60001, SERIES 1220)
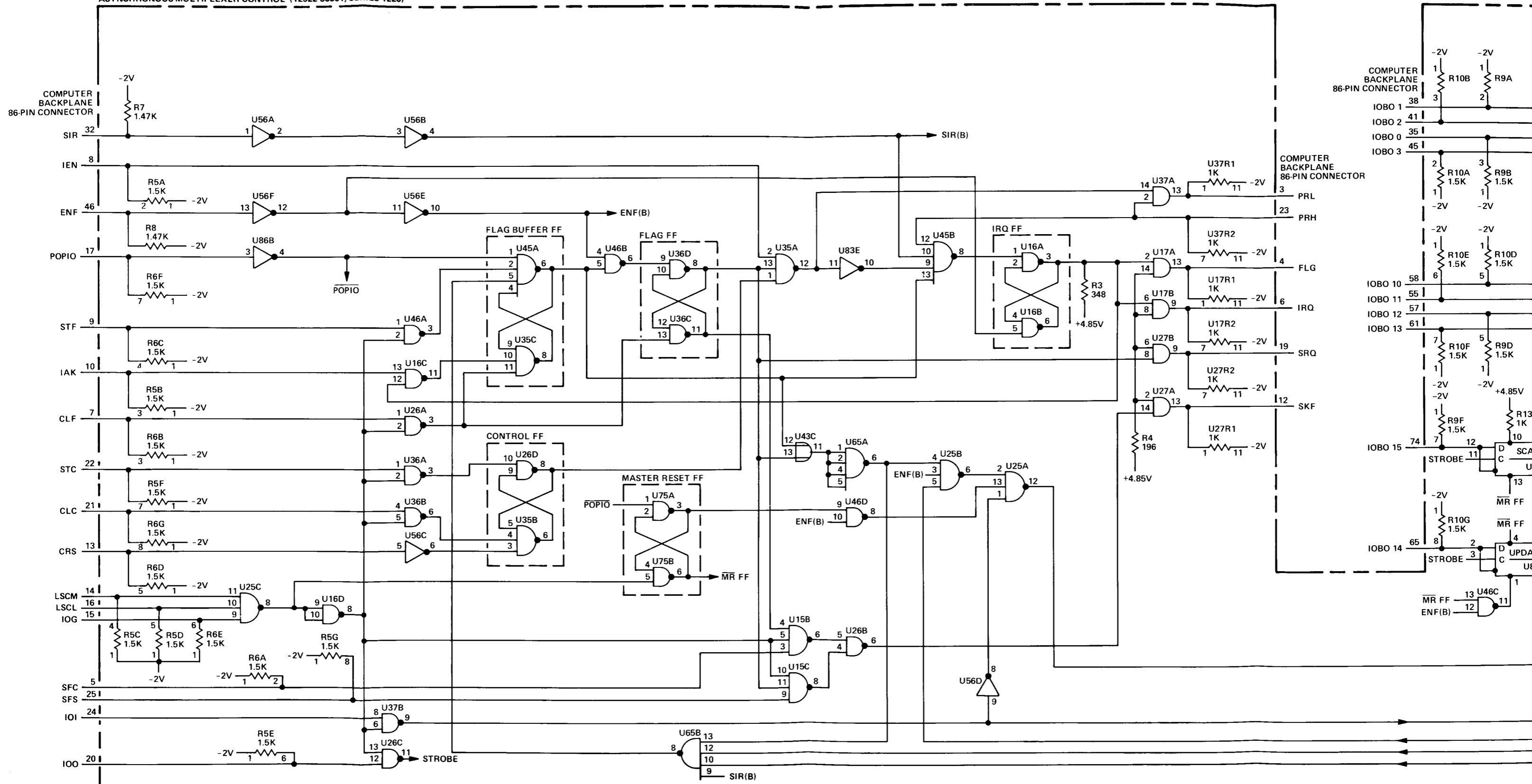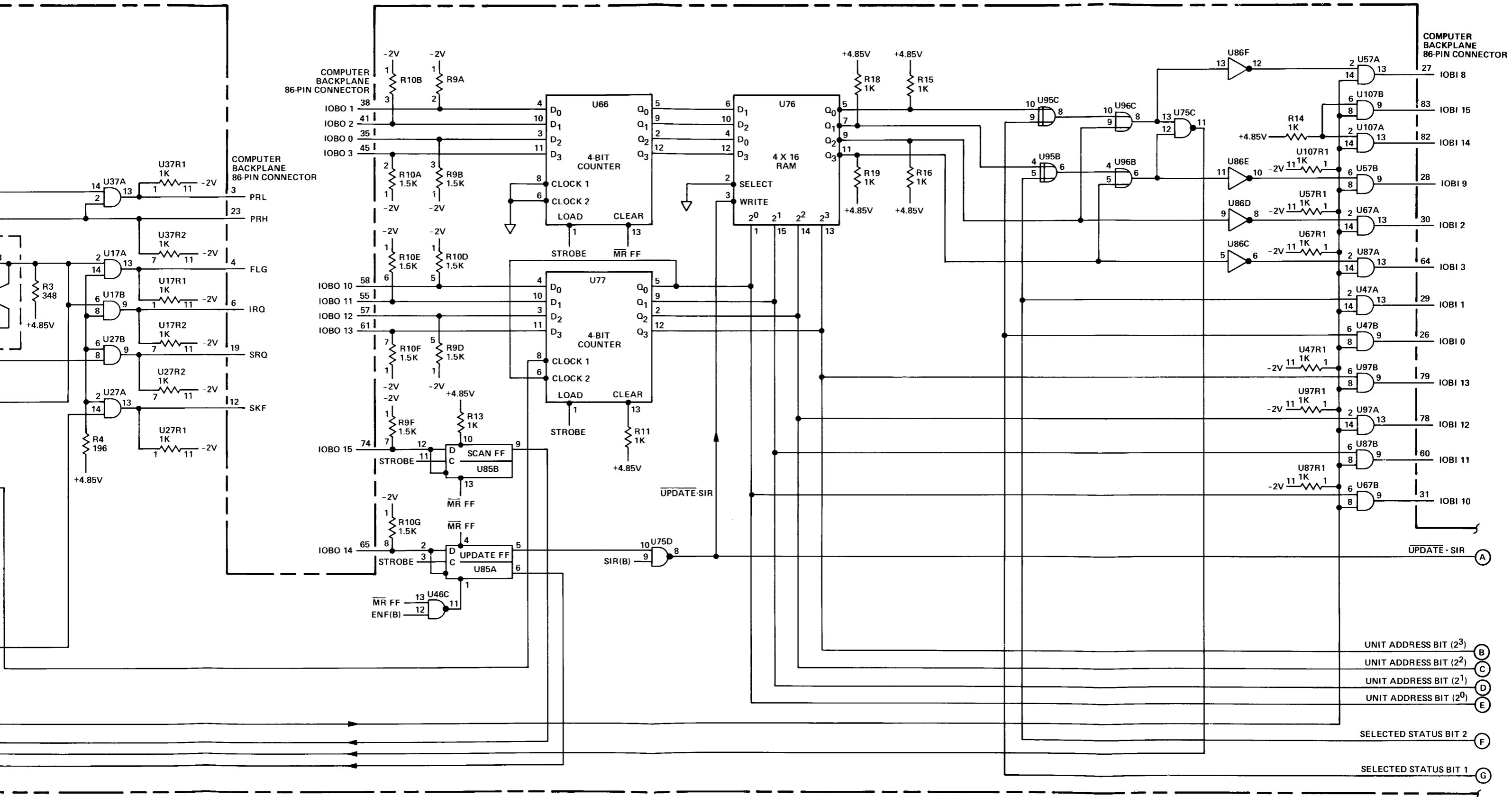
2176-16B (SHEET 1 OF 2) SEE SHEET 2 FOR NOTES.

Figure 5-4. Asynchronous Multiplexer Control PCA,
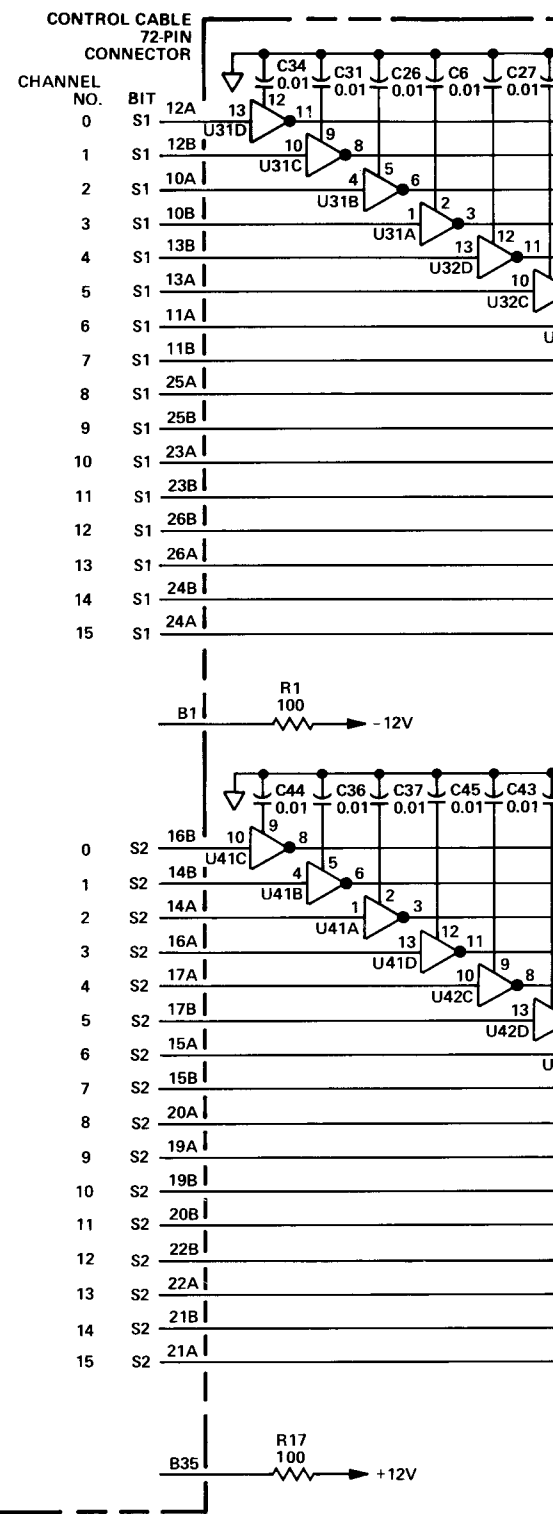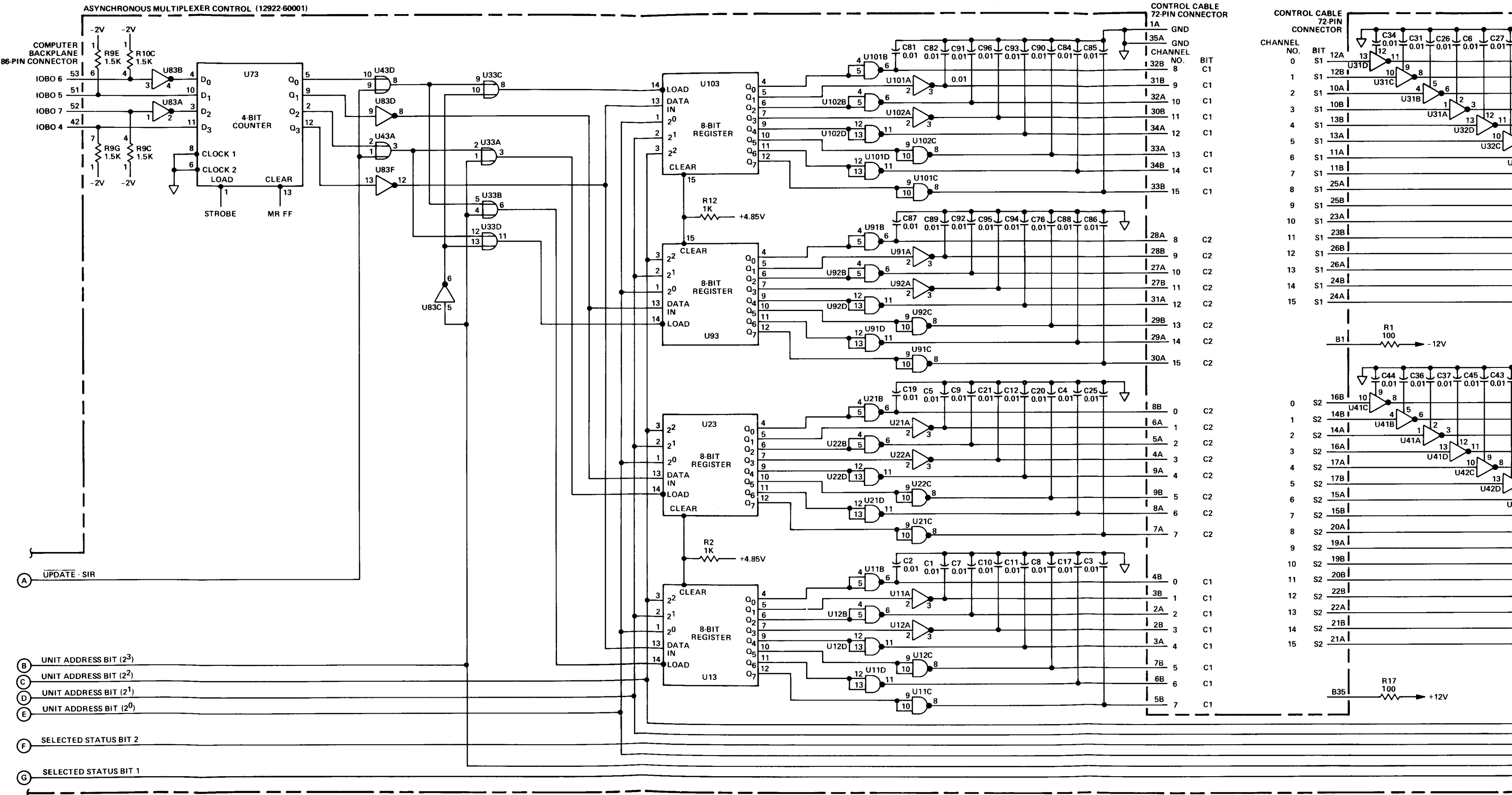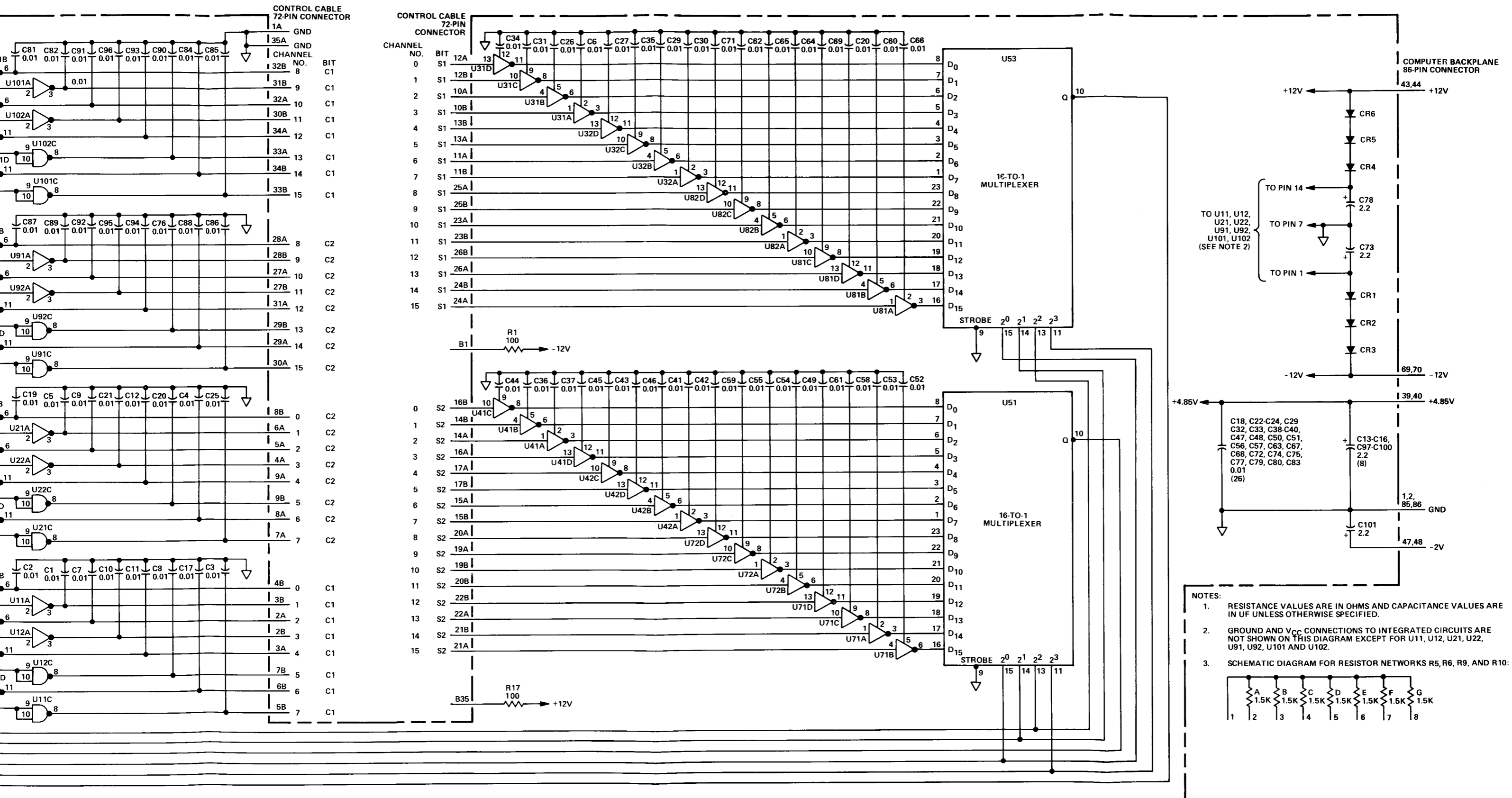(12922-60001), Parts Location and
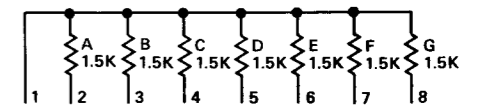Schematic Diagrams (Sheet 1 of 2)

Figure 5-4. Asynchronous Multiplexer Control PCA,
(12922-60001), Parts Location and
Schematic Diagrams (Sheet 2 of 2)

REPLACEABLE PARTS VI

6-1. INTRODUCTION.

6-2.   This section provides information for ordering replacement parts for the HP 12920A and optional 12920A-001 Asynchronous Multiplexer Interface Kits.

6-3. INTERFACE KIT PARTS.

6-4.   Table 6-1 lists the major parts of the interface kits in numerical order of part numbers and gives the total quantity for each part. Attaching parts for the connector panel are listed near the end of table 6-1.

6-5. CONNECTOR PANEL PARTS.

6-6.   A breakdown of the parts comprising the connector panel is listed in table 6-2 by order of index number. The parts are referenced to the exploded view in figure 6-1 by the index numbers which are in the order of disassembly, except for attaching parts which are indexed immediately after the parts they attach.

6-7.   Items in the DESCRIPTION column of table 6-2 are indented to indicate item relationship. In addition, the symbol "— — — x — — —" follows the last of one or more attaching parts. Indention is as follows:

MAJOR ASSEMBLY
* Subassembly
* Attaching Parts for Subassembly
** Subassembly Parts
** Attaching Parts for Subassembly Parts

6-8.   The columns in table 6-2 provide the following information for each part:

a.   FIG. & INDEX NO. The figure and index number of the replaceable parts as shown in the exploded view.

b.   HP PART NO. The HP part number for each replaceable part.

c.   DESCRIPTION. The description of each replaceable part. Refer to table 6-5 for an explanation of abbreviations used in the DESCRIPTION column.

Table 6-1. Asynchronous Multiplexer Interface Kit (12920A and 12920A-001),
Numerical Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
12921-60001	Asynchronous Multiplexer Data PCA, Upper Select Code	28480	12621-60001	1
12921-60002	Asynchronous Multiplexer Data PCA, Lower Select Code	28480	12921-60002	1
12921-60003	Asynchronous Multiplexer Data Cable Assembly	28480	12921-60003	1
12922-60001	Asynchronous Multiplexer Control PCA (NOTE 1)	28480	12922-60001	1
12922-60003	Asynchronous Multiplexer Control Cable (NOTE 1)	28480	12922-60003	1
30062-60002	Terminal Controller/Multiplexer Connector Panel	28480	30062-60002	1
	(Attaching Parts for Standard Mounting)			
2680-0106	* Screw, Machine, FH, No. 10-32, 5/8 in.	00000	OBD	8
3050-0007	* Washer, Cup, No. 10	00000	OBD	8
3050-0248	* Washer, Nylon, Cup Filler, No. 10	00000	OBD	8
	— — — x — — —			
	(Attaching Parts for Special Bracket Mounting)			
0590-0079	* Nut, Channel, 1/4-20, for 1-5/8 in. channel	00000	OBD	4
2190-0032	* Washer, Lock, split, 1/4 in. ID	00000	OBD	8
0570-0108	* Bolt, Machine, Hexagon Head, 1/4-20, 3/4 in.	00000	OBD	8
2950-0004	* Nut, Plain, Hexagon, 1/4-20	00000	OBD	4
30062-00002	* Bracket, Connector Panel Mounting	28480	30062-00002	2
	— — — x — — —			
30062-60003	Asynchronous Multiplexer Test Cable	28480	30062-60003	1

NOTES:

1. All parts listed are part of the 12920A multiplexer; the optional 12920A-001 multiplexer contains only part no. 12922-60001 and 12922-60003.
2. Parts contained on interface printed-circuit assemblies are listed in section V.
3. Manufacturer's code 28480 is for Hewlett-Packard Company, Palo Alto, California.

d. MFR CODE. A five digit code that denotes a typical manufacturer of the part. Refer to table 6-6 for a list of manufacturers.

e. MFR PART NO. The manufacturer's part number for each replaceable part.

f. UNITS PER ASSY. The total quantity of each part used in the assembly or subassembly to which it belongs.

6-9. NUMERICAL LISTS.

6-10. Every replaceable part for the interface kit is listed by electrical or mechanical usage in tables 6-3 and 6-4, respectively. Table entries are in numerical order by HP part number.

6-11. The DESCRIPTION column and MFR CODE column of the tables use abbreviations and five digit codes, respectively. The abbreviations used in the description column are explained in table 6-5, and the five digit codes used in the MFR CODE column are explained in table 6-6.

6-12. PCA PARTS LISTS.

6-13. A separate replaceable parts table and separate parts location diagrams are provided for interface printed-circuit assemblies. These are located in section V of this manual, preceding the appropriate schematic diagram.

6-14. The parts tables in section V contain the same information as the numerical lists in tables 6-3 and 6-4 except that total quantities are not listed. The parts are listed in order of reference designation in the tables in section V.

6-15. ORDERING INFORMATION.

6-16. To order replacement parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. Specify the following information for each part ordered:

a. Identification of the instrument, kit, or assembly containing the part.

b. Hewlett-Packard part number for each part.

c. Description of each part.

d. Circuit reference designation for each part (if applicable).

Table 6-2. Terminal Controller/Multiplexer Connector Panel, Replaceable Parts

FIG & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
6-1-	30062-60002	Terminal Controller/Multiplexer Connector Panel	28480	30062-60002	1
1	30062-60001	* Printed Circuit Connector Panel (Attaching Parts)	28480	30062-60001	1
2	1251-2294	* Spacer, Threaded, male and female, No. 4-40, 3/8 in.	00000	OBD	32
3	2200-0139	* Screw, Machine, PH, No. 4-40, 1/4 in.	00000	OBD	8
	2190-0003	* Washer, Lock, split, No. 4	00000	OBD	8
		— — — x — — —			
4	1251-2416	** Connector, 25 pin	28480	1251-2416	16
5	0380-0334	** Spacer, No. 4-40, 3/8 in.	00000	OBD	2
6	1251-2935	** Connector, 50 pin (Attaching Parts)	74868	57-40500-9	5
7	0520-0128	** Screw, Machine, PH, No. 2-56, 1/4 in.	00000	OBD	2
8	2190-0045	** Washer, Lock, split, No. 2	00000	OBD	2
9	0380-1034	** Spacer, No. 2-56, 7/16 in.	00000	OBD	2
		— — — x — — —			
10	30062-80001	** Board, Etched, PC	28480	30062-80001	1
11	30062-00001	* Connector Panel Frame	28480	30062-00001	1
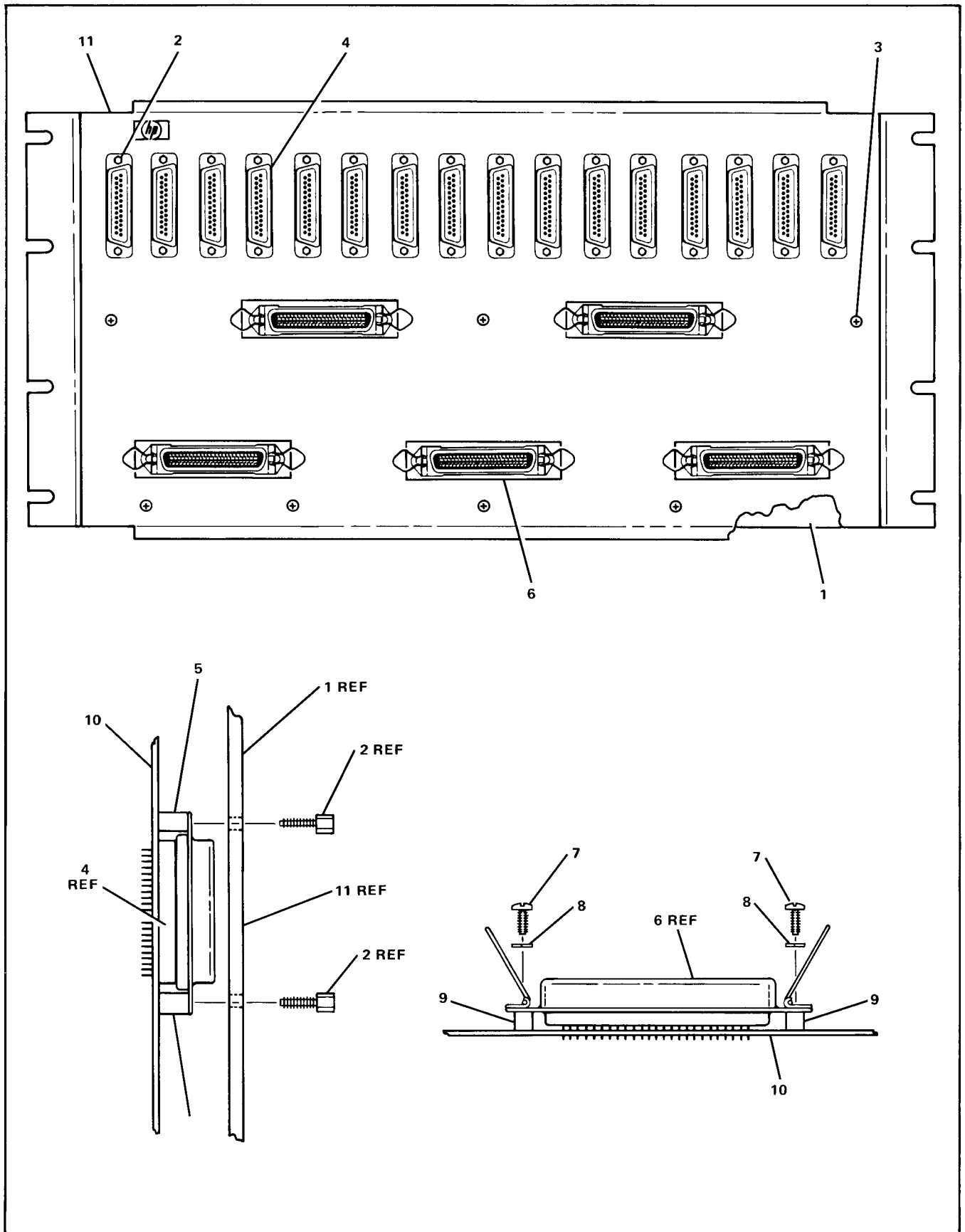
Figure 6-1. Terminal Controller/Multiplexer Connector Panel, Exploded View

Table 6-3. Numerical Listing of Electrical Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0140-0192	Capacitor, Fxd, Mica, 68 pF, 5%	28480	0140-0192	2
0140-0198	Capacitor, Fxd, Mica, 200 pF, 5%	72136	RDM 15F201J1C	1
0160-0938	Capacitor, Fxd, Mica, 1000 pF, 5%	72136	RDM15E102J1C	16
0160-2055	Capacitor, Fxd, Cer, 0.01 uF, +80 –20%, 100 VDCW	56289	C023F101F103ZS22-CDH	117
0160-2307	Capacitor, Fxd, Mica, 47 pF, 5%	28480	0160-2307	1
0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	56289	150D225X902A2-DYS	11
0180-0291	Capacitor, Fxd, Elect, 1.0 uF, 10%, 35 VDCW	56289	150D105X9035A2-DYS	35
0410-0459	Crystal, 4.320 MHz, ±0.002%, 25°C	28480	0410-0459	1
0683-1015	Resistor, Fxd, Comp, 100 ohms, 5%, 1/4W	01121	CB1015	4
0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4W	01121	CB1025	6
0683-1215	Resistor, Fxd, Comp, 120 ohms, 5%, 1/4W	01121	CB1215	1
0683-1525	Resistor, Fxd, Comp, 1500 ohms, 5%, 1/4W	01121	CB1525	1
0683-1825	Resistor, Fxd, Comp, 1800 ohms, 5%, 1/4W	01121	CB1825	2
0698-3102	Resistor, Fxd, Met Flm, 237 ohms, 1%, 1/2W	28480	0698-3102	1
0698-3407	Resistor, Fxd, Met Flm, 1.96k ohms, 1%, 1/2W	28480	0698-3407	2
0698-3440	Resistor, Fxd, Met Flm, 196 ohms, 1%, 1/8W	28480	0698-3440	2
0698-3445	Resistor, Fxd, Met Flm, 348 ohms, 1%, 1/8W	28480	0698-3445	2
0757-0180	Resistor, Fxd, Met Flm, 31.6 ohms, 1%, 1/8W	28480	0757-0180	2
0757-0279	Resistor, Fxd, Met Flm, 3.16k ohms, 1%, 1/8W	28480	0757-0279	17
0757-0280	Resistor, Fxd, Flm, 1k ohm, 1%, 1/8W	28480	0757-0280	9
0757-0416	Resistor, Fxd, Met Flm, 511 ohms, 1%, 1/8W	28480	0757-0416	2
0757-0799	Resistor, Fxd, Met Flm, 121 ohms, 1%, 1/2W	28480	0757-0799	2
0757-1094	Resistor, Fxd, Met Flm, 1.47k ohms, 1%, 1/8W	28480	0757-1094	4
0764-0013	Resistor, Fxd, Met Ox, 56 ohms, 5%, 2W	28480	0764-0013	1
1200-0199	Socket, Crystal	20940	R7-100	1
1251-2416	Connector, 25 pin	28480	1251-2416	16
1251-2935	Connector, 50 pin	74868	57-40500-9	5
1810-0020	Resistor Network, Flm (7 resistor)	28480	1810-0020	60
1820-0054	Integrated Circuit, TTL	01295	SN7400N	5
1820-0068	Integrated Circuit, TTL	12040	SN7410N	3
1820-0069	Integrated Circuit, TTL	01295	SN7420N	3 (2)
1820-0077	Integrated Circuit, TTL	01295	SN7474N	2
1820-0127	Integrated Circuit, TTL	02763	U6A900259X	1
1820-0140	Integrated Circuit, TTL	04713	SC7513PK	2
1820-0141	Integrated Circuit, TTL	04713	SC7514PK	7
1820-0174	Integrated Circuit, TTL	01295	SN7404N	3
1820-0205	Integrated Circuit, TTL	04713	SC7528PK	4
1820-0231	Integrated Circuit, TTL	07263	U6B931659X	5
1820-0239	Integrated Circuit, TTL	04713	SC7527PK	2
1820-0250	Integrated Circuit, TTL	28480	1820-0250	1
1820-0261	Integrated Circuit, TTL	01295	SN7412N	1
1820-0282	Integrated Circuit, TTL	01295	SN7486N	1
1820-0294	Integrated Circuit, TTL	12040	SD9935	2
1820-0301	Integrated Circuit, TTL	01295	SN7475N	14
1820-0328	Integrated Circuit, TTL	04713	SN7402N	8
1820-0367	Integrated Circuit, TTL	01295	SN7495N	3
1820-0370	Integrated Circuit, TTL	01295	SN74H00N	12
1820-0371	Integrated Circuit, TTL	01295	SN74H10N	5
1820-0373	Integrated Circuit, TTL	01295	SN74H20N	1 (2)
1820-0376	Integrated Circuit, TTL	01295	SN74H40N	6
1820-0377	Integrated Circuit, TTL	01295	SN74H50N	3
1820-0424	Integrated Circuit, TTL	04713	SN14751	5
1820-0435	Integrated Circuit, TTL	01295	SN74180N	2
1820-0494	Integrated Circuit, TTL	28480	1820-0494	1
1820-0509	Integrated Circuit, DTL	04713	MC1488L	12
1820-0512	Integrated Circuit, TTL	01295	SN74H74N	1
1820-0616	Integrated Circuit, TTL	07263	U7B932259X	10
1820-0640	Integrated Circuit, TTL	01295	SN74150N	3
1820-0715	Integrated Circuit, Digital	01295	SN74H106N	3
1820-0733	Integrated Circuit	28480	1820-0733	2 (3)
1820-0765	Integrated Circuit, TTL	01295	SN74197N	3
1820-0076	Integrated Circuit, Digital	01295	SN7476N	1 (0)

Table 6-3. Numerical Listing of Electrical Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
1820-0832	Integrated Circuit, TTL	12040	SH15994	2
1820-0833	Integrated Circuit, TTL	07263	SL18556	4
1820-0839	Integrated Circuit, TTL	01295	SN35872	8
1820-0956	Integrated Circuit, CTL	07263	U6A995679X	25
1820-0990	Integrated Circuit, DTL	04713	SC24504LK	12
1901-0159	Diode, Si, 0.75A, 400 PIV	04713	SR1358-4	12
1902-0049	Diode, Breakdown, 6.19V, 5%	04713	SZ10939-122	2
8159-0005	Jumper Wire	28480	8159-0005	1
12921-60001	Asynchronous Multiplexer Data PCA, Upper Select Code	28480	12921-60001	1
12921-60002	Asynchronous Multiplexer Data PCA, Lower Select Code	28480	12921-60002	1
12921-60003	Asynchronous Multiplexer Data Cable Assembly	28480	12921-60003	1
12922-60001	Asynchronous Multiplexer Control PCA	28480	12922-60001	1
12922-60003	Asynchronous Multiplexer Control Cable	28480	12922-60003	1
30062-60002	Asynchronous Multiplexer Connector Panel	28480	30062-60002	1
30062-60003	Asynchronous Multiplexer Test Cable	28480	30062-60003	1
30062-80001	Board, Etched	28480	30062-80001	1

NOTE: If card 12921-60002, series 1203 is supplied, use TQ numbers in parentheses ( ).

Table 6-4. Numerical Listing of Mechanical Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0380-0334	Spacer, No. 4-40, 3/8 in.	00000	OBD	32
0380-1034	Spacer, No. 2-56, 7/16 in.	00000	OBD	10
0520-0128	Screw, Machine, PH, No. 2-56, 1/4 in.	00000	OBD	10
0570-0108	Bolt, Machine, Hexagon Head, 1/4-20, 3/4 in.	00000	OBD	8
0590-0079	Nut, Channel, 1/4-20, for 1-5/8 in channel	00000	OBD	4
1251-2294	Spacer, Threaded, male and female, No. 4-40, 3/8 in.	00000	OBD	32
2190-0003	Washer, Lock, split, No. 4	00000	OBD	8
2190-0032	Washer, Lock, split, 1/4 in. ID	00000	OBD	8
2190-0045	Washer, Lock, split, No. 2	00000	OBD	10
2200-0139	Screw, Machine, PH, No. 4-40, 1/4 in.	00000	OBD	8
2680-0106	Screw, Machine, FH, No. 10-32, 5/8 in.	00000	OBD	8
2950-0004	Nut, Plain, Hexagon, 1/4-20	00000	OBD	4
3050-0007	Washer, Cup, No. 10	00000	OBD	8
3050-0248	Washer, Nylon, Cup Filler, No. 10	00000	OBD	8
30062-00001	Panel, Connector	28480	30062-00001	1
30062-00002	Bracket, Connector Panel Mounting	28480	30062-00002	2

HEWLETT **hp** *PACKARD*

PAPER TAPE NO. 12920-16001
AND NO. 12920-16002

12920 A/B
ASYNCHRONOUS MULTIPLEXER
INTERFACE DIAGNOSTIC

for

hp 2100 SERIES COMPUTERS

reference manual

HEWLETT hp *PACKARD*

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

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Section I

INTRODUCTION

1-1. GENERAL

This diagnostic test program confirms proper operation of the HP 12920A or 12920B
Asynchronous Multiplexer Interface. The basic I/O portion of the cards which
includes the Flag and Control circuits will be tested. The status, control, re-
ceive and transmit features will be tested. This testing will use the test
cable(s) in conjunction with the communications multiplexer panel.

Two absolute binary tapes are used to test the data and control boards. Binary
tape number 12920-16001 tests the data boards. Binary tape number 12920-16002
tests the control board.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. HP 2100 series computer with a minimum 4K memory.
b. An HP 12920B Asynchronous Multiplexer Interface consisting of:
       (1) 12920-60001 Upper Select Code Data Board
       (1) 12920-60002 Lower Select Code Data Board
       (1) 12922-60001 Control Board
    or an HP 12920A Asynchronous Multiplexer consisting of:
       (1) 12921-60001 Upper Select Code Data Board
       (1) 12921-60002 Lower Select Code Data Board
       (1) 12922-60001 Control Board
c. A test cable (HP 30062-60003).
d. A communication multiplexer panel (30062-60002).
e. A console teleprinter device for message reporting (recommended but not
   required).
f. A paper tape reading device (for loading only).

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator Product No. 24296 used for equipment configuration
   and as a console device driver. The product includes the following part no.:
       Binary object tape   Part No. 24296-60001
       Manual   Part No. 02100-90157
b. HP 12920 Async. Mux. Diagnostic binary object tape, Part Nos. 12920-16001
   and 12920-16002.

The Diagnostic serial number (DSN) is contained in memory location 126_8 of the
program. The DSN for the Data Board is 103010_8 and the DSN for the Control Board
is 103011_8.

Section II

PROGRAM ORGANIZATION

2-1.   ORGANIZATION

This diagnostic program is divided into two absolute binary tapes: (1) 12920
Data Board Tape, consisting of eight tests; (2) 12922 Control Board Tape, con-
sisting of six tests.

Each tape has a control and an initialization section which prepares the diagnostic
by accepting the select code and options required by the tests. In addition to
that, each tape has a basic I/O test which consists of seven subtests.

The Data Board tape includes tests which verify the operation of the send and re-
ceive data paths along with BREAK, PARITY, DIAGNOSE, ECHO, SYNC and CHARACTER
LOST circuits.

The Control Board tape includes tests on the ADDRESS REGISTER, COMMAND, STATUS,
COMMAND REGISTER ADDRESSING, STATUS INTERRUPT and SCAN circuits.

These tests are called into execution by the control section as sequential or
selectable subroutines.

2-2.   TEST CONTROL AND EXECUTION

The program outputs a title message to the console device if present for operator
information then executes the tests according to the options selected on the
switch register by the operator. The control section mainly checks switch
register bits 15, 13 and 12.

The control also keeps count of the number of passes that have been completed
and will output the pass count at the completion of each pass (if switch register
bit 10 is clear). The count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User
selection or default will determine which test sections will be executed. (See
2-3 of PROGRAM ORGANIZATION.)

2-3.   SELECTION OF TESTS BY OPERATOR

The operator has the capability to select his own tests or sequence of tests
with the help of bit 9 in the switch register. Paragraph 3-4 outlines the test
selection.

2-4.   MESSAGE REPORTING

There are two types of messages, error and information. Error messages are used
to inform the operator of a failure of the card to respond to a given control
or sequence. Information messages are used to inform the operator of the progress

of the diagnostic or instruct the operator to perform some operation related to the interface's function. In this case an associated halt will occur to allow the operator time to perform the function, the operator must then press RUN.

If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available.

Example - Error with halt
Message: EØ16 CLC CH ERROR
Halt Code: $1Ø2Ø16_8$ (T or Memory Data Register)

Example - Information with halt
Message: HØ24 PRESS PRESET (EXT & INT), RUN
Halt Code: $1Ø2Ø24_8$

Example - Information only
Message: HØ25 BI-0 COMP
Halt Code: None

Error messages can be suppressed by selection of the switch register bit 11 and error halts can be suppressed by switch register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by Switch Register bit 10. Operator intervention is suppressed by setting Switch Register bit 8 (i.e., Preset Test in BI-0). When Switch Register bit 12 is set, the tests that are selected will be repeated. All operator intervention will be suppressed.

2-5.   PROGRAM LIMITATIONS

2-6.   PRIORITY STRING

The capability of the interface to receive, pass and deny priority is not completely checked by this diagnostic. If the interface does not receive priority (PRH from next lower select code) an error EØ14 NO INT will occur. To check this remove a board of a lower select code and run the Basic I/O test and the above mentioned error should occur. Checking the interface's ability to pass or deny priority is beyond the scope of this diagnostic.

Section III

OPERATING PROCEDURES

3-1.   LOADING AND CONFIGURING

3-2.   SINGLE COMPUTER ENVIRONMENT

Loading and configuring the diagnostic in a single computer environment should be done as follows:

1. Load Diagnostic Configurator into computer, if diagnostic has not been previously configured.
2. Configure the Diagnostic Configurator as described in M.O.D. (02100-90157).
3. At this time the user may optionally choose to dump a copy of the configured configurator. If so, set 'P' reg for $\emptyset$X7677 ('X' will vary as to memory size) set bits $\emptyset$-5 of 'S' reg to select code of punch and press 'RUN'.
4. Load diagnostic into computer (Data or Control tape). Follow step 3 above if a configured paper tape is desired.
5. Set 'P' reg to 100_8 and set the switch reg as follows:
    (In case of restarting or reconfiguring set 'P' reg to 100_8 and continue with the new switch reg setting.)

Figure 3-1.   Switch Register Settings

15 14 13 12	11	10	9 8 7 6	5 4 3 2 1 $\emptyset$
Transmit Port #	B/A	AUTO	Receive Port #	Interface Select Code

Port Number $\emptyset$-15

1 → 12920A
or
$\emptyset$ → 12920B
MUX

Port Number $\emptyset$-15

For Data: Lower Select Code
For Control: Interface
              Select Code

NOTE: If bits 12-15 and 6-9 are zero diagnostic will assume auto mode.
        A port is defined as one of the 16 connectors J$\emptyset$-J15 on the connector panel No. 30062-60002.

6. Press 'RUN', computer will halt and display: 1$\emptyset$2$\emptyset$74. Follow step 3 above if a configured paper tape is desired.
7. Set switch register to desired options, as described in Table 3-3. Bit 12 is used to loop on the diagnostic if set. Bit 13 is used to loop on a given test that is running at the time. Bit 15, if set, will halt the computer at the completion of a test. Press RUN and the diagnostic will begin.

3-3.   DIAGNOSTIC LOADING IN TWO COMPUTER ENVIRONMENT

When loading the diagnostic using two computers as in 2000C or 2000F systems, the following steps are followed:

1. Load Diagnostic Configurator into system computer.

3-1

2. Configure as previously described (refer Diagnostic Configurator 02100-90157).
   Be sure to configure to memory size, options and select codes of the I/O
   processor not the system processor.
3. Load Multiplexer diagnostic (Data or Control tape) into the system computer.
4. Using Diagnostic Configurator "Dump" routine as follows to transfer configured
   diagnostic from system computer to I/O processor.
   a. Set I/O processor "P" register to start of protected loader (Ø177ØØ for
      8K), press: preset Int/External, loader Enable and Run.
   b. Set "P" register of SYSTEM computer to ØX7677 (Ø17677 if I/O processor is
      8K). Set the switch register with the select code of the Processor
      Interconnect Card (12566) of the System Computer (1ØB for 2000C' and
      2000F systems). Press preset EXT/INT, and RUN.
   c. I/O processor will display 1Ø2Ø77 when loaded. Halt system computer.
   d. Select "P" register 1ØØB in I/O processor and proceed in configuring
      diagnostic as previously described in paragraph 3-2 no. 5.

3-4. TEST SELECTION BY OPERATOR

The control portion of the program provides for the operator to select his own
test or sequence of tests to be run. The operator sets switch register bit 9
to indicate he wants to make a selection and press RUN. The computer will come
to a halt 102075 to indicate it is ready for the selection. If the program is
running, that test will be completed and then the program will halt. Now the
operator loads the A register with the tests desired. The A register bit Ø
represents Test ØØ, bit 1 represents Test Ø1, and so on up to bit X which repre-
sents Test X*. The operator must then clear switch register bit 9 and press run.
The operators selection will then be run. If the operator clears all bits then
all the tests defined in Table 3-1, or 3-2 will be executed.

*Refer to Table 4-1.

Test Selection Summary

Table 3-1.

A-REGISTER BIT	IF SET WILL EXECUTE <u>DATA</u> BOARD
0	Test 00 BI-0 Test
1	Test 01 Send/Receive Test
2	Test 02 Break Test
3	Test 03 Parity Test
4	Test 04 Diagnostic
5	Test 05 Echo Test
6	Test 06 Sync Test
7	Test 07 Character Lost Test

Table 3-2.

A-REGISTER BIT	IF SET WILL EXECUTE <u>CONTROL</u> BOARD
0	Test 00 BI-0 Test
1	Test 01 Address Register Test
2	Test 02 Command and Register Test
3	Test 03 Command Register Addressing Test
4	Test 04 Status Interrupt Test
5	Test 05 Scan Test

Refer to Section IV for complete description of each test.

Table 3-3. Switch Register Options

BIT	MEANING IF SET
0	
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (102075); user may specify a new group of tests in the A register, clear bit 9 and then press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or teletype is not present. Also those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A register will contain the test number in octal.

Section IV

DIAGNOSTIC PERFORMANCE

4-1.   TESTS DESCRIPTION

4-2.   TEST Ø BASIC I/O CHECKS

Subtest 1 - Checks the ability to clear set and test the interrupt system. The
           following instruction combinations are tested:

           CLF 0 - SFC 0
           CLF 0 - SFS 0
           STF 0 - SFC 0
           STF 0 - SFS 0

           Errors in the above sequences produce error messages EØØØ-EØØ3 as
           shown in Table 4-2.

Subtest 2 - Checks the ability to clear, set and test the card select code. The
           following instruction combinations are tested:

           CLF CH - SFC CH
           CLF CH - SFS CH
           STF CH - SFC CH
           STF CH - SFS CH

           Errors in the above sequences produce error messages E005-E010 as
           shown in Table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the
           flag and control set on the card and the interrupt system off. The
           sequence of instructions is shown below:

           STF Ø
           STF CH
           STC CH
           CLC Ø

           The CLF Ø instruction should inhibit an interrupt from occurring.
           Error message EØØ4 occurs if CLF Ø fails.

Subtest 4 - Checks that the flag of the card under test is not set when all other
           select code flags are set. Error message EØ11 occurs if a flag is
           set incorrectly.

Subtest 5 - Checks the ability of the card to interrupt. With the flag and
           control set and the interrupt system on, there should be an interrupt
           on the I/O channel. If not, error message EØ14 occurs. Checks that
           the interrupt occurred where expected. The interrupt should not
           occur before a string of priority affecting instructions are executed.
           The following instructions are used to check the hold off operation:

4-1

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages EØ12 and EØ15 will occur if this is not true. Checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message EØ13 will occur if this is not true. Checks that no instruction was missed during the interrupt (EØ26 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the CH control and flag set, there is no interrupt following a CLC CH instruction. The following sequence of instructions are used.

```
STC CH
STF CH
STF Ø
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message EØ16 will occur.

Checks that the CLC Ø instruction inhibits interrupts when the CH control and flag are set. The following sequence of instructions is used.

```
CLF CH
STC CH
STF CH
STF Ø
CLC Ø
```

If the CLC Ø fails to inhibit an interrupt, error message EØ17 will occur.

Subtest 7 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) buttons on the front panel performs the following actions:

1. Sets I/O flag (EXTERNAL).
2. Clears control (EXTERNAL).
3. Turns off the interrupt system (INTERNAL).
4. Clears the I/O data lines (EXTERNAL).

4-3.   DESCRIPTION OF 12920 MUX Data Tests

4-4.   TEST 1 SEND/RECEIVE TEST

This test sends and receives an alternate 1's and Ø's pattern on the two ports specified during the configuration routine. The send and receive ports are

configured for six different BAUD rate (2400, 1200, 600, 300, 150 and 110) and the largest character size (nine data bits plus two stop bits). The test is then repeated with the complement data pattern. In each send and receive test the flag is checked for operation complete, and the port number is checked to see if the correct port has interrupted.

4-5. TEST 2 BREAK TEST

Sends and receives a non-zero test character on a port and checks the Break bit (bit 2) of the status word after each send and receive to see that it is set to zero.

Sends and receives a break character (all zeros) on a port; and checks the Break bit of the status word after each send and receive to see that it is set to one.

4-6. TEST 3 PARITY TEST

Sends and receives odd ASCII parity. Checks bit 15 (parity check bit) of the receive word for a one.

Sends and receives even ASCII parity. Check bit 15 (parity check bit) of the receive word for a zero.

4-7. TEST 4 DIAGNOSE TEST

Tests the ability to route send data to the auxiliary ports 16-20 when bit 11 (diagnose bit) of send parameter word is set to a one.

4-8. TEST 5 ECHO TEST

Receives a test character on each port with bit 12 (echo bit) of the receive parameter word set to a one. Tests the ability to echo character back on the corresponding send port.

4-9. TEST 6 SYNC TEST

Tests the ability to send an all mark (all ones) character when bit 11 (sync bit) of the output data word is a one.

4-10. TEST 7 CHARACTER LOST TEST

Tests the ability to detect the reception of two characters on a receive port without the computer responding, and to flag this condition by setting bit 1 of the status word to a one.

4-11.   DESCRIPTION OF 12922 MUX CONTROL TESTS

4-12.   TEST 1 ADDRESS REGISTER

Test (ART) - The address register test sends an address to the interface board
             then reads back the address for verification. This check is made
             for all 16 addresses. Also the address register is set to zero
             and then incremented through all 16 addresses by executing LIA
             instructions. After each LIA the address is verified.

4-13.   TEST 2 COMMAND AND STATUS TEST

Test (CST) - This program sends command word to the command registers. The com-
             mand register outputs are connected to the EIA line drivers. The
             test cable routes the signals to the EIA line receivers. The line
             receiver inputs are routed through the multiplexer into the IOBI
             bus. The input status is checked against the expected status.

4-14.   TEST 3 COMMAND REGISTER ADDRESSING TEST

Test (CRAT) - This program checks for proper addressing to the command registers
              and checks for an address being mapped to more than one address
              at a time.

4-15.   TEST 4 STATUS INTERRUPT TEST

Test (SIT) - This program tests the ability to set the flag when input status
             does not compare with the stored status.

4-16.   TEST 5 SCAN TEST

Test (SCAN) - The program sets up a port with a control word such that an
              interrupt will occur when the address register reaches that port
              number minus one. The I/O flag is cleared and the interface board
              is set in the SCAN mode. The next ENF signal from the computer
              should increment the address register to the port where the
              interrupt will occur. This sets the flag and stops the address
              register from incrementing. The flag is checked for a one and
              the address is verified.

Table 4-1. Halt Code Summary

HALT	DIAGNOSTIC	MEANING
TESTS 0_8 to 7_8		
102000-102056	12920	Error (E) information (H) messages 00-56$_8$.
TESTS 0_8 to 5_8		
102000-102040	12922	Error (E) information (H) messages 00-40$_8$.
CONTROL		
102072		Port number input error.
102073		Select code input error.
102074		Select code input complete.
102075		User selection request.
102076		End of Test (A = Test number).
102077		End of diagnostic run.
106077		Trap cell halts in location 2-77$_8$.

NOTE: See Table 4-2 for complete explanation of individual halts.

Table 4-2. Error, Information Messages and Halts
for _Data_ and _Control_ Boards

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102072	START	None	The port numbers entered during the configuration are invalid. Set the correct values in the switch register and press RUN.
102073	Configuration	None	I/O select code entered at configuration invalid. Must be greater than 7_8. Re-enter a valid select code and press RUN.
102074	Configuration	None	Select code entered during configuration valid. Enter program option bits in switch register and press RUN.
102075	Test Control	None	Test selection request resulting from switch register bit 9 being set. Enter in A register the desired group of tests to be executed, clear bit 9 and press RUN.
102076	Test Control	None	End of test halt resulting from switch register bit 15 being set (A register has the test number). To continue press RUN.
102077 AREG=PASS	Test Control COUNT	PASS XXXXXX	Diagnostic run complete. Switch register options may be changed. To continue press RUN.
106077	Test Control	None	Halt stored in location 2-77$_8$ to trap interrupts which may occur unexpectedly because of hardware malfunctions. M register contains the I/O slot which interrupted. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.
NONE	Test Control	ASYNC MULTIPLEXER DATA BOARD DIAGNOSTIC ASYNC MULTIPLEXER CONTROL BOARD DIAGNOSTIC	
NONE	Test Control	Test XX	Information message before error message (XX = test number). Message occurs only once within a test but is suppressed for any subsequent messages within the same test.

Table 4-2. Error, Information Messages and Halts
for Data and Control Boards (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102000	Test Ø	E000 CLF Ø-SFC Ø ERROR	CLF/SFC Ø combination failed. CLF did not clear flags or SFC caused no skip with flags clear.
102001	Test Ø	E001 CLF Ø-SFS Ø ERROR	CLF/SFS Ø combination failed. CLF did not clear flags or SFS caused skip with flags clear.
102002	Test Ø	E002 STF Ø-SFC Ø ERROR	STF/SFC Ø combination failed. STF did not set flags or SFC caused skip with flags set.
102003	Test 0	E003 STF Ø-SFS Ø ERROR	STF/SFS Ø combination failed. STF did not set flags or SFS caused no skip with flags set.
102004	Test 0	E004 CLF Ø DID NOT INHIBIT INT	With card flag and control set, CLF Ø did not turn off interrupt system.
102005	Test 0	E005 CLF CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102006	Test 0	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102007	Test 0	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set flag or SFC caused skip with flag set.
102010	Test 0	E010 STF CH-SFS CH ERROR	STF/SFS CH combination failed. STF did not set flag or SFS caused no skip with flag set.
102011 AREG = XX$_8$	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. XX = select code that caused that card flag to set.
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURRED	Card interrupt a second time after initial interrupt was processed.

Table 4-2. Error, Information Messages and Halts
for <u>Data</u> and <u>Control</u> Boards (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102014	Test 0	E014 NO INT	No interrupt occurred with card flag and control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0	E016 CLC CH ERROR	CLC CH did not clear card control with the interrupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear control with the interrupt system on.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card flag.
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I-O LINES	PRESET (EXT) did not clear I/O data lines.
102024	Test 0	H024 PRESS PRESET (EXT & INT),RUN	Press PRESET (External, Internal), RUN.
NONE	Test 0	H025 BI-O COMP	Basic I/O Tests completed.
102026	Test 0	E026 INT EXECUTION ERROR	Interrupt was not processed correctly.

Table 4-3. Messages and Error Halts for Data Board Diagnostic

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102030	SEND/REC	E030 SEND PORT XX DID NOT INTERRUPT	Send port XX did not cause an external interrupt within timeout period of 300 milliseconds. A-Register contains the value of XX.
102031	SEND/REC DIAG	E031 RECEIVE PORT XX DID NOT INTERRUPT	Receive port XX did not cause an external interrupt within time-out period of 300 milliseconds. A-Register contains the value of XX.
102032	SEND/REC	E032 SEND PORT NUMBER IS XX SHOULD BE YY	Data was sent out on a port different than the one intended. A-Register contains value XX and B-Register contains value YY.
102033	SEND/REC	E033 RECEIVE PORT NUMBER IS XX SHOULD BE YY	Data was received on a port different than the one intended. A-Register contains value XX and B-Register contains value YY.
102034	SEND/REC	E034 DATA RECEIVED ON PORT XX IS XXXX SHOULD BE YYYY	Data sent did not compare with data received. A-Register contains value XXXX and B-Register contains value YYYY. Press RUN the A-Register will
106034	SEND/REC		contain port number XX. Press RUN to continue.
102035	SEND/REC	E035 S-R BIT SHOULD BE SET	When data was transmitted the send/receive status bit indicated received data.
102036	SEND/REC	E036 S-R BIT SHOULD BE RESET	When data was received the send/receive status bit indicated send data.
102037	BREAK	E037 BREAK BIT SHOULD NOT BE SET	A non-zero character is followed by a null character. The status is obtained during the transmission of the null. This test verifies that the break condition is buffered.

Table 4-3. Messages and Error Halts for <u>Data</u> Board Diagnostic (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102040	BREAK	E040 BREAK BIT SHOULD NOT BE SET	A non-zero test character was sent but bit 2 of the status word was not set to a zero.
102041	BREAK	E041 BREAK BIT SHOULD BE SET	A zero test character was sent but bit 2 of status word was not set to a one.
102042	PARITY	E042 PARITY BIT SHOULD BE SET	Odd ASCII parity sent but bit 15 of received word was not set to a one.
102043	PARITY	E043 RAW PARITY BIT 7 ERROR	Odd ASCII parity sent. A check is made on bit 7 of the received data. This bit is generated in the parity generator of the send section and not modified by the receive position.
102044	PARITY	E044 PARITY BIT SET	Even ASCII parity sent but bit 15 of received word was not set to a zero.
102045	PARITY	E045 RAW PARITY BIT 7 ERROR	Even ASCII parity sent. Similar to E043 except for even parity.
102046	DIAGNOSE	E046 SEND DATA NOT ON AUXILIARY PORT XX	Bit 11 (diagnose) of send parameters was set but data was not routed to auxiliary port XX. A-Register contains value XX.
102047	DIAGNOSE	E047 RECEIVED DATA NOT ON AUXILIARY PORT XX	Bit 11 (diagnose) of received parameters was set but data received was not routed to auxiliary port XX. A-Register contains value XX.
102050	ECHO	E050 NO ECHO ON PORT XX	Bit 12 (echo) of receive parameters was set but data was not echoed back on port XX. A-Register contains value XX.
102051	SYNC	E051 SYNC TEST FAILED	Failed to send an all mark (all ones) character when sync bit was set to a one and all data bits were ones.

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102052	SYNC	E052 SYNC TEST FAILED (PTY=1)	Failed to receive an all mark (all ones) character when sync bit was set to a one and data bits plus parity were ones.
102053	CHAR-LOST	E053 CHARACTER LOST FAILED	Bit 1 (character lost) of status word should be set to a one to indicate character-lost condition.
102054	ANY	E054 SEEK BIT IS A ONE SHOULD BE A ZERO	During a seek operation the seek bit (bit 15) failed to reset within time-out period of 300 milliseconds.
102055	ANY	E055 SEEK STAYED SET	After issuing a CLC Ø to clear the interface the SEEK remained a one for more than 100 ms.
102056	ANY	E056 SEEK FAILED TO SET AFTER CLC Ø	A CLC Ø instruction is given to clear the interface. The SEEK bit should go to a one then to a zero.

Table 4-4. Error Messages and Halts for <u>Control</u> Board Diagnostic

HALT CODE	SECTION	MESSAGE	COMMENTS
102027	Test 0	E027 PRESET DID NOT CLEAR STATUS ON PORT XX	The status register was not cleared on port XX after preset.
102030	Test 1	E030 THE PORT ADDRESS IS XX SHOULD BE YY	The program selected port YY but the board returned with port XX. The A-Register contains XX and B-Register contains YY.
102031	Test 1	E031 THE PORT ADDRESS IS XX SHOULD BE YY	The LIA instruction failed to increment the address register. The actual port XX did not compare with the expected port YY. The A-Register contains XX and B-Register contains YY.
102032	Test 2	E032 STATUS ON PORT XX IS XXXXXX SHOULD BE YYYYYY	The status on port XX didn't compare with the expected status. For non teleprinter option A-Register contains actual status XXXXXX. B-Register contains expected status YYYYYY. Press RUN the A-Register will contain port number XX. Press RUN to continue.
106032	Test 2		
102033	Test 3	E033 OUTPUT ON PORT XX CHANGES PORT YY	An output was made to 15 ports (XX). After each output, port YY was tested to see if it was altered. B-Register contains XX. A-Register contains YY.
102034	Test 4	E034 STORED STATUS #1 FAILED TO INTERRUPT	A control word sets up stored status #1 to cause an interrupt and no interrupt occurred.
102035	Test 4	E035 STORED STATUS #2 FAILED TO INTERRUPT	A control word sets up stored status #2 to cause an interrupt and no interrupt occurred.
102036	Test 4	E036 I-O FLAG FAILS TO CLEAR. SIT ABORTED.	Cannot clear I/O flag. The Status Interrupt Test (SIT) was aborted.

Table 4-4. Error Messages and Halts for Control Board Diagnostics
(continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102037	Test 5	E037 SCAN TEST FAILED	During an SCAN operation the I/O flag failed to set.
102040	Test 5	E040 SCAN TEST INTERRUPT OCCURRED ON PORT XX SHOULD BE PORT YY	An interrupt occurs during the SCAN operation the port number is XX should be YY. A-Register contain XX, B-Register contains YY.

Communications
Multiplexer Panel   Test Cable
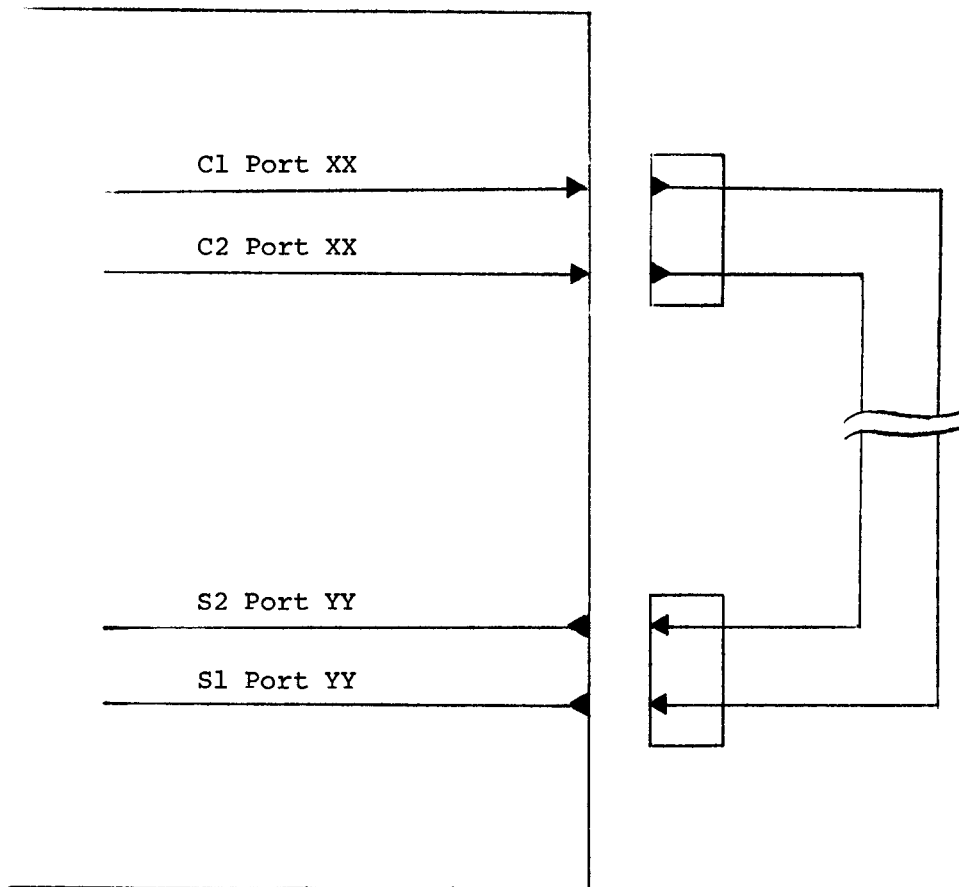   30062-60002   30062-60003

Figure 4-1. Test connector scheme for routine command (Cn)
             output and status (S_n) input signal lines.

CH X   8 Test Cables   CH Y

Ø ┤├─────────)   (─────────┤├ 1

2 ┤├─────────)   (─────────┤├ 3

4 ┤├─────────}   )─────────┤├ 5

6 ┤├─────────{   )─────────┤├ 7

8 ┤├─────────{   )─────────┤├ 9

10 ┤├─────────}   )─────────┤├ 11

12 ┤├─────────}   )─────────┤├ 13

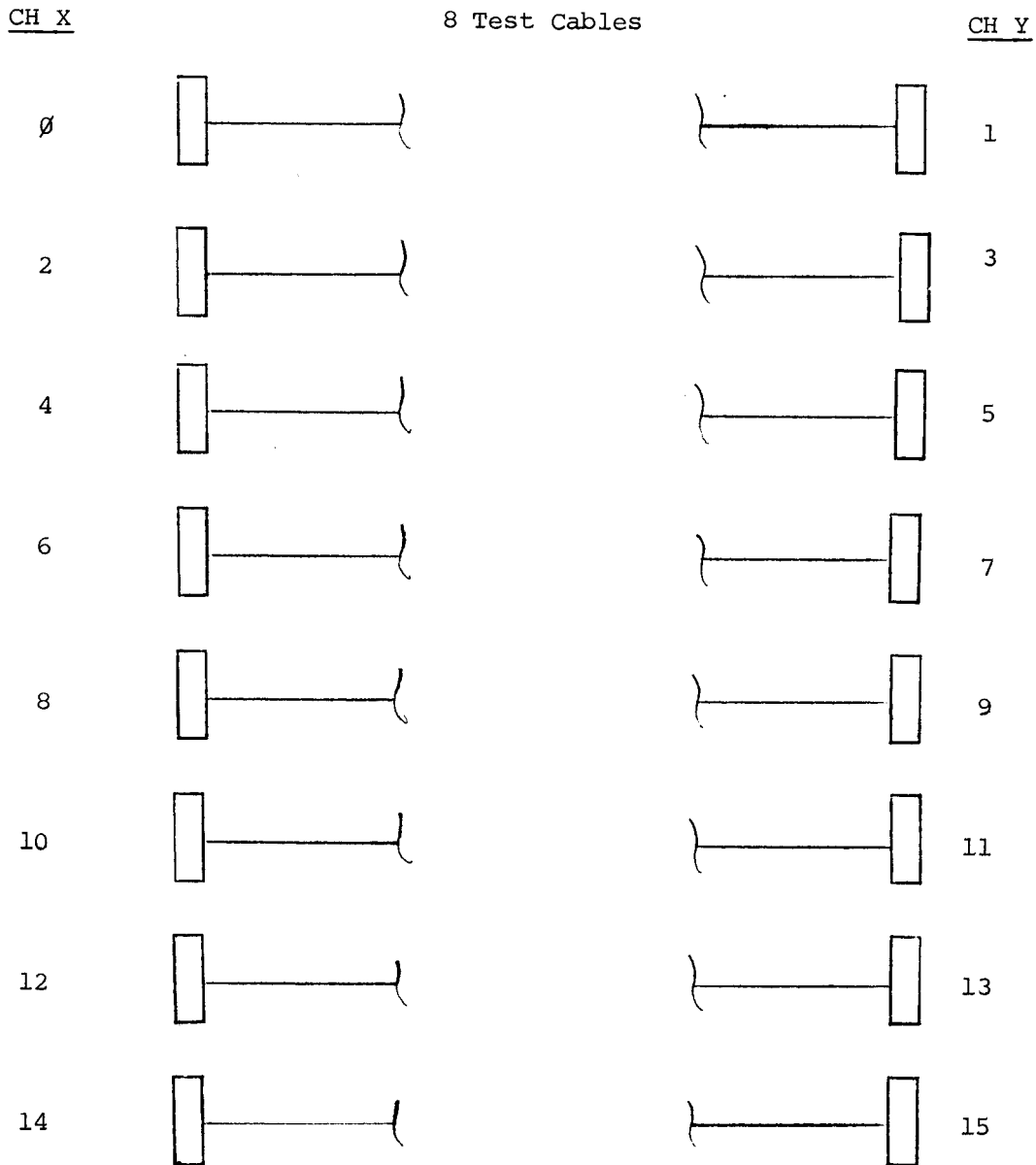14 ┤├─────────{   )─────────┤├ 15

Figure 4-2. Test cables scheme for automatic mode.

NOTE: Only one test cable is furnished with the diagnostic. To
       run all 16 ports in sequential order the operator must
       obtain 7 additional test cables and connect them as shown.
       Bit 10 must be set during the configuration.

HP 2100A

ASYNCHRONOUS MULTIPLEXER CONTROL TEST

HP Product No. HP 24255

HEWLETT **hp** *PACKARD*

11000 Wolfe Road
Cupertino, California 95014

May 1972

HP 2100A ASYNCHRONOUS MULTIPLEXER CONTROL TEST

This diagnostic confirms the proper operation of the HP 12922A Multiplexer
Control Interface Board and the control and status lines through the
HP 30062A Communications Multiplexer Panel for the HP 2100A Computer.

The program provides convenient modes of testing. The operator can repeat
each function test within the diagnostic as often as desired; or he can run
the entire program, stopping at the end of each function test to evaluate
the results.

OPERATING ENVIRONMENT

This diagnostic requires an HP 2100A Computer running under the control of
a HP 2000C with the high speed option, HP 2000E or HP 2000F Time-Shared
BASIC System. The HP 2000E system uses only one 2100A Computer. The HP
2000C and HP 2000F systems use two 2100A Computers, one as the central
processor and the other as the I/O processor.

Before using the diagnostic, the HP 30062-60003 test cable(s) must be
connected to the HP 30062A Communications Multiplexer Panel.

On the HP 2000E system, a teleprinter can be used to report errors or diag-
nostic messages. On the HP 2000C and HP 2000F systems (and on the HP 2000E
system if no teleprinter is available) errors and messages are reported by
coded displays in the computer MEMORY DATA register.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

If a teleprinter is to be used (HP 2000E system only), the SIO teleprinter
driver must be loaded and configured before the diagnostic is loaded. The
operator then loads the program tape and configures the program for the I/O
select code of the multiplexer control interface board by setting the switch
register according to Table 1.

1

> *NOTE: To avoid reconfiguring the diagnostic program (and the
> teleprinter driver) for each use, run the SIO System Dump
> program to punch a copy of the configured teleprinter
> driver and the configured diagnostic program.*

Run Modes

After the diagnostic program has been loaded and configured (or a configured
diagnostic tape has been loaded), the user decides in which of two possible
modes the diagnostic is to run.

Mode 1

> Mode 1 tests two channels. The user attaches the HP 30062-60003 test
> cable to the two channels on the multiplexer panel. He indicates
> which pair of multiplexer channels the program is to test by setting
> the switch register according to Table 2. The channels tested can be
> changed by returning to the CFGCH routine and setting new channel num-
> bers into the switch register according to Table 2.

Mode 2

> Mode 2 tests all 16 channels (eight pairs) in sequence. The user
> must obtain seven additional HP 30062-60003 test cables and connect
> them according to Figure 1. To indicate that the diagnostic is to
> test all 16 channels, set on bit 15 of the switch register (Table 2).

Before running the diagnostic, the operator should initiate run options (such
as suppressing error messages and repeating function tests) by setting the
switch register according to Table 3.

Diagnostic Errors

If any errors are detected during execution, the program types a message (if error messages are not suppressed) and halts with an error halt displayed in the computer MEMORY DATA register. Exceptions: trap-cell and configuration halts do not include messages.

Trap-cell halts are not recoverable. The cause of a trap-cell halt (beyond the scope of this diagnostic) should be determined before restarting the diagnostic.

When a teleprinter is not available and the program halts, the halt code is displayed in the MEMORY DATA register. Data displayed to the operator is contained in the computer A and/or B registers. Consult Table 4 for the meaning of the A- or B-register contents.

PROGRAM ORGANIZATION

The diagnostic program consists of the following test routines.

TWP   This bootstrap routine transfers the diagnostic program to the I/O processor from the central processor computer. In the HP 2000C and HP 2000F systems, the TWP routine is read into the central processor through the photoreader. Then the rest of the diagnostic program tape is read and the program transferred to the I/O processor. The bootstrap reads one character at a time and passes it to the I/O processor basic binary loader on one of the communications channels. The bootstrap routine is not used in the HP 2000E system; no separate I/O processor exists.

CFGIO   Reads the switch-register settings and configures the diagnostic for the proper I/O select code, with or without teleprinter.

CFGCH   Reads the switch register and configures the diagnostic to test the two channels indicated (mode 1) or, if switch register bit 15 is set on, configures the diagnostic to test all channels in sequence (mode 2).

INIT   Sets all trap-cell halts in locations 2_8 through 77_8. Types the starting message on the teleprinter (if program option bit 9 is set off).

BI/O   Clears the multiplexer control interface I/O logic, checks all flag instructions and the ability to enable and disable interrupts. BI/O then forces an interrupt, checks the interrupt return address and determines whether the interrupt was acknowledged. Then BI/O checks the control reset instructions and, if switch register bit 10 is set on, the PRESET switch checks for flag set, interrupts disabled, control cleared, and command registers cleared.

ART   ART has two sets of tests. The first set sends an address to the interface board and then reads back the address to verify that the address register is functioning properly (for all 16 addresses). The second set clears the address register and increments it through all 16 addresses (by executing LIA instructions). Each time one of the LIA instructions is executed, the address register is incremented by one. After each LIA instruction is executed, the address register is examined to verify that it is functioning properly.

CST   Each command register output is connected to a line driver. The test cable routes signals from a line driver to a line receiver. Each line receiver input is connected to the IOBI bus through the multiplexer. This test sends a command to each of the command registers. When the signals are received by the associated line receivers, the input status is compared with the expected status.

CRAT   Checks for proper addressing to the command registers and checks for an address being mapped to more than one address at a time.

SIT   Tests the ability to set the I/O flag when the input status does not match the stored status.

SCAN   Sets up a channel with a control word so that an interrupt will occur when the address register contains that channel number. Then the address register is set to the channel number minus one, the I/O flag is cleared, and the interface board is put in the SCAN mode. The next Enable Flag (ENF) signal from the computer should increment the address register, thus causing an interrupt. When the interrupt is sensed, the test program checks the contents of the address register.

OPERATING INSTRUCTIONS: HP 2000E SYSTEM

a. Halt the HP 2100A Computer.

b. If a configured version of the diagnostic tape is available, skip directly to step i below.

c. Use the Basic Binary Disc Loader (BBDL) to load the SIO teleprinter driver (if the teleprinter is to be used) and configure that driver. Consult Software Operating Procedures, *HP 2100A FRONT PANEL PROCEDURES* (HP 5951-1371).

d. Use the BBDL to load the HP 12922A asynchronous multiplexer control test tape.

> *NOTE:*   *The first foot of the test tape contains the bootstrap routine for the HP 2000C and HP 2000F systems. This routine may be skipped by placing the tape in the photo-reader behind the bootstrap routine so it will not be loaded.*

e. Set a starting address of 2_8.

f. Set the switch register to the octal I/O select code used by the multi-plexer control interface board, according to Table 1.

g. Press RUN. The computer halts with 107076_8 displayed in the computer MEMORY DATA register.

h. If desired, use the SIO System Dump program to punch a copy of the configured diagnostic (and SIO teleprinter driver if it was loaded in step c). If a copy is not desired, skip this step and continue with step j.

i. Use the BBDL to load the configured diagnostic tape.

j. Set the switch register to the octal representations of the decimal multiplexer control channel numbers to be tested (for two-channel test-ing) or set on switch register bit 15 if all 16 channels are to be tested (see Table 2).

k. Install the test cable to the multiplexer control channels chosen in step j. If all 16 channels are to be tested (bit 15 set on in step j), eight test cables should be installed according to Figure 1. If only two channels are to be tested, one test cable should be installed.

l. Press RUN. The computer halts with 107077_8 displayed in the MEMORY DATA register.

m. Set the switch register for the desired program run options, according to Table 3.

n. Press RUN.

    1. If program option bits 9 and 11 are set off, the diagnostic types a message (Table 4, message H8) and starts the first test.

    2. To access a specific test, set program option bit 15 on. The pro-gram halts at the end of each test and prints out a message on the teleprinter, if one is available. Press RUN to continue. Set pro-gram option bit 14 on to suppress error halts until the desired test is reached. Then set bit 13 on to loop through the test. Set bit 13 off to advance the program to the next test after execution of the current test.

3. Set program option bit 12 on to halt program execution after one complete cycle of the program. Press RUN. If bit 8 is set on, the program loops back to the CFGCH routine and halts with 107073_8 displayed in the MEMORY DATA register. If bit 8 is set off, the program loops back to the BI/O routine.

4. To reconfigure the diagnostic for a new I/O select code for the multiplexer control interface board, set a starting address of 111_8 and perform steps f through n.

5. To restart the diagnostic without reconfiguring, set a starting address of 110_8 and perform steps m through n.

OPERATING INSTRUCTIONS: HP 2000C AND HP 2000F SYSTEMS

a. Halt both the central processor and the I/O processor.

b. Using the Basic Binary Disc Loader (BBDL) and the photoreader for the central processor, load the diagnostic tape. The computer halts with 102077_8 displayed in the MEMORY DATA register after one foot of the tape (containing the TWP bootstrap routine) has been read. Consult Software Operating Procedures, *HP 2100A FRONT PANEL PROCEDURES* (HP 5951-1371).

c. Set a starting address of 2_8 in the central processor.

d. Press INTERNAL PRESET, EXTERNAL PRESET then press RUN on the central processor. The bootstrap program runs in a loop waiting for step e.

e. Start execution of the Basic Binary Loader in the I/O processor. The central processor resumes reading the diagnostic tape. When the entire tape has been loaded, the I/O processor halts with 102077_8 in the MEMORY DATA register. The central processor bootstrap program continues to loop. The central processor is no longer used, and may be ignored.

*** PERFORM THE REMAINING STEPS USING THE I/O PROCESSOR ***

f. Set a starting address of 2_8.

g. Configure the diagnostic program by setting the switch register to the desired I/O select code as shown in Table 1. Bit 9 must be set on to indicate that no teleprinter is available.

h. Press RUN. The computer halts with 107076_8 displayed in the MEMORY DATA register.

i. Set the switch register to the octal representation of the decimal multiplexer control channel numbers to be tested (for two-channel testing) or set on switch register bit 15 if all 16 channels are to be tested (see Table 2).

j. Install the test cable to the multiplexer control channels chosen in step i. If all 16 channels are to be tested (bit 15 on in step i) install eight test cables according to Figure 1. If only two channels are to be tested, install one test cable.

k. Press RUN. The computer halts with 107077_8 displayed in the MEMORY DATA register.

l. Set the switch register for the desired run options according to Table 3.

m. Press RUN.

1. To access a specific test, set program option bit 15 on. The program halts at the end of each test. Set program option bit 14 on to suppress error halts until the desired test is reached. When the desired test is reached, set bit 13 on to loop through the test. Set bit 13 off to advance the program to the next test after execution of the current test.

2. Set program option bit 12 on to halt the program after one complete cycle of execution. Press RUN. If bit 8 is set on, the program loops back to the CFGCH routine and halts with 107073_8 displayed in the MEMORY DATA register. If bit 8 is set off, the program loops back to the BI/O routine.

3. To reconfigure the diagnostic for a new I/O select code for the multiplexer control interface board, set a starting address of 111_8 and perform steps g through m.

4. To restart the diagnostic without reconfiguring, set a starting address of 110_8 and perform steps l and m.

ERROR ANALYSIS

Messages to the operator typed on the teleprinter (if available) are prefixed by an alphanumeric code. The H prefix indicates an operating instruction while the E prefix indicates an error message.

All halts display a value in the computer MEMORY DATA register. If no teleprinter is available for messages, the meaning of the halt is found in Table 4 opposite the halt code. Any data to be read is found in the A and/ or B register. Press RUN to continue program execution after an error halt (except trap-cell halts).

Table 1

Multiplexer Select Code Configuration--Switch Register Settings

Bits	Description
0-5	Select code for the I/O channel containing the multiplexer control interface.
6-8	Not used.
9	If set on, a teleprinter is not available. If set off, a teleprinter is available.
10-15	Not used.

Table 2

Multiplexer Control Channel Numbers--Switch Register Settings

Bits	Description
0-3	Multiplexer control channel number.
4-5	Not used.
6-9	Multiplexer control channel number.
10-14	Not used.
15	Set on to test all 16 channels in sequence (mode 2 operation). This switch overrides the setting of all other switches.

Table 3

Program Options--Switch Register Settings

Bits	Description
0-7	Unused.
8	If set on, return the program to the CFGCH routine at the end of the program and halt with 107073_8 displayed in the MEMORY DATA register. The operator starts at step i of the operating instructions for HP 2000C and HP 2000F or step j of the operations instructions for HP 2000E. If set off, return program to the BI/O test at the end of the cycle.
9	If set on, omit start and stop messages on the teleprinter. If set off, print start and stop messages.
10	If set on, execute the PRESET test. If set off, omit the PRESET test.
11	If set on, suppress all printouts. If set off, type messages on the teleprinter.
12	If set on, halt the program at the end after one complete cycle. If set off, return to the CFGCH or BI/O routine at the end of the program, depending on the setting of bit 8.
13	If set on, recycle the current test instead of advancing to the next test within the diagnostic. If set off, advance to the next test.
14	If set on, suppress error halts. If set off, halt on error.
15	If set on, each separate test within the diagnostic runs and halts (with the appropriate message typed on the teleprinter if available). Go on to the next test by pressing RUN. Repeat the current test by setting bit 13 on and pressing RUN. If set off, execute each test without halting between tests.

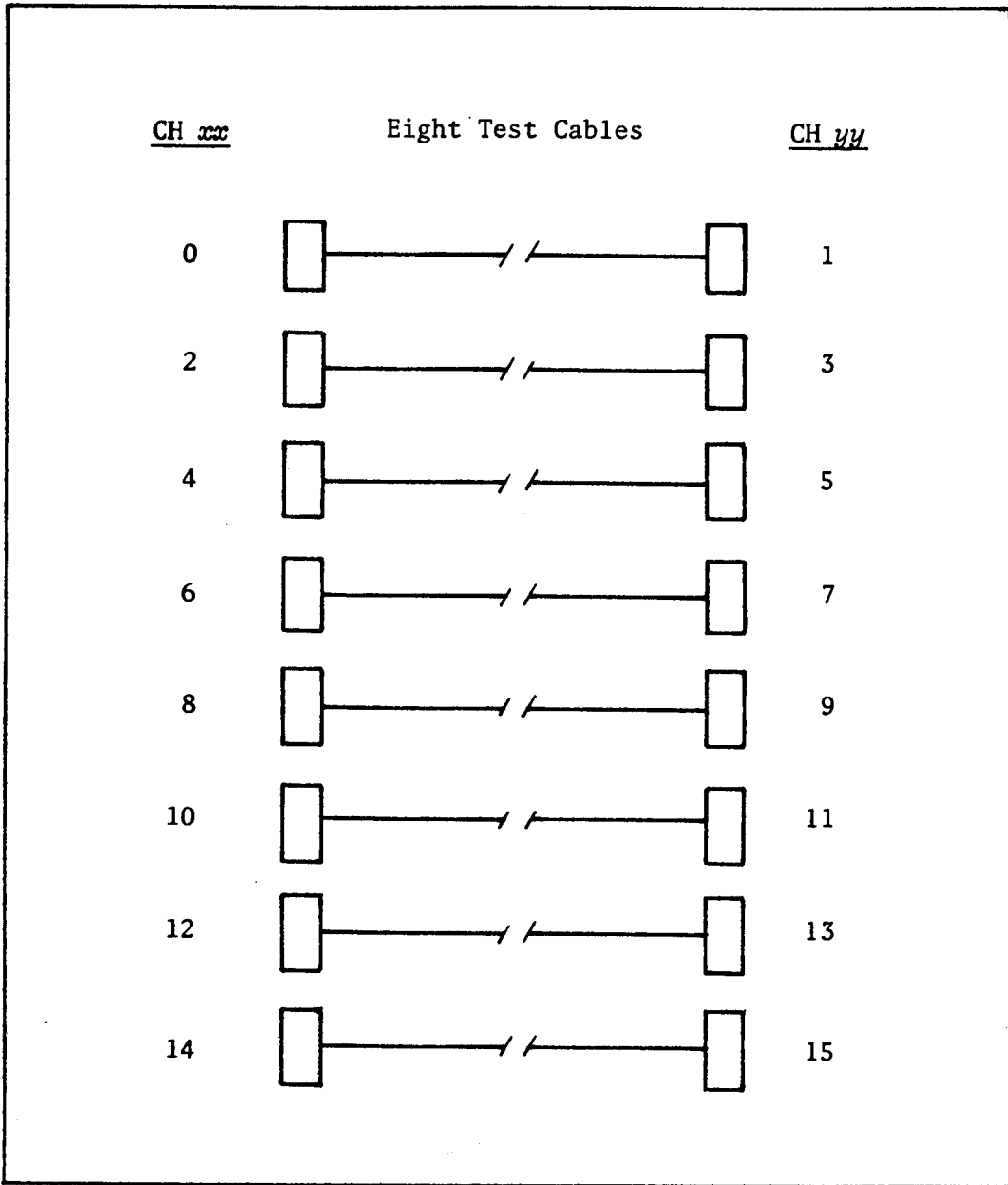CH _xx_   Eight Test Cables   CH _yy_

Figure 1

Test Cable Scheme for Mode 2

NOTE: *Only one test cable is furnished with the diagnostic. To test all 16 channels in mode 2, the operator must obtain seven additional test cables and connect them as shown. Bit 15 must be set on during the multiplexer control channel configuration.*

Table 4
Diagnostic Messages

Memory Data	Routine	Message	Comments
1060xx	Any	None.	Trap-cell interrupt. P=memory address when interrupted, xx= the trap cell location.
102001	BI/O	E1. CLF DID NOT CLEAR FLAG OR SFS CAUSED SKIP WITH FLAG CLEAR	Test the ability to clear the interface flag and test the SFS instruction.
102002	BI/O	E2. SFC DID NOT SKIP WITH FLAG CLEAR	Test the ability of the SFC instruction.
102003	BI/O	E3. STF DID NOT SET FLAG, OR SFC CAUSED SKIP WITH FLAG SET	Test the ability to set the interface flag and test the SFC instruction.
102004	BI/O	E4. SFS DID NOT SKIP WITH FLAG SET.	Test the SFS instruction.
102005	BI/O	E5. DID NOT INTERRUPT	Test the interface interrupt capability.
102006	BI/O	E6. THE RETURN ADDRESS IS NOT CORRECT	The return address that resulted from the interrupt is incorrect.
102007	BI/O	H7. PRESS PRESET, THEN PRESS RUN	Press INTERNAL and EXTERNAL PRESET.
No Halt	INIT	H8. START ASYNC MULTI- PLEXER CONTROL DIAG- NOSTIC	Start message (omitted if bit 9 set).
102010	BI/O	E10. PRESET DID NOT SET THE FLAG	EXTERNAL PRESET logic failed.
102011	BI/O	H11. END BI/O	Select options and press RUN.
102012	BI/O	E12. INTERRUPTED AFTER CLF ∅	CLF 0 should prevent inter- rupts.
102013	BI/O	E13. PRESET DID NOT SET FLAG AND DID NOT DISABLE INTERRUPTS	INTERNAL and EXTERNAL PRESET failed.

Table 4 (cont.) Diagnostic Messages

Memory Data	Routine	Message	Comments
102014	BI/O	E14. INTERRUPT ACKNOW-LEDGE DID NOT WORK. TEST ABORTED	Remaining tests of BI/O are terminated.
102015	BI/O	E15. CLC Ø DID NOT CLEAR CONTROL F/F	Control F/F did not reset with CLC 0 instruction.
102016	BI/O	E16. PRESET DID NOT CLEAR CONTROL F/F	EXTERNAL PRESET logic failed.
102017	BI/O	E17. CLF Ø OR SFS Ø DID NOT WORK	CLF 0 did not disable inter-rupts or SFS 0 caused a bad skip.
102020	BI/O	E20. CLF Ø OR SFC Ø DID NOT WORK	CLF 0 did not disable inter-rupts or SFC 0 caused a bad skip.
102021	BI/O	E21. STF Ø OR SFC Ø DID NOT WORK	STF 0 did not enable inter-rupts or SFC 0 caused a bad skip.
102022	BI/O	E22. STF Ø OR SFS Ø DID NOT WORK	STF 0 did not enable inter-rupts or SFS 0 caused a bad skip.
102023	BI/O	E23. PRESET DID NOT DISABLE INTERRUPTS	INTERNAL PRESET logic failed.
102024	BI/O	E24. CLC CH,C DID NOT CLEAR FLAG OR SFC DID NOT SKIP WITH FLAG CLEAR	This tests the ",C" part of the instruction to clear flag.
102025	BI/O	E25. CLC ON CHANNEL DID NOT CLEAR CONTROL FLIP-FLOP	Control F/F did not reset with CLC SC instruction (SC=channel of interface).
102026	BI/O	E26. PRESET DID NOT CLEAR STATUS ON CHANNEL XX	The status register was not cleared on channel XX after preset.
102027	ART	E27. THE CHANNEL ADDRESS IS XX SHOULD BE YY	The program selected channel YY but the board returned with channel XX. The A register contains XX and the B register contains YY.

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Table 4 (cont.) Diagnostic Messages

Memory Data	Routine	Message	Comments
102030	ART	E30. THE CHANNEL ADDRESS IS XX SHOULD BE YY	The LIA instruction failed to increment the address register. The actual channel XX did not compare with the expected channel YY. The A register contains XX and the B register contains YY.
102031	ART	H31. END OF ADDRESS REGISTER TEST	Select options and press RUN.
102032	CST	E32. STATUS ON CHANNEL XX IS XXXXXX SHOULD BE YYYYYY	The status on channel XX did not compare with the expected status. For teleprinter operation, press RUN to continue. For non teleprinter operation, the B register contains the actual status XXXXXX and the A register contains the expected status YYYYYY. Press RUN and the A register will contain the channel number XX. Then press RUN to continue.
102033	CST	H33. END OF COMMAND AND STATUS TEST	Select options and press RUN.
102034	CRAT	E34. OUTPUT ON CHANNEL XX CHANGES CHANNEL YY	An output was made to 15 channels (XX). After each output, channel YY was tested to see if it was altered. B register contains XX. A register contains YY.
102035	CRAT	H35. END OF COMMAND REGISTER ADDRESS-ING TEST	Select options and press RUN.
102036	SIT	E36. STORED STATUS #1 FAILED TO INTERRUPT	A control word sets up stored status #1 to cause an interrupt and no interrupt occurred.
102037	SIT	E37. STORED STATUS #2 FAILED TO INTERRUPT	A control word sets up stored status #2 to cause an interrupt and no interrupt occurred.

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Table 4 (cont.) Diagnostic Messages

Memory Data	Routine	Message		Comments
102040	SIT	E40.	I/O FLAG FAILS TO CLEAR. SIT ABORTED	Cannot clear I/O flag. The SIT is aborted.
102041	SIT	H41.	END OF STATUS INTERRUPT TEST	Select options and press RUN.
102042	SCAN	E42.	SCAN TEST FAILED	During a SCAN operation the I/O flag failed to set.
102043	SCAN	E43.	SCAN TEST INTERRUPT OCCURRED ON CHANNEL XX SHOULD BE CHANNEL YY	An interrupt occurs during the SCAN operation; the channel number is XX should be YY. The A register contains XX, the B register contains YY.
102044	SCAN	H44.	END OF SCAN TEST	Select option and press RUN.
102077	END	H77.	DIAGNOSTIC HAS BEEN COMPLETED	End of test. If bit 12 of switch register is set, program will halt (102077).
107073	CFGCH	None.		Configure the multiplexer control channel numbers according to Table 2. (Step i of operating instructions for HP 2000C, HP 2000F, step j of operating instructions for HP 2000E).
107074	CFGCH	None.		The channel numbers entered during the multiplexer channel configuration are invalid. Set the correct values in the switch register and press RUN.
107075	CFGIO	None.		The select code (switch register bits 5-0) is invalid. (Valid codes are 10_8-77_8.) Set the correct select code, then press RUN.

Table 4 (cont.) Diagnostic Messages

Memory Data	Routine	Message	Comments
107076	CFGIO	None.	The I/O select code configuration is now complete. Follow the HP 2000E operating instructions at step h or the HP 2000C and HP 2000F operating instructions at step i.
107077	CFGCH	None.	The multiplexer channel configuration is now complete. Follow the HP 2000C and HP 2000F operating instructions at step 1 or the HP 2000E operating instructions at step m.