OPERATING AND SERVICE MANUAL

12566B,
12566B-001, 12566B-002, 12566B-003
MICROCIRCUIT INTERFACE KITS

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Card Assemblies

12566-60024, Rev. 1130, 1148
12566-60025, Rev. 1130, 1148

Note

Retain this manual with the applicable computer
system documentation.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2.   This manual provides general information, installation and programming instructions, theory of operation, maintenance instructions, and replaceable parts information for the HP 12566B Microcircuit Interface Kit (see figure 1-1).

1-3. DESCRIPTION.

1-4.   The interface kit provides a means to transfer data bidirectionally between an HP computer and a peripheral I/O device. The interface card provided with the kit has a 16-bit output register for data transfers from the computer and a 16-bit input register for data transfers into the computer. A Device Command signal from the interface card enables the peripheral device and, optionally, gates the output register to the output lines. The interface card accepts a Device Flag signal from the peripheral device to gate data into the input register and to generate an interrupt signal to the computer. Control signal and data lines are compatible with DTL/TTL logic levels and speeds.

1-5. EQUIPMENT SUPPLIED.

1-6.   The standard interface kit consists of the following items:

   a. One microcircuit interface card, part no. 12566-60024. (Transfers ground-true signals to/from I/O device.)

   b. One connector Kit, 48-pin, part no. 5060-8339.

   c. One connector, 24-pin, part no. 1251-0032.

   d. One cable, 36 twisted-pair, 15 feet, part no. 8120-1846.

   e. One Operating and Service Manual, part no. 12566-90015.

1-7. OPTIONS

1-8.   In addition to the standard kit, three options are available; they are described in paragraphs 1-9 through 1-16.

1-9.   OPTION 001.

1-10.   The option 001 interface kit provides a 24-pin connector kit, part no. 5060-8340 in place of the 48-pin connector kit, part no. 5060-8339. The option 001 kit is identical to the standard kit in all other respects.

1-11.   The 24-pin connector shorts each pin on the front of the printed circuit card to the adjacent pin on the back of the card. This shorts each data input line to the equivalent data output line, providing one set of 16 bidirectional data lines instead of separate input and output lines. Option 001 is useful for party line applications.

1-12.   OPTION 002.

1-13.   The option 002 interface kit includes a microcircuit interface card (part no. 12566-60025) that transfers positive-true signals to/from the I/O device, rather than ground-true signals as provided by the card in the standard kit. The option 002 kit is identical to the standard kit in all other respects.

1-14.   The output line inverters used on the option 002 interface card are not "or-tieable". Thus, the option 002 kit cannot be used in directly connected party line applications.
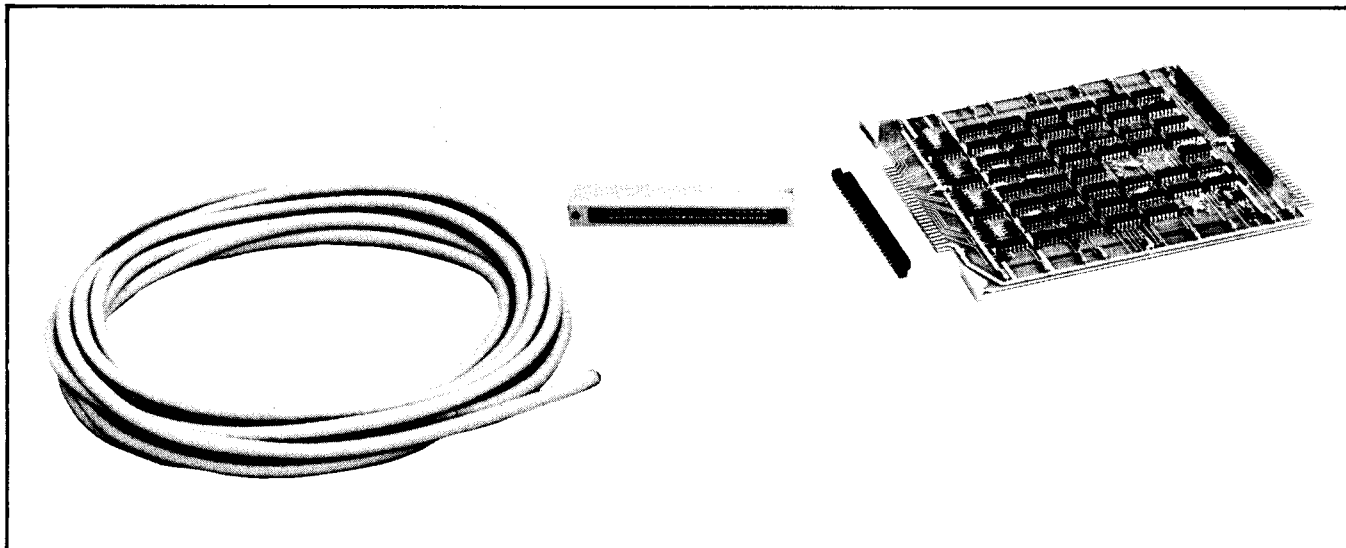
Figure 1-1. HP 12566B Microcircuit Interface Kit

1-15.   OPTION 003.

1-16.   The option 003 interface kit does not include the connector kit and interconnecting cable specified in paragraph 1-6.

1-17.   IDENTIFICATION.

1-18.   Printed circuit card revisions are identified by a letter, a date code, and a division code stamped on the card (e.g., A-1130-22). The letter code identifies the version of the etched trace pattern on the unloaded card. The date code (middle digits) refers to the electrical characteristics of the loaded card. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the card. If the date code stamped on the printed circuit card does not agree with the date code shown on the title page of this manual, there are differences between your card and the card described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-19.   SPECIFICATIONS.

1-20.   Table 1-1 lists specifications for the microcircuit interface card included in the kit.

Table 1-1. Interface Card Specifications

CHARACTERISTICS	SPECIFICATIONS
Output Levels:	
"1" state	0 to +0.5V dc, 31 mA max.
"0" state	+2.4 to +5.0V dc, 1k impd.
Input Levels:	
"1" state	0 to +0.5V dc, 15 mA
"0" state	+2.4 to +5.0V dc
Current Requirements: (Supplied by computer)	
+4.5V dc Supply	1.1A
−2V dc Supply	0.05A
Card Dimensions:	
Width	7-3/4 inches (196,8 mm)
Height	8-11/16 inches (220,7 mm)
Weight:	
Net	18 oz (544.8 gm)
Shipping	2 lb (908 gm)

SECTION II

INSTALLATION

2-1.   INTRODUCTION.

2-2.   This section provides information on unpacking and inspection, preparation for use, installation, and reshipment of the interface kit.

2-3.   UNPACKING AND INSPECTION.

2-4.   If the shipping container is damaged upon receipt, request that the carrier's agent be present when the equipment is unpacked. Inspect the card for damage (scratches, cracks, loose components, etc.). If the card is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (HP Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged equipment without waiting for any claims against the carrier to be settled.

2-5.   PREPARATION FOR USE.

2-6.   Because the interface kit is designed for a variety of applications, an interconnecting cable must be either fabricated or otherwise available for the particular peripheral I/O device used, and jumpers on the printed circuit card must be placed in the positions that will effect desired operation. Paragraphs 2-7 through 2-12 give instructions for cable fabrication (where necessary) and jumper placement.

2-7.   CABLE FABRICATION.

2-8.   The 48-pin connector kit furnished with the interface kit (or the 24-pin connector kit furnished with the option 001 kit) provides the required connection at the computer end of the interconnecting cable. The connector for the device end of the cable must be furnished by the user.

2-9.   Due to the fast rise times and low voltage level outputs from the microcircuit interface card, the interconnecting cable must be of the twisted-pair type. A special cable (part no. 8120-1846) fulfilling this requirement is available through any HP Sales and Service Office.

2-10.   Figures 2-1 and 2-2 show details of cable fabrication. The procedure for wiring the 48-pin connector is as follows:

    a.   Insert approximately 10 inches of cable into the connector hood.

    b.   Strip the outer jacket of the cable back 5 inches.

    c.   Prepare a bus wire from 22-gauge bare-copper wire and solder it to pins BB and 24 of the connector as shown in figure 2-1.
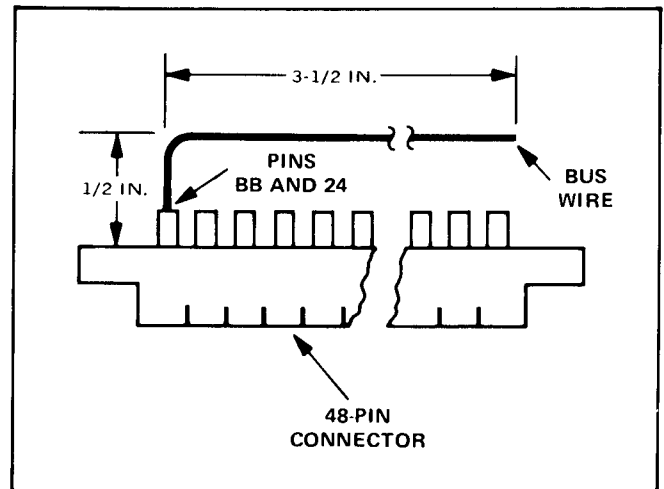
Figure 2-1. Bus Wire Details

    d.   Divide the 36 twisted-pairs into groups of six pairs each.

    e.   Starting at the end of the 48-pin connector nearest pins BB and 24, connect the first six pairs as follows:

        (1) Solder the six colored signal wires to their respective pins on the connector and insulate each pin with tubing as shown in figure 2-2.

        (2) Solder the six white ground wires to the bus wire and insulate with shrink tubing as shown in figure 2-2.

    f.   Repeat substeps (1) and (2) with the remaining groups of wires until all wires are soldered to the connector and insulated.

    g.   Trim off any excess bus wire and install the 48-pin connector in the connector hood using the two self-tapping screws.

    h.   Install the cable clamp and tighten it in place with the setscrew.

SHRINK
TUBING

BUS WIRE

SOLDER   CUTTING
AREA   LENGTH

SHRINK
TUBING

ITEM	DESCRIPTION	PART NO.
1	CONNECTOR HOOD	5040-6071
2	SELF-TAPPING SCREW (A)	0624-0098
3	MOUNTING BLOCK	5040-6072
4	SELF-TAPPING SCREW (B)	0624-0098
5	PAN-HEAD SCREW (4-40 x .562")	— — — —
6	HEX NUT (4-40 x .187")	— — — —
7	CONNECTOR, 48 PIN	1251-0335
8	CABLE CLAMP	5040-6003 OR 5040-6004
9	SET SCREW	3030-0143
10	CABLE, 36 TWISTED PAIR	8120-1846 OR EQUIVALENT

Figure 2-2. Cable Fabrication Diagram and Parts List

2-11. CIRCUIT CARD JUMPERS.

2-12.   Table 2-1 lists the jumper wires on the interface card and specifies the function associated with each jumper position. Figure 5-2 (5-4 for option 002) shows the location of each jumper on the circuit card. Use table 2-1 to determine which jumper positions give the desired operating characteristics.

Table 2-1. Interface Card Jumper Functions

JUMPER	POSITION	FUNCTION
W1		DEVICE COMMAND SIGNAL
	A	Provides a ground-true Device Command signal starting at T4.
	B	Provides a positive-true Device Command signal starting at T4.
	C	Provides a pulsed, ground-true Device Command signal starting at T6.
W2		DEVICE COMMAND FF
	A	Device Command FF clears on the positive-going edge of Device Flag signal.
	B	Device Command FF clears on the negative-going edge of Device Flag signal.
	C	ENF signal clears Device Command FF.
W3		DEVICE FLAG SIGNAL
	A	Sets the Flag Buffer FF and strobes input data on the positive-going edge.
	B	Sets the Flag Buffer FF and strobes input data on the negative-going edge.
W4		OUTPUT DATA REGISTER
	A	Output data is gated by the Data FF
	B	Output data is continuously available to the I/O device.
W5 (bits 0-3) W6 (bits 4-7) W7 (bits 8-11) W8 (bits 12-15)		INPUT DATA REGISTER
	W5, W6, W7, W8 Connected	Device Flag signal latches listed bits of the input data register.
	W5, W6, W7, W8 Disconnected	Listed bits of the input data register follow the input lines from the I/O device.
W9		DEVICE COMMAND FF
	A	Allows the CLC, CRS, and Device Flag signals to clear the Device Command FF.
	B	Allows only the CRS and Device Flag signals to clear the Device Command FF. This action is required for DMA operations.

2-13. INSTALLATION.

2-14.   Before installing the interface card in the computer, determine that the additional power consumed by the card will not overload the computer power supply. Power requirements of the card are given in table 1-1; instructions for calculating available power are given in the applicable computer manual. If sufficient power is available, and if the interconnecting cable has been fabricated and the jumper wires have been positioned for desired operation, install the interface kit as follows:

a.   Turn off power at the computer and at the I/O device.

b.   Gain access to the computer card cage and insert the interface card into the card slot corresponding to the desired I/O select code.

c.   Connect the 48-pin connector of the interconnecting cable (24-pin in option 001 kits) to the 48-pin edge of the interface card.

d.   Connect the other end of the interconnecting cable to the proper connector on the I/O device.

e.   Verify proper operation by performing the General Purpose Register Diagnostic test. Instructions for performing the diagnostic test are contained in the Diagnostic Program Procedure (part number 12554-90023 for the 2114, 2115, and 2116 Computers; part number 12554-90026 for the 2100 Computer) in the Manual of Diagnostics.

2-15. RESHIPMENT.

2-16.   If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the number of the kit.

2-17.   Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-18.   If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to assure careful handling.

Note

In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

SECTION III

PROGRAMMING

3-1.   INTRODUCTION.

3-2.   This section provides assembly language program-ming information for the interface kit. A sample program for a specific application is included.

3-3.   For information concerning software systems used with the computer, software interfacing, and operating pro-cedures, refer to the applicable software manuals provided with the computer documentation.

3-4.   OPERATION AND TIMING.

3-5.   Section IV of this manual provides theory of oper-ation for the circuits on the interface card. A flowchart, figure 4-1, is provided to show the operating sequence of the interface card and, consequently, the time relationships of the individual operations. A timing diagram is also given as an inset on the logic diagrams, figures 5-3 and 5-5.

3-6.   GENERAL PROGRAM CONSIDERATIONS.

3-7.   The flag circuit on the interface card can be moni-tored by a program to determine the status of either an input or an output device. When an input device is con-nected to the interface card, a set Flag FF indicates that data is in the input register and can be read into the com-puter. If the Flag FF is not set, the external device is in the process of transferring data to the input register.

3-8.   When an output device is connected to the inter-face card, a set Flag FF indicates that the device has received a previous data word and is ready to receive another word. If the Flag FF is not set, the external device is busy and cannot receive more data.

3-9.   If an I/O device is capable of both input and output operations, data can be transferred from the com-puter to the device via the output register and transferred from the device to the computer via the input register. Data may be transferred into or out of either register without affecting the other register, but the Flag FF can be asso-ciated with only one register at a time. Thus, if input and output operations are performed sequentially, the Flag FF sets when data is transferred to the input register, indicating to the computer that data is available. Program instructions must clear the Flag FF (STC,C instruction in sample pro-grams) before the output operation. After the device receives the output data, the Flag FF sets again, indicating to the computer that the data was received and that another data word may be sent.

3-10.   As an aid to writing programs, the sequence of program steps required to input a data word and output a data word are given in tables 3-1 and 3-2, respectively. The programs use the skip-if-flag-set method of determining device status, and are written for an interface card inserted in the computer I/O slot corresponding to select code 14.

Table 3-1. Sample Input Program

LABEL	OPCODE	OPERAND	COMMENTS
	:		MAIN PROGRAM
	JSB	INPUT	Jump to input subroutine.
	STA	CODE	Store A-register contents in memory location CODE.
	:		
			SUBROUTINE
INPUT	NOP		Entry point.
	STC	14B,C	Command I/O device to perform its operation.
	SFS	14B	Has I/O device completed its operation?
	JMP	*-1	No, jump back to SFS instruction.
	LIA	14B	Yes, transfer input data to A-register.
	JMP	INPUT,I	Return to main program.

Table 3-2. Sample Output Program

LABEL	OPCODE	OPERAND	COMMENTS
	:		MAIN PROGRAM
	LDA	N	Load A-register with con-tents of memory location N.
	JSB	OUTPT	Jump to output subroutine.
	:		
			SUBROUTINE
OUTPT	NOP		Entry point.
	SFS	14B	Is I/O device ready for data?
	JMP	*-1	No, jump back to SFS instruction.
	OTA	14B	Yes, transfer output data to microcircuit interface card.
	STC	14B,C	Command I/O device to accept data.
	JMP	OUTPT,I	Return to main program.

The programs show only the steps involved with the actual data transfer; for a complete program written for a specific application, refer to the line printer program in table 3-3.

3-11. LINE PRINTER PROGRAM.

3-12. The interface kit may be used to interface an HP 2767A Line Printer with an HP computer. A sample pro-

gram, written for this application, is given in table 3-3.

3-13. The sample program is provided to show how the input and output program segments of tables 3-1 and 3-2 fit into a complete program. For further information about the program, the line printer characteristics, or the interface card jumper positions, refer to the Operating and Service Manual for the line printer interface kit (part number 12653-90002).

Table 3-3. Line Printer Program

```
      0001                    ASMB,A,L,B,T
      NEXT    001012
      NEWD    001020
      OUT     001022
      N       001036
      BFCTR   001037
      BFADD   001040
      BUFAD   001041
      BUFF    001042
      LF      001107
      LP      000014
      CHRCT   001110
      **  NO ERRORS*
      0001                    ASMB,A,L,B,T
      0002*   THIS IS A SAMPLE PROGRAM FOR THE HP 80-COLUMN
      0003*   LINE PRINTER
      0004*
      0005*
      0006  01000             ORG 1000B
      0007  01000 065110      LDB CHRCT    INITIALIZE SWITCH TO KEEP TRACK
      0008*                                OF THE LEFT OR RIGHT CHARACTER
      0009*                                WITHIN WORD
      0010  01001 061036      LDA N        INITIALIZE PRINT LINE
      0011  01002 071037      STA BFCTR    COUNTER
      0012  01003 061041      LDA BUFAD    INITIALIZE PRINT LINE BUFFER
      0013  01004 071040      STA BFADD    ADDRESS POINTER
      0014  01005 102514      LIA LP       GET LINE-PRINTER STATUS. B15=0
      0015  01006 002020      SSA          INDICATES: PAPER LOADED, GATE
      0016*                                CLOSED, SPEED OKAY, POWER ON,
      0017*                                TEMPERATURE OKAY
      0018  01007 102010      HLT 10B      B15=1
      0019  01010 000010      SLA          B0=0 INDICATES LINE PRINTER
      0020*                                READY, ON-LINE AND NOT BUSY
      0021  01011 102011      HLT 11B      B0=1 LINE PRINTER BUSY
      0022  01012 161040 NEXT LDA BFADD,I  PICK-UP CHARS AND DETERMINE WHICH
      0023  01013 006011      SLB,RSS      CHAR WITHIN WORD IS TO BE OUTPUT
      0024  01014 025020      JMP NEWD     GO TO OUTPUT LEFT CHARACTER
      0025  01015 035040      ISZ BFADD    UPDATE POINTER TO NEXT WORD
      0026  01016 005200      RBL          INDICATE LEFT CHAR TO BE
      0027*                                OUTPUT NEXT
      0028  01017 025022      JMP OUT      OUTPUT CHARACTER
      0029  01020 001727 NEWD ALF,ALF     POSITION SO LEFT CHARACTER
      0030*                                CAN BE OUTPUT NEXT
      0031  01021 005200      RBL          INDICATE RIGHT CHAR TO BE
      0032*                                OUTPUT NEXT
      0033  01022 102614 OUT  OTA LP       OUTPUT CHARACTER
```

Table 3-3. Line Printer Program (Continued)

```
0034   01023 103714           STC  LP,C      STROBE INTO LINE PRINTER BUFFER
0035*                                         AND CLEAR INTERFACE BUFFER
0036   01024 102314           SFS  LP        WAIT FOR COMPLETION OF CHARACTER
0037   01025 025024           JMP  *-1        TRANSFER
0038   01026 035037           ISZ  BFCTR     INCREMENT LINE OUTPUT COUNTER
0039   01027 025012           JMP  NEXT      OUTPUT MORE CHARACTERS
0040   01030 061107           LDA  LF        OUTPUT LINE-FEED
0041   01031 102614           OTA  LP         CHARACTER
0042   01032 103714           STC  LP,C       AND STROBE INTO LINE
0043*                                          PRINTER BUFFER
0044   01033 102314           SFS  LP        WAIT FOR LINE-FEED OPERATION
0045   01034 025033           JMP  *-1        COMPLETION
0046   01035 102012           HLT  12B       OPERATION COMPLETE HALT
0047   01036 177667      N    DEC  -73
0048   01037 000000      BFCTR BSS  1
0049   01040 000000      BFADD BSS  1
0050   01041 001042      BUFAD DEF  BUFF
0051   01042 052110      BUFF  ASC  17,THIS IS A SAMPLE PROGRAM USING THE
       01043 044523
       01044 020111
       01045 051440
       01046 040440
       01047 051501
       01050 046520
       01051 046105
       01052 020120
       01053 051117
       01054 043522
       01055 040515
       01056 020125
       01057 051511
       01060 047107
       01061 020124
       01062 044105
0052   01063 020110                ASC  13, HEWLETT-PACKARD 80-COLUMN
       01064 042527
       01065 046105
       01066 052124
       01067 026520
       01070 040503
       01071 045501
       01072 051104
       01073 020070
       01074 030055
       01075 041517
       01076 046125
       01077 046516
0053   01100 020114                ASC   7, LINE PRINTER
       01101 044516
       01102 042440
       01103 050122
       01104 044516
       01105 052105
       01106 051040
0054   01107 000012      LF    OCT  12
0055   00014             LP    EQU  14B       LINE PRINTER SELECT CODE
0056   01110 125252      CHRCT OCT  125252
0057                           END
**   NO ERRORS*
```

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section provides both general and detailed theory of operation for the interface kit. A flowchart, figure 4-1, is provided to show the overall operating details of the kit and the time relationships of the various signals.

4-3. OVERALL DESCRIPTION.

4-4. The microcircuit interface card is a multi-use interface card designed to transfer data between an HP computer and a peripheral I/O device. Two registers are provided on the card. The output storage register provides temporary storage of data sent out by the computer; the input storage register provides temporary storage of data sent to the computer from the I/O device. Control signals from the computer cause the interface card to generate a Device Command signal which turns on the I/O device. When device operation is complete, the device sends a Device Flag signal to the interface card. The computer accepts input data when the Device Flag signal is received or, if the computer interrupt system is in use, when the interface card sends an interrupt signal to the computer.

4-5. FUNCTIONAL CIRCUIT DESCRIPTION.

4-6. The following paragraphs describe operation of the various circuits contained on the interface card. For further information about the computer input/output system, refer to the instruction manuals supplied with the computer.

4-7. POWER-ON AND PRESET CIRCUIT.

4-8. When computer power is turned on or the PRE-SET switch is pressed (or EXTERNAL PRESET, depending on computer model), the computer sends POPIO(B) and CRS signals to the interface card. The POPIO(B) signal is inverted and sets the Flag Buffer FF; the Flag Buffer FF and the ENF signal set the Flag FF at computer time T2. Inverted again to its original logic level by gate U85A, the POPIO(B) signal clocks the output register. Since the IOBO lines from the computer are low (false) during turn-on or preset, the POPIO(B) signal clears the output register. The inverted CRS signal clears both the Control and Device Command FFs.

4-9. STORAGE REGISTERS.

4-10. The two storage registers on the interface card contain 16 flip-flops each. Integrated circuits U33, U53, U73, and U93 form the output storage register; U23, U43, U63, and U83 form the input storage register.

4-11. The IOO signal from the computer, delayed by the IOO Delay FF, gates computer data from the IOBO lines into the output register. Register contents are present on the output lines to the device at all times, or gated onto the output lines, as determined by the position of jumper W4.

4-12. If jumpers W5 through W8 are disconnected, the input register always contains the data that is present on the input lines from the I/O device. If the four jumpers are connected, a Device Flag signal from the I/O device gates data into the input register. Data from the input register is gated onto the IOBI lines by an IOI signal from the computer.

4-13. FLAG CIRCUIT.

4-14. The Flag FF, Flag Buffer FF, and Device Flag pulse-shaping network comprise the flag circuit. One condition that is required to transfer data between the computer and the I/O device is that the Flag FF be set. The Flag FF is always set at time T2 of the machine cycle following setting of the Flag Buffer FF. The Flag Buffer FF is set by any of three methods: during power turn-on or preset by the POPIO(B) signal, by programming an STF instruction, or by a Device Flag signal from the external device. The Flag and Flag Buffer FFs are both cleared by a CLF program instruction; the Flag Buffer FF is also cleared by an IAK signal from the computer when an interrupt request is acknowledged.

4-15. The I/O device indicates to the computer that it is ready to receive data, or that it has transferred data to the computer, by sending a Device Flag signal to the interface card. The output of the Device Flag pulse-shaping network combines with the clear-side output of the Flag FF to provide a low output from gate U87B. This low output sets the Flag Buffer FF. At computer time T2, the set-side output of the Flag Buffer FF and the ENF signal from the computer set the Flag FF. If the computer interrupt system is enabled, a program interrupt occurs after the Flag FF sets; if the interrupt system is disabled, the computer program must check the status of the Flag FF to determine when it sets.

4-16. CONTROL CIRCUIT.

4-17. The computer enables the I/O device for a data transfer by sending an STC signal to the interface card; the STC signal is the result of an STC program instruction. The Control FF and the Device Command FF form the control circuit, and both flip flops are set by the STC signal. The Control FF sets when the first STC signal is sent to the interface card and remains set until a CRS or CLC signal is received. When set, the Control FF fulfills one condition for enabling the interrupt circuit. The Device Command FF, when set, sends a Device Command signal to the I/O

device, enabling its operation. In addition to being cleared by a CRS or CLC signal, the Device Command FF is cleared as a result of a Device Flag signal or, at computer time T2, by the ENF signal, depending on placement of jumper W2.

4-18.   INTERRUPT CIRCUIT.

4-19.   The interrupt circuit, formed by the IRQ FF and associated gating, interrupts computer operation on a priority basis. A data transfer between computer and I/O device takes place during the interruption of normal program execution. When the Flag and Control FFs are set and an IEN signal is supplied from the computer, initial conditions for an interrupt are met. The resulting low output of U25A provides a low PRL signal to lower priority interface cards. The low PRL signal prevents interrupts from all lower priority devices. At time T5 (SIR signal) the low output of U35A sets the IRQ FF. Setting the IRQ FF provides FLG and IRQ signals which cause the computer to initiate a program interrupt.

4-20.   At the next time T2, the ENF signal clears the IRQ FF to allow any higher priority device to request service during the interrupt. If no higher priority device requests service, the PRH signal remains high, as do the other inputs to gate U35A, and at time T5, the SIR signal sets the IRQ FF a second time. The FLG and IRQ signals are then used to indicate the interrupt address.

4-21.   The computer sends an IAK signal to the interface card to clear the Flag Buffer FF and executes the instruction contained in memory at the interrupt address. At time T2, the ENF signal clears the IRQ FF. Clearing the Flag Buffer FF prevents the IRQ FF from being set again after the requested interrupt is enabled. The Flag FF remains set, however, to maintain the low PRL signal to lower priority devices until processing of the requested interrupt is complete. To clear the Flag FF and enable lower priority devices, a CLF instruction must be programmed.

4-22.   SKIP-ON-FLAG CIRCUIT.

4-23.   The skip-on-flag circuit allows a data transfer to occur without use of the computer interrupt system. An SKF signal is sent to the computer from the interface card to signal the computer to skip the next program instruction. If an SFS instruction is programmed (SFS signal to the interface card), the SKF signal is generated when the Flag FF is set. If an SFC instruction is programmed (SFC signal to the interface card) the SKF signal is generated when the Flag FF is cleared. When the computer receives the SKF signal, it performs the program instructions necessary to effect the data transfer.

4-24.   SELECT CODE DETECTOR.

4-25.   When the I/O device is addressed by the computer, the SCM and SCL signals are true (high) at the interface card. The IOG(B) signal is true when a program instruction pertains to any I/O device. These three signals combine at gate U54A to provide an enabling signal for this specific interface card. Thus, the interface card responds only to those program instructions specifying the select code of the I/O slot into which the card is inserted.

4-26.   PARTY LINE CIRCUIT.

4-27.   The party line circuit, composed of the Party Line FF and associated gating, is used in party line applications in which all devices are connected to a common Device Command signal line. Jumpers W1 and W2 are placed in position "C". The Party Line FF delays the Device Command signal until time T6. This allows data signals on the output lines to settle before the Device Command signal is sent. The Device Command signal is used by the device to strobe the data from the computer. The Device Command signal is removed when the Party Line FF is cleared at the beginning of time T3 of the next machine cycle.
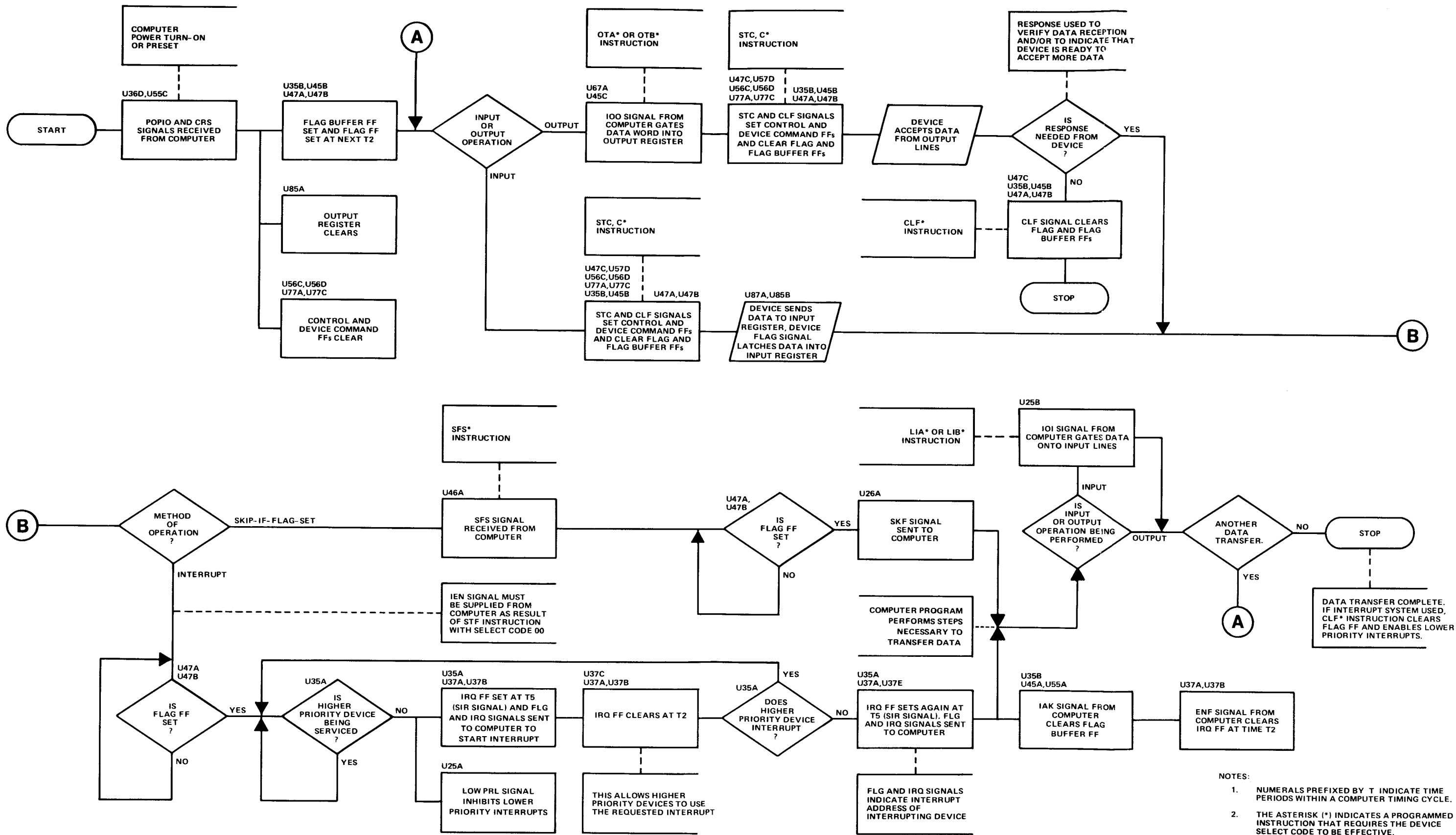
Figure 4-1. Flowchart of Operating Sequence

SECTION V

MAINTENANCE

5-1. INTRODUCTION.

5-2.   This section contains troubleshooting and diagnostic information for the interface kit. Logic diagrams, component location diagrams, a signal-to-pin index, and replaceable parts lists are included.

5-3. PREVENTIVE MAINTENANCE.

5-4.   Detailed preventive maintenance procedures and schedules are given in the computer system documentation. There are no separate preventive maintenance schedules for the interface kit; however, it is a good practice to remove dust and visually inspect the interface card whenever the card is removed from the computer.

5 5. DIAGNOSTIC TEST.

5-6.   Use the General Purpose Register Diagnostic to verify proper operation of the interface kit. The Diagnostic Program Procedure (part no. 12554-90023 for the 2114, 2115, and 2116 Computers; part no. 12554-90026 for the 2100 Computer) in the Manual of Diagnostics gives operating information for the diagnostic test. The flag, control, and interrupt circuits and the data storage registers are checked for proper operation when the diagnostic test is performed.

5-7. TROUBLESHOOTING.

5-8.   Troubleshoot the interface kit by performing the diagnostic test and analyzing any error halts that occur during the test. To further isolate troubles, refer to the signal-to-pin index (table 5-1), the integrated circuit diagrams and characteristics (figure 5-1), the appropriate parts location diagram (figure 5-2 or 5-4), and the appropriate logic diagram for the interface card (figure 5-3 or 5-5). Replaceable parts lists, in order of reference desginations, are provided in tables 5-2 and 5-3.

Table 5-1. Interface Card Signal-to-Pin Index

FROM I/O DEVICE		TO I/O DEVICE	
PIN	SIGNAL	PIN	SIGNAL
1	BIT 0	A	BIT 0
2	BIT 1	B	BIT 1
3	BIT 2	C	BIT 2
4	BIT 3	D	BIT 3
5	BIT 4	E	BIT 4
6	BIT 5	F	BIT 5
7	BIT 6	H	BIT 6
8	BIT 7	J	BIT 7
9	BIT 8	K	BIT 8
10	BIT 9	L	BIT 9
11	BIT 10	M	BIT 10
12	BIT 11	N	BIT 11
13	BIT 12	P	BIT 12
14	BIT 13	R	BIT 13
15	BIT 14	S	BIT 14
16	BIT 15	T	BIT 15
23,AA	DEVICE FLAG	22,Z	DEVICE COMMAND
24	GROUND	BB	GROUND
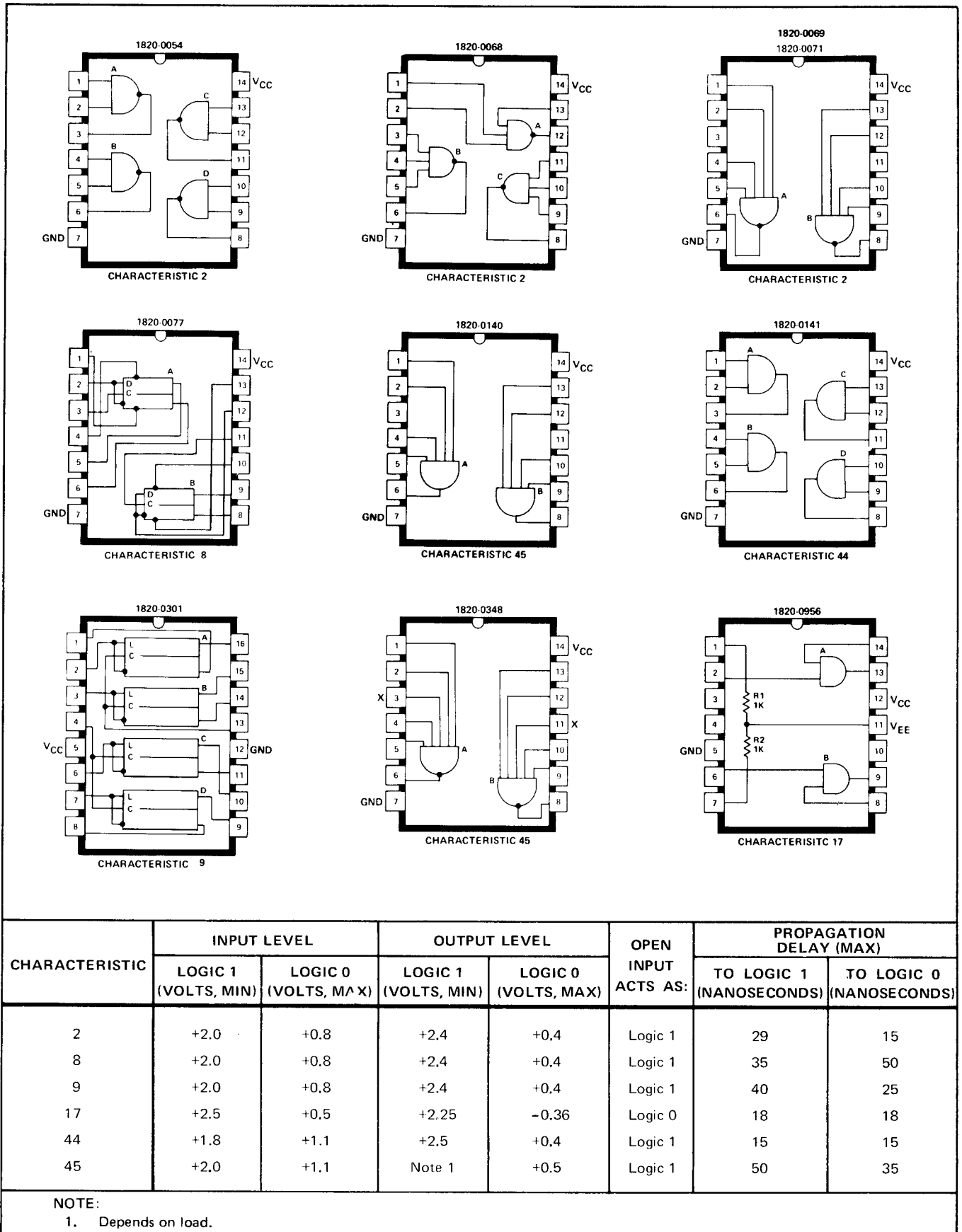
Figure 5-1. Integrated Circuit Diagrams and Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	PROPAGATION DELAY (MAX)	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
8	+2.0	+0.8	+2.4	+0.4	Logic 1	35	50
9	+2.0	+0.8	+2.4	+0.4	Logic 1	40	25
17	+2.5	+0.5	+2.25	-0.36	Logic 0	18	18
44	+1.8	+1.1	+2.5	+0.4	Logic 1	15	15
45	+2.0	+1.1	Note 1	+0.5	Logic 1	50	35

NOTE:
1. Depends on load.

Table 5-2. Card 12566-60024 (Standard and Option 001), Replaceable Parts

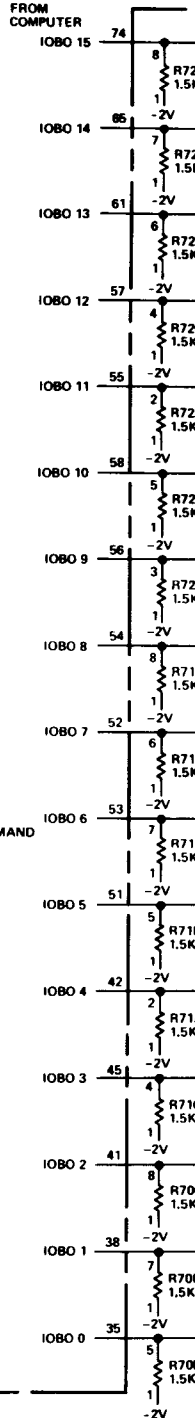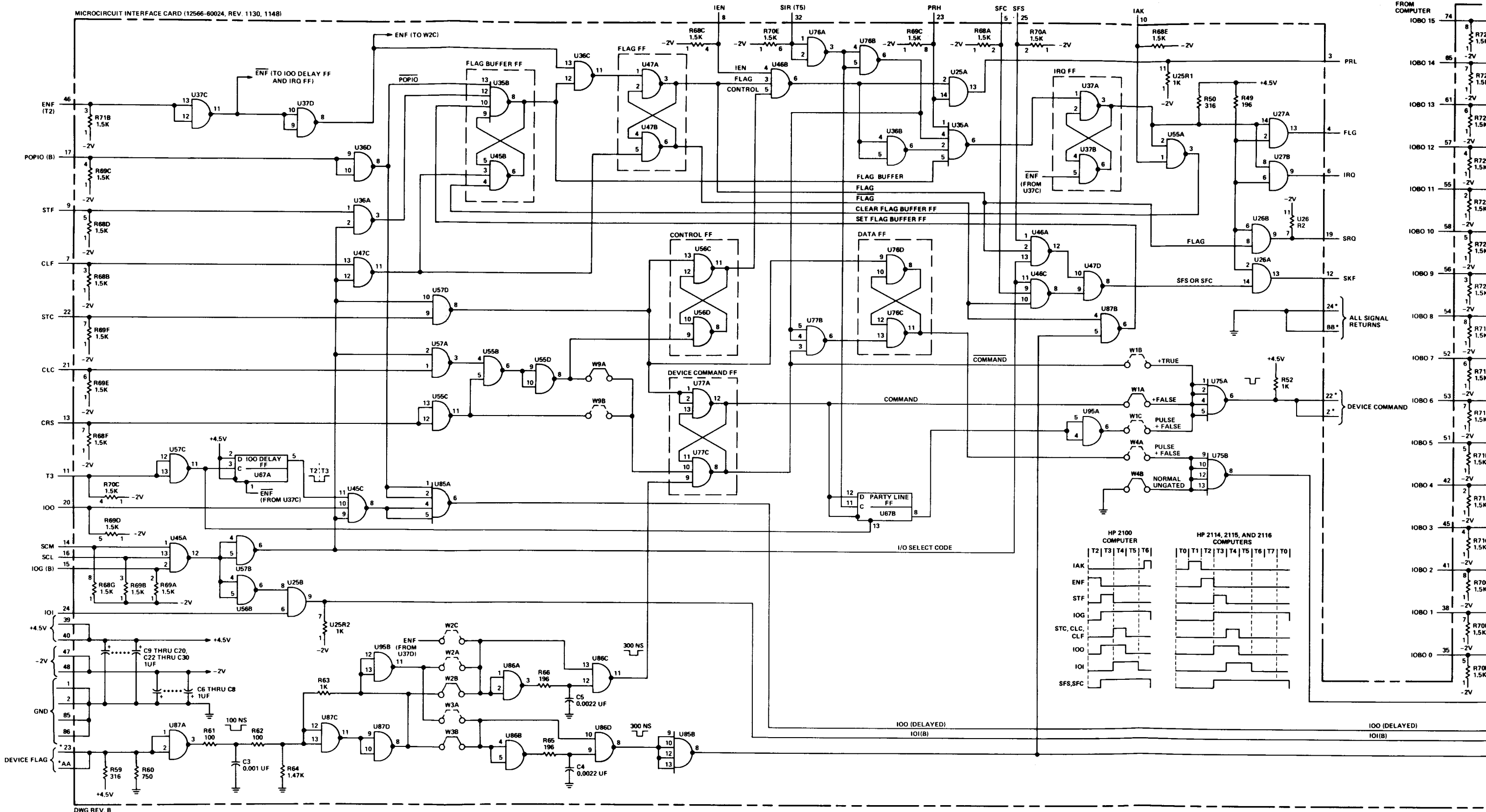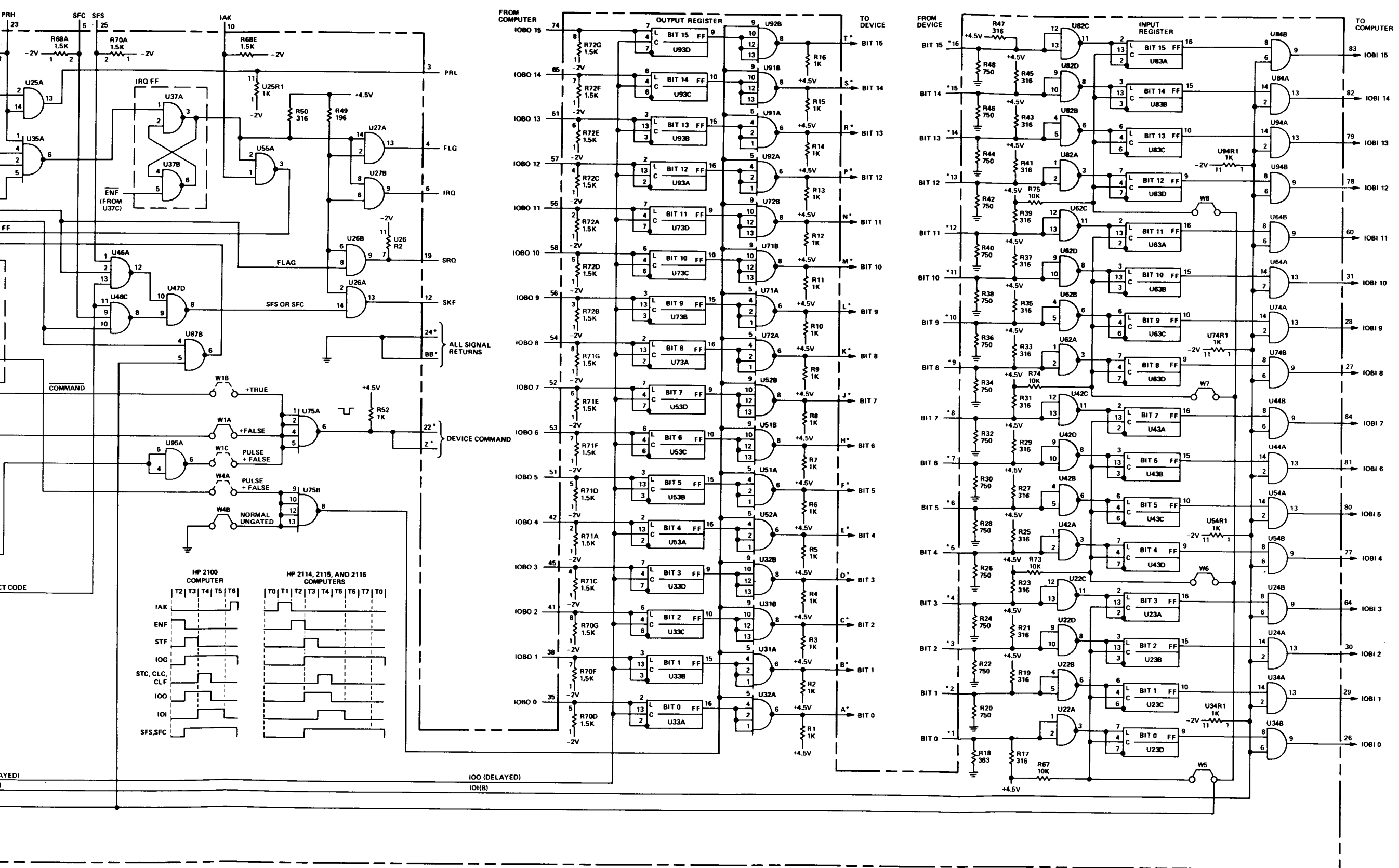| REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C3	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C4,5	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154
C6 thru C20, C22 thru C30	0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X-9035A2
R1 thru R16,52,63	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F
R17,19,21,23,25,27,29,31,33,35,37, 39,41,43,45,47,50,59	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F
R18,20,22,24,26,28,30,32,34,36,38, 40,42,44,46,48,60	0757-0420	Resistor, Fxd, Flm, 750 ohms, 1%, 1/8W	28480	0757-0420
R49,65,66	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R61,62	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401
R64	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R67,R73 thru R75	0757-0442	Resistor, Fxd, Flm, 10k, 1%, 1/8W	14674	MF4CD1002F
R68 thru R72	**1810-0020**	**Resistor, Network (7 fxd flm resistors)**	**28480**	**1810-0020**
U22,36,37,42,47,55,56,57,62,76,82, 86,87,95	1820-0054	Integrated Circuit, TTL	01295	SN7400N
U23,33,43,53,63,73,83,93	1820-0301	Integrated Circuit, TTL	01295	SN7475N
U24 thru U27,34,44,54,64,74,84,94	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U31,32,51,52,71,72,91,92	1820-0348	Integrated Circuit, DTL	01295	SN15844N
U35	1820-0069	Integrated Circuit, TTL	01295	SN7420N
U45,46,77	1820-0068	Integrated Circuit, TTL	12040	SN7410N
U67	1820-0077	Integrated Circuit, TTL	01295	SN7474N
U75,85	1820-0071	Integrated Circuit, TTL	01295	SN7440N
W1 thru W9	8159-0005	Jumper Wire	28480	8159-0005
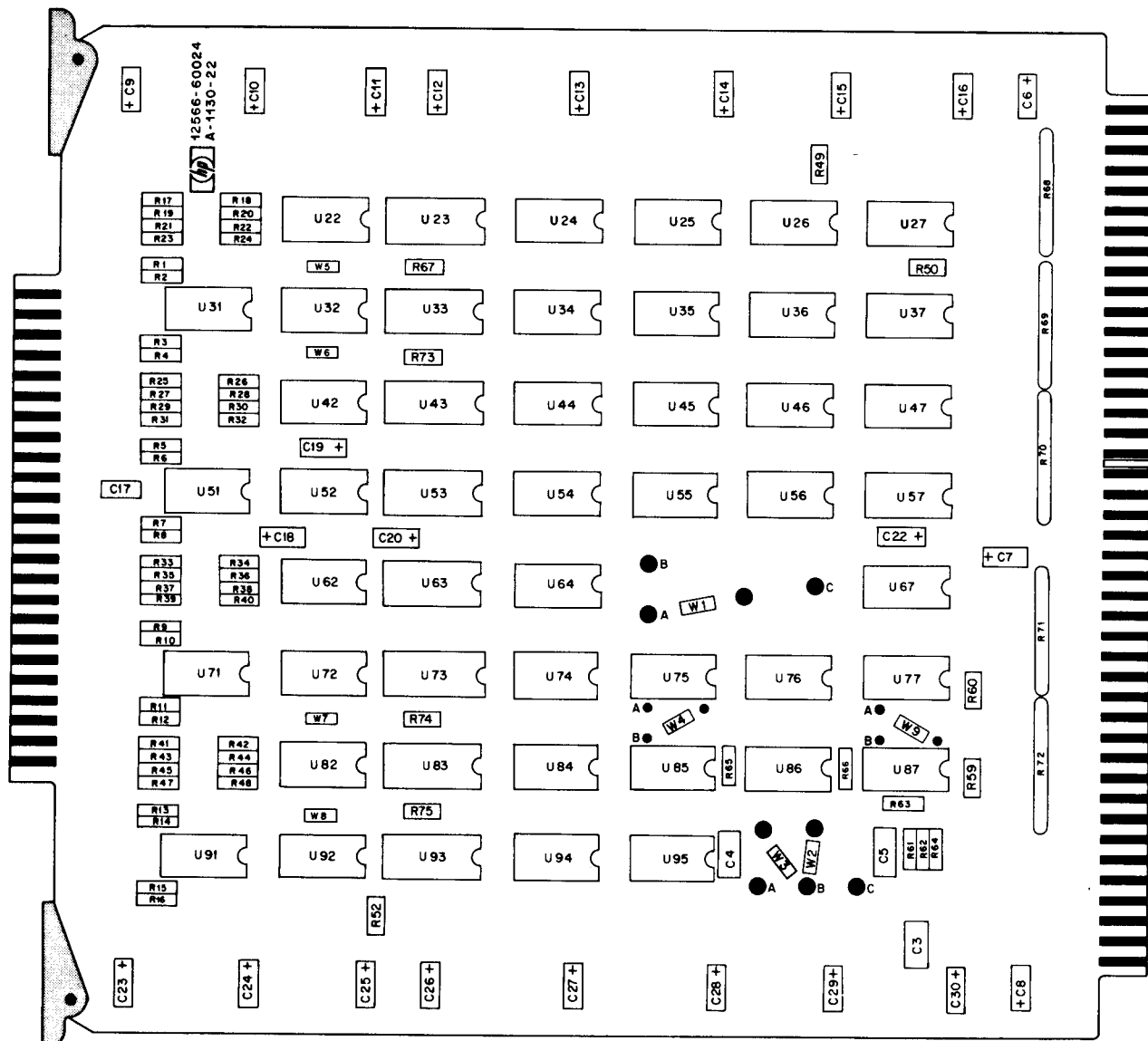
12566B

DWG REV B

THIS DIAGRAM ALSO APPLIES TO CARD REV A-1148-22 AND B-1148-22

Figure 5-2. Card 12566-60024 (Standard and Option 001), Parts Location Diagram

MICROCIRCUIT INTERFACE CARD (12566-60024, REV. 1130, 1148)

FROM COMPUTER

IEN 8
SIR (T5) 32
PRH 23
SFC SFS 25
IAK 10

ENF (TO W2C)

ENF (TO IOO DELAY FF AND IRQ FF)

POPIO

FLAG BUFFER FF

FLAG FF

U36C
U47A
U47B
U45B
U35B

IEN
FLAG
CONTROL

U46B
U76A
U76B

FLAG BUFFER
FLAG
FLAG

U25A
U36B
U35A

IRQ FF
U37A
U37B

ENF (FROM U37C)

U55A
U27A FLG 4
U27B IRQ 6

ENF (T2) 46
POPIO (B) 17
STF 9
CLF 7
STC 22
CLC 21
CRS 13
T3 11
IOO 20

R71B 1.5K
R69C 1.5K
R68D 1.5K
R68B 1.5K
R69F 1.5K
R69E 1.5K
R68F 1.5K
R70C 1.5K
R69D 1.5K
-2V

U37C
U37D
U36D
U36A
U47C
U57D
U57A
U55B
U55D
U57C
U45C
U85A

CONTROL FF
U56C
U56D

DATA FF
U76D
U76C
U77B

DEVICE COMMAND FF
U77A
U77C

D IOO DELAY FF
U67A
ENF (FROM U37C)

D PARTY LINE FF
U67B

CLEAR FLAG BUFFER FF
SET FLAG BUFFER FF

FLAG
U46A
U46C
U47D
U87B

SFS OR SFC

COMMAND
COMMAND

I/O SELECT CODE

U26B SRQ 19
U26A SKF 12
R2 U26
-2V

W1B +TRUE
W1A +FALSE
W1C PULSE + FALSE
W4A PULSE + FALSE
W4B NORMAL UNGATED

U75A
U95A
U75B

R52 1K
+4.5V

DEVICE COMMAND

ALL SIGNAL RETURNS

R50 316 R49 196 +4.5V
U25R1 1K
-2V

W9A
W9B

IOBO 15 74
IOBO 14 65
IOBO 13 61
IOBO 12 57
IOBO 11 55
IOBO 10 58
IOBO 9 56
IOBO 8 54
IOBO 7 52
IOBO 6 53
IOBO 5 51
IOBO 4 42
IOBO 3 45
IOBO 2 41
IOBO 1 38
IOBO 0 35

SCM 14
SCL 16
IOG (B) 15
IOI 24

U45A
U57B
U25B
U56B

R68G 1.5K R69B 1.5K R69A 1.5K
U25R2 1K
-2V

+4.5V 39
40
-2V 47
48
GND 1
2
85
86
DEVICE FLAG 23
AA

C9 THRU C20, C22 THRU C30 1UF
C6 THRU C8 1UF

U87A
R61 100 R62 100
100 NS
C3 0.001 UF
R64 1.47K

R59 316 R60 750
+4.5V

U87C
U87D
R63 1K

U95B
ENF (FROM U37D)

W2C
W2A
W2B
W3A
W3B

U86A
R66 196
U86C 300 NS
C5 0.0022 UF

U86B
R65 196
U86D 300 NS
C4 0.0022 UF

U85B

IOO (DELAYED)
IOI (B)

IOO (DELAYED)
IOI (B)

PRL 3

HP 2100 COMPUTER
T2 T3 T4 T5 T6

HP 2114, 2115, AND 2116 COMPUTERS
T0 T1 T2 T3 T4 T5 T6 T7 T0

IAK
ENF
STF
IOG
STC, CLC, CLF
IOO
IOI
SFS, SFC

DWG REV. B

Figure 5-3. Card 12566-60024 (Standard and Option 001), Logic Diagram

Table 5-3. Card 12566-60025 (Option 002), Replaceable Parts

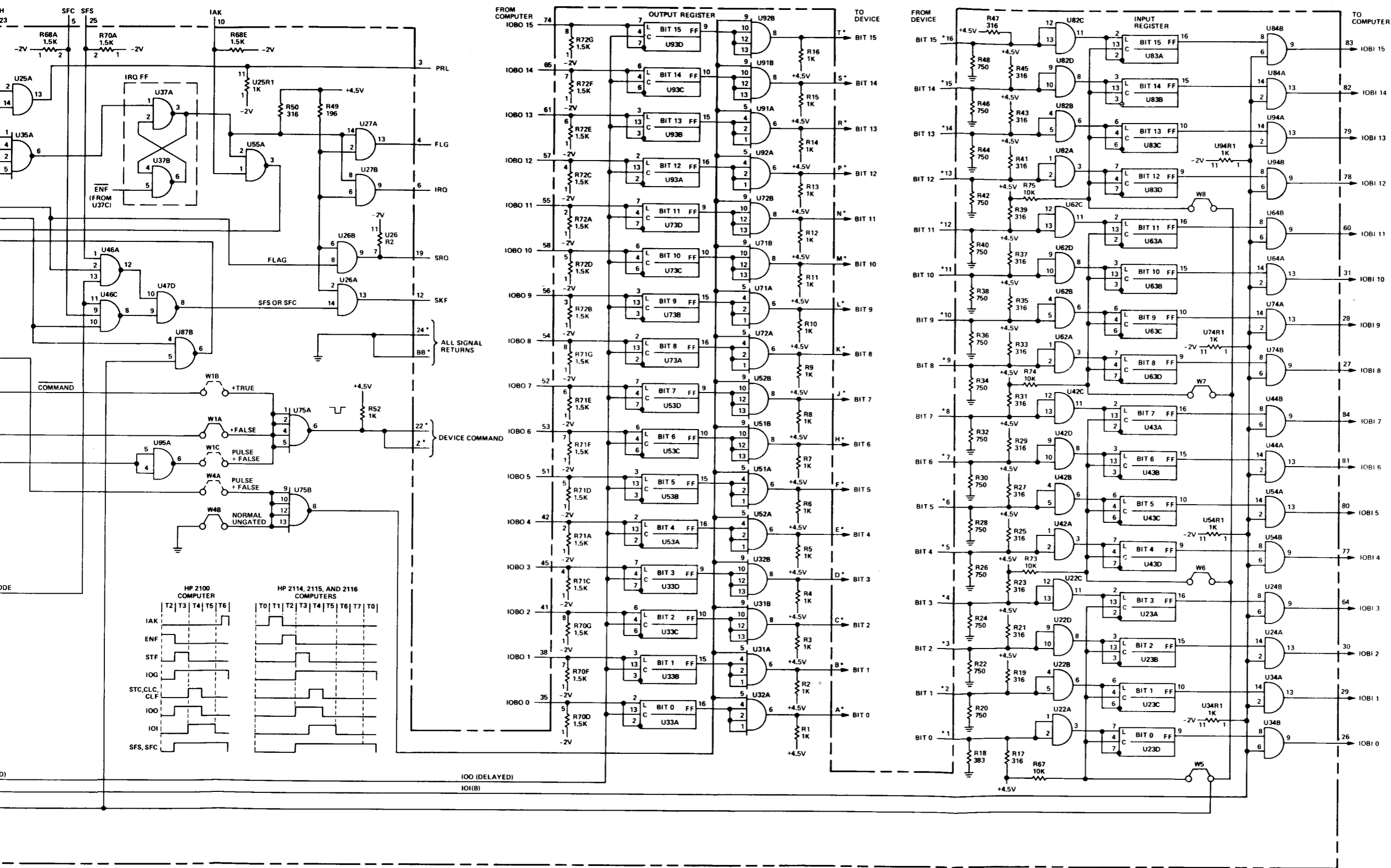| REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C3	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C4,5	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154
C6 thru C20,C22 thru C30	0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X-9035A2
R1 thru R16,52,63	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F
R17,19,21,23,25,27,29,31,33,35,37, 39,41,43,45,47,50,59	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F
R18,20,22,24,26,28,30,32,34,36,38, 40,42,44,46,48,60	0757-0420	Resistor, Fxd, Flm, 750 ohms, 1%, 1/8W	28480	0757-0420
R49,65,66	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R61,62	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401
R64	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R67,R73 thru R75	0757-0442	Resistor, Fxd, Flm, 10k, 1%, 1/8W	14674	MF4CD1002F
R68 thru R72	1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020
U22,42,62,82	1820-0141	Integrated Circuit, TTL	04713	MC3001P
U23,33,43,53,63,73,83,93	1820-0301	Integrated Circuit, TTL	01295	SN7475N
U24 thru U27,34,44,54,64,74,84,94	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U31,32,51,52,71,72,91,92	1820-0140	Integrated Circuit, TTL	04713	MC3026P
U35	1820-0069	Integrated Circuit, TTL	56289	SN7420N
U36,37,47,55,56,57,76,86,87,95	1820-0054	Integrated Circuit, TTL	01295	SN7400N
U45,46,77	1820-0068	Integrated Circuit, TTL	12040	SN7410N
U67	1820-0077	Integrated Circuit, TTL	01295	SN7474N
U75,85	1820-0071	Integrated Circuit, TTL	01295	SN7440N
W1 thru W9	8159-0005	Jumper Wire	28480	8159-0005
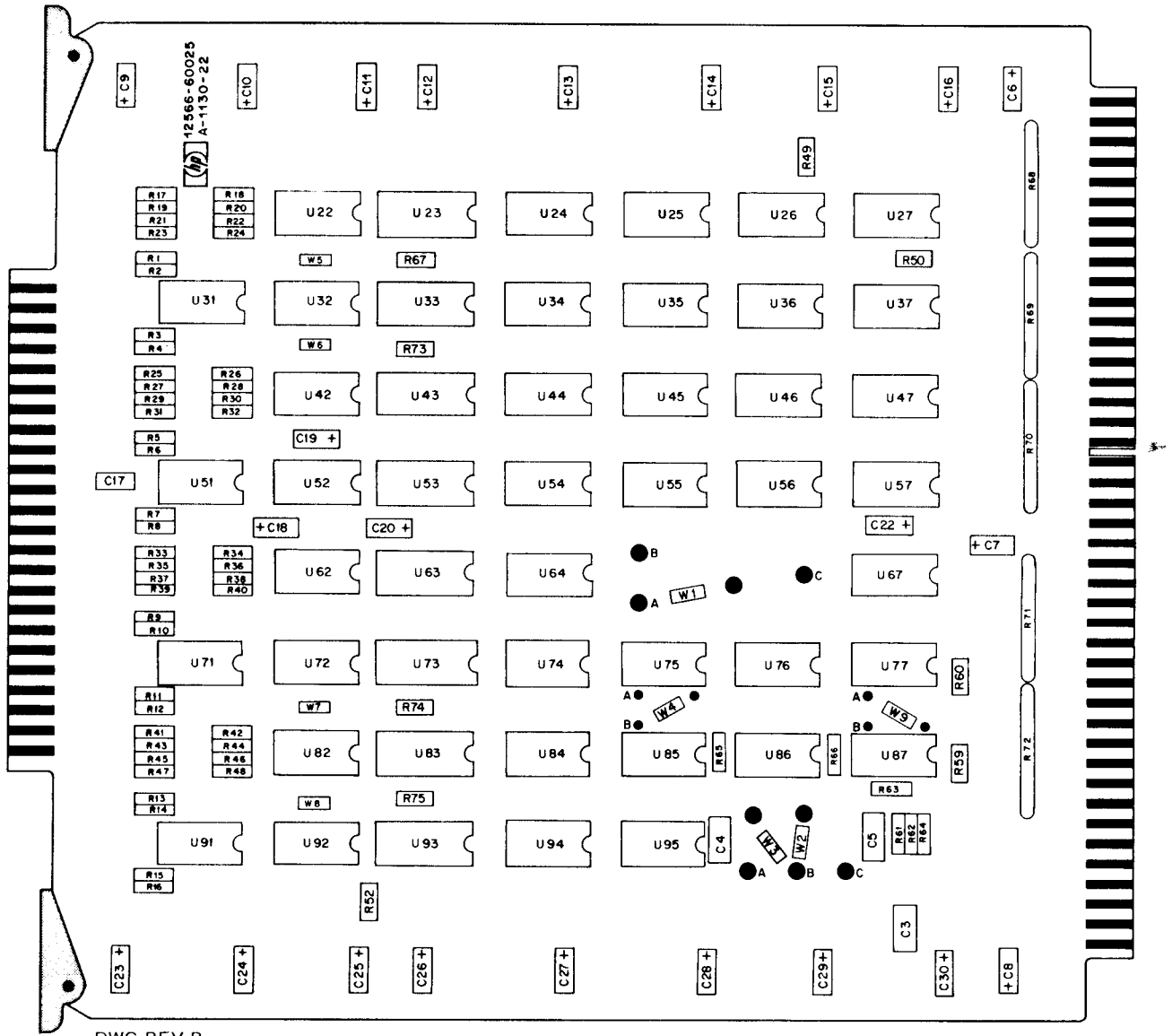
12566B

Figure 5-4. Card 12566-60025 (Option 002), Parts Location Diagram
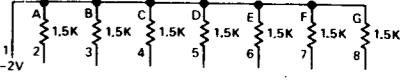
Figure 5-5. Card 12566-60025 (Option 002),
Logic Diagram

SECTION VI

REPLACEABLE PARTS

6-1.   INTRODUCTION.

6-2.   This section contains information for ordering replacement parts for the interface kits. Table 6-1 lists parts in alphanumeric order by HP part number and lists the following information for each part.

   a. Description of the part. (Refer to table 6-2 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

   b. Typical manufacturer of the part in a five-digit code; refer to the list of manufacturers in table 6-3.

   c. Manufacturer's part number.

   d. Total quantity of each part used in the applicable interface kit.

6-3.   A separate parts list is provided in section V along with the parts location view for the standard and optional interface cards. The parts lists present the parts in alphanumeric order by reference designation.

6-4.   ORDERING INFORMATION.

6-5.   To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the back of this manual for addresses.) Specify the following information for each part ordered:

   a. Interface kit model number.
   b. Circuit card revision number.
   c. Hewlett-Packard part number.
   d. Description of each part.
   e. Circuit reference designation.

Table 6-1. Numerical Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ	
				STD & OPT 001	OPT 002
0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153	1	1
0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154	2	2
0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X-9035A2	24	24
0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440	3	3
0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F	18	18
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F	18	18
0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	28480	0757-0401	2	2
0757-0420	Resistor, Fxd, Flm, 750 ohms, 1%, 1/8W	28480	0757-0420	17	17
0757-0442	Resistor, Fxd, Flm, 10k, 1%, 1/8W	14674	MF4CD1002F	4	4
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094	1	1
1251-0332	Connector, 24-pin	28480	1251-0332	1	1
1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020	5	5
1820-0054	Integrated Circuit, TTL	01295	SN7400N	14	10
1820-0068	Integrated Circuit, TTL	01295	SN7410N	3	3
1820-0069	Integrated Circuit, TTL	01295	SN7420N	1	1
1820-0071	Integrated Circuit, TTL	01295	SN7440N	2	2
1820-0077	Integrated Circuit, TTL	01295	SN7474N	1	1
1820-0140	Integrated Circuit, TTL	04713	MC3026P	0	8
1820-0141	Integrated Circuit, TTL	04713	MC3001P	0	4
1820-0301	Integrated Circuit, TTL	01295	SN7475N	8	8
1820-0348	Integrated Circuit, DTL	01295	SN15844N	8	0
1820-0956	Integrated Circuit, CTL	07263	U6A995679X	11	11
8120-1846*	Cable, 36-twisted pair, 15 feet	28480	8120-1846	1	1
8159-0005	Jumper Wire	28480	8159-0005	9	9
5060-8339*	Connector Kit, 48-pin	28480	5060-8339	1 (STD ONLY)	1
5060-8340*	Connector Kit, 24-pin	28480	5060-8340	1 (OPT 001 ONLY)	0
12566-60024	Microcircuit Interface Card	28480	12566-60024	1	0
12566-60025	Microcircuit Interface Card	28480	12566-60025	0	1
12566-90015	Operating and Service Manual	28480	12566-90015	1	1

*Not supplied with option 003.

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