analog-digital devices manual

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GRI
ANALOG-DIGITAL
DEVICES

MANUAL

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TABLE OF CONTENTS

APPENDICES

PRINTS

CHAPTER I

ANALOG/DIGITAL DEVICES

1.0 Introduction:

The GRI complement of peripherals includes a line of Analog-Digital devices* mounted on small device operator cards that plug into the rear I/O section of the GRI family of computers.

The line is intended for modest applications of analog equipment, i.e. those which do not have large numbers of inputs or stringent analog signal handling requirements. The line is simple to use and install and will satisfy all general applications for analog front-end in a convenient manner.

Analog signals are generally handled by A to D converters of varying precision and speed capabilities. When choosing A to D equipment for use in a system, the user is urged to remember that the measurements obtained from an A to D will be no more accurate than the transducers that produced the measurements and that accuracy and speed are two parameters which are somewhat inconsistent in A to D conversion equipment.

There are two ways of viewing a word which is produced by an A to D converter. A 10-bit unipolar A to D has a full scale calibration of 10.23 volts. Ten bits represents a maximum count of 1023. The value of the least significant bit is then 10.23v/1023 or 0.01v.

*Interchangeable between GRI 99 and GRI 909 computers.

We then say the A to D resolution is 10mv per bit. If the A to D word is viewed as an integer (right justified), we have only to multiply the binary word by 10 to obtain the voltage represented by the word in millivolts. In normal use, the reading in volts is meaningless. The voltage is usually produced by a transducer and represents physical units such as pressure, temperature, flow, etc. The full scale calibration is expressed as, say 102.3 psi. The A to D word may be viewed as a left justified fraction (binary point to the left of the most significant bit). The conversion in this case to engineering units is done by multiplying the A to D reading by the full scale factor using conventional fixed point arithmetic. Floating point arithmetic may also be used by converting the A to D fraction to floating point format. The exponent for the A to D would be 0. Note that in a system requiring a selectable gain amplifier in front of an A to D, it is a simple matter to use floating point if the amplifier gain ranges are chosen as powers of 2, i.e. 2, 4, 8, 16, etc. The exponents then become 1, 2, 3, etc.

Multiplexers are used in front of an A to D to allow many voltages to be sampled by a single A to D. GRI multiplexers are solid state (FET), high level devices. That is, they are not capable of handling micro-volt level signals such as those produced by thermcouples. For small numbers of such low level inputs, separate amplifiers may be used to convert to high level signals before multiplexing.

Voltages may be generated in a system through a D to A converter. The conversion from a binary word representing engineering units is handled in the reverse manner as described earlier for A to D converters.

CHAPTER II

ANALOG TO DIGITAL CONVERSION

2.0 Introduction:

There are two common varieties of A to D converters. These are the successive approximation types and the integrating or counting types. These A to D converters are closed loop, simple, servo systems and all function in the same general fashion. A register is used to hold the digital representation of the voltage to be measured. This digital number is converted to an analog voltage which is some percentage of the full scale analog input range. The converted voltage is compared to the incoming voltage in a difference amplifier. This amplifier is called a comparitor and produces a go no-go digital output that essentially indicates equality or inequality between the analog representation of the register and the incoming unknown voltage. The register contents are controlled by logic, whose basic control signal comes from the comparitor. Thus, as long as the comparitor indicates an error (inequality), the control logic will continue to modify the register until equality or equilibrium is reached. Fig. 2-1 is a general block diagram of an A to D converter.

The manner in which the register is altered determines the basic type of converter. The successive approximation converter alters the digital register with a series of approximations that cause the guessed analog value to follow the series

$$\frac{1}{2}V_{FS}+\frac{1}{4}V_{FS}+\frac{1}{8}V_{FS}+. . +\frac{1}{2^n}V_{FS}$$

Where V_{FS} is the full scale value of the voltage, and n is the number of bits in the converter. The control logic will set each guess and extinguish it if the comparitor indicates that

$$V_{GUESS} > V_{IN}$$

If, however, $V_{GUESS} \leq V_{IN}$, the guess is left in the register and the next lower order is added to those previously taken and left. As the progression approaches the low order bit of the register, the increments added to the guessed voltage get smaller and the guessed voltage converges on the actual voltage. Fig. 2-2 shows an eight-bit successive approximation converter converging on a value which is less than 3/4 of full scale. The speed at which the approximations may be taken is a function of the speed of the comparator, and the speed of the ladder network which converts the guess register to a voltage. The speeds of these two will vary with the magnitudes of the voltages involved, and the accuracy of conversion required (number of bits of precision). Speeds on the order of 750ns per bit to 2 us per bit are typical. The total conversion time is, of course, the time per bit times the number of bits in the converter. This is exclusive of any settling time required for signal conditioning such as high impedance amplifiers in front of the comparator. Comparators are generally low input devices and will require a high impedance amplifier in front of them if multiplixing is used or if the signal source cannot work into a low inpedance.

Another form of converter drives the register as a counter that starts at 0 as the initial guess and increments the contents by 1 as long as the comparator indicates that

$$V_{GUESS} \leq V_{IN}$$

The counting stops when $V_{GUESS} \geq V_{IN}$. This converter requires, on the average, $\frac{1}{2}(2^n - 1)t_B$ u seconds where t_B is the conversion time per bit and n is the number of bits in the conversion register. Note that the maximum conversion time will take twice as long if the measured voltage is the full scale value. A ten bit converter with a bit time of 1 us will take a maximum of 1.023ms to convert a full scale value.

The counting type of converter, although less expensive, has the drawback of not being very good at measuring AC voltages of any significant frequency. This time of conversion is also called the aperture of the A to D. The aperture of any type of A to D may be improved by using a sample and hold amplifier in front of the A to D.

There are many other types of A to D converters, most of which are variations on the two standard themes presented here.

2.1 Specifications:

The GRI-909 line of A to D converters use the successive approximation technique and cover a wide range of capabilities. All are mounted on the small device operator cards that plug into the rear section of the computer.

Electrical:

Input

Analog Input Voltage Ranges	0V to +10v full scale
	0V to +5v full scale
	-5v to +5v full scale
	-10v to +10v full scale
Input Overvoltage	±15 VDC
Input Impedance	10 Megohms

Performance:

Resolution	1 part in 256 (8 bit)
	1 part in 1024 (10 bit)
	1 part in 4096 (12 bit)
Accuracy	.025% of FS ±1/2 LSB

Coding	Binary (unipolar) (Bit 15=MSB)
	2's complement (bipolar)
	(Bit 15 = sign)
	(Bit 14 = MSB)
Temperature coefficient	±10 ppm/°C of FS
Conversion rate	1.3 us per bit (low speed)
	.75 us per bit (high speed)

Conversion time (including settling)

8 Bit	10 Bit	12 Bit
14.5 us	21 us	23.6 us (low speed)
6.1 us	15.5 us	17 us (high speed)

Input power	±A 40ma
	+5v 640ma

Environmental:

Operating temperature range	0°C to 50°C
Storage	-55°C to +85°C
Relative humidity	95% non-condensing

2.2 Device Operator:

The device operator is connected as a source of data only. The system address may be chosen via a set of staples according to the instructions in Appendix B. The suggested mnemonic for the operator is ADC and the device is normally set for a system address of 65 for factory test purposes. Data is transferred from the ADC by any instruction that references it as a source, e.g.:

%RASX	MACHINE CODE
RR ADC,AX	65 0000 11
RMID ADC,0	65 0010 06 000000
JC ADC,ETZ,100	65 0100 03 000100

The ADC must be started by a function output command. Its value should not be read until the ADC input ready flag sets, indicating that conversion has been completed. If the converter has been in use, its input ready flag should be cleared by the same function command that starts the conversion, e.g:

```
% RASX                   MACHINE CODE          ; Action

FO CLIF,ADC               02 1000  65      ; clear IRDY flag

FO STRT,ADC               02 0001  65      ; start ADC

FO CLIF STRT, ADC         02 1001  65      ; clear & start ADC
                              [0]
SF ADC, [NOT] IRDY        65 100   02
                              [1]
```

The ADC is also provided with an interrupt connection to allow the IRDY flag to automatically notify the computer upon conversion completion. The Interrupt Status Register bit and interrupt jump address may be chosen by the user according to the instructions in Appendix B. These are normally set at the factory for test purposes to:

ISR bit 12

Interrupt Address 52 (53, 54)

The ISR bit is set, typically, by an instruction such as:

```
I 10000 TO ISR       06 0010 04
                        010000
```

Ths interrupt system will cause the SC on interrupt to be stored in loc 52. Operation of the program resumes at loc 53 which normally contains a non-trap disturbing jump to the service routine such as:

```
I ADSER-1 TO SC      53:  06 0010 07
                     54:  ADSER-1
```

The conversion rate (1.3us or .75us per bit) is used to calculate how long the flag will be down after start of a conversion. Thus, in a 10-bit low speed ADC, the conversion time will be 13us. There is, however, a settling time spec of 8us for the ADC's amplifiers. This requirement is only of interest if the input to the ADC is switched through a multiplexer, a sample and hold unit, or a variable gain amplifier. When such switching occurs, the user must provide sufficient time (8us) between the switching of the input voltage and the starting of the ADC in order to obtain a digitized reading that is within the accuracy spec of the ADC. Conversion and settling times are given in table 2-3 for the various ADC units available.

2.3 Programming:

Programming the ADC is a relatively simple matter. A simple service subroutine which excludes any settling time, returns with the ADC value in AX after starting the ADC:

```
ADSER:  FO CLIF STRT, ADC       ; START ADC
        SF ADC,IRDY
        MRI .-2,SC              ; WAIT FOR CONVERSION
        RR ADC,AX
        RR TRP,SC               ; RETURN
```

The settling time requirement is logically considered with the multiplexing subroutine.

Typical conversion to volts of the value in AX is handled as follows:

```
; CONVERT TO VOLTS
  CONV:  RMI TRP,0
         MR FS,AY          ;get full scale value
         JU $SMY           ;multiply by AX (ADC)
         MS SF,P1          ;add 1 to scale factor
         JU $SSC           ;normalize result
         Wrd  SF           ;scale factor of FS value
         JU $SUS           ;split into integer & fraction
         Wrd  SF
         JUD CONV+1        ;exit with integer in AX, frac. in AY
    FS:  WRD X             ;full scale value as a fraction
    SF:  WRD Y             ;scale factor of full scale value
```

The full scale value is stored as a fraction along with a scale factor. Thus, if

$$FS = 5.1175_{10}v = 5.0741_8 v$$

$$= 0.50741 \times 8^1$$

$$SF = 3 \ (2^3 = 8^1)$$

The full scale bit values for the various size A to D's available are as follows:

Accuracy

	FS / LSB	8	10	12
Range	+5v	5.10v / 20mv	5.115v / 5mv	NA / NA
	+10v	10.20v / 40mv	10.23v / 10mv	10.2375 / 2.5mv
	±5v	5.08v / 40mv	5.11v / 10mv	5.1175 / 2.5mv
	±10v	10.16v / 80mv	10.22v / 20mv	10.235 / 5mv

NOTE: Unipolar ADC's are connected with BIT 15 = MSB. To put this in proper form for fixed point operation, the user may simply shift the data right one position while reading the ADC (making sure the LINK was clear before doing this). Thus:

ADC R1 TO D TABLE

or ADC R1 TO AX

will put the ADC reading in a positive fraction format at the destination end as shown in the following table.

% of FS	ADC RDG (Unipolar)		Shifted rt 1	
	MSB	LSB	MSB	LSB
0	0 . . .	0	0	0
.				
.				
50	1 . . .	0	0 1 . . .	0
.				
.				
100	1 . . .	1	0 1 . . .	1
			Binary Pt	

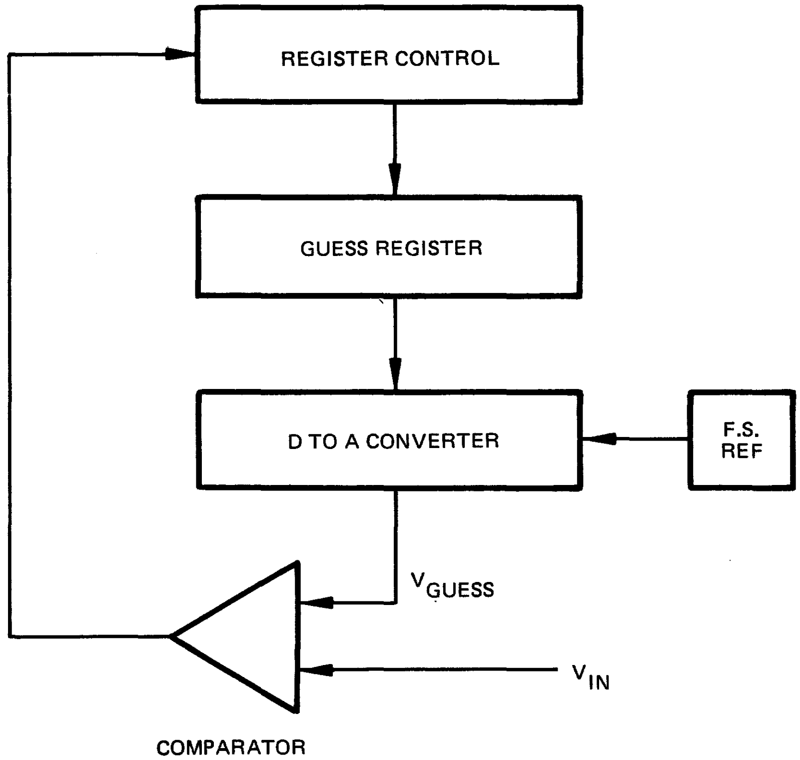


Figure 2-1.

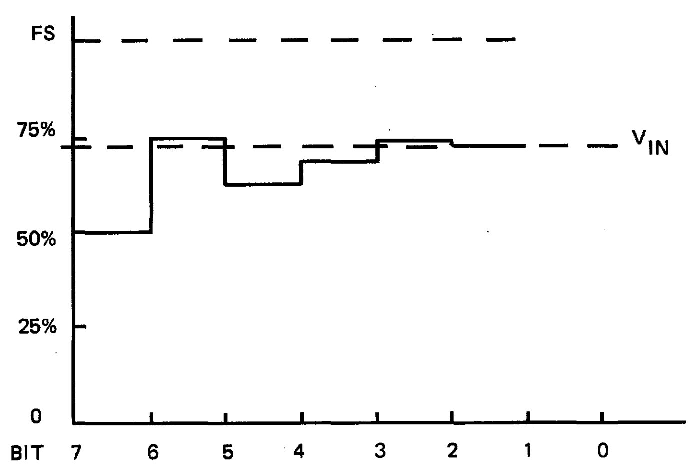


Figure 2-2.

WORD SIZE	8H	8L	10H	10L	12H	12L
CONVERSION TIME(us)	4	10.4	7.5	13	9	15.6
SETTLING TIME (us)	2.1	4.1	6	8	6	8

H=High speed ADC   L=Low speed ADC

TABLE 2-3

CHAPTER III

MULTIPLEXING ANALOG INPUTS

3.0 Whenever a multiplicity of analog signals are to be measured in a computer system, the multiplexer becomes the switch which commutates the signals into the single input of the ADC. The GRI line of multiplexers is available in 8, 16, 24, or 32 inputs on a single, small device operator card that plugs into the rear of the computer.

3.1 Specifications:

Input:

Type	single ended
Range	$\pm$5v, $\pm$10v
Overvoltage	$\pm$15v maximum
"ON" resistance	300 ohms (typical)
"OFF" resistance	100 Megohms (typical)

Performance:

Transfer accuracy	0.01% of full scale
Settling time	1 us to .01% of FS
Input power.	+A 3 ma (8 channels)
	-A 8 ma (8 channels)
	+5 26 ma (8 channels)
	+5 328 ma (logic)

Environmental:

Operating temperature range	0°C to +50°C
Storage temperature	-55°C to +85°C
Relative humidity.	95% non-condensing

3.2 Device Operator:

The device operator is connected as a source and destination of data. The system address may be chosen via a set of staples according to the instructions in Appendix B. The suggested mnemonic for the operator is MUX and the device is normally set for a system address of 64 for factory test purposes. Data transfers to and from the operator may be made by any instructions that reference it as a source, destination, or both, e.g:

% RASX	MACHINE CODE
RR AX,MUX	11 0000 64
RS MUX,P1	64 0100 64
MRID 0,MUX	06 0010 64 000000
JC MUX,ETZ,100	64 0100 03 000100

There are no function commands or status flags associated with the MUX. The settling time of the MUX is 1 us to .01% of FS and therefore requires no special coding of the multiplexing routine. After loading the MUX with a channel address, the next instruction execution period cannot normally occur within less than 1.76 us, thus allowing plenty of time for the MUX to settle. The A to D, however, requires a settling period of 6 or 8 us (see table 2-3). This is the time required for the amplifiers in the ADC to settle after being switched from one input to another through the MUX. This time must be allotted by the program prior to issuing the start ADC command. If this is not done, the converted value may be in error.

3.3 Programming:

Programming the MUX requires a service routine that will determine what order the channels are scanned. The simplest scan order is a binary incremental scan and simply requires that the MUX register be incremented each time a new channel is selected. The MUX register is a 5-bit register and will count modulo 32. Thus, if all 32 channels are implemented on the MUX operator, a scan of all channels simply requires the detection of 0 in the MUX register each time it is incremented. The front end settling time of the ADC (e.g. 8us) must be implemented here. A subroutine to scan 32 channels and put their values in a table might look like this:

```
SCAN:  RMI TRP,0
       MRI VTAB-1,AX          ; initialize value table
       RM AX,POINT
(3)    JU ADSER               ; get a reading
       RMID AX,0              ; store it
       POINT=.-1
       RS MUX,P1              ; next channel
(1)    JCD MUX,ETZ,SCAN+1     ; exit, scan done
(2)    JU SCAN+6
VTAB:  loc .+40               ; value table
```

The settling time for the ADC front end occurs during instructions (1), (2), and (3) and amounts to 5 cycles or 8.8 us seconds. which should be sufficient for the low speed ADC series. When the scan is complete, the MUX register will contain 0 and this will be the first point scanned when the routine is re-entered.

If the MUX is not fully implemented (32 channels), the addresses of those points not implemented must not be selected or the input to the ADC will be an open circuit. This will cause the amplifier on the ADC to saturate and give a full scale reading. To avoid addressing non-existent points, the SCAN routine should count the number of points until the maximum number (8, 16, or 24) has been scanned and then exit.

CHAPTER FOUR

DIGITAL TO ANALOG CONVERSION

4.0 The GRI series of D to A converters are binary weighted ladder networks with a buffer amplifier on the output. The interface board contains a general purpose (full 16 bit) register with the most significant bits connected to the DAC. The register is a standard GP register and is therefore a full parallel transfer type of register, thus avoiding the problems of transient outputs caused by "reset-set" types of registers. The GRI DAC line, therefore, does not require double buffering since these transient spikes cannot occur during loading of the register.

The D to A ladder network is simply a programmable voltage divider connected to a reference source. It is programmable in that there are switches on the legs of the network that are controlled by the bits of the binary word which is to be converted to an analog representation. As bits of the data word are turned on or off, the switches in the various legs of the ladder open and close, and the net value of the voltage divider changes, thus changing the output voltage. The reference voltage is set for full scale and therefore the output is always a percentage of the full scale reference value. Figure 4-1 is a typical ladder network with switches and output amplifier. This arrangement is, in reality, a current summing type of network as opposed to the divider type mentioned earlier. If the LSB switch is closed to the reference source and all other switches are opened (connected to ground), a current is produced in the LSB leg and it gets divided by a factor of 2 at each junction. The contribution of that current to the summing junction is binary weighted according to the number of junctions through which it passed (number of junctions = number of bits in conversion word). Thus, the LSB contributes a current to the amplifier summing junction which causes an output $E_0 = \frac{E_{Ref}}{(2^n-1)}$, e.g. if $E_{Ref} = 10.23v$ and $n = 10$ bits, $E_0 = \frac{10.23}{1023} = 10mv$. Each leg by itself will cause twice the voltage generated by the previous leg to appear at the output. When all switches are closed, the output is the sum of all individual leg contributions, e.g. $E_0 = (10 + 20 + 40 + \ldots.\ 5120)mv = 10.230v$. The advantage of this type of ladder network is that the impedance seen by the amplifier is constant (equal to R) and the accuracy is not dependent on the absolute value of R but on their differences.

The DAC is, of course, an important element in an ADC as mentioned in Chapter 2 since it is used to close the feedback loop.

4.1 Specifications:

The GRI line of D to A converters cover a wide range of capabilities. All are mounted on the small device operator cards that plug into the rear section of the computer.

Electrical:

Output:

Analog Output Voltage Ranges	0V to +10V full scale
	$\pm$5V full scale
Output Impedance	0.1 ohms

Performance:

Absolute Accuracy	±0.025 of FS
Linearity	±1/2LSB (8,10 bits)
	±1 LSB (12 bits)
Resolution	1 part in 256 (8 bits)
	1 part in 1024 (10 bits)
	1 part in 4096 (12 bits)
Coding	Binary (0V to +10V) (Bit 15=MSB
	2's complement (±5V)
	(Bit 15 = SIGN)
	(Bit 14 = MSB)
Temperature coefficient	±30 PPM/°C
Output Current	±5ma (typical)
Output Slewing Rate	10V/usec
Settling Time	5usec to ±0.05% of FS
Input Power	±A - 30ma
	+5V - 370ma

Environmental:

Operating Temperature Range	0°C to 50°C
Storage	-55°C to +85°C
Relative Humidity	95% non-condensing

4.2 Device Operator:

The device operator consists of a GP,16 bit register connected as both a source and destination of data. The system address may be chosen via a set of staples according to the instructions in Appendix B. The suggested mnemonic for the operator is DAC, and the device is normally set for a system address of 61 for factory test purposes. Data is transferred to or from the DAC by any register or memory reference instruction, e.g:

FAST	MACHINE CODE
AX TO DAC	11 0000 61
D 100 TO DAC	06 0001 61
	000100
DAC P1	61 0100 61
C DAC P1	61 0110 61
IF DAC ETZ GO TO 100	61 0100 03
	000100

There are no flags or functions associated with the DAC, but the programmer must bear in mind the settling time specifications of the unit, i.e. the DAC will produce an output change for a change in data sent to the DAC, but it will not settle at its steady state value faster than 5 usec. (see Section 4.3).

The DAC may be had with a 0 to +10V or a ±5V range. This may be changed by the user by simply clipping and inserting one staple (see logic print 17-047-017).

4.3 Programming:

Programming the DAC amounts to simply transmitting binary fractions to it from memory or other sources such as registers. The user must bear in mind that the DAC has a 5 usec settling spec. This means that a step change in value will not be accurate to within ±0.05% of the FS value until 5 usec of settling time has been allowed. When using the DAC to generate periodic functions, this may or may not be of consequence, depending on the faithfulness desired in generating the function. For steady state usage, however, a delay of at least 5 usec (approximately 3 cycles) should be introduced prior to changing the value. This permits settling of the DAC output.

The full scale bit values for the various size DAC's available are as follows:

Accuracy

	FS \ $\frac{1}{2^n-1}$ FS	8	10	12
*Range	+10V	39.22mv	9.78mv	2.442mv
	±5V	39.37mv	9.785mv	2.443mv

*The DAC's, unlike the ADC's, are calibrated only for a 10V or ±5V full scale value.

When using the 0 to +10V range, the user must remember that the machine word is left justified and Bit 15 is the MSB of the data word. Thus, signed data should be left shifted as it is sent to the DAC. The user may send signed data to the DAC and assume that the zero offset is half scale (i.e. 5 volts). This will result in a set of readings that range from $-V_{FS}$ = 0V through 0 = +5V and $+V_{FS}$= +10V.

The bipolar DAC accepts 2's complement numbers with Bit 15 = sign bit. The binary point in the unipolar case is assumed to be to the left of Bit 15 and in the bipolar case, to the right of Bit 15. Thus, to generate a voltage that represents a physical constant, simply convert that constant to a percentage of the full scale value and transmit it to the DAC, e.g. a table of values for pressure calculations is based on a full scale value of 100 psi. A DAC is to be used to drive the Y axis of a scope display. Each value is converted to a fraction of full scale P.F.S. = $V_i/100$, and sent to the DAC. The resulting display will be proportional to the original values with the full scale deflection representing the full scale value of the pressure.

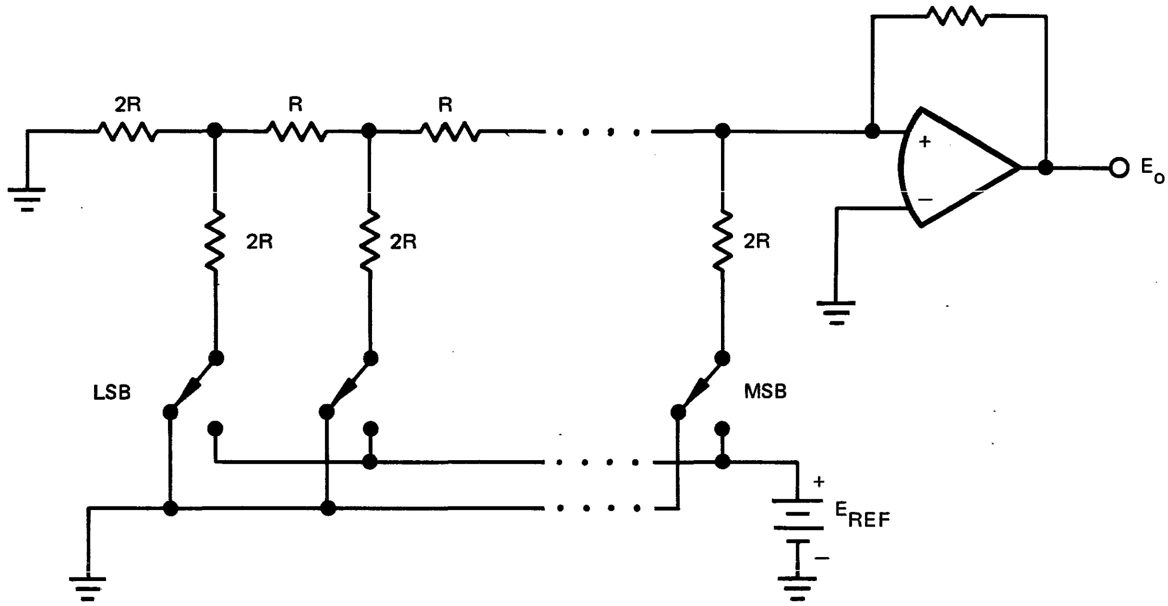


Figure 4-1. Binary Ladder DAC

CHAPTER V

SAMPLE AND HOLD UNIT

5.0 A sample and hold device is essentially an analog memory. Very crudely, it is a capacitor and a single pole double throw switch as shown in Figure 5-1. When sampling the input voltage Vi, the switch connects the voltage source to the capacitor which allows it to charge up to a value approaching Vi. This, of course, is a function of the time constant formed from the source impedance R_s and the sample and hold capacitor C_H. If the switch is in the sample position sufficiently long the capacitor will charge to within the digitizing accuracy of the system. The switch may then be thrown to the hold position which connects the capacitor to the ADC for digitizing. The hold capacitor C_H will discharge through the input impedance R_i of the ADC, but if this is sufficiently high compared to the source impedance R_s it will take a much longer time to lose the charge in the hold position than it took to build the charge in the sample position. During this time, the converter will be, for all practical purposes, digitizing a DC voltage.

In practice, SHU's are used to decrease the aperture time of the ADC (see Section 2.0). The charging of the sample capacitor must, of course, be rapid in order to achieve better aperture time, and the discharge rate in the hold mode should be many orders of magniture greater than the sample or charging time. This is accomplished through the use of an operational amplifier in the practical SHU. Figure 5-2 is a block diagram of the GRI sample and hold unit.

5.1 Specifications:

The GRI 99 Sample and Hold Unit (SHU) is mounted on a small device operator card that plugs directly into the rear section of the computer.

Electrical:

Analog Input Voltage Ranges	0V to +10V FS 0V to +5V FS -5V to +5V FS -10V to +10V FS
Input Overvoltage	±15V (Max) with a recovery time of 3us
Input Impedance	>100 megohms
Input Source Current	2namps typical 7namps maximum
Analog Output Voltage Ranges	0V to +10V 0V to -5V -5V to +5V -10V to +10V
Output Current	±5 MA

Performance:

Bandwidth	DC to 200 KHz (max.) full power @ 3db point
Acquisition Time	5 us (Max) to ±0.025% FS of input signal
Aperture Time	time uncertainty of 50 ns(max)
Hold Decay Rate	1 MV in 1 MS
Output Slewing Rage	30V/us
Gain	+1.00
Accuracy (25°c)	±0.025% FS
Linearity	∓0.01%
Temperature Coefficient	∓20 ppm/°C
Long Term Stability	±0.01%/6 months
Input Power	∓A 35 ma ∓5 115 ma

Environmental:

Operating Temperature Range	0°C to 50°C
Storage	-55°C to + 85°C
Relative Humidity	95% non-condensing

5.2 Device Operator:

The device operator is connected to respond to function output commands only. It's system address is generally the same as the multiplexer operator and is chosen via a set of staples according to the instructions in Appendix B. The suggested mnemonic for the operator is MUX with the FO command bits being represented by SAMP and HOLD respectively. To initiate a sample, the command is:

% RASX	MACHINE CODE
FO SAMP,MUX	02 0010 64

To terminate a sample, the command is

FO HOLD, MUX	02 0001 64

5.3 Programming:

The specified acquisition time is 5 us to 0.025% of FS. Since this time is reasonably short compared to instruction timing, it is suggested that the user insert NOP's between the sample and hold commands to fill in the acquisition time. Thus the sequence

```
FO    SAMP,MUX
NOP
NOP
FO    HOLD, MUX
```

will result in 3 cycles between the sample and hold actions, or 5.28 us. This will produce a holding accuracy comparable to the resolution of a 12 bit ADC. The acquisition time, of course, includes output settling time.

The aperture of the SHU will affect the frequency response of the unit at various accuracy levels. The aperture is defined as the uncertainty in switching from the sample to the hold mode. When in the sample mode, the unit is tracking the input voltage. When placed in the hold mode, the switching uncertainty (or aperture time) is 50 ns. Fig. 5-3 is a graph of the accuracy that can be expected of the SHU for various frequency input signals.

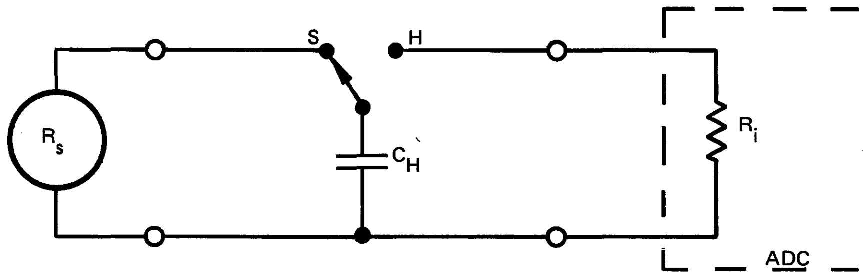


Figure 5-1. Simple Sample and Hold Unit

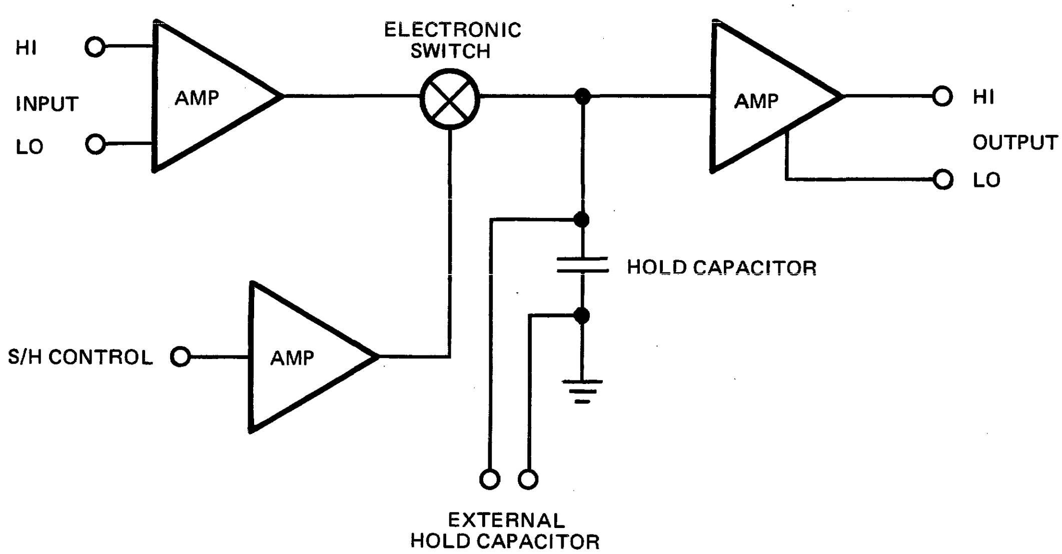


Figure 5-2. GRI Sample and Hold Unit

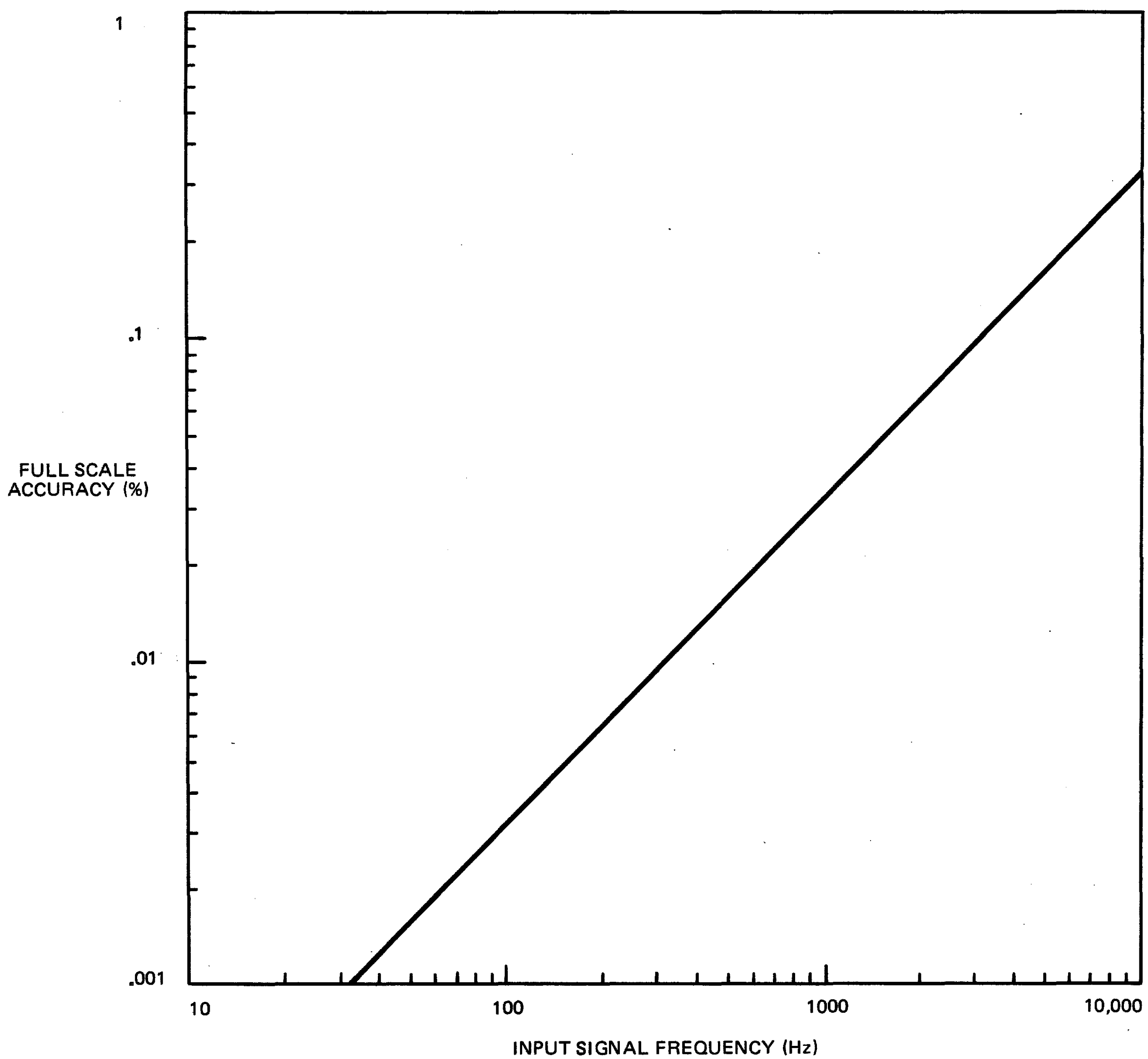


Figure 5-3. Error Due to Aperture as a Function of Input Signal Frequency

APPENDIX A

INSTALLATION

A to D Converters:

The ADC operator uses the interrupt system and therefore requires PIN-POUT jumpers (S40-215) to be inserted in positions SE-S5 and SF-S6 in all vacant slots between the lefthand side of the machine, as viewed from the rear, and the ADC board.

If there are other device operators which require use of $\pm$A voltages, their total current requirement must not exceed 100ma for +A and 100ma for -A. If the current capability has been exceeded by addition of the ADC, a supplementary supply will have to be added to the machine. The supplementary supply is installed in the last slot on the right of the I/O bus in the rear of the processor. The orange and purple quick disconnects that supply $\pm$A to the bottom righthand side of the I/O bus must be disconnected and taped. They may then be taped or tied out of the way.

The analog signal is brought into the ADC via a coaxial connector at the bottom rear edge of the device operator card. The plug for this connector is available from Sealectro (#50-024-0000). It is for use with a subminiature coax, type RG188 or RG174.

A bipolar ADC is merely an offset version of a unipolar ADC. Thus a $\pm$5 volt ADC is still a 10 volt FS unit but a bias of -5 volts has been introduced into the operational amplifier on the front end of the ADC so that the Ø reading of the ADC corresponds to a -5 volt unput, the half scale reading (+5 volts) corresponds to a Ø volt input, and the full scale reading (+10 volts) corresponds to a +5 volt input.

There are two pot adjustments on the ADC board, one for Ø offset and one for full scale (gain). Note that Ø offset applies to the true ADC Ø reading which is not the same as the Ø volt input on a bipolar unit. Similarly, the full scale or gain adjustment applies to the positive most reading on the ADC. Note also that the bipolar ADC's present 2's complement results which mean there will be one missing value on the positive full scale end. Thus a 12 bit bipolar ADC (± 5VFS) presents

100000000000 = -5.1200v and

011111111111 = +5.1175v

Note that the first reading is not useable in the standard arithmetic packages as a legitimate binary number.

The following table gives the adjustment values for the various size ADC's in the family.

ADC	F.S.	Adjust Offset at	Adjust Gain at
8	+5v	Øv	+5.10v
8	±5v	-5.12v	+5.08v
8	+10v	Øv	10.20v
8	±10v	-10.24v	+10.16v
10	+5v	Øv	+5.115v
10	±5v	-5.12v	+5.11v
10	+10v	Øv	+10.23v
10	±10v	-10.24v	+10.22v
12	±5	-5.1200v	+5.1175v
12	+10	Øv	+10.2375v
12	±10	-10.240v	+10.235v

Key the following loop into memory:

	loc	
FO STRT CLIF,ADC	100	02 1001 65
SF ADC, IRDY	101	65 1000 02
JU .-1	102	00 0100 03
	103	101
RR ADC,27	104	65 0000 27
JU .-5	105	00 0100 03
	106	100

Dial Device Select switches to 27, start the loop, and apply the rated negative most voltage to the analog input line from a precision source. This should be done out at the transducer that will supply the voltage to be digitized. Adjust the offset pot until zero readings (unipolar units) of the largest negative number (bipolar units) are displayed on the console display register (Device Select Switches = 27_8). Adjustment of offset will interact with the gain adjustment which affects the positive full scale reading. Using a precision source (or the transducer itself) produce a full scale, known positive voltage (i.e. +5.1175v for a 12 bit, bipolar ADC) at the cable end which feeds the ADC input. Adjust gain for the proper positive full scale reading displayed on the display register. After adjusting the gain, the offset should be rechecked and adjusted if necessary. Alternately adjusting offset and gain will eventually result in the proper digital readings (usually within two iterations).

On bipolar units the Øv input reading (which is really the half scale point on the ADC) should be checked. This may be done by shorting the input. After gain and offset adjustments have been made the center point should fall right in place if the ADC were perfectly linear. If the center or Ø input of the bipolar ADC does not produce a Ø reading and this is desired, the user can shift both the gain and offset adjustments by a half a bit or so in order to obtain a Ø ADC reading at half scale. At any rate the ADC readings should be within half a bit at half scale. Half bit adjustments are obtained by setting the input reference value halfway between two increments of readings. Thus to move half a bit away from the negative full scale value on a 12 bit bipolar ADC, set the reference input at -5.11625 (1.25mv greater than -5.1175v) and adjust for a -FS ADC reading at that point. See A-5 for a graphical explanation of offset and gain adjustments. After adjustments have been made, a histogram test of known voltages applied to the ADC should be run to assure proper adjustment.

Multiplexers:

The MUX operator should be located in the first slot to the left of the ADC operator. Note that ±A voltages are required by the MUX. Prior to installation, check the loading of ±A to determine whether or not an auxiliary supply is required. A short coaxial jumper is supplied with the MUX to couple the analog signal to the ADC. This cable also uses a Sealectro subminiature coax connector #50-024-0000. The 32 analog signal connections are made via the PC edge connection at the rear of the card using the 48 pin I/O connector with cable clamp (S40-216 with S40-204 contacts), supplied with the MUX option. The grounding of the signals brought to this connector becomes extremely important as the resolution of the ADC increases. At 2.5mv per bit, it does not take much common mode to normal mode conversion to introduce a 2.5mv error on a particular channel. Figures A-1, A-2 are connection charts which show a common or return connection for each signal pair. Thus, the ground connection for channels 0 and 3 is pin L. The common signal connections are connected to analog ground which is also the processor's logic ground and eventually becomes the frame ground back at the power supply. Since all of the analog device operators are single ended systems, differential voltages may be handled as shown in Figure A-3.

In noisy environments, the signals should be handled over twisted shielded pair or subminiature coax, particularly as the resolution of the converter increases. As common mode currents in the ground system increase, there will be a point at which extreme ground provisions must be taken. Figure A-4 shows a simplified version of the mode problem arising in single ended front ends. The analog equipment and the computer are tied to building ground at two different points. Between them, there is a large current called I_{cm} which consists of the ground currents of every piece of equipment in the building that is tied to building ground. There is a finite ground grid resistance, R_{gg}, between the two ground points; and they will therefore be at different potentials. If we assume the computer ground is the 0 reference, the analog equipment ground is at a slightly higher potential V_{cm}. Ignoring the impedance of the signal source E_s, both the ground line and the signal line are at this common mode potential V_{cm}.

The potential V_{cm} is:

$$V_{cm} = I_{cm} R_{gg}$$

The common mode current in the ground return of the signal is

$$I_{cmsg} = V_{cm}/R_{sg}$$

The common mode current in the signal line is:

$$I_{cms} = V_{cm}/(R_s + R_{in})$$

where R_{in} is the input impedance to ground of the A to D. R_{in} is very large (10M) and effectively swamps out R_s, therefore:

$$I_{cms} \cong V_{cm}/R_{in}$$

A common mode voltage V will appear across R_{in} which will be measured by the ADC along with the signal E_s. This voltage is:

$$\begin{aligned} V &\cong I_{cms} R_{in} \\ &= R_{in} (V_{cm}/R_{in}) \\ &= V_{cm} \end{aligned}$$

This, of course, is an over-simplified presentation of what happens, but it does vividly demonstrate that common mode voltage can appear directly across the input to an A to D. Looking at some numbers for a moment:

If the distances over the ground grid are large, a typical number for R_{gg} might be 0.01 ohms. In a medium size plant with lots of motors and equipment all tied to building ground, we might find 100 amperes of ground current in which case:

$$V_{cm} = I_{cm} R_{gg} = .01 \text{ X } 100 = 1 \text{ volt} = V$$

This voltage which is now measured by the ADC could be handled as a fixed offset by subtracting it from the actual ADC reading, which now represents:

$$V_{adc} = E_s + V_{cm}$$

$$\text{Actual } V_{meas} = V_{adc} - V_{cm}$$

However, the I_{cm} is not a constant; it varies severely as motors and equipment are started up and shut down. Treating V_{cm} as a fixed offset is, therefore, impractical. The only solutions with the single ended system are:

a) disconnect the analog equipment from building ground (float it)

b) short circuit the common mode voltage with a ground connection between the equipment grounds whose resistance is <u>very</u> low compared to the resistance of the signal lines.

Solution a) is not always feasible because of plant safety practices. It is, however, a good solution where permissible. Solution b) would be extremely costly, for it could conceivably involve a large amount of copper.

As these common mode currents become excessive, the grounding system will become extremely expensive, and the best solution becomes differential amplifiers for each signal. As the number of signals increases, it becomes economical to consider a more sophisticated, outboard differential multiplexer and ADC system, which may be interfaced to the GRI-909 series through the Gate Input and General Output Register cards.

The offset and gain adjustments of the ADC should be checked through the multiplexer. The loop previously given for this may be modified by adding the instruction:

	loc	
RR, SWR,MUX	77	10 0000 64

and changing the last instruction to

	loc	
JU 77	105	00 0100 03
	106	77

This will allow selection of different channels when performing the gain and offset adjustments.

D to A Converters:

The DAC operator does not use the interrupt system, and therefore its installation requires no attention to PIN-POUT, DIN-DOUT jumpers.

If there are other device operators which require the use of $\pm$A voltages, their total current requirements must not exceed 100ma for +A and 100ma for -A. If the current capability has been exceeded by addition of the DAC(s), a supplementary supply will be required.

The analog output is brought out of the DAC via a coaxial connector at the bottom rear edge of the device operator card. The plug for this connector is available from Sealectro (#50-029-0000) and is to be used with subminiature coax, type RG188 or RG174.

There is one pot adjustment on the DAC for zero offset. This is set at the factory but may have to be re-adjusted by the user as the DAC is used over a long period of time.

The offset adjustment affects the 0 value of the DAC and may be adjusted as follows:

1. Transmit 0's to the DAC via the console
2. With a voltmeter whose resolution is at least as good as the DAC being adjusted (i.e. 40mv, 10mv, or 2.5mv), adjust the pot for a zero reading on the meter.

Sample and Hold Unit:

The SHU does not use the interrupt system, and therefore its installation requires no attention to PIN-POUT,DIN-DOUT jumpers.

If there are other device operators which require the use of the $\pm$A voltage, their total current requirement must not exceed 100 ma for +A and 100ma for -A. If the current capability is exceeded by addition of an SHU, a supplementary supply is required.

The SHU should physically be located between the MUX and ADC Cards in the system. The analog input and output on the SHU are brought out to two coaxial connectors at the bottom rear edge of the device operator card. The plug for this connector is available from Sealectro (#50-029-000) and is to be used with subminiature coax, type RG188 or RG174.

The upper most connector is the input to the SHU and the lower most connector is the SHU output. The SHU input is generally connected to the MUX output (or signal source) and the SHU output is generally connected to the input of the ADC operator.

There is a pot adjustment built into the sample and hold module on the board and is the dumped charge adjustment. This is preset at the factory and is adjusted for a hold offset at Vin=Ø volts (i.e. a grounded analog input).

The leakage rate in the hold mode may be decreased by the addition of an external capacitor. This, however, increases the acquisition time. The leakage rate for an external capacitance is:

$$LR = \frac{1}{1+\frac{1000}{C_e}} \quad \text{mv per ms}$$

The acquisition time for an external capacitance is:

$$AT = 5+\frac{C_e}{200} \quad \text{us}$$

where C_e = external hold capicitance in pf. Thus for a 1000 pf external hold capacitor, the leakage rate is 0.5 mv per ms and the acquisition time is 10 us.

ANALOG MULTIPLEXER
CONNECTIONS

CHANNEL #	OCTAL ADDR	INPUT PINS SIGNAL	INPUT PINS COMMON
Ø	Ø	14	16
1	1	R	T
2	2	15	16
3	3	S	T
4	4	23	25
5	5	a	c
6	6	24	25
7	7	b	c
8	10	21	22
9	11	20	22
10	12	y	z
11	13	x	z
12	14	v	w
13	15	18	19
14	16	u	w
15	17	17	19
16	20	K	L
17	21	9	10
18	22	8	10
19	23	J	L
20	24	F	H
21	25	D	H
22	26	6	7
23	27	4	7
24	30	B	C
25	31	A	C
26	32	2	3
27	33	1	3
28	34	M	P
29	35	11	13
30	36	12	13
31	37	N	P

Figure A-1

MUX CONNECTOR (rear view)

ETCH SIDE			COMPONENT SIDE
Ch 25	A	1	Ch 27
Ch 24	B	2	Ch 26
COMMON	C	3	COMMON
Ch 21	D	4	Ch 23
KEY	KEY		KEY
Ch 20	F	6	Ch 22
COMMON	H	7	COMMON
Ch 9	J	8	Ch 8
Ch 6	K	9	Ch 7
COMMON	L	10	COMMON
Ch 28	M	11	Ch 29
Ch 31	N	12	Ch 30
COMMON	P	13	COMMON
Ch 1	R	14	Ch 0
Ch 3	S	15	Ch 2
COMMON	T	16	COMMON
Ch 14	U	17	Ch 15
Ch 12	V	18	Ch 13
COMMON	W	19	COMMON
Ch 11	X	20	Ch 9
Ch 10	Y	21	Ch 8
COMMON	Z	22	COMMON
Ch 5	a	23	Ch 4
Ch 7	b	24	Ch 6
COMMON	c	25	COMMON

Figure A-2

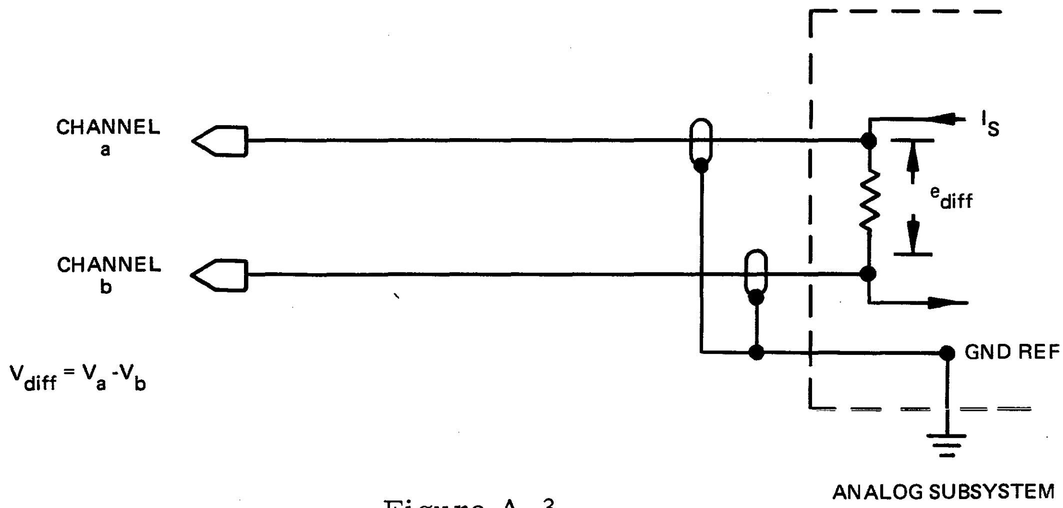


Figure A-3

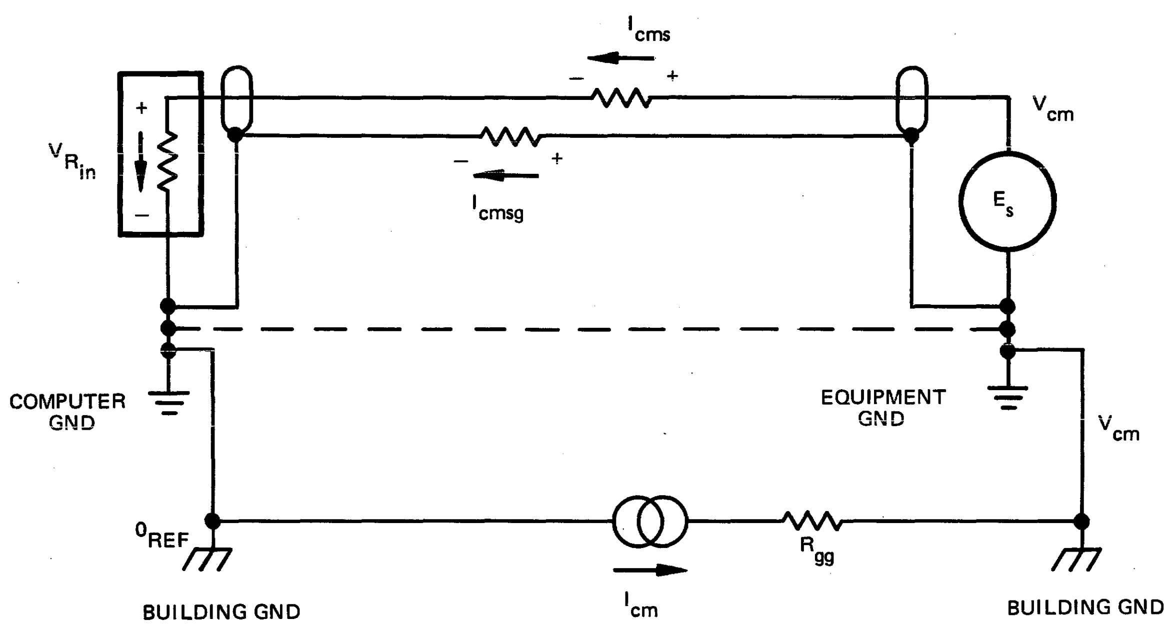


Figure A-4

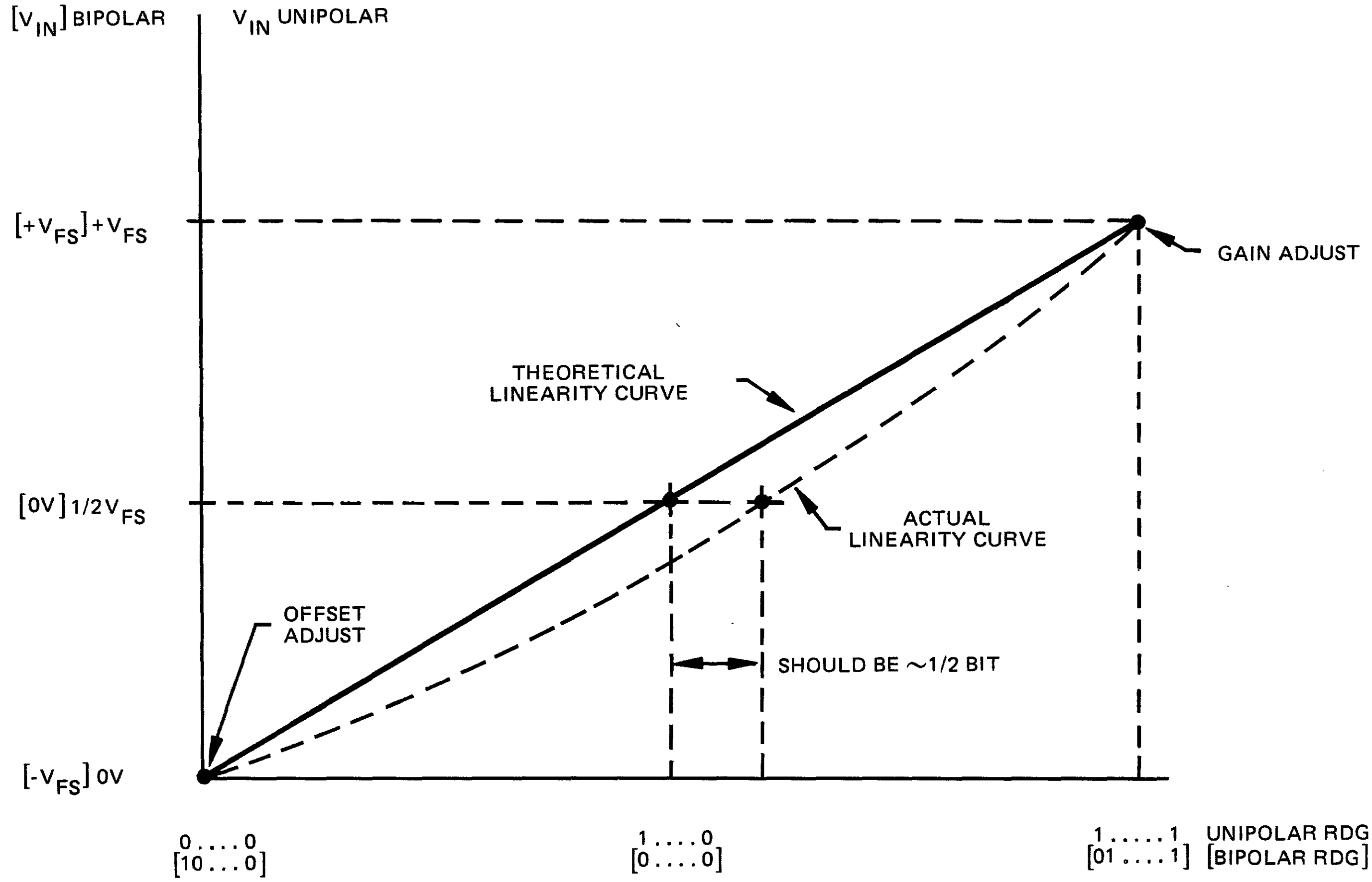

[VIN] BIPOLAR
VIN UNIPOLAR
[+VFS]+VFS
[0V] 1/2VFS
[-VFS] 0V
GAIN ADJUST
THEORETICAL LINEARITY CURVE
ACTUAL LINEARITY CURVE
OFFSET ADJUST
SHOULD BE ~1/2 BIT
0 0
[10 . . . 0]
1 0
[0 . . . . 0]
1 1
[01 . . . . 1]
UNIPOLAR RDG
[BIPOLAR RDG]

Figure A-5

APPENDIX B

DEVICE ADDRESS AND INTERRUPT SELECTION

Device Address Selection:

The device address selection consists of a dual row of staples marked "1" and "0" surrounding decoders (7430) in positions A1 (DAB decode) and L1 (SAB decode). To set an address in a board, insert staples in row "1" for those SAB or DAB bits which are to be decoded as 1's. Insert staples in row "0" for those SAB or DAB bits which are to be decoded as 0's. The example shown on Page B-6 is for an address of 65_8.

Device Interrupt Control:

Some devices provide for a choice of interrupt status bit and interrupt address generation. Where the interrupt status bit is to be chosen, the same SB and DB bits must be chosen. Interrupt address generation provides for up to four 1's to be generated on any of the 16 DB lines. For example, assume that the desired interrupt address for a device is 45_8, 468, 47_8. Only the first address of the group need be generated, and this will be the address that the SC is stored in when the interrupt occurs. The generated address plus 1 (46_8) will be the location in which program operation resumes after the interrupt. To generate 45_8, we need three 1's generated, e.g:

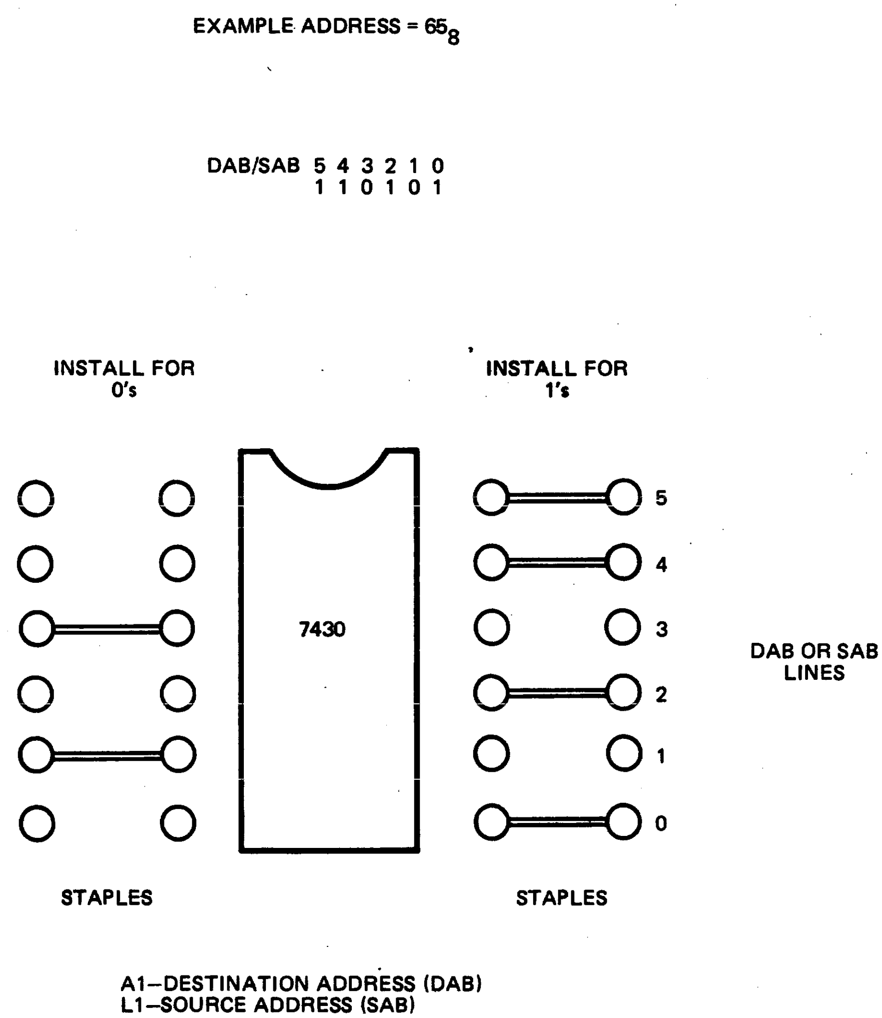
$$45_8 = 100101_2$$

DB bits 0, 2, 5 must be connected to the address generator gates. Note that one of the four gates is not required and is, therefore, left open.

The wiring of interrupt functions is described with each device manual in a tabular form.

NOTE: All device operators are set for a specific device address and interrupt controls at the factory in order to facilitate testing of the boards. The user may alter these addresses if he desires by following the instructions in the device manual. In systems where multiples of the same operator are used, the user must, of course, change the addresses and interrupt controls.

The interrupt controls, however, need not all be different. The same status bit, for example, is often assigned to a group of like devices. For example, 5 general output registers are put into a system. They may all be assigned to the same status bit, but each one will generate a unique interrupt address. When all boards are on the same status bit level, there is a hardware priority imposed by the order in which the boards are plugged into the rear of the GRI-909. This priority is determined by the PINL-POUTL chain and runs from left to right (highest to lowest) looking at the rear of the machine.



Variable Address Selection

INTERRUPT STATUS BIT CONNECTION TABLE

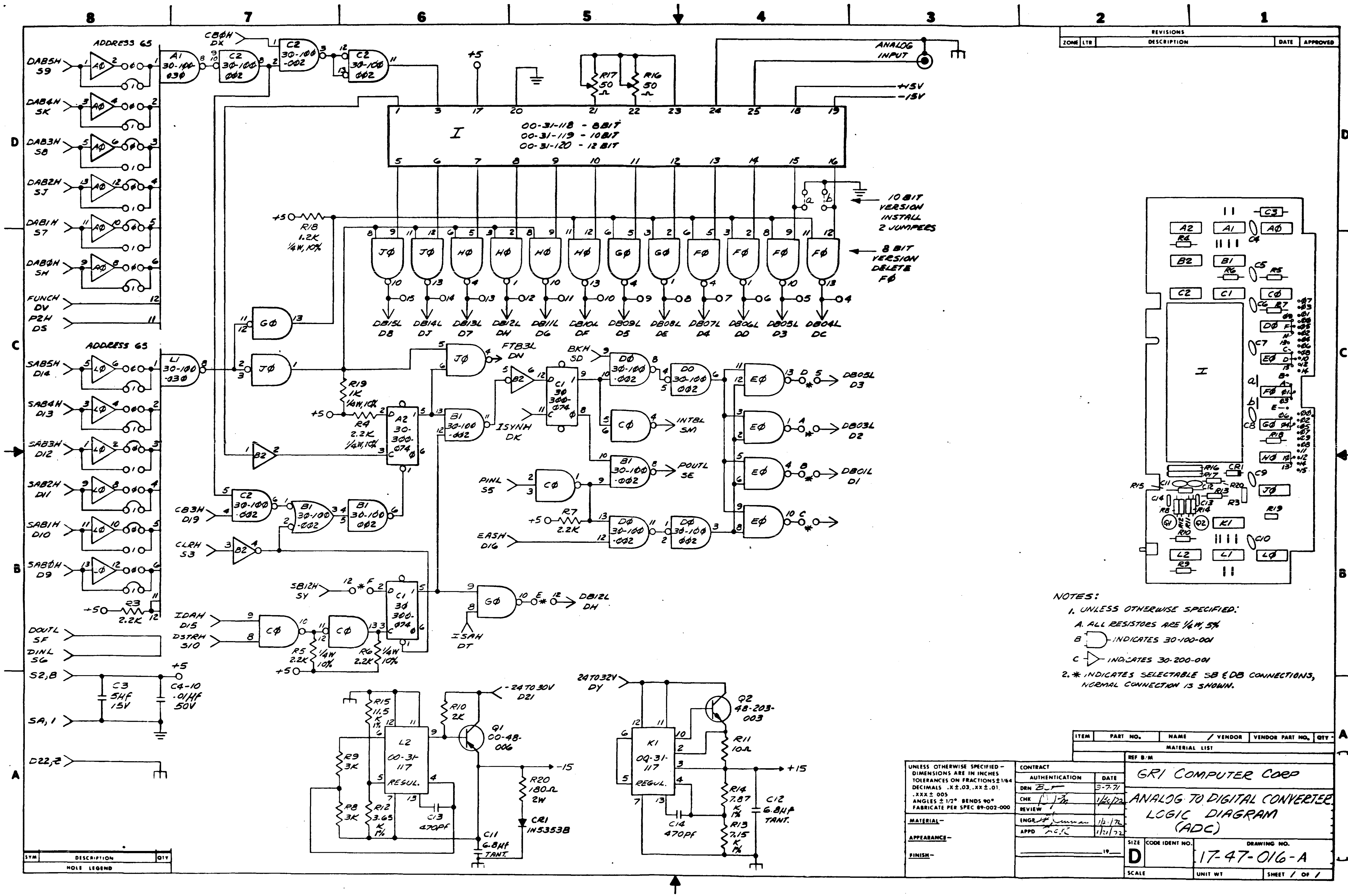
ADC

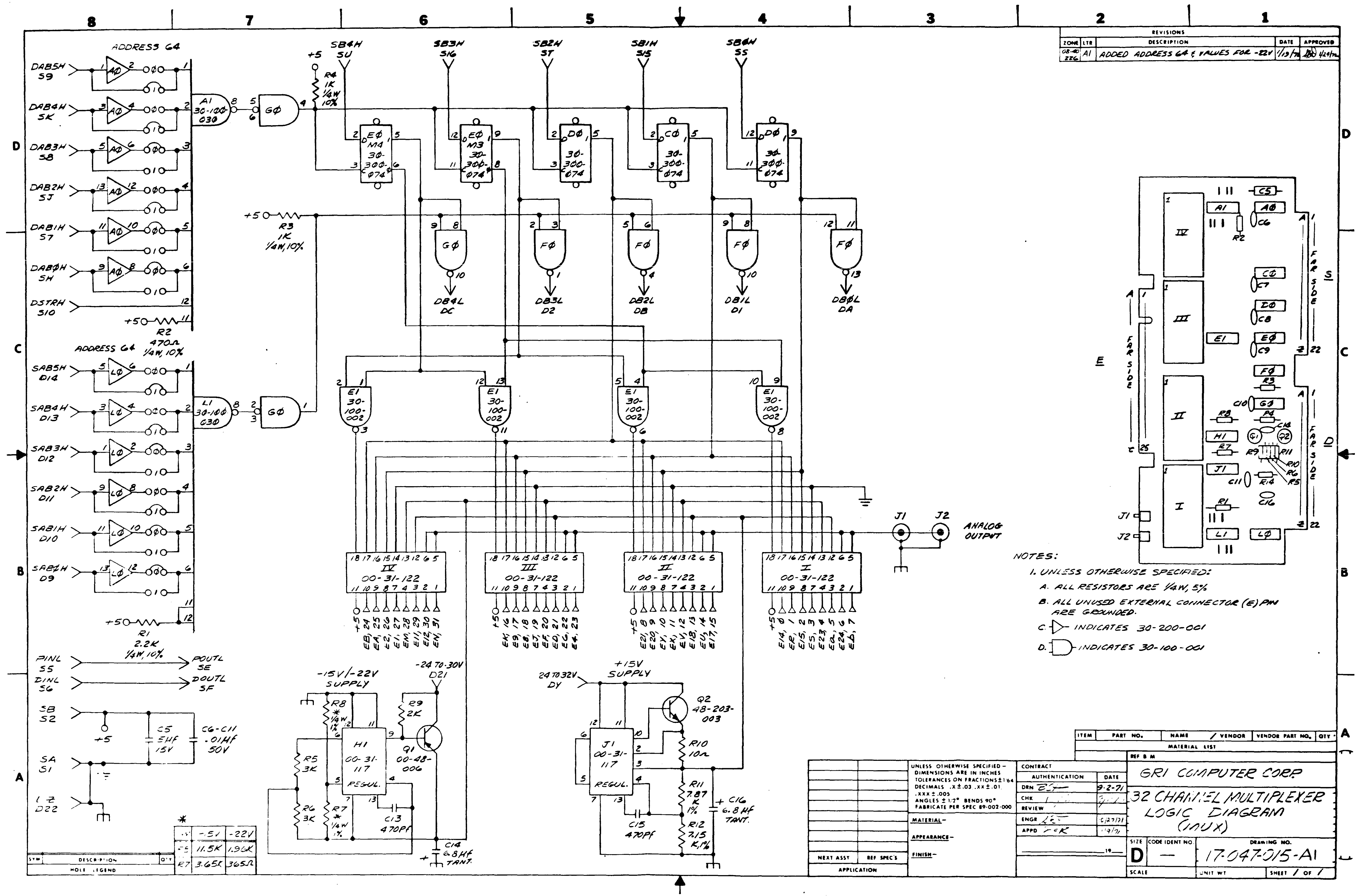
SB DATA INPUT	TO	ONE SB DATA LINE
pad F	to pad on connector finger SS	SBØØ
	S15	SB Ø1
	ST	SB Ø2
	S16	SB Ø3
	SU	SB Ø4
	S17	SB Ø5
	SV	SB Ø6
	S18	SB Ø7
	SW	SB Ø8
	S19	SB Ø9
	SX	SB 1Ø
	S20	SB 11
	SY	SB 12
	S21	SB 13
	SZ	SB 14
	S22	SB 15

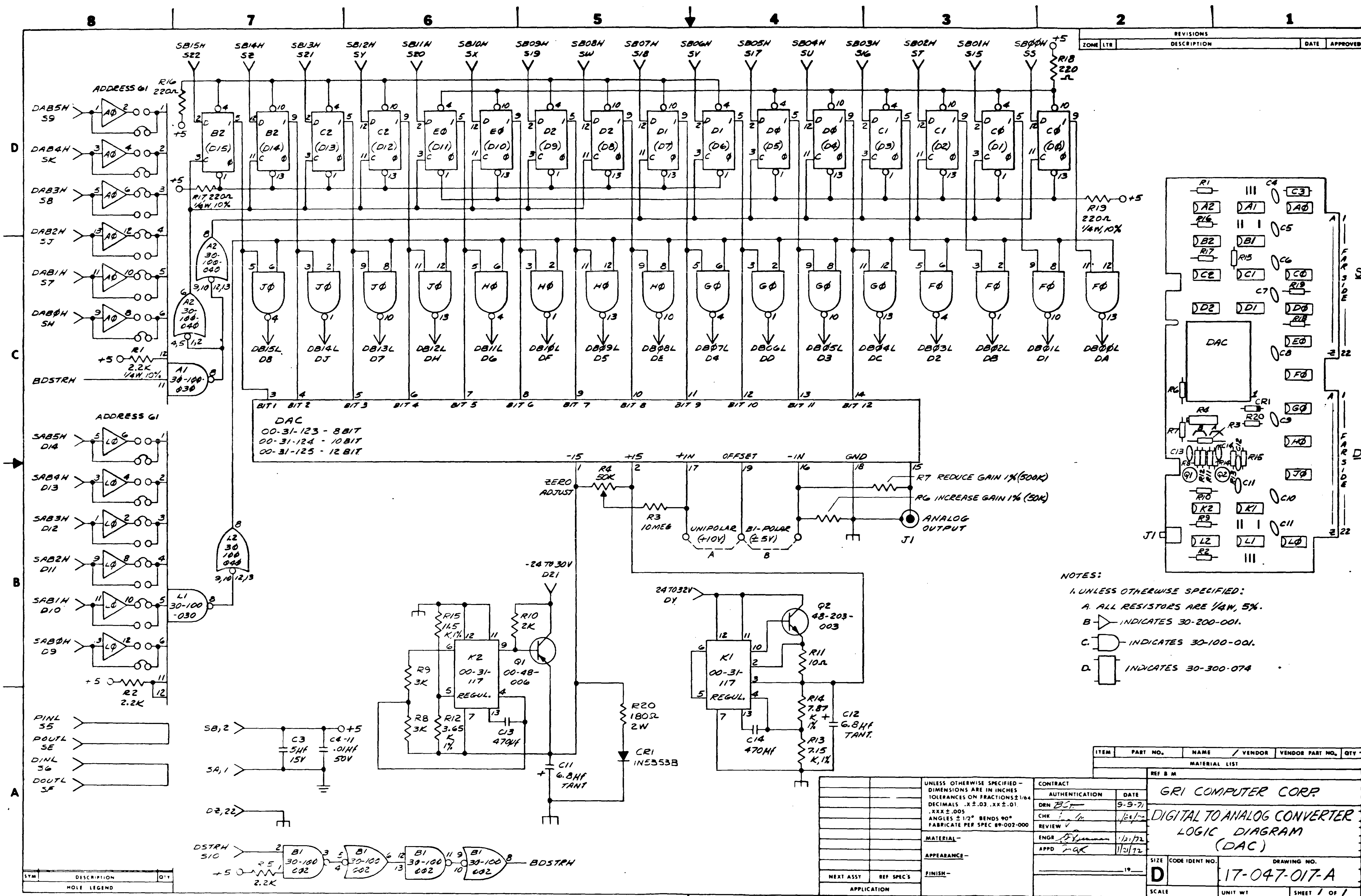
INTERRUPT STATUS BIT CONNECTION TABLE (cont.)

DB DATA OUTPUT	ADC TO	ONE DB DATA LINE pad on connector finger	
pad Ê		DA	DB ØØ
		D1	DB Ø1
		DB	DB Ø2
		D2	DB Ø3
		DC	DB Ø4
		D3	DB Ø5
		DD	DB Ø6
		D4	DB Ø7
		DE	DB Ø8
		D5	DB Ø9
		DF	DB 10
		D6	DB 11
		DH	DB 12
		D7	DB 13
		DJ	DB 14
		D8	DB 15

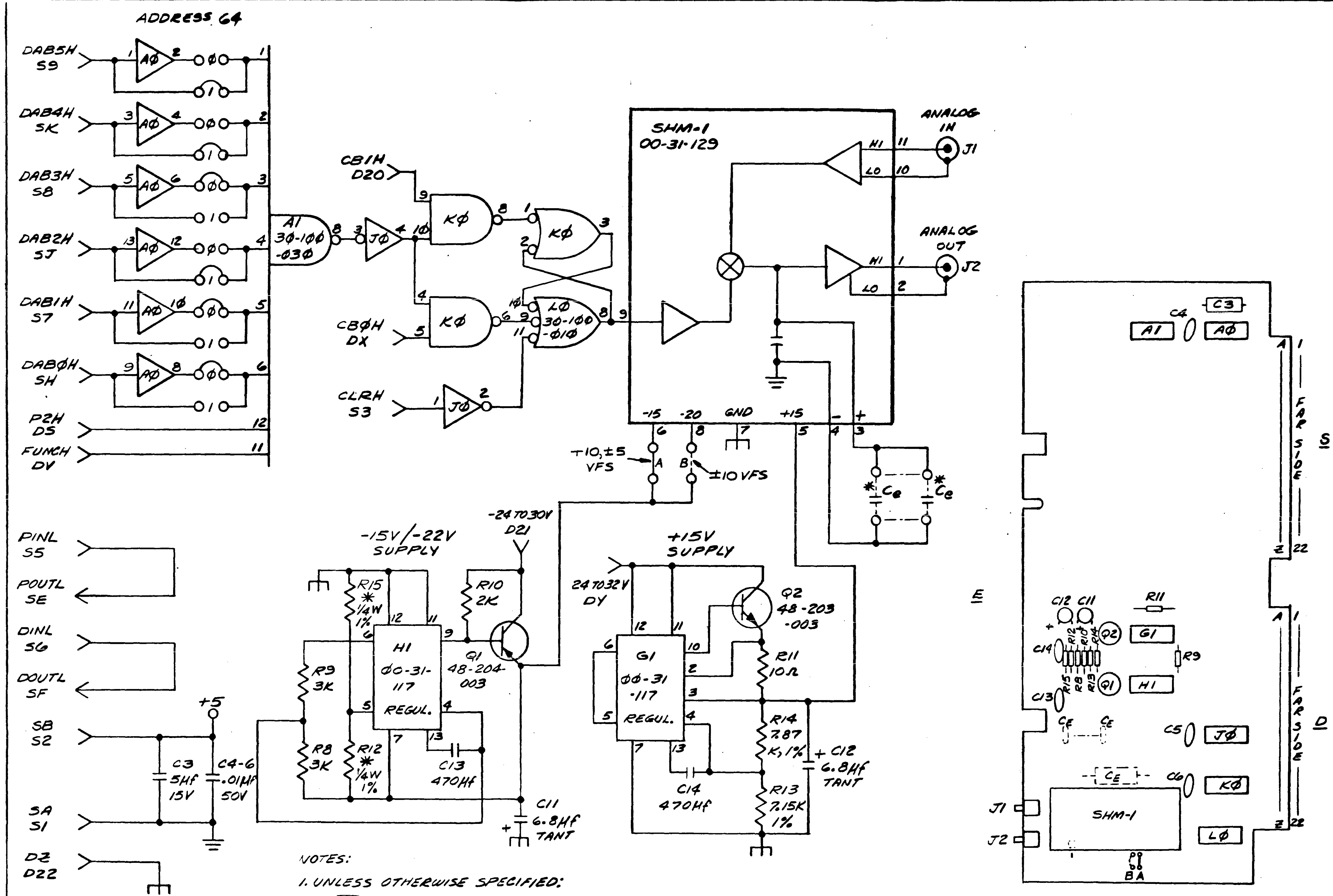
ADDRESS GENERATOR OUTPUTS	TO	UP TO FOUR DB DATA LINES
pad A		(See Above)
B		
C		
D		


ADDRESS 65
DAB5H S9
DAB4H SK
DAB3H S8
DAB2H SJ
DAB1H S7
DAB0H SH
FUNCH DV
P2H DS
SAB5H D14
SAB4H D13
SAB3H D12
SAB2H D11
SAB1H D10
SAB0H D9
DOUTL SF
DINL S6
S2,B
SA,1
D22,2
C3 5µF 15V
C4-10 .01µF 50V
CB0H DX
CB3H D19
CLRH S3
SB12H SY
IDAH D15
DSTRH S10
ANALOG INPUT
+15V
-15V
R17 50Ω
R16 50Ω
00-31-118 - 8 BIT
00-31-119 - 10 BIT
00-31-120 - 12 BIT
R18 1.2K 1/4W, 10%
10 BIT VERSION INSTALL 2 JUMPERS
8 BIT VERSION DELETE F0
DB15L D8
DB14L DJ
DB13L D7
DB12L DH
DB11L D6
DB10L DF
DB09L D5
DB08L DE
DB07L D4
DB06L DD
DB05L D3
DB04L DC
FTB3L DN
BKH SD
INTBL SM
POUTL SE
PINL S5
EASH D16
ISYNH DK
ISAH DT
DB05L D3
DB03L D2
DB01L D1
DB12L DH
R19 1K 1/4W, 10%
R4 2.2K 1/4W, 10%
R7 2.2K
R5 2.2K 1/4W 10%
R6 2.2K 1/4W 10%
R3 2.2K
-24 TO 30V D21
24 TO 32V DY
R15 11.5 K 1%
R9 3K
R8 3K
R12 3.65 K 1%
L2 00-31-117 REGUL.
C13 470pF
R10 2K
Q1 00-48-006
R20 180Ω 2W
CR1 1N5353B
C11 6.8µf TANT.
-15
K1 00-31-117 REGUL.
C14 470pF
Q2 48-203-003
R11 10Ω
R14 7.87 K 1%
R13 7.15 K 1%
C12 6.8µF TANT.
+15
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 1/4W, 5%
B INDICATES 30-100-001
C INDICATES 30-200-001
2. * INDICATES SELECTABLE SB & DB CONNECTIONS, NORMAL CONNECTION IS SHOWN.
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
ITEM PART NO. NAME / VENDOR VENDOR PART NO. QTY
MATERIAL LIST
UNLESS OTHERWISE SPECIFIED - DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ±1/64 DECIMALS .X±.03, .XX±.01, .XXX±.005 ANGLES ±1/2° BENDS 90° FABRICATE PER SPEC 89-002-000
MATERIAL -
APPEARANCE -
FINISH -
CONTRACT
AUTHENTICATION DATE
DRN 3-7-71
CHK 1/26/72
REVIEW
ENGR 1/21/72
APPD 1/21/72
GRI COMPUTER CORP
ANALOG TO DIGITAL CONVERTER LOGIC DIAGRAM (ADC)
SIZE D
CODE IDENT NO.
DRAWING NO. 17-47-016-A
SCALE
UNIT WT
SHEET 1 OF 1
SYM DESCRIPTION QTY
HOLE LEGEND


REVISIONS
ADDED ADDRESS 64 & VALUES FOR -22V
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 1/4W, 5%
B. ALL UNUSED EXTERNAL CONNECTOR (E) PIN ARE GROUNDED.
C. INDICATES 30-200-001
D. INDICATES 30-100-001
ADDRESS 64
ANALOG OUTPUT
-15V/-22V SUPPLY
+15V SUPPLY
GRI COMPUTER CORP.
32 CHANNEL MULTIPLEXER LOGIC DIAGRAM (MUX)
17-047-015-A1
SHEET 1 OF 1



ADDRESS 61
DAC
00-31-123 - 8 BIT
00-31-124 - 10 BIT
00-31-125 - 12 BIT
ZERO ADJUST
R7 REDUCE GAIN 1% (500K)
R6 INCREASE GAIN 1% (50K)
ANALOG OUTPUT
UNIPOLAR (+10V)
BI-POLAR (±5V)
K2 00-31-117 REGUL.
K1 00-31-117 REGUL.
Q1 00-48-006
Q2 48-203-003
CR1 1N5353B
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 1/4W, 5%.
B. INDICATES 30-200-001.
C. INDICATES 30-100-001.
D. INDICATES 30-300-074
REVISIONS
MATERIAL LIST
HOLE LEGEND
UNLESS OTHERWISE SPECIFIED – DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ±1/64 DECIMALS .X ±.03 .XX ±.01 .XXX ±.005 ANGLES ± 1/2° BENDS 90° FABRICATE PER SPEC 89-002-000
NEXT ASSY
REF SPEC'S
APPLICATION
MATERIAL–
APPEARANCE–
FINISH–
CONTRACT
AUTHENTICATION
DATE
DRN 9-9-71
ENGR 1/21/72
APPD 1/21/72
GRI COMPUTER CORP.
DIGITAL TO ANALOG CONVERTER
LOGIC DIAGRAM
(DAC)
SIZE D
DRAWING NO.
17-047-017-A
SHEET 1 OF 1



NOTES:

1. UNLESS OTHERWISE SPECIFIED:

A — INDICATES 30-100-002

B — INDICATES 30-200-001

2 * Ce - SEE MANUAL FOR VALUE

*

SHM	-15V	-22V
R15	11.5K	1.96K
R12	3.65K	365Ω

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS

X	XX	XXX
±.030	±.015	±.005

ANGLES ±1°

ALL RESISTORS 1/4 W ± 10 %

MATERIAL

REMOVE ALL SHARP EDGES

DRAWN — DATE

CHECKED — DATE

ENG — DATE

APPROVED — DATE

FIRST USED ON

FINISH

GRI COMPUTER CORP

SAMPLE & HOLD LOGIC DIAGRAM (SHU)

DRAWING NO.

SIZE	TYPE	PROD	NUMBER	REV
C	17	47	018	A

SCALE — WEIGHT — SHEET 1 of 1

GRI Computer Corporation
320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164
TEL: (617) 969-0800