GRC DLV11 INTERFACE

SPECIFICATIONS

DEVICE ADDRESSING: DIP SWITCH Z - 7

ADDRESS=LLXYZ0

W	1	X	2	3	4	Y	5	6	7	Z	8	9	10
		0	0	0	0	0	0	0	0	0	0	0	0
		1	0	0	1	1	0	0	1	1	0	0	1
		2	0	1	0	2	0	1	0	2	0	1	0
		3	0	1	1	3	0	1	1	3	0	1	1
		4	1	0	0	4	1	0	0	4	1	0	0
		5	1	0	1	5	1	0	1	5	1	0	1
6	0	6	1	1	0	6	1	1	0	6	1	1	0
7	1	7	1	1	1	7	1	1	1	7	1	1	1

(Column headers: SWITCH 1 | SWITCH # 2 3 4 | SWITCH # 5 6 7 | SWITCH # 8 9 10)

ON= 1

OFF= 0

INTERRUPT VECTOR ADDRESSING: DIP SWITCH 2-10

ADDRESS=000XY0

X	5	4	Y	3	2	1
0	0	0	0	0	0	0
1	0	1	1	0	0	1
2	1	0	2	0	1	0
3	1	1	3	0	1	1
			4	1	0	0
			5	1	0	1
			6	1	1	0
			7	1	1	1

ON= 1
OFF= 0

for LSI 11   — Consol = 177560 Add , 60 vect.
             port #1 = 176500 odd , 300 vect
                #2 = 176510   , 310
                #3 = 176520   , 320

UART OPTIONS: DIP SWITCH 2-27

        ON = 0
        OFF = 1

PARITY: SWITCH #1

        EVEN PARITY = OFF
        ODD PARITY = ON

NUMBER OF STOP BITS: SWITCH #2

        ONE STOP BIT = ON
        TWO STOP BITS = OFF

NUMBER OF DATA BITS: SWITCHES #3 AND 4

# DATA BITS	SWITCH #4	SWITCH #3
8	OFF	OFF
7	OFF	ON
6	ON	OFF
5	ON	ON

PARITY BIT PRESENT: SWITCH #5

        BIT PRESENT = ON
        NO BIT PRESENT = OFF

PROGRAMMABLE BAUD RATE: SWITCHES #6 AND 7

FUNCTION	SWITCH #6	SWITCH #7
NOT USED	OFF	OFF
DISABLE	OFF	ON
ENABLE	ON	OFF
NOT USED	ON	ON

HALT. BREAK: SWITCH #8

        ENABLE = ON
        IGNORE = OFF

        PROCESSOR WILL HALT WHEN BREAK KEY IS PRESSED.

BAUD RATE SELECTION: ROTARY SWITCH 2-29

| | | PROGRAMMABLE XCSR BITS | | | |
SWITCH POS	BAUD RATE	15	14	13	12
0	50	0	0	0	0
1	75	0	0	0	1
2	110	0	0	1	0
3	134.5	0	0	1	1
4	150	0	1	0	0
5	300	0	1	0	1
6	600	0	1	1	0
7	1200	0	1	1	1
8	1800	1	0	0	0
9	2000	1	0	0	1
A	2400	1	0	1	0
B	3600	1	0	1	1
C	4800	1	1	0	0
D	7200	1	1	0	1
E	9600	1	1	1	0
F	19200	1	1	1	1

TO USE PROGRAMMABLE BAUD RATE OPTION: BITS 12-15 OF THE XCSR (ADDRESS=177564) WILL CHANGE THE BAUD RATE OF   THE DLV11 UNDER PROGRAM CONTROL. SETTING BIT 11 IN THE XCSR TRANSFERS BAUD RATE TO PROGRAM CONTROL.   NOTE THAT THE XCSR IS WRITE ONLY. THE BIT WILL BE CLEARED BY A RESET IN- STRUCTION, AND IS CLEARED AT POWER UP.