ELTEC
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EUROCOM-17-5xx

Dual 68040 CPU Board with Graphics

Service Manual

Revision 1 A
for
EUROCOM-17-5xx Hardware Revision 1.A

Rev.	Changes	Date
1 A	valid for Hardware Revision 1.A	31.01.95, T.K.

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This equipment generates and can radiate radio frequencies. If not installed in accordance with the instruction manual, it may cause interference to radio communications. The equipment has not been tested for compliance with the limits for class A computing devices, pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against such interference, but temporary usage is permitted as per regulations. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense is required to take whatever measures may be required to shield the interference.

DISCLAIMER!
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Conventions

If not otherwise specified, addresses are written in hexadecimal notation and identified by a leading dollar sign ("$").

Signal names preceded by a slash ("/"), indicate that this signal is either active low or that this signal becomes active with the trailing edge.

b bit
B byte
K kilo, means the factor 400 in hex (1024 decimal)
M mega, the multiplication with 100 000 in hex (1 048576 decimal)
MHz 1 000 000 Hertz

Board-specific abbreviations:

ASR	Address Substitution Register
AUI	Attachment Unit Interface
BLT	Block Transfer
BTO	Bus Time-out
CAS2	Compare and Swap 2 Instruction
CLUT	Color Look-up Table
CPU	Central Processing Unit
CPU2CON	Secondary CPU Control Register
CSR	Control/Status Register
CTS	Clear to Send
DAC	Digital to Analog Converter
DMA	Direct Memory Access
DTE	Data Terminal Equipment
ESR	Enable Slave Register
FIFO	First In First Out
IACK	Interrupt Acknowledge
ICF	Interprocessor Communication Facility
ICGS	Interprocessor Communication Global Switches
ICMS	Interprocessor Communication Module Switches
ILACC	Integrated Local Area Communications Controller
IOC-2	I/O Controller Asic
LAN	Local Area Network
LEB	Local Extension Bus
LIRQ	Local Interrupt Request
MAU	Medium Attachment Unit
MBAR	Memory Base Address Register

MBLT	Multiplexed Block Transfer
MPC	Multi-Protocol Controller
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RAM	Random Access Memory
RBF	Receive Buffer Full
RMC	Read-Modify-Write Cycle
RTC	Real-time Clock
RTS	Request to Send
SBR	Slave Base Address Register
SCSI	Small Computer Systems Interface
SCR	System Control Register
SILC	Serial Interface Level Converter
SRAM	Static RAM
SMR	Slave Mask Register
TBE	Transmit Buffer Empty
TTL	Transistor Transistor Logic
VIC	VMEbus Interface Chip
VRAM	Video RAM
VTG	Video Timing Generator
UAT	Unaligned Transfer

1 Signal Names

The following is a listing of all signal names on the EUROCOM-17-5xx and an explanation of their meaning.

Table 1: Signal Names

Name	Meaning
+12V	**+12 v**olt power supply
+3V3	**+3.3 v**olt power supply
+5VSTBY	**+5 V st**and**by** power supply
-12V	**-12 v**olt power supply
16MHZ	**16 MHz** clock used for keyboard and ILACC
20MHZ	**20 MHz** clock used for ILACC and MPC
/2IPL(0:2)	**I**nterrupt **p**riority **l**ines to secondary CPU
5MHZ	**5 MHz** clock used for CIOs and local interrupt decoder
A(1:31)	VMEbus **a**ddress lines
/ABEN	**A**ddress **b**uffer **en**able for VMEbus
/ACFAIL	VMEbus **ACFAIL** signal
/ACLD	**A**ddress **c**onverter **l**oa**d** of IOC-2
AGND	**A**nalog **g**rou**nd** for graphic CLUT
ALE	**A**ddress **l**atch **e**nable of ILACC
AM(0:5)	VMEbus **a**ddress **m**odifier
ASCTRL	**A**ddress **s**ize **c**on**tr**o**l** from System CIO to address decoder
/ASIZ0	**A**ddress **siz**e **0** from address decoder to VIC
/ASIZ1	**A**ddress **siz**e **1** from address decoder to VIC
/ASV	**A**ddress **s**trobe **V**MEbus
/AVEC	**A**uto**vec**tor signal of secondary CPU
/BB	**B**us **b**usy signal of '040 bus
/BBSY	VMEbus **b**us **bs**y signal
BCLK	**B**us **c**loc**k**
BCLK/2	**B**us **c**loc**k** divided by **2**
BCLK1	**B**us **c**loc**k 1**

Table 1: Signal Names (Continued)

Name	Meaning
BCLK2	**B**us **cl**oc**k 2**
BCLK3	**B**us **cl**oc**k 3**
BCLKD	**B**us **cl**oc**k d**elayed
/BCLKEN	**B**us **cl**oc**k en**able signal
/BCLR	VMEbus **b**us **cl**ea**r** signal
/BERRV	**B**us **err**or **V**MEbus
/BG0IN	VMEbus **b**us **g**rant **0 in**
/BG0OUT	VMEbus **b**us **g**rant **0 out**
/BG1	**B**us **g**rant **1** (primary CPU)
/BG1IN	VMEbus **b**us **g**rant **1 in**
/BG1OUT	VMEbus **b**us **g**rant **1 out**
/BG2	**B**us **g**rant **2** (secondary CPU)
/BG20	**B**us **g**rant for '0**20** bus
/BG2IN	VMEbus **b**us **g**rant **2 in**
/BG2OUT	VMEbus **b**us **g**rant **2 out**
/BG3IN	VMEbus **b**us **g**rant **3 in**
/BG3OUT	VMEbus **b**us **g**rant **3 out**
/BGACK	**B**us **g**rant **ack**nowledge for '020 bus
/BGCONV	**B**us **g**rant for bus **conv**erter
/BGILACC	**B**us **g**rant for **ILACC**
/BGLEB	**B**us **g**rant for **LEB**
/BGSCSI	**B**us **g**rant for **SCSI** (NCR53C720)
/BGVME	**B**us **g**rant for **VME**bus (VIC on '020 bus)
BLK	**Bl**an**k** for hex display
/BLT	**Bl**ock **t**ransfer
/BR(0:3)	VMEbus **b**us **r**equest **0-3**
/BR1	**B**us **r**equest **1** (primary CPU)
/BR2	**B**us **r**equest **2** (secondary CPU)
/BRCONV	**B**us **r**equest bus **conv**erter
/BRILACC	**B**us **r**equest **ILACC**

Table 1: Signal Names (Continued)

Name	Meaning
/BRLEB	**B**us **r**equest **LEB**
/BRSCSI	**B**us **r**equest **SCSI**
/BRVME	**B**us **r**equest **VME**bus (VIC)
C2CTS	**C**hannel **2** **c**lear **t**o **s**end
C2DCD	**C**hannel **2** **d**ata **c**arrier **d**etect
C2DTR	**C**hannel **2** **d**ata **t**erminal **r**eady
C2RTS	**C**hannel **2** **r**equest **t**o **s**end
C2RXD	**C**hannel **2** **r**eceive **d**ata
C2TXD	**C**hannel **2** **t**ransmit **d**ata
C3CTS	**C**hannel **3** **c**lear **t**o **s**end
C3DCD	**C**hannel **3** **d**ata **c**arrier **d**etect
C3DTR	**C**hannel **3** **d**ata **t**erminal **r**eady
C3GND1	**C**hannel **3** **g**rou**nd** pin **1**
C3GND4	**C**hannel **3** **g**rou**nd** pin **4**
C3RTS	**C**hannel **3** **r**equest **t**o **s**end
C3RXD	**C**hannel **3** **r**eceive **d**ata
C3TXD	**C**hannel **3** **t**ransmit **D**ata
C4CTS	**C**hannel **4** **c**lear **t**o **s**end
C4DCD	**C**hannel **4** **d**ata **c**arrier **d**etect
C4DTR	**C**hannel **4** **d**ata **t**erminal **r**eady
C4GND1	**C**hannel **4** **g**rou**nd** pin **1**
C4GND4	**C**hannel **4** **g**rou**nd** pin **4**
C4RTS	**C**hannel **4** **r**equest **t**o **s**end
C4RXD	**C**hannel **4** **r**eceive **d**ata
C4TXD	**C**hannel **4** **t**ransmit **d**ata
CACTRL	**Ca**che **c**on**t**ro**l** from system CIO to address decoder
/CBLANK	**C**omposite **blank**
/CDIS	**C**ache **dis**able
/CHSYNC	**C**omposite/**h**orizontal **sync** signal
CIOPA(0:7)	User **CIO p**ort **A 0-7**

Table 1: Signal Names (Continued)

Name	Meaning
CIOPC(0:3)	User **CIO p**ort **C 0-3**
CL1882	**Cl**ear sync generator signal
CLK40MHZ	**Clock 40 MHz**
CLKI	**Clock i**n (keyboard controller)
CLKLEB	**Clock** for **LEB**
CLKO	**Clock o**ut (keyboard controller)
CPUID	**CPU id**entification
/CSFEPR	**C**hip **s**elect **F**lash **EPR**OM
/CSKBD	**C**hip **s**elect **k**ey**b**oar**d** controller
/CSLEB	**C**hip **s**elect **LEB**
/CSMBX	**C**hip **s**elect **m**ail**b**o**x**
/CSREV	**C**hip **s**elect **rev**ision register
/CSRTC	**C**hip **s**elect **r**eal **t**ime **c**lock
/CSSCIO	**C**hip **s**elect **s**ystem **CIO**
/CSSCSI	**C**hip **s**elect **SCSI**
/CSSER	**C**hip **s**elect **ser**ial interface (MPC)
/CSUCIO	**C**hip **s**elect **u**ser **CIO**
/CSUEPR	**C**hip **s**elect **u**ser **EPR**OM
/CSVCNTR	**C**hip **s**elect **v**ideo **c**o**ntr**oller
/CSVDRES	**C**hip **s**elect **vid**eo controller **res**et
/CSVIC	**C**hip **s**elect **VIC**
/CSWDG	**C**hip **s**elect **w**atch**d**o**g**
/CVSYNC	**C**omposite/**v**ertical **sync** signal
D(0:31)	VMEbus **d**ata lines
DATI	**Dat**a **i**n (keyboard controller)
DATO	**Dat**a **o**ut (keyboard controller)
/DENO	**D**ata **en**able **o**ut for VMEbus buffers
DIGCLK	Graphic **dig**ital **cl**oc**k** output
DIRGR	**Dir**ection **gr**aphic data buffers
DLE	**D**ata **l**atch **e**nable signal of CPUs

Table 1: Signal Names (Continued)

Name	Meaning
/DS(0)	VMEbus **d**ata **s**trobe **0**
/DS(1)	VMEbus **d**ata **s**trobe **1**
DSCTRL0	**D**ata **s**ize **c**on**t**ro**l 0** from system CIO to address decoder
DSCTRL1	**D**ata **s**ize **c**on**t**ro**l 1** from system CIO to address decoder
DSF	Video RAM function select signal
/DTACK	VMEbus **d**a**t**a **ack**nowledge
/DTCL	**D**a**t**a acknowledge signal of **CL**-CD2401
EN24	**En**able A**24** slave decoder
EN32	**En**able A**32** slave decoder
/ENADR	**En**able **ad**d**r**ess bus from '040 bus to '020 bus
/ENDIGO	**En**able **di**gital **g**raphic **o**utput
/ENGR	**En**able **gr**aphic data buffer
ENICF1	**En**able **ICF 1** slave decoder
ENICF2	**En**able **ICF 2** slave decoder
/ENLIACK	**En**able **l**ocal **IACK** on I/O bus
/ENSLSEL	**En**able **sl**ave **sel**ect
/ENSNOOP	**En**able **snoop** control
EPRA(0:1)	**EPR**OM **a**ddress **0** and **1** on I/O bus
FC(0:2)	**F**unction **c**ode **0-2**
/FCIACK	**F**unction **c**ode for **IACK**
/FIRES	**FI**FO **res**et
FRAMEIN	**Frame in**active
GA(0:8)	**G**raphic video RAM **a**ddress bus
GD(0:31)	**G**raphic video RAM **d**ata bus
GND	**G**rou**nd**
GNDOSC	**G**rou**nd** for PLL **osc**illator
/GRST	**G**lobal **r**e**s**e**t**
/GSEL	**G**roup **sel**ect output of I/O bus decoder
/HALT	**HALT** signal of '020 bus
HI10	Pulled **hi**gh on page **1**0

Table 1: Signal Names (Continued)

Name	Meaning
HI13	Pulled **hi**gh on page **13**
HIGH501	Pulled **high** on page **5**
HIGH502	Pulled **high** on page **5**
HIGH503	Pulled **high** on page **5**
HIGH504	Pulled **high** on page **5**
HIGH505	Pulled **high** on page **5**
HIGH506	Pulled **high** on page **5**
HIGH6	Pulled **high** on page **6**
HIGH7	Pulled **high** on page **7**
/HOLDA	**Hold a**cknowledge for ILACC
HSYNC	**H**orizontal **SYNC** output
/HSYNC	**H**orizontal **SYNC** inverted
/I1IPL(0:2)	**I**n **1 i**nterrupt **p**riority **l**ine **0-2** (from VIC to PAL 02)
I5MHZ	**I**nverted **5 MHz** clock
IA(0:19)	**I**/O bus **a**ddress **0..19**
/IACK	VMEbus **i**nterrupt **ack**nowledge signal
/IACK6	**I**nterrupt **ack**nowledge for level **6**
/IACKCLCD	**I**nterrupt **ack**nowledge for **CL**-**CD**2401
/IACKIN	VMEbus **i**nterrupt **ack**nowledge **in** signal
/IACKLEB	**I**nterrupt **ack**nowledge for **LEB**
/IACKOUT	VMEbus **i**nterrupt **ack**nowledge **out** signal
ICFD(0:7)	**I**nterprocessor **c**ommunication **f**acility **d**ata **0-7**
/ICFSEL1	**I**nterprocessor **c**ommunication **f**acility **sel**ect **1**
/ICFSEL2	**I**nterprocessor **c**ommunication **f**acility **sel**ect **2**
ID(0:7)	**I**/O bus **d**ata **0-7**
/ILACC	Chip select for **ILACC**
INIT	**Init**ialization LED
/IOAS	**I/O** bus **a**ddress **s**trobe
/IORD	**I/O** bus **rea**d signal
/IORDI	**I/O** bus **rea**d **i**n (CIO reset workaround)

Table 1: Signal Names (Continued)

Name	Meaning
/IOWE	**I/O** bus **w**rite **e**nable
/IRESET	**I**nternal **RESET**
/IRQ(1:7)	VMEbus **i**nterrupt **req**uest lines
/IRQ4	Local **i**nterrupt **req**uest level **4**
/IRQ6	Local **i**nterrupt **req**uest level **6**
/IRQCLI	**I**nterrupt **req**uest **CL**-CD2401
/IRQETH	**I**nterrupt **req**uest from **Eth**ernet
/IRQKBD	**I**nterrupt **req**uest from **k**ey**b**oar**d** controller
/IRQLEB	**I**nterrupt **req**uest from **LEB**
/IRQSCIO	**I**nterrupt **req**uest from **s**ystem **CIO**
/IRQSCSI	**I**nterrupt **req**uest from **SCSI** controller
/IRQUCIO	**I**nterrupt **req**uest from **u**ser **CIO**
/ISPEN	**I**n **s**ystem **p**rogramming **en**able
/JSEL	Boot **sel**ect Flash/user EPROM
KBDCLK	**K**ey**b**oar**d** **cl**oc**k**
KBDDATA	**K**ey**b**oar**d** **data**
LA(0:31)	**L**ocal **a**ddress **0-31** ('040 bus)
/LADI	**L**atch **ad**dress **i**n (VMEbus to '020 bus)
/LADO	**L**atch **ad**dress **o**ut ('020 bus to VMEbus)
LAEN	**L**ocal **a**ddress **en**able (VIC)
LD(0:31)	**L**ocal **d**ata ('040 bus)
LD1882	**L**oa**d** sync generator
LDP	**L**eft **d**ecimal **p**oint of hex display
/LEDI	**L**atch **e**nable **d**ata **i**n (VMEbus to '020 bus)
/LEDO	**L**atch **e**nable **d**ata **o**ut ('020 bus to VMEbus)
/LIACKO	**L**ocal **i**nterrupt **ack**nowledge **o**ut
LIRQ2	**L**ocal **i**nterrupt **req**uest **2**
/LLINE	**L**ow **line**
/LOCK	**LOCK** signal of '040 bus
LR/W	**L**ocal **r**ead/**w**rite

Table 1: Signal Names (Continued)

Name	Meaning
LSIZ(0:1)	**L**ocal **siz**e **0-1** ('040 bus)
/LWDENIN	**L**ow **w**ord **d**ata **en**able **in** (VIC)
/LWORD	VMEbus **l**ong **word** signal
/MASTER	ILACC is **master** of '020 bus
/MDIS	**M**MU **dis**able
/MI	**M**emory **i**nhibit
/MIO	**M**emory **i**nhibit **o**ut
/MPSEL	**Sel**ect color look-up table
/MWB	**M**odule **w**ants **b**us
/O1IPL(0:2)	**O**ut **1** **i**nterrupt **p**riority **l**ines **0-2**
ODD	**Odd** field signal
P(0:3)	**P**ixel port **0..3**
P(8:11)	**P**ixel port **8..11**
P(16:19)	**P**ixel port **16..19**
P(24:63)	**P**ixel port **24..63**
PAB(0:31)	**P**hysical **a**ddress **b**us ('020 bus)
/PABF	**P**ort **A** **b**urst **f**lag
PAFIEN	**P**ort **A** **FI**FO **en**able
/PAFIREQ	**P**ort **A** **FI**FO **req**uest
PAFIRW	**P**ort **A** **FI**FO **r**ead/**w**rite
PAMS	**P**ort **A** **m**aster/**s**lave
/PAS	**P**hysical **a**ddress **s**trobe ('020 bus)
/PBDBCENI	**P**ort **B** **d**ata **b**uffer **c**lock **en**able **i**nput
/PBDBCENO	**P**ort **B** **d**ata **b**uffer **c**lock **en**able **o**utput
/PBDOEN	**P**ort **B** **d**ata **o**utput **en**able
/PBERR	**P**hysical **b**us **err**or ('020 bus)
PBFIAF	**P**ort **B** **FI**FO **a**lmost **f**ull flag
/PBFICEN	**P**ort **B** **FI**FO **c**lock **en**able
/PBFIRW	**P**ort **B** **FI**FO **r**ead/**w**rite
/PBLANK	Complosite **blank** control output

Table 1: Signal Names (Continued)

Name	Meaning
PBMS	**P**ort **B** **m**aster/**s**lave
PBSW(0:4)	**P**ort **B** **sw**ap 0-4
/PBSWCEN	**P**ort **B** **sw**ap **c**lock **en**able
PCLK1	**P**rocessor **cl**oc**k** CPU **1**
PCLK2	**P**rocessor **cl**ock CPU **2**
PDB(0:31)	**P**hysical **d**ata **b**us **0-31** ('020 bus)
/PDS	**P**hysical **d**ata **s**trobe ('020 bus)
/PDSACK(0)	**P**hysical **d**ata **s**ize **ack**nowledge **0** ('020 bus)
/PDSACK(1)	**P**hysical **d**ata **s**ize **ack**nowledge **1** ('020 bus)
PI(32:35)	**P**ixel port **i**nternal **32..35**
PI(40:43)	**P**ixel port **i**nternal **40..43**
PI(48:51)	**P**ixel port **i**nternal **48..51**
PIXDEL	**Pix**el **del**ay signal
/PMI	**P**rimary CPU **m**emory **i**nhibit
PSC0	**P**rimary CPU **s**noop **c**ontrol **0**
PSC1	**P**rimary CPU **s**noop **c**ontrol **1**
PSEL	**P**ort **sel**ect signal
PSIZ(0)	**P**hysical **siz**e **0** ('020 bus)
PSIZ(1)	**P**hysical **siz**e **1** ('020 bus)
PST(0)	**P**rocessor **st**atus **0** (primary CPU)
PST(2)	**P**rocessor **st**atus 1 (primary CPU)
PST(3)	**P**rocessor **st**atus **3** (primary CPU)
/PWR	**P**hysical **wr**ite ('020 bus)
PXCLK	**Pix**el **cl**oc**k**
/RAMSEL	**RAM sel**ect
RASADR	**RAS ad**d**r**ess signal
/RDCIO	**R**ea**d** for **CIO**s (CIO reset work-around)
RDP	**R**ight **d**ecimal **p**oint of hex display
/READYL	**Ready L**ANCE (ILACC)
RESCYC	**Res**et **cyc**le

Table 1: Signal Names (Continued)

Name	Meaning
/RESET	**Reset** (main reset signal)
/RESOUT	**Res**et **out**
RFCLK	**Ref**resh **cl**oc**k**
/RMC	**R**ead **m**odify write **c**ycle ('020 bus)
/RSTMAX	**Res**e**t** from **MAX**695
/RSTO1	**R**ese**t o**ut **1** (for Ethernet controller)
/RSTOO	**Res**e**t o**ut **o**utput of primary CPU
/RSTSL	**Res**e**t sl**ave CPU (secondary CPU)
/SAS	**S**ynchronized **a**ddress **s**trobe
/SBGACK	**S**ynchronized **b**us **g**rant **ack**nowledge
/SBRILA	**S**ynchronized **b**us **r**equest from **ILA**CC
/SBRLEB	**S**ynchronized **b**us **r**equest from **LEB**
/SBRVME	**S**ynchronized **b**us **r**equest from **VME**bus (VIC)
SCLK	**S**erial **cl**oc**k** for video RAM
/SCLKC	**S**erial **cl**oc**k c**ontrol for video RAM
/SCON	**S**ystem **con**troller enable
/SCSIACK	**SCSI ack**nowledge
/SCSIATN	**SCSI at**te**n**tion
/SCSIBSY	**SCSI b**u**sy**
/SCSIC/D	**SCSI c**ontrol/**d**ata
SCSIDB(0:15)	**SCSI d**ata **b**us **0-15**
SCSIDP0	**SCSI d**ata **p**arity **0**
SCSIDP1	**SCSI d**ata **p**arity **1**
/SCSII/O	**SCSI i**nput/**o**utput
/SCSIMSG	**SCSI m**e**s**sa**g**e
/SCSIREQ	**SCSI req**uest
/SCSIRST	**SCSI r**e**s**e**t**
/SCSISEL	**SCSI sel**ect
SDCLK	**S**erial **d**ata **cl**ock output
SDIO	**S**erial **d**ata **i**nput/**o**utput

Table 1: Signal Names (Continued)

Name	Meaning
/SDS	**S**ynchronized **d**ata **s**trobe
/SEL16G	**Sel**ect **16 g**ated
/SEL20	**Sel**ect '0**20** bus
/SEL24	**Sel**ect **24**
/SEL24G	**Sel**ect **24 g**ated
/SEL32	**Sel**ect **32**
/SEL32G	**Sel**ect **32 g**ated
SEN-	Negative **sen**se signal for +3V3 voltage
/SERIACK	**Ser**ial **i**nterrupt **ack**nowledge
/SLAVE	**Slave** select signal for bus converter
/SMI	**S**econdary CPU **m**emory **i**nhibit
SSC0	**S**econdary CPU **s**noop **c**ontrol **0**
SSC1	**S**econdary CPU **s**noop **c**ontrol **1**
STATUS	Primary CPU **status** LED
/SWTOUT	**Sw**itch **out**
SYNSWAP	**Syn**c signal **swap**
SYSCLK	VMEbus **sys**tem **cl**oc**k**
/SYSFAIL	VMEbus **sys**tem **fail** signal
/SYSRESET	VMEbus **sys**tem **reset** signal
/TA	**T**ransfer **a**cknowledge
/TBI	**T**ransfer **b**ust **i**nhibit
/TCI	**T**ransfer **c**ache **i**nhibit
TCK	**T**est **c**loc**k**
TDI	**T**est **d**ata **i**n
TDO	**T**est **d**ata **o**ut
TDO01	**T**est **d**ata **o**utput **1**
TDO02	**T**est **d**ata **o**utput **2**
TDO03	**T**est **d**ata **o**utput **3**
TDO04	**T**est **d**ata **o**utput **4**
TDOBT	**T**est **d**ata **o**utput **Bt**445

Table 1: Signal Names (Continued)

Name	Meaning
TDOCP1	**T**est **d**ata **o**utput **CPU1**
/TEA	**T**ransfer **e**rror **a**cknowledge
THRCLK	**T**ransmit **h**olding **r**egister **cl**oc**k**
/TIP	**T**ransfer **i**n **p**rogress
TM(0:2)	**T**ransfer **m**odifier **0-2**
TMS1	**T**est **m**ode **s**elect **1**
/TRST	**T**est **r**e**s**e**t**
/TS	**T**ransfer **s**tart
TT0	**T**ransfer **t**ype **0**
TT1	**T**ransfer **t**ype **1**
/UWDENIN	**U**pper **w**ord **d**ata **en**able **in** (VIC)
VA0	**V**ideo RAM **a**ddress 0
VA1	**V**ideo RAM **a**ddress 1
VCC	Supply **v**oltage
VCCOSC	Supply **v**oltage for **osc**illator
VICCLK	**VIC cl**oc**k**
/VMESEL	**VME**bus **sel**ect
/VRESET	**V**IC **reset** output
/VROE	**V**ideo **R**AM **o**utput **e**nable
VSYNC	**V**ertical **sync**
/WDGOUT	**W**atch**d**og **out**put
WDS	**W**atch**d**og **s**tatus
/WORD	**Word** select for VMEbus
/WRB(0:3)	**Wr**ite **b**yte **0-3**
/WRCOMP	**Wr**ite VME slave **comp**arator
/WRITE	VMEbus **write** signal

2 Description of Schematics

2.1 Connectors P1 and P2

Circuit diagram, page 1.

X101 carries all signals necessary for A24/D16 VMEbus. Most of the control signals are connected to the VIC on page 3.

Row b of X102 carries the additional signals necessary for A32/D32 operation of the VMEbus. Rows a and c are used for serial, parallel and SCSI I/O.

Several block capacitors provide a clean power supply for the various chips of the EUROCOM-17-5xx. D101 suppresses high voltage transients on the +5 V power supply.

2.2 Connectors LEB and Memory Module

Circuit diagram, page 2.

X201 is the 32-bit version of ELTEC's Local Extension Bus. Several daughter boards can be fitted on the EUROCOM-17-5xx here. For detailed description of the LEB, see the LEB specification available from ELTEC.

X202 is the EUROCOM-17-5xx memory module connector. Several memory modules can be installed via this connector without making any changes on the base board necessary. The connector covers all 32 data and 32 address lines of the CPU bus and additionally some control signal times.

2.3 VIC

Circuit diagram, page 3.

U301 is the VMEbus interface chip. Most of the VMEbus control signals are connected to the VIC. On the local side the VIC has a 68020/30 like asynchronous bus interface. Since the VIC requires additional buffers for interfacing the data and address lines from/to the VMEbus it also provides some signals for controlling these buffers (/LADO, /LADI, /LEDO, /LEDI, DDIR, /ABEN, /UWDENIN, /LWDENIN, /DENO, /SWDEN, /ISOBEN).

Also the VIC contains the interrupt controller for VMEbus and the local interrupts. When one of the several interrupt conditions becomes true, the VIC requests interrupt service via /IPL(0:2) from the CPU. When the CPU performs the IACK-cycle the /FCIACK signal becomes low to indicate the interrupt-acknowledge read-cycle. Depending on the source of the interrupt the VIC performs a VMEbus IACK-cycle, or delivers the interrupt vector, or asserts the /LIACKO signal. /LIACKO is fed into U1701 that decodes which of the other devices shall deliver the interrupt vector.

S3 enables the system controller functions of the VIC when it is set to position 2-3.

U304 - U306 are used to synchronize several signals for the '020 arbiter.

U302 is a special synchronizer for the /PDS signal. This signal may be high for less than one clock cycle. This short time cannot be captured by a normal synchronizer. U302 also gates the VMEbus slave select signals with the corresponding enable signals. Furthermore, the /PBDBC0 signal for the IOC-2 and the 5 MHz clock for the CIO timing state machine are generated in U302.

The 64-bit VIC uses the /SCON pin to enable D64 function of the VMEbus buffers. To disable these functions when a 32-bit VIC is used J301 must be set to position 1-2.

2.4 VMEbus Buffers and Comparators

Circuit diagram, page 4.

U401 - U403 are address/data buffers, counters, and comparators specially designed to support the VIC. Most of the control signals of U401-403 are connected with the corresponding outputs of the VIC. /WRCOMP and PAB(2) are used to initialize the VMEbus slave comparators. U401 is used for A32, U402 for A24, and U403 for A16 access. For full support of the VIC's ICF features, U404 and U405 form a second programmable A16 decoder. The /LCOUT, /VCOUT, /LCIN, and /VCIN pins of U401-403 are used to propagate the carry of the BLT address counters.

2.5 CPUs

Circuit diagram, page 5.

U501 and U502 are the two CPUs. Most of their signals are connected together. U506 buffers address LA(0:7) for the I/O bus.

The jumpers J501 - J506 are used for the separate CPU VCC plane. The jumpers must be closed on an EUROCOM-17-5xx.

J507 is used for the boundary scan daisy chain. The jumper must be closed if no secondary CPU is installed, otherwise no PLDs can be programmed on the board. If a secondary CPU is installed, this jumper must be open, else TDI, TDO of the CPU2 JTAG port will be shortened.

2.6 SCSI Interface

Circuit diagram, page 6.

The SCSI controller U601 directly interfaces the '040 bus to a 16-bit SCSI bus. The SCSI controller performs DMA to the DRAM of the EUROCOM-17-5xx for fetching its program or for data transfer between the RAM and the SCSI bus. RN601-RN604 terminate the SCSI bus when the EUROCOM-17-5xx is located at the end of the SCSI bus. To be removable they are mounted on sockets.

2.7 Serial Interface

Circuit diagram, page 7.

U701 is a four channel serial interface chip called Multiprotocol Controller (MPC). It is connected to the '020 bus of the EUROCOM-17-5xx. Channel 0 is interfaced to X703 via U703, and supports two wire handshake with RS 232 levels. Channel 1 has four wire handshake and RS 232 levels. Channels 2 and 3 may be adapted to various signal levels by using ELTEC's SILC modules.

2.8 Ethernet Interface

Circuit diagram, page 8.

U801 is the ILACC Ethernet Controller. The ILACC has a built-in DMA controller to access the main memory of the EUROCOM-17-5xx. Since the ILACC has a multiplexed address/data bus the registers U804 and U805 capture the address when the ILACC performs DMA. Some control signals of the ILACC are connected to the '020 bus (/PDS, /PWR, /PSIZ(0:1)) while others are interfaced via U1701 (/READYL, /PDSACK(0:1), /BGACK, /PAS, /HOLDA). The standard AUI interface of the ILACC is connected to X801.

2.9 CIOs, Switches, Display

Circuit diagram, page 9.

U901 is used to read the hex switches on the front panel, to drive the hex display, and for board control functions. RN910 - RN916 ensure that the board control signals are high when the CIO is reset. U902 is the User CIO which is commonly used as printer port via ADAP and CONV boards. The CIOs share the /LIRQ6 input of the VIC with the MPC. The CIOs are connected to the I/O bus of the IOC-2.

2.10 Video RAM

Circuit diagram, page 10.

U1001-U1002 are used to buffer the data bus of the ‘040 bus. U1003-U1003 are 1 MB of video RAM, U1005 512 KB of overlay RAM accessible from the ‘040 bus via GD(0:31) and from the pixel port of the color look-up table BT445 via P(0:63). The overlay RAM is connected to the lower nibbles of either byte in a longword of the ‘040 bus.

2.11 Address Generator, Address Multiplexer, Sync Generator

Circuit diagram, page 11.

U1104-U1108 are the address multiplexers for the video RAM which is either addressed by the ‘040 bus (LA(0:19)) or by the VRAM controller (TRA(2:19)).

Input B of the multiplexer selects the VRAM controller when it is high. Input A selects RAS address when it is high.

U1101 is used to realize the address generator and VRAM controller. The internal registers can be accessed via the I/O bus. U1102 implements the sync generator. U1109 is used to buffer the sync signals.

If no graphic is installed on the EUROCOM-17-5xx, J1101 must be closed to bypass the boundary scan graphic devices.

J1102 is an additional jumper which should be open. This jumper is assigned to bypass the BT445 and both CPUs in the boundary scan path if necessary.

2.12 RAMDAC and Interface

Circuit diagram, page 12.

The RAMDAC U1201 reads data from its pixel port P(0:63) and converts them to red, green and blue outputs. The internal registers of the Bt445 can be accessed via the I/O bus. RN1201 terminates the video cable at the beginning. D1201-D1206 protect the RAMDAC against over- or under voltage.

A flat display can be connected via the VGA connector, too.Therefore, U1216 buffers the TTL data signals.

J1202 is used to enable the digital outputs for the flat display.

Via J1201 selects whether to supply normal or inverted clock at the VGA connector.

U1205 is used as a reference for the pixel clock generator. U1202 is used to supply a reference voltage for the internal PCC.

2.13 IOC-2 and Bus Converter

Circuit diagram, page 13.

The IOC-2 U1301 interfaces all data and address lines between the '040 bus and the '020 bus. The control signals are translated by U1302. U1302 incorporates several state-machines to handle lots of different cycles in both directions of the bus converter. One highlight is the dynamic bus-sizing that is performed in conjunction with the IOC-2. '040 to '020 operation is started when either /SEL20 or /GSEL become low or when TT0 and TT1 indicate IACK cycles. When the '020 bus is occupied, identified by /BG20 low, or if the FIFOs in the IOC-2 are busy, identified by FIRES high, U1302 sends a retry acknowledge to the '040 bus. Otherwise, it drives PBMS low to enable the address buffers in the IOC-2 from the '040 bus to the '020 bus and enables several control signals. After that it drives /PAS and /PDS low. Then it waits for a reply on the /PDSACK(0:1) or /PBERR signals. When it got the reply it decides whether the transfer is complete or additional cycles are necessary (dynamic bus-sizing). In the first case it sends the appropriate data and reply to the '040 bus. In the second case it uses the PBSW(0:4) to control the data swapper and registers in the IOC-2 and generates a next bus cycle on the '040 bus. This happens until the size requested by the '040 bus is

satisfied, which may be up to 16 cycles when a line access is performed to a byte slave on the LEB. '020 to '040 operation is started when /SLAVE and /SAS and /SDS become low. In this case the bus converter requests the '040 bus and performs the appropriate cycles. Highlight of the slave operation is block transfer where burst cycles are performed on the '040 bus with the aid of the FIFOs in the IOC-2. The IOC-2 also has an I/O bus where most of the peripheral devices and the EPROMs are connected.

U1303 is used to enable the '020 address bus during IACK cycles, too. This work-around is used because some VMEbus boards need A4-A32 high during an IACK cycle.

2.14 Watchdog and Reset

Circuit diagram, page 14.

U1402 contains the power monitor and the watchdog timer. When the power is below 4.65 V U1402 generates /RESOUT which resets the whole board via the VIC. S4 can also be used to generate reset. As long as the WDI input of the MAX695 is in high impedance state the watchdog timer is disabled. A positive edge on /CSWDG triggers one flip-flop of U1405 and enables the watchdog. From that on the WDI input of the MAX595 must toggle at least one time per watchdog period to prevent a watchdog reset. When a watchdog reset occurs the other flip-flop of U1405 is cleared. This indicates the watchdog reset to the System CIO (via WDS) and drives the left decimal point of the hex display (LDP). The watchdog indicator flip-flop is set with power-on reset or when the watchdog is triggered the next time. Half of U1406 and U1407 collect various reset signals and distribute them to the different devices. J1401 allows to select between two watchdog periods.

The /GRST signal is used to force a reset state during in system programming of the PLDs.

2.15 Clock Generation and Refresh

Circuit diagram, page 15.

U1504 is a PLL clock driver well suited for '040 systems. It generates PCLK and BCLK according the specification of the MC68040/MC68060. Since BCLK is needed for a lot of devices four BCLK outputs are available. This helps to keep the traces on the PCB short. J1501, J1502 are used to realize a EUROCOM-17-5xx version with 33 MHz PLCK and 33 MHz BCLK. Normally, BCLK is half of PCLK. So, the default jumper settings are 1-2. U1501 and U1502 generate 5 MHz and 20 MHz which are needed by the peripheral devices. U1505 delivers 64 MHz for the VIC. U1506 divides the 64 MHz by 4. This clock is used by the keyboard controller, the ILACC, and the refresh counter U1507.

2.16 EPROM, Flash EPROM, and SRAM

Circuit diagram, page 16.

The Flash EPROM U1601 is normally used to hold the basic initialization routines and the RMon monitor program. For programming a 28F02, J1611 must be closed. The soldering jumper J1603 allows also the use of a 29F04 which requires no programming voltage. U1602 is the user EPROM. J1605 can be set to position 1-2 for EPROMs that require +5 V at their pin 1 for read operation. To allow longword reads to the EPROMs the IOC-2 incorporates a byte collector. When the CPU reads the EPROMs the IOC-2 increments EPRA(0:1) until a longword is available for the CPU. U1603 is a 2, 8, or 32 KB battery buffered SRAM with real-time clock. It is used by the RMon to hold user configurable data. J1602, J1606 and J1607 allow adaption to the 2, 8, or 32 KB version of the SRAM/RTC. U1604 is a buffer for LA(8:19) required by the EPROMs.

If a MK 48T18 is installed, J1602 must be changed from position 1-2 to 2-3. If a DS1644 is installed, J1602 must be changed from position 1-2 to 2-3. J1606, J1607 must be closed and R1602 must be removed. The Dallas timekeeper RAMs do not offer the feature to check the battery. The SGS Thomson devices allow to check an internal battery OK flag.

2.17 Keyboard Controller, Control Logic

Circuit diagram, page 17.

X1701 is a 6-pin mini DIN connector for connection of PS/2 compatible keyboards. The EUROCOM-17-5xx communicates with the keyboard via two bidirectional signals KBDDATA and KBDCLK. The two capacitors C201 and C202 suppress cross talk between the two signals.

The keyboard controller U1703 is connected to the I/O bus of the IOC-2.

The revision EEPROM is U1704 which can be write-protected via J1702. The serial EPROM is connected to U1701 via SDIO and SDCLK.

U1701 implements the control logic to interface the ILACC, CIOs and the serial revision EEPROM.

U1701 also contains the CIO reset work-around which ensures that CIOs are not reset when Motorola bus protocol is used on the I/O bus.

The IACK decoder that decodes which of the other devices shall deliver the interrupt vector is implemented in U1701, too.

Also the slave CPU control, '040 buffer mode control and the IOC-2 configuration is realized in U1701.

When /RSTL is set to high, the secondary CPU starts to run. The secondary CPU may be interrupted by three sources: the LEB via /IRQLEB, the VIC timer via LIRQ2 and the primary CPU by writing the secondary CPU control register. Furthermore, the appropriate VIC reset signals are generated by U1701.

J1703 routes one of the VMEbus interrupts IRQ1, 3, 5, 7 to the secondary CPU.

J1701 selects booting from the Flash EPROM or user EPROM.

2.18 Address Decoding and Arbiter

Circuit diagram, page 18.

U1801 is the main address decoder. It also generates /TBI and /TCI for those regions not covered by the IOC-2. The decoder for the peripheral devices handled by the IOC-2 is implemented in U1801, too. The decoder becomes active when the IOC-2 drives /IOAS low. The device select signals are gated with the PAMS signal which is low when the bus converter is active from the 040 to the 020 bus.

U1804 allows programming of the snoop mode for the two CPUs. U1805 is used to enable the VMEbus slave select signals. This is necessary because the comparators are undefined on power-on.

U1802 is the 020 bus and 040 bus arbiter. U1802 also generates the STATUS signal which indicates activity of the primary CPU. The memory inhibit signals of the two CPUs are also combined in U1802. Since this introduces wait-states to the RAM cycles, this function can be switched off by J1801 for single processor operation. Furthermore, U1802 generates the /PBFIRW signal from /PRW and /FIRES to optimize BLT performance.

X1801 is the JTAG port connector. It is used for on-board programming of the MACH445 and for the boundary scan test.

3 Hardware Selftest

After reset a selftest checks all vital parts of the EUROCOM-17-5xx. The status display on the front panel is used to signal which test is in progress, or what kind of exception occurred, with a unique number. The status display is updated at the beginning of each test (see Table 2: 'Hardware Test Display Values'). If a test fails or if an exception occurs during the test, the test of that device is repeated until it is successful.

This description reflects version 2.6 of the RMon.

While selftest is running the right decimal point of the display is on.

Since the system CIO must be initialized before any value can be displayed, the first number that can normally be seen on the display is '2'. Some tests consist of more than one part. In this case the invisible upper nibble of the display value is used to distinguish between these parts. If such a test fails, it is vital to know the invisible part of the display value (subvalue). The easiest way to check this is to connect a storage oscilloscope to /CSSCIO and to inspect the I/O bus data lines ID(0:7).

Table 2: Hardware Test Display Values

Display	Subvalue [1)]	Task in Progress
1	0	First access to the hex display
1	1	Initialize Snoop Control Register
2	0	System CIO initialization
3	0	Calculate checksum of EPROM part
4	0	First access to VIC
4	1	VIC initialization
5	0	RAM test: Long Word access to 0
5	1	RAM test: Byte write and long read
5	2	RAM test: Word write and long read
5	3	RAM test: Random test pattern
6	0	VME Address Decoder access
7	0	Graphic: Access to controller
7	1	Graphic: Test of CLUT
7	2	Graphic: Word test pattern to Frame Buffer
7	3	Graphic: Random test pattern
8	0	MK48T12/18: Check if battery empty
8	1	MK48T12/18: RAM test
9	1	Test secondary CPU present
9	2	CL-CD2401: Access to GFRCR
9	3	CL-CD2401: Test register access
9	4	NCR53C720: Check if present
9	0	Warmstart entry
A	0	Address error exception
B	0	Bus error exception
C	0	Illegal instruction exception
D	0	Any other exception

1. Nibble not visible.

3.1 Reset

Display: undefined (disabled)

If the display remains dark after reset, the following things should be checked:

- PCLK, BCLK and /RESET at U501
- BCLK and /RESET at U1301
- about 4 µs after /RESET has gone high /BR1 should go low
- the arbiter U505 drives /BG1 low
- the CPU U501 asserts /BB, /TS, /TIP, ..., and LA(0:31) = $0000.0000
- the IOC-2 generates /CSFEPR (or /CSUEPR if J1301 is closed)
- the EPROM delivers the first byte of the initial stack pointer
- after some 100 ns the IOC-2 increments EPRA(0:1)
- after four bytes have been fetched the IOC-2 asserts the initial stack pointer at LD(0:31) and gives /TA
- the CPU reads the initial program counter
- the CPU reads the location where the initial program counter points to
- the CPU tests ICR and IOALR registers of the IOC-2 for correct values
- the CPU initializes some IOC-2 registers
- the CPU writes 01 to the display
- the CPU writes the Snoop Control Register (only if layout ≥ 2)

3.2 System CIO Initialization

Display: 2 Subvalue: 0 (disabled or enabled)

At the end of the initialization the display is enabled. The initialization is only repeated if an exception occurs.

3.3 EPROM Checksum

Display: 3 Subvalue: 0

If this test fails the address lines IA(0:19) and LA(0:19) should be checked whether there are shortcuts or interruptions (the data lines should be ok).

3.4 First Access to VIC

Display: 4 Subvalue: 0

The only way to fail this test is that an exception occurs (normally bus error) or that the computer hangs. This is the first access from the '040 bus to the '020 bus. The following things should be checked:

- the CPU reads ICFR1 of the VIC at $FEC0.10AF
- the IOC-2 generates /GSEL and /IOAS
- U1302 generates PBMS and /ENADR low
- the IOC-2 drives PAB(0:31)
- U1801 generates /CSVIC
- U1302 generates /PAS and /PDS
- the VIC asserts PDB(0:7) and /DSACK(0:1)
- U1302 deasserts /PAS and /PDS
- U1302 deasserts PBMS, /ENADR and asserts /TA

3.5 Minimum VIC Initialization

Display: 4 Subvalue: 1

This test fails if a value can't be stored in the appropriate VIC register (i.e. the value read differs from the value written). Check PAB(0:7), PDB(0:7) and PBSW(0:4) lines.

3.6 RAM Test

Display: 5 Subvalue: 0

Various test pattern are written to $0000.0000 and read back. If they are not the same, the test is repeated. If the test fails, the following should be inspected:

- refresh is running (/RFACK is low for some 100 ns every 16 µs, CAS before RAS refresh on DRAM and VRAM)
- the CPU writes to $0000.0000
- RAM controller generates /RAS(0) (early cycle start)
- CASADR becomes high about 13 ns after /RAS(0) goes low
- /RAMSEL becomes low
- RAM controller drives /WRB(0:3) low and asserts /CAS(0) low
- RAM controller drives /TA low
- RAM controller deasserts /RAS(0) and /CAS(0)
- on the read cycle B0D(0:31) have the same data pattern as during the write

The test may hang if the DRAM controller fails to generate /TA. If the test is successful the data lines to bank 0 of the DRAM are all right.

Display: 5 Subvalue: 1 and 2

If the test fails, there is normally something wrong with the /WRB(0:3) signals.

Display: 5 Subvalue: 3

If this test fails, there is normally something wrong with the addressing of the DRAM. Inspect VRAD(2:8), RA(8:10) and IA(23:24). Also there may be something wrong with bank 1 of the DRAM (if present).

3.7 VMEbus Address Decoder

Display: 6 Subvalue: 0

Since the VMEbus decoders can't be read back, this only fails if an exception occurs.

3.8 Access to Video Controller

Display: 7 Subvalue: 0

If the first access to the video controller ends in a bus error, it is assumed that the board has no graphic interface and none of the following graphic tests is performed. The board then uses the serial port for I/O.

3.9 Test of CLUT

Display: 7 Subvalue: 1

The CLUT of the video controller is written with random values and then read back. If the values are not the same, the test is repeated. This tests the I/O bus to the color look-up table. Note that the CLUT registers are only 8 bits wide. A CLUT write cycle roughly runs in the following order:

- the CPU writes to the CLUT
- the IOC-2 generates /GSEL and /IOAS, ID(0:7), /IOROI
- address decoder U1801 generates /MPSEL
- U1301 deasserts /IOAS, /IOROI and asserts /TA

Read cycles are performed in the correponding manner.

3.10 Video RAM Test

Display: 7 Subvalue: 2 and 3

These tests are very similar to the RAM tests described in Section 3.6 'RAM Test'.

3.11 MK48T12 Battery Test

Display: 8 Subvalue: 0

If the battery of the MK48T12 is exhausted, the first write operation after power-on fails. If this happens, the RMon uses EPROM initialization values regardless of the setting of the hex switch S902 and a message is printed.

3.12 MK48T12 RAM Test

Display: 8 Subvalue: 1

One byte of the SRAM is tested with some test pattern.

3.13 Secondary CPU

Display: 9 Subvalue: 1

The presence of a secondary CPU is tested by trying to run a small program on it. If the secondary CPU is present, it alters a memory location. This can be detected by the primary CPU.

3.14 Serial Controller Access

Display: 9 Subvalue: 2

This test fails if there is a bus error or if the Global Firmware Revision Code Register is zero.

3.15 Serial Controller Register Test

Display: 9 Subvalue: 3

Various test patterns are written to the A Receive Buffer Address Lower register of the CL-CD2401. The test fails if the values read are different from written values.

3.16 SCSI Controller

Display: 9 Subvalue: 4

The NCR53C720 is reset and two registers are tested whether they have the correct initial values. If not, a flag is set which later prevents initialization of the NCR53C720 that would lead to a hang-up. If the NCR53C720 is not present booting and using the RMon **scsi** command also causes a hang-up, but at least RMon runs.

3.17 Watchdog

During a test the watchdog may be triggered unintentionally. In this case the board is reset after the watchdog period has expired and the left decimal point on the display is set. Typically this happens periodically. Note that the watchdog input of the MAX695 has a rather high impedance, so that moisture or dirt on the board may trigger the watchdog.

3.18 Halt and Hang-up

There are several ways the computer can crash.

- The CPU enters the HALT state when nested exceptions occur. In this case the LED near the reset button on the front panel goes off.
- The CPU accesses an address where no /TA or /TEA occurs. In this case the LED near the reset button stays on and /BB and /TIP are low all the time. Normally no such holes exist in the address map of the EUROCOM-17-5xx, so that this only happens when the addressed device doesn't respond.
- The CPU accesses an address where it always gets a retry acknowledge (/TA and /TEA low). This happens if FIRES gets stucks high or /BG20 gets stuck low.

3.19 Exceptions

If an exception occurs during selftest, the exception handler writes one of the letters 'A', 'B', 'C', or 'D' onto the display (depending on the kind of exception) and enters a delay loop, so that the letter can be recognized. After that the faulty test is repeated. This typically leads to the next exception so that two altering letters can be seen on the display.

There is a little trap in conjunction with the display because the upper nibble of port C of the CIO is used as write enable for the lower nibble (only those bits in the lower nibble are written where the corresponding bit in the upper nibble is clear). Alternating writes of $14 and $0B for example lead to alternating '5' and 'B' on the display.

3.20 Untested Peripherals

The User CIO and the Ethernet Controller are not tested because they are not necessary for RMon.

4 Default Parameters for RMon

Table 3: Default Parameters of RMon 2.6 located on EUROCOM-17-5xx

Beginning	End	Description
Group A: I/O Initialization		
$0800	$087F	VIC parameter
$0880	$088F	- reserved -
$0890	$08AF	Serial channel 1 parameters
$08B0	$08CF	Serial channel 2 parameters
$08D0	$08EF	Serial channel 3 parameters
$08F0	$090F	Serial channel 4 parameters
$0910	$092F	CIO1 parameters
$0930	$094F	CIO2 parameters
$0950	$0951	SCSI chip parameter
$0952	$0AEF	- reserved -
Group B: Address Information		
$0AF0	$0AF1	ICF1 address
$0AF2		ICF2 address
$0AF3		VME A24 slave address
$0AF4	$0AF5	VME A32 slave address
$0AF6		VME A24 slave size
$0AF7		VME A32 slave size
$0AF8		VME enable bits
$0AF9	$0B47	- reserved -
Group C: Hooks		
$0B48	$0B4F	User hooks
$0B50	$0B63	- Reserved -
$0B64	$0B67	Company name
$0B68	$0B6B	Board name
$0B6C	$0B6F	Portation

Table 3: Default Parameters of RMon 2.6 located on EUROCOM-17-5xx (Continued)

Beginning	End	Description
Group D: Boot Parameters		
$0B70		Autoboot flags
$0B71		Operating system
$0B72		SCSI controller ID
$0B73		SCSI controller Hardware
$0B74		SCSI logical unit number
$0B75		Special boot flag
$0B76		Sector size (unused)
$0B78		Base address for RAM/ROM boot
$0B7C		Own SCSI ID
$0B7D		Retry counter for NetBoot
$0B7E		Delay until autoboot starts
$0B80	$0B87	- reserved -
$0B88	$0BC7	Drive command
$0BC8	$0BD7	Own internet address
$0BD8	$0C17	Internet bootfile name (incl. host internet address)
$0C18	$0C1B	Slave board address
$0C1C	$0C1D	BootP flag
$0C1E	$0C1F	Network boot time-out value
$0C20	$0C4F	Server name
$0C50	$0C57	- reserved -
Group E: Board Information		
$0C58		- reserved -
$0C59		Character I/O port number
$0C5A	$0C5B	- reserved -
$0C5C		Watchdog enable flag
$0C5D	$0C67	- reserved -
$0C68	$0C87	Internal board information
$0C88	$0C8D	-reserved -
$0C8E		Board ID
$0C90	$0C93	RMon base address
$0C94		Number of CPUs installed
$0C95		- reserved -
$0C96		Memory size in MB

Table 3: Default Parameters of RMon 2.6 located on EUROCOM-17-5xx (Continued)

Beginning	End	Description
Group F: Video Descriptor		
$0CA0		Graphic Mode
$0CA1		Graphic Bit Mode
$0CA2		Display Start Address
$0CA6	$0CA9	Size of Graphic Plane
$0CAA	$0CAD	Size of Display Window
$0CAF	$0CB0	Fore- and Background color
$0CB1	$0CB2	Number of Columns and Lines
$0CB3		Video Descriptor Format
$0CB4	$0CB7	Position of Character Window
$0CC0	$0CFF	Video Timing Parameter
$0D00	$0DFB	-reserved -
$0DFC	$0DFF	Checksum

Type declarations for the following definitions:

```
struct io_data
{
  unsigned char value;
  unsigned char registerno;
};
```

4.1 Group A: I/O Initialization ($0000.0800 - $0000.0AEF)

4.1.1 VIC Parameter

- **Definition:** **struct io_data vic[0x40];**
- **Description:** Initialization values for VIC registers. First member is value, second member is VIC register number. Register number '-1' marks end.

Some of these values may be overwritten, depending on the system configuration value 'ramsize'. Have a close look at the specification of this value first.

- **RAM Address:** $0000.0800 - $0000.087F
- **Default Data:**

```
{0x00, 0xab}, {0xf0, 0xaf}, {0x60, 0xb3}, {0x40, 0x57},
{0x01, 0xa7}, {0x46, 0xa3}, {0x00, 0xb7}, {0x12, 0xc3},
{0x82, 0xc7}, {0x16, 0xcb}, {0x82, 0xcf}, {0x00, 0xd3},
{0x00, 0xd7}, {0x00, 0xdb}, {0x00, 0xdf}, {0x80, 0x7f},
{0x81, 0x07}, {0x82, 0x0b}, {0x83, 0x0f}, {0x84, 0x13},
{0x85, 0x17}, {0x86, 0x1b}, {0x87, 0x1f}, {0x1c, 0x53},
{0x77, 0x47}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}
```

4.1.2 Serial Channel 1 Parameter

- **Definition:**

```
1  struct serial_data {
2    unsigned long baud;
3    unsigned char bitchar;
4    unsigned char parity;
5    unsigned char stopb;
6  };
```

- **Description:** Initialization values for CD2401 Channel 1.
- **RAM Address:** $0000.0890 - $0000.08AF
- **Default Data:**

```
9600, 8, 0, 0,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff,
```

4.1.3 Serial Channel 2 Parameter

- **Definition:**

```
1  struct serial_data {
2    unsigned long baud;
3    unsigned char bitchar;
4    unsigned char parity;
5    unsigned char stopb;
6  };
```

- **Description:** Initialization values for CD2401 Channel 2.
- **RAM Address:** $0000.08B0 - $0000.08CF
- **Default Data:**

```
9600, 8, 0, 0,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff,
```

4.1.4 Serial Channel 3 Parameter

- **Definition:**

```
1  struct serial_data {
2    unsigned long baud;
3    unsigned char bitchar;
4    unsigned char parity;
5    unsigned char stopb;
6  };
```

- **Description:** Initialization values for CD2401 Channel 3.
- **RAM Address:** $0000.08D0 - $0000.08EF
- **Default Data:**

```
9600, 8, 0, 0,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff,
```

4.1.5 Serial Channel 4 Parameter

- **Definition:**

```
1  struct serial_data {
2    unsigned long baud;
3    unsigned char bitchar;
4    unsigned char parity;
5    unsigned char stopb;
6  };
```

- **Description:** Initialization values for CD2401 Channel 4.
- **RAM Address:** $0000.08F0 - $0000.090F
- **Default Data:**

```
9600, 8, 0, 0,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff, 0xff,
0xff,
```

4.1.6 CIO 1 Parameter

- **Definition:** **struct io_data cio1[0x10];**
- **Description:** Initialization values for CIO 1.
  First member is value, second member is CIO register number. Register number '-1' marks end.
- **RAM Address:** $0000.0910 - $0000.092F
- **Default Data:**

{0x89, 0x40}, {0x00, 0x41}, {0x00, 0x20}, {0x00, 0x28},
{0x80, 0x23}, {0xff, 0x2b}, {0xf0, 0x06}, {0x94, 0x01},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}

4.1.7 CIO 2 Parameter

- **Definition:** **struct io_data cio2[0x10];**
- **Description:** Initialization values for CIO 2.
  First member is value, second member is CIO register number. Register number '-1' marks end.
- **RAM Address:** $0000.0930 - $0000.096F
- **Default Data:**

{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff},
{0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}, {0xff, 0xff}

4.1.8 SCSI Chip Parameter

- **Definition:** **unsigned char ownid;**
  unsigned char rstflag;
- **Description:** Initialization values for the SCSI controller. The first byte holds the own SCSI ID. The second byte is used as flag. If set to a value not equal to zero, the RMon will generate a SCSI Reset at cold- and warmstart.
- **RAM Address:** $0000.0950 - $0000.0951
- **Default Data:** **0x07, 0x01**

4.2 Group B: Address Information ($0000.0AF0 - $0000.0B47)

4.2.1 ICF1 Address

- **Definition:** **unsigned short icf1_addr;**
- **Description:** Slave address of ICMS in VMEbus short I/O range. Only bits 15-6 are used for A15-A6 of slave address. By default, RMon enables this slave access.
- **RAM Address:** $0000.0AF0 - $0000.0AF1
- **Default Data:** **$8000**

4.2.2 ICF2 Address

- **Definition:** **unsigned char icf2_addr;**
- **Description:** Slave address of ICGS in VMEbus short I/O range. Only bits 7-0 are used for A15-A8 of slave address. By default, RMon disables this slave access.
- **RAM Address:** $0000.0AF2
- **Default Data:** **$00**

4.2.3 VMEbus A24 Slave Address

- **Definition:** **unsigned char std_addr;**
- **Description:** Slave address of VMEbus standard I/O range. Only bits 7-4 are used for A23-A20 of slave address. By default, RMon enables this slave access.
- **RAM Address:** $0000.0AF3
- **Default Data:** **$80**

4.2.4 VMEbus A32 Slave Address

- **Definition:** **unsigned short ext_addr;**
- **Description:** Slave address of VMEbus extended I/O range. Only bits 15-4 are used for A31-A20 of slave address. By default, RMon enables this slave access.
- **RAM Address:** $0000.0AF4
- **Default Data:** **$8000**

4.2.5 VMEbus A24 Slave Size

- **Definition:** **unsigned char std_size;**
- **Description:** Size of VMEbus slave standard address range in MB.
- **RAM Address:** $0000.0AF6
- **Default Data:** **$01**

4.2.6 VMEbus A32 Slave Size

- **Definition:** **unsigned char ext_size;**
- **Description:** Size of VMEbus slave extended address range in 16 MB.
- **RAM Address:** $0000.0AF7
- **Default Data:** **$10**

Changing the VMEbus A24 or A32 slave size does not effect the hardware because the VMEbus A24 and A32 slave size is fixed to 4 MB.

4.2.7 VMEbus Enable Bits

- **Definition:** **unsigned char vme_enable;**
- **Description:** VMEbus slave access enable flags
  bit 3: ICF2,
  bit 2: ICF1,
  bit 1: standard,
  bit 0: extended
- **RAM Address:** $0000.0AF8
- **Default Data:** **$05** (enables ICF1, extended)

4.3 Group C: Hooks ($0000.0B48 - $0000.0B6F)

- **Definition:** **unsigned long user_hook[6];**
- **Description:** Pointer list to user hooks.
  hook[0]: init,
  hook[1]: entry,
  hook[2]: reserved,
  hook[3]: reserved,
  hook[4]: reserved,
  hook[5]: reserved,
  hook[6]: reserved,
  hook[7]: company name,
  hook[8]: board name
  hook[9]: portation.
- **RAM Address:** $0000.0B48 - $0000.0B6F
- **Default Data:**

$FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF, $FFFF.FFFF

4.4 Group D: Boot Parameters ($0000.0B70 - $0000.0C57)

4.4.1 Autoboot Flag

- **Definition:** **unsigned char autoboot;**
- **Description:** Autoboot flags.
  Bit 7: Not autoboot,
  Bit 1: debug output,
  Bit 0: OS-9 debug enable
  This value is configurable by means of the setup utility.
- **RAM Address:** $0000.0B70
- **Default Data:** **$82**

4.4.2 Operating System

- **Definition:** **unsigned char os;**
- **Description:** Operating system.
  $FF: OS-9,
  $FE: LynxOS
  This value is configurable by means of the setup utility.
- **RAM Address:** $0000.0B71
- **Default Data:** **$FF**

4.4.3 SCSI Controller ID

- **Definition:** **unsigned char conid;**
- **Description:** Controller ID. This value is configurable by means of the setup utility.
- **RAM Address:** $0000.0B72
- **Default Data:** **$06**

4.4.4 SCSI Controller Hardware

- **Definition:** **unsigned char conhard;**
- **Description:** Controller hardware.
  $00: Omti,
  $01: SCSI Harddisk,
  $02: SCFL,
  $03: TEAC SCSI Floppy
  $04: TEAC FC-1-01 SCSI Floppy
  This value is configurable by means of the setup utility.
- **RAM Address:** $0000.0B73
- **Default Data:** **$01**

4.4.5 SCSI Logical Unit Number

- **Definition:** **unsigned char lun;**
- **Description:** Logical unit number.
  Valid values: $00, $20, $40, $60.
  This value is configurable by means of the setup utility.
- **RAM Address:** $0000.0B74
- **Default Data:** **$00**

4.4.6 Special Boot Flag

- **Definition:** **unsigned char specboot;**
- **Description:** Special bootstraps
  $FF: None,
  $FD: Streamer tape,
  $FE: Ramdisk,
  $FC: Ethernet,
  $FB: ROM boot (wait for NMI),
  $FA: Direct ROM boot,
  This value is configurable by means of the setup utility.
- **RAM Address:** $0000.0B75
- **Default Data:** **$FF**

4.4.7 Sector Size

- **Definition:** **unsigned short secsize;**
- **Description:** OS-9 sector size. RMon does not use this value.
- **RAM Address:** $0000.0B76
- **Default Data:** **$FFFF**

4.4.8 Base Address of RAM/ROM Boot

- **Definition:** **unsigned long romkerneladdr;**
- **Description:** Base address of ROM kernel or RAM disk.
  This value is used for special bootstraps '$FB' and '$FA'. It is configurable by means of the setup utility.
- **RAM Address:** $0000.0B78
- **Default Data:** **$0000.0000**

4.4.9 Retry Counter for Network Boot

- **Definition:** **unsigned char;**
- **Description:** Retry counter for network boot.
  This value is used as counter to call the network bootstrap port until the RMon is called again.
- **RAM Address:** $0000.0B7D
- **Default Data:** **$00**

4.4.10 Delay until Auto Starts

- **Definition:** **unsigned start autob;**
- **Description:** This value specifies the delay (seconds) before the autoboot sequence starts.
- **RAM Address:** $0000.0B7E
- **Default Data:** **$0009**

4.4.11 Logical Sector Offset

- **Definition:** **unsigned long lsnoffset;**
- **Description:** Logical Sector Offset
- **RAM Address:** $0000.0B80
- **Default Data:** **$0000.0000**

4.4.12 Device Command

- **Definition:** **unsigned char drive_cmd[0x40];**
- **Description:** Drive commands. The command list for configurated drive will be copied here by the setup utility.
- **RAM Address:** $0000.0B88 - $0000.0BC7
- **Default Data:**

$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00

4.4.13 Own Internet Address

- **Definition:** **unsigned char internethost[0x10];**
- **Description:** Internet host address.
  Notation: xxx.xxx.xxx.xxx
  'xxx': address component (all values ASCII)
  This string must always be zero filled for a correct termination. It is configurable by means of the setup utility.
- **RAM Address:** $0000.0BC8 - $0000.0BD7
- **Default Data:**

$30, $2E, $30, $2E, $30, $2E, $30, $00,
$00, $00, $00, $00, $00, $00, $00, $00

4.4.14 Internet Boot File Name

- **Definition:** **unsigned char internetboot[0x40];**
- **Description:** Boot file address/name.
  Notation: xxx.xxx.xxx.xxx:filename
  'xxx': address component (all values ASCII)
  This string must always be zero filled for a correct termination. It is configurable by means of the setup utility.
- **RAM Address:** $0000.0BD8 - $0000.0C17
- **Default Data:**

$30, $2E, $30, $2E, $30, $2E, $30, $3A,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00

4.4.15 BootP Flag

- **Definition:** **unsigned short bootp;**
- **Description:** This value specifies the network boot port number.
  0x0000: TFTP
  0x0001: BOOTP
- **RAM Address:** $0000.0C1C
- **Default Data:** **$0000**

4.4.16 Network Boot Time-out

- **Definition:** **unsigned start nettaut;**
- **Description:** Time-out value for network boot.
- **RAM Address:** $0000.0C1E
- **Default Data:** **$0010**

4.4.17 Server Name

- **Definition:** **unsigned char sname [0x30];**
- **Description:** Server name.
  This string must always be zero filled for a correct termination.
- **RAM Address:** $0000.0C20 - 0C4F
- **Default Data:**

$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00,
$00, $00, $00, $00, $00, $00, $00, $00

4.5 Group E: Board Information ($0000.0C58 - $0000.0C9B)

4.5.1 Character I/O Ports

- **Definition:** **unsigned char portno;**
- **Description:** Character I/O port.
  Valid values: 1 - 2 for default SCC driver.
- **RAM Address:** $0000.0C59
- **Default Data:** **$00**

4.5.2 Watchdog Enable Flag

- **Definition:** **unsigned char wdog_enable;**
- **Description:** Enable watchdog timer.
  Bit 0 = 0: watchdog disabled
  Bit 0 = 1: watchdog enabled
- **RAM Address:** $0000.0C5C
- **Default Data:** **$00**

4.5.3 Internal Board Information

- **Definition:** **unsigned char board_info[0x20];**
- **Description:** ELTEC internal board information for service purposes.
  This information is changed be the RMon during startup.

These values should not be modified!!!

- **RAM Address:** $0000.0C68 - $0000.0C87
- **Default Data:**

$30, $41, $41, $31, $31, $31, $30, $30,
$30, $30, $30, $30, $30, $04, $55, $55,
$FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF,
$FF, $FF, $FF, $FF, $FF, $FF, $FF, $FF

4.5.4 CPU Board Identification

- **Definition:** **unsigned char board_id;**
- **Description:** Unique number for each hardware platform.
  Valid values:
  13: E16
  14: IBAM-30
  15 E17
  27 E27 or E17-500

This value should not be modified!!!

- **RAM Address:** $C8E
- **Default Data:** 27

4.5.5 RMon Base Address

- **Definition:** **unsigned long rmon;**
- **Description:** Base address of RMon jump table for user-applicable routines.
- **RAM Address:** $0000.0C90
- **Default Data:** **$FE00.0000**

4.5.6 Number of CPUs

- **Definition:** **unsigned char scpu;**
- **Description:** Holds the number of CPUs installed on the board. This value is changed by RMon during coldstart.
  Valid values:
  $01: One CPU installed
  $02: Two CPUs installed
  $FF: Only one CPU installed
- **RAM Address:** $0000.0C94
- **Default Data:** **$01**

4.5.7 Size of Local Memory

- **Definition:** **unsigned short memsize;**
- **Description:** Size of local memory in MB found during cold- or warmstart.
  This value is changed by RMon
- **RAM Address:** $0000.0C96
- **Default Data:** **$FFFF**

4.6 Group F: Video Descriptor

4.6.1 Graphic Mode

- **Definition:** **unsigned char rto_mode;**
- **Description:**
  Bits 0 - 3: Internal number used as index in the video descriptor table
  Bit 4: Enable Overlay
  Bit 5: Enable Digital output
- **RAM Address:** $0000.0CA0
- **Default Data:** **$02**

4.6.2 Graphic Bit Mode

- **Definition:** **unsigned char rto_gbm;**
- **Description:**
  Number of bits per pixel.
  Valid values:
  $03: 8 Bits per pixel
  $02: 4 Bits per pixel
  $01: 2 Bits per pixel
  $00: 1 Bit per pixel
- **RAM Address:** $0000.0CA1
- **Default Data:** **$03**

4.6.3 Display Start Address

- **Definition:** **unsigned char rto_baseaddr;**
- **Description:**
  Start address of video frame buffer.
  Valid values:
  $0FC0.0000: Start address of normal video mode
  $0FE0.0000: Start address of overlay buffer
- **RAM Address:** $0000.0CA2
- **Default Data:** **$0FC0.0000**

4.6.4 Size of Graphic Plane

- **Definition:** **unsigned short rto_plnsizx, rto_plnsizy;**
- **Description:** Size of graphic plane in X and Y direction.
- **RAM Address:** $0000.0CA6 - $0000.0CA9
- **Default Data:** **800, 600**

4.6.5 Size of Display Window

- **Definition:** **unsigned short rto_plnsizx, rto_plnsizy;**
- **Description:** Size of window in X and Y direction.
- **RAM Address:** $0000.0CAA - $0000.0CAD
- **Default Data:** **800, 600**

4.6.6 Number of Fore-Background Color

- **Definition:** **unsigned char rto_fcol, rto_bcol;**
- **Description:** Number of foreground and background color.
  Valid values:

0: black	8: grey
1: navy blue	9: blue
2: dark green	10: green
3: dark cyan	11: cyan
4: dark red	12: red
5: dark magenta	13: magenta
6: dark yellow	14: yellow
7: light grey	15: white

- **RAM Address:** $0000.0CAF - $0000.0CB0
- **Default Data:** **0, 15**

4.6.7 Number of Columns and Lines

- **Definition:** **unsigned char rto_noofclms, rto_nooflins;**
- **Description:** This values define the number of columns and lines of the character window.
- **RAM Address:** $0000.0CB1 - $0000.0CB2
- **Default Data:** **80, 24**

4.6.8 Video Descriptor Format

- **Definition:** **unsigned char rto_vdform;**
- **Description:** Format of video descriptor.
  Valid values:
  $00: No position follows.
  The character window is placed in the center of the display window.
  $01: The following two values specify the position of the character window within the display window.
- **RAM Address:** $0000.0CB3
- **Default Data:** 0

4.6.9 Position of Character Window

- **Definition:** **unsigned short rto_wdworgx, rto_wdworgy;**
- **Description:** Position of the left upper pixel of the character window within the display window.
- **RAM Address:** $0000.0CB4 - $0000.0CB7
- **Default Data:** **0, 0**

4.6.10 Video Timing Parameter

- **Definition:** **unsigned long rto_param[0x38];**
- **Description:** Video Timing description.
  The values within this array have the meaning:

RAM Address	Mnemonic	Meaning	Unit
$0000.0CC0	pfreq	Pixel Frequency	[Hz]
$0000.0CC4	hres	Horiz. Resolution	[pixel]
$0000.0CC8	hperiod	Horiz. Period	[pixel]
$0000.0CCC	hsync	Horiz. Sync width	[pixel]
$0000.0CD0	hbporch	Horiz. Back Porch	[pixel]
$0000.0CD4	vres	Vert. Resolution	[lines]
$0000.0CD8	vperiod	Vert. Period	[lines]
$0000.0CDC	vsync	Vert. Sync width	[lines]
$0000.0CE0	vbporch	Vert. Back Porch	[lines]
$0000.0CE4	syncmode	Sync Mode	
$0000.0CE8	eqlen	Equalization width	[pixel]
$0000.0CEC	serlen	Serration width	[pixel]
$0000.0CF0	eqstart	Equalization start	[lines]
$0000.0CF4	eqserin	Equ./Ser. interval	[lines]
$0000.0CF8	vres[2]	reserved	

The bits of the 'syncmode' ($0000.0CE4) have the following meaning:

Bit Position	Mnemonic	Meaning
0x0000	HPOS	Horiz. sync is positive
0x0002	VPOS	Vert. sync is positive
0x0004	GSYNC	Sync on Green
0x0008	CSYNC	Composite Sync
0x0010	TSYNC	Tessellated Sync
0x0080	DBLANKP	Disable blank pedestal

- **RAM Address:** $0000.0CC0 - $0000.0CFF
- **Default Data:**

40000000, 800, 1056, 128, 88, 600, 628, 4, 23,
0x0000, 64, 128, 1, 8, 0, 0,

4.7 Checksum

- **Definition:** **unsigned long checksum;**
- **Description:** NVRAM checksum.
  This value is read only and is set or compared by the RMon commands **re** or **we**, respectively.
- **RAM Address:** $0000.0BFC - $0000.0BFF
- **Default Data:** **$FFFF.FFFF**

5 Parts List

Table 4: Parts List, Hardware Rev. 1.A

Part No.	Count	Part Type	Case	Socket	Comment
C100	1	C,C,100NF-2R	C,1206-BOT-S-K		
C101..104	4	C,T,33/10-1/2R	CAP,TA-ETR3		
C105	1	C,T,10/16-SMD	CAP,TA-C/D-TOP		
C106	1	C,T,10/25-1/2R	CAP,TA-ETR3		
C107	1	C,T,10/16-SMD	CAP,TA-C/D-TOP		
C108	1	C,C,10NF-2R	C,1206-BOT-S-K		
D101	1	DIO,TVS305	DIODE,DO-35-5R		
X101	1	X,P1	CONN,VG96		
X102	1	X,P2	CONN,VG96		
X103..104	2	BOLZEN_106	BOLZEN_106		
..213	13	R,1K-SMD	R,1206-BOT-S-K		
X201	1	X,LEB,100-BAS	X,LEB,100-BAS		
X202	1	X,2X50-F-SMD	X,2X50-F-SMD-BS		
J301	1	J,1X3-DC12-SMD	J,1X3-DC12-SMD-L		
R301	1	R,4K7-SMD	R,1206-BOT-S-K		
R302	1	R,1K-SMD	R,1206-BOT-S-K		
R303	1	R,150-SMD	R,1206-BOT-S-K		
U301	1	VIC068-PQF-5	PGA,145-PIN	Q	
U302	1	CE20V8-7-PLCC	PLCC,28-PIN		E27_*06
U304..306	3	74F5074-SO	SO,14-PIN		
U401..403	3	CY7C964-QFP	QFP,64-PIN		
U404	1	74F374-SO	SO,20-PIN		
U405	1	74F521-SO	SO,20-PIN		
J501..507	7	J,1X2-SMD	J,1X2-SMD-LS		
R501..502	2	R,1K-SMD	R,1206-BOT-S-K		
R503	1	R,150-SMD	R,1206-BOT-S-K		
R504	1	R,1K-SMD	R,1206-BOT-S-K		

Table 4: Parts List, Hardware Rev. 1.A (Continued)

Part No.	Count	Part Type	Case	Socket	Comment
R505..510	6	R,470-SMD	R,1206-BOT-S-K		
R512	1	R,470-SMD	R,1206-BOT-S-K		
R513	1	R,1K-SMD	R,1206-BOT-S-K		
R514	1	R,470-SMD	R,1206-BOT-S-K		
R515..523	9	R,1K-SMD	R,1206-BOT-S-K		
T501..504	4	J,1X1-SMD	J,1X1-SMD		
U501..502	2	68060-50-PGA	PGA,223-PIN-18-X	Q	
U506	1	74F245-SO	SO,20-PIN		
R601..602	2	R,1K-SMD	R,1206-BOT-S-K		
RN601..604	4	RN,8X220/330	RN,8xX/Y-1.1	Q	
U601	1	NCR53C720-QFP	SQFP,208-PIN		
C701..704	4	C,C,100PF-2R	C,1206-BOT-S-K		
D701	1	DIO,1N4148	DIODE,DO-35		
R701	1	R,470-SMD	R,1206-BOT-S-K		
R702..704	3	R,2K2-SMD	R,1206-BOT-S-K		
R705..712	8	R,10-SMD	R,1206-BOT-S-K		
U701	1	CL-CD2401-QFP	QFP,100-PIN		
U703..704	2	SN75C1406-SO	SO,16-PIN-DBL		
X701..702	2	X,SILC-RS232C	SILC,HYBRID-1.4	Q	
X703	1	X,6-PIN-AMP+S	X,6-PIN-AMP+S		
C801	1	C,T,47/10-SMD	CAP,TA-C/D-TOP		
C802	1	C,C,100NF-2R	C,1206-BOT-S-K		
C803..804	2	C,V,10NF-1R	C,1206-BOT-S-K		
L801	1	L,100UH	L,2-PIN-5R		
R801	1	R,470-SMD	R,1206-BOT-S-K		
R802	1	R,1K-SMD	R,1206-BOT-S-K		
R803..806	4	R,40.2-0805	R,0805-BOT-S-K		
R807	1	PTC425	PTC425		
R808..811	4	R,1K-SMD	R,1206-BOT-S-K		
U801	1	AM79C900-PLCC	PLCC,84-PIN		

Table 4: Parts List, Hardware Rev. 1.A (Continued)

Part No.	Count	Part Type	Case	Socket	Comment
U804..805	2	74ABT16374-SO	SO,48-PIN		
X801	1	X,MD-F,15-GW/GND	CONN,15-PIN-DF		
R901	1	R,330-SMD	R,1206-BOT-S-K		
R902..916	15	R,4K7-SMD	R,1206-BOT-S-K		
S901..902	2	S,HEX-H	SW,HEX,9-PIN-ALT		
U901..902	2	Z8536-PLCC	PLCC,44-PIN		
U903	1	TIL311	DIP,14-PIN,100		
R1001	1	R,470-SMD	R,1206-BOT-S-K		
R1002	1	R,150-SMD	R,1206-BOT-S-K		
U1001..1002	2	74ABT16646-SO	SO,56-PIN		
U1003..1005	3	TMS55166-70DGH	SOP64		
U1006	1	74ACT257-SO	SO,16-PIN-BOT		
U1007	1	74F32-SO	SO,14-PIN-BOT		
U1008..1010	3	74ACT257-SO	SO,16-PIN-BOT		
J1101	1	J,1X2-SMD	J,1X2-SMD-LS		
J1102	1	J,1X3-SMD	J,1X3-SMD-LS		
R1101..1116	16	R,22-SMD	R,1206-BOT-S-K		
U1101	1	MACH445-15-QFP	QFP,100-PIN		E27_*04
U1102	1	LM1882CM-SO	SO,20-PIN		
U1103	1	DELAY,SO,5X5	SO,8-PIN-BOT		
U1104..1108	5	74ACT153-SO	SO,16-PIN		
U1109	1	74ABT125-SO	SO,14-PIN-BOT		
C1201..1204	4	C,C,100NF-2R	C,1206-BOT-S-K		
C1205..1207	3	C,C,10NF-2R	C,1206-BOT-S-K		
C1208..1209	2	C,C,100NF-2R	C,1206-BOT-S-K		
C1210	1	C,T,47/10-SMD	CAP,TA-C/D-TOP		
C1211	1	C,C,10NF-2R	C,1206-BOT-S-K		
C1213	1	C,C,10NF-2R	C,1206-BOT-S-K		
C1214	1	C,T,4.7/25-SMD	CAP,TA-C/D-TOP		
C1215	1	C,C,1NF-2R	C,1206-BOT-S-K		

Table 4: Parts List, Hardware Rev. 1.A (Continued)

Part No.	Count	Part Type	Case	Socket	Comment
D1201..1206	6	DIO,LL101A	MM-TOP		
J1201	1	J,1X3	J,1X3		
J1202	1	J,1X2	J,1X2		
L1201	1	FB,60MHZ	FB		
R1201	1	R,22-SMD	R,1206-BOT-S-K		
R1202	1	R,10K-SMD	R,1206-BOT-S-K		
R1203	1	R,523-MF	R,1206-BOT-S-K		
R1204	1	R,1K-MF	RES,1/4W		
R1205	1	R,40.2-MF	RES,1/4W		
R1210	1	PTC425	PTC425		
R1211	1	R,1K-SMD	R,1206-BOT-S-K		
RN1201	1	RN,8X150	RN,8xXX-1.1	Q	
U1201	1	BT445-PQFP	PQFP,160-PIN		
U1202	1	LM385	TO-92		
U1203	1	74ABT125-SO	SO,14-PIN		
U1204	1	74AS1000-SO	SO,14-PIN		
U1205	1	OSC,25.175MZ-SMO	OSC,4-PIN-SMO		
U1207	1	74AS1000-SO	SO,14-PIN-BOT		
U1216	1	74ABT646-SO	SO,24-PIN		
X1201	1	X,15/3-DF-G	X,15/3-DF-G		
R1301	1	R,1K-SMD	R,1206-BOT-S-K		
U1301	1	IOC2	SQFP,208-IOC2		
U1302	1	MACH445-15-QFP	QFP,100-PIN		E27_*03
U1303	1	74ABT125-SO	SO,14-PIN-BOT		
C1402	1	C,T,10/25-1/2R	CAP,TA-ETR3		
J1401	1	J,1X2-SMD	J,1X2-SMD-LS		
R1401..1402	2	R,3K3-SMD	R,1206-BOT-S-K		
R1403	1	R,22-SMD	R,1206-BOT-S-K		
R1404	1	R,470-SMD	R,1206-BOT-S-K		
R1405..1407	3	R,220-SMD	R,1206-BOT-S-K		

Table 4: Parts List, Hardware Rev. 1.A (Continued)

Part No.	Count	Part Type	Case	Socket	Comment
R1408	1	R,3K3-SMD	R,1206-BOT-S-K		
R1409	1	R,100K-SMD	R,1206-BOT-S-K		
R1410..1411	2	R,3K3-SMD	R,1206-BOT-S-K		
U1402	1	MAX695-SO	SO,16-PIN-WP		
U1405	1	74LS74-SO	SO,14-PIN		
U1406	1	74ACT125-SO	SO,14-PIN		
U1407	1	74F125-SO	SO,14-PIN		
C1501..1506	6	C,C,100NF-2R	C,1206-BOT-S-K		
C1507	1	C,T,10/16-1R	C,TA-C-TOP		
C1508	1	C,C,100NF-2R	C,1206-BOT-S-K		
C1509	1	C,C,1NF-2R	C,1206-BOT-S-K		
C1510	1	C,C,330PF-2R	C,1206-BOT-S-K		
C1511	1	C,C,3.3NF-2R	C,1206-BOT-S-K		
C1512..1514	3	C,E,220/10	C,EKR05		
D1501	1	DIO,BYS21-45	DIODE,A398a		
D1502..1505	4	DIO,BYM10-50	GL-41		
J1501..1502	2	J,1X3-SMD	J,1X3-SMD-LS		
L1501	1	L,35UH	L,4-PIN-ALT		
Q1501	1	SI-9430DY	SO,8-PIN-BOT		
Q1502	1	SI-9410DY	SO,8-PIN-BOT		
R1501	1	R,10-SMD	R,1206-BOT-S-K		
R1502	1	R,22-SMD	R,1206-BOT-S-K		
R1503	1	R,1K-SMD	R,1206-BOT-S-K		
R1504	1	R,22-SMD	R,1206-BOT-S-K		
R1505	1	R,47-SMD	R,1206-BOT-S-K		
R1506	1	R,470K-SMD	R,1206-BOT-S-K		
R1507	1	R,330-SMD	R,1206-BOT-S-K		
R1508	1	R,47-SMD	R,1206-BOT-S-K		
R1509	1	R,1K-SMD	R,1206-BOT-S-K		
R1510	1	R,10-SMD	R,1206-BOT-S-K		

Table 4: Parts List, Hardware Rev. 1.A (Continued)

Part No.	Count	Part Type	Case	Socket	Comment
R1511..1512	2	R,22-SMD	R,1206-BOT-S-K		
R1513	1	R,10-SMD	R,1206-BOT-S-K		
R1514	1	R,22-SMD	R,1206-BOT-S-K		
R1515..1516	2	R,10-SMD	R,1206-BOT-S-K		
R1517..1518	2	R,22-SMD	R,1206-BOT-S-K		
R1519	1	R,1K-SMD	R,1206-BOT-S-K		
R1520	1	R,10K-SMD	R,1206-BOT-S-K		
R1521..1522	2	R,100-SMD	R,1206-BOT-S-K		
R1523	1	R,0.025-MF	L03-MEDIUM		
R1524	1	R,180-SMD	R,1206-BOT-S-K		
U1501	1	OSC,40MHZ-SMO	OSC,4-PIN-SMO		
U1502	1	74ACT161-SO	SO,16-PIN		
U1503	1	OSC,33.33MHZ-SMO	OSC,4-PIN-SMO		
U1504	1	MC88915FN100	PLCC,28-PIN		
U1505	1	OSC,64MHZ-SMO	OSC,4-PIN-SMO		
U1506	1	74ACT161-SO	SO,16-PIN		
U1507	1	74LS393-SO	SO,14-PIN		
U1508	1	LTC1148CN-3.3	SO,14-PIN-BOT		
U1509	1	DELAY,SO,5X5	SO,8-PIN		
C1603	1	C,T,10/16-SMD	CAP,TA-C/D-TOP		
J1601	1	J,1X2	J,1X2		
J1602..1603	2	J,1X3-DC12-SMD	J,1X3-DC12-SMD-L		
J1605	1	J,1X3	J,1X3		
J1606..1607	2	J,1X2-SMD	J,1X2-SMD-LS		
R1601	1	R,10K-SMD	R,1206-BOT-S-K		
R1602	1	R,0-SMD	R,1206-BOT-S-K		
U1601	1	28F020-150-PLCC	PLCC,32-PIN		
U1602	1	SOCKET,32-PIN	DIP,32-PIN		
U1603	1	MK48T08B20@	DIP,28-PIN		
U1604	1	74ACT16245-SO	SO,48-PIN		

Table 4: Parts List, Hardware Rev. 1.A (Continued)

Part No.	Count	Part Type	Case	Socket	Comment
C1701..1702	2	C,C,68PF-2R	C,1206-BOT-S-K		
J1701..1702	2	J,1X2	J,1X2		
J1703	1	J,2X3-SMD	J,2X3-SMD-LS		
R1701..1702	2	R,3K3-SMD	R,1206-BOT-S-K		
R1703	1	PTC425	PTC425		
R1704..1707	4	R,2K2-SMD	R,1206-BOT-S-K		
R1708	1	R,10K-SMD	R,1206-BOT-S-K		
R1709..1711	3	R,2K2-SMD	R,1206-BOT-S-K		
U1701	1	MACH445-15-QFP	QFP,100-PIN		E27_*02
U1702	1	74F125-SO	SO,14-PIN-BOT		
U1703	1	MACH210-20-PLCC	PLCC,44-PIN		E27_*07
U1704	1	FM24C04-SO	SO,8-PIN-BOT		
U1705	1	74F125-SO	SO,14-PIN		
X1701	1	X,MINI-DIN-6-POL	X,MINI-DIN-6-POL		
J1801	1	J,1X3-DC12-SMD	J,1X3-DC12-SMD-L		
R1801..1805	5	R,1K-SMD	R,1206-BOT-S-K		
R1808	1	R,220-SMD	R,1206-BOT-S-K		
R1809..1810	2	R,1K-SMD	R,1206-BOT-S-K		
U1801	1	MACH445-20-QFP	QFP,100-PIN		E27_*01
U1802	1	MACH210-10-PLCC	PLCC,44-PIN		E27_*05
U1804..1805	2	74ACT174-SO	SO,16-PIN		
X1801	1	X,2X5-F-SMD-BS	X,2X5-F-SMD-BS		

Figure 1: Parts Location Diagram (Top View)

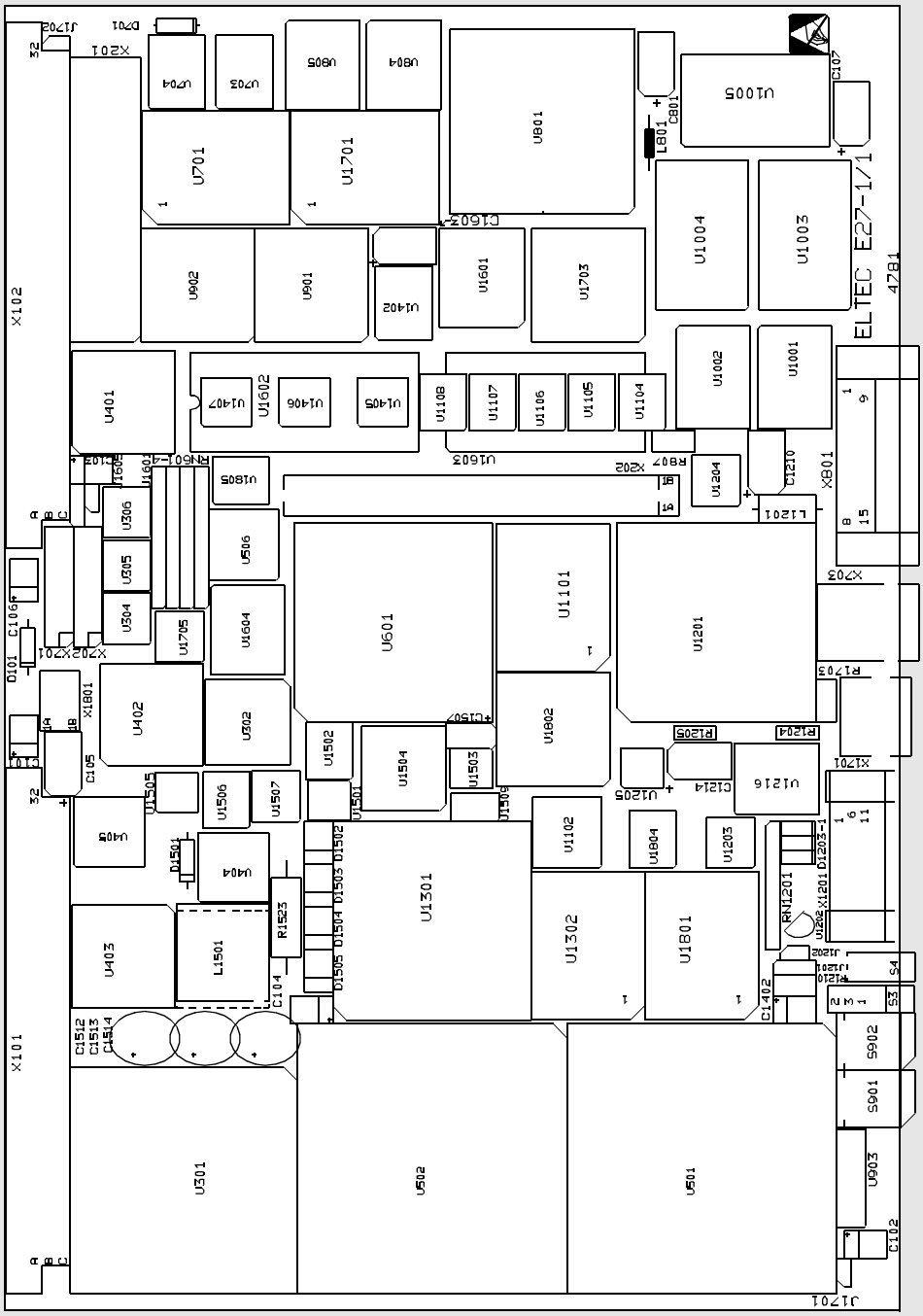

Figure 2: Parts Location Diagram (Bottom View)

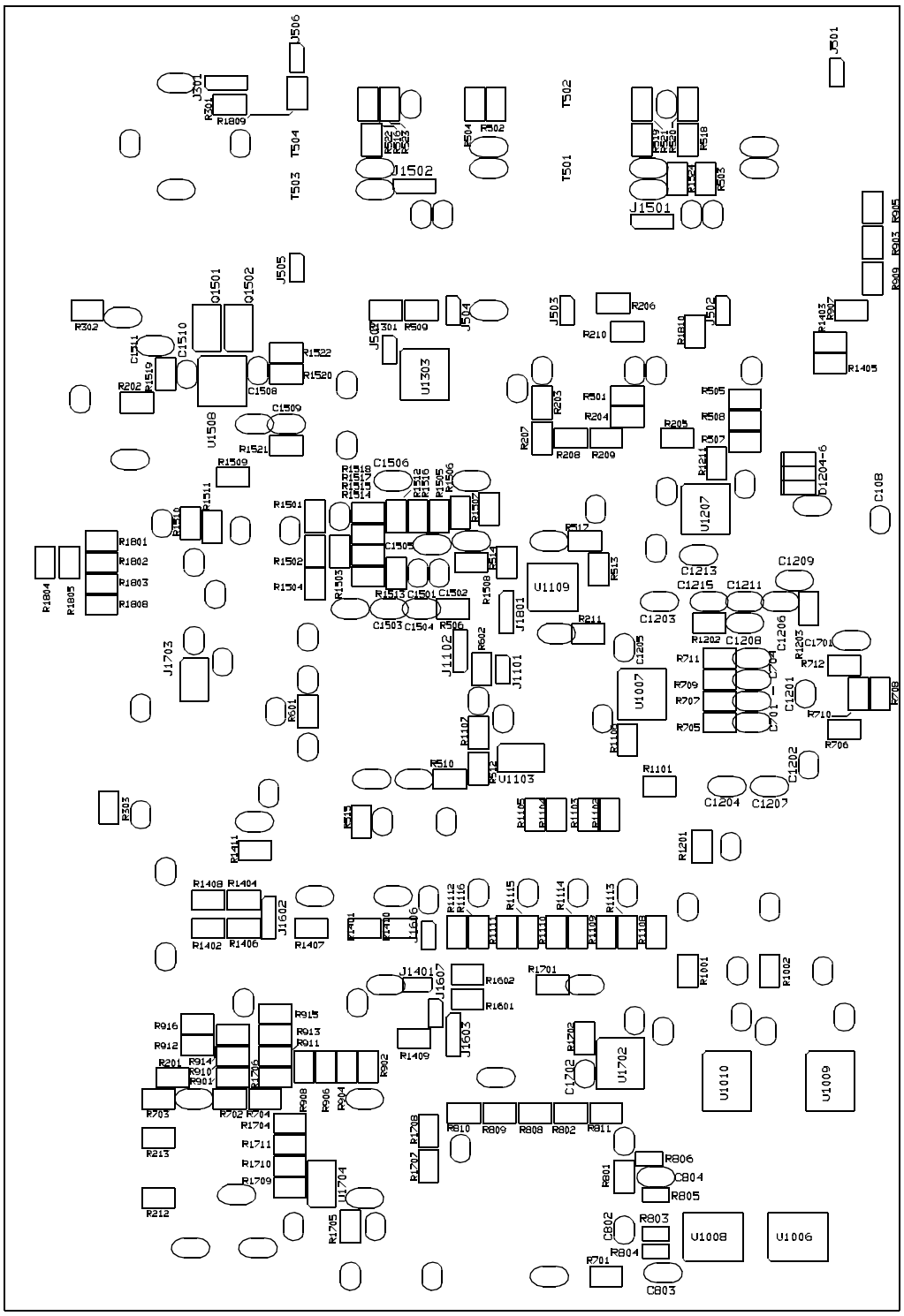

Figure 3: Jumper Location Diagram (Bottom View)

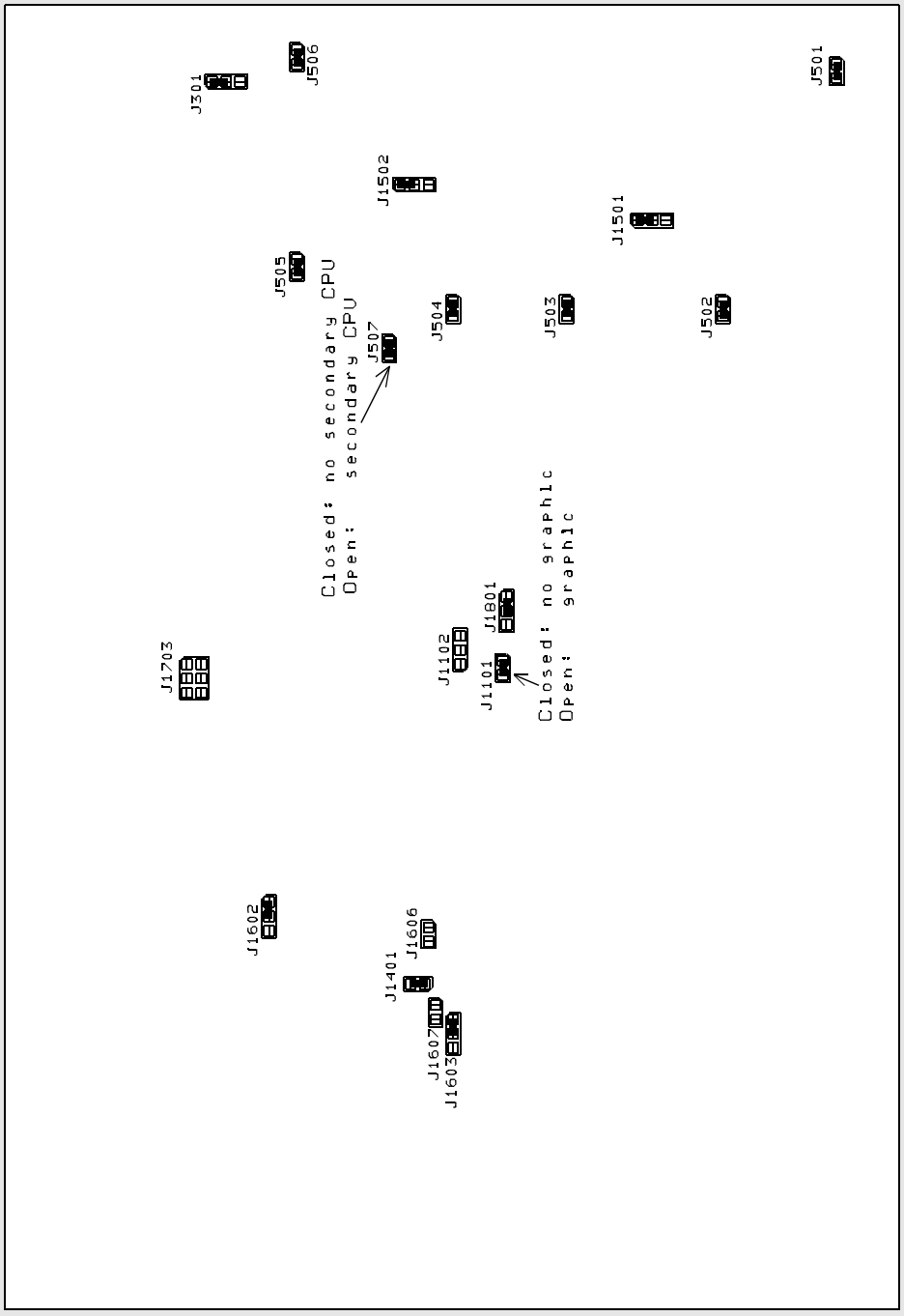

Figure 4: Jumper Location Diagram (Top View)