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PROGRAM

MICRO NOVA LOGIC TEST

TAPE

095-000423-00

ABSTRACT

THE MICRO NOVA LOGIC TEST IS A MAINTENANCE PROGRAM DESIGNED TO TEST THE MICRO NOVA CENTRAL PROCESSING UNIT. IT IS A FUNCTIONAL TEST OF THE LOGIC USED TO IMPLEMENT THE MICRO NOVA INSTRUCTION SET. ALSO INCLUDED IS A MINIMUM LEVEL TEST OF THE CPU I/O INSTRUCTIONS, TELETYPE I/O, AND PROGRAM INTERRUPT.

```
 0001 MNLGC MACRO REV 04.00              12:18:03 12/03/76
01
02
03
04
05
06
07              /*****************************************************************
08              /
09              / NAME: MNLGCT.SR                          PART NUMBER: 094-000034
10              /
11              /
12              / DESCRIPTION: MICRO NOVA LOGIC TEST
13              /
14              /
15              / REVISION HISTORY:
16              /
17              /       REV.            DATE
18              /
19              /       00              12/03/76
20              /
21              /
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23              / ALL RIGHTS RESERVED.
24              *****************************************************************
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 0002 MNLGC
01              /               MICRO NOVA LOGIC TEST
02              /1.     ABSTRACT
03              /       THE MICRO-NOVA LOGIC TEST IS A MAINTENANCE PROGRAM
04              /       DESIGNED TO TEST THE MICRO-NOVA CENTRAL PROCESSING
05              /       UNIT.  IT IS A FUNCTIONAL TEST OF THE LOGIC
06              /       USED TO IMPLEMENT THE MICRO-NOVA INSTRUCTION SET.
07              /       ALSO INCLUDED IS A MINIMUM LEVEL TEST OF THE
08              /       CPU I/O INSTRUCTIONS,TELETYPE I/O, AND
09              /       PROGRAM INTERRUPT.
10              /2. MACHINE REQUIREMENTS
11              /2.1    MICRO NOVA PROCESSOR
12              /2.2    4K OF READ/WRITE MEMORY
13              /2.3    BASIC I/O TELETYPE INTERFACE
14              /
15              /4.     OPERATING PROCEDURE
16              /4.1    VERIFY THAT THE MICRO-NOVA WILL PERFORM ALL
17              /       CONSOLE FUNCTIONS, I.E, EXAMINE/EXAMINE NEXT
18              /       DEPOSIT/DEPOSIT NEXT AC'S EXAMINE/DEPOSIT
19              /4.2    LOAD THE PROGRAM VIA THE BINARY LOADER.
20              /4.3    NORMAL STARTING ADDRESS IS 200
21              /4.4    OPTIONAL STARTING ADDRESSES ARE:
22              /       170     START WITH OUT CAT/KITTEN
23              /       171     START WITH CAT/KITTEN(MUST HAVE BEEN
24              /               PREVIOUSLY LOADED.)
25              /4.5    IF NOT A AUTO-START FROM DTOS THE
26              /       MACHINE SHOULD HALT AT LOC. 503. THIS VERIFIES CPU CAN
27              /       HALT IF THERE IS AN ERROR. PROCEED BY TYPING A "P".
28              /4.6    PROCESSOR SHOULD CONTINUE TO RUN WITHOUT HALTING
29              /       TELETYPE SHOULD STUTTER FOR 60 CHARACTERS
30              /       THE TYPEOUT "PASS" SHOULD OCCUR AND THE TEST
31              /       SHOULD CONTINUE TO LOOP WITH THE TELETYPE RUNNING
32              /       AT A SLOWER RATE IF THERE ISN'T CAT/KITTEN LOADED.
33              /
34              /4.7    TO RESTART , START AT LOC 170,171
35              /       SEE SEC. 4.4
36              /
37              /5.     ERROR DESCRIPTION
38              /5.1    DETECTED ERRORS WILL CAUSE THE PROGRAM TO DO A
39              /       PROCESSOR HALT.
40              /5.2    RECORD THE STATE OF THE PROCESSOR AND REGISTERS
41              /       AT THE TIME OF THE HALT.  CONSULT THE LISTING
42              /       AT THE ADDRESS OF THE ERROR HALT FOR PROBABLE
43              /        CAUSES OF THE FAILURE. CONSTRUCT A LOOP THAT
44              /       WILL REPEAT THE FAILURE AND SCOPE AS REQUIRED.
45              /6.     PROGRAM DESCRIPTION
46              /       THIS PROGRAM IS A COLLECTION OF SMALL TESTS,
47              /       EACH TEST IN SEQUENCE BASED ON PREVIOUS TESTS
48              /       WORKING AND DESIGNED TO TEST AS SMALL AN ADDI-
49              /       TIONAL PIECE OF THE LOGIC AS POSSIBLE.
50              /
51              /7. CAT/KITTEN OPERATION
52              /       IF THE PROGRAM WAS LOADED FROM DTOS WITH CAT
53              /       OR KITTEN THE PROGRAM WILL RUN IT IN
54              /       THE BACKGROUND AFTER ONE PASS OF USING THE TTY
55              /       INTERRUPTS. THE PROGRAM WILL RUN MUCH
56              /       SLOWER ALLOWING THE CAT/KITTEN AMPLE TIME TO
57              /       COMPLETE A PASS.
58              /       NOTE:
59              /       LOCATION 170 CAN BE USED AS A STARTING ADDRESS
60              /       TO OMIT CAT/KITTEN OPERATION.
```

```
0003 MNLGC
                        .TITL MNLGCT
02
03                  ;DEFINE MICRO NOVA/NOVA 3 SPECIAL INSTRUCTIONS
04
05        061401        .DIAC PSH = 061401        ;DIB AC,1         PUSH STACK
06        061601        .DIAC POP = 061601        ;DIBC AC,1        POP STACK
07        062401        .DUSR SAVE= 062401        ;DIC 0,1          SAVE ON STACK
08        062601        .DUSR RTRN= 062601        ;DICC 0,1         STACK RETURN
09        061001        .DIAC MTSP =61001         ;MOVE TO STACK POINTER
10        060001        .DIAC MTFP =60001         ;MOVE TO FRAME POINTER
11        061201        .DIAC MFSP = 61201        ;MOVE FROM STACK POINTER
12        060201        .DIAC MFFP = 60201        ;MOVE FROM FRAME POINTER
13        071077        .DUSR RTCEN=071077        ;DOA 2,77         ENABLE RTC
14        065077        .DUSR RTCDS=065077        ;DOA 1,77         DISABLE RTC
15        100010        .DUSR TRAP= 100010        ;ALC#,NO SKP      TRAP INSTR.
16        061277        .DUSR I.RST=061277        ;DOAC 0,CPU       I/O RESET
17
18        073301        .DUSR MMUL= DUCP 2,1      ;MUL              MULTIPLY
19        073101        .DUSR MDIV= DUCS 2,1      ;DIV              DIVIDE
```

```
10004 MNLGC
01                                  .LOC 0
02 000000 000007            DIRT
03 000001 100000            ,0
04                                  .LOC 45
05 000045 000147            EGGS
06                                  .LOC 60
07 000060 000046 TPLOC: 46
08 000061 000047 TPADR: 47
09 000062 100024 C24: 100024
10 000063 100034 C34: 100034
11 000064 100037 C37: 100037
12 000065 000001 K1: 1
13 000066 000002 K2: 2
14 000067 000003 K3: 3
15 000070 000004 K4: 4
16 000071 000006 K6: 6
17 000072 000010 K10: 10
18 000073 000020 K20: 20
19 000074 000040 K40: 40
20 000075 000100 K100: 100
21 000076 000200 K200: 200
22 000077 000377 K377: 377
23 000100 000400 K400: 400
24 000101 001000 K1000: 1000
25 000102 002000 K2000: 2000
26 000103 004000 K4000: 4000
27 000104 010000 K10K: 10000
28 000105 020000 K20K: 20000
29 000106 040000 K40K: 40000
30 000107 100000 K100K: 100000
31 000110 020400 KLDA.: 20400    ;= TO AN LDA 0,. OFF PAGE0
32 000111 000300 K300:   300
33 000112 100300 KD300:  #300
34 000113 025252 K25252: 25252
35 000114 052525 K52525: 52525
36 000115 125251 KCBE:   125251  ;EVEN # BITS
37 000116 052525 KCBO:   052525  ;ODD # BITS
38 000117 077777 K77777: 077777
39 000120 000005 K5:     5
40 000121 001400 KJRET:  JMP 0,3 ;JSR RETURNS TYPE JMP
41 000122 100001 KCOM:   COM 0,0,SKP
42 000123 000000 K0:     0
43 000124 000074 K60:    60.
44 000125 000000 KATSW:  0       ;-1 IF CAT/KITTEN STARTED
```

```
10005 MNLGC
01 00126 000074 TESTK:  060.
02 00127 000215 K215:   215
03 00130 000212 K212:   212
04 00131 000323 K323:   323
05 00132 000133 ADKTST: KTST
06 00133 000000 KTST:   0
07 00134 000000         0
08 00135 000000         0
09
10 00136 000320 K320:   320
11 00137 002300 JMP3K:  JMP @300
12 00140 000001 PKR00:  1
13 00141 000001 PKR01:  1
14 00142 004034 LLOOP:  LOOPL
15 00143 004030 SETUL:  SETLP
16 00144 063752 ARANG:  RANGN
17 00145 004662 IHMUL:  XHMUL
18 00146 004564 IHMD:   HMD
19
20 00147 000000 EGGS:   0       /AUTO RUN SW
21 00150 000000         0       /DEV CODE
22 00151 000000         0       /CAT SW
23 00152 000000         0       /# PASSES THIS RUN
24 00153 000000         0       /DTOS RETURN ADDRESS
25       000170         .LOC 170
26               /START HERE TO RUN W/O CAT/KITTEN
27 00170 102441 NOCAT:  SUBO 0,0,SKP
28 00171 102000 STCAT:  AUC 0,0
29 00172 040151         STA 0,EGGS+2    /SET CAT SWITCH
30 00173 002174         JMP .+1
31 00174 000470         RESTR
32       000200         .LOC 200
33 00200 002202 START:  JMP @BGNADR     /NORMAL START
34 00201 000000         0
35 00202 000470 BGNADR: RESTR
36
37               /LOCATIONS 277-301 RESERVED FOR TESTING
38       000277         .LOC 277
39 00277 000000         0
40 00300 000000         0
41 00301 000000         0
42
43       000470         .LOC 470
44               /RESTART AT THIS POINT
45 00470 102400 RESTR:  SUB 0,0
46 00471 040125         STA 0,KATSW
47 00472 101400         INC 0,0
48 00473 040140         STA 0,PKR00
49 00474 040141         STA 0,PKR01
50 00475 000403         JMP AAA
```

```
10006 MNLGC
01       000500         .LOC 500
02 00500 061277 AAA:    DOAC 0,CPU
03 00501 020147         LDA 0,EGGS
04 00502 101005         MOV 0,0,SNR     /DON'T HALT IF AUTO-RUN
05 00503 063077         HALT            /TO TEST HALT INSTRUCTION
06               /THIS SERIES WILL VERIFY THAT AN ALC
07               /INSTRUCTION WILL NOT SKIP/THEN SKIP UNCONDITIONALLY
08               /ERR HALT INDICATES EXTRANEOUS SKIP
09 00504 020066 A1A:    LDA 0,K2        /AC0 = 2
10 00505 072077         MSKO 2          /MASK OUT TTI INT.
11 00506 100000         COM 0,0         /COM SHD NOT CAUSE SKIP IR13,14,15=000
12 00507 100001         COM 0,0,SKP     /COM SKIP ALWAYS IR13,14,15=001
13 00510 063077         HALT
14
```

```
10007 MNLGC
01
02
03                ;TEST CARRY (CRY FLOP) AND SKIP LOGIC
04
05                ;A9A:
06 00511 102022           ADCZ 0,0,SZC      ;ZC,IR14,NOT IR15
07 00512 063077           HALT              ;ZERO INPUT TO CARRY FAILED
08
09 00513 102023           ADCZ 0,0,SNC      ;SNC NOT SEE CALC,IR15
10 00514 102002           ADC 0,0,SZC       ;ALSO TEST ZERO HOLD OF CRY
11 00515 063077           HALT              ;IF CRY=1 SEE NOT IR12 OR
12                ;A9B:
13 00516 102026           ADCZ 0,0,SEZ      ;CARRY=0 ZC,IR14,NOT IR15
14 00517 063077           HALT              ;INVOLVES SAME GATES AS SZC (?)
15
16 00520 102043           ADCO 0,0,SNC      ;TEST FOR TRUE CALC=IR15
17 00521 063077           HALT              ;1'S INPUT TO CRY CALC WAS NOT 1
18
19 00522 102042           ADCO 0,0,SZC      ;TEST FOR CALC,IR15 FALSE
20 00523 102003           ADC 0,0,SNC       ;ALSO TEST ONES HOLD OF CRY
21 00524 063077           HALT              ;IF CRY=0 SEE NOT IR12
22
23                ;A9C:
24 00525 102046           ADCO 0,0,SEZ      ;AGAIN TEST NOT ZC,IR14,NOT IR15
25 00526 102003           ADC 0,0,SNC       ;SAME GATES AS LAST TEST (SZC)
26 00527 063077           HALT              ;EXCEPT FOR ZR,IR13
27
28                ;OF TRANSITION TO 0 ON ZC
29 00530 102022 A9D:      ADCZ 0,0,SZC      ;SKIP ON ZC,IR14,NOT IR15
30 00531 063077           HALT              ;SEE CRY,IR11 THROUGH NOT SCI
31
32 00532 102040           ADCO 0,0          ;SET CRY=1
33 00533 102023           ADCZ 0,0,SNC      ;TRANSITION CRY TO 0
34 00534 102002           ADC 0,0,SZC       ;CHECK 0 REALLY GOT THERE
35 00535 063077           HALT              ;CRY=0 IS SNC FAILED
36
37                ;CARRY=0 COMING INTO NEXT TEST CHECK NOT CRY,NOT IR10
38                ;A9E:
39 00536 102023           ADCZ 0,0,SNC      ;ALSO NOT (CRY,IR11)
40 00537 102002           ADC 0,0,SZC       ;CRY SHD HAVE STAYED 0
41 00540 063077           HALT              ;ALSO ZC AND LOAD CARRY USED
```

```
10008 MNLGC
01
02
03                ;TEST CARRY TO TRANSITION FROM 0 TO 1
04                ;A9F:
05 00541 102020           ADCZ 0,0,         ;SET CRY=1
06 00542 102042           ADCO 0,0,SZC      ;MAKE IT=1 AGAIN NOT CRY,IR10
07 00543 102003           ADC 0,0,SNC       ;DID 1 REALLY GET TO CRY
08 00544 063077           HALT              ;IF CRY=1 SZC FAILED
09
10                ;TEST COMPLIMENT OF CARRY IR11,IR10
11                ;A9G:
12 00545 102020           ADCZ 0,0          ;SET CRY=0
13 00546 102002           ADCC 0,0,SZC      ;TRANS CRY 0 TO 1 (SZC NOT)
14 00547 102003           ADC 0,0,SNC       ;CRY SHD=1
15 00550 063077           HALT              ;CRY=0 SEE CALC,LOAD CARRY
16
17                ;A9H:
18 00551 102040           ADCO 0,0          ;SET CRY=1
19 00552 102003           ADCC 0,0,SNC      ;ZC SHD BE TRUE (NOT SNC)
20 00553 102002           ADC 0,0,SZC       ;CARRY SHD REALLY=0
21 00554 063077           HALT              ;CRY=1 SEE ZC AND LOAD CARRY
22
23                ;TEST CARRY NO LOAD IR12=1 TO PREVENT CARRY CHANGE
24
25                ;A9I:
26 00555 102020           ADCZ 0,0
27 00556 102052           ADCO# 0,0,SZC     ;NO LOAD CRY IR12=1
28 00557 102002           ADC 0,0,SZC
29 00560 063077           HALT              ;CALC,IR12
30
31                ;A9J:
32 00561 102040           ADCO 0,0
33 00562 102033           ADCZ# 0,0,SNC     ;CRY SHD STAY=1 IR12=1
34 00563 102003           ADC 0,0,SNC
35 00564 063077           HALT              ;ZC,NOT LOAD CARRY
```

```
10009 MNLGC
01
02
03                      ;TEST FOR ADC TO SET AC0=MOSTLY 1'S AND SNR TO SKIP
04                      ;START BUILDING INSTRUCTIONS TO CREATE CONSTANTS
05                      ;VERY LITTLE LOGIC IS VERIFIED YET
06                  ;A20:
07 00565 102005         ADC 0,0,SNR         ;ANY RESULT IN AC0 SHD CAUSE SKP
08 00566 063077         HALT                ;AC0 ANYTHING BUT 0 IS SNR FAILED
09
10                    ;SZR SHOULD NOT SKIP WHEN AC0 NOT=0
11                  ;A21:
12 00567 102004         ADC 0,0,SZR         ;TEST A2 INDICATES AC0 NOT=0
13 00570 102005         ADC 0,0,SNR         ;AS RESULT OF AN ADC
14 00571 063077         HALT                ;SZR SKIPPED IF AC0 NOT=0
15
16                    ;ATTEMPT TO GENERATE AN ALL 0'S CONSTANT VIA ADC+COM
17                    ;ALSO TESTS SZR TO SKIP IN GROSS CASE
18                  ;A22:
19 00572 102000         ADC 0,0             ;ADC MAY NOT YET=-1
20 00573 100004         COM 0,0,SZR         ;OR COM MAY ALSO FAIL
21                  ; RESULT DOES NOT=0
22 00574 063077             HALT            ;RESULT IN AC0 SHOULD HELP TO
23                    ;AC0=0 IS SZR FAILED TO SKIP IR15=0 IN SKIP LOGIC
24
25                    ;TEST ZERO CARRY SKIP FROM COM 0,0
26                  ;A23:
27 00575 102020         ADCZ 0,0            ;0 TO CARRY=1 TO AC0
28 00576 100002         COM 0,0,SZC         ;CARRY SHD STILL=0
29 00577 063077         HALT
30
31                    ;TEST SKIP EITHER ZERO WITH BOTH AC AND CARRY=0
32
33                  ;A24:
34 00600 102020         ADCZ 0,0
35 00601 100006         COM 0,0,SEZ         ;BOTH RESULT AND CARRY=0
36 00602 063077         HALT                ;SEZ FAILED BOTH=0
37
38                    ;TEST SKIP EITHER ZERO WITH AC=0 AND CARRY=1
39
40                  ;A25:
41 00603 102040         ADCO 0,0
42 00604 100006         COM 0,0,SEZ         ;RES=0 BUT CARRY=1
43 00605 063077         HALT                ;SEE ZR,IR13,NOT IR15
```

```
10010 MNLGC
01
02                    ;THE NEXT SERIES OF TESTS VERIFY
03                    ;THAT REFERENCING ONE AC DOES NOT DISTURB THE OTHERS
04                      .MACRO ACITS        ;AC ISOLATION TEST^1
05                  ;ACI^1:
06                      ADC ^2,^2
07                      COM ^2,^2           ;SET AC^2 TO 0
08                      ADC ^3,^3           ;SET AC^3 TO -1
09                      ADC ^4,^4           ;SET AC^4 TO -1
10                      ADC ^5,^5           ;SET AC^5 TO -1
11                      MOV ^2,^2,SZR       ;TEST AC^2 TO STILL=0
12                      HALT                ;AC^3 DESTINATION DISTURBED AC^2
13                  %
14
15                      ACITS   00      0       1       2       3
16                  ;ACI00:
17 00606 102000         ADC 0,0
18 00607 100000         COM 0,0 ;SET AC0 TO 0
19 00610 126000         ADC 1,1 ;SET AC1 TO -1
20 00611 152000         ADC 2,2 ;SET AC2 TO -1
21 00612 176000         ADC 3,3 ;SET AC3 TO -1
22 00613 101004         MOV 0,0,SZR         ;TEST AC0 TO STILL=0
23 00614 063077         HALT                ;AC1 DESTINATION DISTURBED AC0
24                      ACITS   01      1       2       3       0
25                  ;ACI01:
26 00615 126000         ADC 1,1
27 00616 124000         COM 1,1 ;SET AC1 TO 0
28 00617 152000         ADC 2,2 ;SET AC2 TO -1
29 00620 176000         ADC 3,3 ;SET AC3 TO -1
30 00621 102000         ADC 0,0 ;SET AC0 TO -1
31 00622 125004         MOV 1,1,SZR         ;TEST AC1 TO STILL=0
32 00623 063077         HALT                ;AC2 DESTINATION DISTURBED AC1
33                      ACITS   02      2       3       0       1
34                  ;ACI02:
35 00624 152000         ADC 2,2
36 00625 150000         COM 2,2 ;SET AC2 TO 0
37 00626 176000         ADC 3,3 ;SET AC3 TO -1
38 00627 102000         ADC 0,0 ;SET AC0 TO -1
39 00630 126000         ADC 1,1 ;SET AC1 TO -1
40 00631 151004         MOV 2,2,SZR         ;TEST AC2 TO STILL=0
41 00632 063077         HALT                ;AC3 DESTINATION DISTURBED AC2
42                      ACITS   03      3       0       1       2
43                  ;ACI03:
44 00633 176000         ADC 3,3
45 00634 174000         COM 3,3 ;SET AC3 TO 0
46 00635 102000         ADC 0,0 ;SET AC0 TO -1
47 00636 126000         ADC 1,1 ;SET AC1 TO -1
48 00637 152000         ADC 2,2 ;SET AC2 TO -1
49 00640 175004         MOV 3,3,SZR         ;TEST AC3 TO STILL=0
50 00641 063077         HALT                ;AC0 DESTINATION DISTURBED AC3
```

```
10011 MNLGC
01
02
03                ;THE FOLLOWING TESTS INSURE 0'S ISOLATION
04                ;OF AC TO AC
05
06                      .MACRO ACIT2    ;0'S ISOLATION TEST
07                ;ACIA1:
08                      ADC A2,A2       ;SET ACA2=-1
09                      COM A2,A3       ;SET 0'S TO ACA3
10                      COM A2,A4       ;SET 0'S TO ACA4
11                      COM A2,A5       ;SET 0'S TO ACA5
12                      COM A2,A2,SZR   ;ACA2 SHD STILL=-1
13                      HALT            ;0'S TO ACA3 DISTURBED ACA2
14                %
15                      ACIT2   04      0       1       2       3
16                ;ACI04:
17 00642 102000         ADC 0,0 ;SET AC0=-1
18 00643 104000         COM 0,1 ;SET 0'S TO AC1
19 00644 110000         COM 0,2 ;SET 0'S TO AC2
20 00645 114000         COM 0,3 ;SET 0'S TO AC3
21 00646 100004         COM 0,0,SZR     ;AC0 SHD STILL=-1
22 00647 063077         HALT            ;0'S TO AC1 DISTURBED AC0
23                      ACIT2   05      1       2       3       0
24                ;ACI05:
25 00650 126000         ADC 1,1 ;SET AC1=-1
26 00651 130000         COM 1,2 ;SET 0'S TO AC2
27 00652 134000         COM 1,3 ;SET 0'S TO AC3
28 00653 120000         COM 1,0 ;SET 0'S TO AC0
29 00654 124004         COM 1,1,SZR     ;AC1 SHD STILL=-1
30 00655 063077         HALT            ;0'S TO AC2 DISTURBED AC1
31                      ACIT2   06      2       3       0       1
32                ;ACI06:
33 00656 152000         ADC 2,2 ;SET AC2=-1
34 00657 154000         COM 2,3 ;SET 0'S TO AC3
35 00660 140000         COM 2,0 ;SET 0'S TO AC0
36 00661 144000         COM 2,1 ;SET 0'S TO AC1
37 00662 150004         COM 2,2,SZR     ;AC2 SHD STILL=-1
38 00663 063077         HALT            ;0'S TO AC3 DISTURBED AC2
39                      ACIT2   07      3       0       1       2
40                ;ACI07:
41 00664 176000         ADC 3,3 ;SET AC3=-1
42 00665 160000         COM 3,0 ;SET 0'S TO AC0
43 00666 164000         COM 3,1 ;SET 0'S TO AC1
44 00667 170000         COM 3,2 ;SET 0'S TO AC2
45 00670 174004         COM 3,3,SZR     ;AC3 SHD STILL=-1
46 00671 063077         HALT            ;0'S TO AC0 DISTURBED AC3
47
48
49
```

```
10012 MNLGC
01                ;AT THIS POINT IN THE TEST THE FOLLOWING
02                ;ITEMS HAVE BEEN VERIFIED
03                ;1. NONE OF THE ALC INSTRUCTIONS SKIP EXTRANEOUSLY
04                ;2. CRY CAN BE SET TO 1 OR 0 AND CRY SKIPS
05                      ;FUNCTION CORRECTLY
06                ;3. A CONSTANT OTHER THAN 0 CAN BE GENERATED
07                      ;BY AN ADC ANY AC TO ITSELF
08                ;4. A CONSTANT THAT AT LEAST APPEARS TO=0 CAN
09                      ;BE GENERATED BY AN ADC+COM ANY AC TO ITSELF
10                ;5. ANY AC MAY BE REFERENCED BY EITHER
11                      ;AN ADC OR COM WITHOUT DISTURBING THE OTHERS
12                ;6. SNR SKIPS ON =1 DOES NOT SKIP ON 0
13                ;7. SZR SKIPS ON 0 DOES NOT SKIP ON =1
14                ;8. NO TRANSFER (IR 12=1) INHIBITS CARRY CHANGE
15
16                ;TEST LEFT SHIFT OF A 1 INTO 0 CRY
17                ;A40:
18 00672 102020         ADCZ 0,0
19 00673 101102         MOVL 0,0,SZC    ;MAKE LEFT SHIFT CRY IN=1
20 00674 101003         MOV 0,0,SNC     ;TEST FOR CRY REALLY=1
21 00675 063077         HALT            ;LEFT SHIFT IR9 FAILED
22                ;TEST LEFT SHIFT OF A 0 INTO A CRY OF 1
23
24                ;A41:
25 00676 100103         COML 0,0,SNC    ;CRY INPUT (ZC)
26 00677 101002         MOV 0,0,SZC     ;DID 0 REALLY GET TO CRY
27 00700 063077         HALT            ;LEFT SHIFT (IR9) 0 INTO CRY
28
29
```

```
10013 MNLOC
01
02                  ;TEST FOR NO BITS TO PICK UP ON SHIFT LEFT
03
04                ;A42:
05 00701 102020           ADCZ 0,0          ;AC0=-1  CRY=0
06 00702 100105           COML 0,0,SNR      ;TEST RESULT LEVELS=0
07 00703 101004           MOV 0,0,SZR       ;AND ACTUAL RESULT=0
08 00704 063077           HALT              ;AC0 L SHOULD=0
09                  ;TEST THE TRANSFER OF A CRY=1 INTO BIT 15 AC 0
10                ;A43:
11 00705 102040           ADCO 0,0
12 00706 100105           COML 0,0,SNR      ;CRY SHOULD=1 TO AC 15
13 00707 063077           HALT              ;IF AC0=0 SEE ALU 15
14                  ;IN ABOVE TEST ALU LEVEL INPUT IS NOT SCI (FALSE)
15                  ;TEST BIT 15=1 STRAIGHT TRANSFER THROUGH
16
17                ;A44:
18 00710 102040           ADCO 0,0
19 00711 100104           COML 0,0,SZR      ;IN CASE LEVEL NOT SUM 15 FAILS
20 00712 101005           MOV 0,0,SNR       ;AC0=+1 RESULT IS NON ZERO
21 00713 063077           HALT
22                  ;OR "NOT SUM 15" FALSE INTO ZR AND'S IN SKP LOGIC
23
24                  ;TEST RIGHT SHIFT LOGIC INTO CRY
25                  ;TEST ONES SHIFT INTO A 0 CRY
26                  ;TEST OF IR8=1 ENABLES RIGHT SHIFT INPUTS
27                ;A45:
28 00714 102223           ADCZR 0,0,SNC     ;TEST INPUT TO CRY=1
29 00715 063077           HALT
30
31                ;A46:
32 00716 102222           ADCZR 0,0,SZC     ;INPUT TO CRY=1
33 00717 100003           COM 0,0,SNC       ;CRY RIGHT SHD STILL=1
34 00720 063077           HALT
35                  ;TEST RIGHT 0 INPUT TO CRY=1
36
37                ;A47:
38 00721 102040           ADCO 0,0
39 00722 100203           COMR 0,0,SNC
40 00723 100002           COM 0,0,SZC
41 00724 063077           HALT              ;CRY SHOULD=0
42                  ;
```

```
10014 MNLOC
01
02                  ;TEST FOR NO BITS TO PICK UP ON RIGHT SHIFT
03
04                ;A48:
05 00725 102020           ADCZ 0,0          ;(AC0)=-1 CRY=0
06 00726 100205           COMR 0,0,SNR      ;SHIFT 0'S RIGHT
07 00727 101004           MOV 0,0,SZR       ;RESULT SHOULD REMAIN=0
08 00730 063077           HALT              ;RIGHT SHIFT ALL 0'S FAILED
09                  ;EXAMINE AC0 TO DETERMINE BITS PICKED SHIFT RIGHT
10                  ;SHIFT CRY=1 RIGHT INTO BIT 0
11                  ;ALSO TEST BIT 0=1 INTO NOT ZR
12                ;A49:
13 00731 102040           ADCO 0,0          ;CRY=1 AC0=-1
14 00732 100204           COMR 0,0,SZR      ;RIGHT SHIFT 0'S CRY=1 TO BIT 0
15 00733 101205           MOVR 0,0,SNR      ;TEST RESULT TO REALLY HOLD
16 00734 063077           HALT              ;RIGHT SHIFT CRY=1 FAILED
17                  ;OR NOT SUM 0 INTO ZR AND GATES IN SKIP LOGIC (AC0=100000)
18
19                  ;TEST RIGHT SHIFT OF AC0=0'S INTO AC1
20                  ;START BUILDING DOUBLE REGISTERS FOR TEST USAGE
21
22                ;A50:
23 00735 102000           ADC 0,0
24 00736 125020           ADCZ 1,1
25 00737 104200           COMR 0,1
26 00740 125004           MOV 1,1,SZR
27 00741 063077           HALT              ;RIGHT SHIFT ALL 0'S TO AC1
28
29                  ;TRANSFER CRY=1 INTO AC1 BIT 0 SHIFT RIGHT
30                ;A51:
31 00742 102000           ADC 0,0           ;AC0=-1
32 00743 104040           COMO 0,1          ;AC1=0  CRY=1
33 00744 104200           COMR 0,1          ;RIGHT SHIFT NOT(0) TO AC1
34 00745 125005           MOV 1,1,SNR       ;RESULT SHD=NOT 0 BIT 0=1
35 00746 063077           HALT              ;AC1 SHD=100000
36                  ;ABOVE TESTS WERE TO VERIFY TRANSFER OF AC0 TO AC OCCURS
37                  ;RIGHT SHIFT OR CRY=1 TO BIT 0 WAS PREV. VERIFIED
```

```
10015 MNLGC
01                      ;SETUP NEXT SERIES OF RIGHT SHIFT TESTS
02 000747 102040        ADCO 0,0
03 000750 100200        COMR 0,0
04 000751 101005        MOV 0,0,SNR
05 000752 063077        HALT                    ;BIT 0 SETUP FAILED
06
07 000753 101200        MOVR 0,0
08 000754 101200        MOVR 0,0
09 000755 101200        MOVR 0,0
10 000756 101200        MOVR 0,0
11 000757 101200        MOVR 0,0
12 000760 101200        MOVR 0,0
13 000761 101200        MOVR 0,0
14 000762 101200        MOVR 0,0
15 000763 101200        MOVR 0,0
16 000764 024075        LDA 1,K100
17 000765 100414        SUB# 0,1,SZR            ;CHECK INTERMEDIATE RESULT
18 000766 063077        HALT                    ;AC0 == AC1 ?
19 000767 101200        MOVR 0,0
20 000770 101200        MOVR 0,0
21 000771 101200        MOVR 0,0
22 000772 101200        MOVR 0,0
23 000773 101200        MOVR 0,0
24 000774 101200        MOVR 0,0
25 000775 105205 ASR15: MOVR 0,1,SNR            ;TEST BIT 15=1 R TO CRY
26 000776 125004        MOV 1,1,SZR             ;AC1 SHD=0'S
27 000777 063077        HALT
28 001000 125003        MOV 1,1,SNC             ;AND CRY SHD=1
29 001001 063077        HALT
```

```
10016 MNLGC
01                      ;LEFT SHIFT SINGLE BIT TESTS
02                      ;SET UP A 1 IN BIT 15
03
04 001002 102040        ADCO 0,0
05 001003 101104        COML 0,0,SZR
06 001004 101005        MOV 0,0,SNR
07 001005 063077        HALT                    ;AC0 SHD=1 SETUP FAILED
08
09 001006 101100        MOVL 0,0
10 001007 101100        MOVL 0,0
11 001010 101100        MOVL 0,0
12 001011 101100        MOVL 0,0
13 001012 101100        MOVL 0,0
14 001013 101100        MOVL 0,0
15 001014 101100        MOVL 0,0
16 001015 101100        MOVL 0,0
17 001016 024100        LDA 1,K400
18 001017 122414        SUB# 1,0,SZR            ;CHECK INTERMEDIATE RESULT
19 001020 063077        HALT                    ;AC0 = AC1?
20
21 001021 101100        MOVL 0,0
22 001022 101100        MOVL 0,0
23 001023 101100        MOVL 0,0
24 001024 101100        MOVL 0,0
25 001025 101100        MOVL 0,0
26 001026 101100        MOVL 0,0
27 001027 101100        MOVL 0,0
28 001030 105105 ASL15: MOVL 0,1,SNR            ;AC0=100000
29 001031 125004        MOV 1,1,SZR             ;RESULT LEFT SHD=0'S
30 001032 063077        HALT                    ;PICKED UP EXTRA BITS LEFT
31 001033 125003        MOV 1,1,SNC
32 001034 063077        HALT                    ;LOST CARRY LAST LEFT SHIFT
```

```
10017 MNLGC
01                      ;SET UP SERIES OF RIGHT SHIFT TESTS
02                      ;BY SETTING AC0 TO 077777
03 01035 102000                 ADC 0,0
04 01036 100240                 COMOR 0,0               ;SEQUENCE MUST LIKELY TO
05 01037 100000                 COM 0,0                 ;SET AC0=077777
06 01040 113005                 COM 0,2,SNR
07 01041 063077                 HALT                    ;SETUP FAILED CRY=0 TO BIT 0
08 01042 105000                 MOV 0,1
09 01043 150000                 COM 2,2                 ;RETEST INSTRUCTION
10 01044 132000                 ADC 1,2                 ;CHECK SEQUENCE
11 01045 150004                 COM 2,2,SZR             ;JUST TO MAKE SURE IT WORKS
12 01046 063077                 HALT                    ;COMPARE OF AC0=077777 FAILED
13
14 01047 101240                 MOVOR 0,0
15 01050 101240                 MOVOR 0,0
16 01051 101240                 MOVOR 0,0
17 01052 101240                 MOVOR 0,0
18 01053 101240                 MOVOR 0,0
19 01054 101240                 MOVOR 0,0
20 01055 101240                 MOVOR 0,0
21 01056 101240                 MOVOR 0,0
22 01057 101240                 MOVOR 0,0
23 01060 101240                 MOVOR 0,0
24 01061 101240                 MOVOR 0,0
25 01062 101240                 MOVOR 0,0
26 01063 101240                 MOVOR 0,0
27 01064 101240                 MOVOR 0,0
28 01065 101240                 MOVOR 0,0
29
30                      ;ASH31:
31 01066 105240                 MOVOR 0,1               ;TEST 177776 TO =1
32 01067 130004                 COM 1,2,SZR             ;ALSO RETEST ABOVE SEQ
33 01070 063077                 HALT
34 01071 101002                 MOV 0,0,SZC
35 01072 063077                 HALT                    ;CRY SHD=0 FROM LAST MOVOR
36
37                      ;SETUP SERIES OF LEFT SHIFT TESTS SET AC0=177776
38 01073 102000                 ADC 0,0                 ;AC0=-1
39 01074 100140                 COMOL 0,0               ;SHD NOW=+1
40 01075 100000                 COM 0,0
41 01076 104224                 COMZR 0,1,SZR
42 01077 063077                 HALT                    ;LEFT SHIFT SETUP FAILED
43 01100 125003                 MOV 1,1,SNC
44 01101 063077                 HALT                    ;LEFT SHIFT SETUP FAILED
```

```
10018 MNLGC
01                      ;LEFT SHIFT SINGLE 0 BIT TESTS
02 01102 101140                 MOVOL 0,0
03 01103 101140                 MOVOL 0,0
04 01104 101140                 MOVOL 0,0
05 01105 101140                 MOVOL 0,0
06 01106 101140                 MOVOL 0,0
07 01107 101140                 MOVOL 0,0
08 01110 101140                 MOVOL 0,0
09 01111 101140                 MOVOL 0,0
10 01112 101140                 MOVOL 0,0
11 01113 101140                 MOVOL 0,0
12 01114 101140                 MOVOL 0,0
13 01115 101140                 MOVOL 0,0
14 01116 101140                 MOVOL 0,0
15 01117 101140                 MOVOL 0,0
16 01120 101140                 MOVOL 0,0
17 01121 105140                 MOVOL 0,1               ;SHD RESULT IN AC1=-1
18 01122 130004                 COM 1,2,SZR             ;TEST FOR AC2 RESULT=0
19 01123 063077                 HALT                    ;COULD HAVE FAILED L16 TO L30
20 01124 151002                 MOV 2,2,SZC             ;CRY SHD=0 FROM BIT 0
21 01125 063077                 HALT                    ;BIT 0 TO CRY FAILED
22
23
24                      ;TEST ADD OF ALL 0'S TO GENERATE NO CARRIES
25                      ;ANC001:
26 01126 102000                 ADC 0,0
27 01127 100000                 COM 0,0                 ;SETS AC0=0
28 01130 103004                 ADD 0,0,SZR             ;RESULT OF ADD SHD STILL=0
29 01131 063077                 HALT                    ;ADD 0+0 GENERATED A CARRY
30 01132 101002                 MOV 0,0,SZC             ;ABOVE ADD SHD LVE CRY=0
31 01133 063077                 HALT                    ;INTO CRY SEE CARRY OUT
32
33
34                      ;TEST ADD OF ALL 1'S TO GENERATE NO CARRIES,DEST.=0
35 01134 102000                 ADC 0,0                 ;AC0=-1
36 01135 105000                 MOV 0,1                 ;AC1=-1
37 01136 100000                 COM 0,0                 ;AC0=0
38 01137 123000                 ADD 1,0                 ;ADD AC1 TO AC0
39 01140 101002                 MOV 0,0,SZC             ;CARRY SHD BE =0
40 01141 063077                 HALT
```

```
10019 MNLGC
01
02                ;SINGLE BIT CARRY TESTS
03                  ;CONSTANTS ARE SET UP BY ALREADY TESTED SHIFT
04
05                        .MACRO ADDT0
06                ;BIT A2 ADDED TO ITSELF,
07                ;CARRY INTO A3,AC0 GOES FROM A4 T0 A5
08                ;AC0A1:
09                        ADD 0,0
10                %
11                  ;SET UP BIT 15 FOR ADD TESTS
12 01142 102000           ADC 0,0
13 01143 100145           COMOL 0,0,SNR
14 01144 063077           HALT              ;AC0 SHD=+1
15
16                        ADDT0 00,15,14,1,2
17                ;BIT 15 ADDED TO ITSELF,
18                ;CARRY INTO 14,AC0 GOES FROM 1 T0 2
19                ;AC00:
20 01145 103000           ADD 0,0
21                        ADDT0 01,14,13,2,4
22                ;BIT 14 ADDED TO ITSELF,
23                ;CARRY INTO 13,AC0 GOES FROM 2 T0 4
24                ;AC01:
25 01146 103000           ADD 0,0
26                        ADDT0 02,13,12,4,10
27                ;BIT 13 ADDED TO ITSELF,
28                ;CARRY INTO 12,AC0 GOES FROM 4 T0 10
29                ;AC02:
30 01147 103000           ADD 0,0
31                        ADDT0 03,12,11,10,20
32                ;BIT 12 ADDED TO ITSELF,
33                ;CARRY INTO 11,AC0 GOES FROM 10 T0 20
34                ;AC03:
35 01150 103000           ADD 0,0
36                        ADDT0 04,11,10,20,40
37                ;BIT 11 ADDED TO ITSELF,
38                ;CARRY INTO 10,AC0 GOES FROM 20 T0 40
39                ;AC04:
40 01151 103000           ADD 0,0
41                        ADDT0 05,10,9,40,100
42                ;BIT 10 ADDED TO ITSELF,
43                ;CARRY INTO 9,AC0 GOES FROM 40 T0 100
44                ;AC05:
45 01152 103000           ADD 0,0
46                        ADDT0 06,9,8,100,200
47                ;BIT 9 ADDED TO ITSELF,
48                ;CARRY INTO 8,AC0 GOES FROM 100 T0 200
49                ;AC06:
50 01153 103000           ADD 0,0
51                        ADDT0 07,8,7,200,400
52                ;BIT 8 ADDED TO ITSELF,
53                ;CARRY INTO 7,AC0 GOES FROM 200 T0 400
54                ;AC07:
55 01154 103000           ADD 0,0
56 01155 024100           LDA  1,K400
57 01156 176414           SUBM 0,1,SZR      ;CHECK INTERMEDIATE RESULT
58 01157 063077           HALT              ;AC0 NOT 400
59                        ADDT0 08,7,6,400,1000
60                ;BIT 7 ADDED TO ITSELF,
```

```
 0020 MNLGC
01                ;CARRY INTO 6,AC0 GOES FROM 400 T0 1000
02                ;AC08:
03 01160 103000           ADD 0,0
04                        ADDT0 09,6,5,1000,2000
05                ;BIT 6 ADDED TO ITSELF,
06                ;CARRY INTO 5,AC0 GOES FROM 1000 T0 2000
07                ;AC09:
08 01161 103000           ADD 0,0
09                        ADDT0 10,5,4,2000,4000
10                ;BIT 5 ADDED TO ITSELF,
11                ;CARRY INTO 4,AC0 GOES FROM 2000 T0 4000
12                ;AC10:
13 01162 103000           ADD 0,0
14                        ADDT0 11,4,3,4000,10000
15                ;BIT 4 ADDED TO ITSELF,
16                ;CARRY INTO 3,AC0 GOES FROM 4000 T0 10000
17                ;AC11:
18 01163 103000           ADD 0,0
19                        ADDT0 12,3,2,10000,20000
20                ;BIT 3 ADDED TO ITSELF,
21                ;CARRY INTO 2,AC0 GOES FROM 10000 T0 20000
22                ;AC12:
23 01164 103000           ADD 0,0
24                        ADDT0 13,2,1,20000,40000
25                ;BIT 2 ADDED TO ITSELF,
26                ;CARRY INTO 1,AC0 GOES FROM 20000 T0 40000
27                ;AC13:
28 01165 103000           ADD 0,0
29                        ADDT0 14,1,0,40000,100000
30                ;BIT 1 ADDED TO ITSELF,
31                ;CARRY INTO 0,AC0 GOES FROM 40000 T0 100000
32                ;AC14:
33 01166 103000           ADD 0,0
34
35 01167 101002           MOV 0,0,SZC
36 01170 063077           HALT              ;CARRY SHD BE ZERO NOW
37 01171 101103           MOVL 0,0,SNC      ;LOOK AT BIT 0
38 01172 063077           HALT              ;SHOULD HAVE BEEN A 1
39 01173 101004           MOV 0,0,SZR       ;ALL BITS SHD BE 0'S NOW
40 01174 063077           HALT
```

```
10021 MNLGC
01
                    ;AND00:
02 01175 102000             ADC 0,0             ;SET AC0=-1
03 01176 103405             AND 0,0,SNR         ;AC0=-1
04 01177 063077             HALT
05 01200 104004             COM 0,1,SZR         ;AC1 SHD = 0,AC0 = -1
06 01201 063077             HALT
07 01202 107404             AND 1,1,SZR         ;AC1 SHD = 0
08 01203 063077             HALT
09 01204 107404             AND 0,1,SZR         ;AC1 SHD = 0
10 01205 063077             HALT
11 01206 123404             AND 1,0,SZR         ;AC0,AC1 NOW = 0
12 01207 063077             HALT                ;ERROR STOP
13
14                    ;DEFINE BIT TEST MACRO FOR AND INSTRUCTION
15                          .MACRO ANDTS
16                  ;AND#1:
17                          MOV 0,1             ;AC0=#3
18                          AND 0,1,SNR         ;BIT #2 SHD REMAIN=1
19                          HALT
20                          MOV 1,2
21                          ADC 0,2
22                          COM 2,2,SZR         ;TEST FOR EXTRA BITS
23                          HALT                ;MORE THAN 1 BIT IN AND OF #3
24                    ;NOW TEST AND OF COMPLIMENTS
25                  ;AN#1A:
26                          COM 0,1
27                          AND 0,1,SZR
28                          HALT                ;AND OF #3 AND ITS COM FAILED
29                    ;TEST AND OF COMPLIMENTS WITH DEST=#3 AND SRC=COM
30                  ;AN#1B:
31                          MOV 0,1
32                          COM 1,2
33                          AND 2,1,SZR
34                          HALT                ;AND OF #3 AND ITS COM FAILED
35                    ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
36                          MOVZL 0,0           ;SET UP NEXT TEST
37                  %
38
39
40                    ;SET UP AC0=1 FOR FIRST AND TEST
41
42 01210 102000             ADC 0,0
43 01211 100145             COMOL 0,0,SNR
44 01212 063077             HALT
```

```
10022 MNLGC
01
02                          ANDTS 04,15,1
03                  ;AND04:
04 01213 105000             MOV 0,1             ;AC0=1
05 01214 107405             AND 0,1,SNR         ;BIT 15 SHD REMAIN=1
06 01215 063077             HALT
07 01216 131000             MOV 1,2
08 01217 112000             ADC 0,2
09 01220 150004             COM 2,2,SZR         ;TEST FOR EXTRA BITS
10 01221 063077             HALT                ;MORE THAN 1 BIT IN AND OF 1
11                    ;NOW TEST AND OF COMPLIMENTS
12                  ;AN04A:
13 01222 104000             COM 0,1
14 01223 107404             AND 0,1,SZR
15 01224 063077             HALT                ;AND OF 1 AND ITS COM FAILED
16                    ;TEST AND OF COMPLIMENTS WITH DEST=1 AND SRC=COM
17                  ;AN04B:
18 01225 105000             MOV 0,1
19 01226 130000             COM 1,2
20 01227 147404             AND 2,1,SZR
21 01230 063077             HALT                ;AND OF 1 AND ITS COM FAILED
22                    ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
23 01231 101120             MOVZL 0,0           ;SET UP NEXT TEST
24                          ANDTS 05,14,2
25                  ;AND05:
26 01232 105000             MOV 0,1             ;AC0=2
27 01233 107405             AND 0,1,SNR         ;BIT 14 SHD REMAIN=1
28 01234 063077             HALT
29 01235 131000             MOV 1,2
30 01236 112000             ADC 0,2
31 01237 150004             COM 2,2,SZR         ;TEST FOR EXTRA BITS
32 01240 063077             HALT                ;MORE THAN 1 BIT IN AND OF 2
33                    ;NOW TEST AND OF COMPLIMENTS
34                  ;AN05A:
35 01241 104000             COM 0,1
36 01242 107404             AND 0,1,SZR
37 01243 063077             HALT                ;AND OF 2 AND ITS COM FAILED
38                    ;TEST AND OF COMPLIMENTS WITH DEST=2 AND SRC=COM
39                  ;AN05B:
40 01244 105000             MOV 0,1
41 01245 130000             COM 1,2
42 01246 147404             AND 2,1,SZR
43 01247 063077             HALT                ;AND OF 2 AND ITS COM FAILED
44                    ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
45 01250 101120             MOVZL 0,0           ;SET UP NEXT TEST
46                          ANDTS 06,13,4
47                  ;AND06:
48 01251 105000             MOV 0,1             ;AC0=4
49 01252 107405             AND 0,1,SNR         ;BIT 13 SHD REMAIN=1
50 01253 063077             HALT
51 01254 131000             MOV 1,2
52 01255 112000             ADC 0,2
53 01256 150004             COM 2,2,SZR         ;TEST FOR EXTRA BITS
54 01257 063077             HALT                ;MORE THAN 1 BIT IN AND OF 4
55                    ;NOW TEST AND OF COMPLIMENTS
56                  ;AN06A:
57 01260 104000             COM 0,1
58 01261 107404             AND 0,1,SZR
59 01262 063077             HALT                ;AND OF 4 AND ITS COM FAILED
60                    ;TEST AND OF COMPLIMENTS WITH DEST=4 AND SRC=COM
```

```
0023 MNLGC
01                      ;AN06B:
02 01263 105000                 MOV 0,1
03 01264 130000                 COM 1,2
04 01265 147404                 AND 2,1,SZR
05 01266 063077                 HALT                    ;AND OF 4 AND ITS COM FAILED
06                        ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
07 01267 101120                 MOVZL 0,0               ;SET UP NEXT TEST
08                              ANDTS 07,12,10
09                      ;AND07:
10 01270 105000                 MOV 0,1                 ;AC0=10
11 01271 107405                 AND 0,1,SNR             ;BIT 12 SHD REMAIN=1
12 01272 063077                 HALT
13 01273 131000                 MOV 1,2
14 01274 112000                 ADC 0,2
15 01275 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
16 01276 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 10
17                        ;NOW TEST AND OF COMPLIMENTS
18                      ;AN07A:
19 01277 104000                 COM 0,1
20 01300 147404                 AND 0,1,SZR
21 01301 063077                 HALT                    ;AND OF 10 AND ITS COM FAILED
22                      ;TEST AND OF COMPLIMENTS WITH DEST=10 AND SRC=COM
23                      ;AN07B:
24 01302 105000                 MOV 0,1
25 01303 130000                 COM 1,2
26 01304 147404                 AND 2,1,SZR
27 01305 063077                 HALT                    ;AND OF 10 AND ITS COM FAILED
28                        ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
29 01306 101120                 MOVZL 0,0               ;SET UP NEXT TEST
30                              ANDTS 08,11,20
31                      ;AND08:
32 01307 105000                 MOV 0,1                 ;AC0=20
33 01310 107405                 AND 0,1,SNR             ;BIT 11 SHD REMAIN=1
34 01311 063077                 HALT
35 01312 131000                 MOV 1,2
36 01313 112000                 ADC 0,2
37 01314 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
38 01315 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 20
39                        ;NOW TEST AND OF COMPLIMENTS
40                      ;AN08A:
41 01316 104000                 COM 0,1
42 01317 107404                 AND 0,1,SZR
43 01320 063077                 HALT                    ;AND OF 20 AND ITS COM FAILED
44                      ;TEST AND OF COMPLIMENTS WITH DEST=20 AND SRC=COM
45                      ;AN08B:
46 01321 105000                 MOV 0,1
47 01322 130000                 COM 1,2
48 01323 147404                 AND 2,1,SZR
49 01324 063077                 HALT                    ;AND OF 20 AND ITS COM FAILED
50                        ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
51 01325 101120                 MOVZL 0,0               ;SET UP NEXT TEST
52                              ANDTS 09,10,40
53                      ;AND09:
54 01326 105000                 MOV 0,1                 ;AC0=40
55 01327 107405                 AND 0,1,SNR             ;BIT 10 SHD REMAIN=1
56 01330 063077                 HALT
57 01331 131000                 MOV 1,2
58 01332 112000                 ADC 0,2
59 01333 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
60 01334 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 40
```

```
0024 MNLGC
01                        ;NOW TEST AND OF COMPLIMENTS
02                      ;AN09A:
03 01335 104000                 COM 0,1
04 01336 107404                 AND 0,1,SZR
05 01337 063077                 HALT                    ;AND OF 40 AND ITS COM FAILED
06                      ;TEST AND OF COMPLIMENTS WITH DEST=40 AND SRC=COM
07                      ;AN09B:
08 01340 105000                 MOV 0,1
09 01341 130000                 COM 1,2
10 01342 147404                 AND 2,1,SZR
11 01343 063077                 HALT                    ;AND OF 40 AND ITS COM FAILED
12                        ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
13 01344 101120                 MOVZL 0,0               ;SET UP NEXT TEST
14                              ANDTS 10,9,100
15                      ;AND10:
16 01345 105000                 MOV 0,1                 ;AC0=100
17 01346 107405                 AND 0,1,SNR             ;BIT 9 SHD REMAIN=1
18 01347 063077                 HALT
19 01350 131000                 MOV 1,2
20 01351 112000                 ADC 0,2
21 01352 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
22 01353 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 100
23                        ;NOW TEST AND OF COMPLIMENTS
24                      ;AN10A:
25 01354 104000                 COM 0,1
26 01355 107404                 AND 0,1,SZR
27 01356 063077                 HALT                    ;AND OF 100 AND ITS COM FAILED
28                      ;TEST AND OF COMPLIMENTS WITH DEST=100 AND SRC=COM
29                      ;AN10B:
30 01357 105000                 MOV 0,1
31 01360 130000                 COM 1,2
32 01361 147404                 AND 2,1,SZR
33 01362 063077                 HALT                    ;AND OF 100 AND ITS COM FAILED
34                        ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
35 01363 101120                 MOVZL 0,0               ;SET UP NEXT TEST
36                              ANDTS 11,8,200
37                      ;AND11:
38 01364 105000                 MOV 0,1                 ;AC0=200
39 01365 107405                 AND 0,1,SNR             ;BIT 8 SHD REMAIN=1
40 01366 063077                 HALT
41 01367 131000                 MOV 1,2
42 01370 112000                 ADC 0,2
43 01371 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
44 01372 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 200
45                        ;NOW TEST AND OF COMPLIMENTS
46                      ;AN11A:
47 01373 104000                 COM 0,1
48 01374 107404                 AND 0,1,SZR
49 01375 063077                 HALT                    ;AND OF 200 AND ITS COM FAILED
50                      ;TEST AND OF COMPLIMENTS WITH DEST=200 AND SRC=COM
51                      ;AN11B:
52 01376 105000                 MOV 0,1
53 01377 130000                 COM 1,2
54 01400 147404                 AND 2,1,SZR
55 01401 063077                 HALT                    ;AND OF 200 AND ITS COM FAILED
56                        ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
57 01402 101120                 MOVZL 0,0               ;SET UP NEXT TEST
58                              ANDTS 12,7,400
59                      ;AND12:
60 01403 105000                 MOV 0,1                 ;AC0=400
```

```
01 01404 107405          AND 0,1,SNR      ;BIT 7 SHD REMAIN=1
02 01405 063077          HALT
03 01406 131000          MOV 1,2
04 01407 112000          ADC 0,2
05 01410 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
06 01411 063077          HALT             ;MORE THAN 1 BIT IN AND OF 400
07                   ;NOW TEST AND OF COMPLIMENTS
08                   ;AN12A:
09 01412 104000          COM 0,1
10 01413 107404          AND 0,1,SZR
11 01414 063077          HALT             ;AND OF 400 AND ITS COM FAILED
12                   ;TEST AND OF COMPLIMENTS WITH DEST=400 AND SRC=COM
13                   ;AN12B:
14 01415 105000          MOV 0,1
15 01416 130000          COM 1,2
16 01417 147404          AND 2,1,SZR
17 01420 063077          HALT             ;AND OF 400 AND ITS COM FAILED
18                   ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
19 01421 101120          MOVZL 0,0        ;SET UP NEXT TEST
20                       ANDTS 13,6,1000
21                   ;AND13:
22 01422 105000          MOV 0,1          ;AC0=1000
23 01423 107405          AND 0,1,SNR      ;BIT 6 SHD REMAIN=1
24 01424 063077          HALT
25 01425 131000          MOV 1,2
26 01426 112000          ADC 0,2
27 01427 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
28 01430 063077          HALT             ;MORE THAN 1 BIT IN AND OF 1000
29                   ;NOW TEST AND OF COMPLIMENTS
30                   ;AN13A:
31 01431 104000          COM 0,1
32 01432 107404          AND 0,1,SZR
33 01433 063077          HALT             ;AND OF 1000 AND ITS COM FAILED
34                   ;TEST AND OF COMPLIMENTS WITH DEST=1000 AND SRC=COM
35                   ;AN13B:
36 01434 105000          MOV 0,1
37 01435 130000          COM 1,2
38 01436 147404          AND 2,1,SZR
39 01437 063077          HALT             ;AND OF 1000 AND ITS COM FAILED
40                   ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
41 01440 101120          MOVZL 0,0        ;SET UP NEXT TEST
42                       ANDTS 14,5,2000
43                   ;AND14:
44 01441 105000          MOV 0,1          ;AC0=2000
45 01442 107405          AND 0,1,SNR      ;BIT 5 SHD REMAIN=1
46 01443 063077          HALT
47 01444 131000          MOV 1,2
48 01445 112000          ADC 0,2
49 01446 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
50 01447 063077          HALT             ;MORE THAN 1 BIT IN AND OF 2000
51                   ;NOW TEST AND OF COMPLIMENTS
52                   ;AN14A:
53 01450 104000          COM 0,1
54 01451 107404          AND 0,1,SZR
55 01452 063077          HALT             ;AND OF 2000 AND ITS COM FAILED
56                   ;TEST AND OF COMPLIMENTS WITH DEST=2000 AND SRC=COM
57                   ;AN14B:
58 01453 105000          MOV 0,1
59 01454 130000          COM 1,2
60 01455 147404          AND 2,1,SZR
```



```
01 01456 063077          HALT             ;AND OF 2000 AND ITS COM FAILED
02                   ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03 01457 101120          MOVZL 0,0        ;SET UP NEXT TEST
04                       ANDTS 15,4,4000
05                   ;AND15:
06 01460 105000          MOV 0,1          ;AC0=4000
07 01461 107405          AND 0,1,SNR      ;BIT 4 SHD REMAIN=1
08 01462 063077          HALT
09 01463 131000          MOV 1,2
10 01464 112000          ADC 0,2
11 01465 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
12 01466 063077          HALT             ;MORE THAN 1 BIT IN AND OF 4000
13                   ;NOW TEST AND OF COMPLIMENTS
14                   ;AN15A:
15 01467 104000          COM 0,1
16 01470 107404          AND 0,1,SZR
17 01471 063077          HALT             ;AND OF 4000 AND ITS COM FAILED
18                   ;TEST AND OF COMPLIMENTS WITH DEST=4000 AND SRC=COM
19                   ;AN15B:
20 01472 105000          MOV 0,1
21 01473 130000          COM 1,2
22 01474 147404          AND 2,1,SZR
23 01475 063077          HALT             ;AND OF 4000 AND ITS COM FAILED
24                   ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
25 01476 101120          MOVZL 0,0        ;SET UP NEXT TEST
26                       ANDTS 16,3,10000
27                   ;AND16:
28 01477 105000          MOV 0,1          ;AC0=10000
29 01500 107405          AND 0,1,SNR      ;BIT 3 SHD REMAIN=1
30 01501 063077          HALT
31 01502 131000          MOV 1,2
32 01503 112000          ADC 0,2
33 01504 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
34 01505 063077          HALT             ;MORE THAN 1 BIT IN AND OF 10000
35                   ;NOW TEST AND OF COMPLIMENTS
36                   ;AN16A:
37 01506 104000          COM 0,1
38 01507 107404          AND 0,1,SZR
39 01510 063077          HALT             ;AND OF 10000 AND ITS COM FAILED
40                   ;TEST AND OF COMPLIMENTS WITH DEST=10000 AND SRC=COM
41                   ;AN16B:
42 01511 105000          MOV 0,1
43 01512 130000          COM 1,2
44 01513 147404          AND 2,1,SZR
45 01514 063077          HALT             ;AND OF 10000 AND ITS COM FAILED
46                   ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
47 01515 101120          MOVZL 0,0        ;SET UP NEXT TEST
48                       ANDTS 17,2,20000
49                   ;AND17:
50 01516 105000          MOV 0,1          ;AC0=20000
51 01517 107405          AND 0,1,SNR      ;BIT 2 SHD REMAIN=1
52 01520 063077          HALT
53 01521 131000          MOV 1,2
54 01522 112000          ADC 0,2
55 01523 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
56 01524 063077          HALT             ;MORE THAN 1 BIT IN AND OF 20000
57                   ;NOW TEST AND OF COMPLIMENTS
58                   ;AN17A:
59 01525 104000          COM 0,1
60 01526 107404          AND 0,1,SZR
```

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 0027 MNLGC
01 01527 063077          HALT                ;AND OF 20000 AND ITS COM FAILED
02                     ;TEST AND OF COMPLIMENTS WITH DEST=20000 AND SRC=COM
03                  ;AN17B:
04 01530 105000          MOV 0,1
05 01531 130000          COM 1,2
06 01532 147404          AND 2,1,SZR
07 01533 063077          HALT                ;AND OF 20000 AND ITS COM FAILED
08                     ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
09 01534 101120          MOVZL 0,0           ;SET UP NEXT TEST
10                       ANDTS 18,1,40000
11                  ;AND18:
12 01535 105000          MOV 0,1             ;AC0=40000
13 01536 107405          AND 0,1,SNR         ;BIT 1 SHD REMAIN=1
14 01537 063077          HALT
15 01540 131000          MOV 1,2
16 01541 112000          ADC 0,2
17 01542 150004          COM 2,2,SZR         ;TEST FOR EXTRA BITS
18 01543 063077          HALT                ;MORE THAN 1 BIT IN AND OF 40000
19                     ;NOW TEST AND OF COMPLIMENTS
20                  ;AN18A:
21 01544 104000          COM 0,1
22 01545 107404          AND 0,1,SZR
23 01546 063077          HALT                ;AND OF 40000 AND ITS COM FAILED
24                     ;TEST AND OF COMPLIMENTS WITH DEST=40000 AND SRC=COM
25                  ;AN18B:
26 01547 105000          MOV 0,1
27 01550 130000          COM 1,2
28 01551 147404          AND 2,1,SZR
29 01552 063077          HALT                ;AND OF 40000 AND ITS COM FAILED
30                     ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
31 01553 101120          MOVZL 0,0           ;SET UP NEXT TEST
32                       ANDTS 19,0,100000
33                  ;AND19:
34 01554 105000          MOV 0,1             ;AC0=100000
35 01555 107405          AND 0,1,SNR         ;BIT 0 SHD REMAIN=1
36 01556 063077          HALT
37 01557 131000          MOV 1,2
38 01560 112000          ADC 0,2
39 01561 150004          COM 2,2,SZR         ;TEST FOR EXTRA BITS
40 01562 063077          HALT                ;MORE THAN 1 BIT IN AND OF 100000
41                     ;NOW TEST AND OF COMPLIMENTS
42                  ;AN19A:
43 01563 104000          COM 0,1
44 01564 107404          AND 0,1,SZR
45 01565 063077          HALT                ;AND OF 100000 AND ITS COM FAILED
46                     ;TEST AND OF COMPLIMENTS WITH DEST=100000 AND SRC=COM
47                  ;AN19B:
48 01566 105000          MOV 0,1
49 01567 130000          COM 1,2
50 01570 147404          AND 2,1,SZR
51 01571 063077          HALT                ;AND OF 100000 AND ITS COM FAILED
52                     ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
53 01572 101120          MOVZL 0,0           ;SET UP NEXT TEST
```

```
 0028 MNLGC
01
02                   ;THE NEXT SERIES OF TESTS VERIFY THAT "AND"
03                   ;DOES NOT EFFECT "CRY"
04
05                ;AND24:
06 01573 102040          ADCO 0,0
07 01574 103422          ANDZ 0,0,SZC
08 01575 063077          HALT
09                ;AND25:
10 01576 102020          ADCZ 0,0
11 01577 103443          ANDO 0,0,SNC
12 01600 063077          HALT                ;CRY WENT TO 0 (AND =1 TO =1)
13
14                ;AND26:
15 01601 102000          ADC 0,0
16 01602 100040          COMO 0,0
17 01603 103422          ANDZ 0,0,SZC        ;FURTHER TEST AND IN SCI LOGIC
18 01604 063077          HALT                ;CRY WENT TO 1 AND 0 TO 0
19
20                ;AND27:
21 01605 102000          ADC 0,0
22 01606 100020          COMZ 0,0
23 01607 103443          ANDO 0,0,SNC
24 01610 063077          HALT                ;CRY WENT 1 TO 0 AND OF 0 TO 0
```

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10029 MNLGC
01                ;VERIFY THE EXISTENCE OF INC INSTRUCTION
02                ;FIRST TIME FOR "INC" INSTRUCTION
03              ;INC00:
04 01611 102000           ADC 0,0
05 01612 100000           COM 0,0
06 01613 101405           INC 0,0,SNR       ;RESULT=0 POSSIBLY ALU CRY NOT
07 01614 063077           HALT              ;AC0 SHD=+1
08 01615 105224           MOVZR 0,1,SZR     ;MAKE SURE ONLY +1 NO EXTRAS
09 01616 063077           HALT              ;EXAMINE AC0 FOR EXTRA BITS INC
10
11                ;TEST INC OF +1 TO +2 (2ND TIME FOR INC)
12              ;INC01:
13 01617 102000           ADC 0,0
14 01620 100140           COMOL 0,0         ;AC0=+1
15 01621 105120           MOVZL 0,1         ;AC1=+2
16 01622 101405           INC 0,0,SNR       ;1+1 SHD=2
17 01623 063077           HALT              ;BIT 15 CARRY TO BIT 14(?)
18 01624 100000           ADC 0,1           ;AC1 SHD NOW=-1 (IF INC WORKED)
19 01625 124004           COM 1,1,SZR       ;AND COM SHD BE 0
20 01626 063077           HALT              ;AC0 INC'D+1 INCORRECT
21                ;EXAMINE AC0 FOR ALU FAILURE IT SHD=+2
22                ;IF AC0 DOES=+2 EXAMINE AC1 FOR ADC+COM FAILURE
23
24                ;TEST TO INSURE ONLY SRC REG IS INVOLVED IN INC
25              ;INC02:
26 01627 102000           ADC 0,0
27 01630 100000           COM 0,0           ;AC0=0
28 01631 104140           COMOL 0,1         ;AC1=1
29 01632 125140           MOVOL 1,1         ;=3
30 01633 101405           INC 0,1,SNR       ;0+1 SHD=1
31 01634 063077           HALT              ;ALU CRY FAILED (?) ALRDY TESTED
32 01635 131224           MOVZR 1,2,SZR     ;AC1 SHD ONLY=1
33 01636 063077           HALT              ;PROBABLY DESTINATION REG ALSO ADDED
```

```
10030 MNLGC
01
02                ;TEST INC TO CARRY THROUGH ALL 1 BITS
03                ;DEFINE MACRO FOR CARRY TESTS
04                      .MACRO INCTS
05                ;AC0=A4 COMING INTO TEST,+1=AC1=A5
06                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
07                ;BITA2 INTO BITA3 WITH RESULT=AC1
08              ;INCA1:
09                      INC 0,2,SNR       ;AC0=A4+1 AND BE NON ZERO
10                      HALT              ;INC RESULT SHD=A5
11                      MOV 2,3
12                      ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
13                      COM 3,3,SZR       ;THEN 0
14                      HALT
15                      MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
16                      MOVZL 1,1         ;SET UP RESULT NEXT TEST
17              %
18
19                ;SET UP FIRST CARRY TEST
20 01637 102000           ADC 0,0
21 01640 100000           COM 0,0
22 01641 105140           MOVOL 0,1
23
24                      INCTS 03,ALUCRY,15,0,1
25                ;AC0=0 COMING INTO TEST,+1=AC1=1
26                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
27                ;BITALUCRY INTO BIT15 WITH RESULT=AC1
28              ;INC03:
29 01642 111405           INC 0,2,SNR       ;AC0=0+1 AND BE NON ZERO
30 01643 063077           HALT              ;INC RESULT SHD=1
31 01644 155000           MOV 2,3
32 01645 136000           ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
33 01646 174004           COM 3,3,SZR       ;THEN 0
34 01647 063077           HALT
35 01650 101140           MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
36 01651 125120           MOVZL 1,1         ;SET UP RESULT NEXT TEST
37                      INCTS 04,15,14,1,2
38                ;AC0=1 COMING INTO TEST,+1=AC1=2
39                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
40                ;BIT15 INTO BIT14 WITH RESULT=AC1
41              ;INC04:
42 01652 111405           INC 0,2,SNR       ;AC0=1+1 AND BE NON ZERO
43 01653 063077           HALT              ;INC RESULT SHD=2
44 01654 155000           MOV 2,3
45 01655 136000           ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
46 01656 174004           COM 3,3,SZR       ;THEN 0
47 01657 063077           HALT
48 01660 101140           MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
49 01661 125120           MOVZL 1,1         ;SET UP RESULT NEXT TEST
50                      INCTS 05,14,13,3,4
51                ;AC0=3 COMING INTO TEST,+1=AC1=4
52                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
53                ;BIT14 INTO BIT13 WITH RESULT=AC1
54              ;INC05:
55 01662 111405           INC 0,2,SNR       ;AC0=3+1 AND BE NON ZERO
56 01663 063077           HALT              ;INC RESULT SHD=4
57 01664 155000           MOV 2,3
58 01665 136000           ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
59 01666 174004           COM 3,3,SZR       ;THEN 0
60 01667 063077           HALT
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 0031 MNLGC
01 01670 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
02 01671 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
03                       INCTS 06,13,12,7,10
04                    ;AC0=7 COMING INTO TEST,+1=AC1=10
05                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
06                    ;BIT13 INTO BIT12 WITH RESULT=AC1
07                 ;INC06:
08 01672 111405          INC 0,2,SNR      ;AC0=7+1 AND BE NON ZERO
09 01673 063077          HALT             ;INC RESULT SHD=10
10 01674 155000          MOV 2,3
11 01675 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
12 01676 174004          COM 3,3,SZR      ;THEN 0
13 01677 063077          HALT
14 01700 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
15 01701 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
16                       INCTS 07,12,11,17,20
17                    ;AC0=17 COMING INTO TEST,+1=AC1=20
18                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
19                    ;BIT12 INTO BIT11 WITH RESULT=AC1
20                 ;INC07:
21 01702 111405          INC 0,2,SNR      ;AC0=17+1 AND BE NON ZERO
22 01703 063077          HALT             ;INC RESULT SHD=20
23 01704 155000          MOV 2,3
24 01705 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
25 01706 174004          COM 3,3,SZR      ;THEN 0
26 01707 063077          HALT
27 01710 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
28 01711 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
29                       INCTS 08,11,10,37,40
30                    ;AC0=37 COMING INTO TEST,+1=AC1=40
31                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
32                    ;BIT11 INTO BIT10 WITH RESULT=AC1
33                 ;INC08:
34 01712 111405          INC 0,2,SNR      ;AC0=37+1 AND BE NON ZERO
35 01713 063077          HALT             ;INC RESULT SHD=40
36 01714 155000          MOV 2,3
37 01715 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
38 01716 174004          COM 3,3,SZR      ;THEN 0
39 01717 063077          HALT
40 01720 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
41 01721 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
42                       INCTS 09,10,9,77,100
43                    ;AC0=77 COMING INTO TEST,+1=AC1=100
44                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
45                    ;BIT10 INTO BIT9 WITH RESULT=AC1
46                 ;INC09:
47 01722 111405          INC 0,2,SNR      ;AC0=77+1 AND BE NON ZERO
48 01723 063077          HALT             ;INC RESULT SHD=100
49 01724 155000          MOV 2,3
50 01725 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
51 01726 174004          COM 3,3,SZR      ;THEN 0
52 01727 063077          HALT
53 01730 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
54 01731 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
55                       INCTS 10,9,8,177,200
56                    ;AC0=177 COMING INTO TEST,+1=AC1=200
57                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
58                    ;BIT9 INTO BIT8 WITH RESULT=AC1
59                 ;INC10:
60 01732 111405          INC 0,2,SNR      ;AC0=177+1 AND BE NON ZERO
```

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 0032 MNLGC
01 01733 063077          HALT             ;INC RESULT SHD=200
02 01734 155000          MOV 2,3
03 01735 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
04 01736 174004          COM 3,3,SZR      ;THEN 0
05 01737 063077          HALT
06 01740 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
07 01741 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
08                       INCTS 11,8,7,377,400
09                    ;AC0=377 COMING INTO TEST,+1=AC1=400
10                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
11                    ;BIT8 INTO BIT7 WITH RESULT=AC1
12                 ;INC11:
13 01742 111405          INC 0,2,SNR      ;AC0=377+1 AND BE NON ZERO
14 01743 063077          HALT             ;INC RESULT SHD=400
15 01744 155000          MOV 2,3
16 01745 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
17 01746 174004          COM 3,3,SZR      ;THEN 0
18 01747 063077          HALT
19 01750 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
20 01751 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
21                       INCTS 12,7,6,777,1000
22                    ;AC0=777 COMING INTO TEST,+1=AC1=1000
23                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
24                    ;BIT7 INTO BIT6 WITH RESULT=AC1
25                 ;INC12:
26 01752 111405          INC 0,2,SNR      ;AC0=777+1 AND BE NON ZERO
27 01753 063077          HALT             ;INC RESULT SHD=1000
28 01754 155000          MOV 2,3
29 01755 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
30 01756 174004          COM 3,3,SZR      ;THEN 0
31 01757 063077          HALT
32 01760 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
33 01761 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
34                       INCTS 13,6,5,1777,2000
35                    ;AC0=1777 COMING INTO TEST,+1=AC1=2000
36                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
37                    ;BIT6 INTO BIT5 WITH RESULT=AC1
38                 ;INC13:
39 01762 111405          INC 0,2,SNR      ;AC0=1777+1 AND BE NON ZERO
40 01763 063077          HALT             ;INC RESULT SHD=2000
41 01764 155000          MOV 2,3
42 01765 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
43 01766 174004          COM 3,3,SZR      ;THEN 0
44 01767 063077          HALT
45 01770 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
46 01771 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
47                       INCTS 14,5,4,3777,4000
48                    ;AC0=3777 COMING INTO TEST,+1=AC1=4000
49                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
50                    ;BIT5 INTO BIT4 WITH RESULT=AC1
51                 ;INC14:
52 01772 111405          INC 0,2,SNR      ;AC0=3777+1 AND BE NON ZERO
53 01773 063077          HALT             ;INC RESULT SHD=4000
54 01774 155000          MOV 2,3
55 01775 136000          ADC 1,3          ;ADC SUM OF 1+3 SHD=-1
56 01776 174004          COM 3,3,SZR      ;THEN 0
57 01777 063077          HALT
58 02000 101140          MOVOL 0,0        ;SET UP CONSTANTS NEXT TEST
59 02001 125120          MOVZL 1,1        ;SET UP RESULT NEXT TEST
60                       INCTS 15,4,3,7777,10000
```

```
0033 MNLGC
01                      ;AC0=7777 COMING INTO TEST,+1=AC1=10000
02                      ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
03                      ;BIT4 INTO BIT3 WITH RESULT=AC1
04                    ;INC15:
05 02002 111405                 INC 0,2,SNR       ;AC0=7777+1 AND BE NON ZERO
06 02003 063077                 HALT              ;INC RESULT SHD=10000
07 02004 155020                 MOV 2,3
08 02005 136000                 ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
09 02006 174004                 COM 3,3,SZR       ;THEN 0
10 02007 063077                 HALT
11 02010 101140                 MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
12 02011 125120                 MOVZL 1,1         ;SET UP RESULT NEXT TEST
13                              INCTS 16,3,2,17777,20000
14                      ;AC0=17777 COMING INTO TEST,+1=AC1=20000
15                      ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
16                      ;BIT3 INTO BIT2 WITH RESULT=AC1
17                    ;INC16:
18 02012 111405                 INC 0,2,SNR       ;AC0=17777+1 AND BE NON ZERO
19 02013 063077                 HALT              ;INC RESULT SHD=20000
20 02014 155000                 MOV 2,3
21 02015 136000                 ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
22 02016 174004                 COM 3,3,SZR       ;THEN 0
23 02017 063077                 HALT
24 02020 101140                 MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
25 02021 125120                 MOVZL 1,1         ;SET UP RESULT NEXT TEST
26                              INCTS 17,2,1,37777,40000
27                      ;AC0=37777 COMING INTO TEST,+1=AC1=40000
28                      ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
29                      ;BIT2 INTO BIT1 WITH RESULT=AC1
30                    ;INC17:
31 02022 111405                 INC 0,2,SNR       ;AC0=37777+1 AND BE NON ZERO
32 02023 063077                 HALT              ;INC RESULT SHD=40000
33 02024 155000                 MOV 2,3
34 02025 136000                 ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
35 02026 174004                 COM 3,3,SZR       ;THEN 0
36 02027 063077                 HALT
37 02030 101140                 MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
38 02031 125120                 MOVZL 1,1         ;SET UP RESULT NEXT TEST
39                              INCTS 18,1,0,77777,100000
40                      ;AC0=77777 COMING INTO TEST,+1=AC1=100000
41                      ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
42                      ;BIT1 INTO BIT0 WITH RESULT=AC1
43                    ;INC18:
44 02032 111405                 INC 0,2,SNR       ;AC0=77777+1 AND BE NON ZERO
45 02033 063077                 HALT              ;INC RESULT SHD=100000
46 02034 155000                 MOV 2,3
47 02035 136000                 ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
48 02036 174004                 COM 3,3,SZR       ;THEN 0
49 02037 063077                 HALT
50 02040 101140                 MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
51 02041 125120                 MOVZL 1,1         ;SET UP RESULT NEXT TEST
```

```
0034 MNLGC
01
02                      ;TEST INC OF =1 AC TO=0 WITH CRY COMP 0 TO 1
03                    ;INC20:
04 02042 102040                 ADCO 0,0
05 02043 101424                 INCZ 0,0,SZR
06 02044 063077                 HALT              ;INC=1 DID NOT=0
07 02045 101003                 MOV 0,0,SNC
08 02046 063077                 HALT              ;CRY OUT DID NOT COM 0 TO 1
09                      ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALT
10                      ;TEST INC OF=1 AC TO=0 AND CRY TO COMP 1 TO 0
11
12                    ;INC21:
13 02047 102020                 ADCZ 0,0
14 02050 101444                 INCO 0,0,SZR
15 02051 063077                 HALT              ;INC=1 DID NOT=0
16 02052 101002                 MOV 0,0,SZC
17 02053 063077                 HALT              ;CRY OUT DID NOT COM 1 TO 0
18                      ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALT
```

```
10035 MNLGC
01
02                ;FIRST USE OF NEG INSTRUCTION
03                ;NEG=1 TO =1 TO VERIFY CORRECT INSTR REF
04
05              ;NEG00:
06 02054 102000           ADC 0,0
07 02055 100405           NEG 0,0,SNR
08 02056 063077           HALT              ;NEG MAY=COM+INC+SUB
09 02057 105224           MOVZR 0,1,SZR
10 02060 063077           HALT              ;NEG OF =1 SOMETHING OTHER THAN +1
11                ;EXAMINE AC0 FOR ALU ERROR
12
13                ;THE NEGATION OF +1 SHD=-1
14
15              ;NEG01:
16 02061 102000           ADC 0,0           ;SET=-1
17 02062 100140           COMOL 0,0         ;MAKES AC0=1
18 02063 100405           NEG 0,0,SNR       ;MAKES AC0=-1
19 02064 063077           HALT              ;(?)
20 02065 104004           COM 0,1,SZR       ;RESULT REALLY=-1
21 02066 063077           HALT              ;NEG OF +1 SOMETHING OTHER THAN -1
22                ;EXAMINE AC0 FOR ALU ERROR OR AC1 FOR COM
23
24                ;DEFINE MACRO FOR FURTHER TESTS OF NEG
25                      ,MACRO NEGTS
26                ;AC0=^4 COMING INTO TEST IT SHD NEG TO=^5
27                ;NEG IS EQUIVALENT TO COM+INC
28                ;CARRY IS THROUGH BIT ^2 BUT SHOULD STORE AT BIT ^3
29                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
30              ;NEG^1:
31                      NEG 0,2,SNR       ;^4+1 SHD=^5
32                      HALT              ;CARRY WENT THROUGH BIT ^3
33                ;AC2=^5 IT SHOULD NEG AGAIN TO=AC0 OR ^4
34              ;NG^1A:
35                      NEG 2,3           ;AC2=^5 3 SHD=^4
36                      ADC 0,3           ;AC3 SHD NOW=-1
37                      COM# 3,3,SZR      ;AND ITS COM=0
38                      HALT              ;^5 DID NOT NEG TO ^4
39                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF ^4
40                      MOVZL 0,0
41              %
```

```
10036 MNLGC
01
02                ;SET UP NEG TESTS
03                ;START WITH AC0=1 AC1=0
04                ;2ND TEST AC0=2 AC1=1
05
06 02067 126000           ADC 1,1           ;SET UP AC1=-1
07 02070 120140           COMOL 1,0         ;AC0=+1
08
09                        NEGTS 03,ALUCRY,15,1,177777
10                ;AC0=1 COMING INTO TEST IT SHD NEG TO=177777
11                ;NEG IS EQUIVALENT TO COM+INC
12                ;CARRY IS THROUGH BIT ALUCRY BUT SHOULD STORE AT BIT 15
13                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
14              ;NEG03:
15 02071 110405           NEG 0,2,SNR       ;1+1 SHD=177777
16 02072 063077           HALT              ;CARRY WENT THROUGH BIT 15
17                ;AC2=177777 IT SHOULD NEG AGAIN TO=AC0 OR 1
18              ;NG03A:
19 02073 154400           NEG 2,3           ;AC2=177777 3 SHD=1
20 02074 116000           ADC 0,3           ;AC3 SHD NOW=-1
21 02075 174014           COM# 3,3,SZR      ;AND ITS COM=0
22 02076 063077           HALT              ;177777 DID NOT NEG TO 1
23                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 1
24 02077 101120           MOVZL 0,0
25                        NEGTS 04,15,14,2,177776
26                ;AC0=2 COMING INTO TEST IT SHD NEG TO=177776
27                ;NEG IS EQUIVALENT TO COM+INC
28                ;CARRY IS THROUGH BIT 15 BUT SHOULD STORE AT BIT 14
29                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
30              ;NEG04:
31 02100 110405           NEG 0,2,SNR       ;2+1 SHD=177776
32 02101 063077           HALT              ;CARRY WENT THROUGH BIT 14
33                ;AC2=177776 IT SHOULD NEG AGAIN TO=AC0 OR 2
34              ;NG04A:
35 02102 154400           NEG 2,3           ;AC2=177776 3 SHD=2
36 02103 116000           ADC 0,3           ;AC3 SHD NOW=-1
37 02104 174014           COM# 3,3,SZR      ;AND ITS COM=0
38 02105 063077           HALT              ;177776 DID NOT NEG TO 2
39                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 2
40 02106 101120           MOVZL 0,0
41                        NEGTS 05,14,13,4,177774
42                ;AC0=4 COMING INTO TEST IT SHD NEG TO=177774
43                ;NEG IS EQUIVALENT TO COM+INC
44                ;CARRY IS THROUGH BIT 14 BUT SHOULD STORE AT BIT 13
45                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
46              ;NEG05:
47 02107 110405           NEG 0,2,SNR       ;4+1 SHD=177774
48 02110 063077           HALT              ;CARRY WENT THROUGH BIT 13
49                ;AC2=177774 IT SHOULD NEG AGAIN TO=AC0 OR 4
50              ;NG05A:
51 02111 154400           NEG 2,3           ;AC2=177774 3 SHD=4
52 02112 116000           ADC 0,3           ;AC3 SHD NOW=-1
53 02113 174014           COM# 3,3,SZR      ;AND ITS COM=0
54 02114 063077           HALT              ;177774 DID NOT NEG TO 4
55                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 4
56 02115 101120           MOVZL 0,0
57                        NEGTS 06,13,12,10,177770
58                ;AC0=10 COMING INTO TEST IT SHD NEG TO=177770
59                ;NEG IS EQUIVALENT TO COM+INC
60                ;CARRY IS THROUGH BIT 13 BUT SHOULD STORE AT BIT 12
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                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG06:
02116 110405                  NEG 0,2,SNR       ;10+1 SHD=177770
02117 063077                  HALT              ;CARRY WENT THROUGH BIT 12
                        ;AC2=177770 IT SHOULD NEG AGAIN TO=AC0 OR 10
                      ;NG06A:
02120 154400                  NEG 2,3           ;AC2=177770 3 SHD=10
02121 116000                  ADC 0,3           ;AC3 SHD NOW=-1
02122 174014                  COM# 3,3,SZR      ;AND ITS COM=0
02123 063077                  HALT              ;177770 DID NOT NEG TO 10
                        ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 10
02124 101120                  MOVZL 0,0
                              NEGTS 07,12,11,20,177760
                        ;AC0=20 COMING INTO TEST IT SHD NEG TO=177760
                        ;NEG IS EQUIVALENT TO COM+INC
                        ;CARRY IS THROUGH BIT 12 BUT SHOULD STORE AT BIT 11
                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG07:
02125 110405                  NEG 0,2,SNR       ;20+1 SHD=177760
02126 063077                  HALT              ;CARRY WENT THROUGH BIT 11
                        ;AC2=177760 IT SHOULD NEG AGAIN TO=AC0 OR 20
                      ;NG07A:
02127 154400                  NEG 2,3           ;AC2=177760 3 SHD=20
02130 116000                  ADC 0,3           ;AC3 SHD NOW=-1
02131 174014                  COM# 3,3,SZR      ;AND ITS COM=0
02132 063077                  HALT              ;177760 DID NOT NEG TO 20
                        ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 20
02133 101120                  MOVZL 0,0
                              NEGTS 06,11,10,40,177740
                        ;AC0=40 COMING INTO TEST IT SHD NEG TO=177740
                        ;NEG IS EQUIVALENT TO COM+INC
                        ;CARRY IS THROUGH BIT 11 BUT SHOULD STORE AT BIT 10
                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG08:
02134 110405                  NEG 0,2,SNR       ;40+1 SHD=177740
02135 063077                  HALT              ;CARRY WENT THROUGH BIT 10
                        ;AC2=177740 IT SHOULD NEG AGAIN TO=AC0 OR 40
                      ;NG08A:
02136 154400                  NEG 2,3           ;AC2=177740 3 SHD=40
02137 116000                  ADC 0,3           ;AC3 SHD NOW=-1
02140 174014                  COM# 3,3,SZR      ;AND ITS COM=0
02141 063077                  HALT              ;177740 DID NOT NEG TO 40
                        ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 40
02142 101120                  MOVZL 0,0
                              NEGTS 09,10,9,100,177700
                        ;AC0=100 COMING INTO TEST IT SHD NEG TO=177700
                        ;NEG IS EQUIVALENT TO COM+INC
                        ;CARRY IS THROUGH BIT 10 BUT SHOULD STORE AT BIT 9
                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG09:
02143 110405                  NEG 0,2,SNR       ;100+1 SHD=177700
02144 063077                  HALT              ;CARRY WENT THROUGH BIT 9
                        ;AC2=177700 IT SHOULD NEG AGAIN TO=AC0 OR 100
                      ;NG09A:
02145 154400                  NEG 2,3           ;AC2=177700 3 SHD=100
02146 116000                  ADC 0,3           ;AC3 SHD NOW=-1
02147 174014                  COM# 3,3,SZR      ;AND ITS COM=0
02150 063077                  HALT              ;177700 DID NOT NEG TO 100
                        ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100
02151 101120                  MOVZL 0,0
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                              NEGTS 10,9,8,200,177600
                        ;AC0=200 COMING INTO TEST IT SHD NEG TO=177600
                        ;NEG IS EQUIVALENT TO COM+INC
                        ;CARRY IS THROUGH BIT 9 BUT SHOULD STORE AT BIT 8
                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG10:
02152 110405                  NEG 0,2,SNR       ;200+1 SHD=177600
02153 063077                  HALT              ;CARRY WENT THROUGH BIT 8
                        ;AC2=177600 IT SHOULD NEG AGAIN TO=AC0 OR 200
                      ;NG10A:
02154 154400                  NEG 2,3           ;AC2=177600 3 SHD=200
02155 116000                  ADC 0,3           ;AC3 SHD NOW=-1
02156 174014                  COM# 3,3,SZR      ;AND ITS COM=0
02157 063077                  HALT              ;177600 DID NOT NEG TO 200
                        ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 200
02160 101120                  MOVZL 0,0
                              NEGTS 11,8,7,400,177400
                        ;AC0=400 COMING INTO TEST IT SHD NEG TO=177400
                        ;NEG IS EQUIVALENT TO COM+INC
                        ;CARRY IS THROUGH BIT 8 BUT SHOULD STORE AT BIT 7
                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG11:
02161 110405                  NEG 0,2,SNR       ;400+1 SHD=177400
02162 063077                  HALT              ;CARRY WENT THROUGH BIT 7
                        ;AC2=177400 IT SHOULD NEG AGAIN TO=AC0 OR 400
                      ;NG11A:
02163 154400                  NEG 2,3           ;AC2=177400 3 SHD=400
02164 116000                  ADC 0,3           ;AC3 SHD NOW=-1
02165 174014                  COM# 3,3,SZR      ;AND ITS COM=0
02166 063077                  HALT              ;177400 DID NOT NEG TO 400
                        ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 400
02167 101120                  MOVZL 0,0
                              NEGTS 12,7,6,100,177000
                        ;AC0=100 COMING INTO TEST IT SHD NEG TO=177000
                        ;NEG IS EQUIVALENT TO COM+INC
                        ;CARRY IS THROUGH BIT 7 BUT SHOULD STORE AT BIT 6
                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG12:
02170 110405                  NEG 0,2,SNR       ;100+1 SHD=177000
02171 063077                  HALT              ;CARRY WENT THROUGH BIT 6
                        ;AC2=177000 IT SHOULD NEG AGAIN TO=AC0 OR 100
                      ;NG12A:
02172 154400                  NEG 2,3           ;AC2=177000 3 SHD=100
02173 116000                  ADC 0,3           ;AC3 SHD NOW=-1
02174 174014                  COM# 3,3,SZR      ;AND ITS COM=0
02175 063077                  HALT              ;177000 DID NOT NEG TO 100
                        ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100
02176 101120                  MOVZL 0,0
                              NEGTS 13,6,5,2000,176000
                        ;AC0=2000 COMING INTO TEST IT SHD NEG TO=176000
                        ;NEG IS EQUIVALENT TO COM+INC
                        ;CARRY IS THROUGH BIT 6 BUT SHOULD STORE AT BIT 5
                        ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                      ;NEG13:
02177 110405                  NEG 0,2,SNR       ;2000+1 SHD=176000
02200 063077                  HALT              ;CARRY WENT THROUGH BIT 5
                        ;AC2=176000 IT SHOULD NEG AGAIN TO=AC0 OR 2000
                      ;NG13A:
02201 154400                  NEG 2,3           ;AC2=176000 3 SHD=2000
02202 116000                  ADC 0,3           ;AC3 SHD NOW=-1
```

```
 0039 MNLGC
01 02203 174014          COM# 3,3,SZR      ;AND ITS COM=0
02 02204 063077          HALT              ;176000 DID NOT NEG TO 2000
03                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 2000
04 02205 101120          MOVZL 0,0
05                       NEGTS 14,5,4,4000,174000
06                    ;AC0=4000 COMING INTO TEST IT SHD NEG TO=174000
07                    ;NEG IS EQUIVALENT TO COM+INC
08                    ;CARRY IS THROUGH BIT 5 BUT SHOULD STORE AT BIT 4
09                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
10                 ;NEG14:
11 02206 110405          NEG 0,2,SNR       ;4000+1 SHD=174000
12 02207 063077          HALT              ;CARRY WENT THROUGH BIT 4
13                    ;AC2=174000 IT SHOULD NEG AGAIN TO=AC0 OR 4000
14                 ;NG14A:
15 02210 154400          NEG 2,3           ;AC2=174000 3 SHD=4000
16 02211 116000          ADC 0,3           ;AC3 SHD NOW=-1
17 02212 174014          COM# 3,3,SZR      ;AND ITS COM=0
18 02213 063077          HALT              ;174000 DID NOT NEG TO 4000
19                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 4000
20 02214 101120          MOVZL 0,0
21                       NEGTS 15,4,3,14000,170000
22                    ;AC0=10000 COMING INTO TEST IT SHD NEG TO=170000
23                    ;NEG IS EQUIVALENT TO COM+INC
24                    ;CARRY IS THROUGH BIT 4 BUT SHOULD STORE AT BIT 3
25                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
26                 ;NEG15:
27 02215 110405          NEG 0,2,SNR       ;10000+1 SHD=170000
28 02216 063077          HALT              ;CARRY WENT THROUGH BIT 3
29                    ;AC2=170000 IT SHOULD NEG AGAIN TO=AC0 OR 10000
30                 ;NG15A:
31 02217 154400          NEG 2,3           ;AC2=170000 3 SHD=10000
32 02220 116000          ADC 0,3           ;AC3 SHD NOW=-1
33 02221 174014          COM# 3,3,SZR      ;AND ITS COM=0
34 02222 063077          HALT              ;170000 DID NOT NEG TO 10000
35                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 10000
36 02223 101120          MOVZL 0,0
37                       NEGTS 16,3,1,20000,160000
38                    ;AC0=20000 COMING INTO TEST IT SHD NEG TO=160000
39                    ;NEG IS EQUIVALENT TO COM+INC
40                    ;CARRY IS THROUGH BIT 3 BUT SHOULD STORE AT BIT 1
41                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
42                 ;NEG16:
43 02224 110405          NEG 0,2,SNR       ;20000+1 SHD=160000
44 02225 063077          HALT              ;CARRY WENT THROUGH BIT 1
45                    ;AC2=160000 IT SHOULD NEG AGAIN TO=AC0 OR 20000
46                 ;NG16A:
47 02226 154400          NEG 2,3           ;AC2=160000 3 SHD=20000
48 02227 116000          ADC 0,3           ;AC3 SHD NOW=-1
49 02230 174014          COM# 3,3,SZR      ;AND ITS COM=0
50 02231 063077          HALT              ;160000 DID NOT NEG TO 20000
51                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 20000
52 02232 101120          MOVZL 0,0
53                       NEGTS 17,2,1,40000,140000
54                    ;AC0=40000 COMING INTO TEST IT SHD NEG TO=140000
55                    ;NEG IS EQUIVALENT TO COM+INC
56                    ;CARRY IS THROUGH BIT 2 BUT SHOULD STORE AT BIT 1
57                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
58                 ;NEG17:
59 02233 110405          NEG 0,2,SNR       ;40000+1 SHD=140000
60 02234 063077          HALT              ;CARRY WENT THROUGH BIT 1
```

```
 0040 MNLGC
01                    ;AC2=140000 IT SHOULD NEG AGAIN TO=AC0 OR 40000
02                 ;NG17A:
03 02235 154400          NEG 2,3           ;AC2=140000 3 SHD=40000
04 02236 116000          ADC 0,3           ;AC3 SHD NOW=-1
05 02237 174014          COM# 3,3,SZR      ;AND ITS COM=0
06 02240 063077          HALT              ;140000 DID NOT NEG TO 40000
07                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 40000
08 02241 101120          MOVZL 0,0
09                       NEGTS 18,1,0,100000,100000
10                    ;AC0=100000 COMING INTO TEST IT SHD NEG TO=100000
11                    ;NEG IS EQUIVALENT TO COM+INC
12                    ;CARRY IS THROUGH BIT 1 BUT SHOULD STORE AT BIT 0
13                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
14                 ;NEG18:
15 02242 110405          NEG 0,2,SNR       ;100000+1 SHD=100000
16 02243 063077          HALT              ;CARRY WENT THROUGH BIT 0
17                    ;AC2=100000 IT SHOULD NEG AGAIN TO=AC0 OR 100000
18                 ;NG18A:
19 02244 154400          NEG 2,3           ;AC2=100000 3 SHD=100000
20 02245 116000          ADC 0,3           ;AC3 SHD NOW=-1
21 02246 174014          COM# 3,3,SZR      ;AND ITS COM=0
22 02247 063077          HALT              ;100000 DID NOT NEG TO 100000
23                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100000
24 02250 101120          MOVZL 0,0
```

```
10041 MNLGC
01                ;AC0=0 COMING INTO TEST IT SHD NEG TO =0
02                ;CARRY IS THROUGH BIT 0 AND SHOULD COM CRY
03                ;NEG19:
04 02251 110404           NEG 0,2,SZR       ;-0+1=0
05 02252 063077           HALT              ;SEE AC2 NOT=0
06                ;AC2 =0 IT SHD NEGATE TO =0 IN AC3
07                ;NG19A:
08 02253 154404           NEG 2,3,SZR
09 02254 063077           HALT              ;0 DID NOT NEG TO 0
10
11                  ;NEGATING 0 SHOULD COMPLIMENT CRY 0 TO 1
12
13                ;NEG20:
14 02255 102000           ADC 0,0
15 02256 100040           COMO 0,0
16 02257 100423           NEGZ 0,0,SNC
17 02260 063077           HALT              ;NEG 0 DID NOT SET CRY
18
19                  ;NEGATING 0 SHOULD COM CRY 1 TO 0
20
21                ;NEG21:
22 02261 102000           ADC 0,0
23 02262 100020           COMZ 0,0
24 02263 100442           NEGO 0,0,SZC
25 02264 063077           HALT              ;NEG 0 DID NOT CLR CRY
```

```
10042 MNLGC
01
02                  ;TEST FOR EXISTANCE OF SUB INSTRUCTION
03                  ;FIRST TIME FOR SUB
04
05                ;SUB00:
06 02265 102000           ADC 0,0           ;AC0=-1
07 02266 102404           SUB 0,0,SZR       ;SUB -1 FROM -1
08 02267 063077           HALT              ;EXAMINE AC0 FOR ERR SHD=0
09                  ;SUBTRACT +1 FROM +1 CHECK FOR 0 RESULT (2ND SUB)
10                ;SUB01:
11 02270 102000           ADC 0,0
12 02271 100405           NEG 0,0,SNR       ;SET AC0=+1
13 02272 063077           HALT              ;SET UP FAILED AC0 SHD=+1
14 02273 102404           SUB 0,0,SZR       ;+1-+1 SHD=0
15 02274 063077           HALT              ;SUB +1-+1 FAILED SEE AC0
16
17                  ;DEFINE SUBTRACT "SUB" TEST MACRO
18
19                        .MACRO SUBTS
20                  ;AC0=A2 COMING INTO THIS TEST A2-A2 SHOULD=0 RESULT
21                  ;0-A2 NEGATED-A2 SHD=0 INTO AC3
22                ;SUBA1:
23                        MOVO 0,1
24                        SUBZ 0,1,SZR
25                        HALT              ;A2-A2 SEE AC1 SHD=0
26                        MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
27                        HALT    ;AC0=A2(?) CRY SHD=1
28                        ADC 2,2
29                        COM 2,2 ;MAKE AC2=0 FOR TEST
30                  ;0-A2 SHOULD=-A2 NEGATED TO AC3
31                        SUB 0,2           ;0-A2
32                        NEGZ 2,3          ;NEGATED SHD=A2
33                        SUBO 0,3,SZR      ;A2-A2 SHD=0 AGAIN
34                        HALT
35                        MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
36                        HALT              ;CRY OUT FAILED
37                        MOVZL 0,0         ;SET UP NEXT TEST
38                %
39
40                  ;SET UP SUBTRACT TESTS
41 02275 102000           ADC 0,0
42 02276 100140           COMOL 0,0
```

```
10043 MNLGC
01
02                      SUBTS 02,1
03                    ;AC0=1 COMING INTO THIS TEST 1-1 SHOULD=0 RESULT
04                    ;0-1 NEGATED-1 SHD=0 INTO AC3
05                  ;SUB02:
06 02277 105040             MOVO 0,1
07 02300 106424             SUBZ 0,1,SZR
08 02301 063077             HALT            ;1-1 SEE AC1 SHD=0
09 02302 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
10 02303 063077             HALT    ;AC0=1(?) CRY SHD=1
11 02304 152000             ADC 2,2
12 02305 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
13                    ;0-1 SHOULD=-1 NEGATED TO AC3
14 02306 112400             SUB 0,2         ;0-1
15 02307 154420             NEGZ 2,3        ;NEGATED SHD=1
16 02310 116444             SUBO 0,3,SZR    ;1-1 SHD=0 AGAIN
17 02311 063077             HALT
18 02312 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
19 02313 063077             HALT            ;CRY OUT FAILED
20 02314 101120             MOVZL 0,0       ;SET UP NEXT TEST
21                          SUBTS 03,2
22                    ;AC0=2 COMING INTO THIS TEST 2-2 SHOULD=0 RESULT
23                    ;0-2 NEGATED-2 SHD=0 INTO AC3
24                  ;SUB03:
25 02315 105040             MOVO 0,1
26 02316 106424             SUBZ 0,1,SZR
27 02317 063077             HALT            ;2-2 SEE AC1 SHD=0
28 02320 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
29 02321 063077             HALT    ;AC0=2(?) CRY SHD=1
30 02322 152000             ADC 2,2
31 02323 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
32                    ;0-2 SHOULD=-2 NEGATED TO AC3
33 02324 112400             SUB 0,2         ;0-2
34 02325 154420             NEGZ 2,3        ;NEGATED SHD=2
35 02326 116444             SUBO 0,3,SZR    ;2-2 SHD=0 AGAIN
36 02327 063077             HALT
37 02330 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
38 02331 063077             HALT            ;CRY OUT FAILED
39 02332 101120             MOVZL 0,0       ;SET UP NEXT TEST
40                          SUBTS 04,4
41                    ;AC0=4 COMING INTO THIS TEST 4-4 SHOULD=0 RESULT
42                    ;0-4 NEGATED=4 SHD=0 INTO AC3
43                  ;SUB04:
44 02333 105040             MOVO 0,1
45 02334 106424             SUBZ 0,1,SZR
46 02335 063077             HALT            ;4-4 SEE AC1 SHD=0
47 02336 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
48 02337 063077             HALT    ;AC0=4(?) CRY SHD=1
49 02340 152000             ADC 2,2
50 02341 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
51                    ;0-4 SHOULD=-4 NEGATED TO AC3
52 02342 112400             SUB 0,2         ;0-4
53 02343 154420             NEGZ 2,3        ;NEGATED SHD=4
54 02344 116444             SUBO 0,3,SZR    ;4-4 SHD=0 AGAIN
55 02345 063077             HALT
56 02346 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
57 02347 063077             HALT            ;CRY OUT FAILED
58 02350 101120             MOVZL 0,0       ;SET UP NEXT TEST
59                          SUBTS 05,10
60                    ;AC0=10 COMING INTO THIS TEST 10-10 SHOULD=0 RESULT
```

```
0044 MNLGC
01                    ;0-10 NEGATED-10 SHD=0 INTO AC3
02                  ;SUB05:
03 02351 105040             MOVO 0,1
04 02352 106424             SUBZ 0,1,SZR
05 02353 063077             HALT            ;10-10 SEE AC1 SHD=0
06 02354 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
07 02355 063077             HALT    ;AC0=10(?) CRY SHD=1
08 02356 152000             ADC 2,2
09 02357 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
10                    ;0-10 SHOULD=-10 NEGATED TO AC3
11 02360 112400             SUB 0,2         ;0-10
12 02361 154420             NEGZ 2,3        ;NEGATED SHD=10
13 02362 116444             SUBO 0,3,SZR    ;10-10 SHD=0 AGAIN
14 02363 063077             HALT
15 02364 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
16 02365 063077             HALT            ;CRY OUT FAILED
17 02366 101120             MOVZL 0,0       ;SET UP NEXT TEST
18                          SUBTS 06,20
19                    ;AC0=20 COMING INTO THIS TEST 20-20 SHOULD=0 RESULT
20                    ;0-20 NEGATED-20 SHD=0 INTO AC3
21                  ;SUB06:
22 02367 105040             MOVO 0,1
23 02370 106424             SUBZ 0,1,SZR
24 02371 063077             HALT            ;20-20 SEE AC1 SHD=0
25 02372 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
26 02373 063077             HALT    ;AC0=20(?) CRY SHD=1
27 02374 152000             ADC 2,2
28 02375 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
29                    ;0-20 SHOULD=-20 NEGATED TO AC3
30 02376 112400             SUB 0,2         ;0-20
31 02377 154420             NEGZ 2,3        ;NEGATED SHD=20
32 02400 116444             SUBO 0,3,SZR    ;20-20 SHD=0 AGAIN
33 02401 063077             HALT
34 02402 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
35 02403 063077             HALT            ;CRY OUT FAILED
36 02404 101120             MOVZL 0,0       ;SET UP NEXT TEST
37                          SUBTS 07,40
38                    ;AC0=40 COMING INTO THIS TEST 40-40 SHOULD=0 RESULT
39                    ;0-40 NEGATED-40 SHD=0 INTO AC3
40                  ;SUB07:
41 02405 105040             MOVO 0,1
42 02406 106424             SUBZ 0,1,SZR
43 02407 063077             HALT            ;40-40 SEE AC1 SHD=0
44 02410 101007             MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
45 02411 063077             HALT    ;AC0=40(?) CRY SHD=1
46 02412 152000             ADC 2,2
47 02413 150000             COM 2,2 ;MAKE AC2=0 FOR TEST
48                    ;0-40 SHOULD=-40 NEGATED TO AC3
49 02414 112400             SUB 0,2         ;0-40
50 02415 154420             NEGZ 2,3        ;NEGATED SHD=40
51 02416 116444             SUBO 0,3,SZR    ;40-40 SHD=0 AGAIN
52 02417 063077             HALT
53 02420 101002             MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
54 02421 063077             HALT            ;CRY OUT FAILED
55 02422 101120             MOVZL 0,0       ;SET UP NEXT TEST
56                          SUBTS 08,100
57                    ;AC0=100 COMING INTO THIS TEST 100-100 SHOULD=0 RESULT
58                    ;0-100 NEGATED-100 SHD=0 INTO AC3
59                  ;SUB08:
60 02423 105040             MOVO 0,1
```

```
 0045 MNLGC
01 02424 106424          SUBZ 0,1,SZR
02 02425 063077          HALT                ;100-100 SEE AC1 SHD=0
03 02426 101007          MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
04 02427 063077          HALT     ;AC0=100(7) CRY SHD=1
05 02430 152000          ADC 2,2
06 02431 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
07                     ;0-100 SHOULD=-100 NEGATED TO AC3
08 02432 112400          SUB 0,2             ;0-100
09 02433 154420          NEGZ 2,3            ;NEGATED SHD=100
10 02434 116444          SUBO 0,3,SZR        ;100-100 SHD=0 AGAIN
11 02435 063077          HALT
12 02436 101002          MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
13 02437 063077          HALT                ;CRY OUT FAILED
14 02440 101120          MOVZL 0,0           ;SET UP NEXT TEST
15                       SUBTS 09,200
16                     ;AC0=200 COMING INTO THIS TEST 200-200 SHOULD=0 RESULT
17                     ;0-200 NEGATED-200 SHD=0 INTO AC3
18                   ;SUB09:
19 02441 105040          MOVO 0,1
20 02442 106424          SUBZ 0,1,SZR
21 02443 063077          HALT                ;200-200 SEE AC1 SHD=0
22 02444 101007          MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
23 02445 063077          HALT     ;AC0=200(7) CRY SHD=1
24 02446 152000          ADC 2,2
25 02447 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
26                     ;0-200 SHOULD=-200 NEGATED TO AC3
27 02450 112400          SUB 0,2             ;0-200
28 02451 154420          NEGZ 2,3            ;NEGATED SHD=200
29 02452 116444          SUBO 0,3,SZR        ;200-200 SHD=0 AGAIN
30 02453 063077          HALT
31 02454 101002          MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
32 02455 063077          HALT                ;CRY OUT FAILED
33 02456 101120          MOVZL 0,0           ;SET UP NEXT TEST
34                       SUBTS 10,400
35                     ;AC0=400 COMING INTO THIS TEST 400-400 SHOULD=0 RESULT
36                     ;0-400 NEGATED-400 SHD=0 INTO AC3
37                   ;SUB10:
38 02457 105040          MOVO 0,1
39 02460 106424          SUBZ 0,1,SZR
40 02461 063077          HALT                ;400-400 SEE AC1 SHD=0
41 02462 101007          MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
42 02463 063077          HALT     ;AC0=400(7) CRY SHD=1
43 02464 152000          ADC 2,2
44 02465 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
45                     ;0-400 SHOULD=-400 NEGATED TO AC3
46 02466 112400          SUB 0,2             ;0-400
47 02467 154420          NEGZ 2,3            ;NEGATED SHD=400
48 02470 116444          SUBO 0,3,SZR        ;400-400 SHD=0 AGAIN
49 02471 063077          HALT
50 02472 101002          MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
51 02473 063077          HALT                ;CRY OUT FAILED
52 02474 101120          MOVZL 0,0           ;SET UP NEXT TEST
53                       SUBTS 11,1000
54                     ;AC0=1000 COMING INTO THIS TEST 1000-1000 SHOULD=0 RESULT
55                     ;0-1000 NEGATED-1000 SHD=0 INTO AC3
56                   ;SUB11:
57 02475 105040          MOVO 0,1
58 02476 106424          SUBZ 0,1,SZR
59 02477 063077          HALT                ;1000-1000 SEE AC1 SHD=0
60 02500 101007          MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
```

```
 0046 MNLGC
01 02501 063077          HALT     ;AC0=1000(7) CRY SHD=1
02 02502 152000          ADC 2,2
03 02503 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
04                     ;0-1000 SHOULD=-1000 NEGATED TO AC3
05 02504 112400          SUB 0,2             ;0-1000
06 02505 154420          NEGZ 2,3            ;NEGATED SHD=1000
07 02506 116444          SUBO 0,3,SZR        ;1000-1000 SHD=0 AGAIN
08 02507 063077          HALT
09 02510 101002          MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
10 02511 063077          HALT                ;CRY OUT FAILED
11 02512 101120          MOVZL 0,0           ;SET UP NEXT TEST
12                       SUBTS 12,2000
13                     ;AC0=2000 COMING INTO THIS TEST 2000-2000 SHOULD=0 RESULT
14                     ;0-2000 NEGATED-2000 SHD=0 INTO AC3
15                   ;SUB12:
16 02513 105040          MOVO 0,1
17 02514 106424          SUBZ 0,1,SZR
18 02515 063077          HALT                ;2000-2000 SEE AC1 SHD=0
19 02516 101007          MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
20 02517 063077          HALT     ;AC0=2000(7) CRY SHD=1
21 02520 152000          ADC 2,2
22 02521 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
23                     ;0-2000 SHOULD=-2000 NEGATED TO AC3
24 02522 112400          SUB 0,2             ;0-2000
25 02523 154420          NEGZ 2,3            ;NEGATED SHD=2000
26 02524 116444          SUBO 0,3,SZR        ;2000-2000 SHD=0 AGAIN
27 02525 063077          HALT
28 02526 101002          MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
29 02527 063077          HALT                ;CRY OUT FAILED
30 02530 101120          MOVZL 0,0           ;SET UP NEXT TEST
31                       SUBTS 13,4000
32                     ;AC0=4000 COMING INTO THIS TEST 4000-4000 SHOULD=0 RESULT
33                     ;0-4000 NEGATED-4000 SHD=0 INTO AC3
34                   ;SUB13:
35 02531 105040          MOVO 0,1
36 02532 106424          SUBZ 0,1,SZR
37 02533 063077          HALT                ;4000-4000 SEE AC1 SHD=0
38 02534 101007          MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
39 02535 063077          HALT     ;AC0=4000(7) CRY SHD=1
40 02536 152000          ADC 2,2
41 02537 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
42                     ;0-4000 SHOULD=-4000 NEGATED TO AC3
43 02540 112400          SUB 0,2             ;0-4000
44 02541 154420          NEGZ 2,3            ;NEGATED SHD=4000
45 02542 116444          SUBO 0,3,SZR        ;4000-4000 SHD=0 AGAIN
46 02543 063077          HALT
47 02544 101002          MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
48 02545 063077          HALT                ;CRY OUT FAILED
49 02546 101120          MOVZL 0,0           ;SET UP NEXT TEST
50                       SUBTS 14,10000
51                     ;AC0=10000 COMING INTO THIS TEST 10000-10000 SHOULD=0 RESULT
52                     ;0-10000 NEGATED-10000 SHD=0 INTO AC3
53                   ;SUB14:
54 02547 105040          MOVO 0,1
55 02550 106424          SUBZ 0,1,SZR
56 02551 063077          HALT                ;10000-10000 SEE AC1 SHD=0
57 02552 101007          MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
58 02553 063077          HALT     ;AC0=10000(7) CRY SHD=1
59 02554 152000          ADC 2,2
60 02555 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
```

```
 0047 MNLGC
01                      ;0-10000 SHOULD=-10000 NEGATED TO AC3
02 02556 112400                 SUB 0,2         ;0-10000
03 02557 154420                 NEGZ 2,3        ;NEGATED SHD=10000
04 02560 116444                 SUBO 0,3,SZR    ;10000-10000 SHD=0 AGAIN
05 02561 063077                 HALT
06 02562 101002                 MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
07 02563 063077                 HALT            ;CRY OUT FAILED
08 02564 101120                 MOVZL 0,0       ;SET UP NEXT TEST
09                              SUBTS 15,20000
10                      ;AC0=20000 COMING INTO THIS TEST 20000-20000 SHOULD=0 RESULT
11                      ;0-20000 NEGATED=20000 SHD=0 INTO AC3
12                    ;SUB15:
13 02565 105040                 MOVO 0,1
14 02566 106424                 SUBZ 0,1,SZR
15 02567 063077                 HALT            ;20000-20000 SEE AC1 SHD=0
16 02570 101007                 MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
17 02571 063077                 HALT    ;AC0=20000(?) CRY SHD=1
18 02572 152000                 ADC 2,2
19 02573 150000                 COM 2,2 ;MAKE AC2=0 FOR TEST
20                      ;0-20000 SHOULD=-20000 NEGATED TO AC3
21 02574 112400                 SUB 0,2         ;0-20000
22 02575 154420                 NEGZ 2,3        ;NEGATED SHD=20000
23 02576 116444                 SUBO 0,3,SZR    ;20000-20000 SHD=0 AGAIN
24 02577 063077                 HALT
25 02600 101002                 MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
26 02601 063077                 HALT            ;CRY OUT FAILED
27 02602 101120                 MOVZL 0,0       ;SET UP NEXT TEST
28                              SUBTS 16,40000
29                      ;AC0=40000 COMING INTO THIS TEST 40000-40000 SHOULD=0 RESULT
30                      ;0-40000 NEGATED=40000 SHD=0 INTO AC3
31                    ;SUB16:
32 02603 105040                 MOVO 0,1
33 02604 106424                 SUBZ 0,1,SZR
34 02605 063077                 HALT            ;40000-40000 SEE AC1 SHD=0
35 02606 101007                 MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
36 02607 063077                 HALT    ;AC0=40000(?) CRY SHD=1
37 02610 152000                 ADC 2,2
38 02611 150000                 COM 2,2 ;MAKE AC2=0 FOR TEST
39                      ;0-40000 SHOULD=-40000 NEGATED TO AC3
40 02612 112400                 SUB 0,2         ;0-40000
41 02613 154420                 NEGZ 2,3        ;NEGATED SHD=40000
42 02614 116444                 SUBO 0,3,SZR    ;40000-40000 SHD=0 AGAIN
43 02615 063077                 HALT
44 02616 101002                 MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
45 02617 063077                 HALT            ;CRY OUT FAILED
46 02620 101120                 MOVZL 0,0       ;SET UP NEXT TEST
47                              SUBTS 17,100000
48                      ;AC0=100000 COMING INTO THIS TEST 100000-100000 SHOULD=0 RESUL
49                      ;0-100000 NEGATED=100000 SHD=0 INTO AC3
50                    ;SUB17:
51 02621 105040                 MOVO 0,1
52 02622 106424                 SUBZ 0,1,SZR
53 02623 063077                 HALT            ;100000-100000 SEE AC1 SHD=0
54 02624 101007                 MOV 0,0,SBN     ;0 CRY SHD =1 FROM CRYOUT
55 02625 063077                 HALT    ;AC0=100000(?) CRY SHD=1
56 02626 152000                 ADC 2,2
57 02627 150000                 COM 2,2 ;MAKE AC2=0 FOR TEST
58                      ;0-100000 SHOULD=-100000 NEGATED TO AC3
59 02630 112400                 SUB 0,2         ;0-100000
60 02631 154420                 NEGZ 2,3        ;NEGATED SHD=100000
```

```
 0048 MNLGC
01 02632 116444                 SUBO 0,3,SZR    ;100000-100000 SHD=0 AGAIN
02 02633 063077                 HALT
03 02634 101002                 MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
04 02635 063077                 HALT            ;CRY OUT FAILED
05 02636 101120                 MOVZL 0,0       ;SET UP NEXT TEST
06
07
```

```
!0049 MNLGC
01                      ;LOAD ACCUMULATOR TESTS FIRST MRI FIRST LDA
02                    ;LDA00:
03 02637 102400                 SUB 0,0
04 02640 105040                 MOVO 0,1
05 02641 020065                 LDA 0,K1        ;K1=1
06 02642 101005                 MOV 0,0,SNR     ;AC IS AT LEAST NON ZERO
07 02643 063077                 HALT            ;DID NOT LOAD AC0 WITH+1
08 02644 105234                 MOVZR# 0,1,SZR  ;CHECK AC0 TO REALLY=+1
09 02645 063077                 HALT            ;SEE AC0 NOT=+1
10                      ;FIRST USE OF MRI OR LDA INSTRUCTION
11                      ;INCORRECT RESULT IN AC0 COULD BE DUE TO ANY OF
12                      ;A VARIETY OF PROBLEMS INCLUDING EFA
13                      ;IF MRI DOES NOT SET ALC INSTRUCTION DECODES AS COMZ 1,0
14                      ;AC0 WILL=-1 AND CARRY WILL=0
15                      ;IF INSTRUCTION DECODES AS I/O IT'S NIO 40(AC0=0)
16                      ;IF DATA IN AC0 IS OTHER THAN 0 OR -1 EFA
17
18                      ;DEFINE MACRO TO VERIFY LDA DOES NOT DISTURB OTHER AC'S
19                              .MACRO LDAT1
20                    ;LDA^1:
21                              ADC ^3,^3       ;SET AC^3=-1
22                              MOV ^3,^4
23                              MOV ^3,^5
24                              LDA ^2,K1       ;LOAD +1 TO AC^2
25                              AND ^3,^4
26                              AND ^4,^5
27                              COM ^5,^5,SZR   ;AC^5 SHD =-1
28                              HALT            ;LDA OF ^2 DIST AC^3,AC^4,AC^5
29                      %
30
31                              LDAT1 01,0,1,2,3
32                    ;LDA01:
33 02646 120000                 ADC 1,1 ;SET AC1=-1
34 02647 131000                 MOV 1,2
35 02650 133000                 MOV 1,3
36 02651 020065                 LDA 0,K1        ;LOAD +1 TO AC0
37 02652 133400                 AND 1,2
38 02653 157400                 AND 2,3
39 02654 174004                 COM 3,3,SZR     ;AC3 SHD =-1
40 02655 063077                 HALT            ;LDA OF 0 DIST AC1,AC2,AC3
41                              LDAT1 02,1,2,3,0
42                    ;LDA02:
43 02656 152000                 ADC 2,2 ;SET AC2=-1
44 02657 155000                 MOV 2,3
45 02660 141000                 MOV 2,0
46 02661 024065                 LDA 1,K1        ;LOAD +1 TO AC1
47 02662 157400                 AND 2,3
48 02663 163400                 AND 3,0
49 02664 100004                 COM 0,0,SZR     ;AC0 SHD =-1
50 02665 063077                 HALT            ;LDA OF 1 DIST AC2,AC3,AC0
51                              LDAT1 03,2,3,0,1
52                    ;LDA03:
53 02666 176000                 ADC 3,3 ;SET AC3=-1
54 02667 161000                 MOV 3,0
55 02670 165000                 MOV 3,1
56 02671 030065                 LDA 2,K1        ;LOAD +1 TO AC2
57 02672 163400                 AND 3,0
58 02673 107400                 AND 0,1
59 02674 124004                 COM 1,1,SZR     ;AC1 SHD =-1
60 02675 063077                 HALT            ;LDA OF 2 DIST AC3,AC0,AC1
```

```
 0050 MNLGC
01                              LDAT1 04,3,0,1,2
02                    ;LDA04:
03 02676 102000                 ADC 0,0 ;SET AC0=-1
04 02677 105000                 MOV 0,1
05 02700 111000                 MOV 0,2
06 02701 034065                 LDA 3,K1        ;LOAD +1 TO AC3
07 02702 107400                 AND 0,1
08 02703 133400                 AND 1,2
09 02704 150004                 COM 2,2,SZR     ;AC2 SHD =-1
10 02705 063077                 HALT            ;LDA OF 3 DIST AC0,AC1,AC2
```

```
10051 MNLGC
01                      ;FURTHER TEST OF LDA INSTRUCTION
02 02700 020113         LDA 0,K25252
03 02701 024114         LDA 1,K52525
04 02710 107404         AND 0,1,SZR
05 02711 063077         HALT
06 02712 024114         LDA 1,K52525
07 02713 101100         MOVL 0,0
08 02714 106404         SUB 0,1,SZR
09 02715 063077         HALT
```

```
10052 MNLGC
01                      ;FIRST TEST OF BYTE SWAP "S"
02                      ;CALC .IR8,IR9 INTO ALU SHIFTER
03
04                    ;SWP00:
05 02716 102745         SUBOS 0,0,SNR
06 02717 101324         MOVZS 0,0,SZR   ;FIRST USE OF "S" AC0=0
07 02720 063077         HALT            ;EXAMINE AC0 FOR "SWAP" ERR
08                    ;SWP01:
09 02721 102323         ADCZS 0,0,SNC   ;CRY SHD REMAIN=0
10 02722 101302         MOVS 0,0,SZC    ;SAME
11 02723 063077         HALT            ;SEE ZC SHIFTER
12                    ;SWP02:
13 02724 102722         SUBZS 0,0,SZC   ;CRY SHD REMAIN=1
14 02725 101303         MOVS 0,0,SNC    ;SAME
15 02726 063077         HALT            ;SEE ZC SHIFTER
16                    ;SWP03:
17 02727 102725         SUBZS 0,0,SNR   ;A 1 IN CRY SHD NOT AFFECT "S"
18 02730 101344         MOVOS 0,0,SZR   ;TRY SWAP 0'S WITH CRY=1
19 02731 063077         HALT            ;EXAMINE AC0 FOR CRY "S"
20                    ;ERROR DEPENDS ON A 1 IN BIT 0 OR 15 SEE ALU SHIFTER
21
22                    ;DEFINE SWAP TEST MACRO
23                          .MACRO SWPTS
24                    ;AC0=A6 AC1=A7
25                    ;SWPA1:
26                          LDA 0,A2        ;GET A6
27                          LDA 1,A3        ;A7 EXPECTED RESULT
28                          MOVZS 0,3               ;"S" BIT A4 TO BIT A5
29                          SUB 1,3,SZR
30                          HALT            ;FAILED EX AC2
31                    %
32
33
34
35                          SWPTS 04,K1,K400,15,7,1,400
36                    ;AC0=1 AC1=400
37                    ;SWP04:
38 02732 020065             LDA 0,K1        ;GET 1
39 02733 024100             LDA 1,K400      ;400 EXPECTED RESULT
40 02734 115320             MOVZS 0,3               ;"S" BIT 15 TO BIT 7
41 02735 136404             SUB 1,3,SZR
42 02736 063077             HALT            ;FAILED EX AC2
43                          SWPTS 05,K2,K1000,14,6,2,1000
44                    ;AC0=2 AC1=1000
45                    ;SWP05:
46 02737 020066             LDA 0,K2        ;GET 2
47 02740 024101             LDA 1,K1000     ;1000 EXPECTED RESULT
48 02741 115320             MOVZS 0,3               ;"S" BIT 14 TO BIT 6
49 02742 136404             SUB 1,3,SZR
50 02743 063077             HALT            ;FAILED EX AC2
51                          SWPTS 06,K4,K2000,13,5,4,2000
52                    ;AC0=4 AC1=2000
53                    ;SWP06:
54 02744 020070             LDA 0,K4        ;GET 4
55 02745 024102             LDA 1,K2000     ;2000 EXPECTED RESULT
56 02746 115320             MOVZS 0,3               ;"S" BIT 13 TO BIT 5
57 02747 136404             SUB 1,3,SZR
58 02750 063077             HALT            ;FAILED EX AC2
59                          SWPTS 07,K10,K4000,12,4,10,4000
60                    ;AC0=10 AC1=4000
```

```
0053 MNLGC
                        ;SWP07:
002751 020072                   LDA 0,K10       ;GET 10
002752 024003                   LDA 1,K4000     ;4000 EXPECTED RESULT
002753 115320                   MOVZS 0,3               ;"S" BIT 12 TO BIT 4
002754 136004                   SUB 1,3,SZR
002755 063077                   HALT            ;FAILED EX AC2
                                SWPTS 08,K20,K10K,11,3,20,10000
                        ;AC0=20 AC1=10000
                        ;SWP08:
002756 020073                   LDA 0,K20       ;GET 20
002757 024004                   LDA 1,K10K      ;10000 EXPECTED RESULT
002760 115320                   MOVZS 0,3               ;"S" BIT 11 TO BIT 3
002761 136004                   SUB 1,3,SZR
002762 063077                   HALT            ;FAILED EX AC2
                                SWPTS 09,K40,K20K,10,2,40,20000
                        ;AC0=40 AC1=20000
                        ;SWP09:
002763 020074                   LDA 0,K40       ;GET 40
002764 024005                   LDA 1,K20K      ;20000 EXPECTED RESULT
002765 115320                   MOVZS 0,3               ;"S" BIT 10 TO BIT 2
002766 136004                   SUB 1,3,SZR
002767 063077                   HALT            ;FAILED EX AC2
                                SWPTS 10,K100,K40K,9,1,100,40000
                        ;AC0=100 AC1=40000
                        ;SWP10:
002770 020075                   LDA 0,K100      ;GET 100
002771 024006                   LDA 1,K40K      ;40000 EXPECTED RESULT
002772 115320                   MOVZS 0,3               ;"S" BIT 9 TO BIT 1
002773 136004                   SUB 1,3,SZR
002774 063077                   HALT            ;FAILED EX AC2
                                SWPTS 11,K200,K100K,8,0,200,100000
                        ;AC0=200 AC1=100000
                        ;SWP11:
002775 020076                   LDA 0,K200      ;GET 200
002776 024007                   LDA 1,K100K     ;100000 EXPECTED RESULT
002777 115320                   MOVZS 0,3               ;"S" BIT 8 TO BIT 0
003000 136004                   SUB 1,3,SZR
003001 063077                   HALT            ;FAILED EX AC2
                                SWPTS 12,K400,K1,7,15,400,1
                        ;AC0=400 AC1=1
                        ;SWP12:
003002 020100                   LDA 0,K400      ;GET 400
003003 024005                   LDA 1,K1        ;1 EXPECTED RESULT
003004 115320                   MOVZS 0,3               ;"S" BIT 7 TO BIT 15
003005 136004                   SUB 1,3,SZR
003006 063077                   HALT            ;FAILED EX AC2
                                SWPTS 13,K1000,K2,6,14,1000,2
                        ;AC0=1000 AC1=2
                        ;SWP13:
003007 020101                   LDA 0,K1000     ;GET 1000
003010 024006                   LDA 1,K2        ;2 EXPECTED RESULT
003011 115320                   MOVZS 0,3               ;"S" BIT 6 TO BIT 14
003012 136004                   SUB 1,3,SZR
003013 063077                   HALT            ;FAILED EX AC2
                                SWPTS 14,K2000,K4,5,13,2000,4
                        ;AC0=2000 AC1=4
                        ;SWP14:
003014 020102                   LDA 0,K2000     ;GET 2000
003015 024070                   LDA 1,K4        ;4 EXPECTED RESULT
003016 115320                   MOVZS 0,3               ;"S" BIT 5 TO BIT 13
```

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0054 MNLGC
003017 136004                   SUB 1,3,SZR
003020 063077                   HALT            ;FAILED EX AC2
                                SWPTS 15,K4000,K10,4,12,4000,10
                        ;AC0=4000 AC1=10
                        ;SWP15:
003021 020103                   LDA 0,K4000     ;GET 4000
003022 024072                   LDA 1,K10       ;10 EXPECTED RESULT
003023 115320                   MOVZS 0,3               ;"S" BIT 4 TO BIT 12
003024 136004                   SUB 1,3,SZR
003025 063077                   HALT            ;FAILED EX AC2
                                SWPTS 16,K10K,K20,3,11,10000,20
                        ;AC0=10000 AC1=20
                        ;SWP16:
003026 020104                   LDA 0,K10K      ;GET 10000
003027 024073                   LDA 1,K20       ;20 EXPECTED RESULT
003030 115320                   MOVZS 0,3               ;"S" BIT 3 TO BIT 11
003031 136004                   SUB 1,3,SZR
003032 063077                   HALT            ;FAILED EX AC2
                                SWPTS 17,K20K,K40,2,10,20000,40
                        ;AC0=20000 AC1=40
                        ;SWP17:
003033 020105                   LDA 0,K20K      ;GET 20000
003034 024074                   LDA 1,K40       ;40 EXPECTED RESULT
003035 115320                   MOVZS 0,3               ;"S" BIT 2 TO BIT 10
003036 136004                   SUB 1,3,SZR
003037 063077                   HALT            ;FAILED EX AC2
                                SWPTS 18,K40K,K100,1,9,40000,100
                        ;AC0=40000 AC1=100
                        ;SWP18:
003040 020106                   LDA 0,K40K      ;GET 40000
003041 024075                   LDA 1,K100      ;100 EXPECTED RESULT
003042 115320                   MOVZS 0,3               ;"S" BIT 1 TO BIT 9
003043 136004                   SUB 1,3,SZR
003044 063077                   HALT            ;FAILED EX AC2
                                SWPTS 19,K100K,K200,0,8,100000,200
                        ;AC0=100000 AC1=200
                        ;SWP19:
003045 020107                   LDA 0,K100K     ;GET 100000
003046 024076                   LDA 1,K200      ;200 EXPECTED RESULT
003047 115320                   MOVZS 0,3               ;"S" BIT 0 TO BIT 8
003050 136004                   SUB 1,3,SZR
003051 063077                   HALT            ;FAILED EX AC2
```

```
!0055 MNLGC
01                      ;DEFINE MACRO FOR NO LOAD TESTS (IR12=1)
02                      .MACRO NOLOD
03                      ;NLDA1:
04                              ADC ^2,^2       ;AC^2=-1
05                              COM# ^2,^2,SNR  ;ATTEMPT TO MAKE ZEROS
06                              COM ^2,^2,SZR   ;AC^2 SHD HAVE =-1
07                              HALT            ;AC^2 ALTERED IR12=1
08                              ADC# ^2,^2,SZR ;NOLOAD 1'S
09                              MOV ^2,^2,SZR   ;AC^2 SHD STILL=0'S
10                              HALT            ;IR12=1 DID NOT BLOCK 1'S
11                      %
12                              NOLOD 1,0
13                      ;NLD1:
14 003052 102000                ADC 0,0 ;AC0=-1
15 003053 100015                COM# 0,0,SNR    ;ATTEMPT TO MAKE ZEROS
16 003054 100004                COM 0,0,SZR     ;AC0 SHD HAVE =-1
17 003055 063077                HALT            ;AC0 ALTERED IR12=1
18 003056 102014                ADC# 0,0,SZR ;NOLOAD 1'S
19 003057 101004                MOV 0,0,SZR     ;AC0 SHD STILL=0'S
20 003060 063077                HALT            ;IR12=1 DID NOT BLOCK 1'S
21                              NOLOD 2,1
22                      ;NLD2:
23 003061 126000                ADC 1,1 ;AC1=-1
24 003062 124015                COM# 1,1,SNR    ;ATTEMPT TO MAKE ZEROS
25 003063 124004                COM 1,1,SZR     ;AC1 SHD HAVE =-1
26 003064 063077                HALT            ;AC1 ALTERED IR12=1
27 003065 126014                ADC# 1,1,SZR ;NOLOAD 1'S
28 003066 125004                MOV 1,1,SZR     ;AC1 SHD STILL=0'S
29 003067 063077                HALT            ;IR12=1 DID NOT BLOCK 1'S
30                              NOLOD 3,2
31                      ;NLD3:
32 003070 152000                ADC 2,2 ;AC2=-1
33 003071 150015                COM# 2,2,SNR    ;ATTEMPT TO MAKE ZEROS
34 003072 150004                COM 2,2,SZR     ;AC2 SHD HAVE =-1
35 003073 063077                HALT            ;AC2 ALTERED IR12=1
36 003074 152014                ADC# 2,2,SZR ;NOLOAD 1'S
37 003075 151004                MOV 2,2,SZR     ;AC2 SHD STILL=0'S
38 003076 063077                HALT            ;IR12=1 DID NOT BLOCK 1'S
39                              NOLOD 4,3
40                      ;NLD4:
41 003077 176000                ADC 3,3 ;AC3=-1
42 003100 174015                COM# 3,3,SNR    ;ATTEMPT TO MAKE ZEROS
43 003101 174004                COM 3,3,SZR     ;AC3 SHD HAVE =-1
44 003102 063077                HALT            ;AC3 ALTERED IR12=1
45 003103 176014                ADC# 3,3,SZR ;NOLOAD 1'S
46 003104 175004                MOV 3,3,SZR     ;AC3 SHD STILL=0'S
47 003105 063077                HALT            ;IR12=1 DID NOT BLOCK 1'S
```

```
!0056 MNLGC
01                      ;FIRST USE OF STA INSTRUCTION
02
03                      ;STA00:
04 003106 102000                ADC 0,0
05 003107 040133                STA 0,KTST      ;FIRST USE OF STA
06 003110 024133                LDA 1,KTST      ;FIRST LDA OF LOC "KTST"
07 003111 134004                COM 1,2,SZR     ;SKIP IF LDA GOT -1 BACK
08 003112 063077                HALT            ;LDA FROM LOC "0" IS IN AC1
09                      ;NO= STORE 0'S IN LOC KTST RETRY LDA KTST
10                      ;STA01:
11 003113 102400                SUB 0,0
12 003114 040133                STA 0,KTST      ;2ND STA IN LOC "KTST"
13 003115 024133                LDA 1,KTST      ;2ND LDA OF LOC "KTST"
14 003116 125004                MOV 1,1,SZR     ;SKP IS LDA GOT 0'S BACK
15 003117 063077                HALT
16                      ;IF EITHER OF ABOVE HALTS EXAMINE LOC CONTAINING STA
17                      ;IN CASE ADDRESSING MODE 1 ENABLED
```

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10057 MNLGC
01                      ;CONTINUATION OF LDA TESTS
02                      ;ADDRESSING MODE 01 (IR7=1 IR6=0)
03
04                    ;LDA29:
05 03120 102000               ADC 0,0           ;SET AC0=-1
06 03121 020400               LDA 0,.           ;FIRST LDA WITH IR7=1
07 03122 024110               LDA 1,KLDA,       ;GET LDA 0,, FROM PAGE 0
08 03123 100404               SUB 0,1,SZR       ;RESULT LAST 2 LOADS SHD BE=
09 03124 063077               HALT              ;LDA 0 IR7=1 FAILED
10                      ;EXPECTED RESULT IN AC0 PROBABLY LOADED LOC "0" INSTEAD
11                      ;AT THIS POINT IN TEST "LOC 0"=0
12                      ;NOW TEST FORWARD "LDA .+1" +1 OFFSET
13                    ;LDA30:
14 03125 126000               ADC 1,1
15 03126 024401               LDA 1,.+1         ;GET NEXT MEM LOC
16 03127 020400               LDA 0,.+0         ;ALSO 0=LDA 0,,
17 03130 131000               MOV 1,2           ;SAVE LDA RESULTS
18 03131 112404               SUB 0,2,SZR       ;SKP BOTH LDA'S CORRECT
19 03132 063077               HALT              ;AC0 AND 1 SHD BOTH=LDA 0,.
20                      ;USE NEGATIVE OFFEST FOR THE FIRST TIME
21                      ;NOW TEST MODE 01 NEGATIVE OFFSET OF-1
22                    ;LDA31:
23 03133 126000               ADC 1,1
24 03134 020400               LDA 0,.           ;GET THIS INST TO AC0
25 03135 024777               LDA 1,.-1         ;FIRST USE - OFFSET TO AC1
26 03136 131000               MOV 1,2           ;SAVE LDA RESULTS
27 03137 112404               SUB 0,2,SZR       ;SKP BOTH LDA'S CORRECT
28 03140 063077               HALT
29                      ;LDA ALL AC'S WITH LDA 0,, USING FORWARD OFFSETS
30                    ;LDA32:
31 03141 034403               LDA 3,.+3
32 03142 030402               LDA 2,.+2
33 03143 024401               LDA 1,.+1
34 03144 020400               LDA 0,.
35 03145 100414               SUB# 0,1,SZR
36 03146 063077               HALT              ;LDA 1,.+1 FAILED
37 03147 112414               SUB# 0,2,SZR
38 03150 063077               HALT              ;LDA 2,.+2 FAILED
39 03151 116414               SUB# 0,3,SZR
40 03152 063077               HALT              ;LDA 3,.+3 FAILED
41
42                      ;TEST LDA SEQUENCE OF - OFFSETS
43                    ;LDA33:
44 03153 020400               LDA 0,.
45 03154 024777               LDA 1,.-1
46 03155 030776               LDA 2,.-2
47 03156 034775               LDA 3,.-3
48 03157 100414               SUB# 0,1,SZR
49 03160 063077               HALT              ;LDA .-1 FAILED
50 03161 112414               SUB# 0,2,SZR
51 03162 063077               HALT              ;LDA .-2 FAILED
52 03163 116414               SUB# 0,3,SZR
53 03164 063077               HALT              ;LDA .-3 FAILED
```

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10058 MNLGC
01                      ;TEST FOR EXISTENCE OF ISZ INSTR
02                      ;FIRST USE OF ISZ INSTRUCTION
03                    ;ISZ00:
04 03165 102400               SUB 0,0
05 03166 040133               STA 0,KTST
06 03167 152000               ADC 2,2           ;SET AC2=-1 ISZ COULD=LDA OR STA
07 03170 040133               ISZ KTST          ;+1 LOC KTST SHD NOW=+1
08 03171 100001               MOV 0,1,SKP       ;ALU CRY MIGHT NOT=1
09 03172 063077               HALT              ;ISZ (0+1) SKIPPED
10 03173 024133               LDA 1,KTST        ;SEE SETSKP AND ZR SKIP
11 03174 121225               MOVZR 1,0,SNR     ;MAKE SURE ISZ RESULT
12 03175 101003               MOV 0,2,SNC       ;IS=TO+1
13 03176 063077               HALT              ;0+1 DID NOT=+1
14 03177 154004               COM 2,3,SZR
15 03200 063077               HALT              ;ISZ CHANGED AC2
16
17                      ;TEST FOR EXISTENCE OF DSZ INSTRUCTION
18                      ;-1 TO 0 IN LOC KTST SHD=-1
19                      ;FIRST USE OF DSZ INST
20                    ;DSZ00:
21 03201 176400               SUB 3,3
22 03202 040133               STA 0,KTST
23 03203 014133               DSZ KTST          ;-1 TO 0 IN LOC KTST
24 03204 100001               MOV 0,1,SKP
25 03205 063077               HALT              ;DSZ SKIPPED 0-1
26 03206 024133               LDA 1,KTST              ;GET DSZ RESULTS SHD=-1
27 03207 120004               COM 1,0,SZR
28 03210 063077               HALT              ;DSZ RESULT NOT=-1
29 03211 175004               MOV 3,3,SZR       ;AC3 SHD NOT BE DISTURBED
30 03212 063077               HALT              ;DSZ CHANGED AC3
31
32                      ;RETEST ISZ TO SKIP AND NOT CHNGE CRY
33                      ;+1 TO -1 IN LOC KTST
34                    ;ISZ01:
35 03213 102000               ADC 0,0
36 03214 040133               STA 0,KTST        ;(KTST)=-1
37 03215 111120               MOVZL 0,2         ;(AC2=-2) CRY=1
38 03216 040133               ISZ KTST          ;+1=1=SETSKIP,ZR
39 03217 063077               HALT              ;ISZ=1 DID NOT SKIP
40 03220 101003               MOV 0,0,SNC       ;TEST CALC
41 03221 063077               HALT              ;CRY OUT CHANGED CRY
42 03222 020133               LDA 0,KTST
43 03223 101004               MOV 0,0,SZR
44 03224 063077               HALT              ;(LOC 0) DID NOT=0 AFTER ISZ
45 03225 140225               COMZR 2,0,SNR     ;MAKE SURE AC2 STILL=-2
46 03226 101003               MOV 0,0,SNC
47 03227 063077               HALT              ;ISZ CHANGED AC2
```

```
10059 MNLGC
01
02
03                  ;TEST DSZ SETSKP . ZR IN SKIP LOGIC
04                 ;DSZ01:
05 03230 102520             SUBZL 0,0
06 03231 040133             STA 0,KTST          ;(LOC KTST=+1)
07 03232 114000             COM 0,3             ;(AC3=-2)
08 03233 014133             DSZ KTST            ;+1-1=SETSKP . ZR
09 03234 063077             HALT                ;DSZ DID NOT SKIP
10 03235 101002             MOV 0,0,SZC         ;TEST NOT CALC TO STOP CRYOUT
11 03236 063077             HALT                ;CRYOUT CHANGED CRY
12 03237 160225             COMZR 3,0,SNR
13 03240 101003             MOV 0,0,SNC         ;AC3 SHD STILL=-2
14 03241 063077             HALT                ;DSZ CHANGED AC3
15
16                  ;FIRST USE OF JMP INSTRUCTION JMP .+2
17 03242 020402 JMP01:      LDA 0,.+2
18 03243 115001             MOV 0,3,SKP
19 03244 003242             JMP01
20 03245 111001             MOV 0,2,SKP         ;GET TO JMP -
21 03246 000403             JMP .+3
22 03247 000777             JMP .-1
23 03250 063077             HALT
24 03251 116414             SUB# 0,3,SZR
25 03252 063077             HALT                ;JMP CHNGED AC0 OK AC3
```

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10060 MNLGC
01                  ;FIRST USE OF JSR INSTRUCTION
02
03 03253 020402 JSR00:      LDA 0,.+2
04 03254 101001             MOV 0,0,SKP
05 03255 003253             JSR00               ;ADRS THIS TEST
06 03256 004402             JSR .+2             ;FIRST USE JSR
07 03257 063077             HALT                ;JSR DID NOT CHNG PC
08 03260 024070             LDA 1,K4
09 03261 123000             ADD 1,0             ;NOW AC0 AND AC3 SHD BE=
10 03262 116414             SUB# 0,3,SZR
11 03263 063077             HALT                ;JSR FAILED TO LOAD AC3
12                  ;TEST JSR WITH NEG OFFSET
13 03264 020402 JSR01:      LDA 0,.+2
14 03265 101001             MOV 0,0,SKP
15 03266 003264             JSR01               ;ADRS THIS TEST
16 03267 111001             MOV 0,2,SKP
17 03270 000403             JMP .+3
18 03271 004777             JSR .-1             ;FIRST JSR = OFFSET
19 03272 063077             HALT                ;JSR DID NOT CHNG PC
20 03273 024071             LDA 1,K6
21 03274 123000             ADD 1,0
22 03275 116414             SUB# 0,3,SZR
23 03276 063077             HALT
24
25                  ;NOW TEST LDA USING INDEX MODE 2
26                   ;FIRST USE OF INDEXING OFFSET AND INDEX=0
27                 ;LDA34:
28 03277 102000             ADC 0,0
29 03300 040133             STA 0,KTST          ;LOC (KTST)=-1
30 03301 104000             COM 0,1               ;
31 03302 044134             STA 1,KTST+1                ;(LOC KTST+1)=0
32 03303 121400             INC 1,0
33 03304 030132             LDA 2,ADKTST        ;GET ADDR OF KTST
34 03305 155400             INC 2,3             ;AC3 = ADDR KTST +1
35 03306 025000             LDA 1,0,2
36 03307 107414             ADD# 0,1,SZR        ;AC0=+1 (AC1)=-1 IF LDA CORRECT
37 03310 063077             HALT                ;LDA 1,0,2 FAILED
38                  ;MAY HAVE USED AC3 AS INDEX (AC1) WILL=(LOC 1)
39
40                  ;TEST TO MAKE SURE EFA REALLY INDEXES MODE 2
41                 ;LDA35:
42 03311 102000             ADC 0,0
43 03312 104000             COM 0,1
44 03313 131400             INC 1,2             ;AC2=1
45 03314 155400             INC 2,3             ;AC3=2
46 03315 030132             LDA 2,ADKTST        ;GET ADDR OF KTST
47 03316 044133             STA 1,KTST          ;LOC KTST=0
48 03317 040134             STA 0,KTST+1        ;LOC KTST+1=-1
49 03320 025001             LDA 1,1,2           ;GET (LOC KTST+1) TO AC1
50 03321 106414             SUB# 0,1,SZR
51 03322 063077             HALT
```

```
10061 MNLGC
01                      ;NOW USE STA MODE 2 INDEXED
02                      ;ALSO FIRST USE OF AN LDA PAGE 0 BIT 8=1
03
04                  ;STA02:
05 03323 034072             LDA 2,K10       ;THIS LDA PREV TESTED
06 03324 051000             STA 2,0,2       ;STORE 10 IN LOC 10
07 03325 024010             LDA 1,10        ;DIRECT ACCESS 10
08 03326 132414             SUB# 1,2,SZR    ;NOT=LDA OR STA
09 03327 063077             HALT            ;COULD FAIL EFA DISPXTND
10                      ;TRY STA AGAIN WITH + OFFSET
11                      ;CONTENTS OF LOC 10 STILL=10
12                  ;STA03:
13 03330 030072             LDA 2,K10
14 03331 141400             INC 2,0
15 03332 041001             STA 0,1,2       ;11 TO LOC 11
16 03333 024011             LDA 1,11        ;GET 11 DIRECT
17 03334 122414             SUB# 1,0,SZR    ;
18 03335 063077             HALT            ;STA 0,1,2 FAILED
19
20                      ;TRY STA AGAIN WITH - OFFSET
21                  ;STA04:
22 03336 030072             LDA 2,K10
23 03337 144000             COM 2,1
24 03340 045377             STA 1,-1,2      ;COM 10 TO LOC 7
25 03341 020007             LDA 0,7         ;GET IT BACK
26 03342 106414             SUB# 0,1,SZR    ;(LOC 7) SHD=COM 10
27 03343 063077             HALT            ;STA 1,-1,2 FAILED
28
29                      ;USE STA DIRECT TO 300
30                      ;AND LDA INDEXED MODE 3 TO RETRIEVE
31
32                  ;STA05:
33 03344 034076             LDA 3,K200      ;PREP AC2 AND AC3 FOR
34 03345 030075             LDA 2,K100      ;TESTING INDEX 3 GETS AC3
35 03346 054300             STA 3,300       ;DOUBTFUL THAT DISPXTND FAILS
36 03347 160000             COM 3,0
37 03350 025500             LDA 1,100,3     ;FIRST USE OF INDEX 3
38 03351 136414             SUB# 1,3,SZR    ;AC1 AND AC3 SHD=200
39 03352 063077             HALT            ;LDA DIDN'T GET (LOC 300)
40
41                      ;TEST LDA INDEXED AC3 WITH - OFFSET
42
43                  ;STA06:
44 03353 034111             LDA 3,K300
45 03354 030076             LDA 2,K200
46 03355 160400             NEG 3,0
47 03356 044277             STA 0,277       ;-300 TO LOC 277
48 03357 025777             LDA 1,-1,3      ;LOC 277 TO AC1
49 03360 122414             SUB# 1,0,SZR    ;AC1 SHD=AC0
50 03361 063077             HALT            ;LDA 1,-1,3 FAILED
```

```
10062 MNLGC
01                      ;START TESTING AUTO INDEX AND INDIRECTS
02                      ;USING MODE 2 SAFEST WAY TO LOAD LOC 20
03                      ;AND AVOID "AUTO"
04
05                  ;STA07:
06 03362 030073             LDA 2,K20
07 03363 020100             LDA 0,K400
08 03364 114400             NEG 0,3
09 03365 041000             STA 0,0,2       ;FIRST REF MEM LOC 20
10 03366 055001             STA 3,1,2
11 03367 024020             LDA 1,20        ;FIRST DIRECT REF LOC 20
12 03370 122414             SUB# 1,0,SZR    ;AC1 0 AND LOC 20 SHD=400
13 03371 063077             HALT            ;REFERENCE LOC 20 FAILED
14                      ;AUTO ENABLED INTO SET AUTO COULD FAIL IR11=1
15                      ;(20) AC1 AND AC0 SHOULD ALL=400
16
17                      ;FIRST USE OF DEFER FOLLOWS
18                      ;NOT AUTO INDEXED COULD HANG UP VIA NOT CPB0
19                  ;STA08:
20 03372 024072             LDA 1,K10       ;PREPARE REGISTERS
21 03373 044133             STA 1,KTST      ;FOR TEST
22 03374 130400             NEG 1,2
23 03375 051010             STA 2,10        ;10=-10
24 03376 044007             STA 1,7         ;7 AND 11
25 03377 044011             STA 1,11        ;=+10
26 03400 022133             LDA 0,@KTST     ;FIRST TIME IR5=1
27 03401 112414             SUB# 0,2,SZR    ;AC2 AND AC0 SHD=-10
28 03402 063077             HALT            ;FIRST DEFER FAILED
29 03403 020133             LDA 0,KTST
30 03404 106414             SUB# 0,1,SZR    ;LOC KTST SHD=10
31 03405 063077             HALT            ;AUTO INC OR DEC LOC KTST
32                      ;AC0=11 AUTO SET PREMATURELY
```

```
10063 MNLGC
01                      ;NOW TEST DEFER VIA AUTO LOC 20
02                      ;FIRST TIME FOR AUTO
03                      ;IF IT DOESN'T CLEAR GOOD LUCK +1 INST'S STARTS
04                    ;STA09:
05 03400 024111               LDA 1,K300
06 03401 044020               STA 1,20          ;PREPARE REG'S
07 03402 120400               NEG 1,0           ;(20) 300 AND 277=300
08 03403 044301               STA 0,301         ;(301)=-300
09 03404 044300               STA 1,300
10 03405 044277               STA 1,277
11 03406 036020               LDA 3,@20         ;FIRST TIME AUTO
12 03407 116414               SUB# 0,3,SZR      ;(301) 0 AND AC3 SHD=-300
13 03410 063077               HALT              ;AUTO (@20) FAILED LDA
14 03411 030020               LDA 2,20
15 03412 125400               INC 1,1
16 03413 146414               SUB# 2,1,SZR      ;(20) SHD +1 TO=301
17 03414 063077               HALT              ;@20 DID NOT +1
18                      ;AUTO DEC COULD HAVE SET
19                      ;CONTENTS OF LOC 20 WILL=277
20                      ;OR IF DEFER CLRS PREMATURE AC3 WILL=301
21
22                      ;NOW TEST AUTO DEC @30
23                      ;FIRST TIME FOR AUTO DEC
24                    ;STA10:
25 03415 024072               LDA 1,K10         ;NEXT STA COULD HURT IR12=1
26 03416 044030               STA 1,30          ;NO SET AUTO SO AUTO DEC SHD=0
27 03417 134400               NEG 1,3           ;ALU 12 HAS=1 PREVIOUSLY THOUGH
28 03420 054007               STA 3,7           ;7=-10
29 03421 044010               STA 1,10          ;10 11=+10
30 03422 044011               STA 1,11
31 03423 022030               LDA 0,@30         ;FIRST AUTO DEC
32 03424 116414               SUB# 0,3,SZR      ;AC0 AND 3 SHD=-10
33 03425 063077               HALT              ;FIRST AUTO DEC FAILED
34 03426 020030               LDA 0,30
35 03427 115400               INC 0,3
36 03430 136414               SUB# 1,3,SZR
37 03431 063077               HALT              ;(30) NOT=7 AUTO DEC
```

```
10064 MNLGC
01                      ;CASCADE DEFERS THROUGH KTST AND KTST+1
02                      ;FIRST DEFER DEFERRED
03                    ;STA11:
04 03432 024122               LDA 1,KCOM
05 03433 020132               LDA 0,ADKTST
06 03434 123000               ADD 1,0           ;CREATE @KTST+1
07 03435 040133               STA 0,KTST        ;(LOC KTST)=@KTST+1
08 03436 024111               LDA 1,K300        ;(LOC KTST+1)=300
09 03437 044134               STA 1,KTST+1
10 03440 134400               NEG 1,3
11 03441 054300               STA 3,300         ;(300)=-300
12 03442 044301               STA 1,301         ;(301)=300
13 03443 044277               STA 1,277         ;(277)=300
14 03444 032133               LDA 2,@KTST       ;SHD ALSO DEFER @KTST+1 TO LOC 300
15 03445 156414               SUB# 2,3,SZR      ;AC2,3 SHD BOTH=-300
16 03446 063077               HALT              ;DEFER DEFERRED FAILED
```

```
10065 MNLGC
01
02                    ;STORE INDIRECT ADDRESSES IN LOCS 20-37
03                  ;STA12:
04 003455 102620      SUBZR 0,0          ;GENERATE '100000'
05 003456 030073            LDA 2,K20          ;LOAD START ADR
06 003457 030074            LDA 3,K40          ;LOAD UPPER LIMIT
07 003460 113000            ADD 0,2            ;SET INDIRECT BIT
08 003461 117000            ADD 0,3
09 003462 051000 LOOP1:     STA 2,0,2          ;STUFF LOCATION
10 003463 151400            INC 2,2
11 003464 156414            SUB# 2,3,SZR       ;DONE YET?
12 003465 000775            JMP LOOP1
13 003466 024005            LDA 1,STINC        ;UPDATE COMPLETION ADDRESSES
14 003467 044024            STA 1,24
15 003470 024023            LDA 1,STDEC
16 003471 044033            STA 1,33
17 003472 002020            JMP @20            ;START AUTO INCREMENT CHAIN TEST
18 003473 003474 STINC:     .+1
19 003474 063077            HALT               ;LOCATION 24 NOT INCREMENTED
20 003475 024002            LDA 1,C24          ;BUFFER ULIM ='100024'
21 003476 030073            LDA 2,K20
22 003477 113000            ADD 0,2            ;SET INDIRECT BIT
23 003500 030000 LOOP2:     LDA 3,0,2          ;GET UPDATED ADDRESS
24 003501 151402            INC 2,2
25 003502 156414            SUB# 2,3,SZR       ;TEST FOR INCREMENT
26 003503 063077            HALT               ;FAIL- LOCATION NOT INCREMENTED
27 003504 132414            SUB# 1,2,SZR
28 003505 000773            JMP LOOP2
29 003506 030024            LDA 3,24           ;CHECK FOR UPDATING OF DIRECT JUMP
30 003507 030064            LDA 2,STINC        ;CELLS IN AUTO INCREMENT LOCATIONS
31 003510 156014            ADC# 2,3,SZR
32 003511 063077            HALT               ;FAIL- CELL 24 NOT INCREMENTED
33 003512 002037            JMP @37            ;START AUTO DECREMENT CHAIN TEST
34 003513 003515 STDEC:     .+2
35 003514 000402            JMP .+2
36 003515 063077            HALT               ;LOCATION 30 NOT DECREMENTED
37 003516 024064            LDA 1,C37          ;LOAD ULIM ='100037'
38 003517 030063            LDA 2,C34          ;LOAD TEST BUF START ADDRESS
39 003520 030000 LOOP3:     LDA 3,0,2          ;GET UPDATED ADDRESS
40 003521 175400            INC 3,3
41 003522 156414            SUB# 2,3,SZR       ;TEST FOR DECREMENT
42 003523 063077            HALT               ;FAIL- LOCATION NOT DECREMENTED
43 003524 151400            INC 2,2
44 003525 132414            SUB# 1,2,SZR       ;TEST FOR END OF BUFFER
45 003526 000772            JMP LOOP3
46 003527 030033            LDA 3,33           ;CHECK FOR UPDATING OF DIRECT JUMP
47 003530 030063            LDA 2,STDEC        ;CELLS IN AUTO DECREMENT LOCATIONS
48 003531 172014            ADC# 3,2,SZR
49 003532 063077            HALT               ;FAIL- CELL 33 NOT DECREMENTED
50
```

```
10066 MNLGC
01                    ;TEST JMP "@" TO BLOCK SETFETCH AND 2WRADR1
02
03 003533 020402 JMP02:     LDA 0,.+2
04 003534 115001            MOV 0,3,SKP
05 003535 003533            JMP@2
06 003536 002063            JMP @JMP2L
07 003537 063077            HALT               ;JMP @ FAILED TO
08 003540 063077            HALT               ;JMP AT ALL
09 003541 103544 JMP2L:     @.+3
10 003542 063077            HALT               ;@ WAS IGNORED
11 003543 063077            HALT               ;@.+3 MAY BE SKIP ALSO
12 003544 003545            .+1
13 003545 116414            SUB# 0,3,SZR       ;AC0 OR 3 CHANGED ON A JMP@
14 003546 063077            HALT
15
16                    ;JMP SHOULD NOT GENERATE SETSKIP "JMP @"
17                  ;JMP03:
18 003547 020413            LDA 0,JM3K         ;JMP @300
19 003550 040154            STA 0,KTST+1               ;TO LOC KTST+1
20 003551 101400            INC 0,0
21 003552 040153            STA 0,KTST                 ;JMP @301 TO KTST
22 003553 024410            LDA 1,JM3K+1
23 003554 044300            STA 1,300          ;ERROR RETU TO LOC KTST
24 003555 125400            INC 1,1
25 003556 044301            STA 1,301          ;OK RETU TO LOC KTST
26 003557 002132            JMP @ADKTST
27 003560 063077            HALT
28 003561 063077            HALT
29 003562 002300 JM3K:      JMP @300
30 003563 003564            .+1
31 003564 063077            HALT               ;
32
33                    ;LDA INDEXED WITH BIT 0=1
34                    ;SHOULD NOT DEFER
35
36                  ;LDA36:
37 003565 030111            LDA 2,K300
38 003566 144400            NEG 2,1
39 003567 044301            STA 1,301
40 003570 044277            STA 1,277
41 003571 141400            INC 2,@
42 003572 040300            STA 0,300          ;@ WILL GET 301 IN ERROR
43 003573 153240            ALDUM 2,2          ;SET BIT 0=1
44 003574 035000            LDA 3,0,2          ;IR5=0 SHD NOT DEFER
45 003575 116414            SUB# 0,3,SZR
46 003576 063077            HALT               ;INDEX "CPB0" DEFERRED
```

```
;0067 MNLGC
01                      ;LDA AUTO REG 20 SHOULD NOT DEFER
02                      ;WHEN IR5=0 AND (22) BIT 0=1
03
04                  ;LDA3/:
05 03577 030073             LDA 2,K20
06 03600 034111             LDA 3,K300
07 03601 054300             STA 3,300
08 03602 054301             STA 3,301
09 03603 177240             ADDOR 3,3
10 03604 055000             STA 3,0,2
11 03605 153240             ADDOR 2,2
12 03606 021000             LDA 0,0,2
13
14                      ;JSR WITH BIT 0=1 IN INDEX REG
15                      ;SHOULD NOT DEFER AND SHD NOT
16                      ;ALLOW BIT 0 INTO AC3
17
18                  ;JSR02:
19 03607 024402             LDA 0,.+2
20 03610 101001             MOV 0,0,SKP
21 03611 003627             JS02K
22 03612 030122             LDA 2,KCOM          ;COM 0,0,SKP INSTR.
23 03613 054133             STA 2,KTST          ;TO LOC KTST=COM 0,0,SKP
24 03614 024132             LDA 1,ADKTST        ;GET ADDR OF KTST
25 03615 133000             ALD 1,2             ;GENERATE ADDR OF KTST+1+BIT0=1
26 03616 024111             LDA 1,K300
27 03617 137240             ADDOR 1,3
28 03620 044134             STA 1,KTST+1        ;0300 (TO KEEP INVALID 0)
29 03621 042300             STA 0,300           ;DEFER INCORRECT RETURN
30 03622 034121             LDA 3,KJRET         ;(JMP 0,3)
31 03623 054135             STA 3,KTST+2        ;TO GET US BACK
32 03624 100000             COM 0,0
33 03625 005377             JSR -1,2            ;(KTST+2) BIT 0=1 IR5=0 (JSR KTST)
34                      ;ABOVE JSR SHD NOT DEFER JMP 0,3 IN LOC KTST+2
35                      ;SHD BRING US BACK TO JSR +1
36 03626 175112             MOVL# 3,3,SZC       ;AC3 BIT 0 SHD=0
37 03627 063077 JS02K:      HALT                ;DEFERRED OR AC3 BIT 0=1
38 03630 126000             ADC 1,1
39 03631 107000             ADD 0,1             ;AC1=JS02K-1
40 03632 136414             SUB# 1,3,SZR        ;AC3 SHD=JSR+1
41 03633 063077             HALT                ;WRONG ADDRS IN AC3
42
```

```
;0068 MNLGC
01                      ;TEST ISZ TO NOT ALTER AC'S
02                      ;TEMP 00
03                  ;ISZ02:
04 03634 102120             ADCZL 0,0
05 03635 040133             STA 0,KTST          ;(KTST)=-2
06 03636 102400             SUB 0,0
07 03637 126400             SUB 1,1             ;AC'S ALL=0
08 03640 152400             SUB 2,2
09 03641 176400             SUB 3,3
10 03642 010133             ISZ KTST            ;(KTST)=-1
11 03643 014133             DSZ KTST            ;(KTST)=-2
12 03644 010133             ISZ KTST            ;(KTST)=-1
13 03645 010133             ISZ KTST            ;(KTST)=0
14 03646 063077             HALT                ;AC0 NOT=0 OR ISZ SKPD
15 03647 123000             ADD 1,0
16 03650 143000             ADD 2,0
17 03651 163014             ADD# 3,0,SZR
18 03652 063077             HALT                ;AC1-2-OR 3 ALTERED "ISZ"
19 03653 020133             LDA 0,KTST
20 03654 101004             MOV 0,0,SZR         ;(KTST) SHD = 0
21 03655 063077             HALT                ;ISZ KTST DID NOT CHNG (KTST)
22
23                      ;TEST AGAIN 0'S TO NOT ALTER ONES
24                  ;ISZ03:
25 03656 102400             SUB 0,0
26 03657 040133             STA 0,KTST
27 03660 100000             COM 0,0
28 03661 126000             ADC 1,1
29 03662 152000             ADC 2,2
30 03663 176040             ADCO 3,3
31 03664 010133             ISZ KTST
32 03665 010133             ISZ KTST            ;(KTST)=2
33 03666 014133             DSZ KTST            ;(KTST)=1
34 03667 175404             INC 3,3,SZR
35 03670 063077             HALT
36 03671 126000             ADC 1,3
37 03672 156003             ADC 2,3,SNC
38 03673 116014             ADC# 0,3,SZR
39 03674 063077             HALT                ;AC1=2 OR 3
40
```

```
10069 MNLOC
01                ;AUTO INCREMENT SHD NOT ALTER AC'S
02                ;TEMP IS USED FOR AUTO INC
03 03675 034132         LDA 2,ADKTST
04 03676 050023         STA 2,23
05 03677 120400         SUB 1,1
06 03700 044133         STA 1,KTST
07 03701 024115         LDA 0,KCBE      ;125252 (EVEN BITS)
08 03702 104000         COM 0,1
09 03703 111000         MOV 0,2
10 03704 154000         COM 2,3
11 03705 042023         STA 0,@23       ;125252 GOES TO LOC KTST+1
12 03706 117000         ADD 0,3
13 03707 133000         ADD 1,2
14 03710 150414         SUB# 2,3,SZR
15 03711 063077         HALT            ;AUTO INC ALTERED AN AC
16
17                ;AUTO DEC SHD NOT ALTER ANY AC
18 03712 034132         LDA 3,ADKTST
19 03713 175420         INC 3,3         ;POINT TO KTST+1
20 03714 054037         STA 3,37        ;TO AN AUTO DEC
21 03715 024116         LDA 2,KCB0      ;052525
22 03716 140040         COM 2,0
23 03717 111000         MOV 0,1
24 03720 134000         COM 1,3
25 03721 052037         STA 2,@37       ;AUTO DEC TO LOC KTST
26 03722 100414         SUB# 0,1,SZR
27 03723 063077         HALT            ;AC0 OR 1 ALTERED
28 03724 150414         SUB# 2,3,SZR
29 03725 063077         HALT            ;AC2 OR 3 ALTERED
30
31                ;AN LDA WITH IR12=1 SHD NOT "NO LOAD"
32                ;CALC=0
33
34 03726 102000         ADC 0,0
35 03727 040030         STA 0,30
36 03730 100000         COM 0,0
37 03731 020030         LDA 0,30        ;IR 12=1 SHD STILL LOAD
38 03732 100014         COM# 0,0,SZR
39 03733 063077         HALT            ;IR 12=1 STOPPED 2WEN
40
41                ;TEST OF ISZ DSZ
42              IDS01:
43 03734 020066         LDA 0,K2        ;GET VALUE OF 2
44 03735 040411         STA 0,ID01K
45 03736 010410         ISZ ID01K       ;+1
46 03737 014407         DSZ ID01K       ;-1
47 03740 014406         DSZ ID01K       ;-1
48 03741 010405         ISZ ID01K       ;+1
49 03742 024404         LDA 1,ID01K     ;SHD= AGAIN
50 03743 100414         SUB# 0,1,SZR
51 03744 063077         HALT            ;IS DS SEQ FAILED #2
52 03745 101121         MOVZL 0,0,SKP
53 03746 000000 ID01K:  0
54 03747 101004         MOV 0,0,SZR
55 03750 000765         JMP IDS01+1
56
57 03751 000471         JMP MUA00       ;JMP TO MULOV TESTS
```

```
10070 MNLOC
01                ;MULTIPLY DIVIDE TEST COMPATABLE WITH
02                ;THE MOM LOGIC TEST
03
04
05                      .MACRO LCALL
06                      JSR @A1
07                %
08                      .MACRO SETUP
09                      LCALL SETUL
10                %
11                      .MACRO LOOP
12                      LCALL LLOOP
13                %
14                      .MACRO STORE
15                      JSR @IKTOR
16                %
17                      .MACRO MULCK
18                      JSR @1MCK
19                %
20                      .MACRO DIVCK
21                      JSR @1DCK
22                %
23                      .MACRO DIVER
24                      JSR @EDIV
25                %
26                      .MACRO MULER
27                      JSR @EMUL
28                %
```

```
;0071 MNLGC
01
02                ;RANGN=RANDOM # GENERATOR
03                ;SPIN #'S OUT IN A HURRY FORGET THE MATH
04 03752 044453 RANGN:  STA 1,RN.S1
05 03753 050453         STA 2,RN.S2
06 03754 030426         LDA 2,RN.K1       ;7 FOR MASKING AT 8
07 03755 020426         LDA 0,RN.C2       ;CYCLIC CONSTANT
08 03756 024423         LDA 1,RN.C1
09 03757 133404         AND 1,2,SZR       ;ROTAT C2 EVERY 8
10 03760 000404         JMP RAN,1
11 03761 101122         MOVZL 0,0,SZC
12 03762 101400         INC 0,0
13 03763 040420         STA 0,RN.C2
14 03764 024421 RAN.1:  LDA 1,RTABL
15 03765 133000         ADD 1,2           ;TO GET NXT SUM VAR
16 03766 025000         LDA 1,0,2
17 03767 123000         ADD 1,0
18 03770 041000         STA 0,0,2         ;NEW SUM IN VAR
19 03771 024413         LDA 1,RANNM       ;LAST RAN#
20 03772 123300         ADDS 1,0
21 03773 040411         STA 0,RANNM
22 03774 030432 RAN.2:  LDA 2,RN.S2
23 03775 024430         LDA 1,RN.S1
24 03776 010403         ISZ RN.C1
25 03777 000400         JMP 0,3
26 04000 000400         JMP 0,3
27 04001 000000 RN.C1:  0
28 04002 000007 RN.K1:  7
29 04003 123456 RN.C2:  123456
30 04004 000000 RANNM:  0
31 04005 040406 RTABL:  RTABL+1
32 04006 027247          027247
33 04007 145651          145651
34 04010 162724          162724
35 04011 071352          071352
36 04012 034565          034565
37 04013 116272          116272
38 04014 047135          047135
39 04015 113523          113523
40 04016 054411 RANG3:  STA 3,RN.S3       ;FILL AC0 TO 2 WITH RAN #'S
41 04017 004733         JSR RANGN
42 04020 111000         MOV 0,2
43 04021 004731         JSR RANGN
44 04022 105000         MOV 0,1
45 04023 004727         JSR RANGN
46 04024 002403         JMP @RN.S3
47 04025 000000 RN.S1:  0
48 04026 000000 RN.S2:  0
49 04027 000000 RN.S3:  0
```

```
;0072 MNLGC
01                ;SETLP - SET UP LOOP CALL HANDLER
02                ;PERFORMS SAME FUNCTION AS SETUP IN NORMAL TSTS
03                ;ENTERED VIA JSR @SETUL
04
05 04030 054411 SETLP:  STA 3,ST.LA
06 04031 034406         LDA 3,ST.LK
07 04032 054406         STA 3,ST.LC
08 04033 002406         JMP @ST.LA
09                ;LOOPL - PERFORMS SAME FUNCTION AS LOOP
10                ;ENTERED VIA JSR @LLOUP
11
12 04034 014404 LOOPL:  ISZ ST.LC         ;SKIP IS FINI LOOP
13 04035 002404         JMP @ST.LA        ;RESTART LOOP
14 04036 001400         JMP 0,3           ;CONTINUE ON
15 04037 177774 ST.LK:  -4.
16 04040 000000 ST.LC:  0
17 04041 000000 ST.LA:  0
18
19                MDA00:  SETUP   ;0*0=0
20                        LCALL SETUL
21 04042 000143         JSR @SETUL
22                        STOKE
23 04043 006530         JSR @IXTOR
24 04044 000000         0                 ;AC0
25 04045 000000         0                 ;AC1
26 04046 000000         0                 ;AC2
27 04047 006525         JSR @MMUL
28                        MULCK
29 04050 006525         JSR @IMCK
30 04051 000000         0
31 04052 000000         0
32 04053 000000         0
33                        LOOP
34                        LCALL LLOUP
35 04054 000142         JSR @LLOUP
36
37                ;A01:
38                        SETUP
39                        LCALL SETUL
40 04055 000143         JSR @SETUL
41                        STOKE
42 04056 006515         JSR @IXTOR
43 04057 000000         0
44 04060 000000         0
45 04061 177777         -1
46 04062 006512         JSR @MMUL
47                        MULCK
48 04063 006512         JSR @IMCK
49 04064 000000         0
50 04065 000000         0
51 04066 177777         -1
52                        LOOP
53                        LCALL LLOUP
54 04067 000142         JSR @LLOUP
```

```
10073 MNLGC
01                  ;A02:
02                          SETUP
03                          LCALL SETUL
04 04070 006143             JSR @SETUL
05                          STORE
06 04071 006502             JSR @IXTOR
07 04072 000000             0
08 04073 177777             -1
09 04074 000000             0
10 04075 006477             JSR @MMUL
11                          MULCK
12 04076 006477             JSR @IMCK
13 04077 000000             0
14 04100 000000             0
15 04101 000000             0
16                          LOOP
17                          LCALL LLOOP
18 04102 006142             JSR @LLOOP
19
20                  ;A03:
21                          SETUP
22                          LCALL SETUL
23 04103 006143             JSR @SETUL
24                          STORE
25 04104 006467             JSR @IXTOR
26 04105 177777             -1
27 04106 000000             0
28 04107 000000             0
29 04110 006464             JSR @MMUL
30                          MULCK
31 04111 006464             JSR @IMCK
32 04112 000000             0
33 04113 177777             -1
34 04114 000000             0
35                          LOOP
36                          LCALL LLOOP
37 04115 006142             JSR @LLOOP
```

```
10074 MNLGC
01
02                  ;A04:
03                          SETUP
04                          LCALL SETUL
05 04116 006143             JSR @SETUL
06                          STORE
07 04117 006454             JSR @IXTOR
08 04120 000000             0
09 04121 000001             1
10 04122 177777             -1
11 04123 006451             JSR @MMUL
12                          MULCK
13 04124 006451             JSR @IMCK
14 04125 000000             0
15 04126 177777             -1
16 04127 177777             -1
17                          LOOP
18                          LCALL LLOOP
19 04130 006142             JSR @LLOOP
20
21                  ;A05:
22                          SETUP
23                          LCALL SETUL
24 04131 006143             JSR @SETUL
25                          STORE
26 04132 006441             JSR @IXTOR
27 04133 000000             0
28 04134 177777             -1
29 04135 000001             1
30 04136 006436             JSR @MMUL
31                          MULCK
32 04137 006436             JSR @IMCK
33 04140 000000             0
34 04141 177777             -1
35 04142 000001             1
36                          LOOP
37                          LCALL LLOOP
38 04143 006142             JSR @LLOOP
39
```

```
10075 MNLGC
01                ;A06:
02                        SETUP
03                        LCALL SETUL
04 04144 006143           JSR @SETUL
05                        STORE
06 04145 006426           JSR @IXTOR
07 04146 177777           -1
08 04147 177777           -1
09 04150 000000           0
10 04151 006423           JSR @MMUL
11                        MULCK
12 04152 006423           JSR @IMCK
13 04153 000000           0
14 04154 177777           -1
15 04155 000000           0
16                        LOOP
17                        LCALL LLOOP
18 04156 006142           JSR @LLOOP
19
20                ;A07:
21                        SETUP
22                        LCALL SETUL
23 04157 006143           JSR @SETUL
24                        STORE
25 04160 006413           JSR @IXTOR
26 04161 000001           1
27 04162 000002           2
28 04163 000002           2
29 04164 006410           JSR @MMUL
30                        MULCK
31 04165 006410           JSR @IMCK
32 04166 000000           0
33 04167 000005           5
34 04170 000002           2
35                        LOOP
36                        LCALL LLOOP
37 04171 006142           JSR @LLOOP
38 04172 000406           JMP MDA08
39 04173 004567 IXTOR:    SXTOR
40 04174 004602 MMUL:     XMMUL
41 04175 004345 IMCK:     MCK
42 04176 004346 IDCK:     DCK
43 04177 004614 MDIV:     XMDIV
```

```
10076 MNLGC
01                MDA08:  SETUP   ;EXPECT A DIVIDE ERROR
02                        LCALL SETUL
03 04200 006143           JSR @SETUL
04                        STORE           ;AND NO CHANGE TO ACS.
05 04201 006772           JSR @IXTOR
06 04202 000000           0
07 04203 000000           0
08 04204 000000           0
09 04205 006772           JSR @MDIV
10                        DIVCK
11 04206 006770           JSR @IDCK
12 04207 000000           0
13 04210 000000           0
14 04211 000000           0
15                        LOOP
16                        LCALL LLOOP
17 04212 006142           JSR @LLOOP
18
19                ;A09:
20                        SETUP   ;EXPECT DIVIDE ERROR.
21                        LCALL SETUL
22 04213 006143           JSR @SETUL
23                        STORE           ;NO CHANGE TO ACS.
24 04214 006757           JSR @IXTOR
25 04215 177777           -1
26 04216 177777           -1
27 04217 177777           -1
28 04220 006757           JSR @MDIV
29                        DIVCK
30 04221 006755           JSR @IDCK
31 04222 177777           -1
32 04223 177777           -1
33 04224 177777           -1
34                        LOOP
35                        LCALL LLOOP
36 04225 006142           JSR @LLOOP
37
```

```
;0077 MNLGC
01                      ;A10:
02                              SETUP   ;DIVIDE ERROR SHOULD
03                              LCALL SETUL
04 004226 000143                JSR @SETUL
05                              STORE           ;SET THE CARRY
06 004227 000744                JSR @IXTOR
07 004230 177777                -1
08 004231 177777                -1
09 004232 177777                -1
10 004233 101020                MOVZ 0,0
11 004234 000743                JSR @HDIV
12 004235 101003                MOV 0,0,SNC
13                              DIVER
14 004236 000565                JSR @EDIV
15                              LOOP
16                              LCALL LLOOP
17 004237 000142                JSR @LLOOP
18
19                      ;A11:
20                              SETUP
21                              LCALL SETUL
22 004240 000143                JSR @SETUL
23                              STORE
24 004241 000732                JSR @IXTOR
25 004242 000000                0
26 004243 000000                0
27 004244 000001                1
28 004245 000732                JSR @HDIV
29                              DIVCK
30 004246 000730                JSR @IDCK
31 004247 000000                0
32 004250 000000                0
33 004251 000001                1
34                              LOOP
35                              LCALL LLOOP
36 004252 000142                JSR @LLOOP
```

```
;0078 MNLGC
01                      ;A12:
02                              SETUP   ;NO DIVIDE ERROR SHOULD
03                              LCALL SETUL
04 004253 000143                JSR @SETUL
05                              STORE           ;OCCURE AND CARRY SHOULD
06 004254 000717                JSR @IXTOR
07 004255 000000                0               ;BE A ZERO,
08 004256 000000                0
09 004257 000001                1
10 004260 101040                MOVO 0,0
11 004261 000716                JSR @HDIV
12 004262 101002                MOV 0,0,SZC
13                              DIVER
14 004263 000600                JSR @EDIV
15                              LOOP
16                              LCALL LLOOP
17 004264 000142                JSR @LLOOP
18
19                      ;A13:
20                              SETUP   ;4/2=2
21                              LCALL SETUL
22 004265 000143                JSR @SETUL
23                              STORE
24 004266 000705                JSR @IXTOR
25 004267 000000                0
26 004270 000004                4
27 004271 000002                2
28 004272 000705                JSR @HDIV
29                              DIVCK
30 004273 000703                JSR @IDCK
31 004274 000000                0
32 004275 000002                2
33 004276 000002                2
34                              LOOP
35                              LCALL LLOOP
36 004277 000142                JSR @LLOOP
37
```

```
!0079 MNLGC
01                      ;A14:
02                              SETUP   ;CHECK REMAINDER
03                              LCALL SETUL
04 04300 000143                 JSR @SETUL
05                              STORE
06 04301 000672                 JSR @IXTOR
07 04302 000000                 0
08 04303 077777                 77777
09 04304 100000                 100000
10 04305 000672                 JSR @MDIV
11                              DIVCK
12 04306 000670                 JSR @IDCK
13 04307 077777                 77777
14 04310 000000                 0
15 04311 100000                 100000
16                              LOOP
17                              LCALL LLOOP
18 04312 000142                 JSR @LLOOP
19
20                      ;A15:
21                              SETUP
22                              LCALL SETUL
23 04313 000143                 JSR @SETUL
24                              STORE
25 04314 000657                 JSR @IXTOR
26 04315 000000                 0
27 04316 177777                 -1
28 04317 177777                 -1
29 04320 000657                 JSR @MDIV
30                              DIVCK
31 04321 000655                 JSR @IDCK
32 04322 000000                 0
33 04323 000001                 1
34 04324 177777                 -1
35                              LOOP
36                              LCALL LLOOP
37 04325 000142                 JSR @LLOOP
```

```
!0000 MNLGC
01                      ;A16:
02                              SETUP
03                              LCALL SETUL
04 04326 000143                 JSR @SETUL
05                              STORE
06 04327 000644                 JSR @IXTOR
07 04330 000001                 1
08 04331 000000                 0
09 04332 000002                 2
10 04333 000644                 JSR @MDIV
11                              DIVCK
12 04334 000642                 JSR @IDCK
13 04335 000000                 0
14 04336 100000                 100000
15 04337 000002                 2
16                              LOOP
17                              LCALL LLOOP
18 04340 000142                 JSR @LLOOP
19
20                      ;A17:
21 04341 002401                 JMP .+1
22 04342 004364                 MTST
23 04343 004627 EDIV:   DERR
24 04344 004626 EMUL:   MERR
25
26 04345 101021 MCK:    MOVZ 0,0,SKP    ;CHECK MUL RESULT
27 04346 101040 DCK:    MOVO 0,0        ;CHECK DIV RESULT
28 04347 054414                 STA 3,XCKRET
29 04350 035402                 LDA 3,2,3
30 04351 156414                 SUB# 2,3,SZR
31 04352 063077                 HALT            ;AC2 WRONG
32 04353 034410                 LDA 3,XCKRET
33 04354 031400                 LDA 2,0,3
34 04355 035401                 LDA 3,1,3
35 04356 112415                 SUB# 0,2,SNR    ;CHECK AC0
36 04357 136414                 SUB# 1,3,SZR    ;CHECK AC1
37 04360 063077                 HALT            ;ERROR
38 04361 034402                 LDA 3,XCKRET
39 04362 001403                 JMP 3,3
40
41 04363 000000 XCKRET: 0
```

```
!0001 MNLGC
01                MTST:   SETUP   ;CHECK MULTIPLY WITH
02                        LCALL SETUL
03 04364 000143           JSR @SETUL
04 04365 004520           JSR RAN
05 04366 000145           JSR @IMMUL
06 04367 020570           LDA 0,OAC
07 04370 024570           LDA 1,OMQ
08 04371 030570           LDA 2,OMD
09 04372 004535           JSR XMUL          ;PROGRAMED MULTIPLY
10 04373 036146           LDA 3,@IMMD
11 04374 156414           SUB# 2,3,SZR
12 04375 000405           JMP .+5
13 04376 030564           LDA 2,MAC
14 04377 034564           LDA 3,MMQ
15 04400 112415           SUB# 0,2,SNR
16 04401 136414           SUB# 1,3,SZR
17                        MULER             ;MULTIPLY FAILED
18 04402 000742           JSR @EMUL
19                        LOOP
20                        LCALL LLOOP
21 04403 000142           JSR @LLOOP
22
23                DTST:   SETUP   ;CHECK DIVIDE WITH
24                        LCALL SETUL
25 04404 000143           JSR @SETUL
26 04405 004500           JSR RAN ;RANDOM NUMBERS,
27 04406 000573           JSR @IMDIV        ;HARDWARE DIVIDE
28 04407 020550           LDA 0,OAC
29 04410 024550           LDA 1,OMQ
30 04411 030550           LDA 2,OMD
31 04412 004531           JSR XDIV          ;PROGRAMED DIVIDE
32 04413 034551           LDA 3,MMD
33 04414 156414           SUB# 2,3,SZR
34 04415 000405           JMP .+5
35 04416 030544           LDA 2,MAC
36 04417 034544           LDA 3,MMQ
37 04420 112415           SUB# 0,2,SNR
38 04421 136414           SUB# 1,3,SZR
39                        DIVER             ;DIVIDE FAILED
40 04422 000721           JSR @EDIV
41                        LOOP
42                        LCALL LLOOP
43 04423 000142           JSR @LLOOP
```

```
!0002 MNLGC
01 04424 020452 MDTST:    LDA 0,M100        ;MULTIPLY DIVIDE TEST
02 04425 040423           STA 0,FOB
03 04426 004457           JSR RAN
04 04427 004565           JSR XMDIV         ;HARD DIVIDE
05 04430 040447           STA 0,D0
06 04431 044447           STA 1,D1
07 04432 050447           STA 2,D2
08 04433 004547           JSR XMMUL         ;HARD MULTIPLY
09 04434 034525           LDA 3,DMD
10 04435 156414           SUB# 2,3,SZR
11 04436 000413           JMP MDT2
12 04437 030520           LDA 2,DAC
13 04440 034520           LDA 3,DMQ
14 04441 112415           SUB# 0,2,SNR
15 04442 136414           SUB# 1,3,SZR
16 04443 000406           JMP MDT2
17 04444 010404 MDT1:     ISZ FOB
18 04445 000761           JMP MDTST+2
19 04446 002401           JMP @.+1
20 04447 004630           MDTEX
21 04450 000000 FOB: 0
22 04451 020506 MDT2:     LDA 0,DAC         ;EITHER MUL OR DIV
23 04452 024506           LDA 1,DMQ         ;FAILED , TYR TO FIND
24 04453 030506           LDA 2,DMD         ;WHICH ONE,
25 04454 004467           JSR XDIV
26 04455 034422           LDA 3,D0
27 04456 116414           SUB# 0,3,SZR
28 04457 000407           JMP MDT3
29 04460 034420           LDA 3,D1
30 04461 136414           SUB# 1,3,SZR
31 04462 000404           JMP MDT3
32 04463 034416           LDA 3,D2
33 04464 156415           SUB# 2,3,SNR
34 04465 000403           JMP .+3
35                MDT3:   DIVER             ;ITS A DIVIDE ERROR
36 04466 000655           JSR @EDIV
37 04467 000755           JMP MDT1
38 04470 040467           STA 0,DAC
39 04471 044467           STA 1,DMQ
40 04472 050467           STA 2,DMD
41 04473 004434           JSR XMUL
42                        MULER             ;ITS A MULTIPLY ERR
43 04474 000650           JSR @EMUL
44 04475 000747           JMP MDT1
45 04476 177700 M100:     -100
46 04477 000000 D0: 0
47 04500 000000 D1: 0
48 04501 000000 D2: 0
```

```
10083 MNLGC
01 04502 000000 OKAC: 0
02 04503 000000 OKMQ: 0
03 04504 000000 OKMD: 0
04
05 04505 054421 RAN:    STA 3,RANRET    ;GET RANDOM OPERATORS
06              RAN1:   LCALL 4RANG
07 04506 006144         JSR @4RANG
08 04507 110700         NEGS 0,2        ;FORM MQ*MD
09 04510 105120         MOVZL 0,1
10 04511 127100         ADDL 1,1
11 04512 107300         ADDS 0,1
12 04513 112415         SUB# 0,2,SNR
13 04514 000772         JMP RAN1        ;REJECT IF AC=MD
14 04515 142432         SUBZ# 2,0,SZC
15 04516 115001         MOV 0,3,SKP
16 04517 000403         JMP .+3
17 04520 141000         MOV 2,0         ;MAKE AC LESS THAN
18 04521 171000         MOV 3,2         ;MD IN ALL CASES,
19 04522 040435 RAN2:   STA 0,OAC       ;STORE IN ORIGIONAL
20 04523 044435         STA 1,OMQ       ;NUMBER BLOCK..
21 04524 050435         STA 2,OMD
22 04525 002401         JMP @RANRET
23 04526 000000 RANRET: 0
24 04527 054436 XMUL:   STA 3,MSAV      ;PROGRAMED MULTIPLY
25 04530 034436         LDA 3,M20
26 04531 125203         MOVR 1,1,SNC
27 04532 101201         MOVR 0,0,SKP
28 04533 143220         ADDZR 2,0
29 04534 175404         INC 3,3,SZR
30 04535 000774         JMP XMUL+2
31 04536 125260         MOVCR 1,1
32 04537 040743 XMUL1:  STA 0,OKAC      ;STORE RESULTS
33 04540 044743         STA 1,OKMQ
34 04541 050743         STA 2,OKMD
35 04542 002423         JMP @MSAV
36
```

```
10084 MNLGC
01 04543 054422 XDIV:   STA 3,MSAV      ;PROGRAMED DIVIDE
02 04544 142432         SUBZ# 2,0,SZC
03 04545 001400         JMP 0,3         ;OV EXIT
04 04546 034420         LDA 3,M20
05 04547 125120         MOVZL 1,1
06 04550 101100 XDIV1:  MOVL 0,0
07 04551 142412         SUB# 2,0,SZC
08 04552 142400         SUB 2,0
09 04553 125100         MOVL 1,1
10 04554 175404         INC 3,3,SZR
11 04555 000773         JMP XDIV1
12 04556 000761         JMP XMUL1       ;STORE RESULTS.
13 04557 000000 OAC: 0
14 04560 000000 OMQ: 0
15 04561 000000 OMD: 0
16 04562 000000 HAC: 0
17 04563 000000 HMQ: 0
18 04564 000000 HMD: 0
19 04565 000000 MSAV: 0
20 04566 177760 M20: -20
21
22
23 04567 021400 SXTOR: LDA 0,0,3        ;PICK UP ARGUEMENTS
24 04570 025401         LDA 1,1,3
25 04571 031402         LDA 2,2,3
26 04572 042404         STA 0,@XOAC
27 04573 046404         STA 1,@XOMQ
28 04574 052404         STA 2,@XOMD
29 04575 001403         JMP 3,3
30 04576 004557 XOAC: OAC
31 04577 004560 XOMQ: OMQ
32 04600 004561 XOMD: OMD
33 04601 004614 IMDIV: XMDIV
34
```

```
10085 MNLGC
01
02
03 04602 054423 XHMUL:  STA 3,XHRET      ;HARDWARE MULTIPLY
04 04603 073301          MMUL
05 04604 004402          JSR .+2
06 04605 004605          .
07 04606 044754          STA 0,HAC
08 04607 020776          LDA 0,.-2
09 04610 116434          SUBZ# 0,3,SZR
10 04611 000415          JMP MERR
11 04612 020750          LDA 0,HAC
12 04613 000406          JMP XHCOM
13
14 04614 054411 XHDIV:  STA 3,XHRET      ;HARDWARE DIVIDE
15 04615 176440          SUBO 3,3
16 04616 073101          MDIV
17 04617 175004          MOV 3,3,SZR
18 04620 000407          JMP DERR
19 04621 044741 XHCOM:  STA 0,HAC        ;STORE HARDWARE RESULTS.
20 04622 044741          STA 1,HMQ
21 04623 054741          STA 2,HMD
22 04624 002401          JMP @XHRET
23 04625 000000 XHRET: 0
24
25 04626 063077 MERR:   HALT             ;MULTIPLY ERROR
26 04627 063077 DERR:   HALT             ;DIVIDE ERROR HALT
27
28              MDTEX:
29
30       000000         .NOLOC 0
```

```
10086 MNLGC
01
02              ;*******TRAP INSTRUCTION TEST ********
03
04 04630 020406 TP.00:  LDA 0,TP00R      ;PREPARE
05 04631 042061          STA 0,@TPADR     ;RETURN ADDR
06 04632 100010          TRAP             ;TRAP INSTRUCTION
07 04633 063077          HALT             ;ERROR....SHD HAVE TRAPPED
08 04634 000403          JMP .+3
09 04635 004632          .-3              ;POINT TO TRAP INSTR.
10 04636 004637 TP00R:  .+1              ;POINT TO NEXT INSTRUCTION
11 04637 026060          LDA 1,@TPLOC     ;GET PC AT TIME OF TRAP
12 04640 020775          LDA 0,.-3        ;GET TRAP ADDRESS
13 04641 122414          SUB# 1,0,SZR     ;SKP=TRAP WORKED
14 04642 063077          HALT             ;ERROR= TRAP DIDN'T WORK
15
16              ;DEFINE MACRO FOR TESTING TRAP NOT TO DISTURB AC'S
17                      .MACRO TPACT
18              TP.A1:  LDA 0,TPA1R      ;RTN ADDR
19                      STA 0,@TPADR     ;PLACE IN TRAP HANDLER LOCATION
20                      ADC #2,#2        ;SET AC#2 TO -1
21                      TRAP             ;TRAP INSTR
22                      HALT             ;TRAP DIDN'T JMP #46
23                      JMP .+2
24              TPA1R:  .+1              ;RETURN ADDR POINTER
25                      COM# #2,#2,SZR   ;SHD COM TO 0 IF STILL OK
26                      HALT             ;TRAP DISTURBED AC#2
27
28              %
29                      TPACT 01,0
30 04643 020406 TP.01:  LDA 0,TP01R      ;RTN ADDR
31 04644 042061          STA 0,@TPADR     ;PLACE IN TRAP HANDLER LOCATION
32 04645 102000          ADC 0,0 ;SET AC0 TO -1
33 04646 100010          TRAP             ;TRAP INSTR
34 04647 063077          HALT             ;TRAP DIDN'T JMP #46
35 04650 000402          JMP .+2
36 04651 004652 TP01R:  .+1              ;RETURN ADDR POINTER
37 04652 100014          COM# 0,0,SZR     ;SHD COM TO 0 IF STILL OK
38 04653 063077          HALT             ;TRAP DISTURBED AC0
39
40                      TPACT 02,1
41 04654 020406 TP.02:  LDA 0,TP02R      ;RTN ADDR
42 04655 042061          STA 0,@TPADR     ;PLACE IN TRAP HANDLER LOCATION
43 04656 126000          ADC 1,1 ;SET AC1 TO -1
44 04657 100010          TRAP             ;TRAP INSTR
45 04660 063077          HALT             ;TRAP DIDN'T JMP #46
46 04661 000402          JMP .+2
47 04662 004663 TP02R:  .+1              ;RETURN ADDR POINTER
48 04663 124014          COM# 1,1,SZR     ;SHD COM TO 0 IF STILL OK
49 04664 063077          HALT             ;TRAP DISTURBED AC1
50
51                      TPACT 03,2
52 04665 020406 TP.03:  LDA 0,TP03R      ;RTN ADDR
53 04666 042061          STA 0,@TPADR     ;PLACE IN TRAP HANDLER LOCATION
54 04667 152000          ADC 2,2 ;SET AC2 TO -1
55 04670 100010          TRAP             ;TRAP INSTR
56 04671 063077          HALT             ;TRAP DIDN'T JMP #46
57 04672 000402          JMP .+2
58 04673 004674 TP03R:  .+1              ;RETURN ADDR POINTER
59 04674 150014          COM# 2,2,SZR     ;SHD COM TO 0 IF STILL OK
60 04675 063077          HALT             ;TRAP DISTURBED AC2
```

```
 0067 MNLGC
01
02                      TPACT 04,3
03 04676 020406 TP.04:  LDA 0,TP04R     ;RTN ADDR
04 04677 042061         STA 0,@TPADR    ;PLACE IN TRAP HANDLER LOCATION
05 04700 176000         ADC 3,3 ;SET AC3 TO -1
06 04701 100010         TRAP            ;TRAP INSTR
07 04702 063077         HALT            ;TRAP DIDN'T JMP @46
08 04703 000402         JMP .+2
09 04704 004705 TP04R:  .+1             ;RETURN ADDR POINTER
10 04705 174014         COM# 3,3,SZR    ;SHD COM TO 0 IF STILL OK
11 04706 063077         HALT            ;TRAP DISTURBED AC3
12
13
14
15              ;TRY DEFERRING IN TRAP HANDLER ADDRESS
16
17 04707 020112 TP.05:  LDA 0,K0300     ;GET INDIRECT ADDR 300
18 04710 042061         STA 0,@TPADR    ;PLACE IN TRAP HANDLER LOC.
19 04711 020407         LDA 0,TP05R     ;GET RETURN ADDRESS
20 04712 040300         STA 0,300       ;PLACE IN LOC 300
21 04713 020403         LDA 0,.+3
22 04714 040301         STA 0,301       ;PUT HALT IN LOC 301
23 04715 100010         TRAP            ;TRAP INSTR.
24 04716 063077         HALT            ;ERROR HALT..DEFER TEST DIDN'T WORK
25 04717 000402         JMP .+2
26 04720 004721 TP05R:  .+1                     ;RETURN ADDRESS
```

```
10088 MNLGC
01                      ;********STACK TEST ********
02
03                      ;FIRST USE OF STACK INSTRUCTIONS(DEV01)
04                      ;TEST FOR EXISTANCE OF STACK
05 04721 126000 STK.0:  ADC 1,1         ;A MOVE FROM SP SHD
06 04722 065001         MTSP 1
07 04723 152400         SUB 2,2
08 04724 071201         MFSP 2          ;DISTURB THE DESTINATION REG
09 04725 151005         MOV 2,2,SNR
10 04726 063077         HALT            ;STACK INSTR DIDN'T LOAD AC2
11 04727 101112         MOVL# 0,0,SZC   ;CHECK FOR BIT 0 OFF
12 04730 063077         HALT            ;BIT 0 NOT 01
13                      ;IF ABOVE FAILS SEE DEV01 DECODE,STACK ROMS,NOT DCH,NOT IR9,DEV0
14                      ;AT STACK AND GATE
15
16                      ;TRY THE MOVE TO STACK POINTER/MOVE FROM STACK POINTER
17                      ;AND ALSO STACK FRAME
18                      ;
19                      ;DEFINE MACRO FOR USE IN STACK MOVE TESTS
20
21                              .MACRO STTST
22                      ST.A1:  LDA A4,A3       ;PUT A3 IN AC A4
23                              ADC A6,A6       ;SET AC A6 TO -1
24                              MOV A6,A7
25                              MOV A6,A5       ;AC A5,AC A7 = -1
26                              MTA2 A4         ;MOVE AC A4 TO A2
27                              MFA2 A5         ;READ A2 INTO AC A5
28                              SUB#A4,A5,SZR   ;CHECK RETURNED VALUE
29                              HALT            ;STACK ERROR,AC A5 SHD= AC A4
30                              COM# A6,A6,SZR  ;CHECK DISTURB OF AC A6
31                              HALT            ;MFSP A5 DISTURBED AC A6
32                              COM# A7,A7,SZR  ;CHEC AC A7
33                              HALT            ;MFA2 A5 DISTURBED AC A7
34
35                      %
36
37
38                              STTST 00,SP,K0,0,1,2,3
39 04731 020123 ST.00:  LDA 0,K0        ;PUT K0 IN AC0
40 04732 152000         ADC 2,2 ;SET AC2 TO -1
41 04733 155000         MOV 2,3
42 04734 145000         MOV 2,1 ;AC1,AC3 = -1
43 04735 061001         MTSP 0          ;MOVE AC0 TO SP
44 04736 065201         MFSP 1          ;READ SP INTO AC1
45 04737 106414         SUB#0,1,SZR     ;CHECK RETURNED VALUE
46 04740 063077         HALT            ;STACK ERROR,AC1 SHD= AC0
47 04741 150014         COM# 2,2,SZR    ;CHECK DISTURB OF AC2
48 04742 063077         HALT            ;MFSP 1 DISTURBED AC2
49 04743 174014         COM# 3,3,SZR    ;CHEC AC3
50 04744 063077         HALT            ;MFSP 1 DISTURBED AC3
51
52
53 04745 024117 ST.01:  LDA 1,K0777     ;PUT K0777 IN AC1
54 04746 176000         ADC 3,3 ;SET AC3 TO -1
55 04747 161000         MOV 3,0
56 04750 171000         MOV 3,2 ;AC2,AC0 = -1
57 04751 065001         MTSP 1          ;MOVE AC1 TO SP
58 04752 071201         MFSP 2          ;READ SP INTO AC2
59 04753 132414         SUB#1,2,SZR     ;CHECK RETURNED VALUE
60 04754 063077         HALT            ;STACK ERROR,AC2 SHD= AC1
```

```
 0089 MNLGC
01 04755 174014          COM# 3,3,SZR     ;CHECK DISTURB OF AC3
02 04756 063077          HALT             ;MFSP 2 DISTURBED AC3
03 04757 174014          COM# 0,0,SZR     ;CHEC AC0
04 04760 063077          HALT             ;MFSP 2 DISTURBED AC0
05
06                       STTST 02,SP,K100,2,3,0,1
07 04761 030075 ST.02:   LDA 2,K100       ;PUT K100 IN AC2
08 04762 102000          ADC 0,0 ;SET AC0 TO -1
09 04763 103000          MOV 0,1
10 04764 115000          MOV 0,3 ;AC3,AC1 = -1
11 04765 071001          MTSP 2           ;MOVE AC2 TO SP
12 04766 073201          MFSP 3           ;READ SP INTO AC3
13 04767 156414          SUB#2,3,SZR      ;CHECK RETURNED VALUE
14 04770 063077          HALT             ;STACK ERROR,AC3 SHD= AC2
15 04771 174014          COM# 0,0,SZR     ;CHECK DISTURB OF AC0
16 04772 063077          HALT             ;MFSP 3 DISTURBED AC0
17 04773 124014          COM# 1,1,SZR     ;CHEC AC1
18 04774 063077          HALT             ;MFSP 3 DISTURBED AC1
19
20                       STTST 03,FP,K0777,0,1,2,3
21 04775 020117 ST.03:   LDA 0,K0777      ;PUT K0777 IN AC0
22 04776 152000          ADC 2,2 ;SET AC2 TO -1
23 04777 155000          MOV 2,3
24 05000 145000          MOV 2,1 ;AC1,AC3 = -1
25 05001 060001          MTFP 0           ;MOVE AC0 TO FP
26 05002 062001          MFFP 1           ;READ FP INTO AC1
27 05003 126414          SUB#0,1,SZR      ;CHECK RETURNED VALUE
28 05004 063077          HALT             ;STACK ERROR,AC1 SHD= AC0
29 05005 154014          COM# 2,2,SZR     ;CHECK DISTURB OF AC2
30 05006 063077          HALT             ;MFSP 1 DISTURBED AC2
31 05007 174014          COM# 3,3,SZR     ;CHEC AC3
32 05010 063077          HALT             ;MFFP 1 DISTURBED AC3
33
34                       STTST 04,FP,K0,3,2,1,0
35 05011 034123 ST.04:   LDA 3,K0         ;PUT K0 IN AC3
36 05012 120000          ADC 1,1 ;SET AC1 TO -1
37 05013 121000          MOV 1,0
38 05014 131000          MOV 1,2 ;AC2,AC0 = -1
39 05015 074001          MTFP 3           ;MOVE AC3 TO FP
40 05016 072201          MFFP 2           ;READ FP INTO AC2
41 05017 172414          SUB#3,2,SZR      ;CHECK RETURNED VALUE
42 05020 063077          HALT             ;STACK ERROR,AC2 SHD= AC3
43 05021 124014          COM# 1,1,SZR     ;CHECK DISTURB OF AC1
44 05022 063077          HALT             ;MFSP 2 DISTURBED AC1
45 05023 174014          COM# 0,0,SZR     ;CHEC AC0
46 05024 063077          HALT             ;MFFP 2 DISTURBED AC0
47
48                       STTST 05,FP,K0777,1,3,2,0
49 05025 024117 ST.05:   LDA 1,K0777      ;PUT K0777 IN AC1
50 05026 152000          ADC 2,2 ;SET AC2 TO -1
51 05027 141000          MOV 2,0
52 05030 155000          MOV 2,3 ;AC3,AC0 = -1
53 05031 064001          MTFP 1           ;MOVE AC1 TO FP
54 05032 074201          MFFP 3           ;READ FP INTO AC3
55 05033 136414          SUB#1,3,SZR      ;CHECK RETURNED VALUE
56 05034 063077          HALT             ;STACK ERROR,AC3 SHD= AC1
57 05035 150014          COM# 2,2,SZR     ;CHECK DISTURB OF AC2
58 05036 063077          HALT             ;MFSP 3 DISTURBED AC2
59 05037 100014          COM# 0,0,SZR     ;CHEC AC0
60 05040 063077          HALT             ;MFFP 3 DISTURBED AC0
```

```
 0090 MNLGC
01
02                       STTST 06,FP,K1000,0,3,1,2
03 05041 020101 ST.06:   LDA 0,K1000      ;PUT K1000 IN AC0
04 05042 120000          ADC 1,1 ;SET AC1 TO -1
05 05043 131000          MOV 1,2
06 05044 135000          MOV 1,3 ;AC3,AC2 = -1
07 05045 060001          MTFP 0           ;MOVE AC0 TO FP
08 05046 074201          MFFP 3           ;READ FP INTO AC3
09 05047 116414          SUB#0,3,SZR      ;CHECK RETURNED VALUE
10 05050 063077          HALT             ;STACK ERROR,AC3 SHD= AC0
11 05051 124014          COM# 1,1,SZR     ;CHECK DISTURB OF AC1
12 05052 063077          HALT             ;MFSP 3 DISTURBED AC1
13 05053 150014          COM# 2,2,SZR     ;CHEC AC2
14 05054 063077          HALT             ;MFFP 3 DISTURBED AC2
15
16                       STTST 07,FP,K40,2,0,1,3
17 05055 030074 ST.07:   LDA 2,K40        ;PUT K40 IN AC2
18 05056 126000          ADC 1,1 ;SET AC1 TO -1
19 05057 135000          MOV 1,3
20 05060 121000          MOV 1,0 ;AC0,AC3 = -1
21 05061 070001          MTFP 2           ;MOVE AC2 TO FP
22 05062 060201          MFFP 0           ;READ FP INTO AC0
23 05063 142414          SUB#2,0,SZR      ;CHECK RETURNED VALUE
24 05064 063077          HALT             ;STACK ERROR,AC0 SHD= AC2
25 05065 124014          COM# 1,1,SZR     ;CHECK DISTURB OF AC1
26 05066 063077          HALT             ;MFSP 0 DISTURBED AC1
27 05067 174014          COM# 3,3,SZR     ;CHEC AC3
28 05070 063077          HALT             ;MFFP 0 DISTURBED AC3
29
30
```

```
10091 MNLGC
01                ;CHECK INTERREACTION OF SP AND SF MOVE INSTRUCTIONS
02
03 05071 152400 ST.08:  SUB 2,2          ;SET AC2 TO 0
04 05072 070001         MTFP 2           ;PLACE 0'S IN FP
05 05073 152000         ADC 2,2
06 05074 071001         MTSP 2           ;PUT -1 IN SP
07 05075 074201         MFFP 3           ;GET FP
08 05076 175004         MOV 3,3,SZR      ;FP SHD = 0'S
09 05077 063077         HALT             ;AC3/FP NOT= 0'S
10 05100 176400         SUB 3,3
11 05101 074001         MTFP 3           ;NOW TRY SP
12 05102 071201         MFSP 2           ;GET SP
13 05103 150134         COMZL# 2,2,SZR   ;SHD=-1 BEFORE NOW
14 05104 063077         HALT             ;WAS NOT =-1 SP/SF INTERFERNANCE
```

```
10092 MNLGC
01
02                ;SET STACK POINTER TO LOC 400
03                ; FOR THE REST OF THE TESTING
04                ;THERE SHOULD BE ANY FURTHER INTR THRU LOC 1
05                ; AFTER THE MSKO COMMAND
06
07 05105 030100           LDA 2,K400       ;GET ADDR OF 400
08 05106 071001           MTSP 2
09 05107 070001           MTFP 2           ;PUT ADDR OF 400 IN SP/SF
10 05110 102000           ADC 0,0          ;ALL BITS ON
11 05111 062077           MSKO 0           ;MASK OFF TTO/TTI
12 05112 024001           LDA 1,1          ;GET LOC 1
13 05113 044133           STA 1,KTST       ;SAVE IT IN PAGE 0
14 05114 024404           LDA 1,LC1ML      ;ADDR OF HALT
15 05115 044001           STA 1,1          ;PLACE IN LOC 1
16 05116 060177           INTEN            ;ENABLE INT FOR STACK OVERFLOW ERRORS
17 05117 000403           JMP .+3
18 05120 005121 LC1ML:    .+1
19 05121 063077           HALT             ;LOC 1 INTR WILL HALT HERE
20
21
22                ;TEST FOR EXISTANCE OF POP INSTRUCTION
23                ;PP.00:
24 05122 102400           SUB 0,0          ;TRY LOADING A VARIABLE FROM
25 05123 042100           STA 0,@K400              ;MEMORY USING POP INSTR
26 05124 102000           ADC 0,0
27 05125 061601           POP 0            ;SHD GET 0
28 05126 100004           COM 0,0,SZR      ;SHD NOT SKP IF POP WORKED
29 05127 101001           MOV 0,0,SKP      ;SKP OVER HALT
30 05130 063077           HALT             ;POP INSTR DIDN'T LOAD AC0
31
32                ;TRY POP OF -1 FROM STACK INTO AC1
33                ;PP.01:
34 05131 102000           ADC 0,0
35 05132 042100           STA 0,@K400
36 05133 030100           LDA 2,K400
37 05134 071001           MTSP 2           ;PUT 400 IN SP
38 05135 126400           SUB 1,1 ;
39 05136 061601           POP 1            ;POP -1 INTO AC1
40 05137 124014           COMM 1,1,SZR     ;SHD COM TO 0
41 05140 063077           HALT             ;POP DIDN'T LOAD AC1 WITH -1
42
43
44                ;PP.02:
45 05141 024414           LDA 1,PP02R
46 05142 044003           STA 1,3          ;IN CASE OF OVFLO
47 05143 102000           ADC 0,0
48 05144 030100           LDA 2,K400
49 05145 041001           STA 0,1,2        ;PUT -1 INTO LOC 401
50 05146 071001           MTSP 2           ;SET SP TO 400
51 05147 102400           SUB 0,0
52 05150 061401           PSH 0            ;PSH 0 ONTO STACK
53 05151 000405           JMP .+5          ;JMP OVER HALT
54 05152 063077           HALT             ;PSH SKIPPED
55 05153 000403           JMP .+3
56 05154 063077           HALT             ;OVERFLOW ERROR?
57 05155 005154 PP02R:    .-1              ;POINT TO HALT
58 05156 025001           LDA 1,1,2        ;GET PSHD DATA FROM LOC 401
59 05157 125004           MOV 1,1,SZR      ;DID PSH STORE ON STACK?
60 05160 063077           HALT             ;PSH DIDN'T WORK
```

```
 0093 MNLGC
01                      ;DEFINE MACRO FOR PSH/POP TESTING
02
03                      .MACRO PSPT
04                      ;PP.^1:
05                              LDA ^2,^3       ;GET ^3
06                              LDA ^4,PP^1E    ;STACK OVFLO ERR ADDR
07                              STA ^4,3        ;PUT IN LOC 3
08                              PSH ^2          ;PUT AC^2 ON STACK
09                              POP ^4          ;LOAD AC^4 WITH FIRST OFF THE STACK
10                              SUB# ^2,^4,SZR  ;CHECK AC^2 AGAINST AC^4
11                              HALT            ;ERROR,,AC^2 NOT EQUAL TO AC^4
12                                              ;AFTER PSH/POP
13                              JMP .+3
14                      PP^1E:  .+1
15                              HALT            ;STACK OVERFLOW ERROR HALT
16                      %
17                              PSPT 03,0,K0,1
18                      ;PP.03:
19 05161 020123                 LDA 0,K0        ;GET K0
20 05162 024007                 LDA 1,PP03E     ;STACK OVFLO ERR ADDR
21 05163 044003                 STA 1,3 ;PUT IN LOC 3
22 05164 061401                 PSH 0           ;PUT AC0 ON STACK
23 05165 065601                 POP 1           ;LOAD AC1 WITH FIRST OFF THE STACK
24 05166 106414                 SUB# 0,1,SZR    ;CHECK AC0 AGAINST AC1
25 05167 063077                 HALT            ;ERROR,,AC0 NOT EQUAL TO AC1
26                                              ;AFTER PSH/POP
27 05170 000403                 JMP .+3
28 05171 005172 PP03E:  .+1
29 05172 063077                 HALT            ;STACK OVERFLOW ERROR HALT
30                              PSPT 04,1,K2,2
31                      ;PP.04:
32 05173 024066                 LDA 1,K2        ;GET K2
33 05174 030407                 LDA 2,PP04E     ;STACK OVFLO ERR ADDR
34 05175 050003                 STA 2,3 ;PUT IN LOC 3
35 05176 065401                 PSH 1           ;PUT AC1 ON STACK
36 05177 071601                 POP 2           ;LOAD AC2 WITH FIRST OFF THE STACK
37 05200 132414                 SUB# 1,2,SZR    ;CHECK AC1 AGAINST AC2
38 05201 063077                 HALT            ;ERROR,,AC1 NOT EQUAL TO AC2
39                                              ;AFTER PSH/POP
40 05202 000403                 JMP .+3
41 05203 005204 PP04E:  .+1
42 05204 063077                 HALT            ;STACK OVERFLOW ERROR HALT
43                              PSPT 05,2,K6,3
44                      ;PP.05:
45 05205 030071                 LDA 2,K6        ;GET K6
46 05206 034007                 LDA 3,PP05E     ;STACK OVFLO ERR ADDR
47 05207 054003                 STA 3,3 ;PUT IN LOC 3
48 05210 071401                 PSH 2           ;PUT AC2 ON STACK
49 05211 073601                 POP 3           ;LOAD AC3 WITH FIRST OFF THE STACK
50 05212 156414                 SUB# 2,3,SZR    ;CHECK AC2 AGAINST AC3
51 05213 063077                 HALT            ;ERROR,,AC2 NOT EQUAL TO AC3
52                                              ;AFTER PSH/POP
53 05214 000403                 JMP .+3
54 05215 005216 PP05E:  .+1
55 05216 063077                 HALT            ;STACK OVERFLOW ERROR HALT
56                              PSPT,06,3,K40,0
57                      ;PP.06:
58 05217 034074                 LDA 3,K40       ;GET K40
59 05220 020407                 LDA 0,PP06E     ;STACK OVFLO ERR ADDR
60 05221 040003                 STA 0,3 ;PUT IN LOC 3
```

```
 0094 MNLGC
01 05222 075401                 PSH 3           ;PUT AC3 ON STACK
02 05223 061601                 POP 0           ;LOAD AC0 WITH FIRST OFF THE STACK
03 05224 102414                 SUB# 3,0,SZR    ;CHECK AC3 AGAINST AC0
04 05225 063077                 HALT            ;ERROR,,AC3 NOT EQUAL TO AC0
05                                              ;AFTER PSH/POP
06 05226 000403                 JMP .+3
07 05227 005230 PP06E:  .+1
08 05230 063077                 HALT            ;STACK OVERFLOW ERROR HALT
```

```
!0095 MNLGC
01                ;TEST PSH OVER BOUNDARY CAUSES STACK OVERFLOW ERROR
02                ;FIRST LEGAL OVERFLOW ERROR
03
04                ;PP.07:
05 05231 030077           LDA 2,K377        ;GET BOUNDARY -1
06 05232 071001           MTSP 2            ;PUT IN SP
07 05233 030006           LDA 2,STEK2       ;GET GET RETURN ADDR
08 05234 050003           STA 2,3           ;PUT IN LOC 3
09 05235 071401           PSH 2             ;PSH AC2 ON STACK/FORCE OVERFLOW
10 05236 101000           MOV 0,0
11 05237 063077           HALT              ;NO OVERFLOW , CHECK ION
12 05240 000402           JMP .+2
13 05241 005242 STEK2:    .+1
14 05242 075601           POP 3             ;GET STACKED VALUE
15 05243 156414           SUB# 2,3,SZR      ;PSH SHD HAVE COMPLETED
16 05244 063077           HALT              ;PSH DIDN'T COMPLETE STORE OF AC3
17 05245 063577           SKPBZ CPU         ;ION RESET BY OVFLO?
18 05246 063077           HALT              ;ION NOT RESET.
19 05247 060177           INTEN
20
21
22                ;TEST INC/DEC OF SP WITH PSH/POP INSTRUCTIONS
23                ;PP.08:
24 05250 030100           LDA 2,K400
25 05251 141000           MOV 2,0           ;SAVE IT
26 05252 071001           MTSP 2
27 05253 111400           INC 0,2           ;AC2= 401
28 05254 065401           PSH 1             ;PSH INSTR SHD INC SP
29 05255 075201           MFSP 3            ;CHECK IT
30 05256 156414           SUB# 2,3,SZR      ;IS IT = 401?
31 05257 063077           HALT              ;PSH DIDN'T INC SP
32 05260 065601           POP 1
33 05261 071201           MFSP 2            ;SHD BE 400 NOW
34 05262 112414           SUB# 0,2,SZR      ;IS SP = 400?
35 05263 063077           HALT              ;SP NOT DECREMENTED BY POP
```

```
!0096 MNLGC
01
02                ;SAVE / RETURN INSTRUCTION TESTS
03                ;FIRST TIME FOR SAVE INSTRUCTION
04
05                ;SV.00:
06 05264 102400           SUB 0,0           ;SET AC0 TO 0
07 05265 105400           INC 0,1           ;SET AC1 TO 1
08 05266 030100           LDA 2,K400        ;GET VALUE OF 400
09 05267 071001           MTSP 2            ;GET STACK POINTER
10 05270 070001           MTFP 2            ;SET FP TO 400
11 05271 131400           INC 1,2
12 05272 155400           INC 2,3           ;AC2=2, AC3=3
13 05273 101040           MOVO 0,0          ;SET CARRY TO 1
14 05274 062401           SAVE              ;SAVE AC'S
15 05275 175003           MOV 3,3,SNC       ;CHECK THAT CARRY STILL A 1
16 05276 063077           HALT              ;SAVE CHANGED THE CARRY BIT...ERROR
17                                          ;OR SAVE INSTR. SKIPPED...ERROR
18 05277 165000           MOV 3,1           ;PUT AC3 IN AC1
19 05300 075201           MFSP 3
20 05301 166414           SUB# 3,1,SZR      ;SP SHD = AC3
21 05302 063077           HALT              ;STACK POINTER NOT = AC3 AFTER SAVE
22 05303 074201           MFFP 3            ;GET FRAME POINTER
23 05304 166414           SUB# 3,1,SZR      ;FP SHD=AC3
24 05305 063077           HALT              ;FP NOT=AC3
25 05306 030120           LDA 2,K405        ;GET 405 INTO AC2
26 05307 146404           SUB 2,1,SZR       ;CHECK AC1 FOR PROPER VALUE OF SP
27 05310 063077           HALT              ;AC1 NOT = ORIG. SP + 5 ....ERROR HALT
28 05311 021000           LDA 0,0,2         ;DIRECTLY GET SAVED AC3 & CRY
29 05312 101103           MOVL 0,0,SNC      ;IS CRY A 1
30 05313 063077           HALT              ;SAVE INSTR DIDN'T SAVE THE CRY
31 05314 101220           MOVZR 0,0         ;REPOSITION CONTENTS
32 05315 024067           LDA 1,K3          ;AND DROP CARRY BIT
33 05316 106404           SUB 0,1,SZR       ;IS IT = 3?
34 05317 063077           HALT              ;SAVE DIDN'T STORE AC3 CORRECTLY
35 05320 021377           LDA 0,-1,2        ;GET SAVED FP
36 05321 024100           LDA 1,K400
37 05322 106414           SUB#0,1,SZR       ;FP=400 ?
38 05323 063077           HALT              ;SAVE DIDN'T STORE FP CORRECTLY
39 05324 021374           LDA 0,-4,2        ;GET SAVED AC0
40 05325 101004           MOV 0,0,SZR       ;SHD BE = 0
41 05326 063077           HALT              ;AC0 NOT = 0
42 05327 105400           INC 0,1
43 05330 021375           LDA 0,-3,2        ;GET SAVED AC1
44 05331 106414           SUB#0,1,SZR       ;AC1=1?
45 05332 063077           HALT              ;AC1 NOT SAVED CORRECTLY
46 05333 021376           LDA 0,-2,2        ;GET SAVED AC2
47 05334 125400           INC 1,1
48 05335 106414           SUB#0,1,SZR
49 05336 063077           HALT              ;AC2 NOT = 2
```

```
!0097 MNLGC
01
02                ;RTN01:
03 05337 034421           LDA 3,RTN1R      ;PUT RETURN ADDRESS IN AC3
04 05340 030100           LDA 2,K400       ;400
05 05341 071001           MTSP 2           ;INIT SP
06 05342 070001           MTFP 2           ;INIT FP
07 05343 101020           MOVZ 0,0         ;SET CARRY TO 0
08 05344 030065           LDA 2,K1         ;INIT AC2
09 05345 024072           LDA 1,K10        ;INIT AC1
10 05346 020075           LDA 0,K100       ;INIT AC0
11 05347 062401           SAVE             ;SAVE INSTRUCTION********
12 05350 102040           ADCO 0,0         ;SET CARRY TO 1,AC0 TO -1
13 05351 105000           MOV 0,1
14 05352 111000           MOV 0,2
15 05353 113000           MOV 0,3          ;SET ALL AC'S TO -1
16 05354 062601           RTRN             ;RETURN INSTRUCTION**********
17 05355 063077           HALT             ;ERROR HALT..SHD NOT GET HERE
18 05356 063077           HALT             ;IF RETURN INSTR. WORKED
19 05357 000402           JMP .+2
20 05360 005361 RTN1R:    .+1              ;RETURN ADDRESS POINTER
21 05361 054427           STA 3,SV,3       ;SAVE AC3 FOR LATER...SHD = OLD FP
22 05362 175002           MOV 3,3,SZC      ;CHECK CARRY FOR 0
23 05363 063077           HALT             ;SAVE/RETURN CHANGED CARRY..ERROR
24 05364 034065           LDA 3,K1         ;GET K1
25 05365 156414           SUB# 2,3,SZR     ;CHECK AC2
26 05366 063077           HALT             ;AC2 NOT = K1
27 05367 034072           LDA 3,K10
28 05370 136414           SUB# 1,3,SZR     ;AC1 SHD = K10
29 05371 063077           HALT             ;IT DIDN'T
30 05372 034075           LDA 3,K100
31 05373 116414           SUB# 0,3,SZR     ;AC0 SHD = K100
32 05374 063077           HALT             ;IT DIDN'T
33 05375 024100           LDA 1,K400       ;SP/FP SHD BE VALUE
34 05376 071201           MFSP 2           ;GET SP
35 05377 132404           SUB 1,2,SZR      ;CHECK SP FOR ORIG. VALUE OF 400
36 05400 063077           HALT             ;ERROR...NOT = TO 400
37 05401 070201           MFFP 2           ;GET FP
38 05402 132414           SUB# 1,2,SZR     ;CHECK FP TOO!
39 05403 063077           HALT             ;ERROR...NOT = TO 400
40 05404 024404           LDA 1,SV,3       ;GET AC3/FP THAT WAS SAVED
41 05405 132404           SUB 1,2,SZR      ;CHECK
42 05406 063077           HALT             ;OLD FP NOT = CURRENT FP
43 05407 000402           JMP .+2          ;JUMP TO NEXT TEST
44 05410 000000 SV,3:     0                ;SAVE AC3
```

```
!0098 MNLGC
01                ;STACK OVERFLO- TESTS - SAVE INSTRUCTION
02
03                ;STOV1:
04 05411 020406           LDA 0,STOVR      ;GET RETURN ADDRESS
05 05412 040003           STA 0,3          ;PLACE IT IN LOC 3
06 05413 060177           INTEN
07 05414 030100           LDA 2,K400       ;
08 05415 020066           LDA 0,K2         ;
09 05416 112401           SUB 0,2,SNP      ;FORM ADDR OF 376,ALWAS SKIP NEXT
10 05417 005424 STOVR:    STOV2
11 05420 071001           MTSP 2           ;PUT ADDR OF 376 IN SP
12 05421 062401           SAVE             ;FORCE OVER FLOW/INTERRUPT
13 05422 101000           MOV 0,0
14 05423 063077           HALT             ;IF INT. WORKS SHDN'T GET HERE
15
16                ;TRY DISABLE INT./THEN ENABLE
17
18 05424 030100 STOV2:    LDA 2,K400       ;FORM ADDR
19 05425 024066           LDA 1,K2
20 05426 132400           SUB 1,2          ;OF 376
21 05427 071001           MTSP 2           ;PUT 376 IN SP AGAIN
22 05430 020405           LDA 0,STV2R      ;GET ILLEGAL RETURN ADDR
23 05431 040003           STA 0,3          ;PLACE IN LOC 3
24 05432 060277           INTDS            ;DISABLE INT.
25 05433 062401           SAVE             ;FORCE OVERFLOW/INT. DISABLED
26 05434 000403           JMP .+3          ;JMP OVER HALT
27 05435 005436 STV2R:    .+1              ;POINT TO RETURN ADDRESS
28 05436 063077           HALT             ;ILLEGAL RETURN ADDRESS..HALT
29 05437 020406           LDA 0,STV3R      ;GET GOOD RETURN ADDRESS
30 05440 040003           STA 0,3          ;PLACE RETURN ADRESS IN LOC 3
31 05441 060177           INTEN            ;ENABLE INTERRUPTS
32 05442 101000           MOV 0,0
33 05443 063077           HALT             ;SHDN'T GET HERE IF INT. OCCURRED
34 05444 000402           JMP .+2
35 05445 005446 STV3R:    .+1              ;POINT TO RETURN ADDRESS
36 05446 063577           SKPBZ CPU        ;ION SET?
37 05447 063077           HALT             ;ION NOT RESET BY OVFLOW
38 05450 060177           INTEN
```

```
10099 MNLGC
01                ;SET UP ILLEGAL STACK OVERFLOW ADDRESS FOR REST OF TEST
02 05451 020403           LDA 0,ILLSK
03 05452 040003           STA 0,3           ;PUT IN ADDR 3
04 05453 000403           JMP .+3
05 05454 005455 ILLSK:    .+1
06 05455 063077           HALT     ;ILLEGAL STACK OVERFLOW ERROR
07
08                ;REAL TIME CLOCK TESTS
09
10 05456 020412 RT.00:    LDA 0,RT00R       ;GET ADDR FOR RETURN
11 05457 024410           LDA 1,RT00S       ;GET RETRN #2 ADDRESS
12 05460 040002           STA 0,2           ;PLACE IN LOC 2
13 05461 102400           SUB 0,0
14 05462 071077           RTCEN             ;ENABLE RTC INTERRUPTS**********
15 05463 101404           INC 0,0,SZR       ;WAIT FOR INTRP
16 05464 000777           JMP .-1
17 05465 063077           HALT              ;RTC DIDN'T INTRP
18 05466 000403           JMP .+3
19 05467 005477 RT00S:    RT.01-1
20 05470 005471 RT00R:    .+1               ;POINT TO RETURN ADDRESS
21 05471 060177           INTEN             ;INTRA ENABLE AFTER LAST INTR
22 05472 044002           STA 1,2           ;PLACE #2 RETRN IN LOC 2
23 05473 102400           SUB 0,0
24 05474 101404           INC 0,0,SZR
25 05475 000777           JMP .-1
26 05476 063077           HALT              ;2ND INTR FROM RTC DIDN'T OCCUR
27 05477 060177           INTEN             ;RE-ENABLE RTC INTERRUPT
28
29                ;CHECK REAL TIME CLOCK TIMING TEST
30
31 05500 024431 RT.01:    LDA 1,KRTC        ;GET TIMING CONSTANT
32 05501 034431           LDA 3,KRTC2       ;GET WAIT ADD, TIME
33 05502 030414           LDA 2,IRT02       ;GET GOOD RETURN ADDR,
34 05503 020430           LDA 0,ARTER       ;GET ERROR HALT ADDRESS
35 05504 040002           STA 0,2           ;PUT IN LOC 2
36 05505 125404           INC 1,1,SZR
37 05506 000777           JMP .-1           ;WAIT
38 05507 050002           STA 2,2           ;PUT IN LOC 2
39 05510 175404           INC 3,3,SZR       ;WAIT
40 05511 000777           JMP .-1           ;WAIT FOR INTERRUPT
41 05512 063077           HALT              ;INT. TOO LONG
42 05513 000404           JMP RT.02
43 05514 063077 RT.ER:    HALT              ;ERROR HALT..INT. TOO SOON
44 05515 000402           JMP RT.02
45 05516 005517 IRT02:    RT.02             ;NEXT TEST ADDRESS
46
47                ;DISABLE RTC TEST
48 05517 065077 RT.02:    RTCDS             ;DISABLE RTC
49 05520 020410           LDA 0,ARTE2       ;GET ERROR HALT ADDRESS
50 05521 040002           STA 0,2           ;PUT IN LOC 2
51 05522 024133           LDA 1,KTST        ;GET LOC 1 SAVED
52 05523 044001           STA 1,1           ;RESTORE LOC 1
53 05524 020066           LDA 0,K2          ;LOAD AC0 WITH 2
54 05525 062077           MSKO 0            ;RE-ENABLE TTO INTR
55 05526 060177           INTEN
56 05527 000406           JMP IOCK                  ;EXIT THIS TEST
57                                          ;NO MORE RTC INTERRUPTS SHD OCCUR
58 05530 005534 ARTE2: RT.E2
59 05531 177345 KRTC: -283.                 ;SET VALUE TO GIVE 1+ MILLISECONDS
60 05532 177671 KRTC2:  -71.                ;ADDITIONAL WAIT TIME
```

```
 0100 MNLGC
01 05533 005514 ARTER: RT.ER
02                ;ERROR HALT FOR RTC INTERRUPTS WHEN DISABLED
03 05534 063077 RT.E2: HALT               ;ERROR HALT...RTC SHD BE DISABLED
```

```
10101 MNLGC
01                ;CHECK TO SEE IF TIME TO START CAT/KITTEN
02
03 05535 020125 IOCK1:  LDA 0,KATSW             ;GET CAT/KITTEN FLAG
04 05536 101005         MOV 0,0,SNR             ;START IOTSTR IF = 1
05 05537 000422         JMP PROCSS              ;DO PROCESSER TESTING
06 05540 014140         DSZ PKR00               ;
07 05541 002404         JMP .+4
08 05542 024141         LDA 1,PKR01             ;GET VALUE TO RESTORE LOOP CNT
09 05543 044140         STA 1,PKR00             ;PUT IN PKR00
10 05544 101001         MOV 0,0,SKP             ;SKIP NEXT
11 05545 000504         A1A
12 05546 014126         DSZ TESTK               ;I/O TESTING DONE?
13 05547 002776         JMP .-2                 ;NOPE!
14 05550 024100         LDA 1,K400
15 05551 044126         STA 1,TESTK             ;RESTORE TEST COUNT
16 05552 020072         LDA 0,K10
17 05553 040140         STA 0,PKR00
18 05554 040141         STA 0,PKR01             ;RESTORE LOOP COUNTS
19 05555 020067         LDA 0,K3
20 05556 062077         MSKO 0                  ;MASKOUT TTO/TTI INTR
21 05557 002401         JMP .+1
22 05560 006432         PASSC                   ;PRINT PASS ON TTY
```

```
10102 MNLGC
01                ;PROCESSOR I/O INSTR TESTS
02
03 05561 102620 PROCSS: SUBZR 2,2
04 05562 060277         INTDS
05 05563 040001         STA 0,1                 ;INTA!S WILL BE 0
06                ;ION SHD=0 NO SKIP ON BUSY NON ZERO
07 05564 063477 IO.00:  SKPBN CPU               ;ION=0 SHD NOT SKP
08 05565 101001         MOV .+2,SKP
09 05566 063077         HALT                    ;IR8 IR9=00 NO SKIP BN
10                ;POWER LOW SHD=0 NO SKIP ON DONE NON ZERO
11 05567 063677 IO.01:  SKPDN CPU               ;SHD NOT SKP
12 05570 101001         MOV .+2,SKP             ;DIDN'T IR8 IR9=10
13 05571 063077         HALT                    ;SEE PWR LOW=1(SHDN'T)
14
15                ;SKPBZ TO SKP ION=0 FIRST IO SKP TRUE
16 05572 063577 IO.02:  SKPBZ CPU               ;IR8 IR9=01
17 05573 063077         HALT                    ;BUSY=0 DID NOT SKP
18                ;TEST SKPDZ POWER LOW SHD=0
19 05574 063777 IO.03:  SKPDZ CPU               ;IR8 IR9=11
20 05575 063077         HALT                    ;DONE=0 NO SKP(PWR LOW)
21                ;NIO SHD NEITHER SKP NOR ALTER ANY AC'S
22 05576 102000 IO.04:  ADC 0,0
23 05577 105000         MOV 0,1                 ;ALL AC'S=-1
24 05600 131000         MOV 1,2
25 05601 155000         MOV 2,3
26 05602 060077         NIO CPU                 ;MAKE SURE IO SKP=0
27 05603 122001         ADC 1,0,SKP
28 05604 063077         HALT                    ;NIO CPU SKIPPED
29 05605 156000         ADC 2,3
30 05606 162414         SUB# 3,0,SZR
31 05607 063077         HALT                    ;NIO CHANGED AN AC
32
33                      .MACRO IOTS1
34                ;DIA6 A2, CPU SHOULD ONLY ALTER ACA2
35                ;IO.A1:
36                      LDA A2,K5252
37                      MOV A2,A3               ;ALL AC'S=52525
38                      MOV A3,A4
39                      MOV A4,A5
40                      DIA6 A2,CPU             ;A7 A2
41                      SUB# A3,A4,SZR          ;ACA3  SHD = ACA4
42                      HALT                    ;DIA6 SKPD OR ACA3 NOT = ACA4
43                      SUB# A5,A4,SZR
44                      HALT                    ;ACA3,A4ORA5 ALTERED
45                      SUB# A2,A5,SNR          ;DID ACA2 CHANGE?
46                      HALT                    ;ACA2 NOT LOADED
47                .
48
49                      IOTS1 05,0,1,2,3,A,READS
50                ;DIA 0, CPU SHOULD ONLY ALTER AC0
51                ;IO.05:
52 05610 020114         LDA 0,K5252
53 05611 105000         MOV 0,1                 ;ALL AC'S=52525
54 05612 131000         MOV 1,2
55 05613 155000         MOV 2,3
56 05614 060477         DIA 0,CPU               ;READS 0
57 05615 132414         SUB# 1,2,SZR            ;AC1  SHD = AC2
58 05616 063077         HALT                    ;DIA SKPD OR AC1 NOT = AC2
59 05617 172414         SUB# 3,2,SZR
60 05620 063077         HALT                    ;AC1,2OR3 ALTERED
```

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 0103 MNLGC
01 05621 116415          SUB# 0,3,SNR     ;DID AC0 CHANGE?
02 05622 063077          HALT             ;AC0 NOT LOADED
03                       IOTS1 06,1,0,2,3,A,READS
04                   ;DIA 1, CPU SHOULD ONLY ALTER AC1
05                 ;IO,06:
06 05623 024114          LDA 1,K5252
07 05624 121000          MOV 1,0          ;ALL AC'S=52525
08 05625 111000          MOV 0,2
09 05626 155000          MOV 2,3
10 05627 064477          DIA 1,CPU        ;READS 1
11 05630 112414          SUB# 0,2,SZR     ;AC0  SHD = AC2
12 05631 063077          HALT             ;DIA SKPD OR AC0 NOT = AC2
13 05632 172414          SUB# 3,2,SZR
14 05633 063077          HALT             ;AC0,2OR3 ALTERED
15 05634 136415          SUB# 1,3,SNR     ;DID AC1 CHANGE?
16 05635 063077          HALT             ;AC1 NOT LOADED
17                       IOTS1 07,2,3,0,1,A,READS
18                   ;DIA 2, CPU SHOULD ONLY ALTER AC2
19                 ;IO,07:
20 05636 030114          LDA 2,K5252
21 05637 155000          MOV 2,3          ;ALL AC'S=52525
22 05640 161000          MOV 3,0
23 05641 105000          MOV 0,1
24 05642 070477          DIA 2,CPU        ;READS 2
25 05643 162414          SUB# 3,0,SZR     ;AC3  SHD = AC0
26 05644 063077          HALT             ;DIA SKPD OR AC3 NOT = AC0
27 05645 122414          SUB# 1,0,SZR
28 05646 063077          HALT             ;AC3,0OR1 ALTERED
29 05647 146415          SUB# 2,1,SNR     ;DID AC2 CHANGE?
30 05650 063077          HALT             ;AC2 NOT LOADED
31                       IOTS1 08,3,0,1,2,A,READS
32                   ;DIA 3, CPU SHOULD ONLY ALTER AC3
33                 ;IO,08:
34 05651 034114          LDA 3,K5252
35 05652 161000          MOV 3,0          ;ALL AC'S=52525
36 05653 105000          MOV 0,1
37 05654 131000          MOV 1,2
38 05655 074477          DIA 3,CPU        ;READS 3
39 05656 106414          SUB# 0,1,SZR     ;AC0  SHD = AC1
40 05657 063077          HALT             ;DIA SKPD OR AC0 NOT = AC1
41 05660 146414          SUB# 2,1,SZR
42 05661 063077          HALT             ;AC0,1OR2 ALTERED
43 05662 172415          SUB# 3,2,SNR     ;DID AC3 CHANGE?
44 05663 063077          HALT             ;AC3 NOT LOADED
45                       IOTS1 09,0,1,2,3,B,INTA
46                   ;DIB 0, CPU SHOULD ONLY ALTER AC0
47                 ;IO,09:
48 05664 020114          LDA 0,K5252
49 05665 105000          MOV 0,1          ;ALL AC'S=52525
50 05666 131000          MOV 1,2
51 05667 155000          MOV 2,3
52 05670 061477          DIB 0,CPU        ;INTA 0
53 05671 132414          SUB# 1,2,SZR     ;AC1  SHD = AC2
54 05672 063077          HALT             ;DIB SKPD OR AC1 NOT = AC2
55 05673 172414          SUB# 3,2,SZR
56 05674 063077          HALT             ;AC1,2OR3 ALTERED
57 05675 116415          SUB# 0,3,SNR     ;DID AC0 CHANGE?
58 05676 063077          HALT             ;AC0 NOT LOADED
59                       IOTS1 10,1,0,3,2,B,INTA
60                   ;DIB 1, CPU SHOULD ONLY ALTER AC1
```

```
 0104 MNLGC
01                 ;IO,10:
02 05677 024114          LDA 1,K5252
03 05700 121000          MOV 1,0          ;ALL AC'S=52525
04 05701 115000          MOV 0,3
05 05702 171000          MOV 3,2
06 05703 065477          DIB 1,CPU        ;INTA 1
07 05704 116414          SUB# 0,3,SZR     ;AC0  SHD = AC3
08 05705 063077          HALT             ;DIB SKPD OR AC0 NOT = AC3
09 05706 156414          SUB# 2,3,SZR
10 05707 063077          HALT             ;AC0,3OR2 ALTERED
11 05710 132415          SUB# 1,2,SNR     ;DID AC1 CHANGE?
12 05711 063077          HALT             ;AC1 NOT LOADED
13                       IOTS1 11,2,3,1,0,B,INTA
14                   ;DIB 2, CPU SHOULD ONLY ALTER AC2
15                 ;IO,11:
16 05712 030114          LDA 2,K5252
17 05713 155000          MOV 2,3          ;ALL AC'S=52525
18 05714 165000          MOV 3,1
19 05715 121000          MOV 1,0
20 05716 071477          DIB 2,CPU        ;INTA 2
21 05717 166414          SUB# 3,1,SZR     ;AC3  SHD = AC1
22 05720 063077          HALT             ;DIB SKPD OR AC3 NOT = AC1
23 05721 106414          SUB# 0,1,SZR
24 05722 063077          HALT             ;AC3,1OR0 ALTERED
25 05723 142415          SUB# 2,0,SNR     ;DID AC2 CHANGE?
26 05724 063077          HALT             ;AC2 NOT LOADED
27                       IOTS1 12,3,2,0,1,B,INTA
28                   ;DIB 3, CPU SHOULD ONLY ALTER AC3
29                 ;IO,12:
30 05725 034114          LDA 3,K5252
31 05726 171000          MOV 3,2          ;ALL AC'S=52525
32 05727 141000          MOV 2,0
33 05730 105000          MOV 0,1
34 05731 075477          DIB 3,CPU        ;INTA 3
35 05732 142414          SUB# 2,0,SZR     ;AC2  SHD = AC0
36 05733 063077          HALT             ;DIB SKPD OR AC2 NOT = AC0
37 05734 122414          SUB# 1,0,SZR
38 05735 063077          HALT             ;AC2,0OR1 ALTERED
39 05736 166415          SUB# 3,1,SNR     ;DID AC3 CHANGE?
40 05737 063077          HALT             ;AC3 NOT LOADED
41
```

```
0105 MNLGC
01                      ;DOB 0, CPU (MSKO 0) SHOULD NOT HANG "OUT TIME"
02                      ;OUT GOES THROUGH T/S "TQO"
03                      ;FIRST TIME FOR ANY DOA -B OR C
04                    ;IO.13:
05 05740 176000               ADC 3,3
06 05741 024066               LDA 1,K2          ;AC1 = 2
07 05742 121000               MOV 1,0
08 05743 062077               MSKO 0            ;SHD NOT SKP HALT OR ALTER AC'S
09 05744 122404               SUB 1,0,SZR
10 05745 063077               HALT              ;MSKO SKPD OR ALTERED AC0
11 05746 174004               COM 3,3,SZR
12 05747 063077               HALT              ;MSKO ALTERED AC3
13
14                      ;DETERMINE WHICH PATH TO TAKE
15                      ;IN TESTING FROM THIS POINT ON
16                      ;TTO "DONE" IS USED FOR "TRUE" INTERRUPT TESTING
17                      ;TTO DONE=0 AND BUSY=0 "FALSE" INTERRUPT TESTS
18                      ;TTO DONE=0 AND BUSY=1 LOOP BACK TO A1A
19                    IOX00:
20 05750 176000               ADC 3,3           ;SET PASS SWITCH
21 05751 063611               SKPDN TTO         ;DONE=?
22 05752 000414               JMP IOX01         ;=0
23 05753 063511               SKPBZ TTO         ;DONE=1  BUSY MUST=0
24 05754 063077               HALT              ;BUSY=0 OR DONE=1 FAILED
25 05755 063711               SKPDZ TTO         ;DONE=2 Z SHD NOT SKP
26 05756 141001               MOV 0,0,SKP
27 05757 063077               HALT              ;"DZ" ERR OR MAYBE "DN"
28 05760 063411               SKPBN TTO         ;DONE=1  BUSY CAN'T=1
29 05761 002403               JMP @IOX01=2      ;OK TO DO INTR TSTS
30 05762 063077               HALT              ;TTO IS BUSY NOT
31 05763 000765               JMP IOX00
32 05764 000203               INT00
33 05765 020504               A1A               ;START OF LOGIC TEST
34                    IOX01:
35 05766 063511               SKPBZ TTO         ;NO SKP IS WAITING
36 05767 002776               JMP @.-2          ;DON'T WAIT FOR TTO DONE
37 05770 175404               INC 3,3,SZR
38 05771 063077               HALT              ;2ND TRY
39 05772 063711               SKPDZ TTO         ;FINITE TIME TWXT "DN" AND "BZ"
40 05773 000756               JMP IOX00+1       ;MAYBE DONE=1 (TIME LAPSE)
41                      ;TTO DONE AND BUSY=0
42                      ;PERFORM TESTS THAT REQUIRE  INTERRUPT TO BE FALSE
43
44                    ;NIN00:
45 05774 172620               SUBZR 0,0
46 05775 040001               STA 0,1           ;1=00
47 05776 060177               NIOS CPU          ;1 TO ION "SHD NOT SKP"
48 05777 063477               SKPBN CPU         ;BUSY SHD=1 FOR CPU
49 06000 063077               HALT              ;ION DID NOT SET (NIOS SKPD)
50 06001 063477               SKPBN CPU         ;ION=0 HERE IS INTR
51 06002 063077               HALT              ;SEE PI AND NOT INTR
52                      ;THERE SHD BE NO INTR REQUESTS PENDING
53                      ;NIOC SHD CLR ION SKPBZ SHD NOT SKP
54                    ;NIN01:
55 06003 060177               NIOS CPU          ;1 TO ION
56 06004 063577               SKPBZ CPU         ;BUSY=1
57 06005 063477               SKPBN CPU         ;SHD NOT CLR ION
58 06006 063077               HALT              ;BZ SKPD OR BN DIDN'T
59                    ;NIN02:
60 06007 060277               NIOC CPU          ;SHD CLR ION
```

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0106 MNLGC
01 06010 063477         SKPBN CPU       ;BUSY=0
02 06011 063577         SKPBZ CPU
03 06012 063077         HALT            ;"C" DID NOT CLR ION
```

```
0107 MNLGC

                ;DOAC 0,CPU SHD CLR ION

              ;NIN03:
006013 060177         NIOS CPU
006014 061277         I.RST                   ;IORST
006015 063577         SKPBZ CPU
006016 063077         HALT              ;IORST FAILED CLR ION

                ;DOA SHD ONLY CLR IO BUS NOT ION
              ;NIN04:
006017 060177         NIOS CPU
006020 061077         DOA 0,CPU         ;NO "C" ION SHD STILL=1
006021 063477         SKPBN CPU         ;IR8,9=00 DID ION CLR
006022 063077         HALT              ;DIS CLRD ION IR8,9=00
                ;SAME TEST WITH "P" SHD NOT CLR ION IR8,9=11
              ;NIN05:
006023 060177         NIOS CPU
006024 061377         DOAP 0,CPU        ;IR8,9=11 "P" NOT "C"
006025 063477         SKPBN CPU
006026 063077         HALT              ;"P" CLRD ION
                ;"P" PULSE SHD NOT SET ION
              ;NIN06:
006027 060277         NIOC CPU
006030 060377         NIOP CPU          ;IR8,9=11 "P" NOT "S"
006031 063577         SKPBZ CPU
006032 063077         HALT              ;"P" SET ION
                ;"S" WITH ION=1 SHD LEAVE IT=1
              ;NIN07:
006033 060177         NIOS CPU          ;1 TO ION
006034 061177         DOAS 0,CPU        ;AGAIN WITH IORST
006035 063477         SKPBN CPU
006036 063077         HALT              ;2ND "S" CLRD ION
                ;ION=1 AND SKPDN ON DEV 0 SHD NOT SKIP
              ;NIN08:
006037 061277         DOAC 0,CPU
006040 060177         NIOS CPU          ;SET ION
006041 063600         SKPDN 0           ;DEV #0 SHD NOT SKP
006042 101001         MOV 0,0,SKP       ;OK
006043 063077         HALT              ;CPUINST IN IO SKIP

                ;TEST "AND'S" DECODING CPU INST FOR "FALSE"
                .MACRO IOTS2
              ;NIN^A1:
                DOAC 0,CPU
                NIOS CPU          ;SET ION FOR DEV^A2
                SKPBN ^A2         ;TEST NOT BIT ^A3
                MOV 0,0,SKP
                HALT              ;ONLY DEV 77 SHD SKP
                ;IF ABOVE HALT SEE BIT^A3 INTO "CPU INST" AND'S
                %
                IOTS2 09,76,15
              ;NIN09:
006044 061277         DOAC 0,CPU
006045 060177         NIOS CPU          ;SET ION FOR DEV76
006046 063476         SKPBN 76          ;TEST NOT BIT 15
006047 101001         MOV 0,0,SKP
006050 063077         HALT              ;ONLY DEV 77 SHD SKP
                ;IF ABOVE HALT SEE BIT15 INTO "CPU INST" AND'S
                IOTS2 10,75,14
```

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0108 MNLGC

              ;NIN10:
006051 061277         DOAC 0,CPU
006052 060177         NIOS CPU          ;SET ION FOR DEV75
006053 063475         SKPBN 75          ;TEST NOT BIT 14
006054 101001         MOV 0,0,SKP
006055 063077         HALT              ;ONLY DEV 77 SHD SKP
                ;IF ABOVE HALT SEE BIT14 INTO "CPU INST" AND'S
                IOTS2 11,73,13
              ;NIN11:
006056 061277         DOAC 0,CPU
006057 060177         NIOS CPU          ;SET ION FOR DEV73
006060 063473         SKPBN 73          ;TEST NOT BIT 13
006061 101001         MOV 0,0,SKP
006062 063077         HALT              ;ONLY DEV 77 SHD SKP
                ;IF ABOVE HALT SEE BIT13 INTO "CPU INST" AND'S
                IOTS2 12,67,12
              ;NIN12:
006063 061277         DOAC 0,CPU
006064 060177         NIOS CPU          ;SET ION FOR DEV67
006065 063467         SKPBN 67          ;TEST NOT BIT 12
006066 101001         MOV 0,0,SKP
006067 063077         HALT              ;ONLY DEV 77 SHD SKP
                ;IF ABOVE HALT SEE BIT12 INTO "CPU INST" AND'S
                IOTS2 13,57,11
              ;NIN13:
006070 061277         DOAC 0,CPU
006071 060177         NIOS CPU          ;SET ION FOR DEV57
006072 063457         SKPBN 57          ;TEST NOT BIT 11
006073 101001         MOV 0,0,SKP
006074 063077         HALT              ;ONLY DEV 77 SHD SKP
                ;IF ABOVE HALT SEE BIT11 INTO "CPU INST" AND'S
                IOTS2 14,37,10
              ;NIN14:
006075 061277         DOAC 0,CPU
006076 060177         NIOS CPU          ;SET ION FOR DEV37
006077 063437         SKPBN 37          ;TEST NOT BIT 10
006100 101001         MOV 0,0,SKP
006101 063077         HALT              ;ONLY DEV 77 SHD SKP
                ;IF ABOVE HALT SEE BIT10 INTO "CPU INST" AND'S
```

```
10109 MNLGC
01
02                      ;AN "S" PULSE WITH DEV 0 (NOT CPU INST)
03                      ;SHD NOT SET ION
04                    ;NIN15:
05 06102 061277                 DOAC 0,CPU
06 06103 060100                 NIOS 0              ;"NOT" CPU BUT "S"
07 06104 063577                 SKPBZ CPU           ;SEE 9301 GENERATING SETION
08 06105 063077                 HALT                ;ION=1 ILLEGAL (CPU INST NOT)
09
10                      ;A "C" PULSE WITH DEV 0 (NOT CPU INST) SHD NOT CLR ION
11                    ;NIN16:
12 06106 061277                 DOAC 0,CPU
13 06107 060177                 NIOS CPU
14 06110 060200                 NIOC 0              ;NOT CPU BUT "C"
15 06111 063477                 SKPBN CPU           ;ION SHD STILL=1
16 06112 063077                 HALT                ;"C" CLRD ION (NOT CPU=DEV 0)
17
18                      ;IO SKIPS SHD NOT GET TO  PTS1 "S" SHD NOT BE GEN
19                    ;NIN17:
20 06113 061277                 DOAC 0,CPU
21 06114 063577                 SKPBZ CPU           ;IR8,9=01 BUT IS NOT "S"
22 06115 063077                 HALT
23 06116 063577                 SKPBZ CPU           ;ION SHD STILL=0
24 06117 063077                 HALT                ;FIRST BZ GEN'D "S"
25
26                      ;IO SKIP "DN" SHD NOT="C" NO PTS1
27                    ;NIN18:
28 06120 060177                 NIOS CPU
29 06121 063677                 SKPDN CPU           ;IR8,9=10 BUT IS NOT "C"
30 06122 101001                 MOV 0,0,SKP         ;POWER LOW=0 SHD NOT SKP
31 06123 063077                 HALT                ;DN SKP'D WITH ION=1
32 06124 063477                 SKPBN CPU           ;ABOVE HALT SEE NOT IR8
33 06125 063077                 HALT                ;"DN" CLRD ION
34                      ;SET UP ALL CONDITIONS FOR IO SKP EXCEPT IN/OUT TIME
35                    ;NIN19:
36 06126 061277                 DOAC 0,CPU
37 06127 102420                 SUBZ 0,0
38 06130 103577                 ANDCL# 0,0,SBN      ;EVERYTHING=0 NO SKP
39 06131 101001                 MOV 0,0,SKP
40 06132 063077                 HALT                ;AND=SKPBZ CPU
41                      ;SET UP ALL CONDITIONS FOR NIOS CPU EXCEPT PTS1
42                    ;NIN20:
43 06133 061277                 DOAC 0,CPU
44 06134 102040                 ADCO 0,0
45 06135 100177                 COMCL# 0,0,SBN      ;ALL=0 NO SKP
46 06136 063577                 SKPBZ CPU           ;ION SHD STILL=0
47 06137 063077                 HALT                ;COMCL#=NIOS CPU
48
49                      ;SET UP ALL CONDITIONS FOR NIOS CPU
50                      ;EXCEPT IO ALCEN=0
51                    ;NIN21:
52 06140 061277                 DOAC 0,CPU
53 06141 020177                 LDA 0,177           ;NO IOALCEN
54 06142 063577                 SKPBZ CPU           ;SEE IOALCEN (NOT),PTS1
55 06143 063077                 HALT                ;LDA=NIOS CPU
```

```
10110 MNLGC
01                      ;SET UP ALL CONDITIONS FOR IO SKPBZ CPU EX(IN/OUT)
02                    ;NIN22:
03 06144 176400                 SUB 3,3             ;USING AN LDA
04 06145 054177                 STA 3,177           ;MAKE SURE SKP DOESN'T SET
05 06146 054000                 STA 3,0
06 06147 023577                 LDA 0,@177,3        ;ALMOST AN SKPBZ CPU
07 06150 101004                 MOV 0,0,SZR
08 06151 063077                 HALT                ;LDA=SKPBZ CPU
09 06152 014140                 DSZ PKR00
10 06153 002404                 JMP @.+4
11 06154 020141                 LDA 0,PKR01
12 06155 040140                 STA 0,PKR00
13 06156 101001                 MOV 0,0,SKP
14 06157 000504                 A1A
```

```
10111 MNLGC
01
02                  ;START DEL CODE TO TTO
03                  ;FOR INTERRUPT TESTING WHEN DONE=1
04
05                ;TTO00:
06 06160 102000           ADC 0,0           ;-1
07 06161 061111           DOAS 0,TTO        ;OUT TO TTO
08 06162 101000           MOV 0,0           ;STALL
09 06163 063511           SKPBZ TTO
10 06164 000777           JMP .-1
11 06165 061111           DOAS 0,TTO
12 06166 101000           MOV 0,0
13 06167 063411           SKPBN TTO         ;BUSY SHD=1
14 06170 063077           HALT              ;NO SKP TTO "BN"
15 06171 063511           SKPBZ TTO         ;
16 06172 100004           COM 0,0,SZR
17 06173 063077           HALT              ;TTO "BZ" ERR
18 06174 063711           SKPDZ TTO         ;DONE SHD=0 TTO
19 06175 063077           HALT              ;TTO "DZ" ERR
20 06176 063611           SKPDN TTO         ;TTO DONE SHD=0
21 06177 002403           JMP .+3           ;OK LOOP THROUGH TEST
22 06200 063077           HALT              ;TTO DONE=1 IN ERR
23 06201 000401           JMP .+1
24 06202 000504           AIA
25
26                  ;TTO DONE=1 USE TO TEST INTERRUPTS
27 06203 020416 INT00:    LDA 0,INT0K
28 06204 024137           LDA 1,JMP3K
29 06205 030066           LDA 2,K2          ;SET UP FOR
30 06206 050001           STA 2,1           ;TEST FIRST
31 06207 044002           STA 1,2           ;REAL INTERRUPT
32 06210 040300           STA 0,300
33 06211 072077           MSKO 2            ;2 MASK OUT
34 06212 176400           SUB 3,3
35 06213 054000           STA 3,0           ;0 ADRS 0
36 06214 060177           NIOS CPU          ;ION
37 06215 000401           JMP .+1           ;WAIT
38 06216 063077           HALT              ;INTERRUPT DID NOT OCCUR
39 06217 000403           JMP .+3
40 06220 006216           .-2
41 06221 006222 INT0K:    .+1
42 06222 034000           LDA 3,0
43 06223 020775           LDA 0,INT0K-1
44 06224 116414           SUB# 0,3,SZR
45 06225 063077           HALT              ;(0) NOT=NIOS+2
```

```
10112 MNLGC
01
02                  ;TEST TO MAKE SURE #IN LOC 1 WILL DEFER
03 06226 020066 INT01:    LDA 0,K2          ;AND KEEP DEFERING
04 06227 103240           ADDOR 0,0
05 06230 040001           STA 0,1           ;#2 ALSO=COM 0,0,SZC
06 06231 024137           LDA 1,JMP3K       ;JMP #300
07 06232 044003           STA 1,3           ;WILL EXECUTE IN ERR
08 06233 030415           LDA 2,INT1K       ;IF FETCH IS DIRECTLY TO 1
09 06234 050300           STA 2,300         ;OR 2ND DEFER FAILS
10 06235 151400           INC 2,2           ;LEGAL RET
11 06236 050004           STA 2,4           ;WILL BE IN 4
12 06237 103000           ADD 0,0           ;#4=COM 0,0,SZR (WON'T SKIP)
13 06240 103240           ADDOR 0,0
14 06241 040002           STA 0,2           ;#4 TO LOC 2
15 06242 101020           MOVZ 0,0          ;0 CRY JMP #300 IN0
16 06243 060177           NIOS CPU
17 06244 000401           JMP .+1           ;FIRST INTR #0
18 06245 063077           HALT
19 06246 063077           HALT
20 06247 000403           JMP .+3
21                INT1K:
22 06250 006251           .+1
23 06251 063077           HALT              ;LOC 1 OR 2 EXECUTED
24                  ;ABOVE HALT INTERRUPT IS NOT DOING #1
25                  ;OR DEFER BIT IN LOC 1 WAS NOT RECOGNIZED
26
27                  ;ION/IOF SHOULD NOT INTR
28 06252 102400 INT02:    SUB 0,0
29 06253 040000           STA 0,0
30 06254 101240           MOVOR 0,0
31 06255 040001           STA 0,1
32 06256 060177           NIOS CPU          ;ION
33 06257 060277           NIOC CPU          ;IOF
34 06260 000401           JMP .+1           ;STALL
35 06261 024000           LDA 1,0
36 06262 125004           MOV 1,1,SZR
37 06263 063077           HALT              ;INTR AFTER IOF
38
```

```
10113 MNLGC
01
02                    ;MSKO=-1 SHD NOT ALLOW TTO INTR
03 06264 102000 INT03:  ADC 0,0
04 06265 062077         MSKO 0              ;MSKO=-1
05 06266 060177         INTEN
06 06267 000401         JMP .+1             ;STALL
07 06270 024000         LDA 1,0             ;AWHILE
08 06271 063477         SKPBN CPU
09 06272 063077         HALT                ;MASKO=1 ALLOWED TTO INTR
10 06273 125004         MOV 1,1,SZR
11 06274 063077         HALT                ;LOC 0 ALTERED
12 06275 020066         LDA 0,K2            ;AC0 = 2
13 06276 072077         MSKO 2              ;2 TO MASK OUT
14 06277 000401         JMP .+1             ;STALL WAIT FOR INTR
15 06300 024000         LDA 1,0             ;INTR DID NOT OCCUR
16 06301 063577         SKPBZ CPU           ;IF BZ NO SKP
17 06302 063077         HALT
18 06303 125005         MOV 1,1,SNR         ;OR LOC0
19 06304 063077         HALT                ;WAS STILL=0
20                    ;INTERRUPT OVER A SKIP INSTRUCTION
21                    ;SHD STORE THE CORRECT ADDRESS IN LOC 0
22 06305 024410 INT04:  LDA 1,INT4K         ;RET ADRS
23 06306 044001         STA 1,1             ;TO LOC 1
24 06307 060177         NIOS CPU            ;ION
25 06310 125005         MOV 1,1,SNR         ;SET SKIP
26 06311 063077         HALT
27 06312 063077         HALT
28 06313 000403         JMP .+3
29 06314 006312         .-2
30 06315 006316 INT4K:  .+1
31 06316 101001         MOV 0,0,SKP
32 06317 063077         HALT                ;INTR SKIPD
33 06320 020000         LDA 0,0
34 06321 030773         LDA 2,INT4K-1       ;ADRS (LOC 0) SHD=
35 06322 142414         SUB# 2,0,SZR
36 06323 063077         HALT                ;(LOC 0) INCOR
37                    ;INTERRUPT OVER SKIP INST FAILED
38                    ;INTERRUPT AFTER AN I/O SKIP
39                    ;SHD STORE CORRECT RESULT IN LOC 0
40 06324 024410 INT05:  LDA 1,INT5K
41 06325 044001         STA 1,1             ;RET ADRS
42 06326 060177         NIOS CPU            ;ION
43 06327 063477         SKPBN CPU           ;IO SKIP SET SKIP
44 06330 063077         HALT
45 06331 063077         HALT
46 06332 000403         JMP .+3
47 06333 006331         .-2
48 06334 006335 INT5K:  .+1
49 06335 020000         LDA 0,0             ;INTR SKP WILL MISS THIS
50 06336 030775         LDA 2,INT5K-1       ;VALID INTR ADRS
51 06337 142414         SUB# 2,0,SZR
52 06340 063077         HALT                ;INC PC IN LOC 0
53
```

```
10114 MNLGC
01
02                    ;INTERRUPT AFTER A JSR SHD STORE
03                    ;THE CORRECT ADDRESS IN LOC 0
04 06341 030410 INT06:  LDA 2,INT6K
05 06342 050001         STA 2,1
06 06343 153240         ADDOR 2,2           ;BIT 0 OF AC2=1
07 06344 060177         NIOS CPU            ;ION JSR GOES .+2
08 06345 005375         JSR -3,2            ;JSR ADRS CALC BIT 0=1
09 06346 063077         HALT
10 06347 063077         HALT                ;JSR/INT PREVENTS
11 06350 063077         HALT                ;EITHER HALT
12 06351 006352 INT6K:  .+1
13 06352 165401         INC 3,1,SKP         ;JSR+1 SHD=INTR ADRS
14 06353 063077         HALT
15 06354 020000         LDA 0,0             ;GET (LOC 0)
16 06355 101112         MOVL# 0,0,SZC       ;BIT 0 MUST=0
17 06356 063077         HALT                ;BIT 0 LOC 0=1
18 06357 106414         SUB# 0,1,SZR        ;
19 06360 063077         HALT                ;LOC 0 OR AC3 INCORRECT
20                    ;LOC SHD=PC AFTER JSR  (JSR+2)
21                    ;AC3 SHD=PC BEFORE JSR  (JSR+1)
22                    ;NEITHER SHOULD HAVE BIT 0=1 -SEE CPB0-
23                    ;NOT JSR OR NOT ZEROBIT FORCES NOT CPB0
24 06361 102620         SUBZR 0,0           ;ACR0= '100000'
25 06362 040001         STA 0,1
26 06363 014140         DSZ PKR00
27 06364 002404         JMP @.+4
28 06365 020141         LDA 0,PKR01
29 06366 040140         STA 0,PKR00
30 06367 101001         MOV 0,0,SKP
31 06370 000504         A1A
32 06371 014126         DSZ TESTK
33 06372 000410         JMP INT07
34 06373 024124         LDA 1,K60
35 06374 044126         STA 1,TESTK
36 06375 020072         LDA 0,K10
37 06376 040140         STA 0,PKR00
38 06377 040141         STA 0,PKR01                 ;RESTORE LOOP CNT
39 06400 002401         JMP @.+1
40 06401 006432         PASSC
41
42                    ;FIRST LEVEL INTERRUPT TESTS COMPLETE
43                    ;CLR TTO DONE AND ION
44                    ;REDO NON INT TESTS
45 06402 102620 INT07:  SUBZR 0,0
46 06403 040001         STA 0,1
47 06404 101120         MOVZL 0,0
48 06405 040000         STA 0,0
49 06406 060177         NIOS CPU
50 06407 061277         I,RST               ;IORST TO ALL I/O
51 06410 000401         JMP .+1
52 06411 024000         LDA 1,0
53 06412 101004         MOV 0,0,SZR
54 06413 063077         HALT    ;IORST FAILED TO STOP INTERRUPT
55 06414 063511         SKPBZ TTO
56 06415 063077         HALT    ;IORST DID NOT MAKE TTY BUSY=0
57 06416 063411         SKPBN TTO
58 06417 101001         MOV 0,0,SKP
59 06420 063077         HALT    ;TTO BUSY SHD =0
60 06421 063711         SKPDZ TTO
```

```
 0115 MNLGC
01 06422 063077          HALT    ;TTO DONE SHD =0 IORST
02 06423 063611          SKPDN TTO
03 06424 101001          MOV 0,0,SKP
04 06425 063077          HALT
05 06426 063577          SKPBZ CPU
06 06427 063077          HALT
07 06430 002401          JMP .+1
08 06431 005564          IO,00
```

```
10116 MNLGC
01                  ;60 PASSES THROUGH INTERRUPT TESTS = PASS COMPLETE
02 06432 102400 PASSC:  SUB 0,0          ;AC0 = 0
03 06433 061111         DOAS 0,TTO       ;OUTPUT A NULL CHARACTER
04 06434 063511         SKPBZ TTO
05 06435 000777         JMP .-1
06 06436 020127         LDA 0,K215       ;TRY VARIOUS WAIT LOOPS
07 06437 061111         DOAS 0,TTO       ;OUT CAR RET
08 06440 063411         SKPBN TTO        ;BUSY SHD=1
09 06441 063077         HALT
10 06442 063711         SKPDZ TTO        ;DONE SHD=0
11 06443 063077         HALT
12 06444 063511         SKPBZ TTO        ;WAIT LOOP
13 06445 000777         JMP .-1          ;FIRST TIME THIS WAY
14 06446 063611         SKPDN TTO        ;DONE=1 IF REAL "BZ"
15 06447 063077         HALT
16                  ;NOW OUTPUT LINE FEED
17 06450 024130         LDA 1,K212
18 06451 065111         DOAS 1,TTO
19 06452 063711         SKPDZ TTO
20 06453 063077         HALT
21 06454 063411         SKPBN TTO
22 06455 063077         HALT
23 06456 063611         SKPDN TTO        ;FIRST SKPDN
24 06457 000777         JMP .-1          ;WAIT LOOP
25 06460 063511         SKPBZ TTO        ;BUSY=0 IF REAL DONE
26 06461 063077         HALT
27                  ;OUTPUT P
28 06462 030136         LDA 2,K320
29 06463 071111         DOAS 2,TTO
30 06464 063511         SKPBZ TTO        ;ION STILL=1
31 06465 000777         JMP .-1          ;WHEN IT=0 TTO DONE
32 06466 063611         SKPDN TTO        ;TTO DONE=0
33 06467 063077         HALT             ;BZ BEFORE INTR
34
```

```
0117 MNLGC
01                      ;OUTPUT "A"
02 06470 034111         LDA 3,K3P0
03 06471 024125         LDA 1,KATSW     ;GET CAT/KITTEN SW
04 06472 175400         INC 3,3
05 06473 075111         DOAS 3,TTO
06 06474 060177         INTEN
07 06475 125004         MOV 1,1,SZR     ;DON'T CHECK ION IF CAT/KITTEN RUNNING
08 06476 000403         JMP .+3
09 06477 063477         SKPBN CPU       ;ION SHD STILL=1
10 06500 063077         HALT
11 06501 020116 PASL1:  LDA 0,KC80
12 06502 120000         ADC 1,1         ;DO XOR'S
13 06503 131000         MOV 1,2         ;WHILE WAITING
14 06504 113520         ANDZL 0,2       ;ODD BITS XOR'D TO
15 06505 107000         ADD 0,1         ;-1=EVEN BITS
16 06506 146400         SUB 2,1         ;XOR'D TO -1
17 06507 152000         ADC 2,2         ;AGAIN SHOULD=
18 06510 155000         MOV 2,3         ;THE ODD BITS
19 06511 137520         ANDZL 1,3
20 06512 133000         ADD 1,2
21 06513 172400         SUB 3,2
22 06514 142414         SUB# 2,0,SZR
23 06515 063077         HALT            ;PROCESSOR ARITH ERR
24 06516 020125         LDA 0,KATSW     ;CAT/KITTEN RUNNING?
25 06517 101005         MOV 0,0,SNR     ;YES IF SKIPS
26 06520 000404         JMP .+4
27 06521 063511         SKPBZ TTO       ;WAIT FOR BUSY ZERO
28 06522 000757         JMP PASL1       ;SKIP ION CHECK
29 06523 000403         JMP .+3
30 06524 063577         SKPBZ CPU       ;INTR OCCUR YET
31 06525 000754         JMP PASL1       ;NO
32 06526 063611         SKPDN TTO       ;TTO YES DONE=1
33 06527 063077         HALT            ;NO ERROR AT "BZ"
34 06530 030131         LDA 2,K323
35 06531 071111         DOAS 2,TTO      ;OUTPUT FIRST S
36 06532 063511         SKPBZ TTO               ;WAIT FOR TTO
37 06533 000777         JMP .-1
38 06534 063611         SKPDN TTO               ;DONE SHD =1
39 06535 063077         HALT
40 06536 071111         DOAS 2,TTO              ;OUTPUT SECOND S
41 06537 063511         SKPBZ TTO
42 06540 000777         JMP .-1
43 06541 024074         LDA 1,K40
44 06542 065111         DOAS 1,TTO              ;OUT PUT A SPACE
45 06543 063511         SKPBZ TTO
46 06544 000777         JMP .-1
47 06545 060211         NIOC TTO
48
49                  ;DTOS STUFF
50 06546 034045         LDA 3,45
51 06547 021404         LDA 0,4,3
52 06550 101005         MOV 0,0,SNR
53 06551 000417         JMP NXTPAS
54 06552 020125         LDA 0,KATSW
55 06553 101005         MOV 0,0,SNR
56 06554 000417         JMP CKCAT
57 06555 034045 ATOCK:  LDA 3,45
58 06556 021400         LDA 0,0,3
59 06557 101005         MOV 0,0,SNR     ;SKP IS AUTO MODE
60 06560 000410         JMP NXTPAS
```

```
0118 MNLGC
01 06561 035403         DSZ 3,3
02 06562 000406         JMP NXTPAS
03 06563 061277         I.RST
04 06564 021403         LDA 0,3,3
05 06565 034404         LDA 3,4,3       ;GET DTOS RETURN ADDR
06 06566 041776         STA 0,-2,3
07 06567 001400         JMP 0,3                 ;RETURN TO DTOS
08 06570 060177 NXTPAS: INTEN
09 06571 000401         JMP #,+1
10 06572 000504         A1A
```

```
!0119 MNLGC
01
02                ;CKCAT-CHECK IF DTOS RUN WITH CAT/KITTEN
03 06573 021402 CKCAT:  LDA 0,2,3
04 06574 101065         MOV 0,0,SNR     ;SKP IS WITH CAT/KTTN
05 06575 000760         JMP ATOCK       ;NO CAT/KTTN
06 06576 040125         STA 0,KATSW
07 06577 020100         LDA 0,K400
08 06600 040126         STA 0,TESTK     ;SETUP LOOP #
09 06601 035404         LDA 3,4,3
10 06602 030404         LDA 2,K1377
11 06603 150400         SUB 2,3
12 06604 000400         JSR 0,3
13 06605 000750         JMP ATOCK
14 06606 001377 K1377: 1377
15
16 06607 047115 DIRT:   .TXTE ;MNLGCT   001
17       000000         .NOLOC 0
18 06615 000000         0
19 06616 000200         200
20 06617 176774         176774
21 06620 000000         0
22 06621 000000         0
23 06622 000000         0
24 06623 000000         0
25 06624 000000         0
26 06625 147703         .TXTE ;COPYRIGHT (C) DATA GENERAL CORPORATION, 1976
27 06653 146101 ALL RIGHTS RESERVED.
28 06665 047056 .NOLOC 0
29 06671 027011         .END    AAA
```

```
!0120 MNLGC

**000000 TOTAL ERRORS, 00000 PASS 1 ERRORS
```

```
                    117/02
K32Ø   ØØØ13Ø         5/1Ø   116/28
K323   ØØØ131         5/Ø4   117/34
K377   ØØØØ77         4/22   95/Ø5
K4     ØØØØ7Ø         4/15   52/54   53/59   6Ø/Ø8
K4Ø    ØØØØ74         4/19   53/18   54/23   65/Ø6   9Ø/17   93/58   117/43
K4ØØ   ØØØ1ØØ         4/23   16/17   19/56   52/39   53/42   62/Ø7   92/Ø7
                     92/25   92/35   92/36   92/48   95/24   96/Ø8   96/36
                     97/Ø4   97/33   98/Ø7   98/18   1Ø1/14  119/Ø7
K4ØØØ  ØØØ1Ø3         4/26   53/Ø3   54/Ø6
K4Ø5   ØØØ12Ø         4/39   96/25
K4ØK   ØØØ1Ø8         4/29   53/27   54/3Ø
K5252  ØØØ114         4/35   51/Ø3   51/Ø6   1Ø2/52  1Ø3/Ø6  1Ø3/2Ø  1Ø3/34
                    1Ø3/48  1Ø4/Ø2  1Ø4/16  1Ø4/3Ø
K6     ØØØØ71         4/16   6Ø/2Ø   93/45
K6Ø    ØØØ124         4/43   114/34
KATSW  ØØØ125         4/44    5/46   1Ø1/Ø3  117/Ø3  117/24  117/54  119/Ø6
KCBE   ØØØ115         4/36   69/Ø7
KCBO   ØØØ116         4/37   69/21   117/11
KCOM   ØØØ122         4/41   64/Ø4   67/22
KD3ØØ  ØØØ112         4/33   67/17
KJRET  ØØØ121         4/4Ø   67/3Ø
KLDA,  ØØØ11Ø         4/31   57/Ø7
KRTC   ØØ5531        99/31   99/59
KRTC2  ØØ5532        99/32   99/6Ø
KTST   ØØØ133         5/Ø5    5/Ø6   56/Ø5   56/Ø6   56/12   56/13   58/Ø5
                     58/Ø7   58/1Ø   58/22   58/23   58/26   58/36   58/38
                     58/42   59/Ø6   59/Ø8   6Ø/29   6Ø/31   6Ø/47   ØØ/48
                     62/21   62/26   62/29   64/Ø7   64/Ø9   64/14   66/19
                     66/21   67/23   67/28   67/31   68/Ø5   68/1Ø   68/11
                     68/12   68/13   68/19   68/26   68/31   68/32   68/33
                     69/Ø6   92/13   99/51
LC1ML  ØØ5129        92/14   92/18
LCALL  ØØØ511  MC    7Ø/Ø5   72/2Ø   72/34   72/39   72/53   73/Ø3   73/17
                     73/22   73/36   74/Ø4   74/18   74/23   74/37   75/Ø3
                     75/17   75/22   75/36   76/Ø2   76/16   76/21   76/35
                     77/Ø3   77/16   77/21   77/35   78/Ø3   78/16   78/21
                     78/35   79/Ø3   79/17   79/22   79/36   8Ø/Ø3   8Ø/17
                     81/Ø2   81/2Ø   81/24   81/42   83/Ø6
LDAT1  ØØØ412  MC    49/19   49/31   49/41   49/51   5Ø/Ø1
LLOOP  ØØØ142         5/14   72/35   72/54   73/18   73/37   74/19   74/38
                     75/18   75/37   76/17   76/36   77/17   77/36   78/17
                     78/36   79/18   79/37   8Ø/18   81/21   81/43
LOOP   ØØØ515  MC    7Ø/11   72/33   72/52   73/16   73/35   74/17   74/36
                     75/16   75/35   76/15   76/34   77/15   77/34   78/15
                     78/34   79/16   79/35   8Ø/16   81/19   81/41
LOOP1  Ø03462        65/Ø9   65/12
LOOP2  Ø03500        65/23   65/28
LOOP3  Ø3520         65/39   65/45
LOOPL  Ø04Ø34         5/14   72/12
M1ØØ   ØØ4476        82/Ø1   82/45
M2Ø    ØØ4566        83/25   84/Ø4   84/2Ø
MCK    Ø04345        75/41   8Ø/26
MDA0Ø  ØØ4Ø42        69/57   72/19
MDA08  Ø04200        75/38   76/Ø1
MDT1   ØØ4444        82/17   82/37   82/44
MDT2   ØØ4451        82/11   82/16   82/22
MDT3   ØØ446Ø        82/28   82/31   82/35
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MDTEX  ØØ463Ø        82/2Ø   85/28
MDTST  ØØ4424        82/Ø1   82/16
MERR   ØØ462Ø        8Ø/24   85/1Ø   85/25
MSAV   ØØ4365        83/24   83/35   84/Ø1   84/19
MTST   ØØ4364        8Ø/22   81/Ø1
MULCK  ØØØ521  MC    7Ø/17   72/28   72/47   73/11   73/3Ø   74/12   74/31
                     75/11   75/3Ø
MULER  ØØØ527  MC    7Ø/2Ø   81/17   82/42
NEGTS  ØØØ231  MC    35/25   36/Ø9   36/25   36/41   36/57   37/13   37/29
                     37/45   38/Ø1   38/17   38/33   38/49   39/Ø5   39/21
                     39/37   39/53   4Ø/Ø9
NOCAT  ØØØ17Ø         5/27
NOLOD  ØØØ45Ø  MC    55/Ø2   55/12   55/21   55/3Ø   55/39
NXTPA  ØØ657Ø       117/53  117/6Ø  118/Ø2  118/Ø8
OAC    Ø04557        81/Ø6   81/28   82/12   82/22   82/38   83/19   84/13
                     84/3Ø
OKAC   Ø04502        83/Ø1   83/32
OKMD   Ø04504        83/Ø3   83/34
OKMQ   Ø04503        83/Ø2   83/33
OMD    Ø04561        81/Ø8   81/3Ø   82/Ø9   82/24   82/4Ø   83/21   84/15
                     84/32
OMQ    Ø04Ø6Ø        81/Ø7   81/29   82/13   82/23   82/39   83/2Ø   84/14
                     84/31
PASL1  ØØ65Ø1       117/11  117/28  117/31
PASSC  ØØ6432       1Ø1/22  114/4Ø  116/Ø2
PKRØØ  ØØØ14Ø         5/12    5/46  1Ø1/Ø6  1Ø1/Ø9  1Ø1/17  11Ø/Ø9  11Ø/12
                    114/26  114/29  114/37
PKRØ1  ØØØ141         5/13    5/49  1Ø1/Ø8  1Ø1/18  11Ø/11  114/28  114/38
PP02R  Ø05155        92/45   92/57
PP03E  Ø05171        93/2Ø   93/28
PP04E  Ø05203        93/33   93/41
PP05E  Ø05215        93/46   93/54
PP06E  Ø05227        93/59   94/Ø7
PRCSS  Ø05561       1Ø1/Ø5  1Ø2/Ø3
PSPT   ØØØ641  MC    93/Ø3   93/17   93/3Ø   93/43   93/56
RAN    Ø04505        81/Ø4   81/2Ø   82/Ø3   83/Ø5
RAN1   Ø04506        83/Ø6   83/13
RAN2   Ø64522        83/19
RANG3  Ø04Ø16        71/4Ø
RANGN  Ø03752         5/16   71/Ø4   71/41   71/43   71/45
RANNM  Ø04004        71/19   71/21   71/3Ø
RANRE  Ø04526        83/Ø5   83/22   83/23
RAN.1  Ø03764        71/1Ø   71/14
RAN.2  Ø03774        71/22
RESTR  ØØØ47Ø         5/31    5/35    5/45
RN.C1  Ø04ØØ1        71/Ø8   71/24   71/27
RN.C2  Ø04ØØ3        71/Ø7   71/13   71/29
RN.K1  Ø04ØØ2        71/Ø6   71/28
RN.S1  Ø04Ø25        71/Ø4   71/23   71/47
RN.S2  Ø04Ø26        71/Ø5   71/22   71/48
RN.S3  Ø04Ø27        71/4Ø   71/46   71/49
RT0ØR  Ø05470        99/1Ø   99/2Ø
RT0ØS  Ø05467        99/11   99/19
RTABL  Ø04ØØ5        71/14   71/31
RTN1R  Ø05366        97/Ø3   97/2Ø
RT.Ø0  Ø0545Ø        99/16
RT.Ø1  Ø055ØØ        99/19   99/31
RT.Ø2  Ø05517        99/42   99/44   99/45   99/48
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