

**DB11-A
bus repeater
manual**

1st Printing October 1971
2nd Printing January 1972

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FOREWORD

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the DB11-A Bus Repeater. The level of discussion assumes that the user is familiar with basic digital computer theory and basic PDP-11 operation.

Although PDP-11 Unibus signals and data are transferred through the DB11, this manual does not cover operation of the PDP-11 System or the Unibus. A detailed description of the PDP-11 is presented in a set of *PDP-11/20 Manuals*, DEC-11-HR1A-D through DEC-11-HR7A-D; a detailed description of the Unibus is presented in the *PDP-11 Unibus Interface Manual*, DEC-11-HIAA-D.

This manual is supplied with each DB11. Throughout this manual various engineering drawings are referenced. A reduced set of engineering drawings is contained in a separate document entitled *DB11-A Bus Repeater Engineering Drawings*. This document reflects the updated drawings for the DB11 at the time the equipment is shipped and is to be used in conjunction with the *DB11-A Bus Repeater Manual*.

This manual is divided into four chapters:

- a.* general description
- b.* installation planning
- c.* detailed description
- d.* maintenance

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The PDP-11 Unibus is capable of handling 18 unit loads (including a DB11-A). The DB11-A Bus Repeater (hereafter referred to as DB11) allows the Unibus to be extended beyond 20 unit loads. An additional 18 unit loads can be attached to the Unibus using the bus repeater. The bus repeater does not affect the bus cycle time (it adds zero time) of any device before the DB11, and it adds a maximum of 375 ns to the cycle time of devices addressed beyond the bus repeater. Though the Unibus is bidirectional, the DB11 is not *symmetrical*, and therefore, the processor must be on the input side (or left side) of the repeater. This is necessitated by certain one-direction Unibus signals that are implemented in only one direction by the DB11. All signals that must be bidirectional are implemented by the bus repeater.

1.2 FUNCTIONAL DESCRIPTION

The DB11 is a non-programmable device that interfaces two buses (left and right) in four sections:

- a. Bus Repeater Control
- b. Bus D (data) Lines
- c. Bus A (address) Lines
- d. Bus Unidirectional Lines.

For a detailed description of the Unibus lines refer to the *PDP-11 Unibus Interface Manual*, DEC-11-HIAB-D. Figure 1-1 shows the DB11 interfacing two buses or bus sections (refer to Table 3-1 for Unibus signals). The unidirectional lines are directly interfaced; the signals between the buses are independently interfaced. The D and A lines interface data and addresses on the bus through enabling signals generated in the Bus Repeater Control. Thus, the Unibus is controlled through the DB11 Bus Repeater Control.

The DB11 Bus Repeater Control uses the Bus Busy (BBSY) signal of the Unibus as the master controlling signal of the DB11 logic. The DB11 buffers the BBSY signal, enabling it to be bidirectional between the input and output bus. The BBSY signal is used to determine the direction to enable the bus address (A) line circuits. Because the bus master is always asserting the A lines on the bus, the direction of BBSY through the DB11 enabling logic directs the bus A lines through the bus repeater. The BBSY signal combines with bus control line 1 (C1) and the interrupt bus signal (INTR) to determine the direction of the bus D lines. For a DATI bus operation (bus C1 and C0 both a zero), the bus D lines are enabled by the DB11 toward the bus master device. For an INTR signal the bus D lines are enabled by the DB11 to the processor. Slave Sync (SSYN) is enabled through a bidirectional circuit. All one-direction bus signals are gated through the logic without a determination of direction by the DB11. These signals are:

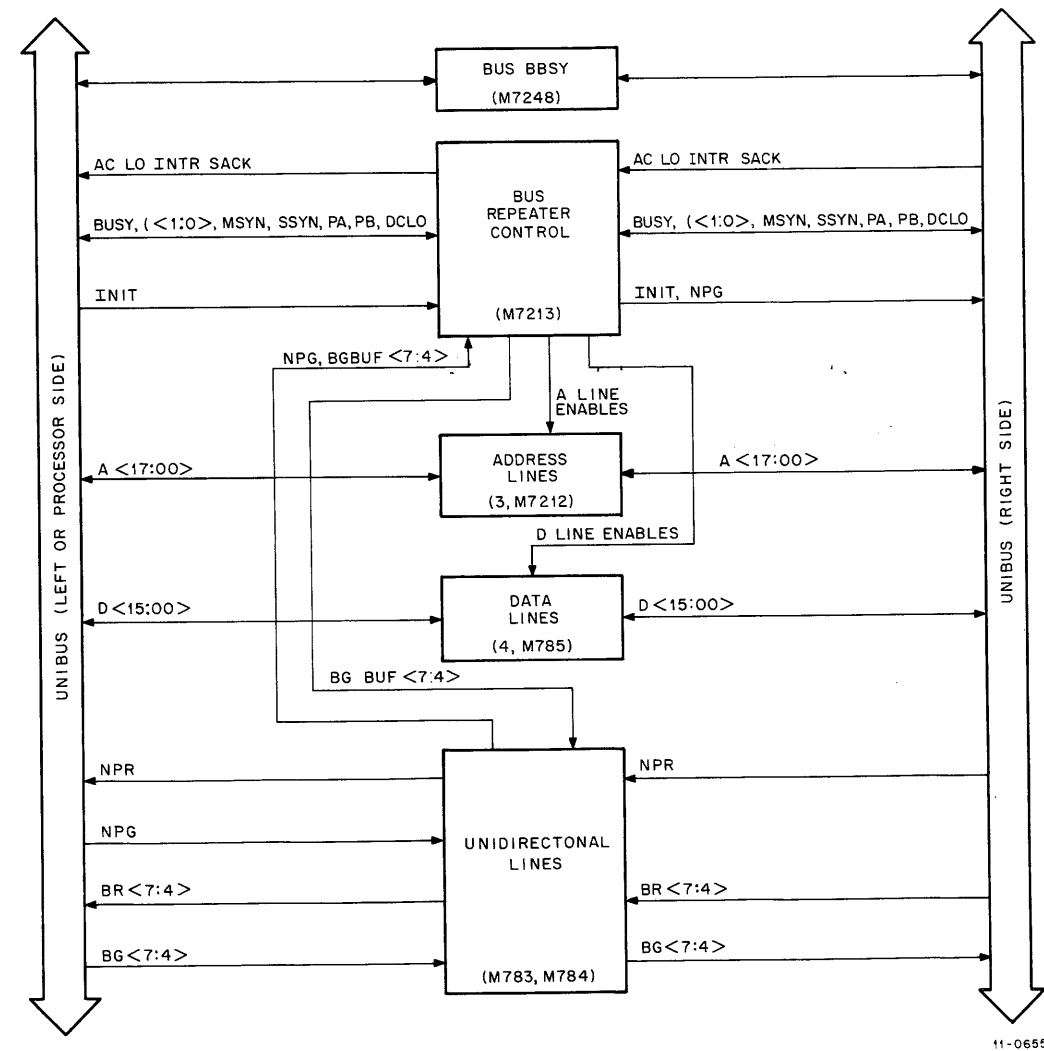


Figure 1-1 DB11 Bus Repeater Block Diagram

- a. INIT
- b. INTR
- c. all Grant
- d. all Bus Request (BR)
- e. SACK
- f. ALCO

The DCLO signal must be bidirectional because the power fail signal can be coming from either side of the buffer; thus, the DCLO signal must be buffered in the same manner as the BBSY signal.

1.3 DB11 SPECIFICATIONS

The DB11 specifications are listed in Table 1-1.

Table 1-1
DB11 Specifications

Specification	Description
Bus Timing	
Time added to bus cycles with master and slave on the same side.	Zero
Time added to bus cycles with master and slave on different sides.	375 ns (worst case)
MSYN signal	This signal arrives at the device 75 ns after the address lines have asserted. (The A lines remain until the MSYN signal drops.)
SSYN signal	This signal arrives no more than 75 ns before data is asserted to the device.
INTR signal	This signal arrives at the processor no more than 75 ns before data is asserted.
Bus Load	The DB11 Bus Repeater represents 2 unit loads to the primary bus (input side).
Power Requirements	
Power Dissipation	At +5V, 2.2A
Environmental Limits	
Temperature	+40°F to 120°F
Relative Humidity	Up to 95%

1.4 RELATED DOCUMENTS

A list of documents relating to the DB11 and pertaining to its use as a bus repeater are included in Table 1-2.

Table 1-2
Related Documents

Title	Number	Description
General		
<i>PDP-11 Handbook</i>	Second Edition, 1970	Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data.
<i>Instruction List</i>	None	Pocket-size list of instructions. Lists group names, functions, codes, and bit assignments. Includes ASCII codes and the bootstrap loader.
<i>Logic Handbook</i>	DEC, 1970	Presents functions and specifications of the M-series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11.
Hardware		
<i>Unibus Interface Manual</i>	DEC-11-HIAB-D	Used in conjunction with this manual; provides detailed theory, flow, and logic descriptions of Unibus and external device logic. Discusses methods of interface construction and provides examples of typical interfaces.
<i>PDP-11/20 System</i>	DEC-11-HR1A-D	Introduction, general description, specifications of entire PDP-11/20 system. Also contains operating procedures and controls and indicators for both PDP-11 and Teletype.
<i>KA11 Processor</i>	DEC-11-HR2A-D	Block diagram discussion, detailed theory of operation related to flow diagrams, instruction set, module descriptions and related logic diagrams, maintenance and adjustments.

Table 1-2 (Cont)
Related Documents

Title	Number	Description
Hardware (Cont)		
<i>MM11-E Core Memory</i>	DEC-11-HR3A-D	General discussion, detailed theory of operation, bus transactions, adjustments, maintenance aids, and logic drawings.
<i>KL11 Teletype Control</i>	DEC-11-HR4A-D	Theory of operation, adjustment and calibration, programming data, maintenance aids, and logic drawings.
<i>H720 Power Supply & Mounting Box</i>	DEC-11-HR5A-D	Power supply block diagram discussion, theory of operation, circuit diagrams. Mounting box description and specifications for all models and cabinets. Includes installation information.
<i>KY11-A Programmer's Console</i>	DEC-11-HR7A	General description, flow diagram discussion, module description and related logic diagram. Operation and controls & indicators covered in <i>PDP-11/20 System Manual</i> .
<i>PDP-11 Conventions</i>	DEC-11-HR6A-D	<ul style="list-style-type: none"> a. General Maintenance b. Logic Symbology c. Drawing Set Explanation d. Processor Signals e. Product Identification Codes f. Glossary g. Abbreviations
Software		
<i>Paper Tape Software Programming Handbook</i>	DEC-11-GGPA-D	Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble and debug PDP-11 programs. Also includes discussion of input/output programming and the floating-point and math package.

CHAPTER 2

INSTALLATION PLANNING

2.1 INTRODUCTION

The information necessary to install the DB11 and to achieve operational status is contained in this chapter. A physical description of the DB11 bus and power connections, and installation testing are also included in this chapter.

2.2 PHYSICAL DESCRIPTION

The DB11 occupies one PDP-11 System unit within the PDP-11 mounting box. Each DB11 Bus Repeater comprises the following:

- a. a PDP-11 System unit
- b. four M785 Transceiver Modules
- c. a M783 Drivers Module
- d. a M784 Receivers Module
- e. three M7212 Address Buffer Modules
- f. a M7213 Buffer Master Module
- g. a M7248 Unibus BBSY Repeater Module
- h. two M920 Bus Connector Modules
- i. two M930 Bus Terminator Modules

These modules are positioned in the PDP-11 System unit as shown in Figure 2-1. (Refer to engineering drawing D-MU-A-01 for module system utilization diagram.) The DB11 must be installed only in the first (SLOT 1) or last (SLOT 6) system unit (BA11). This prevents the DB11 from latching up the DCLO circuit. If a DB11 is placed in any other system unit with other options placed before and after the DB11, the DCLO circuit will be looped through the power harness.

2.3 BUS AND POWER CONNECTIONS

The DB11 bus connections on each side of the bus repeater are provided by two M920 Bus Connector Modules. The M920 Module is a jumper module that connects the PDP-11 Unibus and the PDP-11 system units. Two M920 Modules connect the bus to the DB11 on the output and input side.

On each side of the DB11, a M930 Bus Terminator Module is used to terminate the bus. (Refer to engineering drawings D-IC-DB11-A-04 and D-BD-DB11-A-05 for cable connectors.) This prevents the bus from running through the system unit, which is the case for normal interfaces. All bus information (bus lines) is forced to be passed through and controlled by the DB11 logic. For detailed descriptions of the M920 and M930 Modules refer to the *PDP-11 Unibus Interface Manual*, DEC-11-HIAB-D.

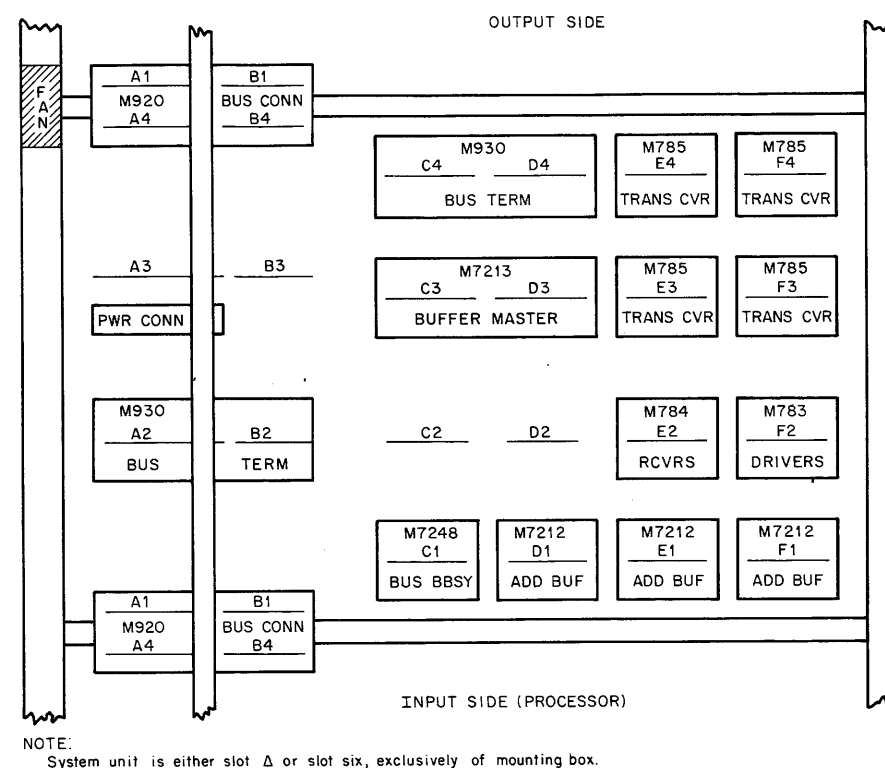


Figure 2-1 DB11 System Unit Layout

Power is supplied to the DB11 logic through the PDP-11 System unit power connection. When power is supplied to the PDP-11 system, the DB11 logic also receives power. This power connection is discussed in detail in the *PDP-11 Unibus Interface Manual*, DEC-11-HIAB-D.

2.4 INSTALLATION TESTING

The DB11 is tested to ensure that the unit has been properly installed and is completely operational. This is accomplished by performing the test in Chapter 4 (Paragraph 4.2).

CHAPTER 3

DETAILED DESCRIPTION

3.1 INTRODUCTION

The DB11 interfaces the Unibus signals between the processor bus side (left) and the extended bus side (right) through four logical units. These units are:

- a. the Bus Repeater Logic (M7213 and M7248 Modules)
- b. the Bus Repeater A Line Logic (three M7212 Modules)
- c. the Bus Repeater D Line Logic (four M785 Modules)
- d. the Bus Repeater Unidirectional Lines Logic (M783 and M784)

Table 3-1 lists the signals interfaced by each logical unit, as well as its source and destination. For a detailed description of the bus signals refer to the *PDP-11 Unibus Interface Manual*, DEC-11-HIAB-D.

Table 3-1
Unibus Signals

Name	Mnemonic	Source	Destination
BUS REPEATER CONTROL (M7213, M7248) SIGNALS INTERFACED			
Data Transfer Signal (for transfer of data to or from master)			
Control	C (1:0)	Master	Slave
Master Sync	MSYN	Master	Slave
Slave Sync	SSYN	Slave	Master
Priority Transfer Signals (for transfer of bus control to a priority selected master)			
Selection Acknowledge	SACK	Next Master	Processor
Bus Busy (M7248)	BBSY	Master	All
Interrupt	INTR	Master	Processor
Initialize and Power Fail Signals			
Initialize	INIT	Processor	All
AC Low	AC LO	Power	All
DC Low	DC LO		
BUS REPEATER A LINE (M7212) SIGNALS INTERFACED			
Address	A (17:00)	Master	All
BUS REPEATER D LINE (M785) SIGNALS INTERFACED			
Data	D (15:00)	Master	Slave

(continued on next page)

Table 3-1 (Cont)
Unibus Signals

Name	Mnemonic	Source	Destination
BUS REPEATER UNIDIRECTIONAL LINES (M783 and M784) SIGNALS INTERFACED			
Non-Processor Request	NPR	Any NPR Devices	Processor
Bus Request	BR (7:4)	Any	Processor
Non-Processor Grant	NPG	Processor	Next Master
Bus Grant	BG (7:4)	Processor	Next Master

In addition to interfacing the signals indicated in Table 3-1, the bus repeater logic also generates the left-to-right and right-to-left enable signals. These signals qualify the direction of bus flow for the DB11 D line logic and A line logic. The directional indication of BBSY on the M7248 Module determines whether the asserted signal bus flow is left-to-right or right-to-left. Engineering drawing D-BD-DB11-A-05 shows a block diagram, signal-by-signal interface of the DB11. The processor side of the DB11 is indicated as the LEFT side.

3.2 BUS REPEATER LOGIC

The bus repeater logic consists of the logic on the M7213 and M7248 Modules (see drawings D-CS-M7213-0-1 and D-CS-M7248-0-1, respectively). The M7213 and M7248 Modules interface the signals indicated in Table 3-1, generate the direction enable signals, and provide the left-to-right buffer gating for the unidirectional bus lines (BG <714>). The signals INHIBIT BUS and INHIBIT INIT for the DB11 are always held low (ground). These signals are only used when the bus repeater is incorporated (2 bus repeaters) in the Bus Switch. For additional information refer to the *DT11 Bus Switch Manual*, DEC-11-HDTA-D.

The DB11 uses the bidirectional BBSY circuit as the master controlling circuit. The direction of BBSY on the bus, whether it inputs the DB11 as LEFT BUS BBSY or RIGHT BUS BBSY, determines the direction to enable the A line circuits (A ENABLE LEFT TO RIGHT or A ENABLE RIGHT TO LEFT, respectively). BBSY is used as the master controlling signal because the master device always asserts the A lines; therefore, BBSY enables the correct enabling signal direction for the DB11. (Engineering drawing D-CS-M7248-0-1 shows the basic BBSY enabling circuit including the generation of the A line enabling signals.) When a device master to the left of the DB11 asserts BBSY, LEFT BUS BBSY asserts low. Because RIGHT BUS BBSY is unasserted (high), LEFT BUS BBSY generates LEFT BUF BBSY. Because INHIBIT BUS is held low for the DB11, A ENABLE LEFT TO RIGHT is generated for the direction of flow on the bus A lines. Thus, RIGHT BUF BBSY is low, because RIGHT BUS BBSY is unasserted.

LEFT BUF BBSY (high) moves to the right via the top path, thus putting BBSY on the entire bus. This level remains until LEFT BBSY is dropped by the master device. When LEFT BBSY is dropped, LEFT BUF BBSY goes low to disable A ENABLE LEFT TO RIGHT and RIGHT BUS BBSY. RIGHT BUF BBSY remains unasserted and, therefore, enables the output gate to RIGHT BUS BBSY to move any LEFT BUS BBSY signal that occurs from the left bus. The circuit works in reverse for a RIGHT BUS BBSY with A ENABLE RIGHT TO LEFT being generated.

When the A line direction enable signal is generated, the MSYN circuit is enabled in the correct direction, according to the A line enable signal. If A ENABLE LEFT TO RIGHT is generated, LEFT BUS MSYN is propagated through a delay to assert RIGHT BUS MSYN and vice versa. This delay causes the MSYN output (right or left) to be delayed 160 ns after the MSYN input is asserted on the input bus for deskewing purposes. This delay only occurs on the assertion or low-going transition of the signal.

The direction to enable the D lines (D LINE RIGHT TO LEFT ENABLE or D LINE LEFT TO RIGHT ENABLE) is determined from BBSY (A line enabling direction), C01, and INTR bus signals. For a DATI or DATIP bus operation (C01 is 0), the D lines are enabled to the device master; for a DATO or DATOB, the D lines are enabled away from the bus master; for an INTR, the D lines are enabled to the processor. The D LINE ENABLE RIGHT TO LEFT signal is generated by any one of the three following conditions:

- a. A DATIP or DATI bus operation with no INTR and the presence of the A ENABLE LEFT TO RIGHT signal (bus master on left or input bus) generates the D line enabling signal (right to left).
- b. A DATO or DATOB with no INTR and the presence of A ENABLE E RIGHT TO LEFT (bus master on right or output bus) generate the D line enabling signal (right to left).
- c. An INTR condition always enables the D lines to the processor (right bus to left bus).

Similarly, to enable the D lines left to right, the absence of RIGHT BUS C01 and A ENABLE RIGHT TO LEFT is required to generate D LINE LEFT TO RIGHT ENABLE. For D line enabling, the enabling conditions are ORed conditions in the logic (see drawing D-CS-M7213-0-1). To enable the D lines from left to right (D LINE LEFT TO RIGHT) either of the following conditions must be present:

- a. A DATI or DATIP with no INTR and the presence of A ENABLE RIGHT TO LEFT (bus master on right bus) generate the D line enabling signal (left to right).
- b. A DATO or DATOB with no INTR and the presence of A ENABLE LEFT TO RIGHT (bus master on left or input bus) generate the D line enabling signal (left to right).

The SSYN circuit is a completely bidirectional circuit. It provides a 75-ns delay above the gate delays to ensure that SSYN arrives at a device before the data. This delay occurs only on the low (asserted) transition of SSYN.

The generation of the D line enabling signals, in turn, enables the parity of the PA and PB bus signals. The D LINE RIGHT TO LEFT ENABLE (L) signal enables RIGHT BUS PA and RIGHT BUS PB through to the left bus, and the D LINE LEFT TO RIGHT ENABLE (L) signal enables LEFT BUS PA and LEFT BUS PB through to the right bus. These lines are treated as Data Lines. The INTR signal is always moved straight through the DB11 from right bus to left bus, because the INTR signal always goes to the processor. This circuit also provides for a 75-ns deskewing delay.

Both the C00 and C01 signals are enabled (in the proper direction) through the DB11 by the A line enabling signals. For example, the LEFT BUS C01 signal is enabled to RIGHT BUS C01 by A ENABLE LEFT TO RIGHT. The C00 and C01 circuits provide a deskewing delay of 75 ns in either direction (both assertion and negation). Thus, LEFT BUS INIT is gated to assert RIGHT BUS INIT (unidirectional), because the INIT signal is generated only by the processor. Conversely, SACK is gated from right to left (RIGHT BUS SACK (L) to LEFT BUS SACK (L) delayed) because SACK is always asserted by the next bus master to the processor. Finally, the power fail AC LO is generated right to left from power to all devices. The INHIBIT AC LO signal is always grounded for DB11 use (used only in DT11 Bus Switch). The NPG and BG circuits are used in conjunction with the unidirectional lines and are discussed in the following paragraphs.

3.3 UNIDIRECTIONAL LINE LOGIC

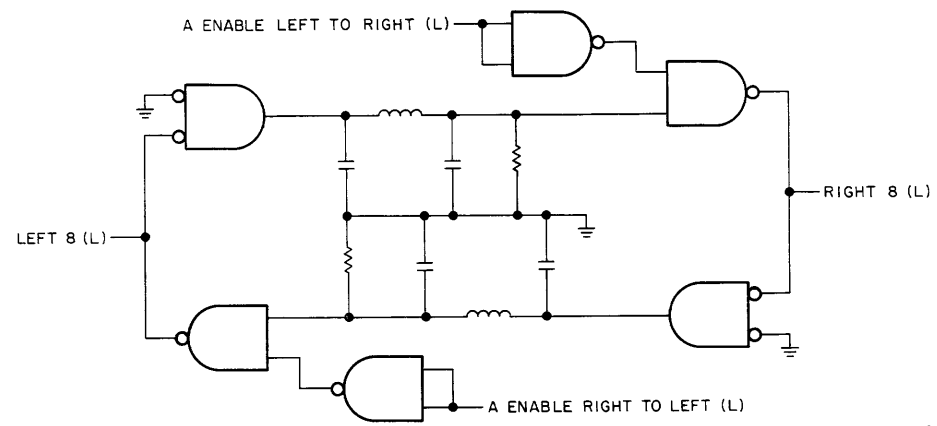
The unidirectional line logic (see drawing D-BS-DB11-A-02) consists of: gating circuits that gate the bus requests (BRs), bus grants (BGs), and non-processor request (NPR) and non-processor grant (NPG) signals. The four bus request levels (BR4, BR5, BR6, and BR7) and the non-processor request signal (NPR) are generated from a device to the processor. Thus, they interface through the DB11 only from right to left (to the processor). The non-processor grant signal (NPG) and the four bus grant levels (BG4, BG5, BG6, and BG7) are buffered through the DB11 (from the processor) to the device that made the request. The grant signals, therefore, are in one direction, left to right in the DB11. These signals are buffer-gated in the M7213 Module (see drawing D-CS-M7213-0-1), with RIGHT BUF NPG generating NPG on the right bus in the M7213. The BG signals are input from the left bus in the M784 Module and output to the right bus in the M783 Module.

3.4 A LINE LOGIC

The A line logic consists of bidirectional gating with an LC network. The LC circuits are linear phase filters that provide an equal 75-ns deskewing delay to the assertion and negation of the A lines. These deskewing delays are required to preserve the guaranteed Unibus timing. Figure 3-1 shows a typical A line circuit (see drawing D-CS-M7212-0-1). One of these circuits is employed by each of the 18 bus address lines (A00 through A17 and by C0 and C1). The LEFT signal, when asserted, gates through to the deskewing delay where the A line enable signal (A ENABLE LEFT TO RIGHT) generated in the M7213 Module gates with the LEFT signal to generate the RIGHT bus A line signal. In the right-to-left bus direction, the circuit works exactly the same with A ENABLE RIGHT TO LEFT enabling the signal to the left bus.

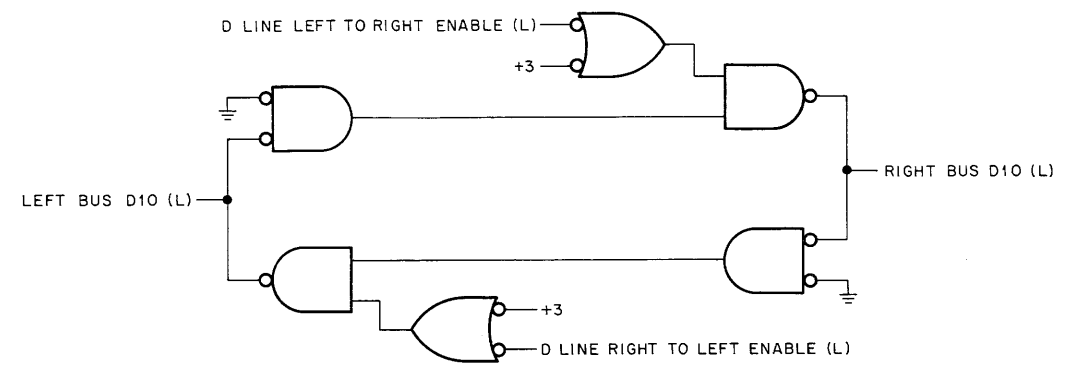
3.5 D LINE LOGIC

The D line logic consists of the bidirectional gating circuits of the M785 Transceiver Modules. A typical circuit for one line is shown in Figure 3-2 (see drawing D-BS-DB11-A-03). Each of the 16 data lines (D00 through D15) is gated into a circuit where the D line enable signals from the M7213 Module gate the data lines to the output bus. For example, the D lines asserted at the left bus are enabled by D LINE LEFT TO RIGHT ENABLE, and all the left bus signals (LEFT BUS D00 – LEFT BUS D15) are gated through to assert the right bus signals (RIGHT BUS D00 – RIGHT BUS D15). When the D lines are inputting at the right side of the DB11, the D LINE RIGHT TO LEFT ENABLE signal asserts from the M7213 Module; the D line signals are then gated onto the left bus. Thus, gating through to the D lines by DB11 depends on the conditions that generate the D line enabling signals.



11-0653

Figure 3-1 A Line Logic Circuit



11-0652

Figure 3-2 D Line Logic Circuit

CHAPTER 4

MAINTENANCE

4.1 INTRODUCTION

Maintenance of the DB11 consists of its operational verification in system use. Testing must be done with the DB11 in a system because the device is non-programmable. The testing procedure consists of the production tests and the field tests.

4.2 PROCEDURES

For production or acceptance testing, special test equipment is utilized to verify on-line performance. In particular, Bus Testors are used with the general test program (GTP) software to verify that the DB11 is responding correctly to all BR (bus requests) and NPR (non-processor requests) level devices. This test configuration is shown in Figure 4-1.

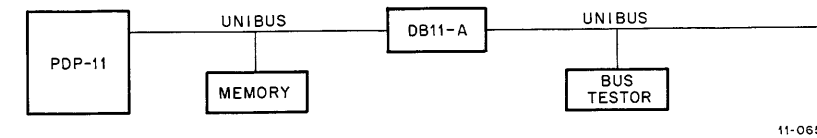


Figure 4-1 Test Configuration

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