pdp11

AD01-D analog-to-digital conversion subsystem manual

digital

DEC-11-HADA-D

AD01-D analog-to-digital conversion subsystem manual

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Edition April 1971
2nd Printing October 1971

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The AD01-D Analog-to-Digital Conversion Subsystem is a peripheral device used with the PDP-11 Computer Systems in data acquisition and control applications. Refer to the *PDP-11 Unibus Interface Manual* for information relevant to the architecture of the computer and peripheral devices.

1.2 PURPOSE

The AD01-D operates under computer or external clock control as a highly flexible analog input device to digitize analog inputs connected to directly addressable, multiplex switch modules. As many as eight multiplex switch modules can be implemented. Each module can service four individual analog inputs.

The basic AD01-D provides 10-bit digitization of unipolar, high-level analog signals with a nominal full-scale range of 0V to +1.25V, +2.5V, +5.0V or +10V. These four ranges are program-selectable and are achieved by a selectable gain amplifier. Options are available for digitization of bipolar analog signals and for sample and hold applications.

1.3 FUNCTIONAL DESCRIPTION

The AD01-D comprises

a. An expandable solid-state input multiplexer

b. A programmable input range selector

c. A high-speed A/D converter

d. The computer interface logic.

The interface logic includes two registers to store control and status information and data. The AD01-D is accessed and controlled by a control and status word with a Move (MOV) instruction. A single control and status word from the computer selects the input range and multiplexer channel and starts the conversion. Other novel features of the interface logic are the ability to place the AD01-D in an interrupting or noninterrupting mode and to select an external clock. In the interrupting mode, the AD01-D can issue an interrupt when conversion is done or when an error condition is produced by starting a new conversion before the previous conversion is complete. The noninterrupting mode enables the converter to approach its maximum throughput rate under program control. After the conversion is complete, the data is easily transferred from the AD01-D to the computer by programming another MOV instruction.

1.4 PHYSICAL DESCRIPTION

The AD01-D Analog-to-Digital Converter Subsystem can be configured and modified according to application needs. All logic, options, and a Type H727 A/B Analog Power Supply are housed in a single, 5-1/4 in., rack-mountable assembly. Insertion slots for the multiplex switch modules, bipolar option, and sample and hold option are prewired to simplify field installation and modification. Only simple jumper wire changes are required. The module complement and optional modules for the AD01-D are listed in Table 1-1; the location of each module is shown in Figure 1-1. Logic power for the AD01-D is supplied by a separate H716 Logic Power Supply, which can be rack mounted. Operation with an input voltage of 115V requires an H727-A power supply and the system is designated AD01-DA; an input voltage of 230V requires an H727-B and the system is designated AD01-DB. If rack mounting of the subsystem is desired, DEC offers a 19-in. industrial Type H950 Cabinet with a blower fan and front and rear doors.

Table 1-1
AD01-D Module Complement

Type/Part No.	Name	Quantity	Location
A124	Four Input Multiplex Switch	1	B16
A124*	Four Input Multiplex Switch	8 (max)	A17-A20 B17-B20
A220	Selectable Gain Buffer Amplifier	1	A16
A862 (AH05)*	Bipolar A/D Converter	1	AB13 (AB12)
A405 (AH04)*	Sample and Hold	1	AB15
A708	Dual Voltage Regulator	1	A24
A812	10-Bit A/D Converter	1	AB12
G736	Request Jumper	1	A10
M105	Address Selector	1	A3
M111	Inverter	1	A9
M112	NOR Gate	1	B7
M113	10 2-Input NAND Gates	1	A7
M161	Binary to Octal/Decimal Decoder	1	B10
M206	Six Flip-Flops	2	AB6
M302	Dual Delay Multivibrator	3	AB11, B8
M501	Schmitt Trigger	1	AB22
M617	6 4-Input NOR Buffers	1	B9
M782	Interrupt Control	1	B3
M783	Unibus ™ Drivers	2	AB5
M784	Unibus Receivers	1	A4
M785	Unibus Transceivers	1	B4
M908	Connector	2	AB21

*Denotes optional modules.

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1.5 SPECIFICATIONS

1.5.1 Environmental

Temperature:	0°C to +55°C, operating -25°C to +85°C, storage
Humidity:	to 90 % without condensation

1.5.2 Power Requirements

Input voltage (ac):	115V/230V ± 10%
Input frequency (ac):	47 Hz to 63 Hz, single phase
Power dissipation:	<75W

1.5.3 Packaging

Size:	Height: 5-1/4 in. Width: 19 in. Depth: 12 in. (plus separate power supply)
Weight:	15 lb

1.5.4 Performance Parameters

Conversion time:	22 μs, including channel and gain selection with or without sample and hold option. Bipolar option adds 7 μs.
Conversion aperture:	17.5 μs, 24 μs with Bipolar Option AH05, or 0.1 μs with Sample and Hold Option AH04
Sample and Hold	
Acquisition:	5 μs to 0.01% of full-scale step change
Aperture:	100 ns
Number of analog input channels:	4 minimum (expandable to 32 in groups of 4)
Input voltage range (program-selectable)	
Unipolar:	0V to 1.25V, +2.5V, +5.0V or +10.0V, full-scale
Bipolar:	0V to ± 1.25V, ± 2.5V, ± 5.0V or ± 10.0V, full-scale
System accuracy:	± 0.1% of full-scale ± 0.125% of full-scale with Sample and Hold Option AH04

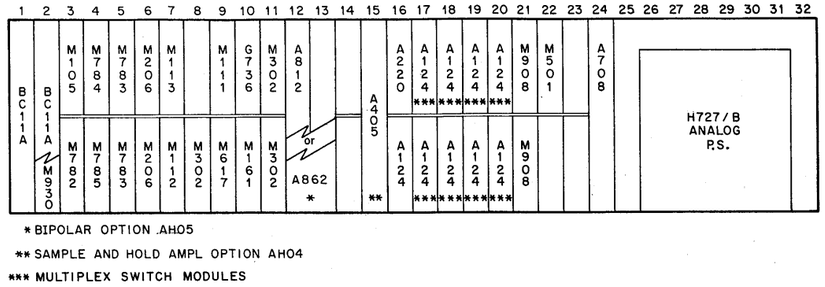


Figure 1-1 AD01-D Configuration

Input impedance:	1000 MΩ in parallel with 20 pF
Input isolation:	Enhancement mode MOS FET switches, off when unselected or power off
Analog input connections:	Plug-in cable modules
Channel selection: (program-selectable)	6-bit address
Overload capability:	±20V on all ranges without damage
Cross-Channel attenuation:	78 dB, dc to 80 Hz for 20V p-p signals, 100-Ω source impedance
Input gain: (program-selectable)	2-bit code

1.6 REFERENCE DOCUMENTS

The following documents are essential to understand the PDP-11 Computer System:

PDP-11 Handbook
PDP-11 Unibus Interface Manual
PDP-11 Maintenance Manuals

The following diagnostic program is required to test the performance of the AD01-D:

AD01-D MainDEC-11-D6AB
A-SP-AD01-D-12 Acceptance Procedure

CHAPTER 2
INSTALLATION AND ADJUSTMENTS

2.1 INSTALLATION PLANNING

The AD01-D is a Type 1943 rack-mountable assembly, which can be installed in the Type H950 Equipment Cabinet. The Type 1943 Assembly has the following dimensions:

Width:	19 in.
Depth:	12 in.
Height:	5-1/4 in.

The associated H716 Logic Power Supply mounts on the rear door of the cabinet.

2.2 ENVIRONMENTAL REQUIREMENTS

The AD01-D and PDP-11 operate in identical environments; the environmental limitations are listed in Chapter 1.

2.3 CONFIGURATIONS

The basic AD01-D Subsystem consists of a 5-1/4 in. rack-mountable logic assembly and a H716 Logic Power Supply. A physical description of the AD01-D and associated options is presented in Chapter 1. The following paragraphs summarize the requirements for installing and configuring the AD01-D.

2.3.1 Channel Expansion

Eight prewired insertion slots are provided in the logic shelf for the multiplex switch modules. The slots are A17 through A20 and B17 through B20 (see Figure 1-1). When expanding the channel capacity, modules must be added in the A level before the B level, progressing from slot 17 toward slot 20.

2.3.2 Bipolar Option AH05

To accommodate A/D conversion of bipolar analog voltages, Bipolar Option AH05 must be installed in the AD01-D logic assembly. The option consists of a replacement Bipolar A/D Converter Module, A862.

The replacement A/D converter occupies two insertion slots while the A812 10-Bit A/D Converter occupies only one. The insertion slot is prewired to accept either A/D converter without wiring changes (see Figure 1-1).

2.3.3 Sample and Hold Amplifier Option AH04

If skewless sampling of analog signals is desired, Sample and Hold Amplifier Option AH04 must be installed in the AD01-D logic assembly. The option consists of a single module designated the A405 Sample and Hold Module. A prewired insertion slot located at AB15 (see Figure 1-1) on the logic assembly is reserved for the module.

2.3.4 Unibus Connections

Only one BC11-A Cable is required to connect the Unibus from the computer to the AD01-D. This cable must be inserted into slot AB01 on the logic assembly. If the AD01-D is the last peripheral device on the Unibus, Terminator Module M930 is inserted in slot AB02; otherwise, this slot is used to connect the Unibus to another peripheral device using another BC11-A Cable.

2.3.5 Multiplexer Channel Connections

The input connections to the multiplexer switch modules are wired to two M908 Connector Modules located in slots AB21 of the logic assembly. The analog signals to be converted should be carried on user-supplied twisted pairs of wires (shielded if necessary). These twisted pairs should be soldered to the appropriate split lugs on the M908 Modules. The assigned channel numbers and the associated pin numbers on the M908 Modules are identified in Table 2-1.

2.3.6 External Clock Connection

As with the multiplexer channel connections, external clock input connections to the timing circuits of the AD01-D are also wired to the M908 Connector Module located in slot A21. If an external clock is to be used in an AD01-D installation, the clock signal should be carried on user-supplied twisted pairs of wires (shielded if necessary). The twisted pair should be soldered to split lugs A1 and B1 or A2 and B1 on the M908 Connector Module in slot A21.

2.4 INSTALLATION PROCEDURE

The installation procedure for the AD01-D Analog Subsystem is as follows:

Step	Procedure
1	Unpack the equipment from the shipping container(s) and inspect the unit(s) for damage. Damage claims should be made to the DEC district supervisor. **NOTE** **DEC Field Service personnel should be available for consultation on potential problems.**
2	Remove the tape that secures the modules and cables in the AD01-D Assembly and varify that the modules and connectors are seated in the proper connector slots (refer to drawing D-MU-AD01-D-02).
3	Mount the AD01-D Assembly in the assigned location (H950 Equipment Cabinet), using the appropriate hardware.

(continued on page 2-2)

Table 2-1
Channel, Module, and Pin Number Cross-Reference List

Channel No.	A124 Multiplex Switch Module Slot	M908 Connector Module		
		Slot	Hot Pin	Gnd Pin
0	A17	A21	B2	C2
1			C1	D1
2			D2	E2
3			E1	F1
4	A18		F2	H2
5			H1	J1
6			J2	K2
7			K1	L1
8	A19		L2	M2
9			M1	N1
10			N2	P2
11			P1	R1
12	A20		R2	S2
13			S1	T1
14			T2	U2
15			U1	V1
16	B17	B21	B2	C2
17			C1	D1
18			D2	E2
19			E1	F1
20	B18		F2	H2
21			H1	J1
22			J2	K2
23			K1	L1
24	B19		L2	M2
25			M1	N1
26			N2	P2
27			P1	R1
28	B20		R2	S2
29			S1	T1
30			T2	U2
31			U1	V1
EXT IN		A21	A1	B1 } Ext Com
EXT IN A			A2	B1 }

Step	Procedure
4	Install the logic power supply and chassis subassembly in the assigned location (refer to drawing D-UA-H716-B-0 for AD01-DA or drawing D-UA-H716-D-0 for AD01-DB).
5	Connect the H716 Logic Power Supply Cable from the power supply to the left end panel of the AD01-D Subsystem where noted.
6	Determine where Unibus is terminated and connect BC11-A Cable to last device. If the AD01-D is the last device on the bus, install the Terminator Modules M930 in slot AB02 of the AD01-D.
7	Perform the acceptance checkout of the AD01-D logic and analog circuits using the MainDEC-11-D6AB Diagnostic Program and A-SP-AD01-D-12 Acceptance Procedure. Adjustment should not be necessary because all potentiometers are sealed at the factory after adjustment.
8	If, at any time, the AD01-D is not within its stated specifications (accuracy), perform the adjustment procedure in Paragraph 2.6. When this adjustment is complete, perform the acceptance tests again.

2.5 OPTION INSTALLATION

The AD01-D options necessitate some changes in the back panel wiring. All information regarding the wiring for each option configuration is given in Figure 2-1. Add and/or delete wires according to this diagram when installing options.

2.6 ADJUSTMENT PROCEDURE

The adjustment procedure for the AD01-D depends on the particular option configuration. If a given option is not included in the AD01-D, disregard the corresponding adjustment procedure. To achieve accurate calibrations, perform the adjustments in the following sequence.

1. Power Supplies
2. Timing
3. A/D Converter (A812 or A862)
4. Sample and Hold A405
5. Switched-Gain Amplifier A220
6. Multiplexer Setup
7. External Sync

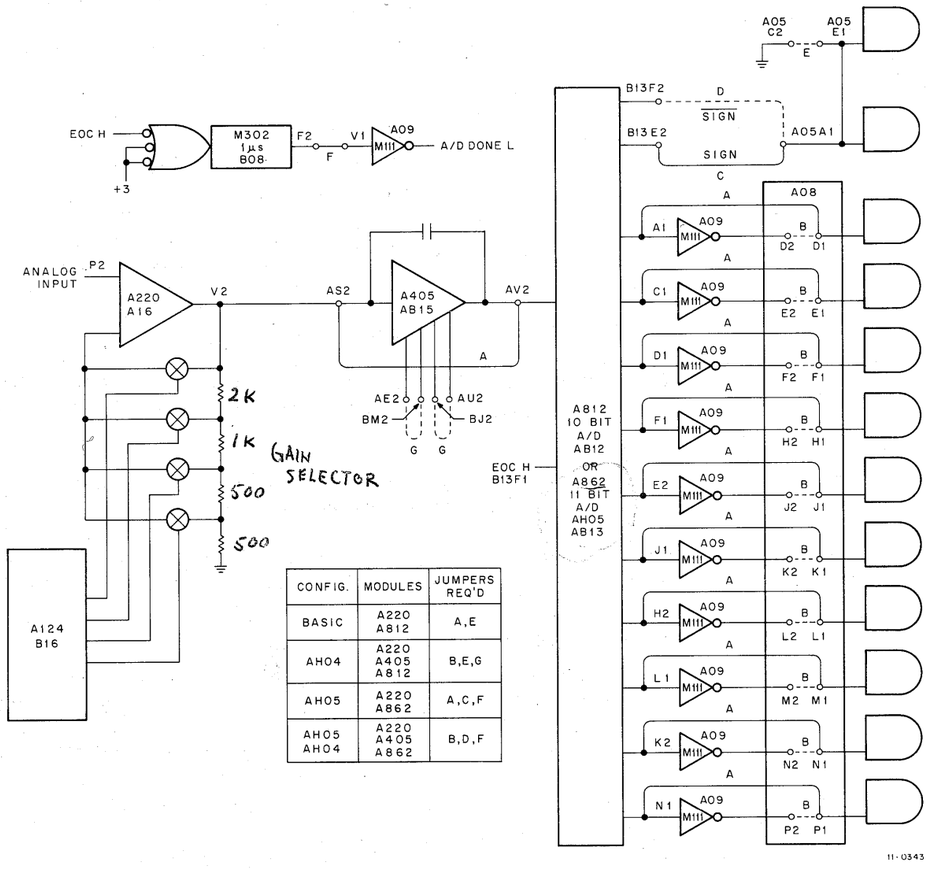
2.6.1 Power Supply Adjustments

Table 2-2 summarizes the necessary information for adjusting the power supplies in the AD01-D.

Table 2-2
Power Supply Adjustments

Supply	Voltage*	Pin	Adjustment Location
H716	+5V ± 0.25V	A03A2 A03C2 (GND)	
H727	+15V ± 0.1V	A24V2	POWER MATE – Top Right (Blue Case)
		A24T2 (GND)	DELTRON – Bottom Right (Black Case)
	-20V ± 0.1V	A24N2	POWER MATE – Top Left (Blue Case)
		A24T2 (GND)	DELTRON – Bottom Left (Black Case)

*Voltage measurement can be made with EDC null meter and DEC 10:1 Divider (refer to Table 5-1).



CONFIG.	MODULES	JUMPERS REQ'D
BASIC	A220 A812	A,E
AH04	A220 A405 A812	B,E,G
AH05	A220 A862	A,C,F
AH05 AH04	A220 A405 A862	B,D,F

Jumper	From	To
A	A09A1 A09C1 A09D1 A09F1 A09E2 A09J1 A09H2 A09L1 A09K2 A09N1 A15S2	A08D1 A08E1 A08F1 A08H1 A08J1 A08K1 A08L1 A08M1 A08N1 A08P1 A15V2
B	A08D2 A08E2 A08F2 A08H2 A08J2 A08K2 A08L2 A08M2 A08N2 A08P2	A08D1 A08E1 A08F1 A08H1 A08J1 A08K1 A08L1 A08M1 A08N1 A08P1
C	B13E2	A05A1
D	B13F2	A05A1
E	A05C2	A05E1
F	B08F2	A09V1
G	A15E2 B15J2	B15M2 A15U2

Figure 2-1 Option Configuration Diagram

Table 2-2 (Cont)
Power Supply Adjustments

Supply	Voltage*	Pin	Adjustment Location
A708	-15V ± 0.1V	A24S2 A24T2 (GND)	No Adjustment
*Voltage measurement can be made with EDC null meter and DEC 10:1 Divider (refer to Table 5-1).			

2.6.2 **Timing Adjustment**

The timing of the AD01-D can be adjusted while running the WAS-IS TEST (SA 270_8) of the diagnostics with inhibit printout option. The required timing adjustments are summarized in Table 2-3.

2.6.3 **A/D Converter**

2.6.3.1 **A812** – The following adjustment should be performed while running the Display Conversion Loop (SA 220_8) of the diagnostic program.

Table 2-3
Timing Adjustments

Module	Slot	Pin	Time
M302	A11	F2	5 μs
M302	A11	T2	0.5 μs
M302	B11	F2	0.5 μs
M302	B11	T2	0.1 μs
M302	B08	F2	1 μs/AH05 only
M302*	B08	T2	2.5 μs 0.1 μs with AH05

*External sync signal is required to set this single-shot, because it derives output signal from Ext Sync input.

NOTE

The procedure should be performed with the A220 and A405 Modules removed from their insertion slots.

Step	Procedure
1	Extend A812 Module using two W982 Extender Modules.
2	Set EDC to 5 mV and connect to B12V2.
3	Adjust comparator sensitivity potentiometer (see Figure 2-2) for $000\ 000_8$ to $000\ 001_8$ on console DATA indicators. (Adjust for $001\ 777_8$ to $001\ 776_8$ if AH04 is installed.)
4	Set EDC to +9.9853V.
5	Adjust reference potentiometer for $001\ 777_8$ to $001\ 776_8$ on console DATA indicators. (Adjust for $000\ 000_8$ to $000\ 001_8$ if AH04 is installed.)

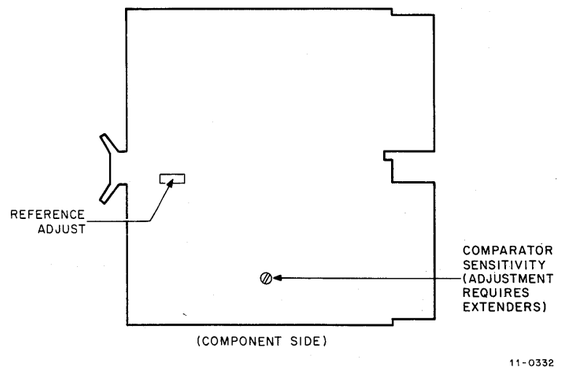


Figure 2-2 A812 A/D Converter

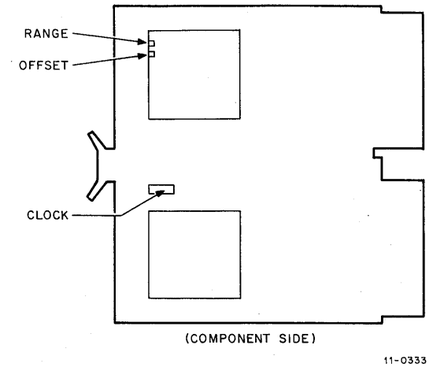


Figure 2-3 A862 A/D Converter

2.6.3.2 **A862 (AH05 Option)** – The following adjustment procedure uses the WAS-IS TEST and the Display Conversion Loop of the diagnostic program. Adjust the A862 A/D Converter as follows:

NOTE

The procedure should be performed with the A220 and A405 Modules removed from their insertion slots.

Step	Procedure
1	Start the WAS-IS TEST (SA 270_8) with inhibit printout bit 13 = 1.
2	Connect scope to B13F1 and adjust clock potentiometer (conversion time) to obtain a 24-μs positive pulse (see Figure 2-3).
3	Stop program and restart at Display Conversion Loop (SA 220_8).
4	Connect EDC to A13J2 and A13F2 (GND). Set EDC to +5 mV ± 2 mV.
5	Adjust offset potentiometer for $000\ 000_8$ to $000\ 001_8$ on console DATA indicators. (Adjust for $001\ 777_8$ to $001\ 776_8$ if AH04 is installed.)

2.6.4 **Sample and Hold A405 (AH04 Option)**

The adjustment procedure of the A405 Module depends on the AD01-D option configuration. Two procedures are outlined below. One procedure applies to systems that have only the AH04 Option (Sample and Hold); the other procedure applies to systems that have both the AH04 and AH05 (Bipolar) Options.

2.6.4.1 **AH04 Option Only** – Adjust the A405 Module as follows:

NOTE

The procedure should be performed with the A220 Module removed from its insertion slot.

Step	Procedure
1	Ensure that all proper jumpers (except those marked G) are installed (see Figure 2-1).
2	Ensure that split lugs A and B on the A405 Module are connected (see Figure 2-4).
3	Start Display Conversion Loop (SA 220_8) of the diagnostic program.
4	Connect EDC to A15S2 and A15F2 (GND). Set EDC to -5 mV.

(continued on Page 2-5)

Step	Procedure
5	Adjust bias potentiometer (see Figure 2-4) on A405 Module for 001 776_8 to 001 777_8 on console DATA indicators.
6	Stop program and turn off computer power.
7	Add jumper wire G to back panel wiring.
8	Turn on computer power and set EDC to 9.9853V.
9	Restart Display Conversion Loop (SA 220_8).
10	Adjust offset coarse potentiometer on A405 for 001 776_8 to 001 777_8 (or as close as possible) on console DATA indicators.
11	Adjust offset fine potentiometer on A405 for 001 776_8 to 001 777_8 on console DATA indicators.

2.6.4.2 **AH04 with AH05 Option Only** – Adjust the A405 Module as follows:

Step	Procedure
1	Ensure that all proper jumpers are installed (see Figure 2-1).
2	Ensure that split lugs A and B on the A405 Module are connected (see Figure 2-4).
3	Connect EDC to A15S2 and A15F2 (GND). Set EDC to +5 mV.
4	Start the Display Conversion Loop (SA 220_8) of the diagnostic program.
5	Adjust bias potentiometer (see Figure 2-4) on A405 Module for 000 001_8 to 000 000_8 on console DATA indicators.

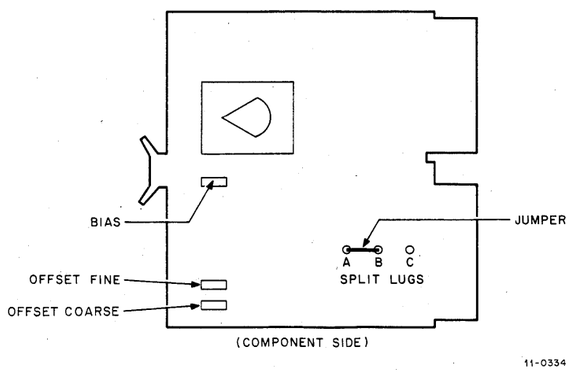


Figure 2-4 A405 Sample and Hold

2.6.5 **Switched-Gain Amplifier A220**

Adjust the A220 Switched-Gain Amplifier as follows:

Step	Procedure
1	Ensure that Module A220 is installed in slot A16 and that Module A124 is installed in slot B16.
2	Connect EDC to A16P2 and A16F2 (GND). Set EDC to +600 μV.
3	Start the Display Conversion Loop (SA 220_8) of the diagnostic program with a gain of 8 (SW6 and SW7 = 1).
4	Adjust input offset potentiometer (Figure 2-5) on A220 Module for 000 001_8 to 000 000_8 on the console DATA indicators.
5	Set EDC to 0.625V and verify that DATA indicators display the following readouts with specified gain settings:

Data (±1 bit)	SW6	SW7	Gain
000100_8	0	0	1
000200_8	1	0	2
000400_8	0	1	4
001000_8	1	1	8

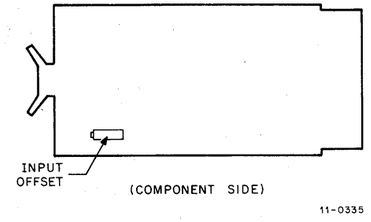


Figure 2-5 A220 Switched-Gain Amplifier

2.6.6 **Multiplexer Setup**

Set up multiplexer as follows:

a. Verify that A124 Multiplexer Switch Modules are installed in the following slots:

CH00	CH03	Slot A17
CH04	CH07	Slot A18
CH08	CH11	Slot A19
CH12	CH15	Slot A20
CH16	CH19	Slot B17
CH20	CH23	Slot B18
CH24	CH27	Slot B19
CH28	CH31	Slot B20

b. If the G735 Test Card Module is available, perform the following procedure:

NOTE

The G735 Module produces eight distinct voltage levels when fed from the EDC. The first level, fed to channels 0, 10_8, 20_8, 30_8 is equal to the input level from the EDC. Each successive level is half the previous one and appears on the next channel, except that the last level is ground. Jumper X should be connected on the module for testing the AD01-D.

Step	Procedure
1	Insert the G735 Module in slot AB21.
2	Connect EDC to the tabs at the handle end, and set EDC to +10V.
3	Set the SR on the console to 270_8 and press start.
4	Load the initial channel of the multiplexer to be tested in DATA bits 00_8 through 04_8, then press CONT. The program will halt.
5	Load the number of channels to be tested in DATA bits 00_8 through 04_8, then press CONT. The program will again halt.
6	Set the SR to all 0s and press CONT. The program should run. After one complete pass, the Teletype bell will sound.
7	Set bit 06 of the SR to 1. The following table is printed:

Channel	Initial Value	Final Value
CH00	1777	1777
CH01	1000	1000
CH02	0400	0400
CH03	0200	0200
CH04	0100	0100
CH05	0040	0040
CH06	0020	0020
CH07	0000	0000
↓		↓
CH37	0000	0000

NOTE

If differences between initial values and final values of more than one count occur, check the multiplexer channel in question. It may be noisy and should be replaced.

c. If the G735 Module is unavailable, perform the following procedure:

Step	Procedure
1	With the program running the Display Conversion Loop (SA 220_8) check each multiplexer channel by moving the EDC to the proper input pins in slot AB21.
2	Verify the correct results on the DATA indicators of the computer.

2.6.7 External Sync

NOTE

Before connecting the external sync to the AD01-D, associated jumpers must be removed. These jumpers are:

EXT IN – A22R2 to A22C2
EXT IN A – B08B2 to B08N2

After connecting the external sync (refer to Table 2-1), the EXTEST and EXFAST Diagnostic Subroutines can be run to verify proper operation of the AD01-D under control of external sync.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 INTRODUCTION

Operation of the AD01-D is controlled entirely by the PDP-11 Computer program. All I/O and control programming is done by issuing the normal memory reference instructions. The nature of the program depends on the system application and the familiarity of the programmer with the particular application and the PDP-11 instruction set.

3.2 ADDRESS FORMAT

The AD01-D is assigned two bus addresses:

a. 776770_8 for the control and status register (CSR)

b. 776772_8 for the data buffer register (DBR).

All information flows between the processor and the AD01-D through these registers. The address format is shown in Figure 3-1.

Figure 3-1 Address Format

3.3 CSR FORMAT

The operating condition of the AD01-D is established by transferring a 16-bit control word or an 8-bit control byte from the processor to the CSR. The status of the AD01-D can be determined by transferring the contents of the CSR to the processor and testing the status bits. The CSR format and bit assignments are illustrated in Figure 3-2. The purpose and description of each bit in the CSR is presented in Table 3-1.

3.4 DBR FORMAT

On command, the AD01-D digitizes the unipolar analog voltage of the selected channel into a 10-bit binary code, using the successive-approximation technique. The bipolar option permits conversion of bipolar analog voltage

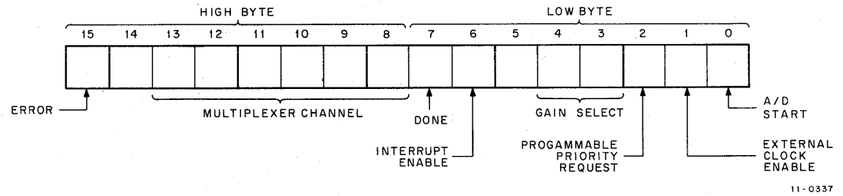


Figure 3-2 CSR Format

Table 3-1
CSR Bits

Bit	Description
15	ERROR(ER) – indicates device has been issued a START command during the time between Start Conversion and Read ADDB. Cleared by INIT. Set by CONVERT command if error condition is present. Cleared under program control when new Gain and MUX Channel data is loaded. **NOTE** **The main purpose of the Error Bit is to indicate timing problems that could occur if an external clock is starting conversions at certain intervals and conversions are being made under program control between the external clock pulses.**
14	Unused.
13-08	MULTIPLEXER CHANNEL (MC) – Selects 1 of 64 multiplexer channels. Loaded under program control. Cleared by INIT.
07	DONE (DN) – Indicates state of converter. Reset by INIT. Set by A/D Done. Reset by reading ADDB. Read only.

(Continued on page 3-2)

Table 3-1 (Cont)
CSR Bits

Bits	Description
06	INTERRUPT ENABLE (IE) – Allows interrupts on A/D Done or Error. Set under program control. Cleared by INIT.
05-03	Unused.
4-3	GAIN SELECT (GS) – Selects gain for programmable gain amplifier. Loaded under program control. Cleared by INIT.
02	PROGRAMMABLE PRIORITY REQUEST SELECT (PS) – Allows selection of bus request line under program control. When bit 02 = 0, bus requests are made at level 7. When bit 02 = 1, bus requests are made at a level determined by bus grant jumper socket on G736 Module. Set under program control. Cleared by INIT.
01	EXTERNAL CLOCK ENABLE (EE) – Allows converter to be controlled by external input. Loaded under program control. Cleared by INIT.
00	A/D START – Start conversion. Loaded under program control. Cleared by INIT. Cleared by A/D Done (Write Only).

into an 11-bit two's complement code with an extended sign format. The digitized analog voltage is stored in the DBR when the conversion is done. A single move instruction can then be programmed to gate the contents of the DBR onto the Unibus. The data format for unipolar and bipolar operation is illustrated in Figure 3-3. Table 3-2 relates the octal representation of the data word to the input analog voltage to highlight differences between unipolar and bipolar operation.

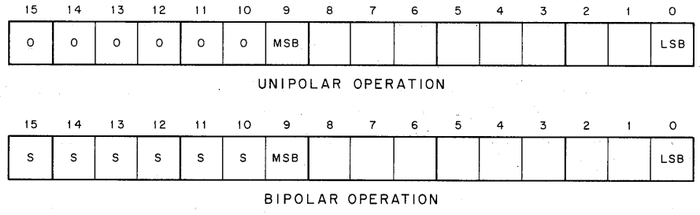


Figure 3-3 DBR Format

3.5 INTERRUPT STRUCTURE

The AD01-D utilizes the interrupt structure of the PDP-11 System to inform the processor that the A/D conversion is done or to indicate that an error condition exists. The interrupt logic in the AD01-D can be enabled or disabled under program control. Bit 06 of the CSR is assigned to enable the interrupt logic. If the interrupt logic is enabled, one of two priority levels can be selected by the program. Bit 02 is assigned to select the priority level. Priority level 7 is enabled when bit 02 is reset, and the priority level established by the bus grant jumper socket on the G736 Module is selected when bit 02 is set. Bus grant jumpers are available for priority levels 4, 5, and 6. When the AD01-D is shipped from the factory, jumper plug S408778 for priority level 5 is installed in the G736 Module.

Table 3-2
Output Notations

Analog Input Voltage*	Unipolar	Bipolar
-10.0	---	176000_8
- 5.0	---	177000_8
0.0	000000_8	000000_8
+ 5.0	001000_8	001000_8
+ 9.9902	001777_8	001777_8

*For 10V full-scale input range. Divide by appropriate gain factor for the input ranges.

3.6 EXTERNAL CLOCK CONTROL

The AD01-D contains two inputs for external control of the conversion process: EXT IN and EXT IN A.

3.6.1 EXT IN

The EXT IN signal is brought into the converter on the M908 Analog Input Module in slot A21, pins A1 and B1 (B1 is EXT common). Input signal conditioning is provided by the M501 Schmitt Trigger circuit. The upper and lower thresholds are set at 1.7V and 1.1V. Input signal swing is limited to ±20V. Input standards are as follows:

Signal swing: ±20V
Loading: 2.7 KΩ to +5V or 1.8 mA at GND

NOTE
Before connecting EXT IN to the AD01-D, the jumper wire from A22R2 to A22C2 should be removed.

3.6.2 EXT IN A

The EXT IN A signal is brought into the converter on the M908 Analog Input Module in slot A21, pins A2 and B1 (B1 is EXT common). This input is T^2L compatible. Triggering is accomplished by a level change from high to low or a pulse to low, the duration of which is $\geqslant$ 50 ns. The fall time of the input trigger should be $<$ 400 ns.

Input standards are as follows:

Signal swing: T^2L logic levels
Timing: Level – high to low fall time $<$ 400 ns
Pulse – high to low, duration $\geqslant$ 50 ns
Loading: 2-1/2 unit loads

NOTE
Before connecting EXT IN A to the AD01-D, the jumper wire from B08B2 to B08N2 should be removed.

3.6.3 External Clock Timing Considerations

Figure 3-4 is a timing diagram that shows the operation of the AD01-D under external clock control. In the external mode, time is not allowed for the switched gain amplifier to settle, thereby initiating a conversion at the time the external signal is applied. Thus, the user must allow at least 5 μs for settling of the input amplifier, if necessary.

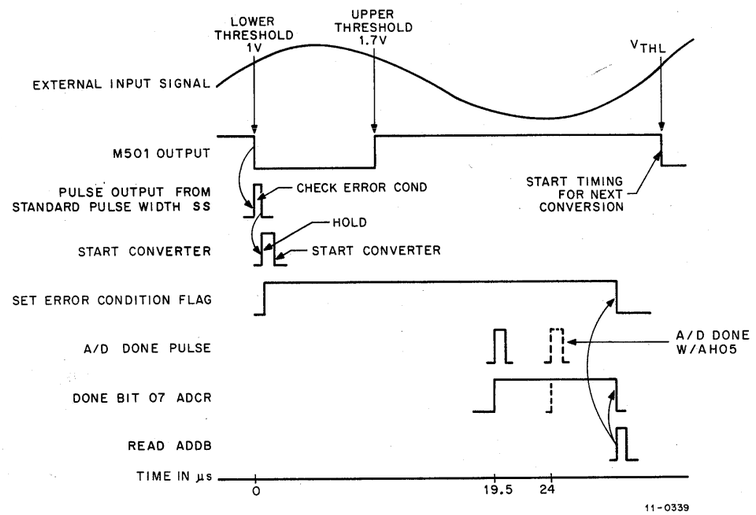


Figure 3-4 External Clock Timing

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 INTRODUCTION

The AD01-D (without options) employs a single high-speed analog-to-digital converter, a gain-selectable amplifier, and an input multiplexer to provide fast multichannel scanning, scaling, and conversion capability. Interface logic compatible with the PDP-11 Computer System is also included in the AD01-D to facilitate direct computer control of the subsystem. This subsystem is intended for use in applications where sampling and processing of analog data from sensors or other external sources is desired. Block and simplified diagrams of the AD01-D are contained in this chapter; detailed block and circuit schematics are included in Chapter 6.

4.2 BLOCK DIAGRAM ANALYSIS

Figure 4-1 is a detailed block diagram of the AD01-D, showing the multiplexer, the gain-selectable amplifier, A/D converter, interface and control logic, and available options. The AD01-D, connected to the Unibus along with other PDP-11 devices, remains dormant unless it is addressed. Two device addresses have been assigned to the AD01-D: One address (776770_8) is used to gain access to the control and status register (CSR); the other address (776772_8) is used to gain access to the data buffer register (DBR). Address Selector M105 recognizes these addresses (A 17:01) and generates clock and gating signals to move data into and out of the AD01-D registers. The mode control bits (C 1:0) and the byte control bit (A 00) determine which of the following clock or gating signals is to be generated by the M105 Address Selector:

a. CLOCK ADCSR WORD
b. CLOCK ADCSR LOW BYTE
c. CLOCK ADCSR HIGH BYTE
d. GATE ADCSR (word)
e. GATE ADDBR (word)

An A/D conversion can be initiated in three different ways:

a. Setting the START bit (ST bit 00) of the CSR by incrementing the CSR word or low byte. This action initiates a conversion of the channel and gain setting that has been established by a previous instruction.

b. Loading a new multiplex channel address into the CSR with a move high byte or word instruction.

NOTE

When the external clock is enabled (EE bit 01 is set), conversions are not started by loading a new channel address or gain setting. The START bit must be set to start the conversion under program control. This feature makes it possible to change gain and multiplex address between external clock pulses.

c. By an external clock. When the external clock is enabled (EE bit 01 is set), a move word instruction cannot be used to enable the external clock and select channel and gain at the same time. This would set the error bit (ER 15).

When a conversion is initiated by setting the START bit, a timing train is generated by the timing generator (see Figure 4-1). The sequence of the timing train and the timing intervals are:

1.	Check error	0.5 μs
2.	Check read	0.6 μs
3.	Hold (CONV H)	5.5 μs
4.	Convert (CONV L)	6.0 μs

The multiplex channel (MC) and GAIN SELECT (GS) bits of the CSR are decoded by the gain and channel decoder to select the programmed channel and gain. The check error pulse produced by the timing generator initializes (clears) the A812 A/D Converter. The Check Error pulse also causes the ERROR bit (ER bit 15) in the CSR to be set if the data of the previous conversion has not been gated out of the DBR. Setting the ERROR bit initiates an interrupt and a trap vector if the interrupt logic is enabled. The second pulse in the timing train, the hold command, causes the A405 Sample and Hold Module to acquire and hold the input analog voltage.

Finally, the Convert pulse is produced to start the A/D converter and set the RD flip-flop. The converter produces 10 output bits, which correspond to the amplitude of the input voltage. The successive (serial) approximation technique is used by the converter. When 10 output bits have been determined, the converter produces an A/D Done pulse to release the A405 Sample and Hold Module so that it will start tracking again and to set the DONE bit (DN bit 07) of the CSR. Setting the DONE bit initiates an interrupt and a trap vector if the interrupt logic is enabled. When a conversion is done, the converter, which serves as the DBR, retains the data word until a new conversion is started. However, if the data is not read before a new conversion is started, an error results. This action is accomplished by the RD flip-flop. Data is read out of the AD01-D simply by programming a move DBR word instruction. This instruction is recognized by the M105 Address Selector, which then generates an ADDBR gate. This gate enables the DBR output drivers to transfer the data onto the Unibus. The gate also resets the RD flip-flop to prevent the error from occurring on the next conversion. Normally, the move DBR word instruction is issued by the processor in response to an interrupt signal from the AD01-D.

As noted before, an interrupt is generated by the M782 Interrupt Control (if enabled) when an error occurs and when the conversion is done. The M782 Module also issues a trap vector (address 000130_8) to inform the processor that the AD01-D issued the interrupt. The processor responds to the interrupt by testing the DONE and ERROR bits of the CSR.

Subject to the result of the test, the program jumps to the move DBR word instruction or an error routine.

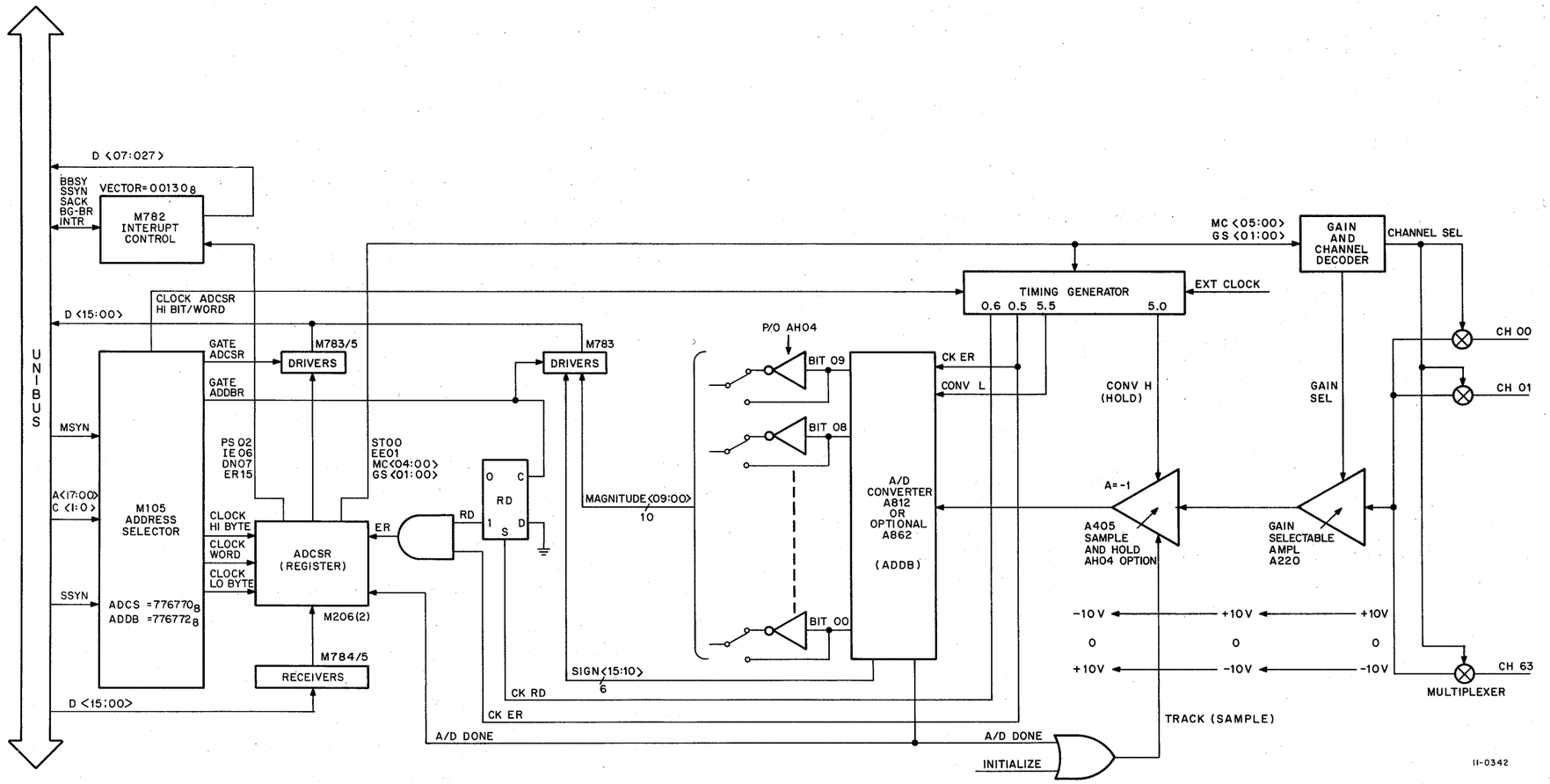


Figure 4-1 AD01-D Block Diagram

4.3 DETAILED CIRCUIT ANALYSIS

The two AD01-D options offer four unique configurations; the following description is organized to reflect these configurations. The order of presentation is as follows:

1. Multiplexer
2. Scaling Amplifier
3. A/D Conversion Configurations
4. Timing
5. Bus Interface

The four configurations accommodate unipolar or bipolar operation with a wide or narrow sampling aperture.

4.3.1 Multiplexer

The multiplexer (drawing D-BS-AD01-D-03) includes at least 4 channels and is expanded to 32 channels in 4-channel increments simply by adding additional A124 Multiplex Modules. The desired channel is selected by a binary decoder that decodes the 6-bit multiplex channel (MC) address received by the CSR. The three most significant bits of the address are decoded by the M161 Octal Decoder to select an A124 Multiplex Module and the two least significant bits of the address are decoded by logic in the multiplexer module itself to select one channel.

4.3.2 Scaling Amplifier

Scaling Amplifier A220 (drawing D-BS-AD01-D-05) provides the AD01-D with an extended dynamic range, the equivalent of up to 14 bits. The amplifier has program-selectable gains of X1, X2, X4, and X8 to achieve this range. The desired gain is selected by a binary decoder (in the associated A124 Module) that decodes the 2-bit gain code received by the CSR.

4.3.3 A/D Converter

The A/D conversion circuits may be configured four different ways using the AH05 Bipolar Option and the AH04 Sample and Hold Option (see Figure 2-1). The sample and hold option reduces the aperture of the AD01-D for skewless sampling applications.

4.3.3.1 **Unipolar with Wide Aperture** – This basic AD01-D configuration is capable of accurately converting unipolar analog voltages. The sampling aperture of this configuration is 17 μs. The configuration consists of the A812 A/D Converter Module and a specific jumper combination as described in Chapter 2. The operation of the A812 Converter is similar to the A811 A/D Converter described in the *Digital Logic Handbook.*

4.3.3.2 **Unipolar with Narrow Aperture** – A sampling aperture of 100 ns is obtained by installing AH04 Sample and Hold Option (see Figure 2-1). This configuration may be useful in analyzing frequency characteristics of unipolar signals or in signal averaging. Installation and calibration procedures are given in Chapter 2. The option consists of a single A405 Module, which is similar to the A404 Module described in the *Digital Logic Handbook.*

4.3.3.3 **Bipolar with Wide Aperture** – Bipolar Option AH05 provides the means for converting bipolar analog voltages. This option consists of a replacement A/D Converter Module (A862). The sampling aperture of this configuration is 24 μs. The converter has a 12-bit conversion capability, but only 11 bits, forming a 10-bit magnitude and 1-bit polarity, are used. The converter uses the successive approximation method in converting analog voltages. A detailed description of the A862 Converter is presented in the *Control Handbook.*

4.3.3.4 **Bipolar with Narrow Aperture** – The Sample and Hold Option (AH04) accommodates skewless sampling of bipolar analog voltages. The sample and hold option reduces the sampling aperture to 100 ns. Installation and calibration procedures are given in Chapter 2.

4.3.4 Timing

All timing pulses are produced by the timing generator circuits (see Figure 4-2) in response to the programmed control word or the external clock. The timing pulses that are produced by the timing generator circuits include the CK ER, CK RD, CONV H, and CONV L pulses. The function of each of these pulses in the A/D converter is described in Paragraph 4.2.

4.3.5 Bus Interface

The M105 Address Selector provides gating signals for up to four device registers. Only two device registers are used in the AD01-D; thus, only two of the select signals from the address selector are implemented. The address selector decodes the 18-bit bus address on A <17:00> to produce the gating signals for the device registers.

To deposit a whole control word into the CSR, both CLOCK ADSCR HIGH BYTE and CLOCK ADSCR LOW BYTE signals are generated at the same time. For more detailed description of the M105 Address Selector Module, refer to the *Digital Logic Handbook* or *PDP-11 Handbook.* The 16-bit CSR and DBR data words are carried on D <15:00> and are gated into and out of the AD01-D registers under control of the gating signals produced by the address selector output logic in response to the programmed instruction. A program-controlled conversion is started simply by depositing a control word or high byte into the CSR, or by incrementing the low byte which sets the START bit (ST00) of the CSR. If the external clock bit (EE01) is reset, all three specified operations activate the timing generator to initiate the conversion. When conversion is complete, the START bit (ST00) is reset and the DONE bit (DN07) is set by the A/D DONE signal. Before a new conversion can be initiated, the data must be read out of the DBR; otherwise, the CSR ERROR bit (ER15) will be set. The ERROR bit is set by the check error (CK RD) signal if the RD flip-flop is not reset by reading the data out of the DBR. The RD flip-flop is set by the CONV signal when the conversion is started, and the CK RD signal is produced each time a conversion is started. Therefore, if another conversion is started before the DBR is read, both RD and CK RD will be high, causing the ERROR bit of the CSR to be set.

The same principles discussed above apply to conversions initiated by an external clock. To effect conversions under external clock control, the external clock enable bit (EE01) of the CSR must be set.

Figure 4-3 illustrates the interrupt logic of the AD01-D. Most of the interrupt logic is contained in the M782 Interrupt Control Module. The interrupt logic allows the AD01-D to request and gain access to the Unibus on a priority basis. There are only two conditions for which the AD01-D may require use of the Unibus: in the event of an error (CSR bit ER15 is set), or when one conversion is done (CSR bit DN07 is set). Before the interrupt logic can request use of the Unibus, the CSR interrupt enable bit (bit IE06) must be set to enable the interrupt logic. Two levels of priority are available to the AD01-D: level 7 and level 4, 5, or 6 as established by Jumper Module G736. Either level can be selected under program control simply by changing the state of the priority select bit (CSR bit PS02). With bit PS02 reset, master control A of the M782 Module is enabled to issue a bus request of the highest priority (BR7). Master control B is enabled to issue a lower priority request (BR4, 5, or 6) when the bit PS02 is set. Setting the DONE or ERROR bits of the CSR activate the enabled master control to issue a bus request. Priority permitting, the processor relinquishes the bus to the AD01-D by issuing a bus grant (BG) signal.

In response to the bus grant signal, the interrupt control of the M782 issues an interrupt command. The vector address of the words in memory contain the address and status of the appropriate device service routine.

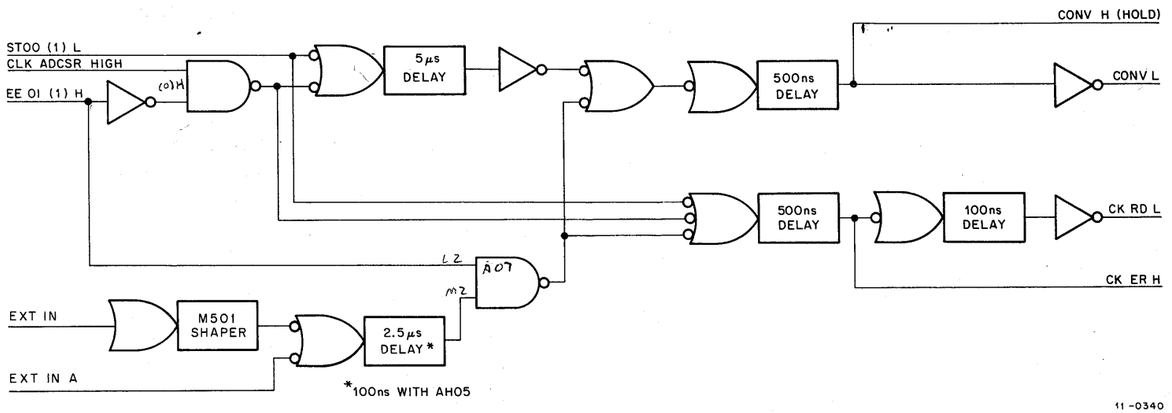


Figure 4-2 Timing Generator Circuit

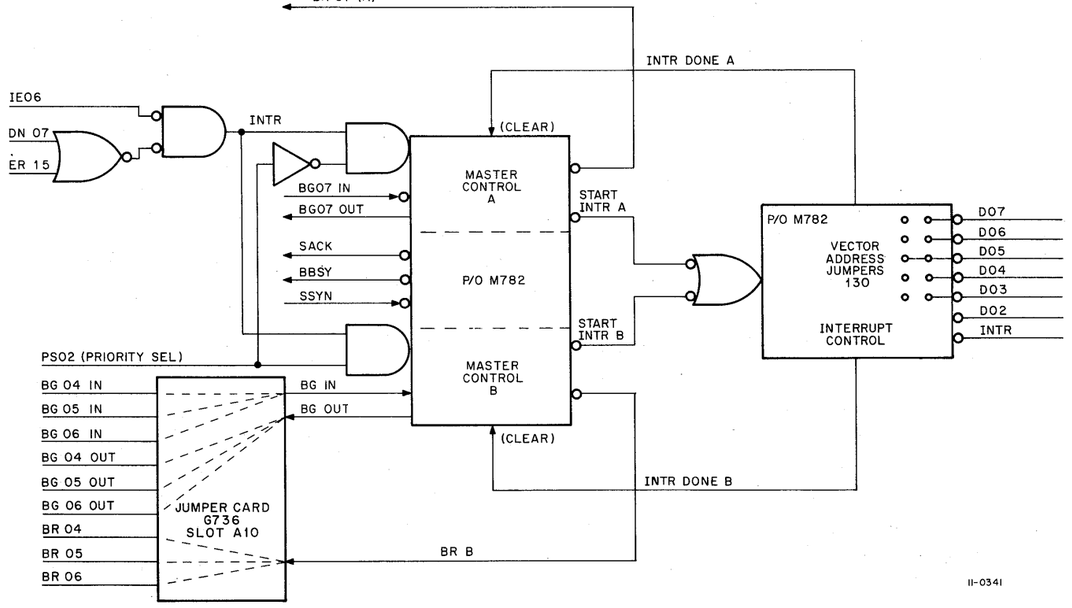


Figure 4-3 AD01-D Interrupt Logic

CHAPTER 5
MAINTENANCE

When operated under normal conditions, the AD01-D Analog Subsystem requires little maintenance (periodic performance of diagnostic programs, cleaning, and inspection). If preventive maintenance is required, follow the procedures outlined in this chapter to return the equipment to maximum operating efficiency.

If a module requires replacement, refer to the spare parts list outlined in this chapter. Do not replace a faulty component without first determining the cause of the failure. Refer to the block schematics associated with each module to determine the location of the components in question.

When conducting a maintenance analysis of the system, make certain that the input conditions required to produce a specified output are met; otherwise, erroneous output readings will result, indicating a nonexisting fault.

5.1 AD01-D MAINDEC-11-D6AB DIAGNOSTIC PROGRAM

The AD01-D diagnostic program is used to test the unique hardware features of the system that cannot be tested with existing MainDEC programs. The program is designed to facilitate troubleshooting by selectively exercising circuits in the AD01-D. Instructions and procedures for loading, operating, and interpreting the results of diagnostic tests are written in clear, concise language for beginning maintenance personnel.

The program tests are divided into the following nine separate tests.

a. **Normal Instruction Tests** – This test consists of 42 subtests that completely checkout the AD01-D logic. Each subtest may be looped 2048 times for reliability.

b. **Conversion Averaging** – This is done with 2 subroutines, CONAV and CONVRT, which together average 128 conversions. SW10=1 inhibits calling these subroutines.

c. **DSPLAY (Display Conversion)** – This routine reads the switch register for channel and gain, performs a corresponding conversion, and displays the result in the data indicators. Thus, calibration can be readily performed, and all channels and gain can be checked directly.

d. **EXTEST (External Conversion Test)** – This routine counts external conversions and prints out after every tenth conversion. It also allows checking for various error cases involving external conversions.

e. **EXFAST (Fast External Conversion Test)** – This routine enables external conversions and checks the error bit after each conversion. An error will occur when the external conversion signal occurs faster than the maximum possible throughput.

f. **FLY (Conversion Print Loop)** – This routine continuously prints the results of conversions at the gain and channel set in the switches. The average of 128 conversions is printed unless SW10 is set. If SW10 is set, the results of single conversions are printed.

g. **TESTX (Single Test Loop)** – This routine allows a single subtest to be run continuously for scope loop purposes. While a scope loop switch option exists, it requires that the user be within the test in which he wishes to loop; in some cases (such as with intermittent failures) that is not easy to do. This subroutine allows the user to load the address of any test from test 0 through test 40 at the halt and then go directly to that test.

h. **WAS-IS (Multiplexer Status, Selection, and Repeatability Test)** – This routine stores an initial conversion value for each channel in the initial table (ITABLE). This initial value is either the average of 128 conversions or the result of a single conversion, depending on the setting of SW10. A single conversion is then taken on each channel and stored in OTABLE (OLD TABLE). From that point, sets of one conversion for each channel are taken and stored in NTABLE (NEW TABLE). OTABLE and NTABLE are compared for ±1 LSB agreement (unless SW9 is set, in which case they must agree exactly; errors are printed out in a CHANNEL XX WAS YYYYYY, is ZZZZZZ format. After the comparison, OTABLE is updated with NTABLE and the process is repeated. If SW5 is set, eight comparisons are made on each channel before going to the following channel. Whenever SW6 is set, a comparison of ITABLE and NTABLE is printed out, which allows drift to be checked. If SW7 is set, NTABLE is compared with ITABLE instead of OTABLE. The bell is rung after every 4096 passes.

i. **SIGMA1 (Repeatability Specification Test)** – This routine tests repeatability to specifications on the channels desired at gains of 4 and 8. Ten thousand conversions are taken at each gain. The specifications have been interpreted to mean that 35 conversions out of the ten thousand may be outside of 2 states at a gain of 4, and the 35 conversions out of ten thousand may be outside of 3 states at a gain of 8.

At a gain of 4, the first 128 conversions are averaged. Then, ten thousand conversions are made, and each is compared to the average. If it is equal to the average, EQUAL is incremented. If it is one less than the average, UNDER is incremented. If it is farther from the average than one count, OUT is incremented. At the end of the ten thousand conversions, a check is made to determine the 2 allowed states (either equal and over or equal and under). The total for the other state (either over or under) is then added to the location OUT. If this total (OUT) is now greater than 35 (DECIMAL), the test fails. The distribution printed out with SW6 or SW7 up is this final setup – the number equal to the average, the number one less than the average, the number one greater than the average, and the total of those differing by more than one count plus those in the nonallowed state.

At a gain of 8, the first 128 conversions are averaged. Then, ten thousand conversions are made, and each is compared to the average. If it is within plus or minus one of the average, EQUAL is incremented. If not, OUT is incremented. At the end of ten thousand conversions, if more than 35 were outside of the 3 allowed states the test fails. The distribution printed out with SW6 or SW7 up is simply the number that were within the 3 states and the number outside of 3 states.

5.2 PREVENTIVE MAINTENANCE

A systematic preventive maintenance program is a useful tool to avert system failures. Proper application of a preventive maintenance program is an aid to both serviceman and user, because detection and prevention of probable failures substantially reduces maintenance and downtime.

Scheduling of computer usage should always include time for maintenance. Careful diagnostic testing can indicate problems that may only occur intermittently during on-line operation.

Weekly program checks and thorough preventive maintenance should be followed, based on the following criteria:

electrical:	1000 hours
mechanical:	500 hours

or at least quarterly.

5.2.1 Preventive Maintenance Tasks

Step	Procedure
1	Clean the exterior and interior of the equipment cabinet using a vacuum cleaner, air blower, or a brush with long soft bristles, and/or cloths moistened in nonflammable solvent. If an air hose is used for cleaning, do not disturb components or wiring.
2	Lubricate hinges, slide mechanisms, and casters, with a light machine oil. Wipe off excess oil.
3	Visually inspect equipment for general condition. Repaint any scratched area with DEC black paint or Krylon Glossy white no. 1501.
4	Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
5	Inspect the following for mechanical security: keys, switches, control knobs, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.
6	Inspect all module mounting panels to ensure that each module is securely seated in its connector. Remove and clean any module that may have collected dirt or dust due to improper air filter service.
7	Inspect power supply components for leaky capacitors, overheated resistor, etc. Replace any defective components.
8	Check the output voltages and ripple contents of the power supply as specified in Paragraph 2.6. Use a multimeter to make these measurements without disconnecting the load. Use an oscilloscope to measure p-p ripple on all dc outputs of the supply. The outputs of the supplies are adjustable; therefore, if any output voltages are not attainable, initiate power supply maintenance. Refer to the block schematic associated with the power supply in question. If ripple content is not within specifications, the power supply is considered defective, and corrective maintenance should be performed.
9	Run AD01-D programs to verify proper equipment operation.
10	Enter preventive maintenance results in a log book.
11	Vibrate the modules and wiring panels, while running the diagnostics.
12	Check all analog adjustments, while running the diagnostics.

5.3 CORRECTIVE MAINTENANCE

The AD01-D Analog Subsystem is constructed of highly reliable modules. The reliability of these circuits, in conjunction with performance of the preventive maintenance tasks, ensures relatively little equipment downtime due to failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct as indicated in the following paragraphs.

The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the block schematics, the operation of specific module circuits, and the location of mechanical and electrical components. Diagnosis and remedial action for a faulty condition can be undertaken logically and systematically in the following phases:

a. Preliminary Investigation
b. System Troubleshooting
c. Logic Troubleshooting
d. Circuit Troubleshooting
e. Repair/Replacement
f. Validation Tests
g. Recording

5.3.1 Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Analyze the problem before attempting to troubleshoot the system. Gather all available information from users who have encountered the problem, and check the system log book for any previous references to the problem.

Do not attempt to troubleshoot using complex system programs alone. Run the AD01-D MainDEC-11-D6AB Diagnostic program and select the shortest, simplest program available that exhibits the error conditions.

5.3.2 System Troubleshooting

When the problem is understood and the proper program has been selected, the logic section of the system at fault should be determined. Obviously, the program that has been selected gives a reasonable idea of what section of the system is failing. However, faults in equipment that transmit or receive information, or improper connection of the system, frequently give fault indications similar to those caused by computer malfunctions.

5.3.3 Logic Troubleshooting

Before attempting to troubleshoot the logic, make certain that proper and calibrated test equipment is available. Always calibrate the vertical preamp and probes of an oscilloscope before using. Ensure that the oscilloscope has a good ac ground and keep the dc ground from the probe as short as possible. Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control pulses or by level transitions that are available on individual module terminals at the wiring side of the logic.

CAUTION

When probing the logic, do not short between pins. Shorting of signal pins to power supply pins may result in damage to components.

5.3.4 Circuit Troubleshooting

Engineering schematic diagrams of each module used in the AD01-D are available; refer to these diagrams for detailed circuit information.

Visually inspect the module on the component side and the printed wiring side to check for overheated or broken components or etch. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

To avoid damaging components, do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested.

Measure the forward and reverse resistances of diodes; diodes should measure approximately 20Ω forward and more than 1000Ω reverse. If readings in each direction are the same and no parallel paths exist, replace the diode.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between collector and emitter, or an open circuit in the base-emitter path, cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50Ω to 100Ω resistance exists between the emitter and the base, or between the collector and the base in the forward direction, and an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy, PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors, the base would be a common-anode connection, and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistance, because many meters apply a positive voltage to the common lead when in the resistance mode.

Because integrated circuits (ICs) contain complex integrated circuits with only the input, output, and power terminals available, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best accomplished under dynamic conditions using a module extender to make terminals readily accessible. Using AD01-D block schematics and module schematics, proceed as follows to locate an IC on a circuit board:

Step	Procedure
1	Hold the module with the handle in your left hand with the component side facing you.
2	ICs are numbered starting at the contact side of the board, upper right-hand corner.
3	The numbers increase toward the handle.
4	When a row is complete, the next IC is located in the next row at the contact end of the board (see Figure 5-1).
5	The pins on each IC are located as illustrated in Figure 5-2.

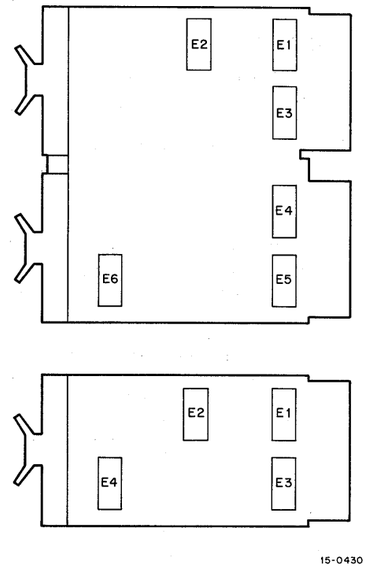


Figure 5-1 IC Location

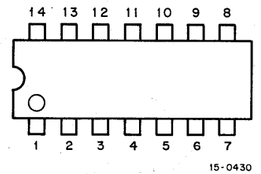


Figure 5-2 IC Pin Location

5.3.5 Validation Tests

Return repaired modules to the location from which they were removed. If a defective module is replaced by a new module while repairs are being made, tag the defective module and note the location from which it was taken and the nature of the failure. When repairs are completed, return the repaired module to its original location, and confirm that the repairs have resolved the problem by running all tests that originally exhibited the problem.

NOTE

If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests.

5.3.6 Recording

Maintain a log book (supplied) of AD01-D failures and corrective maintenance. All maintenance should be recorded in this book. Record all data indicating the symptoms of the fault, the method of fault detection, the component at fault, and any comments that would be helpful in maintaining the equipment in the future.

The log should be maintained on a daily basis, recording all operator usage and corrective maintenance results.

5.4 TEST EQUIPMENT

To service the AD01-D Analog Subsystem, the equipment listed in Table 5-1 is recommended. If recommended equipment is not available, alternate equipment with the same performance specifications should be used.

Table 5-1
Test Equipment Required

Equipment	Manufacturer	Designation
Voltage Standard (EDC)	Electronic Development Corporation	MV-100 (or equivalent)
10:1 Divider	DEC	No. 29-16810
Digital Voltmeter	Hewlett Packard	HP-3460 (or equivalent)
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 453 (or equivalent)
Probe (2)	Tektronix	P6010
X10 Probe (2)	Tektronix	P6008
Module Extender (2)	DEC	W982
Multiplexer Checkout Module	DEC	G735

5.5 MODULE HANDLING AND REPAIR

To insert or extract modules, first turn off all power. To gain access to components on a module, remove the module by exerting a straight, even pull on the module handle to prevent twisting of the printed-wiring board. Insert a type W982 Flip-Chip Module extender into the vacated module mounting panel, then insert the module into the extender. Use two W982 Extender Modules for dual modules.

Do not attempt to repair, adjust, or calibrate the A862 and A812 Analog-to-Digital Converter modules except as noted in the Acceptance and Calibration procedure (A-SP-AD01-12 and 11).

NOTE
Failure to follow this rule may violate the warranty.

5.6 SPARE PARTS

The customer should maintain a spare parts inventory of those modules listed in Table 5-2.

Table 5-2
Spare Parts List

Type/Part No.	Name	Quantity
A124	Four-Input Multiplexer Switch	1
A124*	Four-Input Multiplexer	1
A220	Selectable Gain Buffer Amplifier	1
A862 (AH05)*	Bipolar A/D Converter	1
A405 (AH04)*	Sample and Hold	1
A708	Dual Voltage Regulator	1
A812	10-Bit A/D Converter	1
G736	Request Jumper	1
M105	Address Selector	1
M111	Inverter	1
M112	NOR Gate	1
M113	10 2-Input NAND Gates	1
M161	Binary to Octal/Decimal Decoder	1
M206	Six Flip-Flops	1
M302	Dual Delay Multivibrator	1
M501	Schmitt Trigger	1
M617	6 4-Input NOR Buffers	1
M782	Interrupt Control	1
M783	Unibus Drivers	1
M784	Unibus Receivers	1
M785	Unibus Transceivers	1
M908	Connector	1

*Denotes optional modules.

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains a listing of DEC block schematics and cabling diagrams which are referenced in other chapters of this maintenance manual and are contained in Volume II of this manual. These drawings provide detailed information about the logic and wiring of the AD01-D peripheral.

Table 6-1
AD01-D Engineering Drawings

Drawing Number	Title
D-UA-AD01-D-0	10-Bit ADC with Switched Gain
D-MU-AD01-D-02	Module Utilization
D-BS-AD01-D-03	
D-BS-AD01-D-04	Interface and CSR (2 sheets)
D-BS-AD01-D-05	A/D Converter (2 sheets)
D-IC-AD01-D-06	Analog Input Connectors
D-CS-A812-0-1	10-Bit ACD A812
C-CS-A405-0-1	Sample and Hold A405
D-AD-7006919-0-0	Wired Assembly (AD01-D)
C-CA-H727-A-0	H727-A Power Supply, 115V
C-UA-H727-B-0	H727-B Power Supply, 230V
D-UA-H716-B-0	H716-B Power Supply, 115V
D-UA-H716-D-0	H716-D Power Supply, 230V

APPENDIX A
10—BIT UNIPOLAR CALIBRATION CHART

Date:
Serial No:

AD01-D
10 Bit Unipolar
CALIBRATION CHART

Switching Point		Gain=1 ±10mv ±12.5mv w/AH04		Gain=2 ±5mv ±6.25mv w/AH04		Gain=3 ±2.5mv ±3.125mv w/AH04		Gain=4 ±1.25mv ±1.56mv w/AH04	
From	To	Theor. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage
000000	000001	0.0049		0.0029		0.0012		0.0006	
000001	000002	0.0146		0.0073		0.0036		0.0018	
000003	000004	0.0342		0.0171		0.0085		0.0043	
000004	000005	0.0439		0.0220		0.0110		0.0055	
000007	000010	0.0732		0.0366		0.0183		0.0091	
000010	000011	0.0829		0.0415		0.0207		0.0104	
000017	000020	0.1514		0.0757		0.0378		0.0189	
000020	000021	0.1611		0.0806		0.0403		0.0201	
000037	000040	0.3076		0.1538		0.0769		0.0385	
000040	000041	0.3173		0.1587		0.0793		0.0397	
000076	000077	0.6103		0.3051		0.1526		0.0763	
000077	000100	0.6201		0.3101		0.1550		0.0775	
000100	000101	0.6298		0.3149		0.1575		0.0787	
000176	000177	1.2353		0.6177		0.3088		0.1544	
000177	000200	1.2451		0.6226		0.3113		0.1556	
000200	000201	1.2549		0.6274		0.3137		0.1569	
000376	000377	2.4853		1.2427		0.6213		0.3107	
000377	000400	2.4951		1.2476		0.6238		0.3119	
000400	000401	2.5049		1.2524		0.6262		0.3131	
000776	000777	4.9853		2.4927		1.2463		0.6232	
000777	001000	4.9951		2.4976		1.2488		0.6244	
001000	001001	5.0049		2.5024		1.2512		0.6256	
001376	001377	7.4853		3.7427		1.8713		0.9357	
001377	001400	7.4951		3.7476		1.8738		0.9369	
001400	001401	7.5049		3.7524		1.8762		0.9381	
001576	001577	8.7353		4.3677		2.1838		1.0919	
001577	001600	8.7451		4.3726		2.1863		1.0931	
001600	001601	8.7549		4.3774		2.1887		1.0944	
001775	001776	9.9756		4.9878		2.4939		1.2470	
001776	001777	9.9853		4.9927		2.4963		1.2482	

APPENDIX B
11–BIT BIPOLAR CALIBRATION CHART

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 1/22/71

TITLE AD01-D Calibration Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
		A	SP	AD01-D-11	

DEC FORM NO.
DRA 107

ENGINEERING SPECIFICATION

digital CONTINUATION SHEET

TITLE AD01-D Calibration Procedure

1.0 General Description

This document covers the setup, checkout and calibration of model AD01-DA or -DB analog-to-digital converter subsystems for the PDP-11 family of computers. It also includes information on the installation and adjustment of the AH04 sample and hold option and the AH05 sign bit option.

1.1 Equipment Required

1. PDP-11 Computer
2. Voltage Standard (Electronic Development Corporation MV-100 OREQUIV)
3. Pulse Generator (Data Pulse Wavetek or Equiv.)

Item 1 will hereafter be referred to as the computer.
Item 2 will hereafter be referred to as the EDC.
Item 3 will hereafter be referred to as the Wavetek.

1.2 Software Required

AD01-D MainDec 11-D6AB

2.0 Setup Procedure

Connect the Unibus cable, type BC11, from slots A1, B1 to the computer. Connect the power supply socket and fuseholder (H727) to the service outlet on the computer. Connect the 5 volt logic supply (H716) to the terminal strip on the left end plate as indicated. Insert the following modules:

M930 in slot	AB02
M105	A03
M782	B03
M784	A04
M785	B04
M783	A05
M783	B05
M206	A06
M206	B06
M113	A07
M112	B07
M111	A09
M617	B09
G736	A10
M161	B10

SIZE	CODE	NUMBER	REV
A	SP	AD01-D-11	

DEC FORM NO 16-1022

M302 A11
M302 B11
A708 AB24

Note: Any accurate (±.05%) voltage measuring device can be used in place of a DVM, such as the null meter of the EDC with a 10:1 precision divider network.

2.1 Turn on power to the computer and AD01-D load the referrenced diagnostic program into the computer. While the tape is reading in connect the DVM between pins A3A2 and A3C2 (ground). The reading should be between 4.75v and 5.25v. If it is not,the trouble is in the H716 power supply.

2.1.1 Next connect the DVM between pins B12D2 and A14F2 (F2 is ground) and adjust the +15 volt pot on the regulated power supply (H727 mounted at right of 1943 rack) for between 15.0 and 15.1 volts. Use a 1/8" blade screwdriver for power supply adjustment.

Note: If the power supply has a blue case (Power Mate) the adjustment pots are accessible through the top surface. If it has a black case (Deltron) the pots must be reached through the bottom. In either case, the 15 volt pot is closest to the end plate. The remaining pot is the 20 volt adjustment and is referred to in 2.1.2.

2.1.2 Connect the DVM between pins B19E2 and A19F2 (ground). Adjust the 20 volt pot on the regulated supply (H727) for a DVM reading between 20.0 and 20.1 volt (negative).

2.1.3 Connect the DVM between pins B12E2 and A14F2 (ground). The voltage should be between - 14.8 volts and -15.3 volts. If it is higher, the trouble is in the A708 module. If no voltage, or a very small is present check for shorts in the panel or try changing the A708.

2.2 Interface Checkout

2.2.1 Insert the A812 module in slots AB12. Set the SR to 200 and load address. Reset the SR to zero and start. Push continue twice, then set SR 11 to a one and push continue again. The diagnostic should now run. If the logic is not performing correctly the program will type out the location in the program where the failure took place. In this case, SW13 should be put up to inhibit typeouts and SW14 put up to provide a scope loop. Then referring to the block schematics the particular problem can be corrected. Failing the gain linearity test at this point is not a failure since the programmable gain amplifier is not in the circuit. The diagnostic will ring the teletype bell upon completion of a pass.

2.2.2 Set 270 in the SR and load address. Set the SR to zero then hit continue, now set the SR to one and hit continue again. Finally set the SR to 13 and hit continue the program should now run but no printouts will occur. Now take an oscilloscope with the trigger set to internal proceed to set the one-shot timing as follows:

Pin A11F2 - 5 usec
Pin A11T2 - 500 nsec
Pin B11F2 - 500 nsec
Pin B11T2 - 100 nsec

2.3 A/D Converter Adjustment

2.3.1 Connect the EDC between pins B12V2 and B12F2 (F2 is ground) and set dials for zero volts. Load address 220 and start. Reset the SR to zero. This part of the program displays the A/D converter results via the panel lights of the computer. If the converter is functioning the lights will change as the EDC voltage is increased from zero toward +10 volts. At zero volts no lights should be on, and by +11 volts all lights except for D15 thru D10 should be on (the ten converter bits appear in DØØ to DØ9).

2.3.2 Set the EDC at +5 millivolts and see if the presentation fluctuates between 00000 and 00001 (octal). If it does not, move the EDC up and down around 5mV until such a point is found. If it is between +3 and +7

millivolts, no adjustment is needed. If farther off than that, the zero balance pot on the A812 module must be adjusted. This pot is a single turn 1/4 inch diameter component located near the lower edge of the board about halfway between the pins and the handles. It should be adjusted with the A812 on extender modules. Reset the EDC to +4.9mV and tweak this pot until DØØ just blinks on and off, with all other accumulator lights off. Replace the A812 directly in the socket and recheck. It is normal for the switching point to move a millivolt or two.

2.3.3 Now set the EDC to +9.9853 volts. Turn the full scale adjust pot on the A812 (between the handles) until the presentation fluctuates between 001776 and 001777 (octal). Again, getting this transition within a millivolt or two of the theoretical value is good enough. Check several of the transitions in the first column of the unipolar calibration chart at the back of this document (gain=1 column). If the transitions are all within 10mv of theoretical, the converter is working satisfactorily. If the lights blink randomly at any point, check all the power supply voltages with an AC coupled oscilloscope on its most sensitive range (5mV/div). These voltages and pins are the same as were checked with the DVM, previously. Stop the program and look for oscillations with the scope internally synchronized. If 10X scope probes are used, any repetitive waveform more than 1/4 division peak-to-peak is cause to replace the power supply (or the A708 regulator if the -15 volts is the only supply with a problem).

2.4 Switched Gain Amplifier Adjustment

2.4.1 Insert modules A124 (slot B16) and A220 (slot A16). Connect the EDC between pins A16P2 and A16F2 (ground). Connect the DVM between pins A16V2 and A14F2 (ground). Set the EDC to zero. Adjust the pot on the A220 until the DVM reads zero within 1 millivolt. Start the diagnostic program at 220 set SR6 and SR7 to ones.

This should set the A220 to a gain of 8.

2.4.2 Set EDC to +0.625 volt. The data on the computer should now read 001000 (octal). Set SR6 back to zero. The data should now read 000400. Now set SR7=0 and SR6=1. The data should now read 000200. Finally, set SR6=0 and SR7=0. The data should now read 000100.

2.4.3 If gross errors are experienced in the last test, remove the A124 from B16. Connect a jumper from A16S2 to B16R2, T2, U2, and V2 in turn. If the A220 is good, the sequence of readings on the DVM should be +5.000 volts, +2.5 volts, +1.25 volts and +0.625 volts. If this test passes but 2.4.2 does not, the problem is probably in the A124 (B16). If the switch register has no effect whatsoever, try the M206 (A06).

Now restart the diagnostic at 210. The gain linearity test should now pass. If it does not the problem is probably in the A220 module.

2.5 Multiplexer Setup

2.5.1 Insert the A124 modules as required:

CH00	CH03	Slot
04	07	A17
08	011	A18
12	15	A19
16	19	A20
20	23	B17
24	27	B18
28	31	B19
		B20

2.5.2 If the G735 test card is available proceed as follows. Insert the G735 in slots AB21 and connect the EDC to the tabs at the handle end. Set the EDC to +10.000 volts. Set the SR of the computer to 270 and start. Now load the initial channel of the multiplexers to be tested in bits D00 to D04 (octal) then hit continue. The program will again halt, now load the number of channels to be tested in SR (DØØ to D04) again in octal, and hit continue. Set SR to zero and hit continue again the

program should now run. The was-is printout may or may not occur regardless of this set SR6 to a one. The following table will now print out:

CHANNEL	INITIAL VALUE	FINAL VALUE
CHØØ	1777	1777
CHØ1	1000	1000
CHØ2	0400	0400
CHØ3	0200	0200
CHØ4	0100	0100
CHØ5	0040	0040
CHØ6	0020	0020
CHØ7	0000	0000
↕		↕
CH31		0000

If differences in initial and final values of more than 1 count occur then check the multiplexer channel in question it may be noisy and should be replaced.

2.5.3 If the G735 test card is unavailable then with the program running the display conversion loop (SR 220) each multiplexer channel may be checked by moving the EDC to the proper input pins in slot AB21 and verifying the proper results on the data lights of the computer.

2.5.4 If the system is now fully configured for shipment, run through the unipolar calibration chart at the back of this document. Fill in all lines for a gain of 1, and spot check 4 to 7 readings at each other gain. Note that "triple stating", or skipped codes are acceptable on a gain of 8.

2.5.5 If the AH04 sample and hold option, or the AH05 sign option or both are ordered, proceed to the installation and checkout procedure for those options before filling out the calibration chart. If the AH05 is implemented, use the bipolar calibration chart and remember to inform the diagnostic of the bipolar number format by keying in SR8=1 at the third halt after starting at 200.

2.6 External Sync:

2.6.1 Delete the following wire:

A22R2 to A22C2

Insert the M501 module in slot A22. Connect a wavetek to pins A21A1 and A21B1 (ground). Set the frequency to 0.5 cycles/sec. and the voltage to 5V peak to peak for a sine wave or a 5 volt pulse for a pulse generator. Load and start the diagnostic program at 230, the program should now run printing out each time 10 conversions have been performed. By varying the frequency of the Wavetek the conversion rate will also vary. Now set SW5=1, this causes the program not to set the external enable bit and no printouts should occur. Now set the frequency to 5KHz and connect a scope to pin B08T2. This is the second one shot on the M302 module. The pulse width of this signal should be adjusted for 100 nsec. When this is complete turn power off and add the wire at A22R2 to A22C2.

2.7 Board Cleanliness

2.7.1 The performance of high impedance analog modules, such as A124, A220, A405, can be severely affected by dirt and moisture. Fingerprints are the worst offenders. If erratic or marginal analog performance is observed, clean all of these modules with soap or detergent and water, rinsing well. A conventional dishwasher is best, as it will dry the modules. Attempts to dry modules with a compressed air nozzle will be successful only if the air supply is filtered and oil free. After washing, handle boards only by edges and handles.

2.8 Diagnostic Program Features

The calibration chart can be filled in by using the program at starting address 220 and observing the codes in the accumulator. The printout in paragraph 2.5.2, however, has several useful features. As normally used, each number is the average of 100 (octal) conversions (64 decimal).

The program continually calculates and updates a table of these channel readings. If at any time a

difference of more than one count is found between the old and new reading, a printout is generated, such as:

CHØ5 WAS ØØ4Ø IS ØØ36

If an intentional change is made, such as by changing the EDC setting, or changing the gain by means of SR4 or 5, this printout may not occur, or may pass through spurious values unrelated to the intentional change before settling out to the correct numbers. To guard against these problems, stop the program, make the change, and then hit key continue. The program will therefore be "blinded" during the unpredictable switching transients. Make sure the overload lite on the EDC goes out before allowing the program to continue.

If SR10 is set to a one, the program will monitor single conversions rather than 100 conversion averages. Errors due to external noise, which might be suppressed by averaging, are thereby made evident by a printout. In cases of severe power line or radiated noise, the printer may be kept continuously busy.

If SR9 is set to a one, printout will occur on changes of only one count as well as larger changes. Again, external noise will be more evident.

SR6 and SR7 always control the gain as shown below:

SR7	SR6	GAIN
Ø	Ø	1
Ø	1	2
1	Ø	4
1	1	8

Further information is contained in the listings and description of the diagnostic program.

2.9 G735 Voltage Divider Test Module

The G735 module produces 8 distinct voltage levels when fed from the EDC. The first level, fed to

channels 0,10,20,30 is equal to the input level from the EDC. Each successive level is half the previous one, and appears on the next channel, with the exception that the last level is ground. Do not ship the G735 with the system. It should be replaced by two M908 modules at the end of acceptance.

3.0 Installation of Options

Due to the nature of the various options offered on the AD01 there will be a separate section on installation of the AH04 Sample and Hold (Sec. 3.1). AH05 Sign Bit (Sec. 3.2), and the combination of the two options AH04, AH05 (Sec. 3.3).

3.1 AH04 Sample and Hold

3.1.1 Back Wiring Changes:
Delete the following:

A15S2 to A15V2
AØ9A1 to AØ8D1
C1 to AØ8E1
D1 F1
F1 H1
E2 J1
J1 K1
H2 L1
L1 M1
K2 N1
N1 P1

Add the following wires:

AØ8D2 to AØ8D1
E2 to E1
F2 to F1
H2 to H1
J2 to J1
K2 to K1
L2 to L1
M2 to M1
N2 to N1
AØ8P2 to AØ8P1

3.1.2 A405 Module

Referring to Figure 3.1.2, of the A405 module connect a jumper between split lugs A and B then insert the A405 in slots AB15. Perform the following steps:

1. Connect the EDC to CHØØ if it is implemented A21B2, A21C2 (gnd). If not, connect the EDC to the amplifier (A220) input A16P2, A16F2 (gnd).

2. Set the EDC to -5mv. Start diagnostic program at 220.

3. Adjust the bias pot on the A405 module (Figure 3.1.2) so that data bit ØØ just blinks on and off.

4. Stop the program and turn power off.

5. ADD the following wires to the back panel wiring:
   A15E2 to B15M2
   A15U2 to B15J2

6. Connect the DVM between pins A15U2 and A15F2 (gnd). Set the EDC to 0 volts.

7. Adjust the offset course pot (Figure 3.1.2) so the DVM reads -10.000 volts as possible.

8. Adjust the offset fine pot (Figure 3.1.2) so the DVM reads -10.000 volts.

9. Connect the DVM between pins A15V2 and A15F2 (gnd), the reading should be 10.000 volts. If it is not the procedure should be repeated. The wiring added in Step 5 must be removed before the procedure is started again. Refer to sections 2.5.4 and 2.5.5 and 2.6 for final checkout instructions.

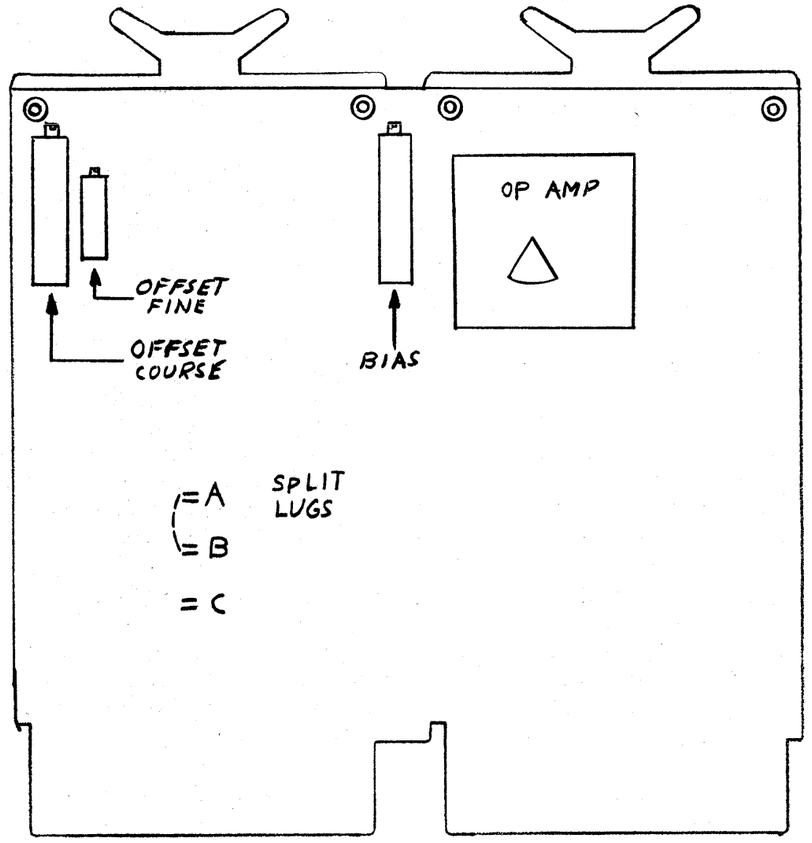


Figure 3.1.2
A405 Module
Component Layout

3.2 AH05 Sign Bit Option

3.2.1 Back Wiring Changes

Delete the following:

AØ5D1 to AØ5C2

Add the following:

BØ8F2 to AØ9V1

3.2.2 The A812 module should be removed from slot AB12 and the A862 module put in slot AB13. Remove the A220 slot A16 and connect the EDC to A16V2 and A16F2(Ground). Set the EDC to +5MV.

3.2.3 A862 Conversion Time

This step will set the conversion time of the A862 A/D converter. First load and start the diagnostic at 270. At the first halt reset the switch register to all zeros and hit continue, at the next halt hit continue again. At the third halt set SW-13 to a one and hit continue. The program should now run performing the Was-Is Test. No printouts will occur since SW13=1. Connect an Osciloscope set at 2V/Div, 10 usec/CM to Pin B13 F1. A positive pulse anywhere from 10 usec to 50 usec should be present. The length of this pulse should be adjusted to 24 usec ± 0.1 usec by means of the clock potentiometer located between the handles on the A862 module. Next connect the scope to BØ8F2 and adjust the top pot on the M302 O.S. to 1 usec.

3.2.4 Offset Adjustment

With the EDC connected as in Section 3.2.2 (@ 5MV) put the diagnostic in the display conversion loop. (SA220). Adjust the offset pot located in the end of the top metal covering on the A862 module so that the LSB just flashes on and off. Turn power off and replace the A220 module. Connect the EDC to pins A16P2 and A16F2 (ground) and set it to 600 microvolts. Start the diagnostic at 220 and set to a gain of 8 (SW6-SW7 =1) Now adjust the offset pot on the A220 so that the LSB just switches on and off. The AH05 is now installed. If this is the last option

to be installed, refer to sections 2.5.4, 2.5.5 and 2.6 for final instructions.

3.3 Installation of AHØ4 with AHØ5 Installed.

3.3.1 Delete the following wires:

AØ9A1	to	AØ8D1
C1		E1
D1		F1
F1		H1
E2		J1
AØ9J1		AØ8K1
H2		L1
L1		M1
K2		N1
N1		P1
B13E2	to	AØ5E1
A15S2	to	A15V2

Add the following wires:

AØ8D2	to	AØ8D1
E2		E1
F2		F1
H2		H1
J2		J1
K2		K1
L2		L1
M2		M1
N2		N1
P2		P1
AØ5E1		B13F2

Referring to Figure 3.1.2 of the A405 module connect a jumper between split lugs A and B then insert the A405 into slots AB15.

3.3.2 Remove the A220 slot A16 and connect the EDC to pin A15S2 and A16F2 (ground). Set the EDC to +5MV and start the Diagnostic at 220. Adjust the offset pot on the A405 module (Figure 3.1.2) for LSB switching at 5MV.

3.3.3 Stop the program and turn power off. Connect the EDC to Pins A16P2 and A16F2 (ground) and install the

A220 module slot A16. Start the diagnostic at SA220 and set the EDC to 600 microvolts. Set the gain to eight (8) SW6, SW7=1 and adjust the offset pot on the A220 for LSB switching. This completes the installation of the AHØ4 with AHØ5. Refer to Sections 2.5.4, 2.5.5 and 2.6 for final instructions.

AD01-D
10 Bit Bipolar
CALIBRATION CHART

Date:
Serial No:

Switching Point		Gain=1 ±10mv ±12.5mv w/AHØ4		Gain=2 ±5mv ±6.25mv w/AHØ4		Gain=4 ±2.5mv ±3.125mv w/AHØ4		Gain=8 ±1.25mv ±1.56mv w/AHØ4	
From	To	Theor. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage
001777	001776	9.9853		4.9926		2.4963		1.2482	
001776	001775	9.9756		4.9878		2.4939		1.2470	
001001	001000	5.0049		2.5024		1.2512		0.6256	
001000	000777	4.9951		2.4976		1.2488		0.6244	
000777	000776	4.9853		2.4927		1.2463		0.6232	
000601	000600	3.7549		1.8774		0.9387		0.4694	
000600	000577	3.7451		1.8726		0.9363		0.4681	
000201	000200	1.2549		0.6274		0.3137		0.1569	
000200	000177	1.2451		0.6226		0.3113		0.1556	
000021	000020	0.1611		0.0806		0.0403		0.0201	
000020	000017	0.1514		0.0757		0.0378		0.0189	
000004	000003	0.0342		0.0171		0.0085		0.0043	
000003	000002	0.0244		0.0122		0.0061		0.0030	
000002	000001	0.0146		0.0073		0.0036		0.0018	
000001	000000	0.0049		0.0024		0.0012		0.0006	
000000	177777	-0.0049		-0.0024		-0.0012		-0.0006	
177777	177776	-0.0146		-0.0073		-0.0036		-0.0018	
177776	177775	-0.0244		-0.0122		-0.0061		-0.0030	
177775	177774	-0.0342		-0.0171		-0.0085		-0.0043	
177750	177747	-0.2393		-0.1196		-0.0598		-0.0299	
177747	177746	-0.2490		-0.1245		-0.0623		-0.0312	
177600	177577	-1.2549		-0.6274		-0.3137		-0.1569	
177577	177576	-1.2647		-0.6324		-0.3162		-0.1581	
177001	177000	-4.9951		-2.4976		-1.2488		-0.6244	
177000	176777	-5.0049		-2.5024		-1.2512		-0.6256	
176777	176776	-5.0147		-2.5074		-1.2537		-0.6269	
176300	176277	-8.1299		-4.0649		-2.0325		-1.0162	
176277	176276	-8.1396		-4.0698		-2.0349		-1.0175	
176003	176002	-9.9756		-4.9878		-2.4939		-1.2470	
176002	176001	-9.9853		-4.9926		-2.4963		-1.2482	

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