# MAGNETIC
# TAPE CONTROL
# 516
## INSTRUCTION MANUAL
## VOLUME 1

**DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS**

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# CHAPTER 1

# INTRODUCTION

## PURPOSE AND SCOPE

The purpose of this instruction manual is to aid personnel in the installation, operation, and maintenance of the DEC Magnetic Tape Control 516 and the associated Interface Unit Type 520, 521, or 522A (Figure 1-1).

## MANUAL ORGANIZATION

Volume I presents a brief description of the system application and specifications in Chapter 1, Introduction. Chapter 2, Tape Control Inputs and Outputs, explains the principal signals exchanged between the tape control and the adjacent units of the PDP-6 system. The next four chapters, Chapters 3 through 6, contain the theory of operation of the tape control logic itself. Chapters 7 through 9 describe the theory of operation for the three types of interface unit that may be used with the tape control, the 520, 521, and 522A, respectively. Chapter 10, Maintenance, contains information useful for inspection, troubleshooting, and repair. Chapter 11, Installation, explains the procedures to be followed when first unpacking and installing the tape control and interface.

Volume II presents complete signal glossary lists in Chapter 12 for the Type 516 Tape Control, and Types 520, 521, and 522A Tape Control Interface Units. Chapter 13 contains introductory information on DEC drawing conventions and all pertinent engineering drawings for this manual.

## Figures

This manual includes four general classes of figures: engineering logic drawings; flow diagrams; circuit schematics; and miscellaneous figures such as photographs, block diagrams, and logic rack layout diagrams. The complete system logic for the tape control is shown in the engineering logic diagrams referenced in Chapter 3 and contained in Volume II. The interface logic is shown in the engineering logic diagrams referenced in Chapters 7, 8, and 9. Flow
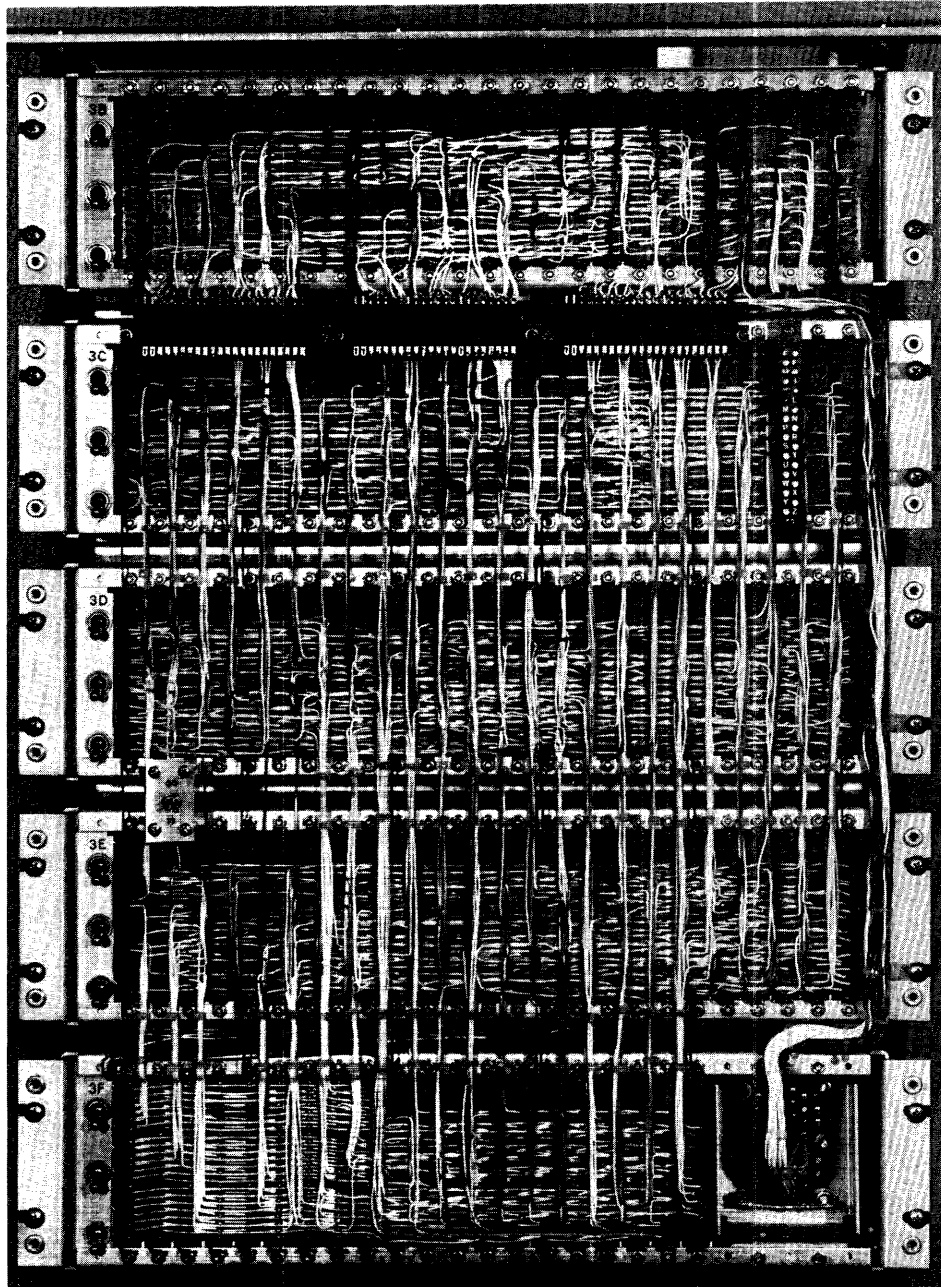
Figure 1-1   Magnetic Tape Control Type 516
and Tape Control Interface Type 521

diagrams of the various system operations are presented in text with Chapters 3 through 6. Circuit schematics and logic rack layout diagrams are contained in Chapter 13.

At the date of issue of this manual, up-to-date engineering drawings are included in Chapter 13. However, in time engineering changes do occur, thus if any discrepency exists between the engineering drawings of this manual and a current set of engineering drawings, the current engineering drawing set is correct.

All engineering logic drawings in Chapter 13 are arranged numerically for quick reference. Furthermore, all circuit schematics of Chapter 13 are arranged in order of circuit type designation (e.g., Negative Diode Module 4114 precedes Diode Module 4115).

## USE OF MANUAL

This manual is intended to serve two purposes: instruction and reference. Chapters 2 through 9 on theory of operation are intended primarily for instruction. These chapters cover the major logical networks and operating sequences of the system in a systematic and detailed manner, but they are not organized for rapid reference. After being read, they rarely need be referred to again.

Once they have been thoroughly understood, the engineering logic drawings and the flow diagrams provide the fastest and most extensive source of reference data. After a reasonable learning period a competent maintenance engineer can orient logic function with particular drawings and even the approximate area of the drawing which shows given sections of the logic.

The flow diagrams add a time dimension to the logic drawings by providing sequential summaries of the specific operations performed during each type of command. Further reference data is provided in Chapter 12, which contains signal glossaries for the tape control and the three interface units.

## SYSTEM APPLICATION

The magnetic tape system provides computer input-output at much faster data rates than most other peripheral devices. It is frequently used as high-capacity storage to augment core memory. Figure 1-2 is a block diagram showing typical tape system configurations. A given system

uses one of three types of interface units; the choice depends on the type of tape transport to be driven. Up to eight transports can be used by each interface-control combination. During both output and input operations, the Magnetic Tape Control 516 receives control information from the processor and generates appropriate signals to cause the interface and selected transport to correctly execute the programmed command.
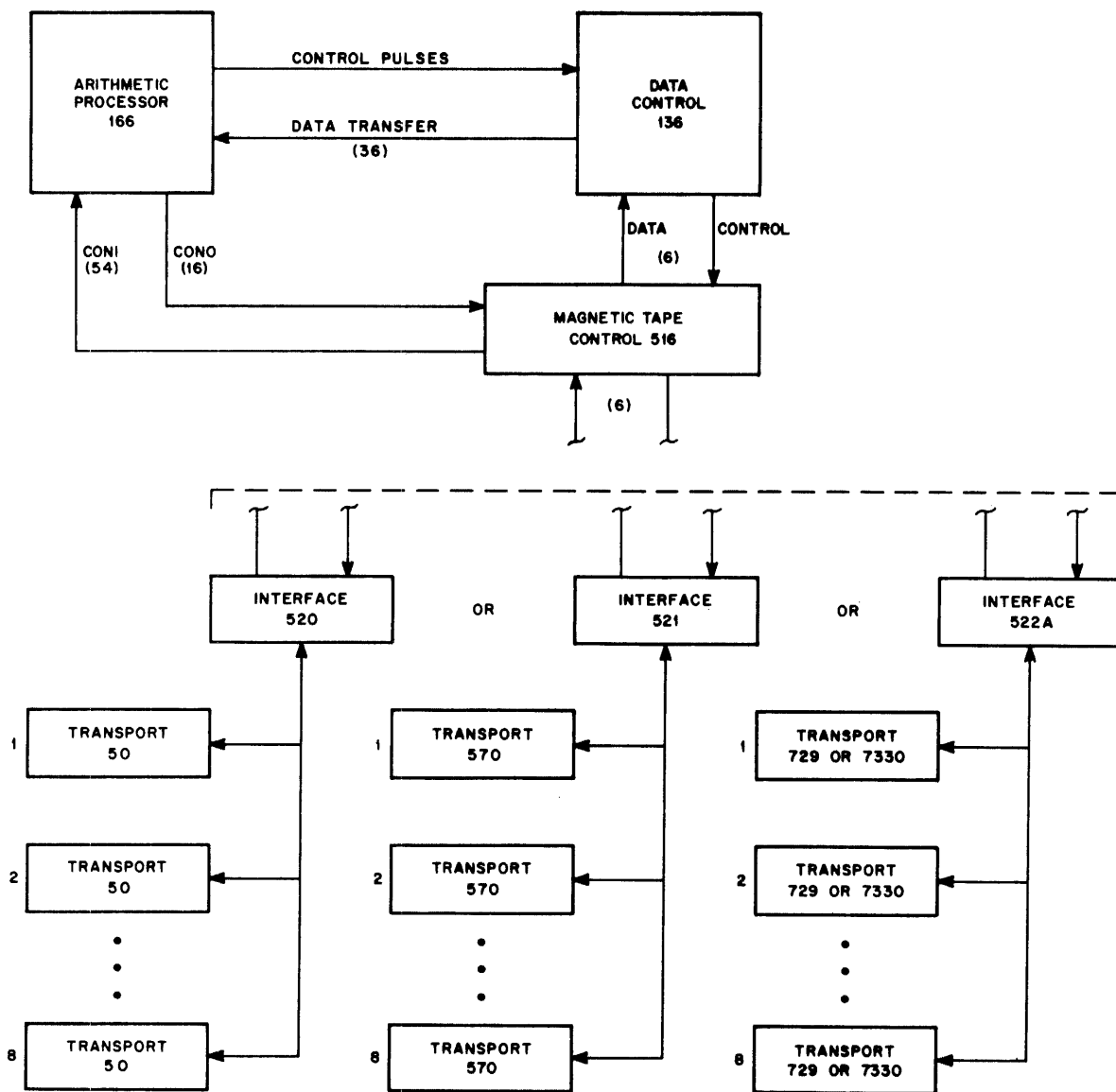


Figure 1-2   Tape Systems Configurations

For output, 36-bit computer words are transferred from the PDP-6 processor to the Data Control 136. The data control, through six sequential shifts out of the high-order end of its

1-4

accumulator, sends the six 6-bit characters (converted from each computer word) to the tape control to be written on tape. The tape control applies the output data characters to the write logic of the selected tape transport via the transport interface.

For input, the sequence is reversed. Data read from the tape in 6-bit characters is sent to the data control via the interface and the tape control. The data control shifts the data into its accumulator until six characters have been assembled into a 36-bit computer word (the end of the accumulator chosen and the direction of the shift depend upon the direction of tape motion, i.e., upon whether the command is read or backward read). The data control then transfers the full 36-bit word into the processor.

## PROGRAMMED OPERATIONS

Both CONI and CONO tape control instructions may be addressed to the Magnetic Tape Control 516.

## CONI Instruction

The processor samples 54 tape control status bits by means of CONI instructions. Three separate device selection addresses are provided; each samples 18 status bits. This permits tape control and transport status information to be sampled directly from the processor control console.

## CONO Instruction

The processor sends 16 bits of control information to the tape control at each CONO 220 tape control instruction. (The tape control also receives CONO 224 and CONO 230 instructions for more specialized functions described later in this chapter under Parity and Priority Interrupt.) The functions controlled by this information include:

1. the choice of the command to be executed (read, write, write file, etc.)

2. the selection of the tape transport that is to carry out the command

3. whether or not the selected transport is to be kept reserved after completing the command

4. the parity mode (binary or BCD)

5. the density at which data is to be written on tape (200, 556, or 800 bits per inch)

6. the slice level at which data is to be read from tape

7. whether or not end of record gaps are to be ignored

8. the priority interrupt channel to be assigned to the tape control.

The functions determined by the 12 more significant CONO 220 bits are listed in Table 3-1 (CB Register Bit Assignment). The remaining four CONO bits are never transferred into the CB register, but they make up two of the control fields listed above. Bit 32 is the maintenance bit; when programmed to be a 1, it causes the tape control to ignore the record gap and treat the entire tape as a single record. Bits 33-35 assign the tape control priority interrupt channel.

## Command Repertoire

By suitably coded CONO 220 instructions, the processor can cause the Magnetic Tape Control 516 to execute any of the following ten commands.

| | |
|---|---|
| Rewind | The selected transport rewinds the tape to load point and stops. |
| Rewind Unload | Rewinds the tape off the takeup reel of the selected transport. |
| Write | Writes N words of six characters each (from consecutive or nonconsecutive memory locations) into one tape record. A lateral parity bit (binary or BCD) is generated for each character written. All characters are read and checked for parity after writing. At the end of the record, an EOR gap is spaced out, and an EOR mark (longitudinal parity check character) is written. |

| Write End of File | Writes an end-of-file record consisting of an end-of-file character (17 octal, BCD) followed by an EOR mark. The tape control does this automatically without use of the Data Control 136. |
|---|---|
| Write Blank Tape | Writes about 3 inches of blank tape and stops. The Data Control 136 is not used. |
| Read Compare | Reads a full record from tape and compares it character by character with output data from the processor memory. Any discrepancy sets the RCE flag. (The EOR mark that follows the tape record is not compared.) |
| Read | Reads one complete record from tape. Each character is shifted into the low-order end of the data accumulator in the Data Control 136 for assembly into 36-bit computer words and transferred into the PDP-6 processor. Although the tape control always reads a full record, the processor can be programmed to read in any lesser amount of data. |
| Read Backward | Identical to read except for the direction of tape motion. Because data is shifted into the high-order end of the data control accumulator, the ordering of characters within each 6-character computer word is the same as for read. The word order is, of course, still inverted. |
| Space Forward | All spacing is done without the use of the Data Control 136. To space forward one record, the tape control reads the record, but does not apply the resulting data to the data control. If a 1 is programmed in bit 24, the space forward command is iterated until a file mark record is reached. |

| Space Backward | To space backward one record, the tape control executes a backward read but does not apply the resulting data to the data control. If a 1 is programmed in bit 24, the space backward command is iterated until a file mark record is reached. |
|---|---|

## Parity

Both lateral and longitudinal parity are checked during all commands except rewind and read compare. Separate error flags are provided for the two types of parity error. The PER flag indicates lateral parity errors, and the LPE flag indicates longitudinal parity errors. Longitudinal parity is always even; lateral parity can be programmed to be odd or even (binary or BCD).

## Priority Interrupt

Seven priority interrupt channels are available. See Chapter 2, Priority Interrupt, for a description of interrupt conditions.

## TAPE FORMAT

All transports driven by the Magnetic Tape Control 516 use 1/2-inch tape containing seven information channels. The tape format is shown in Figure 1-3. The left portion of the figure shows the tape in relation to the read and write heads. The tape moves by the heads vertically — forward direction being downward. The tape is composed of a mylar base coated on one side with an iron oxide composition. The oxide or dull side of the tape faces the heads, with the left edge toward the transport drive plate. The recording density may be either 200, 556, or 800 characters per inch. Tape speed varies depending upon the type of transport used.

The method of recording used is nonreturn-to-zero (NRZI). Although the tape has two basic states of remnant magnetization, the remaining magnetic state of the tape at a given bit position does not determine the value of that bit. A logical 1 is represented by a change from one state of magnetization to the other, in either direction. A logical 0 is represented by a constant state of magnetization. Therefore, to write a series of characters containing all 0s

THIS EDGE FACES
OPERATOR

END POINT
END-OF-TAPE
REFLECTIVE STRIP
ON NONOXIDE
(SHINY) SIDE
OF TAPE

$\frac{1}{2}$"

RECORD i+1

OXIDE (DULL) SIDE
OF TAPE FACES
HEADS

RECORD
GAP

W

LATERAL PARITY
BIT, ODD OR EVEN

RECORD GAP
$\frac{3}{4}$"

$\frac{3}{4}$"

0.30"

EOR MARK
(LONGITUDINAL PARITY
CHECK CHARACTER)

CHANNELS

C   B   A   8   4   2   1

R

END-OF-RECORD GAP

PARITY CHANNEL

EOR MARK

FORWARD

FOUR TO FIVE
CHARACTER SPACES

LOAD
POINT
GAP

RECORD i

6"

ONE
CHARACTER SPACE

LOAD POINT
BEGINNING-OF-TAPE
REFLECTIVE STRIP ON
NONOXIDE (SHINY) SIDE
OF TAPE

Figure 1-3   Tape Format

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is equivalent to writing a section of blank tape. Each time a character is transferred into the write buffer, the NRZI writers produce an equivalent character on the tape. However, because of NRZI method of recording, a transfer into the write buffer is not a normal 1 transfer. Instead, whenever a 1 bit is to be written in a given tape channel, the corresponding flip-flop of the write buffer is complemented, producing a change in tape magnetization. When a 0 is to be written, the corresponding bit of the write buffer remains in its initial state, and there is no change in tape magnetization.

The structure and relative spacing of the individual tape characters is shown in the right portion of Figure 1-3. Each 36-bit computer word is divided into six 6-bit characters. However, the write buffer contains seven flip-flops WB0-6 corresponding to the seven tape channels. The seventh channel (WB6) is the parity channel. A lateral parity bit is generated for each 6-bit data character and written into the parity channel. WB0 writes the most significant data bit; WB5, the least significant. The parity of the character may be either odd (binary) or even (BCD) as specified by the program. In reading the tape, only 1s are detected.

The smallest unit of information that can be written on the tape is a record. Since each computer word contains six 6-bit characters, a record normally contains 6N data characters, where N is the number of words that the processor BLKO (or DATAO) instructions transfer out to the Data Control 136. After the last data character of the record is written, the tape control writes slightly over four character spaces of blank tape (the EOR gap), and clears the write buffer to produce an end-of-record character, the EOR mark. The bit configuration of the EOR mark produced by the write buffer clear leaves an even number of 1 bits in each of the seven channels of the tape (all bits of the write buffer start in the 0 state, and to end in the 0 state they must undergo an even number of transitions). For this reason, the EOR mark is sometimes referred to as the longitudinal parity check character.

The smallest unit of information that can be read by the tape control is also an entire record. This does not mean, however, that the entire record must be deposited in computer memory. Although the tape control always reads the entire record and always sends every data character to the data control accumulator (unless the Data Control 136 is disconnected), the processor need not read in the full record. The processor accepts 6N data characters, where N is the number of words that the processor BLKI (or DATAI) instructions request from the Data Control 136.

After the processor has accepted the last word of input data from the data control data buffer, the data control advances one more word from the data accumulator to the data buffer. All additional characters are then shifted into the data accumulator. These characters, with the exception of the final six characters of the record, are shifted out the end of the accumulator and lost.

The distance that the EOR mark moves beyond the read head, before the tape is stopped, added to the acceleration distance which the tape moves before writing is allowed, produces a section of blank tape between records. This section of blank tape is called a record gap; it is approximately 3/4 inch long. The EOR character always moves slightly further beyond the heads in writing than in reading. This is an added precaution to prevent the generation of inter-record "gap-trash" which might otherwise be produced by failing to erase the entire record gap when writing on previously recorded tape. As long as the erase heads are functioning properly, the precaution is unnecessary. (Since the direction of tape magnetization changes only when 1s are written on tape, the absence of write output data during a write command erases the tape, that is, writes blank tape with a uniform state of magnetization.)

Besides detecting changes in magnetization through the read heads, the tape transports also include a photoelectric system for sensing the beginning and end of the tape (TLP — tape load point, and TEP — tape end point).

The load point and end point of the tape are marked by reflective strips mounted on the side of the tape away from the heads. These strips are detected by photodiodes which sense light reflected from them. In writing on a newly mounted or rewound tape, a gap of about 6 inches is left from the load point before writing can begin.

## TAPE WRITE AND READ SIGNAL FLOW

Figure 1-4 is a simplified block diagram of the tape system write and read paths for a single channel. The actual circuit modules used, and the distribution of these modules between the tape transport and the transport interface, varies depending on the choice of interface and transport. (Refer to the appropriate interface chapter for a description of the specific circuits used with a given transport-interface combination.)
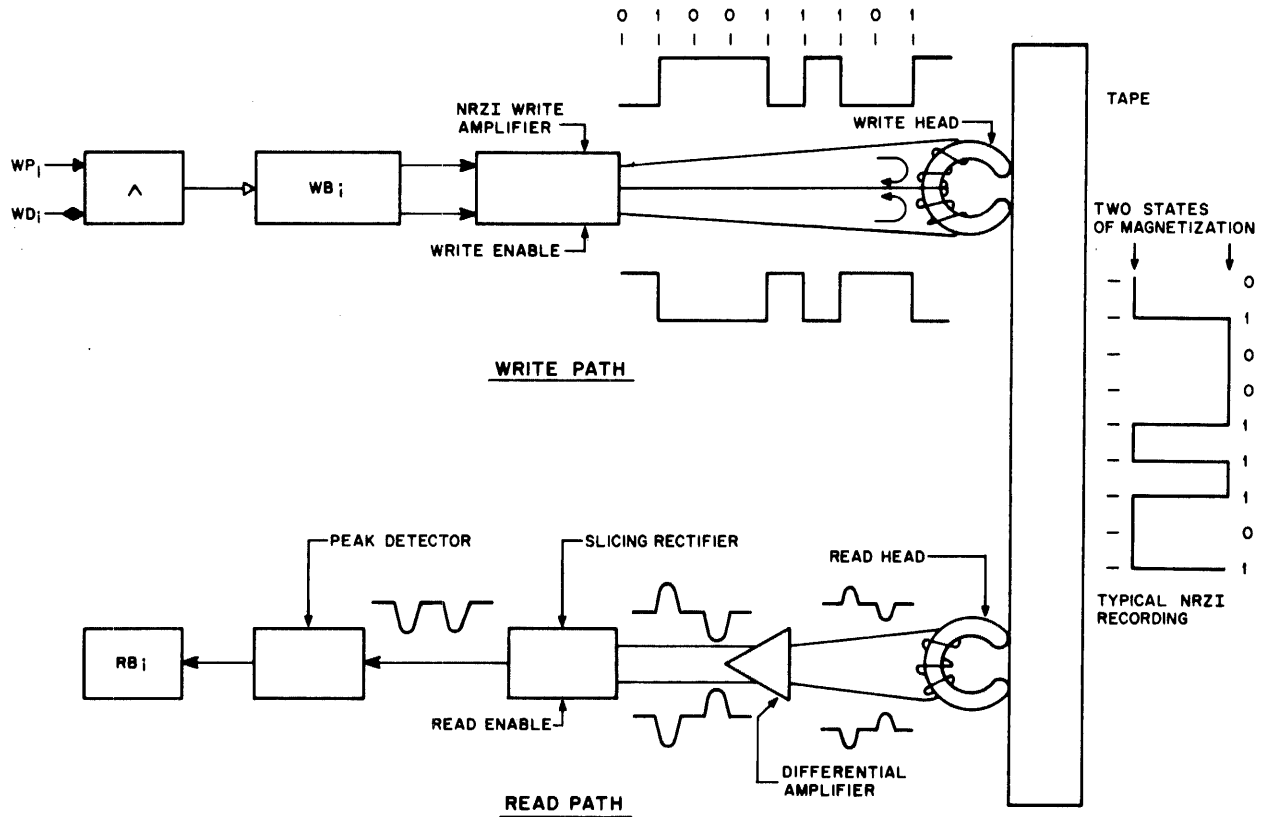
Figure 1-4   Tape Write and Read Signal Flow

## Write Path

The write path is shown at the top of the figure. The $WB_i$ flip-flop is complemented at each WP pulse that occurs while the $WD_i^1$ level is asserted. Both outputs of the $WB_i$ flip-flop are connected (through various drivers not shown in the figure) to an NRZI write amplifier. When gated by a write enable signal, this write amplifier drives one of two oppositely wound coils at the write head. The choice depends on the state of the $WB_i$ flip-flop. If the write enable level is not present, no current flows through either coil.

Whenever a 1 is to be written on tape, $WD_i^1$ causes the $WB_i$ flip-flop to be complemented at the WP pulse. The transition of $WB_i$ terminates the current through one coil and starts it in the other, changing the direction of tape magnetization and writing a 1 on the tape. As long as $WB_i$ remains in the same state, current continues to flow through one side of the coil, and 0s are written on the tape. (The tape is then magnetized in the same direction over a series of character spaces.)

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## Read Path

The read path is shown at the bottom of Figure 1-4. The tape reaches the read head shortly after traversing the write head. As long as the direction of tape magnetization remains constant, no current flows through the read head coil. Each change in the direction of tape magnetization induces a current in the read head. The read current produced by two consecutive tape 1s is shown in the waveforms near the read head.

These signals are applied to a differential read amplifier that provides considerable amplification for difference signals but only fractional amplification for common mode signals. The output of the read amplifier is then sent through a slicing rectifier. This circuit can produce an output only when the read enable level is present. This prevents read signals from being sent to the tape control when tape is in motion but not being read; for example, during the rewind operation. The rectifier produces an output pulse (of one polarity) for every input pulse of either polarity from the read amplifier. However, the rectifier input circuit, to prevent a low-level noise input from generating an unwarranted output pulse, requires a minimum threshold level.

The slicing rectifier output is applied to a peak detector. The peak detector produces a logic pulse output at the peak of the input pulse which, therefore, sets the read buffer flip-flop whenever a 1 is read from the tape.

## SYSTEM DATA

System specifications and physical characteristics are listed in Tables 1-1 and 1-2, respectively.

### TABLE 1-1   SYSTEM OPERATING SPECIFICATIONS

| System Parameters | |
|---|---|
| Number of transports per tape control | 1-8 |
| Recording method | NRZI |
| Characters | 7 bits:  6 data, 1 parity |
| Parity | |
| Lateral | Odd or even |
| Longitudinal | Even (data channels only) |
| Density | 200, 556, or 800 characters/inch |

TABLE 1-1   SYSTEM OPERATING SPECIFICATIONS (continued)

| | 200 | 556 | 800 |
|---|---|---|---|
| Maximum transfer rate (in characters/second) | | | |
| Interface 520, Transport | 15 kc | 41.6 kc | ---- |
| Interface 521, Transport 570 or Interface 522A, Transport 729 | | | |
| (at 112.5 ips) | 22.5 kc | 62.5 kc | 90 kc |
| (at 75 ips) | 15 kc | 41.6 kc | 60 kc |
| Interface 522A, Transport 7330 | 7.2 kc | 20 kc | ---- |

| | |
|---|---|
| Load point gap | 6 inches |
| Inter-record gap | 3/4 inch |
| EOR gap (longitudinal parity character spacing) | 4-5 character spaces |

| Error flags | Function |
|---|---|
| PER | lateral parity error |
| LPE | longitudinal parity error |
| RCE | read comparison error |
| ILC | illegal command |
| Priority interrupt; 7 channels available | Interrupt occurs at end of each record and at illegal commands |
| Status bits | 54 status bits available for sampling at PDP-6 console |

Transport Parameters

| | |
|---|---|
| Read-write heads | 7 channel |
| Tape | |
| Material | 1.5 mil polyester |
| Width | 1/2 inch |
| Length | 2400 feet |
| Reel diameter | 10-1/2 inches |
| Data protection | Write enable lockout ring |

TABLE 1-1   SYSTEM OPERATING SPECIFICATIONS (continued)

Tape Position Indications

| | |
|---|---|
| Load point and end point detection | Photoelectric |
| Full reel and low reel | Mechanical (Used only for Transport Type 50.) |

Meaning of Position Indications

| | |
|---|---|
| Load point | 10 feet from physical beginning of tape |
| End point | 14 feet from physical end of tape |
| Full reel | Less than 100 feet on takeup reel |
| Low reel | Less than 100 feet on supply reel |

| Transport Type | 50 | 570 | 729 | 7330 |
|---|---|---|---|---|
| Multicontrol operation | no | yes | no | no |
| Slice levels available | 1 | 2 | 2 | 2 |
| Tape speed (inches/second) | 75 | 75+ 112.5 | 75+ 112.5 | 36 |
| Maximum rewind speed (inches/second) | 225 | 450 | 550 | 220 |
| Rewind time full reel (seconds) | 400 | <90 | <90 | 1330 |

TABLE 1-2   PHYSICAL CHARACTERISTICS

## Construction

One standard, all-steel construction DEC cabinet.

## Logic Racks

| | |
|---|---|
| Magnetic Tape Control 516 | Four racks |
| Interface 520 | One rack |
| Interface 521 | One rack |
| Interface 522A | Two racks |

## Modules

Standard DEC system plug-in units, series 100 and 4000.

## TABLE 1-2  PHYSICAL CHARACTERISTICS (continued)

### Power Equipment

| For | Use |
|-----|-----|
| Mangetic Tape Control 516, and any interface | Power Control Type 834-836 and two 728 Power Supplies |
| Magnetic Tape Control 516, Data Control 136, and Interface 520 or 521 | Power Control Type 834-836 and two 728 Power Supplies |
| Magnetic Tape Control 516, Data Control 136, and Interface 522A | Power Control Type 834-836 and two 728 Power Supplies |

### Logic

Solid state.  Transistors and crystal diodes utilizing static logic levels (0 vdc and −3 vdc).

### Dimensions

| | |
|---|---|
| Height | 69-1/2 inches |
| Width | 22-1/4 inches |
| Depth | 27-1/8 inches |
| Clearance, front doors | 8-3/4 inches |
| Clearance, rear doors | 14-7/8 inches |

### Weight (lbs)

| | |
|---|---|
| Magnetic Tape Control 516 | 120 |
| Interface 520 or 521 | 20 |
| Interface 522A | 40 |
| Cabinet | 160 |

## TABLE 1-3  POWER REQUIREMENTS

### Line Voltage Input

105 to 125 volts, 60 cycle, single phase

Power plug − Hubble Twist-Loc 3-prong, 30 ampere, 250 volt

## TABLE 1-3  POWER REQUIREMENTS (continued)

### Current Consumption

|  | Surge Amperes | Normal Amperes |
|---|---|---|
| Magnetic Tape Control 516 | 6 | 4 |
| Interface 520 or 521 | 1.5 | 1 |
| Interface 522A | 3 | 2 |

### Power Consumption

|  | Watts |
|---|---|
| Magnetic Tape Control 516 | 460 |
| Interface 520 or 521 | 115 |
| Interface 522A | 230 |

### Heat Dissipation

|  | Btu/Hour |
|---|---|
| Magnetic Tape Control 516 | 1560 |
| Interface 520 or 521 | 392 |
| Interface 522A | 785 |

## REFERENCE CONVENTIONS

The Digital Equipment Corporation engineering drawing conventions and instruction manual referencing should be understood at this point. A study of the material contained in Chapter 13 and the following paragraphs before proceeding with detailed descriptions will save considerable reference time and preserve thought continuity when reading the text that follows.

Any reference to an illustration by a chapter-oriented figure number indicates that the figure is to be found in text following the reference. Any reference to an engineering drawing number indicates that the drawing is to be found in a special drawing section or chapter. All engineering drawings are referenced first by the full drawing number.

Example:  BS-D-516-0-CM

To locate a specific signal or function on a drawing, a system of coordinates is used. As shown on the drawings of Chapter 13, coordinates are designated by a number and letter. Thus, in any drawing reference, coordinate location appears immediately after the number separated by a colon.

Example: BS-D-516-0-CM:D1

To avoid needless repetition of the full drawing number, in-text references can use a short designation form that includes only the difference modifier(s) of the drawing designation plus the coordinates.

Example: -CM:D1

One last text reference convention must be noted. Occasionally it is desirable to indicate the condition of a circuit within a logic description. As shown on the drawings of Chapter 13, circuit locations are identified. For reference in text, this designation is noted; for example, CB24. If the condition of the circuit is to be stated the reference becomes either CB24(1) or CB24(0).

The signal glossaries of Chapter 12 also are an important adjunct to both the text and drawings. These glossaries can be used in a cross indexing manner so that any signal and the conditions that generate it can be easily and completely referenced.

<u>REFERENCE DOCUMENTS</u>

Systems Modules Catalog, C-100          by Digital Equipment Corp.

FLIP CHIP Modules Catalog, C-105        by Digital Equipment Corp.

# CHAPTER 2

# TAPE CONTROL INPUTS AND OUTPUTS

## PROCESSOR

Signals between the processor and the Magnetic Tape Control 516 fall into four major categories: clear signals; signals required for the CONO command; signals required for the CONI command; and priority interrupt request signals.

## Clear Signals

The IOB RESET pulse (see BS-D-516-0-CM:D1) is an ungated clear pulse which is applied to all I/O devices and control units when computer power goes on, or when the operator presses the I/O reset key on the computer console. The program may also generate this reset. The IOB RESET is amplified and sent on to the transport interfaces as POWER CLEAR.

Within the tape control, the IOB RESET clears the command hold buffer, and resets the command sync quad-flop and the tape status quint-flop. It also generates two additional clear pulses MCL and CCB which complete the tape control clear operation. These two clear pulses are also applied to the transport interface (with the new designations STATUS CLEAR and $0 \longrightarrow$ CM). The tape control engineering drawings show one additional clear signal called INT CLR. This pulse is not used at present.

## CONO Signals

The processor CONO (conditions-out) instruction produces an IOB CONO CLR pulse followed 1 μsec later by an IOB CONO SET pulse (BS-D-516-0-CM:A1). These two command pulses are effective only at the I/O device or control unit specified by the CONO instruction device selection code. Although the tape control may occasionally receive CONO 224 and CONO 230 instructions for certain specialized functions (described in Chapter 10), these instructions are exceptions; nearly all tape control CONO instructions use device selection code 220.

When gated by the SEL (Select Tape Control 516) level, which is only asserted when IOS3-9 represent 220 octal (BS-D-516-0-CM:C1), the IOB CONO CLR pulse generates a CLR pulse which clears the command hold buffer CHB20-35. The IOB CONO SET pulse, when gated by the SEL level, transfers the CONO control information into the command hold buffer CHB20-35.

## CONI Signals

The processor CONI (conditions-in) instruction produces an IOB STATUS level. This level is effective only at the I/O device or control unit specified by the CONI instruction device selection code. The IOB STATUS level places status information from the selected device or control unit on the I/O bus for 2.5 μsec. The processor reads the information from the bus into its arithmetic register at the 2-μsec point.

Each of the three device addresses assigned to the tape control, SEL (220 octal), SLT (224 octal), and SCS (230 octal) gates 18 status bits onto the bus (see BS-D-516-0-ST for the specific gating control of the 54 status bits). For maintenance purposes, the most relevant tape control and tape transport status information can be monitored directly at the processor console.

## Priority Interrupt

The processor can assign a priority-interrupt request channel to the tape control by means of a CONO instruction which sets CHB33-35 to some octal number from 1 to 7. If all three bits are 0, no priority interrupt channel is assigned. By asserting the PIE level (BS-D-516-0-CM:A8), the tape control can request a priority interrupt break on the assigned channel. The PI request is sent to the processor by grounding the appropriate PIR (priority interrupt request) line. The lower the channel number, the higher the priority. Breaks on channel 1 take precedence over all other breaks. Breaks on channel 2 take precedence over all breaks except those on channel 1, etc.

The conditions under which the PIE level is asserted are themselves subject to program control. There are four flip-flop switches which determine which of four possible priority interrupt conditions is to be allowed to assert the PIE level (see BS-D-516-0-MD:C6-7). Every CONO 224 instruction sets the four priority interrupt enable switches EFE, LIE, ICE and XNE to the states determined by bits 33, 20, 35, and 21, respectively, of the CONO 224 instruction.

When a given switch flip-flop is set to 1, the corresponding interrupt condition is gated through to assert PIE; when the switch is left in the 0 state, the input condition is not allowed to produce a PIE.

The four priority interrupt conditions that can be enabled to generate PIE are ERF(1), LIF(1), ICR, and XNC. The ERF(1) condition is asserted when the end of record flag is set; this is perhaps the most frequently used interrupt condition. The LIF(1) condition is asserted when the load point interrupt flag is set; this interrupt condition is used primarily during rewind commands. The ICR condition indicates that the interface and control are ready. The XNC condition represents the transfer new command state of the command sync quad-flop (see Chapter 3, Command Sync Quad-Flop). This condition indicates that the tape control is free to accept another CONO 220 command. The XNC interrupt condition is particularly useful during space-to-end-of-file commands when use of the ERE interrupt would be inconvenient. The four interrupt conditions that produce the PIE level are summarized in Table 2-1.

TABLE 2-1   PRIORITY INTERRUPT CONDITIONS

| CONO 224 Bit No. | Sets Switch | Permitting Interrupt Condition to Assert PIE |
|---|---|---|
| 33 | EFE | End of Record Interrupt ERF(1) |
| 20 | LIE | Load Point Interrupt LIF(1) |
| 35 | ICE | Interface and Control Ready ICR |
| 21 | XNE | Transfer New Command Interrupt XNC |

DATA CONTROL 136

The signals between the Data Control 136 and the Mangetic Tape Control 516 pertain to either output (write) operations, or input (read) operations. For any operation in which the data control selects the tape control, the SEL 3 level causes the DCS flip-flop (BS-D-516-0-MD:B7) to be set at BRP.

## Output Signals

During RDC (read compare) and WRT (write) commands, the data control applies the contents of its six high-order accumulator bits DA0-5 to the tape control via the output levels DA0(1)–DA5(1). Negative levels represent 1s in the corresponding accumulator bit positions. Although contents of the six high-order accumulator bits are always present at the tape control input terminals (BS-D-516-0-RD:C1-4), the tape control only samples these outputs during the WRT and RDC commands.

The tape control sends TK/GV LT (take or give character shift left) command pulses to the Data Control 136 during RDC and WRT commands (and also during the input command RED). These command pulses synchronize data control operations to the timing requirements of the tape control and the transports. At the receipt of each TK/GV LT pulse, the data control shifts the contents of its accumulator six bit positions left. This shift advances the next 6-bit output character into position to be sampled by the tape control.

Each character requires a single TK/GV LT pulse; no pulses are required for EOR marks. For all three commands during which the tape control sends TK/GV LT command pulses to the data control, the pulse produces certain common effects in the data control logic. At the arrival of the TK/GV LT, the data accumulator is shifted left by six bit positions, and the data control character counter is incremented by 1.

## Input Signals

During RED, SPF, BER, SPB, and RDC commands (see signal glossary), the transport interface applies the contents of its read buffer register RB to the tape control via the input data levels RBB0(1)–RBB5(1) (BS-D-516-0-RD:B2-5). Negative levels represent 1s in the corresponding read buffer bit positions. The RBB input data is read into the Data Control 136 only during the two commands RED (read) and BER (backward read). If the RED or BER command is in BCD (even) parity mode, the Hollerith code 0 character (12 octal) is converted to 00 octal before being applied to the data control (BS-D-516-0-RD:C1-3).

For the RED command only, the tape control strobes each input data character into the six low-order bits of the data control accumulator with a TK/GV LT pulse. On receiving each TK/GV LT,

the data control shifts its accumulator left six bits to make room for the input character and simultaneously strobes the character into the six low-order accumulator bits DA30-35. As in the case of the RDC and WRT output commands, the data control increments its character counter at each TK/GV LT.

For the BER command only, the tape control strobes each input character into the six high-order bits of the data control accumulator with a TK/GV RT pulse. On receiving each TK/GV RT, the data control shifts its previous accumulator contents right six bits to make room for the input character and simultaneously strobes the character into the six high-order accumulator bits DA0-5. The data control also increments its character counter at each TK/GV RT.

The BER command involves one complication not present with the RED command. When executing a RED command, the EOR gap provides a convenient means of sensing the end of the data record, and the EOR mark is not read as data. However, for the BER command, the EOR mark is read first, then the EOR gap, and finally the data record. Therefore, the EOR mark initially looks like data and it is strobed into the data control by the associated TK/GV RT pulse. The tape control must prevent the data control from treating the EOR mark as a valid data character. It does this by following the EOR mark TK/GV RT with a $0 \longrightarrow$ CCT pulse. This pulse clears the data control character counter and causes the EOR mark to be shifted out and eliminated.

### TRANSPORT INTERFACE

For ready reference, signals from the transport interface are listed in Table 2-2, and signals to the transport interface are listed in Table 2-3. The signals between the tape control and transport interface can be better understood if learned in context as encountered in the subsequent chapters of the manual.

## TABLE 2-2   SIGNALS FROM TRANSPORT INTERFACE

| Signal Name | Function |
|---|---|
| START 2 | Steps 5-flop from TCR to UPS or MOS. (Called STM within the tape control.) |
| BCT | Selected transport reserved by other tape control. (Interface 521 only.) |
| RDY | Transport ready to receive new command. |
| TEP | Tape at end point. |
| TLP | Tape at load point. |
| TWL | Tape write enable lockout ring out. A data-protection condition that disables write circuits. |
| RBCP | Read buffer character present (RB0-5 $\neq$ 0). |
| RBEF | Read buffer end of file. Senses end-of-file character (RB0-5 = 17 octal). |
| TRPE | Tape read parity error. Lateral parity error detected for character just read. |

## TABLE 2-3   SIGNALS TO TRANSPORT INTERFACE

| Output Signal Name | Signal Name Inside Tape Control 516 | Function |
|---|---|---|
| | Clear Pulses | |
| POWER CLEAR | IOB RESET | I/O bus reset (initial ungated clear pulse). |
| STATUS CLEAR | MCL | Motion clear; occurs at beginning of each command. |
| 0 $\longrightarrow$ CM | CCB | Command buffer clear; occurs at termination of command levels. |

TABLE 2-3   SIGNALS TO TRANSPORT INTERFACE (continued)

| Output Signal Name | Signal Name Inside Tape Control 516 | Function |
|---|---|---|
| | Command Levels | |
| WRITE | WWE | Enables write circuits. |
| FOW | - | Forward command. |
| BAC | - | Backward command. |
| REW | - | Rewind command. |
| WEF | - | WRF or WBT command. |
| NOP | - | No operation. |
| | Control Pulses | |
| IOT 7104 | CTT | Start pulse. |
| AC1 ⟶ UN | JNU | Unit selected. |
| MP | MDF | Motion pulse. |
| WP | WCP | Write pulse. |
| START 1 | EOR 2 | Write EOR mark. |
| 0 ⟶ RB | - | Clear read buffer. |
| 1 ⟶ EFF | - | Set end of file flag. |
| 0 ⟶ EFF | - | Reset end of file flag. |

# CHAPTER 3

# COMMAND LOGIC

The command logic accepts control information from the PDP-6 processor, decodes the information, and applies the resulting command signals to the transport interface. The command logic is composed of two buffer registers, a 4-state control device (the command sync quad-flop), and a set of decoding networks which process the control information in the buffer register and generate appropriate command levels for transmission to the selected tape transport.

During the CONO tape control instruction, the 16 low-order bits of the CONO effective address are transferred out from the processor to the command hold buffer CHB (BS-D-516-0-CM). Four of these control bits remain in CHB. The remaining twelve control bits are not decoded in CHB; before being decoded these bits are advanced into the command buffer CB. The advance of these twelve bits from CHB into CB takes place in two successive stages. First four selection bits are transferred to CB to select (and, if necessary, reserve) a transport; second, when the selected transport indicates that it is ready for the command, the other eight control bits are also transferred into CB. From CB, the control bits are applied to the decoding networks. The command decoding networks convert the processor control fields into the command levels required at the transport interface.

The primary function of the command sync quad-flop is to control the timing of these control information transfers, and at their completion, to start the selected tape transport.

## COMMAND SYNC QUAD-FLOP

The command sync quad-flop (BS-D-516-0-CS:C6-8) controls the advance of information from CHB to CB by initiating the JNU pulse and the JNC pulse. The JNU pulse causes the selection of a single transport; JNC applies the command levels of the current instruction to that transport via the transport interface. After the command levels have been applied to the transport, the quad-flop causes the generation of a CTT pulse (−CS:B5) and the selected transport to begin the command.

## Quad-Flop Structure

The command sync quad-flop is composed of four 3-input negative diode NOR gates (3E19, 20, 25). The inputs to each of these four gates are taken from the outputs of the remaining three gates. The result of this arrangement is that the quad-flop functions as a 4-state flip-flop. It remains stable in any one of its four states; the active output is at ground, and the three quiescent outputs are negative logic levels.

## Basic Quad-Flop Cycle

The basic cycle of the command sync quad-flop is shown in Figure 3-1. The basic cycle operations are also shown in steps 1 through 6 of the more detailed command and status logic flow diagram, Figure 3-2. Steps 11 through 13 of the figure show variations from the basic quad-flop cycle which arise during the execution of successive commands in continue mode (CON = 1). These variations are described under Quad-Flop Continue Cycle later in this chapter.
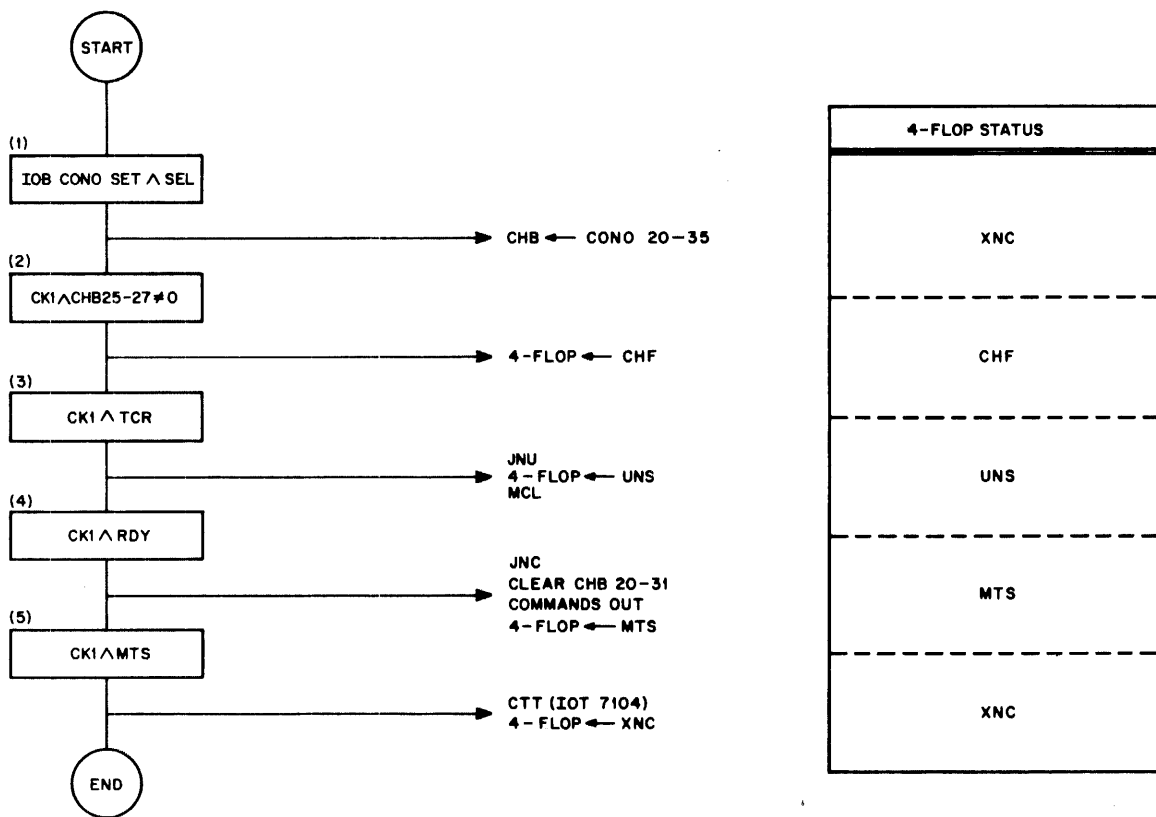


Figure 3-1   Command Sync Quad-Flop Basic Cycle

**Figure 3-2    Command and Status Logic Flow Diagram**

**3-3**

START

(1) IOB CONO CLR∧SEL
→ CLEAR CHB  4-FLOP ← XNC

(2) IOB CONO SET∧SEL
→ CHB ← CONO 20-35

(3) CK1∧CHB25-27≠0
→ 4-FLOP ← CHF

(4) CK1 ∧ TCR → (A)
→ JNU  4-FLOP ← UNS  MCL

(5) CK1 ∧ RDY
→ JNC  CLEAR CHB 20-31  COMMANDS OUT  4-FLOP ← MTS

(6) CK1 ∧ MTS
→ CTT (IOT 7104)  4-FLOP ← XNC

(7) STM

REW  YES / NO
→ 5-FLOP ← MOS

(8) MDF ∧ MOS
→ CCB (0 → CM)  END REW COMMAND  5-FLOP ← TCR

(9) TLP ∧ RWD
→ 5-FLOP ← MOS

(10) MDF ∧ MOS
→ 5-FLOP ← TCR  LIF ← 1

END

(B)

5-FLOP ← UPS

(C)

(8) MDF ∧ UPS
→ 5-FLOP ← RIP

XNC  NO / YES

(9) IOB CONO CLR ∧ SEL
→ CLEAR CHB

(10) IOB CONO SET ∧ SEL
→ CHB ← CONO 20-35

(11) CK1∧CHB25-27≠0
→ 4-FLOP ← CHF

(12) EOR1 ∧ RIP
→ 5-FLOP ← ERM

(13) MDF ∧ ERM

(D)

COMMAND FLOW DIAGRAMS SHOW DETAILED LOGICAL OPERATIONS THAT OCCUR IN THIS INTERVAL

CON(0)  YES / NO
→ CCB (0 → CM)  5-FLOP ← MOS
→ 5-FLOP ← UPS  MCL

(14) MDF ∧ MOS
→ 5-FLOP ← TCR

GO TO A

SEF  YES / NO
→ SAME COMMANDS OUT
→ JNC  4-FLOP ← XNC  NEW COMMANDS OUT

GO TO B

| FIRST COMMAND | | | |
|---|---|---|---|
| STEP NO. | 4-FLOP STATE | 5-FLOP STATE | |
| 1 | XNC | TCR | |
| 2 | XNC | TCR | |
| 3 | CHF | TCR | |
| 4 | UNS | TCR | |
| 5 | MTS | TCR | |
| 6 | XNC | TCR | |
| 7 | XNC | UPS | ~ REW |
| 8 | XNC | RIP | |
| 7 | XNC | MOS | |
| 8 | XNC | TCR | REW |
| 9 | XNC | MOS | |
| 10 | XNC | TCR | |

| SECOND COMMAND | | | |
|---|---|---|---|
| STEP NO. | 4-FLOP STATE | 5-FLOP STATE | |
| 9 | XNC | RIP | |
| 10 | XNC | RIP | ~ REW |
| 11 | CHF | RIP | |
| 12 | CHF | ERM | |
| 13 | CHF | MOS | CON(0) |
| 14 | CHF | TCR | |
| 13 | XNC | UPS | CON(1) ∧ ~ SEF |
| 13 | CHF | UPS | CON(1) ∧ SEF |

## XNC State

Because the quad-flop is reset to XNC state (Transfer New Command) by IOB RESET and IOB CONO CLR, the quad-flop begins each command in XNC. The quad-flop must be in XNC to advance to its second state CHF (Command Hold Full).

## CHF State

The IOB CONO SET pulse (Figure 3-1, step 1) loads the effective address of the current CONO instruction into the command hold buffer. Every tape command code has a 1 in at least one of the three bits 25-27, so CHB25-27 $\neq$ 0 after the IOB CONO SET. Therefore, the first CK1 to occur after IOB CONO SET steps the quad-flop to the CHF state (Figure 3-1, step 2). The CHF state indicates that the command hold buffer is loaded with control information. The quad-flop must be in CHF to advance to its third state UNS (Unit Selected).

## UNS State

As soon as the tape control is ready to initiate a command (indicated by the TCR — Tape Control Ready — state of the tape status quint-flop and CNR(0); refer to Chapter 4, Tape Status Quint-Flop), the next CK1 pulse generates a JNU pulse, and steps the quad-flop from CHF to UNS (Figure 3-1, step 3). The quad-flop must be in UNS state to advance to its fourth state MTS (Magnetic Tape Start). The JNU pulse produces an MCL pulse which clears most of the tape control flip-flops. The JNU pulse also advances the device selection information as stated earlier from CHB28-31 to CB28-31. The contents of CB29-31 specify which of the available transports is to receive the current command. The CB28 bit determines whether that transport is to be kept in a reserved status after the completion of the command or is to be returned to the pool. The JNU pulse is sent to the 521 Interface units as AC1 $\longrightarrow$ UN.

## MTS State

When the selected transport is ready to execute the current command, it sends an RDY level to the tape control. This level enables the next CK1 pulse to generate a JNC pulse (Figure 3-1, step 4). The JNC pulse advances the contents of CHB20-27 into CB20-27. These eight control bits are decoded, and the resulting command levels are applied to the selected transport.

The JNC pulse clears CHB20-31 (once the control information is advanced to CB, it is no longer needed in CHB). The JNC pulse also steps the command sync quad-flop to its fourth and final state MTS.

## Reset to XNC

The CK1 pulse immediately following the CK1 that produced JNC (and applied the command levels to the selected transport) generates the CTT pulse (BS-D-516-0-CS:B8). This pulse resets the command sync quad-flop from MTS to XNC. The same pulse is sent to the transport interface as IOT 7104 and returns from the interface (sometimes delayed, depending on the type of interface used) as START 2. After it reenters the Magnetic Tape Control 516, it is called STM (BS-D-516-0-CS:B3).

The IOT 7104 pulse causes the transport to start tape motion. The STM pulse sets the tape status quint-flop to the UPS acceleration state (see Chapter 4, Tape Status Quint-Flop).

## Quad-Flop Continue Cycle

At any time after the command sync quad-flop is reset to XNC and the tape-status quint-flop has been stepped to UPS, a second CONO instruction can be sent to the tape control. This second instruction transfers new control information into CHB (which has been empty since the JNC pulse of the first instruction cycle). The next CK1 pulse can then advance the quad-flop to the CHF state (see Figure 3-2, step 11).

The first command continues to completion while the second command remains stored in CHB. The MDF pulse at the end of the ERM state of the first command (Figure 3-2, step 13) represents a branch point in the tape control cycle. At that MDF pulse, the tape control enters the continue mode if the CON flip-flop is in the 1 state. (Refer to Continue Logic, later in this chapter, for a more detailed description of the significance of the state of CON.)

If CON = 0, the second instruction does not call for continue mode, and the command sync quad-flop follows the same basic cycle as the first instruction. From CHF, it proceeds to UNS, MTS, and is reset to XNC. This sequence is represented by the left branch of the Figure 3-2 flow diagram (including the jump from step 14 to point A).

However, if CON = 1, indicating that the second instruction does call for continuous mode operation, the quad-flop cycle never advances to UNS or MTS. Instead, the quad-flop is reset directly from CHF to XNC (by the JNC pulse). This continue mode operating sequence is represented by the extreme right branch of the Figure 3-2 flow diagram. The basic quad-flop cycle is cut short during continue mode operations because: 1) no JNU pulse is required during continue mode — the second instruction always selects the same transport interface as the first instruction; and 2) no IOT 7104 pulse is sent to the selected transport — the transport is already moving in the required direction. Therefore, since both the JNU and IOT 7104 pulses are omitted during continue mode instructions, there is no need for the quad-flop to step through the UNS and MTS states; instead it can be reset directly from CHF to XNC (Figure 3-2, step 13, right branch). In continue mode, the MDF pulse that ends the tape-status quint-flop ERM state (Figure 3-2, step 13) also produces a JNC pulse. This JNC pulse resets the quad-flop from CHF to XNC state, clears CHB, and advances the new control information in CHB20-27 into CB20-27, thereby applying the new command levels to the transport interface.

Because certain transitions of the command sync quad-flop are conditioned upon the state of the tape-status quint-flop (the quint-flop TCR state is one of the input conditions governing the generation of JNU and JNC, see BS-D-516-0-CS:A3 and A6) the quad-flop cycle should not be considered in isolation; rather the quad-flop and the quint-flop are to be regarded as two interdependent elements of a single control system. The operation of the complete system is shown in Figure 3-2, and described in Chapter 4, Tape Status Quint-Flop.

## COMMAND HOLD BUFFER

The CHB (BS-D-516-0-CM) is a 16-bit buffer register which receives CONO control information from the I/O bus. During the CONO tape control instruction, the 16 low-order bits of the CONO effective address are loaded into CHB20-35. (Physically, the transfer occurs over conductors IOB2-17. This wiring method is chosen to equalize the loading on the two I/O bus cables. The control information entering CHB20-35 is taken from bits 20-35 of the CONO address; so the use of IOB2-17 instead of IOB20-35 has no logical significance.)

The entire CHB is cleared by the CLR pulse which occurs at IOB RESET, INT CLR, and IOB CONO CLR ∧ SEL. The JNC pulse clears CHB20-21; i.e., all of the twelve CHB bits that

JNC advances into CB. The remaining four CHB bits CHB32-35 are not cleared by JNC, but only by CLR. Since IOB CONO CLR precedes IOB CONO SET by 1 μsec, the CHB is always ready for new control information at the arrival of the IOB CONO SET. That pulse loads the effective address of the current CONO instruction into CHB by means of a 1 transfer. The IOB CONO SET is gated through to the CHB capacitor-diode inputs only when the device selection code of the current CONO instruction specifies the tape control (220 octal). Decoder 3E3 (BS-D-516-0-CM:C1) then produces a SEL level. The IOB CONO CLR pulse is also gated by the SEL level.

The JNU pulse advances the contents of CHB28-31 into CB28-31. These four bits specify which of the available transports is to receive the current command and whether the selected transport is to be kept in a reserved status after the completion of the instruction or is to be returned to pool.

When the selected transport is ready to execute the current instruction, a JNC pulse is generated. This pulse advances the eight high-order CHB bits from CHB20-27 to CB20-27. Once in CB, these eight bits are decoded to produce the command levels required by the current instruction. The JNC pulse also clears CHB20-31.

The four low-order bits CHB32-35 are never advanced into CB. These four bits are used while they are in CHB. Bit CHB32 is the disable EOR 1 maintenance bit. Setting this bit to a 1 with a CONO instruction inhibits the ERE level and prevents the generation of EOR 1 pulses. When the EOR 1 pulses are disabled, the tape control treats the tape essentially as a single record. This permits the entire tape to be traversed with a single command. Bits CHB33-35 assign a priority interrupt channel to the tape control; for a description of the priority interrupt logic refer to Chapter 2, Priority Interrupt. Device address 220 samples CHB20-35 on IOB20-35.

## COMMAND BUFFER

The CB (BS-D-516-0-CM) is a 12-bit buffer register which receives CONO control information from the CHB at the JNU and JNC pulses. This information is decoded only from CB; it has no effect on the transport interface as long as it remains in CHB.

The CCB pulse (clear command buffer) clears CB. This pulse occurs at IOB RESET, INT CLR, and whenever the ILC flip-flop is set (indicating that the current command is illegal). For all noncontinuous commands except rewind, the CCB also occurs at the end of the ERM state of the tape status quint-flop (Figure 3-2, step 13, left branch). This occurrence of CCB terminates the application of the command levels to the transport interface. During the rewind command, the CCB terminates the command levels at the end of the quint-flop MOS state (step 8, REW). The UNU ∧ SNU condition for generating CCB is relevant only at the transport interface.

The contents of CHB28-31 are first advanced into CB28-31 by JNU, and (at least one CK1 interval later) the JNC pulse advances CHB20-27 into CB20-27. The CB contains six data fields. The significance of these fields is indicated in Table 3-1.

### TABLE 3-1   CB REGISTER BIT ASSIGNMENT

| Bits | Function |
|------|----------|
| CB20 | Governs slice level. Set to 1 for old tapes where more signal is required. (Not applicable to Interface 520.) |
| CB21 | Parity mode. Set to 1 for binary (odd) parity; to 0 for BCD (even) parity. |
| CB22-23 | Density in bits per inch.<br>00 = D200<br>01 = D556<br>10 = D800<br>11 = D556 |
| CB24-27 | Command codes. |
| CB28 | When 1, transport is to be kept reserved after completion of command. When 0, transport is to be returned to pool. (Interface 521 only.) |
| CB29-31 | Device selection code. (Can select up to eight tape transports.) |

### COMMAND DECODING

The four command bits CB24-27 are decoded to specify twelve different tape control operations (or no operation). The decoding is done in two stages. Bits CB25-27 are applied to binary-to-octal decoder 3E8 (BS-D-516-0-CM:A4). Three of the eight resulting levels, NOP, WRT,

3-8

and RDC, specify unique tape commands regardless of the state of CB24. The remaining five levels each produce two different commands, the choice depending upon the state of CB24. All commands are summarized in Table 3-2.

For each of the commands except rewind-unload, the command abbreviation represents a signal level actually occurring within the tape control. There is no rewind-unload level generated in the tape control. The REW level is sent directly to the transport interface; but when CB24 contains 1, the CON input to the interface causes the execution of a rewind-unload instead of a normal rewind.

### TABLE 3-2 COMMAND DECODING

| CB25-27 | Decoder Output Level | CB24 | Command to be Executed |
|---------|----------------------|------|------------------------|
| 000 | NOP | X | NOP (No Operation) |
| 001 | REW | 0 | REW (Rewind) |
| | | 1 | Rewind-unload (Not used with Interface 520.) |
| 010 | WRT | X | WRT (Write) |
| 011 | WEF | 0 | WRF (Write file) |
| | | 1 | WBT (Write blank tape) |
| 100 | RDC | X | RDC (Read compare) |
| 101 | RDE | 0 | RED (Read) |
| | | 1 | BER (Backward read) |
| 110 | SPF | 0 | SPF (Space forward) |
| | | 1 | SPF $\wedge$ SEF (Space forward and space to end of file) |

## TABLE 3-2  COMMAND DECODING (continued)

| CB25-27 | Decoder Output Level | CB24 | Command to be Executed |
|---------|----------------------|------|------------------------|
| 111 | SPB | 0 | SPB (Space backward) |
|     |     | 1 | SPB ∧ SEF (Space backward and space to end of file) |

## OUTPUT COMMAND LEVELS

There are four basic command levels sent to the transport interface units: WRITE, BAC, FOW, and REW (write, backward, forward, and rewind BS-D-516-0-CS:A2); at least one of these levels is used with every command. (Other levels and pulses of more specialized application are also sent from the tape control to the interface units; these levels and pulses are described in the context of their generating functions and in the appropriate interface chapters.)

The WRITE level is applied to the transport interface during both WRT and WEF commands. Within the tape control, WRITE is designated WWE. The WRITE level enables the write logic of the selected tape transport.

The BAC level is applied to the transport interface during both BER and SPB commands. Within the tape control, BAC is designated RSB. The BAC level causes the selected tape transport to operate in the backward direction. The BAC level is not sent to the 521 Interface. The FOW level is applied to the transport interface during those commands calling for forward tape motion. It is generated whenever the current command is neither a NOP, a REW, nor an RSB command.

The REW level is applied to the transport interface units during the REW and rewind-unload commands. It causes the selected tape transport to enter the rewind mode (reverse tape motion at about double the normal reading speed). The CON level is applied directly from CB24(1) to the transport interface. When both CON and the REW level are asserted, CON causes the selected transport to execute a rewind-unload.

## ILLEGAL COMMANDS

It is illegal for any command to be given to a transport that is already selected by another tape control (BCT). A read backward or space backward command cannot be given when the tape is at load point (TLP). Neither a write nor a write end-of-file command can be given when the tape write enable lockout ring is out (TWL).

The ILS level (BS-D-516-0-CS:A3) is asserted whenever an illegal command is given, indicating that the tape should not be accelerated. The ILS signal resets CON (and holds it reset regardless of the state of PRO at MDP). The ILS level also prevents the tape status quint-flop from being stepped to the UPS state (Chapter 4, Basic Quint-Flop-First Command), and causes the STM pulse to set the ILC flip-flop. The ILC set produces a CCB pulse that clears the CB register. The CCB pulse is sent to the transport interface as $0 \longrightarrow$ CM. The effect of the CB clear is to terminate the command levels to the interface and thereby to prevent an illegal command from starting tape motion.

The state of ILC can be sampled on IOB18 by device address 224.

## CONTINUE LOGIC

The state of CON (the continue flip-flop; BS-D-516-0-CS:D3) at the MDF pulse marking the end of ERM controls the stepping sequence of the tape status quint-flop and determines the operating cycle of the entire tape control (refer to Chapter 4, ERM state). At the MDP pulse preceding the end of ERM, if ILS is not asserted, the state of CON is determined by the PRO level (proceed; -CM:C7) and the assertion or nonassertion of PRO is, in turn, determined by whether or not the second command is sufficiently similar to the current command to require continue-mode operation.

To establish this similarity, the second command in CHB is compared with the current command in CB. If both commands select the same tape transport and if both require a similar response from that tape transport (motion in the same direction combined with writing — or not writing — for both commands), the PRO level is asserted. The CON flip-flop is then set, causing the tape control to enter continue mode.

Generation of PRO is accomplished by combining a number of subsidiary logic functions, including the CNA, CNB, CNC, RBC, and SEF functions (any one of which indicates that the requisite similarity of commands exists). The full logical conditions for generating PRO are listed and explained in the signal glossary, Chapter 12. Table 3-3 summarizes those command sequences which require continue-mode operations and the associated logic function which generates PRO during each such sequence.

TABLE 3-3  COMMAND SEQUENCES THAT REQUIRE CONTINUE MODE

| Second Command | Current Command | During ERM State the PRO Level is Generated by: |
|---|---|---|
| WRT | WRT | CNA – continue A; (write after write) |
| WEF | WEF | |
| RED | RED | CNB – continue B; (read forward continue) |
| SPF | SPF | |
| RDC | RDC | |
| SPB | SPB | CNC – continue C; (space backward continue) |
| | BER | |
| BER | SPB | RBC – read backward continue |
| | BER | |
| EFF(0) | SPF $\wedge$ CB24(1) | SEF – space to end of file |
| EFF(0) | SPB $\wedge$ CB24(1) | SEF – space to end of file |

# CHAPTER 4

# TAPE STATUS LOGIC

The tape status logic consists of a 5-state control device (the tape status quint-flop) and a programmable delay network which furnishes the basic time delays required to accelerate, move, and decelerate the tape.

## TAPE STATUS QUINT-FLOP

The tape status quint-flop (−CS:C1-6) continuously reflects the current status of the selected tape transport. The initial quiescent state of the quint-flop is called TCR (tape control ready). The second state UPS (up to speed) represents the acceleration period during which the tape is brought up to the required speed for forward or backward commands (but not for rewind; see REW Command Cycle, later in this chapter). During RIP (record in progress), the third state of the quint-flop, the tape is moving at the correct speed for reading or writing. The fourth ERM state (end of record motion) represents the tape runout interval between sensing the EOR mark and beginning to stop the tape. The final MOS (motion stop) state is the deceleration state during which tape motion is stopped.

### Quint-Flop Structure

The tape status quint-flop is composed of five 4-input negative diode NOR gates (3E18, 19, 20). The inputs to each of these five gates are taken from the outputs of the remaining four gates. The result of this arrangement is that the quint-flop functions as a 4-state flip-flop. It remains stable in any one of its five states; the active output is at ground, and the four quiescent outputs are negative logic levels.

### Basic Quint-Flop Cycle — First Command

The basic cycle of the quint-flop is shown in simplified form in Figure 4-1. The same basic cycle operations are shown in greater detail in Figure 3-2. The latter figure not only shows

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the quint-flop operations but also shows the concurrent operations of the command sync quad-flop. In addition to the basic cycle operations, Figure 3-2 also includes certain variations of the basic quint-flop cycle which arise during the rewind command (see REW Command Cycle), and during the execution of successive commands in continue mode (Second Command – CON(1)Λ ∿ SEF and Space to End of File Command – CON(1)ΛSEF in this chapter).

## TCR State

Because the quint-flop is reset to TCR state (Tape Control Ready) by IOB RESET, the quint-flop is always in TCR when the tape control receives its first command. The JNU pulse can be generated and the command sync quad-flop can be stepped from CHF to UNS only when TCR is asserted and the CNR flip-flop contains 0. Except in continue mode, JNC also can be generated only when the quint-flop is in TCR state.

## UPS State

After the transport interface receives the signal to start tape motion, an STM pulse is returned to the tape control (Chapter 3, Reset to XNC). This STM pulse signals the beginning of tape acceleration. Provided that the command is not illegal and not a REW command, the STM advances the tape status quint-flop to the UPS acceleration state (up to speed). The transition from TCR to UPS is shown in Figure 4-1, step 1, and in Figure 3-2, step 7, ∿REW. The quint-flop must be in UPS to advance to its third state RIP (record in progress).

## RIP State

After a predetermined acceleration delay (which varies depending on the nature of the current command), the motion delay logic (see Motion Delay Logic, later in this chapter) produces the MDF pulse that steps the quint-flop from UPS state to RIP state. In the RIP state, the tape is moving at the correct speed for reading or writing. All reading and writing must occur in RIP. (The RIP level is a necessary input condition for generating the RCP pulse, the ERC level, the EMC level, and the ERD delay; these functions are described in Chapters 5 and 6). The transition from UPS to RIP is shown in Figure 4-1, step 2, and in Figure 3-2, step 8, ∿REW. The tape status quint-flop must be in RIP to advance to its fourth state ERM (end record motion).
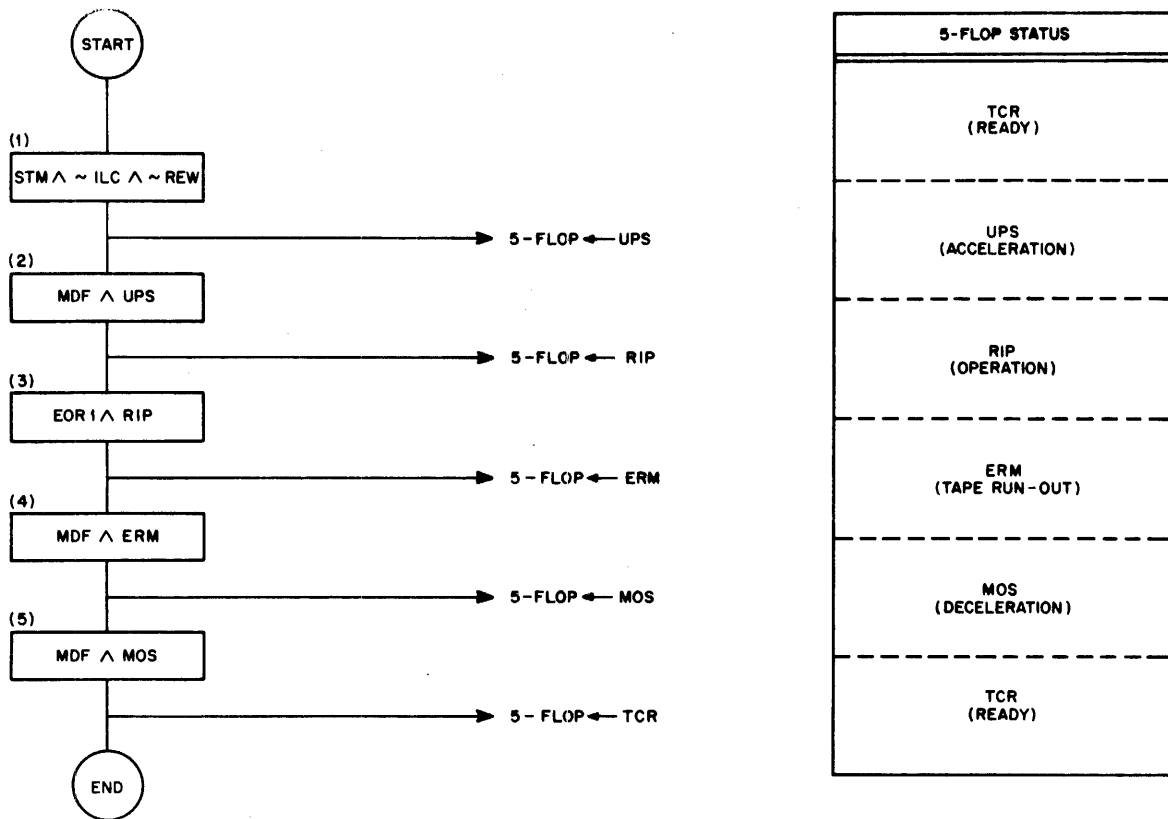
Figure 4-1   Tape Write and Read Signal Flow

## ERM State

When a command reaches the end of record, the EOR gap causes the generation of an EOR 1 pulse. That pulse steps the tape status quint-flop from RIP state to ERM state. The ERM state represents the tape runout interval between sensing the EOR mark and beginning to stop the tape. The ERM level is a necessary input condition for generating the TZA pulse which sets the LPE and RCE flip-flops (see Chapter 6, Read Comparison and Longitudinal Parity). The transition from RIP to ERM is shown in Figure 4-1, step 3, and in Figure 3-2, step 12.

For noncontinuous commands (CON = 0), the quint-flop advances from ERM state to its fifth and final state MOS (motion stop). During continuous-mode commands (CON = 1), the quint-flop is reset directly from ERM to UPS; continue mode operations are described in greater detail under Second Command - CON(1)$\wedge \sim$SEF and Space to End of File Command - CON(1)$\wedge$SEF in this chapter.

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## MOS State

After a predetermined runout delay (which varies depending on the nature of the current command), the motion delay logic (-MD) produces the MDF pulse that steps the tape status quint-flop from ERM state to its final MOS state. The delay selected determines the correct amount of tape which is allowed to run past the tape heads before starting to brake the transport and decelerate the tape. The same MDF pulse that signals the expiration of the ERM runout delay also produces a CCB pulse which clears CB and terminates the application of command levels to the transport interface. The MOS deceleration state represents the time interval required to actually bring the moving tape to a complete stop. The transition from ERM to MOS is shown in Figure 4-1, step 4, and in Figure 3-2, step 13, CON(0). During REW commands, the MOS state is used for an entirely different purpose; the duration of MOS then controls the period during which the REW command level is applied to the transport interface; this alternate function of MOS is described under REW Command Cycle below.

## Reset to TCR

After a predetermined deceleration delay (which varies depending on the nature of the current command), the motion delay logic produces the MDF pulse that resets the tape status quint-flop from MOS state to TCR. This quint-flop reset is shown in Figure 4-1, step 5, and in Figure 3-2, step 14, CON(0). Once the tape status quint-flop is again in the TCR state, the JNU pulse can be generated, advancing the device selection portion of the next (second) command from CHB28-31 to CB28-31, and stepping the command sync quad-flop from CHF to UNS.

The generation of JNU and the CHF to UNS transition of the quad-flop assumes that the quad-flop was in CHF by the time that the tape status quint-flop is reset to TCR. If no new command has been given by the time that the quint-flop reset occurs, CHB remains empty, and the command sync quad-flop remains in XNC until the next CONO tape control command arrives from the processor.

## REW Command Cycle

During the execution of the REW commands, rewind and rewind-unload, the tape status quint-flop follows the sequence of operations shown in Figure 3-2, steps 7-10, REW.

## Command Level Timing

The REW command levels are first applied to the transport interface at the JNC pulse (Figure 3-2, step 5). One CK1 interval later, the CTT pulse is applied to the transport interface, causing an STM pulse to be returned to the tape control, and thereby advancing the quint-flop directly from the TCR state to MOS (Figure 3-2, step 7, REW). The duration of the MOS state determines the period during which the REW command level is applied to the transport interface.

The TCR to MOS transition of the tape status quint-flop is implemented in the following manner. The REW output of the command decoder (Chapter 3, Command Decoding) is inverted (-CM:C4) and applied to input K of the negative diode 3D25 (-CS:D1) preventing the TCR to UPS transition of the tape status quint-flop that normally occurs at the STM pulse during non-REW commands. The same inverted REW level is also applied to input V of capacitor-diode 3E17 (-CS:D5), enabling the STM pulse to step the quint-flop directly from TCR to MOS (as indicated in Figure 3-2, step 7, REW).

After a predetermined delay (which varies depending upon the logical requirements of the type of interface and transport used), the motion delay logic produces the MDF pulse that returns the quint-flop from MOS state to TCR state (step 8, REW). This same MDF pulse produces the CCB pulse that terminates the REW command levels. The CCB pulse is sent to the transport interface as $0 \longrightarrow CM$.

## Deceleration Interval

If the rewinding transport is still selected when it reaches TLP, the tape status quint-flop is once more advanced from TCR to MOS (Figure 3-2, step 9, REW). After a predetermined deceleration delay (unrelated to the command-timing delay described above), the motion delay logic produces another MDF pulse which once more resets the quint-flop from MOS to TCR (step 10, REW). This second reset from MOS to TCR indicates that enough deceleration delay has elapsed to stop tape motion. The same MDF pulse that resets the quint-flop from MOS to TCR is gated by TLP (tape at load point) to set the load point interrupt flag LIF (step 10, REW). If LIE contains 1, the LIF set produces a PIE signal (priority interrupt enable) which notifies the programmer that the selected transport has reached load point. The LIF can also be sampled directly by a CONI 224 instruction.

The MOS deceleration state occurs only if the rewinding transport remains selected until it reaches TLP. (Otherwise, there is no TLP pulse to step the quint-flop to MOS.) This use of the MOS deceleration state during REW command serves as a safeguard to avoid giving a new forward command while the transport is in the process of decelerating. The programmer can take advantage of this safeguard, and can utilize the LIF flag, only by keeping the rewinding transport selected (thus keeping the quint-flop in MOS state) until deceleration is complete.

Although the tape transports have a built-in stop at TLP condition, there is still the hazard of the programmer inadvertently calling for a forward tape command on a given nonselected transport after that transport has reached TLP, but while it still retains some backward momentum. This could result in the quint-flop progressing to RIP state before the tape can come up to full forward speed.

If the programmer is certain that he will not use the rewinding transport again until after it has completed the rewind and come to a full stop, the potential difficulty no longer exists, and there is no need to keep the tape transport selected. A new command to another tape transport can be given at any time after the first time the quint-flop is reset to TCR. This programming procedure is represented by the return path from step 8, REW back to step 1.

## Second Command - CON(0)

A second CONO tape control command can be programmed at any time after the first command advances the tape status quint-flop to the RIP state. In Figure 3-2, the second command is shown as steps 9 and 10, ~REW, but note that the second command need not be given at that specific point of the first command cycle; the second command can be programmed at any point after step 8, ~ REW.

Provided that CON = 0, the second command is executed in exactly the same manner as the first command, except that the transfer of control information from CHB to CB is delayed until CB is cleared and the first command is finished. If the second command is given before the completion of the first command (as in the sequence shown in Figure 3-2), the command sync quad-flop advances from XNC to CHF (step 11), but must wait in CHF state until the first command is completed. As described under Basic Quint-Flop Cycle - First Command above,

the tape status quint-flop completes the first command by advancing from RIP to ERM, then from ERM to MOS, and finally from MOS to TCR; see steps 12-14, CON(0).

Once the tape status quint-flop has been reset to the TCR state, the next CK1 pulse produces a JNU pulse, advancing the contents of CHB28-31 to CB28-31 and selecting a tape transport for the second command. The JNU, in turn, produces an MCL which clears the tape control in preparation for the second command. The same JNU pulse advances the command sync quad-flop from CHF to UNS. The second command then proceeds without further interruption in exactly the same manner as the first command. The completion of the first command is shown in Figure 3-2 as step 14, CON(0), and the generation of JNU is indicated as immediately following that step (connector A at step 4 of the diagram).

## Second Command - CON(1)∧ ~ SEF

Continue mode operation requires a sufficient degree of similarity between the current command and the next (second) command so that there is no need to stop the tape at the end of the current command, (refer to Chapter 3, Continue Logic). Instead, tape motion is allowed to continue. After the runout of sufficient tape for the correct record gap, the second command is executed immediately without any pause to stop and restart the tape. This change from normal non-continuous operation requires modifications in the operating cycles of both the command sync quad-flop and the tape status quint-flop.

### Decision to Enter Continue Mode

At the MDF pulse that concludes the ERM phase of the first command, the state of the CON flip-flop is sampled to determine whether or not the second command is to be executed in continue mode. The state of CON at MDF is, in turn, dependent upon the state of the PRO level at the preceding MDP pulse, which occurred 1 μsec before the MDF pulse. (For a detailed description of the logical conditions which govern the state of the PRO level and determine whether or not the tape control is to enter continue mode at the end of ERM, refer to Chapter 3, Continue Logic.)

## Summary of Quint-Flop and Quad-Flop Operation - CON(0)

If CON(0) is asserted at the MDF that terminates ERM, no continue mode operation is called for, and the tape control follows the CON(0) sequence described previously under Second Command - CONO(0). This sequence is represented by the left branch of the flow diagram; Figure 3-2, steps 13-14, CON(0). The first command is completed in the normal manner. The tape status quint-flop steps through its five states in regular rotation: TCR, UPS, RIP, ERM, MOS, and then is reset to TCR in preparation for the second command. The command sync quad-flop also follows the CON(0) sequence described under Second Command - CONO(0). During the execution of the second command, the quad-flop proceeds through the four states of its cycle in regular rotation: XNC, CHF, then (after waiting for the completion of the first command and the reset of the quint-flop to TCR), UNS, and MTS, and finally a reset to XNC in preparation for still further commands.

## Tape Status Quint-Flop Operation - CON(1)

When CON(1) is asserted at the MDF that terminates ERM (indicating that the second command is to be executed in continue mode), the quint-flop and quad-flop operating cycles differ considerably from those described above. When CON = 1, the tape status quint-flop skips the final MOS state. It proceeds through the first four states as usual, but from ERM it is returned directly to the UPS state instead of being advanced to MOS. The MDF pulse at the end of ERM causes this return to UPS (see Figure 3-2, step 13, CON(1)). Unless the current command is a SEF command, this same MDF pulse also produces a JNC pulse, advancing the control information of the second command from CHB20-27 to CB20-27 and applying the command levels of second command to the transport interface. (If the current command is a SEF command, the JNC pulse is omitted (refer to Space to End of File Command - CON(1)∧SEF below.)

## Command Sync Quad-Flop Operation - CON(1)

The command sync quad-flop cycle is also altered during continue mode operations. Although the quad-flop is stepped from XNC to CHF after the second command is loaded into CHB, regardless of whether or not the second command requires continue mode operation (Figure 3-2, step 11), the quad-flop is never advanced to UNS or MTS when CON contains 1. Instead the same MDF pulse that terminates the ERM state of the tape status quint-flop generates a JNC

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pulse; this JNC resets the command sync quad-flop directly from CHF to XNC (see Step 13, CON(1)). Because the continue mode requires that the same tape transport be selected for successive commands, no JNU pulses are needed. Since the transport is not stopped between commands, the start pulse is also unnecessary; no IOT 7104 pulse is sent to the transport interface, and no STM pulse is returned to the tape control. Because both the JNU pulses and the start pulses are omitted during a series of continue mode commands, the quad-flop cycle can be shortened by deleting both the UNS and MTS states.

## Flow Diagram - CON(1)∧ ∿ SEF

For those continue mode operations in which the current command is not a SEF command, the NDF pulse that terminates ERM produces the sequence of operations represented by the right subbranch of the right branch of the Figure 3-2 flow diagram (step 13, CON(1)∧ ∿ SEF). The MDF pulse steps the tape status quint-flop from ERM state to UPS. The same MDF pulse produces an MCL pulse that clears all tape control flip-flops except the four interrupt enable switches, CON, and LPH in preparation for the next command. The MDF also generates a JNC pulse that steps the command sync quad-flop from CHF state to XNC, advances the control information of the second command into CB, and clears CHB20-21.

After the normal acceleration delay for the type of command represented by the second command, the motion delay logic produces another MDF pulse which steps the tape status quint-flop from UPS state to RIP state. The UPS interval is not used in this case for acceleration, but rather as a tape runout interval to allow for the correct record gap prior to the commencement of the second command RIP state. As soon as the quint-flop is advanced to RIP, the second command is executed in the normal manner.

From connector B at the bottom of the Figure 3-2 flow diagram, the tape control operating sequence returns to the top of the diagram (see step 8, ∿REW). At any time after the MDF pulse that causes the UPS to RIP transition of the quint-flop, a third command can be given. Because the command sync quad-flop is in the XNC state (at step 8, ∿REW), there is no need to bypass steps 9-11. These steps are omitted during the SEF command sequence described in the next paragraph.

## Space to End of File Command - CON(1)∧SEF

If the current command is an SPF (space forward) or SPB (space backward) with CB24(1), the selected transport executes an SEF (space to end of file). This is done by repeating the SPF or SPB command until the file mark record is sensed. The SPF or SPB commands making up the SEF sequence follow the left subbranch of the right branch of the flow diagram (see Figure 3-2, CON(1)∧SEF).


### Command Iteration

The entire SEF sequence is controlled by the single SPF or SBP command in the CB register. That command is executed over and over again until the tape reaches the end-of-file record. During each iteration of the command that occurs while the tape control remains in the SEF loop, the sequence of operations returns from the bottom of Figure 3-2 to the top of the diagram (connector B). Each time the tape status quint-flop advances from ERM state to UPS state (step 13, CON(1)∧SEF), another iteration of the SPF or SBP command begins.

No JNC pulse is produced between successive space commands (see —CS:B3). Therefore, CB is not cleared; and if a second command is programmed during the execution of the SEF, the control information for that command remains in CHB until the SEF is completed. Until CHB is free, no further commands can be sent to the tape control without destroying the second command.


### Quad-Flop States During SEF Loop

The flow diagram shows the programming of a second command during the execution of the SEF loop (Figure 3-2, steps 9-11). This second command is stored in CHB while the SEF is in progress; the presence of the command code in CHB steps the command sync quad-flop from XNC state to CHF (step 11). Since no JNC pulses are produced during the iterated SEF commands, the quad-flop remains in CHF state throughout the SEF loop, and may not be reset to XNC until the SEF is completed. The CHF state of the quad-flop warns the programmer that the CHB is full and that the tape control is not ready to receive a third command. In the flow diagram, this restriction is indicated by the path bypassing steps 9-11 when XNC is not true.

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## Escape from SEF Loop

When the end-of-file record is sensed, the EOF level sets the EFF flip-flop and ends the SEF level. The termination of the SEF level permits the tape control to escape from the SEF loop. The MDF pulse that marks the end of the ERM state of the final SPF or SPB commands (the commands that read the file mark record) then causes the tape control to follow either the left branch of the flow diagram, CON(0), or alternatively, the right subbranch of the right branch of the diagram (CON(1)ΛSEF). The choice depends on whether or not a continue-mode command follows the SEF.

If a continue-mode command follows the SEF (e.g., a BER command following a backward SEF), the MDF that terminates the ERM phase of the final SPB iteration produces a JNC pulse. That JNC pulse advances the new command from CHB to CB, and resets the command sync quad-flop from CHF to XNC. The control then starts to execute the new command, and because XNC is true, still another command can be sent into CHB (Figure 3-2, steps 9-11).

If the command that follows the SEF sequence is not a continue mode command (e.g., a BER command following a forward SEF), the MDF that terminates the ERM phase of the final SPF iteration cannot produce an immediate JNC pulse. Instead, the tape control follows the sequence indicated by the left branch of the flow diagram, CON(0). The tape status quint-flop then progresses from ERM state to MOS (step 13), and from MOS to TCR (step 14). A JNU can then be generated (step 4), advancing the command sync quad-flop to the UNS state. From UNS, the quad-flop advances to MTS and then to XNC. (As soon as the quad-flop is reset to XNC state, CHB is free to accept another command.)

## MOTION DELAY LOGIC

The motion delay logic (BS-D-516-0-MD) is composed of a 4303 Integrating Single Shot module MOD, a set of logically gated delay resistors, a triggering network, and a pair of output pulse amplifiers. Any one of 12 motion delay resistors can be gated into the MOD single shot circuit. Each resistor produces a different delay period. A major advantage of this design is the efficient use of the single delay circuit which provides twelve separate programmed delays. Similar delay networks are used in the write and read logic described in Chapters 5 and 6.

## Triggering

The MOD single shot is triggered by a positive-going level change at input terminal S while a ground level is applied to input terminal T. The rising trailing edge of the SMD output pulse from pulse amplifier 3D19 (-MD:B5) provides the level change. The ground level gate is derived from the terminal K output of negative diode 3D18. The delay period is started by setting MOD to the 1 state. At the expiration of the delay, the MOD resets itself to the 0 state.

## Output Pulses

When the MOD resets itself to the 0 state, a 1-μsec MDP pulse is generated at output terminal J of pulse amplifier 3D19 (-MD:A5). One μsec later, a 1-μsec MDF pulse is generated at output terminal V of pulse amplifier 3D16. In addition to being used within the tape control, the MDF pulse is also sent to the transport interface as MP.

## Delays

Table 4-1 summarizes the operation of the motion delay logic. Although the logical gating of the various delays is the same for each of the five types of transport used with the 516 Control, the actual time constant of the delays used varies in accordance with transport requirements.

The six UPS delays (D1, D2, D11, D6, D4, and D5) are listed at the top of Table 4-1. One of these six UPS delays is used to time each UPS acceleration period. The choice depends upon the nature of the current command and whether or not the tape is at load point.

The next three entries in Table 4-1 are the three ERM delays (D10, D3, and D7). One of these three ERM delays is used to time each ERM tape runout interval. The choice between these three delays depends only upon the nature of the current command.

The next two entries are the MOS delays (D8 and D9). Delay D8 (selected by the REW level) is used to time the duration of the REW command level. Delay D9 (selected by the NOP level) is used to time all tape deceleration periods. The NOP level is asserted from the time that the CCB pulse clears the CB register. During all noncontinuous commands, NOP is asserted when MDF terminates the ERM state of the tape status quint-flop.

The twelfth and final delay D0 is never triggered, but during TCR and RIP the twelfth resistor is gated in to keep the MOD Integrating Single Shot 4303 operative.

## TABLE 4-1   MOTION DELAY LOGIC

| | Selected by | SMD Gen-erated by | SMD Gated by | Purpose of Delay | Time Constant (msec) for Tape Transport Type | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | DEC 50 | DEC 570 | IBM 729V | IBM 729VI | IBM 7330 |
| D1 | UPS ∧ FRD ∧ LPH(0) | STM | UPS | FRD acceleration ( ~ LP) | 1.8 | 5.0 | 3.0 | 2.0 | 9.0 |
| D2 | UPS ∧ FRD ∧ LPH(1) | STM | UPS | FRD acceleration (LP) | 24.0 | 33.0 | 24.0 | 16.0 | 50.0 |
| D11 | UPS ∧ RSB ∧ LPH(0) | STM | UPS | RSB acceleration ( ~ LP) | 3.0 | 5.0 | 3.0 | 2.0 | 9.0 |
| D6 | UPS ∧ WRT ∧ LPH(0) | STM | UPS | WRT acceleration ( ~ LP) | 6.0 | 5.5 | 7.5 | 5.0 | 7.0 |
| D4 | UPS ∧ WRT ∧ LPH(1) | STM | UPS | WRT acceleration (LP) | 78.0 | 66.0 | 48.0 | 32.0 | 140.0 |
| D5 | UPS ∧ WEF | STM | UPS | WEF acceleration | 48.0 | 26.7 | 40.0 | 26.7 | 83.0 |
| D10 | ERM ∧ FRD | EOR 1 | ERM | FRD tape run-out | 2.0 | 1.3 | 1.0 | 0.67 | 9.0 |
| D3 | ERM ∧ RSB | EOR 1 | ERM | RSB tape run-out | 5.5 | 1.5 | 4.0 | 2.7 | 11.8 |
| D7 | ERM ∧ WWE | EOR 1 | ERM | WWE tape run-out | 2.5 | 1.8 | 1.5 | 1.3 | 11.0 |
| D8 | MOS ∧ REW | MDF | MOS | REW command level duration | 20.0 | 11.0 | 20.0 | 11.0 | 30.0 |
| D9 | MOS ∧ NOP | MDF | MOS | MOS deceleration | 12.0 | 11.0 | 17.0 | 11.0 | 17.0 |
| D0 | TCR ∨ RIP | NO | NO | Keeps MOD 4303 circuit operative | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 |

# CHAPTER 5

# WRITE LOGIC

## FUNCTION OF WRITE LOGIC

The write logic (shown in drawing BS-D-516-0-WT) controls the execution of three write commands: WRT, WRF, and WBT (write, write file, and write blank tape). A crystal clock within the write logic governs the rate at which WP pulses are applied to the transport interface and determines the rate at which characters are written on tape. The same internal clock also controls the rate at which the tape control sends TK/GV LT data request command pulses to the Data Control 136.

During the WRT command (see Write later in this chapter), the write logic causes the tape control to request a 6-bit output data character from the Data Control 136, then transfers the character to the transport interface to be written on tape; requests a second output character, writes it on tape, etc. This process continues as long as the Data Control 136 still has data to send (i.e., until the data control reaches the end of the current output record). When the end of the record is reached, the write logic times out an EOR gap of slightly over four character spaces and causes the transport to write an EOR mark.

During the WRF command (see Write File later in this chapter), the write logic causes an end-of-file record to be written. The EOF record consists of a file mark character (17 octal) followed by a 4-character-space EOR gap, followed in turn by an EOR mark. During the WBT command (see Write Blank Tape later in this chapter), the write logic produces a WBT level, but no WP pulses. This causes the tape to advance and erase approximately 3 inches.

## CLOCK CIRCUITRY

The write logic contains two 4407 Crystal Clock circuits which run continuously as long as the tape control is turned on. Clock 1 at location 3C14 (-WT:B4) is adjusted to produce CK1 output pulses at twice the character rate of the tape transport operated at a density of 800 characters per inch. Clock 2 at location 3C15 (-WT:B6) produces CK2 output pulses at twice

the character rate of the transport operated at 556 density. Both clock frequencies are directly proportional to both the density and tape speed of the transport to be used with the tape control.

The principal output of the clock network is the CKP (clock pulse) output from pulse amplifier 3C16. The CKP provides the frequency standard for the character frequency flip-flop CF (—WT:A2). During the period when the EWC flip-flop contains 1, each CKP complements the CF (to see Start Sequence below). For each of the three available character densities (refer to Table 3-1), the CKP pulses are generated at twice the character rate of the tape transport. If D800 is asserted, indicating that the current write command calls for a character density of 800 characters per inch, a CKP pulse is produced at each CK1 pulse (—WT:B6). If D556 is asserted, CKP coincides with CK2. For D200 write commands, CKP is generated at every fourth CK1 (—WT:A6). The 2-stage counter composed of the C/2 and C/4 flip-flops (—WT:A5) provides the required frequency division. For each of the three available densities, the CKP pulses are always produced at exactly twice the frequency at which output characters are currently to be written on the tape.

Besides being used to generate CKP during D800 and D200 write commands, the CK1 pulse is also used directly for several other functions within the tape control. The CK1 pulse is used during noncontinuous commands to trigger JNU, JNC, and CTT. The CK1 is also used to advance the command sync quad-flop from XNC state to CHF whenever a new command is loaded into CHB.

## WRT COMMAND CHARACTER TIMING

The transitions of the character frequency flip-flop CF govern the character rate during write commands. Every 0 to 1 set transition of CF causes the generation of a WCP write clock pulse (—WT:A4). Every 1 to 0 reset transition of CF causes a TK/GV LT (—CS:B4) data request command pulse to be sent to the Data Control 136.

## WP Write Pulse

The WCP is sent to the transport interface as WP (—WT:A4) (at present it is not used within the tape control). At each WP, those flip-flops of the write buffer register which are receiving 1 data levels are complemented, causing the selected tape transport to write a 1 in the corresponding tape channel.

## TK/GV LT Data Request Command Pulse

At the Data Control 136, the TK/GV LT pulse shifts the data accumulator left by six bit-positions, and increments the character counter. During both WRT and RDC commands, the data control applies the contents of its six high-order accumulator DA0-5 to the tape control via the write data output levels WD0(1)-WD5(1) (-WT:C2-4)(see Write-Data Outputs below). The 6-bit left shift caused by each TK/GV LT data request command pulse advances the next output character into position to be sampled by the tape control. As long as output data remains to be written, the sequence continues: a TK/GV LT data request command pulse is sent to the data control at each 1 to 0 transition of CF, and the ensuing output data is written on tape at the 0 to 1 transition of CF.

## Synchronizing Circuit

The CKP pulses provide the complementing signals that cause the transitions of the character frequency flip-flop CF. However, although CKP pulses are continuously generated whenever any one of the three density levels is asserted, they are allowed to complement CF only while the EWC flip-flop contains 1 (-WT:B2). The EWC and WES flip-flops make up a 2-stage synchronizing network; during WRT commands, this network ensures that the write clock pulses sent to the transport interface are complete and are in phase with the CKP.

## Start Sequence

The WRT command can start to write a record only after the tape status quint-flop has reached the RIP state. The MDF pulse, marking the UPS to RIP transition of the quint-flop, produces a BRP pulse (-CS:B6). During the WRT command, the BRP pulse sets the WES flip-flop to the 1 state (-WT:B3). The first CKP that arrives in time sets EWC to 1. (The transition of EWC is not necessarily in exact synchronization with the leading edge of the CKP.) The next CKP, and every succeeding CKP that occurs while EWC(1) is still asserted, complements CF. The transitions of CF are all synchronized with the leading edges of the CKP pulses.

## Stop Sequence

After the last character of a record has been written, the CF flip-flop is in the 1 state. It is reset to the 0 state once more, generating a final TK/GV LT character request command pulse.

The EWD delay (−WT:C7) is set 2.4 μsec after this final TK/GV LT (see End of Record Write Delay below). The set of the EWD delay causes both the EWC and the WES flip-flops to be reset to 0. Because the EWC(1) level is no longer asserted, the following CKP is not permitted to complement the CF, so CF remains reset. Although the final TK/GV LT pulse does cause the data control to shift its accumulator contents left six bit-positions, this final shift does not bring any new data into position to be sampled by the tape control. The final TK/GV LT pulse shifts the last data character out the left end of the data control data accumulator, resets the data control character counter, and sets the DA RQ status bit to 1.

The first output character is always sampled by the tape control and written on tape at the WP that precedes the first TK/GV LT shift. Similarly, the last character of the output record is sampled and written on tape by the WP that precedes the final TK/GV LT shift. The first CF transition is always a set transition which writes the first character of the record. (This character need not be shifted; it is initially in the correct position to be sampled and written out.) The last CF transition is always a reset transition. This reset applies the final TK/GV LT to the data control after the last character has been written.

## WRITE-DATA OUTPUTS

During the WRT and WRF commands, the WD output levels WD0(1)-WD5(1) (−WT:C2-4) transfer write-data to the write buffer register in the transport interface. Ground levels represent 1s in the corresponding bit-positions of the output data character. For the RDC command, the WD output levels apply the same write-data to the LPA; refer to Chapter 6, Read Compare Command for a description of the RDC command.

## WRT and RDC

During the write and read compare commands, the WD outputs are the direct complements of the DA levels from the Data Control 136 for all output characters except 0 BCD. A single-pole, double-throw switch is mounted in front of logic panels 3D and 3E. The switch is necessary if there is a need to write (N) characters per record BCD so that the total number of characters written is not a factor of 6. This is accomplished by filling in with blank characters, left, (BCD 00) in the first word of a record written.

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In BCD (even) parity mode, 00 octal is converted to the 0 character Hollerith code (12 octal) before being written or read-compared, provided the front panel switch is set to 12. If the front panel switch is set to 12, the unmodified 0 character is prohibited in BCD mode because with even parity the parity bit would be 0 also, leaving an entire tape frame with no 1 bits whatever. Such a frame could not be distinguished from blank tape or the total failure to write a character.

To write less than six characters in the first word of a record, the front panel switch must be set to the 00 or up position. This inhibits the conversion of BCD 00 to BCD 12. Caution must be exercised when the switch is set to this position. Conversion of BCD 00 to 12 within a record must be done by the program prior to the execution of a BLKO or data instruction to the 136 Data Control.

When the record is read, the blank character will be ignored. Thus, each word read will be shifted to the left n characters as determined by the number of blank characters written.

For all characters except the BCD 0, the negative output of inverter 3C18 (-WT:C1) causes the DA levels to be inverted and gated through to the corresponding WD outputs. Although the DA levels are negatively asserted, the corresponding WD outputs are asserted at ground. When the 00 octal character occurs in BCD parity (CB21 = 0) and the switch is set to 12, the level DA = 0 appears at terminal J of diode 3C21 (-WT:D3). This level causes two inverters at location 3C5 to ground the WD2(1) and WD4(1) outputs. The remaining four WD outputs are held negative because the corresponding DA levels represent 0 bits. In this way, the six WD outputs form the 0 character Hollerith code 001 010 (12 octal).

## WRF

During the write file command, the WD outputs are not affected by the DA levels from the Data Control 136. The WRF level from negative diode 3C23 (-WT:B4) is applied to terminal P of inverter 3C18. The WRF level causes four inverters at location 3C18 to ground the four low-order WD outputs. The remaining two WD outputs are held negative by diode 3D22. The WRF level causes the WD outputs to assume the configuration of the file mark character 001 111 (17 octal).

# END OF RECORD WRITE DELAY

The 4303 Integrating Single Shot EWD (-WT:C7) controls the interval between the final write pulse of each WRT or WRF record and the EOR 2 pulse which produces the EOR mark (the longitudinal parity check character). The EWD delay is adjusted to write the EOR mark four character spaces beyond the final data character of the record. The delay varies inversely with the density of characters per inch of tape. Any one of three motion delay resistors can be gated into the single shot circuit; each of them produces a delay period appropriate to one of the three available character densities, D200, D556, or D800.

## Triggering of EWD

The delay period is started by setting EWD to the 1 state. The EWD(1) level resets EWC and WES, terminating both the write pulses and the TK/GV LT character request command pulses (refer to Stop Sequence described previously). During the WRF command, the WCP which writes the last, and only, data character of the file mark record is triggered by BRP (-WT:A4). The same BRP pulse starts the EWD delay. The EWD expires four character spaces later, producing the correct 4-character EOR gap between the file mark character and the EOR mark at the end of the file mark record. During the WRT command, the final TK/GV LT pulse of the record sets the EWD delay.

The DA RQ(1) signal (-WT:D6) from the Data Control 136 distinguishes the final TK/GV LT pulse from the preceding TK/GV LT pulses. The Data Control 136 sets its DA RQ status bit to 1 slightly more than 1 μsec after it receives the final TK/GV LT command pulse of each 6-character data word. Provided that additional data words follow, the data control then resets DA RQ to 0 approximately 1 μsec after setting it to 1. If DA RQ is still in the 1 state 2.4 μsec after a given TK/GV LT pulse, this indicates that no further data words are available to be written out; i.e., that the given TK/GV LT command pulse is not only the final pulse of a data word, but further that it is the final pulse of the current record.

All of the TK/GV LT pulses applied to input K of pulse amplifier 3C24 are delayed 2.4 μsec by the chain of three pulse amplifiers 3C24 and 3C25. This allows sufficient time to determine whether or not the data control will keep DA RQ set to 1. The write pulse that writes the last character of the record precedes the final TK/GV LT pulse of the record by one-half a

character interval (refer to Stop Sequence). Therefore, the total record gap delay is one-half a character interval plus 2.4 μsec greater during the WRT command than during the WRF command.

## Output of EWD

At the expiration of the EWD delay, the EWD resets itself to the 0 state and causes pulse amplifier 3D19 (—WT:A7) to generate the EOR 2 pulse. The EOR 2 pulse causes the writing of the EOR mark (the longitudinal parity check character). The EOR 2 is sent to the transport interface as START 1; at present EOR 2 is not used within the tape control. At each START 1, all flip-flops of the write buffer are cleared. The clear complements just those flip-flops that are in the 1 state after the final character of the data record; i.e., just those flip-flops that have already been complemented an odd number of times. Because each time a write buffer flip-flop is complemented the transition causes a 1 to be written on tape, the START 1 clear writes a longitudinal parity check character which yields an even parity for each channel of the record (including the parity channel). Pulse amplifier 3D19 also produces an EOR 2 at MCL as an extra safeguard to ensure that each record begins with every write buffer flip-flop reset to 0.

## WRITE COMMANDS

There are three write commands, WBT, WRF, and WRT. The write blank tape command advances and erases about 3 inches of tape. The write file command causes the writing of a record containing only the single file mark character 17 octal followed by an EOR gap and an EOR mark. The write command writes whatever data record is sent to the tape control from the Data Control 136 and generates an EOR gap followed by an EOR mark. All three write commands cause the transport to read the same data that it is writing. This concurrent read operation terminates the write and write file commands by generating an EOR 1 pulse when the EOR gap is sensed. The write blank tape command is also terminated by the EOR 1 pulse, but for the WBT command EOR 1 is produced by the BRP that marks the end of the UPS acceleration state rather than by sensing the EOR gap. The generation of the EOR 1 pulse is described in the read logic chapter (Chapter 6, End of Record).

## Write Blank Tape (Figure 5-1)

The WEF level is present during each WBT command and causes the application of the WRITE level to the transport interface. Since neither NOP, REW, nor RSB is asserted, a FOW level is also applied to the transport interface for WBT commands (—CS:A1-2). Although the WRITE signal is applied to the transport interface during the WBT command, no write pulses are sent to the interface and no data is written. The write amplifiers are turned on, but the write-head polarity is not switched. The write heads produce the same sense of magnetization through-out the entire length of the tape.



Figure 5-1  Write Blank Tape - WBT

During UPS state of the tape status quint-flop, the transport accelerates the tape. At the end of UPS state, the quint-flop is advanced to RIP, and a BRP pulse is generated (Figure 5-1, step 1). During the write blank tape command, the BRP directly generates the EOR 1 pulse (Figure 5-1, step 2). This EOR 1 causes the tape status quint-flop to advance from RIP to ERM state (Figure 5-1, step 3). The ERF flip-flop will be set to a 1, 3.5 character spaces

after EOR 1, asserting PIE (Figure 5-1, steps 4 and 5). Because the WRT level is not asserted during WBT, the BRP has no effect on the WES flip-flop, and no write clock pulses can be generated (-WT:B3).

The remainder of the command cycle is shown in Figure 3-2, step 13, etc.

## Write File (Figure 5-2)

The WEF level causes the application of the WRITE level to the transport interface. A FOW level is also applied to the transport interface for WRF commands (-CS:A2). During UPS state of the tape status quint-flop, the transport accelerates the tape. At the end of UPS state, the quint-flop is advanced to RIP, and a BRP pulse is generated; Figure 5-2, step 1. The WRF level enables the BRP to produce a single WCP (-WT:A4) which is applied to the transport interface as a WP write pulse (step 2). This WP pulse causes the WD outputs to write the file mark character, 17 octal, on tape; refer to WRF, discussed previously in this chapter.
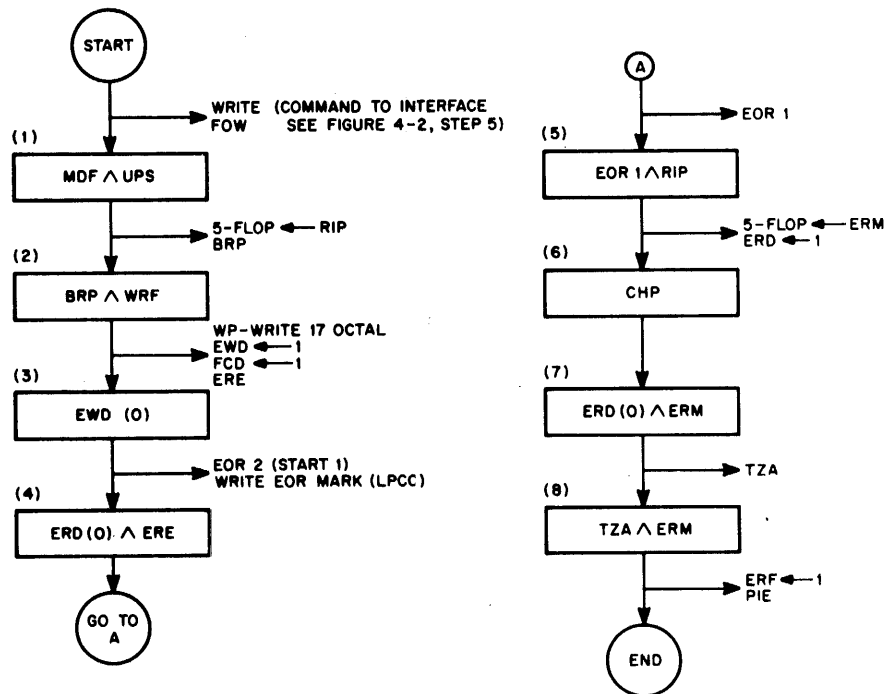


Figure 5-2  Write File - WRF

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The BRP also sets EWD to 1 and begins the EOR gap delay. After the write heads write the file mark character, the read heads read it. The FCD flip-flop is set to 1, and the ERE level is asserted. The ERE level permits the generation of an EOR 1 pulse when the EOR gap is sensed. When the EWD times out, an EOR 2 pulse is generated and sent to the transport interface as START 1. The START 1 writes the EOR mark (longitudinal parity check character) on the tape (step 3).

The WRF command is terminated by the generation of an EOR 1 pulse. The read logic ERD is set each time a character is read and is reset only if the tape displays an empty interval of at least 3.5 character spaces with no characters to be read. Provided that the ERE level is present, the reset of ERD generates an EOR 1 pulse. During the WRF command, the ERD times out and is reset to 0 when the read heads sense the EOR gap (which is four character spaces long). The ERD times out before the EOR mark is reached, producing the EOR 1 pulse (step 4). The EOR 1 pulse advances the tape status quint-flop to ERM state (step 5). The EOR 2 pulse that is generated prior to when the EOR mark is reached sets the ERD delay to 1 (step 6). One μsec after the ERD times out and is reset, pulse amplifiers 3D4 (−RD:B2) produce a TZA pulse (step 7). Because the quint-flop is in ERM state, that TZA pulse sets the end-of-record flag ERF (−MD:B6). Provided that the EFE flip-flop contains 1, the ERF set produces a priority interrupt enable signal PIE (Figure 5-2, step 8). The remainder of the command cycle is shown in Figure 3-2, step 13, etc.

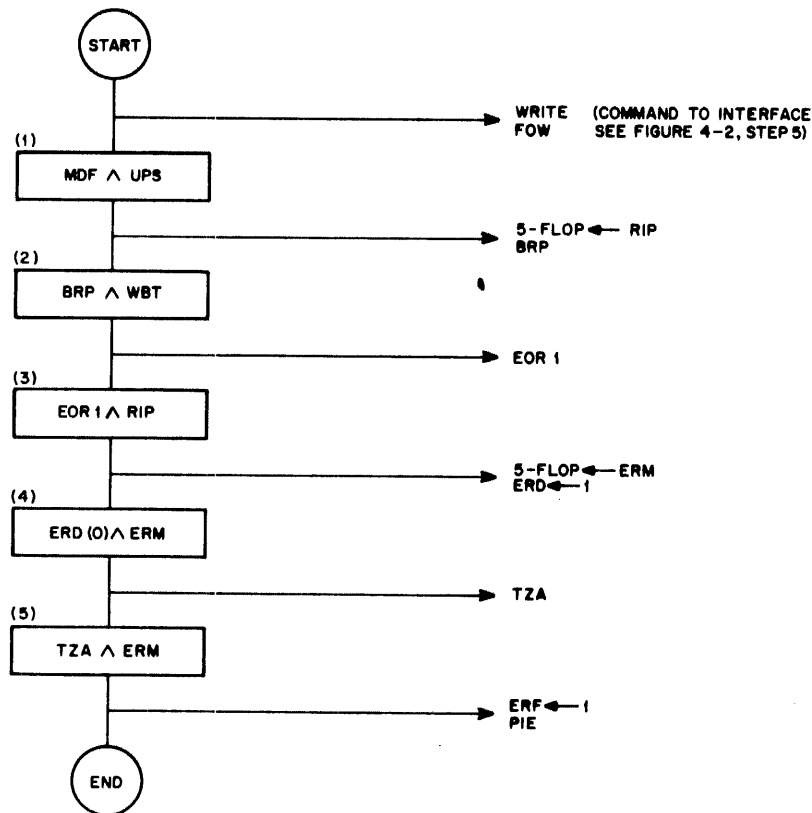## Write (Figure 5-3)

The WRT and FOW levels are applied to the transport interface. During the UPS state of the tape status quint-flop, the transport accelerates the tape. At the end of the UPS state, the quint-flop is advanced to RIP, and a BRP pulse is generated (Figure 5-3, step 1).

The WRT level enables the BRP pulse to set the WES flip-flop (step 2). The first CKP that arrives in time sets the EWC flip-flop to 1 (step 3). The next CKP, and every succeeding CKP that occurs while EWC(1) is still asserted, complements CF. These CKP pulses alternately write the WD output data on tape (step 4) and apply TK/GV LT data request command pulses to the Data Control 136 (step 5).
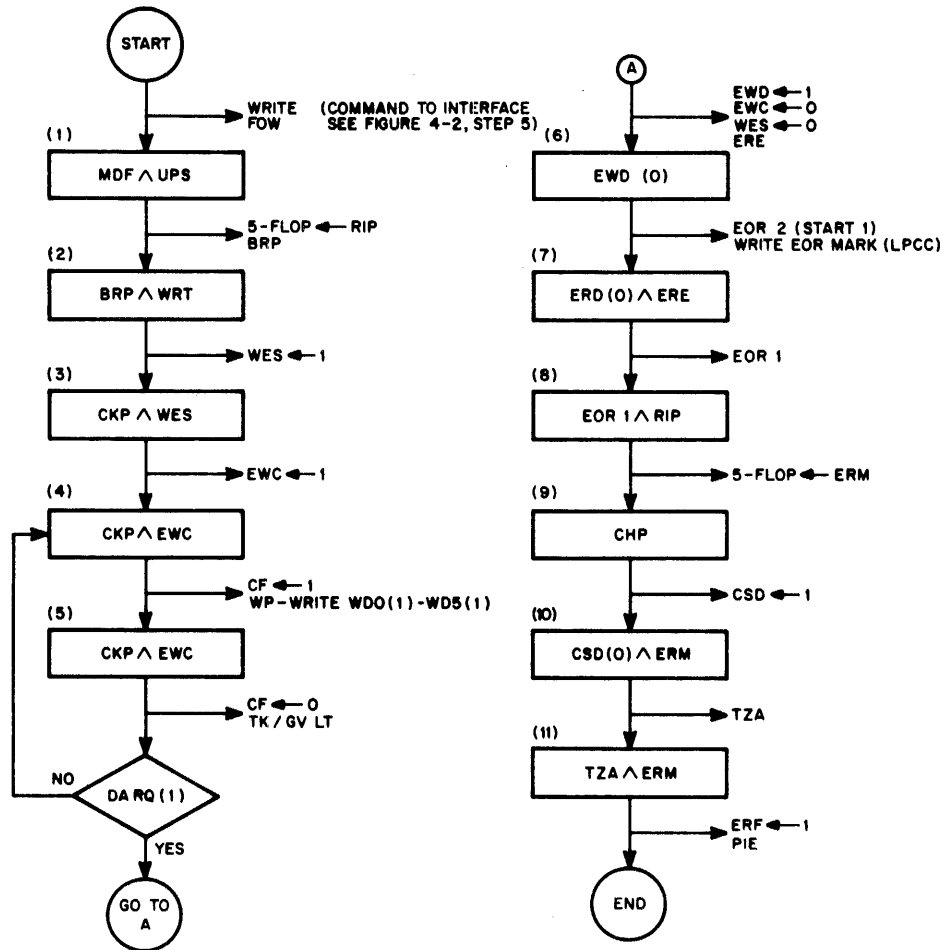
Figure 5-3   Write - WRT

This process continues as long as there is data to be written. When the DA RQ status bit in the Data Control 136 is finally set to 1 (refer to Triggering of EWD, described previously), the end of the current record has been reached and there is no more data to write. The WRT command escapes from the loop represented by steps 4 and 5 of Figure 5-3 and proceeds to execute the remaining operations shown below the DA RQ(1) decision box.

The final TK/GV LT pulse of the record causes the EWD delay to be set to 1. The set of this delay, in turn, resets the EWC and WES flip-flops, signalling that the last data character of the record has been written. The remaining steps of the WRT command (step 6 through 11) are identical to the final steps of the WRF command described under Write File.

# CHAPTER 6

# READ LOGIC

## FUNCTION OF READ LOGIC

The read logic is shown in drawing −RD. It controls the execution of the five read commands: RED, SPF, BER, SPB, and RDC shown on −CM (read forward, space forward, backward read, space backward, and read compare).

The read and space forward commands are almost identical. In both cases, the tape transport reads forward one record while applying the resulting input characters to the tape control. The only difference between the two commands is that TK/GV LT command pulses are applied to the Data Control 136 only for the read command, but not for the space forward. As a result, during the space forward command, the data is never read into the data control accumulator.

The backward read and space backward commands are also almost identical. In both cases, the tape transport reads backward one record while applying the resulting input characters to the tape control. The only difference between the two commands is that TK/GV RT command pulses are applied to the Data Control 136 only for the backward read command, but not for the space backward. As a result, during the space backward command, the data is never read into the data control accumulator.

During the read compare instruction, the tape control compares an output record from the Data Control 136 with an input record read from the tape. The comparison is executed on a character-by-character basis, and at the first discrepancy the RCE flip-flop is set to 1. Whether or not RCE is set in the course of the record, the comparison proceeds until reaching the end of the input record being read from the tape.

## INPUT LEVELS

The pulse $0 \longrightarrow RB$ (−RD:C1) clears the interface read buffer at the beginning and end of each command, preparing it for the 1s transfer of the following character to be read. After a

character has been read from the tape and stored in the read buffer, the read buffer contents are applied to the tape control.

The ground-assertion 1 outputs of the six read buffer data bits RB0-5 are applied to output buffer inverters within the transport interface, and the inverter outputs are, in turn, applied to the tape control as RBB0(1)-RBB5(1) (-RD:C2-3). Negative levels represent 1s in the corresponding read buffer bit positions. The RBB inputs are applied directly to the complement inputs of the LPA to accumulate the longitudinal parity of each of the six data channels (-RD:B2-5).

The RBB levels also provide the input data to the Data Control. For all characters except one, the RBB levels are applied to the data control just as they arrive from the interface reader buffer. The single exception is the Hollerith code 0-character (12 octal). If that character arrives from the transport interface during a BCD parity mode read command, it is always re-converted to 00 octal before being read into the Data Control 136. For further information indicating why this reconversion is required, refer to Chapter 5, WRT and RDC.

## LATERAL PARITY

The tape read parity error level TRPE indicates that a lateral parity error has been detected for the character that has just been read into the read buffer. The TRPE level is sent from the transport interface to the tape control (-RD:B3). Provided that MDC(1) is asserted at RCP time, the tape control sets the parity error flip-flop PER in the transport interface (-RD:B3).

A TRPE level will be produced by an EOR mark with incorrect lateral parity, but the PER flip-flop is only set when the character displaying the lateral parity error is a data character. Consequently, when PER is set to 1, it indicates that a real lateral parity error has been detected. The MCD(1) condition prevents PER from being spuriously set by an EOR mark (which is not re-quired to have correct lateral parity). The MCD delay is described under Miss Character De-tection later in this chapter.

If the file mark is read in binary parity, through a programming error, the PER flip-flop is set to 1. The EFF(1) level causes the PER flip-flop to be reset to 0 at EOR 1, removing this un-wanted parity error indication. The EFF flip-flop is located in the transport interface; its function is to sense the end-of-file character; refer to EFF Set and Reset later in this chapter.

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## CHARACTER SENSING

The purpose of the character sensing logic is to generate a read character present pulse RCP (—RD:B8) whenever a data character has been completely read into the read buffer in the transport interface. This is done in the following manner. The RBCP input signal from the transport interface (—RD:D4) indicates that there is a 1 present in at least one of the five data bits RB0-5 of the interface read buffer. The RBCP level is ORed with the parity bit RB6(1) to produce the character present level CHP. The CHP level is first asserted when the first 1 bit of the current character is read; it terminates when the read buffer is reset.

The commencement of CHP sets the character skew delay CSD (—RD:B7), a 4303 Integrating Single Shot. The CSD provides a sufficient delay to ensure that even a character having the worst permissible degree of skew will have been completely read by the time the delay times out. Any one of three delay resistors can be gated into the CSD circuit; each produces a delay period appropriate for one of the three character densities: D200, D556, or D800.

At the termination of the CSD delay, the single shot output is reset to 0. This reset produces the 0 ——> RB pulse which clears the interface read buffer (—RD:C1). Furthermore, if the tape status quint-flop is in RIP state (indicating that the current character is a data character and not an EOR mark), the reset of CSD also causes the generation of an RCP pulse. The RCP pulse indicates that a data character has been completely read into the interface buffer.

During the read command, the RCP pulse triggers the TK/GV LT command pulse that causes the Data Control 136 to sample the data character in the read buffer (—CS:A6). During the backward read command, the RCP pulse triggers the TK/GV RT pulse (—CS:B4). For the read compare command, the RCP pulse applies the RBB input levels to the LPA and also initiates the triggering of the TZA pulse (—RD:B1).

## MISS CHARACTER DETECTION

The tape control sets the miss character flip-flop MIS (—RD:A6) whenever either one or two data characters have been missed while reading a record or during the read operation that occurs when writing. If three or more characters in succession are missed, the tape control will sense the gap as an end of record. (There is no way of detecting a character or characters that are

missing from the very end of the data record, but this condition is statistically unlikely and not worth the additional circuitry which would be required to detect it.)

The miss character condition is detected by the miss character delay MCD, a 4303 Integrating Single Shot (−RD:C7). While EMC is asserted, the MCD is set at each CHP pulse. Because of the FER(0) condition required to produce EMC, the MCD is set only by data characters and never by the EOR mark (refer to Second Character Detection later in this chapter for further description of the FER flip-flop). The MCD delay is set to time out at an interval of 1.5 character spaces. If no new CHP occurs within the 1.5-character space interval, it is assumed that a character has been missed.

The MCD then resets itself to 0 and sets the MIS flip-flop (−RD:A6). If the MDC reset was a spurious miss character indication caused by the EOR gap, the MIS flip-flop is reset by the EOR 1 pulse. If this is not the case, the next RCP causes the MCS flip-flop (−RD:A7) to be set, indicating that a character (or two characters) have really been missed. The set of MCS confirms the miss character indicating by locking the MIS flip-flop in the 1 state so that it can no longer be reset by the EOR 1 that occurs at the end of the current record.

## READ COMPARISON

The tape control sets the read compare error flip-flop RCE (−RD:B5) to 1 if there is any discrepancy between the output record from the Data Control 136 and the input record from the tape. The actual comparison takes place in the longitudinal parity accumulator LPA (−RD:A2-5) on a character-by-character basis.

The ERC level enables the CSD set (−RD:B2) to generate the read compare strobe pulse RCS. During RDC commands, ERC is asserted throughout the RIP state of the tape status quint-flop (−RD:C5). The ERC level is removed when the quint-flop advances to ERM state to prevent the CSD set corresponding to the EOR mark from producing an RCS. The RCS pulse strobes the write data outputs WD0(1)-WD5(1) into the corresponding LPA flip-flops LPA0-5. The RCS pulse also produces a TK/GV LT pulse which causes the Data Control 136 to advance the next output character into position for read comparison.

When CSD times out and is reset to 0, the resulting RCP applies the RBB0(1)-RBB5(1) input data levels to the complement inputs of the LPA and 1 µsec later generates the TZA pulse (—RD:B8 and B2). The LPA is completely cleared if the WD output character from the data control is identical to the RBB input character from tape. However, if the two characters differ in any bit position, then some bits of LPA are left in the 1 state, and the LPA = 0 level (—RD:D3) is not asserted.

The negation of LPA = 0 enables the TZA pulse to set the RCE flip-flop (—RD:C5). This indicates that the read comparison has failed. After detecting a read compare error, the RCE flip-flop remains in the 1 state until it is reset by the MCL at the beginning of the next command. The LPA is cleared by TZA after each character comparison and is also cleared at the beginning of each command by MCL.

## END OF RECORD

The tape control sets the ERF flip-flop to 1 when the current command has reached the end of the record (—MD:B6). During all commands except RWD, ERF is set by the TZA pulse occurring in the ERM state. When the EFE flip-flop contains 1, ERF(1) is a sufficient condition for generating the priority interrupt enable level PIE (—MD:C7). The MCL pulse resets ERF at the beginning of each command.

## EOR 1 Pulse

The EOR 1 pulse must always be generated before ERF can be set. During forward commands, EOR 1 steps the tape status quint-flop from RIP to ERM, and the ERM level enables TAZ to set ERF.

Pulse amplifier 3D8 generates EOR 1 under three sets of conditions (—RD:C8). For the write blank tape command, an EOR 1 is initiated by BRP at the completion of UPS acceleration state. Should the tape reach load point during an RSB command, an EOR 1 is generated and ERF is set. The third, and most frequent condition for generating the EOR 1 pulse is the reset of the ERD delay in conjunction with the ERE level.

## End of Record Delay and ERE Level

The end of record delay ERD, a 4303 Integrating Single Shot (-RD:C7) is set at each CHP while RIP is asserted. The delay is set to time out an interval equal to 3.5 character spaces at the current character density. If no new CHP occurs within the delay interval, the ERD resets itself to 0, producing an EOR 1 pulse if ERE is asserted. During forward commands, ERD is not set by the EOR mark because RIP is not present at the time the EOR mark is read. During RSB commands, the EOR mark does set ERD, but because ERE is not asserted at the subsequent ERD reset, no EOR 1 pulse is produced.

During RSB commands, the ERE level is not present when the EOR mark is read because the first character detect flip-flop FCD has not yet been set (-RD:A4). There are two other input conditions required for ERE. The RIP condition prevents the generation of an EOR 1 while the ERD delay is timing out to sample LPA parity accumulation. The CHB(0) condition prevents the generation of EOR 1 when a CONO instruction has set the disable-EOR 1 maintenance bit CHB32 to 1. (The tape control then treats the entire tape as essentially a single record.)

## LONGITUDINAL PARITY

In addition to the lateral parity test described previously under Lateral Parity, the tape control also tests for correct longitudinal parity. For all commands except RDC and REW, the longitudinal parity is checked at the end of each record by testing the contents of LPA. Errors are indicated by setting the longitudinal parity error flip-flop LPE to 1 (-RD:B4).

The RBB0(1)-RBB5(1) data input levels are strobed into the complement inputs of the LPA at each RCP pulse and also at the ERD reset corresponding to the EOR mark (-RD:B1). This accumulates the longitudinal parity of each of the six data channels. During either backward or forward commands, the correct longitudinal parity demands an even number of 1 bits in each of the six data channels. If this requirement is met, all six bits of LPA are left cleared at the completion of the record.

The LPE flip-flop is reset by MCL at the beginning of each command. If any bit of LPA contains 1 at the end of the record, a longitudinal parity error is indicated and the LPE flip-flop is set to 1. When the error occurs during an RSB command, LPE is set by diode 3D13; during

forward commands, diode 3D9 sets LPE. For RSB commands, the state of LPA is tested by the EOR 1 pulse that follows the first data character of the record (i.e., the last character to be read). For all forward commands except RDC, the LPA is tested by the TZA pulse that occurs during the ERM state of the tape status quint-flop (the TZA initiated by the EOR 1 pulse and ERD reset).

## END OF FILE

The tape control sets the end-of-file flag EFF in the transport interface whenever a file mark is sensed. Termination of the EOF(0) level ends the SEF level (—CM:D1) and permits the tape control to escape from the space to end-of-file loop; see Chapter 4, Space to End-of-File Command – CON(1) ∧ SEF. The EFF(1) level resets the PER flip-flop at EOR 1, removing the false lateral parity error indication that is generated if the file mark is read in binary parity.

### Second Character Detection

A file mark is always the first and only data character of a file mark record. If a second data character is sensed, the record cannot be a file mark record. The FCD (first character detect) flip-flop (—RD:A7) is set to 1 by the first data character of each record. The SCD (second character detect) flip-flop (—RD:A8) is set by the second data character of each record. This occurs whether the current command is a forward command or a reverse command. However, for RSB commands, the FER flip-flop (—RD:D3) (Figure 3-6:D3) prevents the EOR mark from setting the FCD flip-flop. The FER flip-flop is also used to prevent the assertion of EMC during RSB commands (see previously described Miss Character Detection) to prevent the EOR gap from setting MCD.

### EFF Set and Reset

The interface sends an RBEF level to the tape control whenever a 17 octal character is read. If RB6(0) is also asserted, indicating BCD (even) parity and if the character is the first data character of the current record (SCD = 0), the character is treated as a file mark and an EOF level is generated (—RD:D5). The EOF enables RCP to set EFF (—RD:B2). If additional data characters are in the record, SCD(1) is asserted, and the EFF is reset by the EOR 1 at the end of the record. The EFF is always reset by MCL (STATUS CLEAR) at the beginning of each command.

## READ COMMAND AND SPACE FORWARD COMMAND

The RED and SPF commands (Figure 6-1) are identical except that no TK/GV LT pulses are sent to the DATA Control 136 during the SPF. A FOW level is applied to the transport interface for both commands.

During UPS state, the transport accelerates the tape. At the end of UPS, the tape status quint-flop is advanced to RIP state; see Figure 6-1, step 1. As each data character is sensed, CHP sets the three read logic delays CSD, MCD, and ERD (step 2). The expiration of CSD produces an RCP after each character has been read completely (step 3). During the RED command, but not the SPF, each RCP produces a TK/GV LT pulse. Each of these TK/GV LT pulses causes the Data Control 136 to strobe the character currently being read into the six low-order bits of its data accumulator (at the same time, the accumulator is shifted left six bit-positions). The CSD reset also produces the 0 ——> RB pulse to clear the read buffer in the transport interface.

The RCP that is produced by the first data character of the record sets the first character detect flip-flop FCD (step 4). The next RCP sets the second character detect flip-flop SCD (step 5). The tape control then continues to cycle through the loop containing steps 2 and 3 until reaching the EOR gap at the end of the record. At the EOR gap, the MCD delay times out and then the ERD delay times out. The MCD reset causes the MIS flip-flop to be set to 1. The ERD reset produces an EOR 1 pulse. This EOR 1 pulse resets MIS, and steps the tape-status quint-flop from RIP to ERM state (step 6). EOR 1 resets the ERD delay that remains set while the EOR mark is read.

The CHP produced by the EOR mark does not set CSD to 1 (step 7). Instead, the ERD acts as a skew delay while the EOR mark is accumulated. One μsec after the ERD times out and is reset, a TZA pulse is generated (step 8). If a longitudinal parity error has occurred during the command, this TZA sets the LPE flip-flop to 1. Because the quint-flop is in ERM state, the same TZA pulse sets the end-of-record flag ERF (−MD:B6). Provided that the EFE flip-flop contains 1, the ERF set produces a priority interrupt enable signal PIE (Figure 6-1, step 9). The remainder of the command cycle is shown in Figure 3-2, steps 13, etc.
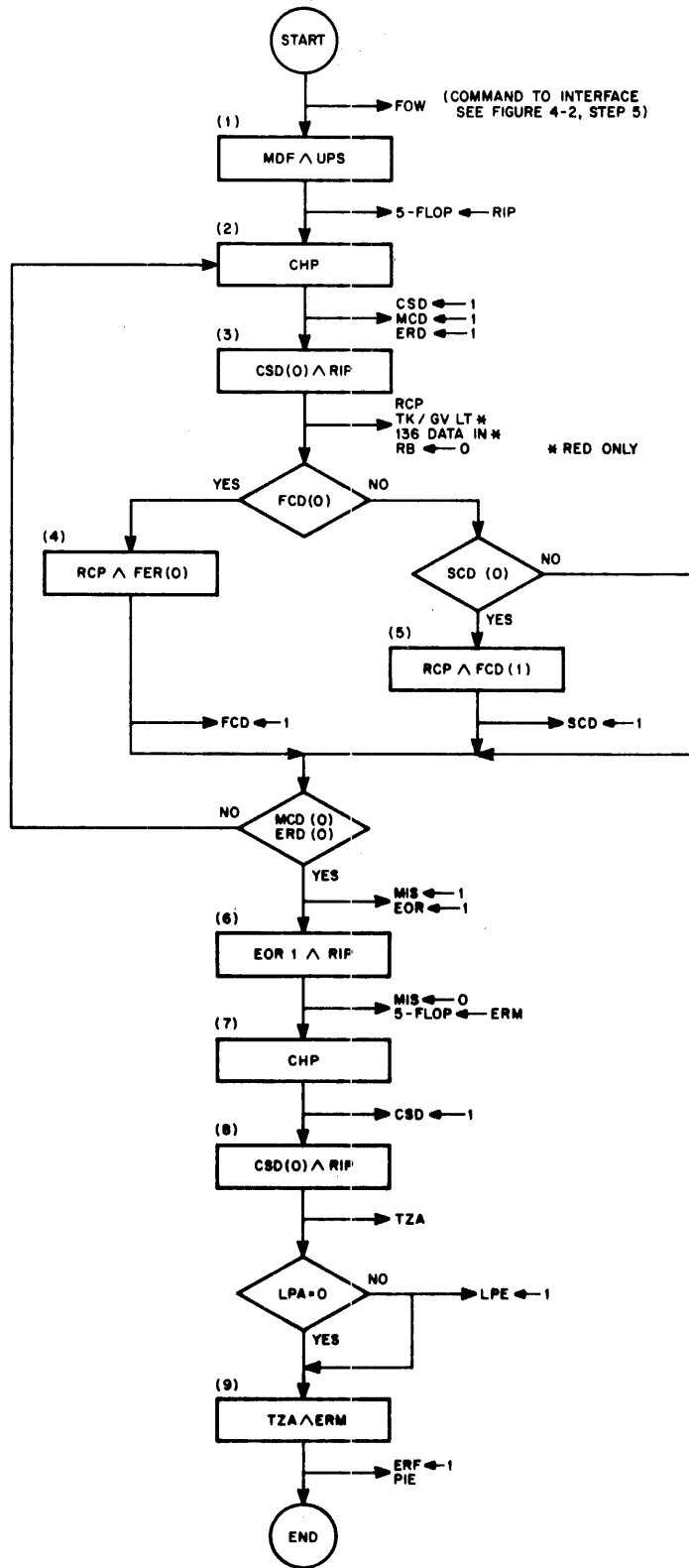
Figure 6-1   Read (RED) and Space Forward (SPF)

## BACKWARD READ COMMAND AND SPACE BACKWARD COMMAND

The BER and SPB commands (Figure 6-2) are identical except that no 0 $\longrightarrow$ CCT pulse and no TK/GV RT pulses are sent to the Data Control 136 during the SPB. A BAC level is applied to the transport interface for both commands.

During UPS state, the transport accelerates the tape. At the end of UPS, the tape status quint-flop is advanced to RIP state, and a BRP pulse is generated, setting the false end of record flip-flop FER; see Figure 6-2, step 1. The first character that is sensed during the BER and SPB commands is not a data character, but the EOR mark. The CHP generated by the EOR mark sets the CSD and ERD delays, but not the MCD delay (step 2).

The expiration of CSD produces an RCP (step 3). The RCP resets the FER flip-flop and causes EMC to be asserted. Assertion of the EMC level permits the MCD delay to be set by all sub-sequent data characters of the record. During the BER command, each RCP, including the EOR mark RCP, produces a TK/GV RT pulse. The CSD reset also produces the 0 $\longrightarrow$ RB pulse to clear the interface read buffer.

After reading the EOR mark, the transport read heads traverse the EOR gap. The ERD delay times out; but because the FCD flip-flop contains 0, ERE is not asserted, and no EOR 1 pulse is produced. The reset of ERD does produce a 0 $\longrightarrow$ CCT pulse (−CS:B5) during the BER com-mand (Figure 6-2, step 4). This pulse prevents the Data Control 136 from treating the EOR mark as data.

The first data character to be read is the last character of the record. The CHP produced by this character sets all three of the read logic delays CSD, MCD, and ERD (step 5). The expi-ration of the CSD produces an RCP after each character has been completely read (step 6). During the BER command, but not the SPB, each RCP produces a TK/GV RT pulse that causes the Data Control 136 to strobe the character currently being read into the six high-order bits of its data accumulator (at the same time the accumulator is shifted right six bit-positions). The CSD reset also produces the 0 $\longrightarrow$ RB pulse to clear the interface read buffer.

The RCP that is produced by the last data character of the record (the first character to be read during a BER or SPB command) sets the FCD (step 7). The next RCP sets the SCD (step 8).

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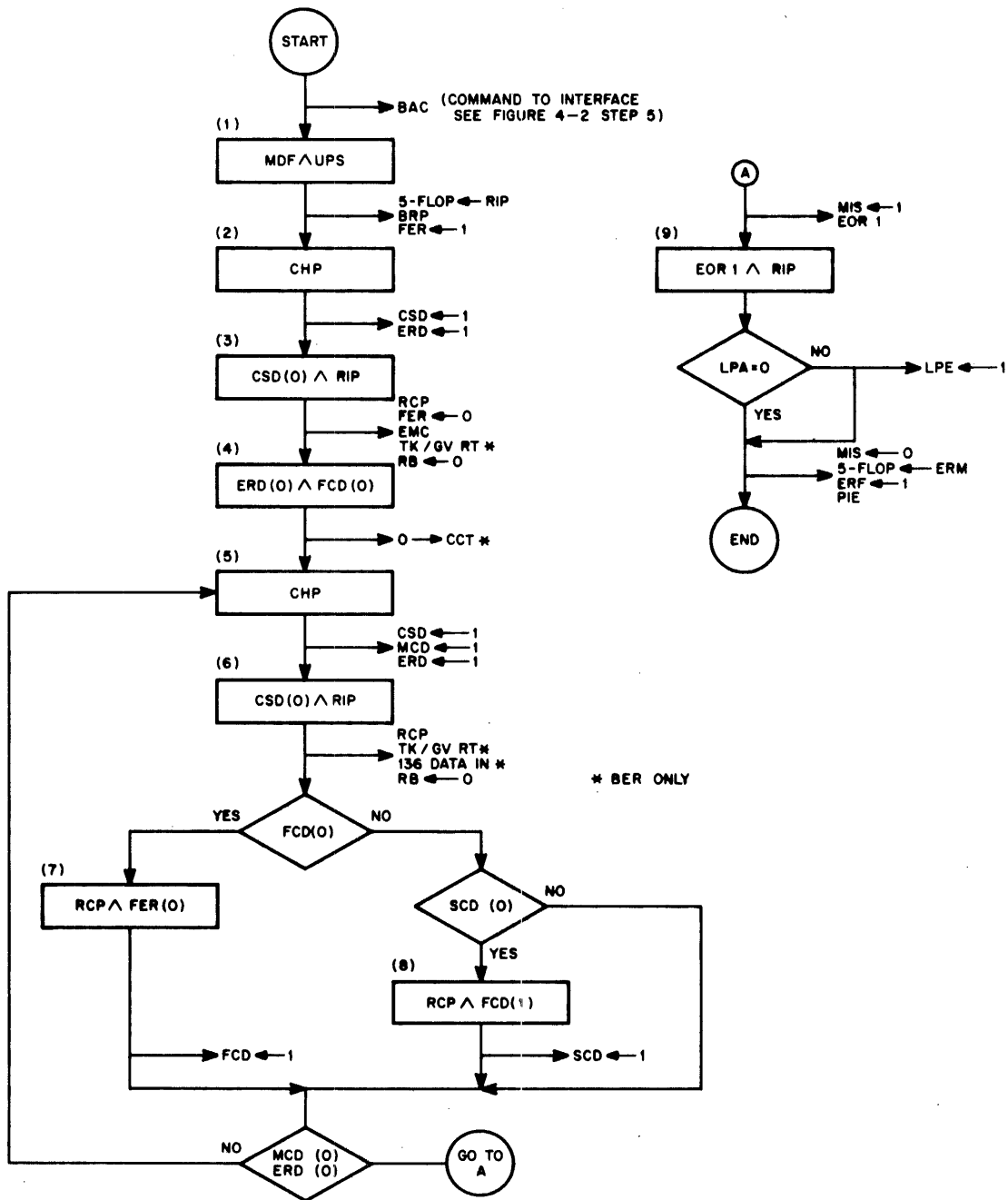
Figure 6-2 Backward Read (BER) and Space Forward (SPF)

The tape control then continues to cycle through the loop containing steps 5 and 6 until reaching the beginning of the record. After the first character of the record is read, the tape continues backward into the record gap (not the EOR gap; that is traversed at the beginning of the command).

At the record gap, the MCD delay times out and the ERD delay times out. The MCD reset causes the MIS flip-flop to be set to 1. The ERD reset produces an EOR 1 pulse. This EOR 1 pulse resets MIS, steps the tape status quint-flop from RIP to ERM state, and resets ERD. Thus, the ERF flip-flop is set seven character times after reading the last character during RSB or 3.5 character times after EOR 1. Provided that the EFE flip-flop contains 1, the ERF set produces a priority interrupt enable signal PIE (Figure 6-2, step 11). Likewise, if a longitudinal parity error has occurred during the command, the LPE flip-flop will be set when ERF is set. The remainder of the command cycle is shown in Figure 3-2, steps 13, etc.

## READ COMPARE COMMAND

A FOW level is applied to the transport interface for the RDC command (Figure 6-3). During UPS state, the transport accelerates the tape. At the end of UPS, the tape status quint-flop is advanced to RIP state and ERC is asserted; see Figure 6-3, step 1. As each data character is read, CHP sets the three read logic delays CSD, MCD, and ERD (step 2). The set of CSD produces an RCS pulse that transfers the WD outputs into LPA0-5 and generates a TK/GV LT pulse (step 3). By shifting the data control accumulator left six bit-positions, the TK/GV LT brings the next output character into position to be sampled by the tape control.

When the CSD delay times out, an RCP pulse is generated, applying the RBB input levels to the complement inputs of the LPA (step 4). The resulting data in LPA is the exclusive OR of the WD outputs and the corresponding RBB inputs; i.e., each bit of LPA contains the WD output or its complement, depending upon whether the RBB input level represents a 0 bit or a 1. One μsec after the RCP, a TZA pulse is generated, testing the state of LPA and simultaneously clearing LPA. If the LPA contains any 1 bits, the read compare error flip-flop RCE is set to 1.

The tape control continues to cycle through the loop containing steps 2 through 5 until reaching the EOR gap at the end of the record. At the EOR gap, the MCD delay times out and then
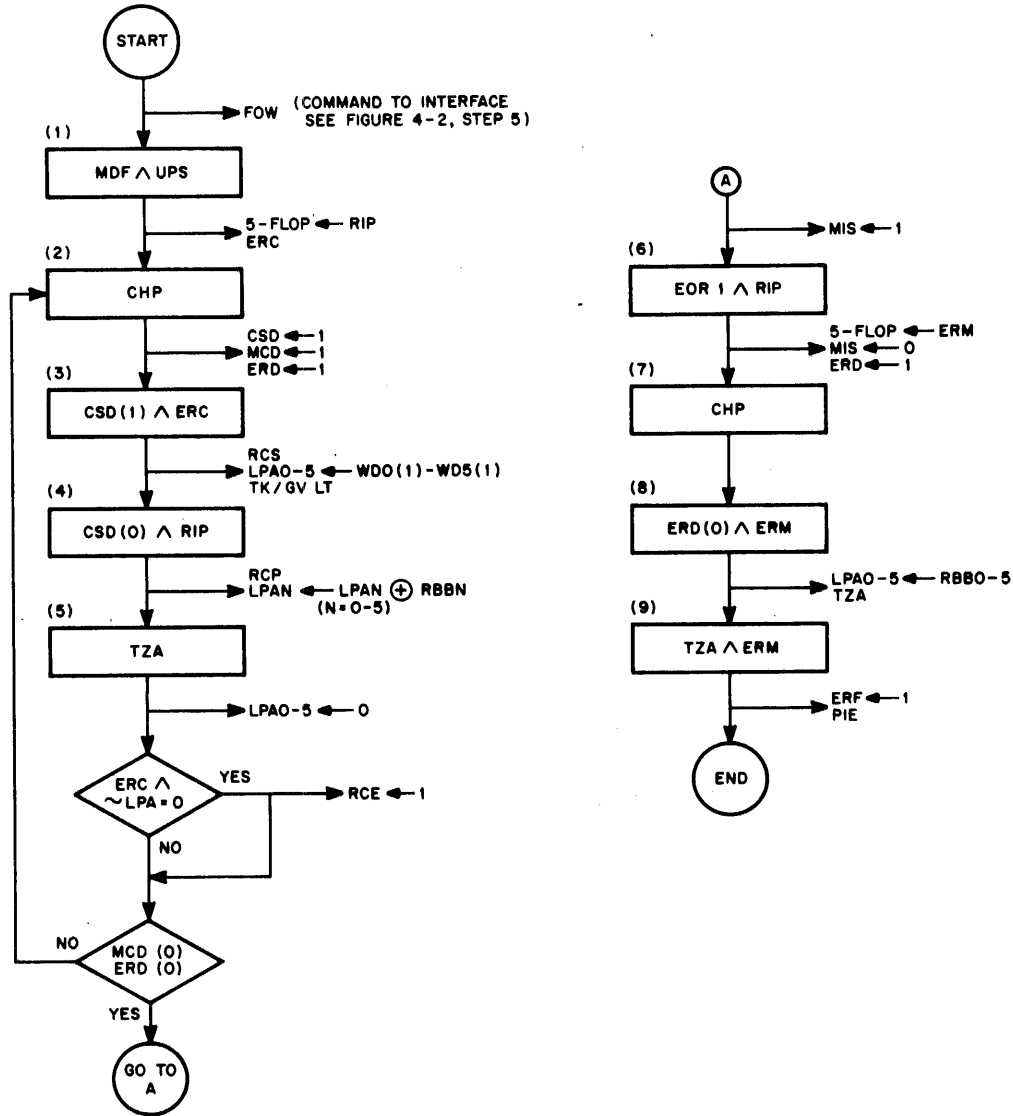
Figure 6-3 Read Compare (RDC)

the ERD delay times out. The MCD reset causes the MIS flip-flop to be set to 1. The ERD re-set produces an EOR 1 pulse. This EOR 1 pulse resets MIS and steps the tape status quint-flop from RIP to ERM state (step 6). EOR 1 resets the ERD delay that remains set while the EOR mark is read.

The CHP produced by the EOR mark does not set the CSD to 1 (step 7). The subsequent reset of ERD (step 8) causes the EOR mark to be applied to the complement inputs of LPA0-5, and 1 µsec later produces a TZA pulse. However, because ERC is no longer asserted after the

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quint-flop enters ERM state, this TZA pulse has no effect on the state of the RCE flip-flop. The transfer of the EOR mark into the LPA is, therefore, harmless for the RDC command. (Moreover, LPA is cleared by MCL at the beginning of the subsequent command.) The TZA pulse produced by the reset of ERD sets the end of record flag ERF (—MD:B6). Provided that the EFE flip-flop contains 1, the ERF set produces a priority interrupt enable signal PIE (Figure 6-3, step 9). The remainder of the RDC command cycle is shown in Figure 3-2, steps 13, etc.

# CHAPTER 7

# TAPE CONTROL INTERFACE 520

The 520 Interface permits the Magnetic Tape Control 516 to control up to eight DEC Tape Transports Type 50. The interface contains write and read buffers, write and read parity networks, and associated logic. The end-of-file flag and lateral-parity-error flag are also located in the interface, as are the drivers that amplify command and selection levels from the tape control and apply these levels to the tape transports.

## SELECTION AND COMMAND INPUTS

Eight unit selection levels UNIT 0-UNIT 7 are also applied to the interface from the tape control (BS-D-520...:D1). The selection level corresponding to the selected tape transport is asserted at ground; the other seven levels remain negative. All eight levels are amplified by 1684 Bus Drivers before being applied to the transports at T UN 0-7. The tape control always selects a transport before applying any command levels to the interface. One of the eight unit selection levels is grounded at the tape control JNU pulse; the command levels are not applied to the interface until the tape control generates a JNC pulse.

Four input command levels are applied to the interface from the tape control: WRITE, FOW, BAC, and REW (-520...:C1). The WRITE level is asserted at ground; the remaining three levels are negatively asserted. The WRITE level is amplified by a 1684 Bus Driver and applied to the tape transport as T WRITE. This signal sets the transport to write status by enabling both the write logic and the read logic. (The capacitor from T WRITE to ground is used to prevent switching noise from reaching the transport.) The WRITE level is also inverted and amplified by a 1690 Inverting Bus Driver, and the resulting signal is applied to the tape transport as T READ. Unless REW is also asserted, the T READ signal sets the transport into the read status, disabling the write logic and enabling the read logic.

The FOW, BAC, and REW levels are inverted and amplified by 1690 Inverting Bus Drivers, and the resulting ground assertion signals are applied to the tape transport as T FOW, T REV, and T REW. The T FOW signal causes the transport to begin forward tape motion; T REV starts

reverse tape motion at normal reading speed; the T REW signal causes the transport to reverse at rewind speed (approximately twice the normal reading speed). The read amplifiers are not enabled during rewind.

## WRITE LOGIC

The write logic accepts the write data outputs from the tape control, generates a lateral parity bit, and complements those bits of the write buffer that correspond to 1 bits of the character being written. Both outputs of each WB flip-flop are applied to the transport write logic.

### Write Data Outputs

During WRT and WRF commands, the six write data outputs WD0-WD5 apply output data characters from the tape control to the interface (-520...:B1-3). Ground levels correspond to 1 bits. The WD levels determine which of the data flip-flops in the write buffer are to be complemented at the write pulse. Both polarities of the six WD outputs are applied to the write parity network. The parity network then generates a seventh level which determines whether or not the write buffer parity flip-flop is to be complemented at the write pulse.

### Write Parity Net

As each 6-bit output character is transferred out to the interface by the WD outputs, the write parity net (-520:B and C4-7) generates an accompanying parity bit. If CB21 (in the tape control command buffer) contains 0, the writing is to be done in BCD (even) parity. The 0 state of CB21 causes a negative PAR 0 input to be applied to the write parity net (-520...:C7). This input causes the net to generate a negative WPAR 1 output if an odd number of the six WD outputs are 1s. The transport then writes a 1 bit in the parity channel for the current character, yielding a character with an even number of 1 bits. If CB21 contains a 1, the writing is to be done in binary (odd) parity. A ground PAR 0 input is then applied to the parity net, and the WPAR 1 output is generated only if an even number of the six WD outputs are 1s.

The write parity net is composed of a 3-stage, 7-input exclusive OR circuit. All of the WD inputs are negative assertion levels. The WPAR 1 output is asserted only if an odd number of the seven inputs are 1 (counting the six WD bits and the contents of CB21). The assertion levels

shown in the two upper stages of the net assume further that the PAR 0 input is asserted negative (i.e. that CB21 is 0, indicating BCD parity). In inverter 3B13, three external 3.3K resistors have been substituted for the normal 1.5K load resistors. This reduces the current through the lower legs of the parity net and avoids excessive loading.

The WEF command level is inverted in the tape control (-CM:C4) and applied to the write parity net as $\overline{\text{WRITE EOF}}$; (-520...:B5). When this level is negative (as it is for write file commands), diode 3B8 holds the WPAR output at ground, inhibiting the generation of a 1 parity bit. The end-of-file character 001 111 (17 octal) should always be written in BCD parity (with a 0 parity bit). The $\overline{\text{WRITE EOF}}$ input ensures that the write parity net produces the correct 0 parity bit for the EOF character even if the programmer should inadvertently give a WRF command with binary parity.

## Write Buffer

The write buffer (-520...:A1-4) is composed of seven 500-kc flip-flops. Both outputs of each flip-flop are amplified by 1684 Bus Drivers and applied to the transport write amplifiers. Depending on the state of the associated WB flip-flop, each write amplifier drives one or the other of two oppositely-wound write-head coils. Each transition of a WB flip-flop terminates the current through one coil, and starts it in the other, changing the sense of tape magnetization, and writing a 1 in the corresponding tape channel. The T-3 driver-power control level (-520:A1) permits switching in resistors to −15 vdc to augment the bus driver power. At present, this feature is not used.

## WB Complement

The data bits WB0-5 are complemented whenever the associated WD outputs are in the 1 state at the write pulse WP. The parity bit WB6 is complemented if the write parity level WPAR 1 is asserted at WP. When a given WD output is in the 1 state, a ground level is applied to the associated input terminal, and inverted (-520...:B1-3).

For WD0-4, the resulting negative level enables Capacitor-Diode 4127 to produce a positive output pulse at the arrival of the WP. This pulse complements the corresponding WB flip-flop

WB0-4. The complement inputs applied to WB5 and WB6 use 4113 Diodes instead of capacitor-diodes, but the result is logically identical. Data bit WB5 is complemented only when WD5 is a 1, and the parity bit WB6 is complemented only when the WPAR 1 level represents a 1 parity bit.

## WB Clear

The START 1 input to the interface (-520...:A1) originates in the tape control as the EOR 2 pulse. This pulse clears all seven WB flip-flops each time it is applied to the interface. A START 1 is produced at the beginning of every command to ensure that every record begins with WB0-6 cleared.

Another START 1 is applied to the interface four to five character spaces after the last data character of each record is written on tape (4 spaces during WRF records, and 4.5 spaces + 2.4 μsec during WRT records). The resulting WB clear produces the EOR mark at the end of the record. The clear complements just those WB flip-flops that are left in the 1 state after the final data character of the record; i.e., those flip-flops that have already been complemented an odd number of times in the course of the record. This yields an even longitudinal parity for each of the seven channels in the record, and thus permits the EOR mark to be used as a longitudinal parity check character. (Only the six data channels are actually checked for longitudinal parity.)

## READ LOGIC

The read logic accepts seven transport signals corresponding to each input data character, assembles the input character in the read buffer, tests it for the correct lateral parity, and applies it to the data control (via the tape control).

## Read Buffer

The read buffer (-520:A4-7) is composed of seven 500-kc flip-flops; six data flip-flops RB0-5 and a lateral parity flip-flop RB6. Each of the RB flip-flops is set to 1 at the peak of every transport input signal on the corresponding read channel. The ground assertion 1 outputs of the six RB data flip-flops are applied to output buffer inverters within the interface, and the inverter outputs are, in turn, applied to the tape control as RBB0(1)-RBB5(1). Negative levels

represent 1s in the corresponding read buffer bit positions. The negative assertion 1 output of the RB parity flip-flop RB6(1) is applied to the tape control directly without inversion.

## RB Clear

The read buffer is cleared by the 0 ——> RB pulse from the tape control. This clear occurs at the beginning of each command to ensure that the buffer starts reading in the correct initial condition. It also occurs after each character is read to prepare the read buffer for the 1s transfer of the next character. The latter clear occurs at CSD(0), the end of the character skew delay. At that time, the current character has been fully entered into the read buffer. The contents of the buffer are sampled at the same time that the buffer is cleared.

## RB Set

At successive changes of tape magnetization, the differential amplifier at each of the transport read heads produces output signals of alternating polarity (the polarity of each signal depending on the sign of the change). Before being applied to the interface, the bipolar output signal for each of the seven tape channels is passed through a rectifying slicer in the transport. The slicer rectifies the output of the differential amplifier and produces a positive output pulse at each input of either polarity. However, no slicer output is generated unless the input exceeds a preset level. (This is to prevent low-level noise inputs from producing spurious output pulses.)

The negative output pulses from each of the seven transport channels are applied to a 1539 Peak Detector and Slicer circuit in the interface (-50:B4-7). When pulsed by an output from the rectifying slicer, each 1539 Peak Detector-Slicer generates two outputs, a negative level, and a negative pulse. The level and pulse are both applied to a 4127 Negative Capacitor-Diode Gate. The capacitor-diode then applies a positive output pulse to the complement input of the corresponding RB flip-flop (setting it to the 1 state, because it was cleared at the preceding 0 ——> RB pulse). The negative enable level is produced by the 1539 Circuit as long as the driving pulse from the transport is above a minimal amplitude. The pulse output of the 1539 coincides with the peak of the input signal.

Therefore, as each character is read by the transport, each of the seven RB flip-flops RB0-6 is set to 1 if there is a change in the magnetization of the corresponding tape channel. Since neither the write heads nor the read heads are ever aligned exactly, there is a finite time dispersion between the peaks of the 1 signals from different channels. The tape control character skew delay CSD is calculated to provide enough delay so that each character is fully entered into the read buffer before the buffer is sampled and cleared.

## RBCP and RBEF

The RBCP level (read buffer character present) is asserted whenever any of the six read buffer data bits RB0-5 contain 1 (-520:C3). This level is sent to the tape control where it is ORed with RB6(1) to produce the CHP (character present) signal.

The RBEF read buffer end-of-file level (-520:C3) is asserted and applied to the tape control when the six data bits of the read buffer RB contain the file mark character (17 octal).

## End-of-File Flag

The EFF flip-flop (-520:A7) is set to 1 to indicate that a file mark has been sensed. Although the EFF flip-flop is physically located in the interface, the signals controlling its set and reset originate in the tape control. The interface sends an RBEF level to the tape control whenever a file-mark character (17 octal) is read. If BR6(0) is also asserted, indicating BCD parity, and the character is the first data character of the current record, the EOF level is asserted, and the character is treated as a file mark.

At the RCP pulse (which coincides with the end of the CSD delay), the tape control applies a 1 $\longrightarrow$ EFF ground pulse to interface input terminal 3B81M, setting EFF. If additional data characters are in the current record, the file mark indication is assumed to be the result of a programming error, and EFF is reset at the EOR 1 pulse that ends the record. The tape control accomplishes this reset by applying a 0 $\longrightarrow$ EFF ground pulse to interface input terminal 3B88K. The EFF is also reset at the beginning of each command by STATUS CLEAR (designated MCL within the tape control).

## Read Parity Net

As each input character is read into the read buffer RB0-6, the read parity net (-520:C and D4-8), checks the character for correct lateral parity. If the parity is not correct, a negative TRPE (tape read parity error) level is sent to the tape control.

The read parity circuit is virtually identical to the write parity net described previously under Write Parity Net, except that it contains one extra leg. Both the PAR 0 and PAR 1 outputs of the CB21 flip-flop are used as inputs to the read parity net. When binary (odd) parity is specified, the PAR 1 level is negatively asserted; and when BCD parity is specified, PAR 0 is negatively asserted. The RB inputs are also negative assertion levels. A parity error TRPE is asserted when PAR 0 is asserted and an odd number of the seven RB bits RB0-6 contain 1s; TRPE is also asserted when PAR 1 is asserted and an even number of the RB bits contain 1s.

## Parity Error Flip-Flop

The parity error flip-flop PER (-520:A8) is set to 1 to indicate that a lateral parity error has occurred. The PER flip-flop is physically located in the interface, but the signals controlling its set and reset originate in the tape control. The interface sends a TRPE level to the tape control whenever the character currently being read displays an apparent parity error. If the character is a data character rather than an EOR mark, the tape control sets the parity error flip-flop by applying a ground pulse to interface input terminal 3B81N. However, if the character displaying the apparent parity error is an EOR mark, MCD(1) is not asserted at RCP time, and the parity error flip-flop is not set. (The EOR mark serves as the longitudinal parity check character and may or may not have correct lateral parity. For this reason, it is necessary to prevent any TRPE signals that are produced by EOR marks from setting the PER flip-flop.)

If the EFF is set to 1, it causes the PER flip-flop to be reset to 0 at EOR 1. This removes the false parity error that would appear if the file mark were read in binary parity through a programming error. The PER is also reset at the beginning of each command by STATUS CLEAR (designated MCL within the tape control).

# CHAPTER 8

# TAPE CONTROL INTERFACE 521

The 521 Interface permits the Magnetic Tape Control 516 to control up to eight DEC Tape Trans-
ports, Type 570. The interface contains a read buffer, write and read parity networks, and
associated logic. The end-of-file flag and lateral-parity-error flag are also located in the
interface, as are various control circuits that process command and selection levels from the
tape control and apply these levels to the tape transports.

## SELECTION AND COMMAND INPUTS

The selection and command inputs select a specific tape transport for the current command and
apply appropriate command levels and pulses to that transport.

### Selection Inputs

Eight unit selection levels UNIT 0-7 are applied to the interface from the tape control (-521:D1).
The selection level corresponding to the selected tape transport is negatively asserted; the
other seven levels remain at ground. All eight levels are sent through buffer inverters before
being applied to the transports as T UNIT 0-7.

The tape control always selects a transport before applying any command levels to the interface.
At the tape control JNU pulse, one of the eight unit selection levels becomes negative. The
JNU pulse is applied to the interface as AC1 $\longrightarrow$ UN (-521:A1). That pulse is delayed 1 μsec
by pulse amplifier 3B25 and amplified by pulse amplifier 3B24 and applied to the transports as
UNIT STROBE. The UNIT STROBE pulse selects the transport specified by the asserted unit
selection level. The command levels are not applied to the interface until the tape control
JNC pulse.

### Command Inputs

Three input command levels are applied to the interface from the tape control: REWIND,
WRITE, and FOW (-521:C1). These inputs, together with the CON 1 level (from CB24 in the

tape control command buffer) determine the type of operation the transport is to commence when it receives a start pulse from the tape control. The WRITE level is asserted at ground; the other two command levels and the CON 1 level are negatively asserted.

The WRITE level is inverted and amplified by a 1690 Inverting Bus Driver, and the resulting signal is applied to the tape transport as T WRITE/READ. A negative T WRITE/READ sets the transport to write status by enabling both the write logic and the read logic. A ground T WRITE/READ prevents the write logic from being enabled. (The capacitors from T WRITE/READ and from T REW to ground are used to prevent switching noise from reaching the transport.)

The FOW level is also inverted and amplified by a 1690 Inverting Bus Driver, and the resulting signal is applied to the tape transport as T FOW/REV. At ground, that signal causes the transport to begin forward tape motion when the start pulse arrives; when negative, the signal calls for reverse tape motion at normal reading speed.

The REW level is amplified by a 1684 Bus Driver and applied to the transport as T REW. That signal causes the transport to reverse at rewind speed (about twice normal reading speed) when the start signal is given. If CB24 (in the tape control command buffer) contains 0, the transport rewinds only as far as the tape load point and stops. However, if CB24 contains 1, a rewind unload command is specified, and the entire tape is rewound. The REWIND COMMAND level and CON 1 (the negative assertion 1 output of CB24) are ANDed and amplified by diode 3B13 and inverter bus driver 3B21 and applied to the transport as T REW/UNLOAD (-521:D3 and C2).

## OTHER CONTROL FUNCTIONS

The present paragraph describes the start sequence, the process of reserving a transport or releasing it to pool (when operating in multicontrol mode), and the use of the T A/B signal.

The tape control CTT pulse is sent to the transport interface as IOT 7104, and returns from the interface to the tape control designated START 2 (-521:C5). If the tape control command buffer bits CB25-27 are all 0, specifying no operation (NOP), the IOT 7104 pulse has no effect on the interface or transports. However, if CB25-27 are nonzero, indicating that the current command calls for tape motion, the $\overline{\text{NOP}}$ level is asserted negative, and the IOT 7104 pulse sets the GO flip-flop.

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The ground assertion 1 output of GO is inverted and amplified by a 1690 Inverting Bus Driver and applied to the transports as T GO. It causes the selected transport to begin the mode of tape motion specified by the command levels (FOW, REV, or REW). The GO flip-flop remains set until the tape control command buffer is cleared by the CCB pulse. The CCB is sent to the interface as $0 \longrightarrow CM$. It clears GO and terminates T GO. The ground assertion 1 output of the GO flip-flop is also used to enable the peak detectors in the read buffer set logic.

## Pool

The 521 Interface and the associated 570 Transports can be operated in multicontrol mode. This means that the same transports can be used by two tape control units (each tape control having its own associated interface). There is a 3-state device in each transport which reflects transport status (A, B, or POOL). These transport-status conditions mean that the transport is currently reserved by the A tape control, that it is reserved by the B tape control, or that it is in the POOL condition (free to be selected).

If CB28 (in the tape control command buffer) contains 1, the transport is to be kept reserved after the completion of the current command. However, if CB28 contains 0, POOL 0 is asserted (-521:B1), and the transport is returned to pool at the conclusion of the current command. The reset of the GO flip-flop causes pulse amplifier 3B24 to generate a RETURN TO POOL pulse at output terminal P. The POWER CLEAR pulse (designated IOB RESET in the 516 Tape Control) also generates a RETURN TO POOL pulse. POWER CLEAR is applied directly to input terminal M of pulse amplifier 3B24; input terminal N is unused.

## T A/B Select

If the current command selects a transport that is already reserved by the other control (the A or B control as the case may be), the reserved transport returns a T A/B signal to the interface (-521:D3). From the interface, the T A/B signal is routed to two places in the tape control. Designated BCT, it is applied via interface output terminal 3B95C to the tape control illegal command logic (-CS:A2). With the designation A/B, it is also sent through terminal 3B88R to the tape control status logic (-ST:B4).

# WRITE LOGIC

The write logic amplifies the write data outputs and write pulses from the tape control and applies them to the write buffer in the transport. The write logic also generates the lateral parity bit and the WRITE RESET level.

## Write Data Outputs

During WRT and WRF commands, the six write data outputs WD0-WD5 apply output data characters from the tape control to the interface (-521:B1-4). Ground levels correspond to 1 bits. The WD levels determine which of the data flip-flops in the transport write buffer are to be complemented at the write pulse. Both polarities of the six WD outputs are applied to the write parity network. The parity network then generates a seventh level which determines whether or not the write buffer parity flip-flop is to be complemented at the write pulse.

## Write Buffer

The write buffer is a 7-bit flip-flop register in the transport logic. Both outputs of each flip-flop are applied to the transport write amplifiers. Depending on the state of the associated write buffer flip-flop, each write amplifier drives one of two oppositely wound write head coils. Each transition of a write buffer flip-flop terminates the current through one coil and starts it in the other, changing the state of tape magnetization and writing a 1 in the corresponding tape channel.

## Write Parity Net

As each 6-bit output character is transferred out to the interface by the WD outputs, the write parity net (521-:B and C1-5) generates an accompanying parity bit. If CB21 (in the tape control command buffer) contains 0, the writing is to be done in BCD (even) parity. The 0 state of CB21 causes a negative PAR 0 input to be applied to the write parity net (-521:C5). This input causes the parity net to generate a 1 parity output (a negative level) if an odd number of the six WD outputs are 1s. The negative parity 1 level is amplified by a 1684 Bus Driver and applied to the transport write buffer via interface output terminal P4-13. The transport then writes a 1 bit in the parity channel for the current character, yielding a character with an even

number of 1 bits. If CB21 contains a 1, the writing is to be done in binary (odd) parity. A ground PAR 0 input is then applied to the parity net, and the 1 parity output is generated only if an even number of the six WD outputs are 1s.

The write parity net is composed of a 3-stage, 7-input exclusive OR circuit. All of the WD inputs are negative assertion levels. The 1 parity output level is asserted negative only if an odd number of the seven inputs are 1 (counting the six WD bits and the contents of CB21). The assertion levels shown in the two upper stages of the net assume that each of the three pairs of WD bits includes a 1 bit and a 0 bit and assumes that the PAR 0 input is negative (i.e. that CB21 is 0, indicating BCD parity). In inverter 3B17, three external 3.3K resistors have been substituted for the normal 1.5K load resistors. This reduces the current through the lower legs of the parity net and avoids excessive loading.

The WEF command level is inverted in the tape control (Figure 3-1C4) and applied to the write parity net as $\overline{\text{WRITE EOF}}$ (-521:B2). When this level is negative (as it is for write file commands), diode 3B12 holds the parity net output at ground, inhibiting the generation of a 1 parity bit. The end-of-file character 001 111 (17 octal) should always be written in BCD parity (with a 0 parity bit). The $\overline{\text{WRITE EOF}}$ input ensures that the write parity net produces the correct 0 parity bit for the EOF character even if the programmer should inadvertently give a WRF command with binary parity.

### Write Reset Flip-Flop

The write reset flip-flop (-521:C3) governs the state of the WRITE RESET output to the transports. Until the write reset flip-flop is set to 1 (grounding WRITE RESET), the transport write buffer flip-flops cannot be complemented. When the write reset flip-flop is reset to 0, the resulting drop in the WRITE RESET level clears the write buffer.

The write reset flip-flop is set to 1 at the first WP write pulse of the record, causing the WRITE RESET level to rise to ground and permitting the write buffer flip-flops to be complemented. All WP pulses are delayed 1 μsec at pulse amplifier 3B25 (-521:C2) before being applied to the transport as WP1 pulses. This gives the WRITE RESET level time to rise to ground before the first WP pulse is applied to the transport write buffer.

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The write reset flip-flop is reset at each START 1 pulse. The START 1 pulse originates in the 516 Tape Control as EOR 2. A START 1 is produced at the beginning of each command to ensure that every record begins with the write reset flip-flop and the write buffer cleared. Another START 1 is applied to the interface four to five character spaces after the last WP pulse of each record (4 spaces during WRF records, and 4.5 spaces + 2.4 $\mu$sec during WRT records). The resulting clear of the write reset flip-flop causes the WRITE RESET output to drop to a negative level and clears the transport write buffer. The clear complements the write buffer flip-flops that are left in the 1 state after the final data character of the record; i.e. those flip-flops that have already been complemented an odd number of times in the course of the record. This yields an even longitudinal parity for each of the seven channels of the record and permits the EOR mark to be used as a longitudinal parity check character. (Only the six data channels are actually checked for longitudinal parity.)

## READ LOGIC

The read logic accepts seven transport signals corresponding to each input data character, assembles the input character in the read buffer, tests it for the correct lateral parity, and applies it to the data control (via the tape control).

### Read Buffer

The read buffer (-521:A5-8) is composed of seven 500-kc flip-flops; six data flip-flops RB0-5 and a lateral parity flip-flop RB6. Each of the RB flip-flops is set to 1 at the peak of every transport input signal on the corresponding read channel. The ground assertion 1 outputs of the six RB data flip-flops are applied to output buffer inverters within the interface, and the inverter outputs are, in turn, applied to the tape control as RBB0(1)-RBB5(1). Negative levels represent 1s in the corresponding bit positions. The negative assertion 1 output of the RB parity flip-flop RB6(1) is applied to the tape control directly without inversion.

### RB Clear

The read buffer is cleared by the 0——>RB pulse from the tape control. This clear occurs at the beginning of each command to ensure that the buffer starts reading in the correct initial condition. It also occurs after each character is read to prepare the read buffer for the 1s

transfer of the next character. The latter clear occurs at CSD(0), the end of the character skew delay. At that time, the current character has been fully entered into the read buffer. The contents of the buffer are sampled at the same time that the buffer is cleared.

## RB Set

At successive changes of tape magnetization, the differential amplifier at each of the transport read heads produces output signals of alternating polarity (the polarity of each signal depending on the sign of the change). The bipolar output signal from each of the seven tape channels is applied to one channel of the 1534 Variable Slicing Rectifier circuits in the interface (-521:B4-8). The 1534 channel rectifies the output of the differential amplifier and produces a positive output pulse at each input of either polarity. However, no output is generated unless the input exceeds a preset slice level. (This is to prevent noise inputs from producing spurious output pulses.)

## Slice Control – Three separate slice levels are used:

1. The slice level is set at 25 percent of the signal amplitude for the read after write (when the tape is most strongly magnetized).

2. A 15 percent slice level is used for normal read operations.

3. A 5 percent slice level is used for old tapes with weak magnetization.

The slice level is controlled by the X and Y inputs to the 1534 circuits. When T WRITE/READ is negative (indicating a write, write file, or write blank tape command), both the X and the Y inputs to the 1534 circuits are grounded, producing the 25 percent slice level. When T WRITE/READ is ground (indicating that one of the read commands is being used), the slice level is determined by the state of CB20 (in the tape control command buffer). If CB20 contains 0, the SLICE 1 input from the tape control is ground. This condition causes a ground level to be applied to the X inputs of the 1534 circuits, and a negative level to be applied to the Y inputs. As a result, the 15 percent normal read slice level is used. However, if CB20 contains 1, the SLICE 1 input is negative, and the X and Y inputs to the 1534 circuits are reversed; X is then negative, and Y is ground. This causes the 1534 circuits to use the 5 percent low read slice level which is appropriate for weakly magnetized tapes.

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<u>Read Enable</u> – The outputs from the seven 1534 Slicing Rectifier Channels are applied to the seven channels of the 1535 Peak Detector Circuits shown in (-521:B5-8). These circuits are enabled only when both the GO flip-flop and the RDE flip-flop (-521:B4) are in the 1 state. The GO flip-flop is set at the IOT 7104 start pulse; the RDE flip-flop is set at the first subsequent MP pulse. This MP pulse originates in the tape control as the MDF pulse marking the end of the UPS acceleration state. Both the GO flip-flop and the RDE flip-flop are cleared at the $0 \longrightarrow CM$ pulse. This read enable gating ensures that the peak detectors are enabled only when the tape is moving at full speed.

<u>Peak Detector Outputs</u> – When enabled and pulsed by an output from the corresponding slicing rectifier channel, each peak detector generates a negative output pulse. The pulse is inverted, and the resulting positive pulse is applied to the complement input of the corresponding RB flip-flop (setting it to the 1 state because it was cleared at the preceding $0 \longrightarrow RB$ pulse).

<u>RBCP and RBEF</u>

The RBCP level (read buffer character present) is asserted whenever any of the six read buffer data bits RB0-5 contain 1 (-521:C7). This level is sent to the tape control where it is ORed with RB6(1) to produce the CHP (character present) signal.

The RBEF read buffer end-of-file level (-521:C6) is asserted and applied to the tape control when the six data bits of the read buffer RB contain the file mark character (17 octal).

## End-of-File Flag

The EFF flip-flop (-521:C8) is set to 1 to indicate that a file mark has been sensed. Although the EFF flip-flop is physically located in the interface, the signals controlling its set and reset originate in the tape control. The interface sends an RBEF level to the tape control whenever a file mark character (17 octal) is read. If BR6(0) is also asserted, indicating BCD parity, and if the character is the first data character of the current record, the EOF level is asserted, and the character is treated as a file mark.

At the RCP pulse (which coincides with the end of the CSD delay), the tape control applies a $1 \longrightarrow EFF$ ground pulse to interface input terminal 3B81M, setting EFF (-521:C8). If additional

data characters are in the current record, the file mark indication is assumed to be the result of a programming error, and EFF is reset at the EOR 1 pulse that ends the record. The tape control accomplishes this by applying a 0 ——→ EFF ground pulse to interface input terminal 3B88K. The EFF is also reset at the beginning of each command by STATUS CLEAR (designated MCL within the 516 Tape Control).

## Read Parity Net

As each input character is read into the read buffer RB0-6, the read parity net (-521:C and D4-8) checks the character for correct lateral parity. If the parity is not correct, a negative TRPE (tape read parity error) level is sent to the tape control.

The read parity circuit is virtually identical to the write parity net described previously under Write Parity Net, except that it contains one extra leg. Both the PAR 0 and PAR 1 outputs of the CB21 flip-flop are used as inputs to the read parity net. When binary (odd) parity is specified, the PAR 1 level is negatively asserted; and when BCD parity is specified, PAR 0 is negatively asserted. The RB inputs are also negative assertion levels. A parity error TRPE is asserted when PAR 0 is asserted and an odd number of the seven RB bits RB0-6 contain 1s; TRPE is also asserted when PAR 1 is asserted and an even number of the RB bits contain 1s.

## Parity Error Flip-Flop

The parity error flip-flop PER (-521:C8) is set to 1 to indicate that a lateral parity error has occurred. The PER flip-flop is physically located in the interface, but the signals controlling its set and reset originate in the tape control. The interface sends a TRPE level to the tape control whenever the character currently being read displays an apparent parity error. If the character is a data character rather than an EOR mark, the tape control sets the parity error flip-flop by applying a ground pulse to interface input terminal 3B81N. However, if the character displaying the apparent parity error is an EOR mark, MCD(1) is not asserted at RCP time, and the parity error flip-flop is not set. (The EOR mark serves as the longitudinal parity check character and may or may not have correct lateral parity. For this reason, it is necessary to prevent any TRPE signals that are produced by EOR marks from setting the PER flip-flop.)

If the EFF is set to 1, it causes the PER flip-flop to be reset to 0 at EOR 1. This removes the false parity error that would appear if the file mark were read in binary parity through a programming error. The PER is also reset at the beginning of each command by STATUS CLEAR, (designated MCL within the 516 Tape Control).

# CHAPTER 9

# TAPE CONTROL INTERFACE 522A

The 522A Interface permits the Magnetic Tape Control 516 or the Magnetic Tape Control 75A to control up to eight Type 729 or Type 7330 Tape Transports. The interface contains a read buffer, write and read parity networks, and associated logic. The end-of-file flag and lateral-error-parity flag are also located in the interface, as are various control circuits that process command and selection levels from the tape control and apply appropriate control signals to the tape transports.

The system logic is shown in four engineering logic drawings, BS-D-522A-0-3(1), (2), (3), and (4). A flow diagram of the interface start sequence and turn around sequence is presented in Figure 9-1.

## COMMAND AND SELECTION INPUTS

The command and selection inputs select a specific tape transport for the current command and cause the interface logic to apply appropriate control signals to that transport.

### Selection Inputs

Eight unit selection levels UNIT 0-7 are applied to the interface from the tape control (-522A(1):B-D1). The selection level corresponding to the selected tape transport is negatively asserted; the other seven levels remain at ground. All eight levels are sent through 4659 DEC-to-IBM line drivers before being applied to the transports as T UNIT 0-7. The tape control always selects the transport to be used in the current command (by asserting the associated unit selection level) before applying command levels to the interface.

### Command Inputs

Four command levels are applied to the interface from the tape control: FOW, BAC, REWIND, and WRITE (-522A(2):B1). These inputs, together with the CON(1) level, (from CB24 in the tape control command buffer (-522A(1):B6), determine the type of operation the transport is to
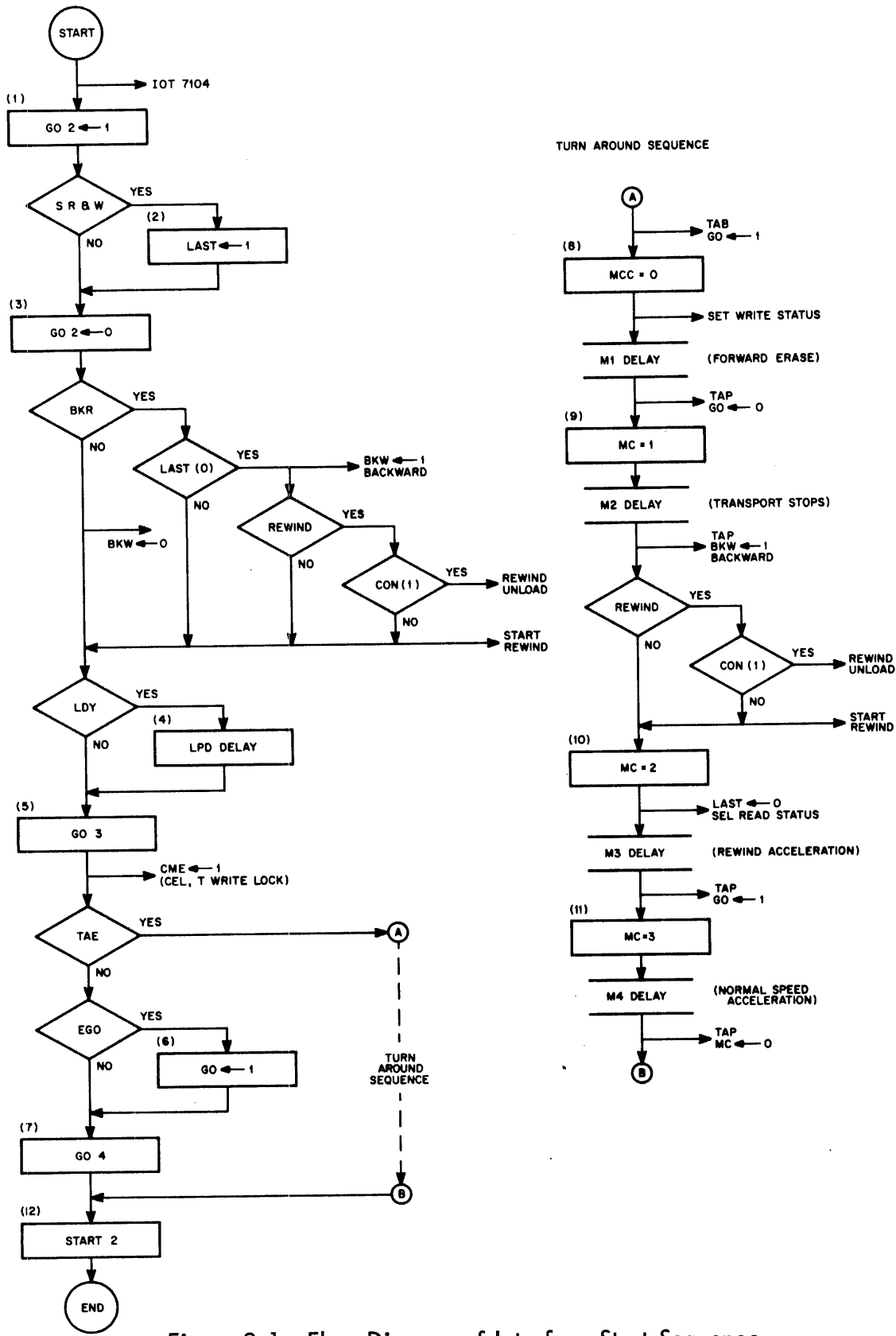
Figure 9-1   Flow Diagram of Interface Start Sequence
(Including Turn Around Sequence When Used)

commence after receiving a start pulse from the tape control and executing the necessary start sequence. The WRITE level is asserted at ground; the other three command levels and the CON(1) level are negatively asserted.

The WRITE level is used to generate T WRITE. The T WRITE, in turn, causes the SET WRITE STATUS signal to be applied to the transports, provides a necessary input condition for generating T WRITE LOCK, and is used to control the read logic slice level. When WRITE is asserted at ground, SET WRITE STATUS sets the selected transport to write status by enabling both the write logic and the read logic. A negative WRITE input does not enable the transport write logic, but rather allows the selected transport to be held in read status, or (through a proper turn around sequence; see Turn Around Sequence below) to be switched from write status to read status.

The FOW command input indicates that the current command calls for forward tape motion and the BAC input calls for backward tape motion (at normal reading speed). The REWIND command input causes the transport to reverse at rewind speed (about twice normal reading speed). If CB24 (in the tape control command buffer) contains 0, the transport rewinds only as far as the tape load point and then stops. However, if CB24 contains 1, CON(1) is asserted, and a rewind unload command is specified; this command rewinds the entire tape.

## SIGNALS BETWEEN INTERFACE AND TRANSPORTS

Various control signals are sent from the interface to the selected transport, and a number of status signals are returned from the transport to the interface. The present paragraph groups these signals by function and summarizes their principal uses. More detailed descriptions of the control and status signals are included in the signal glossaries in Chapter 12.

### Converters

The Tape Transports Type 729 and Type 7330 use and furnish IBM 7090 N and P signals. Consequently, the N and P input signals from the transports are converted to DEC logic levels before being used in the interface logic, and the DEC logic levels from the interface are converted to N and P signals before being applied to the transports. The 7090-to-DEC conversion is

accomplished by DEC 4505 and 4506 modules; for DEC-to-7090 conversion DEC 4659 and 4660 modules are utilized. Table 9-1 summarizes the inputs and outputs of these four converter modules. (For more detailed specifications see DEC System Module Catalog, C-100).

TABLE 9-1   CONVERTER MODULE INPUTS AND OUTPUTS

| Module Type | Input Signal | Resulting Output |
|---|---|---|
| | **7090 to DEC** | |
| 4505 | + P | 0 vdc |
| | - P | - 3 vdc |
| 4506 | - N | 0 vdc |
| | + N | - 3 vdc |
| | **DEC to 7090** | |
| 4659 | 0 vdc | - N |
| | - 3 vdc | + N |
| 4660 | 0 vdc | - P |
| | - 3 vdc | + P |

Motion Control Signals

The interface controls tape motion by applying four motion control signals to the selected transport: T GO, BACKWARD, START REWIND, and REWIND UNLOAD.

For all nonrewind commands, the T GO signal (-522A(2):C8) actually starts tape motion at the selected transport. If the BACKWARD signal (-522A(1):A8) is not present, T GO starts forward tape motion. If BACKWARD is asserted, T GO starts backward tape motion. In either case, when T GO ends, the transport stop sequence begins.

Neither of the two rewind signals is ever asserted unless the BACKWARD signal is also asserted. The BACKWARD and START REWIND signals (-522A(1):A8) cause the selected transport to begin reverse tape motion at rewind speed. The BACKWARD and REWIND UNLOAD signals

(-522A(1):B8) cause the transport to continue the rewind command beyond load point to rewind the entire tape. The BACKWARD signal with either the START REWIND or the REWIND UNLOAD is sufficient to start tape motion; the T GO signal is not required during rewind commands.

The same motion control signals are employed during turn around sequences. To produce the forward erase phase of the turn around, T GO is asserted and ends, and forward tape motion stops. If the turn around sequence calls for a rewind, reverse tape motion begins as soon as BACKWARD and either START REWIND or REWIND UNLOAD is asserted. If the turn around calls for a normal speed backward command, BACKWARD is asserted, and T GO is again asserted, starting backward tape motion.

## Other Transport Control Signals

Besides the motion control signals described above, other control signals are applied to the transports; these signals are described briefly below.

## SET WRITE STATUS (-522A(2):B8)

The SET WRITE STATUS signal is asserted during the forward erase phase of the turn around sequence, and during all write, write file, and write blank tape commands. It enables the write circuits of the selected tape transport, and sets the transport to write status.

## SEL READ STATUS (-522A(1):B8)

If the selected transport is in write status (for the previous command), and if it is necessary to execute a turn around sequence for the current command, the SEL READ STATUS signal switches the transport from write to read status at the proper stage of the turn around sequence. If the transport was initially in read status and is executing another command not requiring write status, the SEL READ STATUS signal merely holds the transport in read status.

## SET HIGH (LOW) DENSITY (-522A(1):B8)

The SET HIGH (LOW) DENSITY signals light the high-(low) density indicator lamps at the 729 Transports. High density is shown when D200 is not asserted; low density is shown when D200 is asserted.

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## TURN OFF TAPE INDICATE (-552A(1):AB)

This signal turns off the TAPE INDICATE light at the transport and ends the TAPE INDICATE signal returned from the transport to the interface. The TAPE INDICATE is turned on only if a write command passes tape end point. A backward or rewind command following such a write command produces TURN OFF TAPE INDICATE.

## WRITE CHARACTER (-522A(2):B8)

Until the write reset flip-flop is set, the WRITE CHARACTER signal prevents any complementing of the transport write buffer. At the end of the record, the write reset flip-flop is reset, and the resulting change in the WRITE CHARACTER signal clears the transport write buffer and writes the EOR mark on tape.

### Status Signals from Transports

The selected tape transport sends the interface status signals to indicate its current condition. These signals are described briefly below.

## SELECT & READY (-522A(1):C, D8)

The SELECT & READY signal indicates that the selected transport is not rewinding and that it is ready to accept the next command. SELECT & READY is called T READY within the interface and RDY in the 516 Control.

## SELECT READY & WRITE (-522A(2):C8)

The SELECT READY & WRITE signal indicates that the transport is set to write status. This means that it has received a write command, and, having met all necessary conditions for writing, has set the read-write status indicator to write status.

## T WRITE LOCK (-522A(1):D6)

The T WRITE LOCK signal indicates that although a write command has been given, the selected transport has remained in read status. (The most common cause of this occurrence is failure to remove the tape write enable lockout ring from the tape reel.) In the 516 Control, T WRITE LOCK is designated TWL.

## TAPE INDICATE (-522A(1):C8)

This signal indicates that the tape has reached or passed the end point while writing. TAPE INDICATE is called T END POINT within the interface, and TEP in the 516 Control.

## REWIND STATUS (-522A(1):C8)

The REWIND STATUS signal indicates that the selected transport is rewinding. This signal is asserted until the transport reaches end point. In the interface, it is called T REWIND; in the 516 Control, it is designated RWD.

## START SEQUENCE

The interface start sequence incorporates a sequential chain of programmed delays designed to provide correct timing for the control signals used with each set of command conditions. A flow diagram of the interface start sequence is presented in Figure 9-1.

## Set LAST

In all cases, the IOT 7104 interface start pulse begins the start sequence by setting the GO 2 delay (-522A(1):A2). The SELECT READY & WRITE signal (-522A(2):C8) is sampled during the time that the GO 2 delay remains set. (When the tape is at load point, the sample period is extended for the duration of the T LOAD POINT signal (-522A(2):D7). If SELECT READY & WRITE is asserted during the sample period, LAST(1) sets the LAST flip-flop; see Figure 9-1, steps 1 and 2. The STATUS LAST OPERATION WRITE level (-522A(2):A1) sends the state of LAST to the tape control status register.

The set of the LAST flip-flop indicates that the selected transport is in write status. If this is the case, certain constraints are imposed on the start sequence. Unless the next command is a write, write file, or write blank tape command, a turn around sequence (see Turn Around Sequence p. 9-10) must be executed to free the transport from write status. The turn around sequence requires either a backward command or a rewind command to switch the transport from write status to read status.

For example, a write command could not be followed immediately by a forward read command. (If this were attempted, the transport would not start.) It is, however, permissible to follow the write command with a backward read, and then to program a forward read. The backward read produces a turn around sequence that switches the transport to read status. When the transport enters read status, the LAST flip-flop is reset to 0, and the transport is free to execute a forward read as its next command.

## Set or Reset BKW

At the expiration of the GO 2 delay, the BKW flip-flop may be either set or reset (Figure 9-1, step 3). If the current command is neither a backward command nor a rewind command, the BKR flip-flop is reset (-522A(1):A2). However, if the current command is a backward or rewind command, BKR is asserted.

The BKR level may be asserted with either of two conditions: LAST (1), or LAST (0). If LAST (1) is asserted, the BKR level calls for a turn around sequence, and the BKW flip-flop is left for the time being in the 0 state. (Assertion of LAST (1) indicates that the preceding command must have been a write, write file, or write blank tape. Because these are all forward commands, BKW must have been in the 0 state at the beginning of the current command.) However, if LAST (0) is asserted, no turn around sequence is required, and at the termination of the GO 2 delay, the BKW flip-flop is immediately set to 1. The BACKWARD signal is applied to the selected transport as long as the BKW flip-flop remains set.

The effect of setting BKW to 1 depends upon two more decision points (designated REWIND and CON (1) in Figure 9-1, step 3). If the REWIND command level is not present, a normal speed backward command is called for, so tape motion does not start when BKW is set and BACKWARD is applied to the transport. (For all normal speed commands, the GO flip-flop must be set and T GO must be applied to the transport to start tape motion. The GO flip-flop is not set until the GO 3 pulse occurs later (step 5) in the start sequence.) However, if the REWIND command level is present, tape motion begins as soon as BKW is set. If CON (1) is asserted, the BACKWARD and REWIND UNLOAD signals are applied to the transport when BKW is set. If CON (0) is asserted, BACKWARD and START REWIND are applied to the transport when BKW is set. In either case, tape motion begins when BKW is set at the expiration of the GO 2 delay.

## Load Point Delay

Depending upon whether or not the LDY level is asserted, the LPD delay (-522A(1):C3) may or may not be included between the termination of the GO 2 delay and the generation of the GO 3 pulse (Figure 9-1, step 4). If LDY is not asserted, the LPD is not set, and the GO 3 pulse is produced as soon as the GO 2 delay times out. However, if LDY is asserted, the GO 2 reset sets LPD, and the GO 3 pulse is not generated until LPD times out.

The LPD provides the delay needed for the tape to move off the load point and for the transport to enter the ready state. For the Type 7339 Transport, the LPD delay is also used for another function. The Type 7330 requires an appreciable time to change direction; relays must switch, the motor fields must change polarity, and the capstan must reverse direction. The LPD provides this change of direction delay for systems using the 7330 Transport.

## Command Enable Last Level

The GO 3 pulse (Figure 9-1, step 5) sets the CME flip-flop (-522A(1):B4). If LAST (0) is asserted, indicating that the selected transport is in read status, the CME set causes the command enable last level CEL to be asserted. The CEL level is a sufficient condition for applying the SEL READ STATUS signal (-522A(1):B8) to the transports. This signal holds the selected transport in read status.

If the current command is a write, write file, or write blank tape command, T WRITE is asserted, and the CEL level causes the T WRITE LOCK signal (-522A(1):D6) to be applied to the tape control. The T WRITE LOCK signal indicates that although a write command has been given, the selected transport has remained in read status. The most common cause of this occurrence is failure to remove the tape write enable lockout ring from the tape reel. In the 516 Control, the T WRITE LOCK signal is designated TWL.

## Normal Start

If no turn around sequence is required, TAE is not asserted, and the interface executes the normal start operations shown in steps 6 and 7 of Figure 9-1. (When a turn around sequence is indicated, TAE is asserted, and the interface executes steps 8 through 11 instead of steps 6 and 7.)

Provided that EGO is asserted, the GO flip-flop is set to 1 at GO 3 (see step 6). The set of GO causes the T GO signal to be applied to the transport, beginning normal speed tape motion. If the BACKWARD signal is asserted, the tape starts to move backward when T GO appears; if BACKWARD is not asserted, the tape starts to move forward at T GO; refer to Set or Reset BKW above.

There are conditions for which EGO is not asserted, and the GO flip-flop is not set. The GO flip-flop is not set for a NOP command. It is not set for a write command given beyond end point or for a write command during which the transport has remained in read status. The GO flip-flop is not set when a write command is followed by a forward read or space command (refer to Set LAST above). Finally, the GO flip-flop is not set for a rewind command given with the transport in read status (no turn around required); for such a command, the REWIND UNLOAD or START REWIND signal described in Set or Reset BKW starts tape motion, and there is no need to set GO.

One μsec after the beginning of GO 3, the trailing edge of that pulse initiates the GO 4 pulse (Figure 9-1, step 7). Provided that no turn around sequence is required, TAE is negated (-522A (1):C5) and the GO 4 pulse triggers the tape control start pulse START 2 (Figure 9-1, step 12). In the 516 Control, START 2 is designated STM.

## Turn Around Sequence

To switch the selected transport from write status to read status, a turn around sequence is required. The turn around first causes the transport to forward erase approximately 3/4 inch of tape. The transport then stops forward tape motion, switches from write status to read status, and begins reverse tape motion at rewind or normal speed (the choice of speed depending on the nature of the turn around command).

A turn around sequence is initiated by giving a rewind or backward command when the selected transport is in write status. A rewind or backward command given while LAST(1) is present causes the assertion of the turn around enable level TAE (-522A(1):B3) and initiates the turn around sequence at GO 3. Instead of following the normal start sequence described under Normal Start, the interface follows the turn around sequence, jumping directly under step 5 of Figure 9-1 to step 8, and proceeding through steps 9-12.

When TAE is asserted, the GO 3 pulse triggers the turn around begin pulse TAB (-522A(2):C5) and starts M1, the first delay of the turn around sequence. Because the EGO level is asserted during turn around, the GO 3 pulse also sets the GO flip-flop (-522A(2):A6), starting forward tape motion for the forward erase phase of the turn around sequence. The first TAD set begins the MCC = 0 level (Figure 9-1, step 8); that level, in turn, applies the SET WRITE STATUS signal (-522A(2):B8) to the selected transport, enabling the transport write circuits during the forward erase phase of the turn around. The forward erase continues until M1, the first TAD delay, times out. The resulting TAP pulse advances the MC counter to MC = 1 (Figure 9-1, step 9) and resets the GO flip-flop (-522A(2):A6). The reset of GO begins to stop the forward motion of the tape. The timeout of the first TAD delay starts the second TAD delay, M2.

During the M2 delay, the tape's forward motion comes to a full stop. The TAP pulse that terminates the M2 delay sets the BKW flip-flop (-522A(1):A3) and applies the BACKWARD signal to the transport. If the current command is a normal speed backward command, no tape motion results. However, if the current command is a rewind unload or rewind, a REWIND UNLOAD or START REWIND signal is applied to the selected transport with the BACKWARD signal, and tape motion begins immediately. The same TAP pulse that sets BKW also advances the MC counter to MC = 2 (Figure 9-1, step 10), resetting the LAST flip-flop (-522A(2):A7) and applying the SEL READ STATUS signal to the selected transport (-522A(1):B8). The SEL READ STATUS signal switches the transport from write status to read status. The timeout of the second TAD delay starts the third TAD delay, M3.

If the current command is a rewind unload or a rewind command, the tape accelerates during the M3 delay. If the current command is a normal speed backward command, acceleration does not begin until the end of the M3 delay. The TAP pulse that terminates the M3 delay and steps the MC counter to MC = 3 (Figure 9-1, step 11), also sets the GO flip-flop to the 1 state. The set of GO applies the T GO signal to the selected transport and starts tape motion (if the current command is a normal speed backward command rather than a rewind command). The timeout of the third TAD delay starts the fourth and final TAD delay, M4.

During the M4 delay, if the current command is a normal speed backward command, the tape reverses across the 3/4 inch section of tape that was forward erased during M1. The TAP pulse

that terminates the M4 delay resets the MC counter to MC = 0. This same TAP (-522A(1):B4) terminates the turn around sequence by generating the tape control start pulse START 2 (Figure 9-1, step 12). In the 516 Control, START 2 is designated STM.

## WRITE LOGIC

The write logic receives the write data outputs and write pulses from the tape control, converts them to - N signals, and applies them to the write buffer in the transport. The write logic also generates the lateral parity bit, the WRITE CHARACTER signal, and the WRT NOK alarm condition.

### Write Data Outputs

During WRT and WRF commands, the six write data outputs WD0-WD5 apply output data characters from the tape control to the interface (-522A(1):B2-5). Ground levels correspond to 1 bits. The WD levels determine which of the data flip-flops in the transport write buffer are to be complemented at the write pulse. The WD outputs are inverted, and both the original WDn(1) levels and their BWDn(0) complements are applied to the write parity network. (At the parity net inputs (-522A(1)C3-6), these signals are shown as WDn(0) and BWDn(1); i.e. at negative assertion rather than ground assertion.) The parity network then generates a seventh output which determines whether or not the write buffer parity flip-flop is to be complemented at the write pulse.

The six write data outputs WD(1)-WD5(1) and the output of the write parity network are applied to the transport write buffer through seven 4659 Line Drivers. At the outputs of the line drivers, these seven signals are redesignated WRITE CH B, A, 8, 4, 2, 1, and C, respectively. The WD (or parity) outputs corresponding to 1 bits produce WRITE CH signals at - N; the 0 bits produce + N signals. The seven WRITE CH signals control the response of the transport write buffer to the write pulses. Those write buffer flip-flops which correspond to 1 outputs (and hence - N signals) are complemented at the write pulse; the remaining write buffer flip-flops are not complemented.

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## Write Buffer

The write buffer is a seven-bit flip-flop register in the transport logic. Both outputs of each flip-flop are applied to the transport write amplifiers. Depending on the state of the associated write buffer flip-flop, each write amplifier drives one or the other of two oppositely wound write head coils. Each transition of a write buffer flip-flop terminates the current through one coil and starts it in the other, changing the state of tape magnetization and writing a 1 in the corresponding tape channel.

## Write Parity Net

As each 6-bit output character is transferred out to the interface by the WD outputs, the write parity net (-522A(1):B, C3-7) generates an accompanying parity bit.

If CB21 (in the tape control command buffer) contains 0, the writing is to be done in BCD (even) parity. The 0 state of CB21 causes a negative PAR 0 input to be applied to the write parity net (-522A(1):C7). This input causes the parity net to generate a 1 parity output (a ground level) if an odd number of the six WD outputs are 1s.

The ground parity 1 level is applied to line driver 3A19, and the WRITE CH C output signal from that circuit is, in turn, applied (at - N) to the transport write buffer parity flip-flop. The parity flip-flop is complemented by the write pulse, and the transport writes a 1 bit in the parity channel for the current character. This yields a character with an even number of 1 bits.

If CB21 contains a 1, the writing is to be done in binary (odd) parity. A ground PAR 0 input is applied to the parity net, and the 1 parity output is generated only if an even number of the six WD outputs are 1s.

The write parity net is composed of a 3-stage, 7-input exclusive OR circuit. All of the WD and BWD inputs are negative assertion levels (-522A(1):C3-6). The 1 parity output level is asserted at ground (-(1):A6) only if an odd number of the seven inputs are 1 (counting the six WD bits and the contents of CB21). The assertion levels shown in the two upper stages of the net assume that each of the three pairs of WD bits includes a 1 bit and a 0 bit and that the PAR 0 input is negative (i.e. that CB21 is 0, indicating BCD parity). In inverter 3B17,

three external 3.3K resistors have been substituted for the normal 1.5K load resistors. This reduces the current through the lower legs of the parity net and avoids excessive loading.

The WEF command level is inverted in the tape control (-CM:C4) and applied to the write parity net as $\overline{\text{WRITE EOF}}$; refer to -522A(1):B5. When this level is negative (as it is for write file commands), inverter 3B22 holds the parity net output negative, inhibiting the generation of a 1 parity bit. The end-of-file character 001 111 (17 octal) should always be written in BCD parity (with a 0 parity bit). The WRITE EOF input ensures that the write parity net produces the correct 0 parity bit for the EOF character even if the programmer should inadvertently give a WRF command with binary parity.

## Write Reset Flip-Flop

The state of the write reset flip-flop (-(2):A3) controls the WRITE CHARACTER signal applied to the transports (-(2):B8). Although the write circuits of the selected transport are enabled when SET WRITE STATUS is asserted, the transport write buffer flip-flops cannot be complemented until the write reset flip-flop is set to 1.

The write reset flip-flop is set to 1 at the first WP pulse of the record. (The WP pulses are delayed 1 μsec before being applied to the transports; this gives the WRITE CHARACTER signal time to change state so that even the first WP of the record is enabled to complement the write buffer bits of the selected transport.)

The write reset flip-flop is reset at each START 1 pulse. The START 1 pulse originates in the 516 Tape Control as EOR 2. A START 1 is produced at the beginning of each command to ensure that every record begins with the write reset flip-flop and the write buffer cleared. Another START 1 is applied to the interface four to five character spaces after the last WP pulse of each record (4 spaces during WRF records, and 4.5 spaces +2.5 μsec during WRT records). The resulting clear of the write reset flip-flop causes the WRITE CHARACTER signal to change state and clears the transport write buffer.

The START 1 clear complements the write buffer flip-flops that are left in the 1 state after the final data character of the record; i.e. those flip-flops that have already been complemented an odd number of times in the course of the record. This yields an even longitudinal parity for

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each of the seven channels of the record and permits the EOR mark to be used as a longitudinal parity check character. (Only the six data channels are actually checked for longitudinal parity.)

The Type 729 and Type 7330 Transports require WRITE CHARACTER signals of opposite polarity; consequently, different outputs of the write reset flip-flop are jumpered to the input of line driver 3B21 (-522A(2):B7), the choice depending on the type of transport used. However, for either transport type, the write reset flip-flop is set to 1 so that the write buffer can be complemented, and the write reset flip-flop is reset to 0 to produce the EOR mark.

## Write Pulse Generation

The WP write pulses originate in the tape control. They are delayed 1 μsec by pulse amplifier 3A22 (-522A(2):A6), are stretched to the correct pulse width by 4301 Delay 3A3, and are applied to the transports via line driver 3A5 (as -N pulses) with the designation WRITE PULSE. The width of the WRITE PULSE may vary from 2 to 12 μsec depending on the type of transport used.

## Write Echo

The write echo flip-flop WOK and the write not OK flip-flop WRT NOK make up a 2-stage alarm network (-(2):A4). During write and write file commands, this network ensures that the programmer has flag notice of any total failure to write a character. The WOK flip-flop is set at each WP pulse. Provided that a 1 is written in (and read back from) at least one of the seven tape channels, a WRITE ECHO signal (-2):B8) is returned from the selected tape transport, resetting the WOK flip-flop.

Normally, each WP pulse writes a character that produces a WRITE ECHO signal return, and the WOK flip-flop is reset by the resulting WOK(0) ground level (-(2):B7); in this case, the WOK flip-flop is reset prior to the arrival of the next WP pulse from the tape control. However, if any WP pulse should fail to produce a WRITE ECHO return, it is likely that a write failure has occurred, and WOK is not reset before the next WP pulse arrives from the tape control. Because the WOK flip-flop remains in the 1 state, the next WP pulse strobes WOK(1) into the WRT NOK flag.

The WRT NOK flag is set whenever there is a total failure to write any character. It remains set throughout the command during which the failure occurs; it is not reset until the STATUS CLEAR at the beginning of the following command. Whenever WRT NOK contains 1, the negative assertion level TO STATUS REGISTER WRITE NOK (-(2):C1) is applied to the tape control status register. (In the 516 Control, this level is designated TFR - AB - WRK NOK.)

## READ LOGIC

The read logic accepts seven transport signals corresponding to each input character, assembles the input character in the read buffer, tests it for the correct lateral parity, and applies it to the data control (via the tape control).

### Read Buffer

The read buffer (-(3):A4-7) is composed of seven 500-kc flip-flops; six data flip-flops RB0-5 and a lateral parity flip-flop RB6. Each of the RB flip-flops is set to 1 at the peak of every transport input signal on the corresponding read channel. The ground assertion 1 outputs of the six RB data flip-flops are applied to output buffer inverters within the interface, and the inverter outputs are, in turn, applied to the tape control as RBB0(1)-RBB5(1). Negative levels represent 1s in the corresponding bit positions. The negative assertion 1 output of the RB parity flip-flop RB6(1) is applied to the tape control directly without inversion.

### RB Clear

The read buffer is cleared by the 0 —→ RB pulse from the tape control. This clear occurs at the beginning of each command to ensure that the buffer starts reading in the correct initial condition. It also occurs after each character is read to prepare the read buffer for the 1s transfer of the next character. The latter clear occurs at CSD(0), the end of the character skew delay. At that time, the current character has been fully entered into the read buffer. The contents of the buffer are sampled at the same time that the buffer is cleared.

### RB Set

At successive changes of tape magnetization, the differential amplifier at each of the transport read heads produces output signals of alternating polarity (the polarity of each signal depending

on the sign of the change). The bipolar output signal from each of the seven tape channels is applied to one channel of the 1534 Variable Slicing Rectifier circuits in the interface (-(3):A and C2). The 1534 channel rectifies the output of the differential amplifier and produces a positive output pulse at each input of either polarity. However, no output is generated unless the input exceeds a preset slice level. (This is to prevent noise inputs from producing spurious output pulses.)

Slice Control - Three separate slice levels are used:

1. The slice level is set at 25 percent of the signal amplitude for the read after write (when the tape is most strongly magnetized).

2. A 15 percent slice level is used for normal read operations.

3. A 5 percent slice level is used for old tapes with weak magnetization.

The slice level is controlled by the X and Y inputs to the 1534 circuits. When T WRITE (-(3):C3) is asserted negatively (indicating a write, write file, or write blank tape command), both the X and the Y inputs to the 1534 circuits are grounded, producing the 25 percent slice level. When T WRITE is ground (indicating that one of the read commands is being used), the slice level is determined by the state of CB20 (in the tape control command buffer). If CB20 contains 0, the SLICE 1 input from the tape control is ground. This causes a ground level to be applied to the X inputs of the 1534 circuits, and a negative level to be applied to the Y inputs. As a result, the 15 percent normal read slice level is used. However, if CB20 contains 1, the SLICE 1 input is negative, and the X and Y inputs to the 1534 circuits are reversed; X is then negative, and Y is ground. This causes the 1534 circuits to use the 5 percent low read slice level which is appropriate for weakly magnetized tapes.

Read Enable - The outputs from the seven 1534 Slicing Rectifier circuits are applied to the seven channels of the 1535 Peak Detector circuits shown in -(3):A-C2. These circuits are enabled only when both the GO flip-flop (-(2):A6) and the RDE flip-flop (-(1):C8) are in the 1 state. This read enable gating ensures that the peak detectors are enabled only when the tape is moving at full speed. The RDE flip-flop is not set until the first MP pulse following IOT

7104. This MP pulse originates in the tape control as the MDF pulse marking the end of the UPS acceleration state (for normal speed commands). Both the GO flip-flop and the RDE flip-flop are cleared at the 0 $\longrightarrow$ CM pulse. For rewind commands not involving a turn around sequence, GO is not set, and the peak detectors are not enabled. For rewind commands that do involve a turn around sequence, the peak detectors are enabled, but because the transport read signals are disabled, no reading can occur.

Peak Detector Outputs - When enabled and pulsed by an output from the corresponding slicing, rectifier channel, each peak detector generates a negative output pulse 1 $\longrightarrow$ RBn (-(3):A-C2). The negative output pulse from each peak detector is inverted, and the resulting positive pulse is applied to the complement input of the corresponding RB flip-flop (setting it to the 1 state because it was cleared at the preceding 0 $\longrightarrow$ RB pulse).

RBCP and RBEF

The RBCP level (read buffer character present) is asserted whenever any of the six read buffer data bits RB0-5 contain 1; see -(3):C3. This level is sent to the tape control, where it is ORed with RB6(1) to produce the CHP (character present) signal.

The RBEF, read buffer end-of-file level, (-(3):C2) is asserted and applied to the tape control when the six data bits of the read buffer RB contain the file mark character (17 octal).

### End-of-File Flag

The EFF flip-flop (-(1):B7) is set to 1 to indicate that a file mark has been sensed. Although the EFF flip-flop is physically located in the interface, the signals controlling its set and reset originate in the tape control. The interface sends an RBEF level to the tape control whenever a file mark character (17 octal) is read. If RB6(0) is also asserted, indicating BCD parity, and the character is the first data character of the current record, the EOF level is asserted, and the character is treated as a file mark.

At the RCP pulse (which coincides with the end of the CSD delay) the tape control applies a 1 $\longrightarrow$ EFF ground pulse to interface input terminal 3B81M, setting EFF (-(1):B7). If additional data characters are in the current record, the file mark indication is assumed to be the result

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of a programming error, and EFF is reset at the EOR 1 pulse that ends the record. The tape control accomplishes this by applying a 0 $\longrightarrow$ EFF ground pulse to interface input terminal 3B88K. The EFF is also reset at the beginning of each command by STATUS CLEAR (designated MCL within the 516 Tape Control).

## Read Parity Net

As each input character is read into the read buffer RB0-6, the read parity net (-(3):C and D4-8) checks the character for correct lateral parity. If the parity is not correct, a negative TRPE (tape read parity error) level is sent to the tape control.

The read parity circuit is vitually identical to the write parity net described previously under Write Parity Net, except that it contains one extra leg. Both the PAR 0 and PAR 1 outputs of the CB21 flip-flop are used as inputs to the read parity net. When binary (odd) parity is specified, the PAR 1 level is negatively asserted; and when BCD parity is specified, PAR 0 is negatively asserted. The RB inputs are also negative assertion levels. A parity error TRPE is asserted when PAR 0 is asserted, and an odd number of the seven RB bits RB0-6 contain 1s; TRPE is also asserted when PAR 1 is asserted and an even number of the RB bits contain 1s.

## Parity Error Flip-Flop

The parity error flip-flop PER (-(1):B7) is set to 1 to indicate that a lateral parity error has occurred. The PER flip-flop is physically located in the interface, but the signals controlling its set and reset originate in the tape control. The interface sends a TRPE level to the tape control whenever the character currently being read displays an apparent parity error. If the character is a data character rather than an EOR mark, the tape control sets the parity error flip-flop by applying a ground pulse to interface input terminal 3B81N. However, if the character displaying the apparent parity error is an EOR mark, MCD(1) is not asserted at RCP time, and the parity error flip-flop is not set. (The EOR mark serves as the longitudinal parity check character and may or may not have correct lateral parity. For this reason, it is necessary to prevent any TRPE signals that are produced by EOR marks from setting the PER flip-flop).

If the EFF is set to 1, it causes the PER flip-flop to be reset to 0 at EOR 1. This removes the false parity error that would appear if the file mark were read in binary parity through a programming error. The PER is also reset at the beginning of each command by STATUS CLEAR (designated MCL within the 516 Tape Control).

# CHAPTER 10

# MAINTENANCE

## GENERAL

The Magnetic Tape Control 516 and the Tape Control Interface 520, 521, or 522A are ordinarily used as peripheral systems of the PDP-6 installation. The maintenance chapters of the PDP-6 Circuits manual and the PDP-6 Processor and Memory manuals include maintenance procedures and suggestions of general relevance not repeated in this manual. Familiarity with this material is essential for the efficient maintenance of the tape control, the interface units, and all other DEC systems used with PDP-6. The topics covered include: Tools and Test Equipment, Removal and Replacement of Modules, Module Troubleshooting, Use of Marginal Check, System Troubleshooting, and Maintenance Logs.

## CAUTION

The procedures described in the maintenance chapters of the PDP-6
Circuits manual and the PDP-6 Processor and Memory manuals should
be thoroughly understood before undertaking troubleshooting and re-
pair of the Magnetic Tape Control 516 and the Tape Control Inter-
face 520, 521, or 522A.

## USE OF DRAWINGS

The complete system logic of the Magnetic Tape Control 516 and the Tape Control Interfaces 520, 521, and 522A is shown in the engineering logic drawings of Chapter 13, Vol. II. Because these engineering logic drawings are the most frequently used source of troubleshooting information, it is important to be familiar with the conventions and symbols which they employ.

Figure 10-1 shows the standard cabling and module location numbering used within the DEC module racks.

## EQUIPMENT LAYOUT

The tape control logic is contained in four DEC logic racks designated from top to bottom 3C-3F (see Figure 10-1). The logic for Interface Units 520 and 521 is contained in logic rack 3B. The 522A Interface requires two racks, 3A and 3B.

The module location and use are shown in the five module location diagrams in Chapter 13, UML-516 (2 drawings), UML-520, UML-521, and UML-522A. Circuit schematics of all modules are presented in order of module type number in Chapter 13.

## PREVENTIVE MAINTENANCE

The cooling fan in the bottom of the bay should be checked daily for proper operation and free flow of air. Under normal operating conditions, the air filter at the bottom of the bay should be changed and cleaned monthly. The correct procedure for changing and cleaning filters is described in the PDP-6 processor manual maintenance chapter.

Preventive maintenance procedures for the system logic should also be scheduled on a regular basis. The same considerations that call for preventive maintenance of the PDP-6 processor apply equally to the peripheral systems. Appropriate maintenance procedures will detect and eliminate most potential malfunctions before they can cause operating errors. Refer to the PDP-6 processor manual for suggested procedures and schedules. The same basic techniques that are used in maintaining the processor (trouble isolation methods, maintenance programs, marginal check, etc.) are equally useful for maintaining the tape control and interface units.

## ADJUSTMENT AND CALIBRATION

There are five 4303 Integrating Single-Shot modules in the Magnetic Tape Control 516 and three such modules in the Tape Control Interface 522A. Each of these modules is used to produce a number of programmed delays. Normally, no adjustment or calibration is required; the delays are set to the proper time constants before the system leaves the factory and there is no appreciable drift. Similar considerations apply to the two 4407 Crystal Clocks in the tape control. Nevertheless, clock frequencies and delay time constants are given below with

SEE NOTE I & 8

SEE NOTE 4

SEE NOTE 4

#61

#81

#117

SEE NOTE 6

#42

SEE NOTE 7

#147

#50

SEE NOTE 5

SEE NOTE 3

LEFT SIDE

SEE NOTE 2
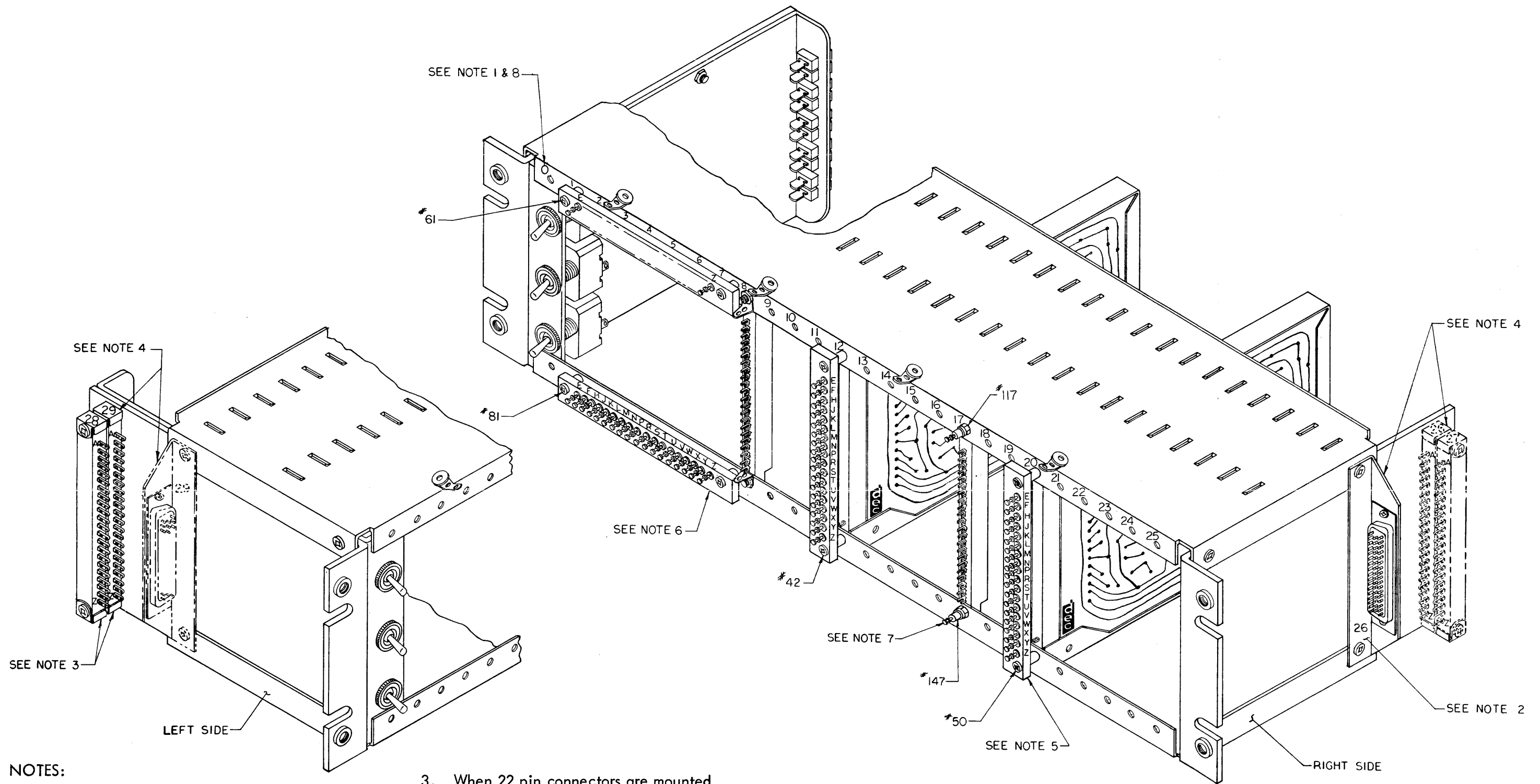
RIGHT SIDE

NOTES:

1. Numbers 0 thru 25 are called basic numbers.

2. When 50 pin connector is mounted on right side of panel, it is #26; when mounted on left side of panel, it becomes #29.

3. When 22 pin connectors are mounted on left side of panel, they are #28 and #29; when mounted on right side of panel, they become #26 and #27.

4. At no time will a 50 pin connector and 22 pin connector mount on the same side.

5. When block is vertically over position, add 30 to basic number.

6. When block is horizontal on top of panel, add 60 to basic number. When block is horizontal on bottom of panel, add 80 to basic number.

7. When standoff is on top, add 100 to basic number. When standoff is on the bottom, add 130 to basic number.

8. Numbers will always read from left to right, when viewed from the front, or wired side, of the rack.

Figure 10-1  Digital Cable and Component Numbering

10-3

procedures for adjustment and calibration. Note, however, that these procedures should not be made a part of routine maintenance schedules. Adjustment and calibration of clocks and delays should be undertaken only if it is necessary.

## Crystal Clocks

The two 4407 Crystal Clocks CK1 and CK2 (shown in —WT:B5 and B6) are adjusted to produce output pulses at twice the character rate of the tape transport operated at 800 density and 556 density, respectively. Clock frequency is proportional to tape speed and depends upon the type of transport used. In Table 10-1, the correct frequency and period are listed for both clocks used with each of the four available tape transports. The adjustment can be made in a single step by mounting the clock on a plug-in extender and monitoring its output with an oscilloscope while varying the setting of the 20K internal potentiometer.

### TABLE 10-1   CRYSTAL CLOCK FREQUENCY AND PERIOD

| Clock | Frequency pps | Period μsec |
|---|---|---|
| Tape Transport Type 50 | | |
| CK1 (D800) | 120   kc | 8.33 |
| CK2 (D556) | 83.3 kc | 12.0 |
| Tape Transport Type 570 | | |
| CK1 (D800) | 180 kc @ 112.5 ips | 5.55 |
|  | 120 kc @ 75 ips | 8.33 |
| CK2 (D556) | 125 kc @ 112.5 ips | 8.0 |
|  | 83.3 kc @ 75 ips | 12.0 |
| Tape Transport Type 729 Mod 5 | | |
| CK1 (D800) | 120   kc | 8.33 |
| CK2 (D556) | 83.3 kc | 12.0 |

TABLE 10-1   CRYSTAL CLOCK FREQUENCY AND PERIOD (continued)

| Clock | Frequency pps | Period μsec |
|---|---|---|
| Tape Transport Type 729 Mod 6 | | |
| CK1 (D800) | 180 kc | 5.55 |
| CK2 (D556) | 125 kc | 8.0 |
| Tape Transport Type 7330 | | |
| CK1 (D800) | 56.6 kc | 17.3 |
| CK2 (D556) | 40   kc | 20.0 |

## MOD Delays

The motion delay logic (–MD) contains a 4303 Integrating Single Shot module MOD and a set of twelve logically gated motion delay potentiometers. The correct time constants for each of the resulting delays are listed in Table 4-1. The delays vary depending upon the type of transport used.

Six of the twelve delays are UPS acceleration delays. These delays are calibrated by monitoring the UPS output of the tape status quint-flop (–CS:C2) with an oscilloscope while giving an appropriate series of commands. For the two UPS load point delays (D2 and D4), a series of write file commands alternating with rewind commands is given. The other four UPS delays are monitored while giving a series of write file commands in noncontinuous mode.

The three ERM tape run-out delays are calibrated in much the same way, except that the ERM output of the tape status quint-flop (–CS:C4) is the terminal monitored. Similarly, the two MOS deceleration delays are monitored at the MOS output of the quint-flop (–CS:C5). The twelfth and final delay D0 need not be calibrated. The function of this delay is to keep the MOD 4303 circuit operative during TCR and RIP; as long as the coarse-delay capacitor connection is not tampered with, the setting of the fine-delay potentiometer does not matter.

## Other Tape Control Delays

Besides the MOD circuit described above, there are four other 4303 Integrating Single Shot modules in the tape control. These four modules are:

1. EWD - End of Record Write Delay (-WT:C7)

2. CSD - Character Skew Delay (-RD:B7)

3. MCD - Miss Character Delay (-RD:B7)

4. ERD - End of Record Delay (-RD:B7)

Associated with each of these four delay modules are three logically gated delay potentiometers, one for each of the three tape densities, D200, D556, and D800. The delays also vary depending upon the type of transport used. The correct time constants are listed in Table 10-2.

The delays listed in Table 10-2 are checked directly at the delay outputs while giving a series of write file commands. (The reason for checking the MOD delays at the quint-flop rather than at the delay outputs is the difficulty of differentiating between successive delays from the same MOD module.)

## Delays in Interface 522A

The 522A Interface contains three 4303 Integrating Single Shot modules, and one 4301 Delay module. These four modules are:

1. GO 2 - Start Delay (UML-516(1):A2)

2. LPD - Load Point Delay (UML-516(1):C3)

3. TAD - Turn Around Delay (UML-516(2):B5)

4. Write Pulse Duration Delay (UML-516(2):A7)

The TAD delay has four logically gated delay potentiometers M1 through M4, each of which produces a different delay period. The other three delays each produce only a single delay period. The delay intervals vary depending upon the type of transport used. The correct time constants are listed in Table 10-3.

## TABLE 10-2  TAPE CONTROL DELAY TIME CONSTANTS

| Delay Density | Time Constant μsec | | |
|---|---|---|---|
| | D200 | D556 | D800 |
| **Tape Transport Type 50** | | | |
| EWD | 270 | 97.5 | 69.5 |
| CSD | 35 | 12 | 9 |
| MCD | 100 | 36 | 25 |
| ERD | 230 | 86 | 58 |
| **Tape Transport Type 570** | | | |
| EWD | 180 | 65 | 46 |
| CSD | 23.5 | 8.0 | 5.0 |
| MCD | 67 | 24 | 17 |
| ERD | 156 | 56 | 38 |
| **Tape Transport Type 729 Mod 5** | | | |
| EWD | 270 | 97.5 | 69.5 |
| CSD | 35 | 12 | 9 |
| MCD | 100 | 36 | 25 |
| ERD | 230 | 86 | 58 |
| **Tape Transport Type 729 Mod 6** | | | |
| EWD | 180 | 65 | 46 |
| CSD | 23.5 | 8.0 | 5.0 |
| MCD | 67 | 24 | 17 |
| ERD | 156 | 56 | 38 |
| **Tape Transport Type 7330** | | | |
| EWD | 556 | 200 | not used |
| CSD | 50 | 25 | not used |
| MCD | 200 | 75 | not used |
| ERD | 470 | 160 | not used |

## TABLE 10-3 INTERFACE 522A DELAY TIME CONSTANTS

| Delay<br>Tape Transport Type | Time Constant<br>729 Mod 5 | 729 Mod 6 | 7330 |
|---|---|---|---|
| GO 2 | 30 µsec | 20 µsec | 30 µsec |
| LPD | 16.5 msec | 11.0 msec | 250 msec |
| TAD-M1 | 12.0 msec | 8.0 msec | 25 msec |
| TAD-M2 | 5.0 msec | 5.0 msec | 10 msec |
| TAD-M3 | 12.0 msec | 6.0 msec | 250 msec |
| TAD-M4 | 5.0 msec | 4.0 msec | 10 msec |
| Write Pulse | 4.0 µsec | 3.0 µsec | 12 µsec |

## PROGRAMMING SUGGESTIONS

A few programming features of the Tape Control 516 and the Interface Units 520, 521, and 522A, which may be of special interest to maintenance personnel are summarized below. Refer to the PDP-6 programming manual for more programming information.

### Successive CONO 220 Commands

It is not necessary to wait until the completion of a given CONO 220 command to program a second one. The command hold buffer is free, and another command can be given whenever the command sync quad-flop is reset to XNC state.

### Writing Past Tape End Point

There is no logical restriction to prevent writing beyond TEP. Consequently, the programmer must use care to avoid writing too far and winding the tape off the supply reel.

### Leaving Rewinding Transports Unselected

While a given transport is rewinding, the programmer may wish to use the tape control to give a new command to another transport. Do not give the nonselected rewinding transport any further commands until its deceleration is complete. (For an explanation of why such premature

commands would be undesirable, refer to Chapter 5, Deceleration Interval.) By keeping the rewinding transport selected, the LIF flag can be used to give a load point interrupt as soon as the tape has come to a full stop. This is the best procedure if the programmer wishes to use the rewinding transport as soon as possible.

## Programmed JNU Pulse

The programmed JNU pulse (−CS:A, B6) provides a means of monitoring the status of any tape transport without applying any command to the transport being monitored. This option is particularly useful when operating with 521 Interface Units in multicontrol mode; refer to Chapter 8. The programmed JNU permits checking the status of a transport that is currently selected to the other tape control.

The programmed JNU is used in the following manner. First, a CONO 220 NOP instruction is given with bits 29-31 containing the device selection code of the transport that is to be monitored. This NOP instruction stores the device selection code in CHB29-31. Next, a CONO 224 instruction is given with a 1 in bit 34. The IOB CONO SET of this CONO 224 instruction produces a programmed JNU pulse which advances the device selection code from CHB29-31 to CB29-31.

The purpose of the two CONO instructions described above is to transfer the device selection code of the transport that is to be monitored into CB29-31. Once the device selection code is stored in CB29-31, the status of the selected transport can then be monitored at will by using a CONI 224 to sample the tape control transport-status register.

There is, however, one programming refinement which should be kept in mind when using the programmed JNU. Every CONO 224 instruction sets the four priority interrupt enable switches EFE, LIE, ICE, and XNE to the states determined by bits 33, 20, 35 and 21 of the CONO 224 instruction. Unless these four flip-flop switches are to be cleared, it is important to code all CONO 224 instructions with 1s in the correct bit positions to maintain the current switch settings.

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## Programmed CHP Pulse

The programmed CHP pulse is used as a maintenance aid. It permits the tape control to be operated without the use of an interface or transports. Each CONO 230 instruction produces a single CHP pulse at the IOB CONO SET (−RD:D8), simulating the reading of a single character from tape. The CONO 230 instructions can be programmed at any desired frequency in order to match the transport character rate.

Simulation of the interface and transport is completed by jumpering the CTT pulse (−CS:B8) back to the START 2 input (−CS:B3) to produce a simulated STM pulse, and by grounding T READY (−ST:B7).

## MAINTENANCE PROGRAMS

At present, there are three MAINDEC programs available for the Magnetic Tape Control 516. The first program facilitates oscilloscope testing; the second program yields hard copy that shows system timing relationships without the use of an oscilloscope, and the third program provides an overall summary of system performance. Brief descriptions of these three programs are presented below.

### Cursory Operation Test for Type 516 Tape Control

This simple program permits the repetition of a single command or an ordered sequence of commands throughout an entire tape. The commands making up the sequence are in a fixed order, but by DATA switches at the console any of these commands may be eliminated from the sequence. All command parameters such as slice level, parity mode, density, etc. are under switch control. Three characters (18 data bits) are set up from the console; these three characters are duplicated in the left and right half of each word written on the tape. Record length is controlled by varying a constant in memory.

### Dynamic Status Presentation for Type 516 Tape Control

This real time maintenance program checks the relative timing of the various tape control state transitions by printing out the contents of all three 18-bit status registers at fixed-time intervals.

The time standard is based on the 60-cps clock and is sufficiently accurate to calibrate the tape control clocks and delays in terms of the numerical time constants given in Tables 10-1 and 10-2. A second operating mode of this program will give decimal readings of specific delay times.

<u>PDP-6 Magnetic Tape Data Test 516</u>

This program thoroughly tests the data handling accuracy of the Magnetic Tape Control 516. The program is designed to measure the system's current level of performance rather than to locate such malfunctions as may be detected. Once it has been determined that the tape control is not performing properly, the Cursory Operation Test and the Dynamic Status Presentation programs described above are used to locate the malfunction that is producing the errors.

Typical error printouts for the data test are listed below.

Normal Error Printout

| OPER: | READ | | | | | | |
|-------|------|------|------|------|------|------|------|
| SR200: | 004022 | SR220: | 000001 | SR224: | 240037 | SR230: | 000030 |
| REC No. | LNGTH | No.ERRORS | PAR. | DENS. | SLEV. | UNIT No. | PAR.ERRORS |
| 185 | 4096 | 3 | E | L | H | 6 | Lat. Long |

| Word No. | WRITTEN | 010111 | 010111 | 010111 | 010111 | 010111 | 010111 |
|----------|---------|--------|--------|--------|--------|--------|--------|
| 3700 | READ | 010101 | 010110 | 010101 | 010111 | 010101 | 010111 |
| | | ↑ | ↑ | ↑ | | ↑ | |

Summary Printout

| RELIABILITY RUN | | | |
|-----------------|------|------|-------|
| UNITS TESTED: | 0 | 1 | 2 |
| FULL LNGTH RCDS: | 13 | 57 | 102 |
| RD ERR RCDS: | 0 | 0 | 0 |
| RD CMP ERR RCDS: | 0 | 0 | 54 |
| RD BCK ERR RCDS: | 0 | 0 | 0 |
| TOTAL WORDS: | 1664 | 7296 | 13056 |

## Summary Printout (continued)

| | | | |
|---|---|---|---|
| RD ERR WDS: | 0 | 0 | 0 |
| RD BCK ERR WDS: | 0 | 0 | 0 |
| WR PAR ERRS: | | | |
| RECOVERABLE: | 0 | 0 | 2 |
| PERMANENT: | 0 | 0 | 0 |
| RD PAR ERRS: | | | |
| RECOVERABLE: | 0 | 0 | 0 |
| PERMANENT: | 0 | 0 | 0 |
| RD BCK PAR ERRS: | | | |
| RECOVERABLE: | 0 | 0 | 0 |
| PERMANENT: | 0 | 0 | 0 |
| RD CMP PAR ERRS: | | | |
| RECOVERABLE: | 0 | 0 | 0 |
| PERMANENT: | 0 | 0 | 0 |
| ABORTED RECORDS: | 0 | 0 | 0 |
| SHORT RECORDS: | 0 | 0 | 0 |

# RECOMMENDED SPARE PARTS

The most economical quantity of spare parts to be maintained depends on the requirements of the individual user, but the following listing is suitable for most installations.

## Module Spares

Quantity: One module of each type that is used in the tape control or interface (or both).

| Module | Tape Control 516 | Interface 520 | Interface 521 | Interface 522A |
|--------|:---:|:---:|:---:|:---:|
| | | Used in | | |
| 1110 | X | | | |
| 1151 | X | | | |
| 1534 | | | X | X |
| 1535 | | | X | X |
| 1539 | | X | | |
| 1684 | | X | | |
| 1685 | | | X | |
| 1690 | | X | X | |
| 4102 | X | X | X | X |
| 4106 | | X | X | X |
| 4111 | | X | X | X |
| 4112 | X | | X | X |
| 4113 | X | X | X | X |
| 4114 | X | | | |
| 4115 | X | | | X |
| 4118 | X | | | |
| 4127 | X | X | | X |
| 4213 | X | | | |
| 4215 | X | X | X | X |
| 4217 | X | | | |
| 4218 | X | | | |

| Module | Used in | | | |
|---|---|---|---|---|
| | Tape Control 516 | Interface 520 | Interface 521 | Interface 522A |
| 4301 | | | | X |
| 4303 | X | | | X |
| 4304 | X | | | X |
| 4305 | X | | | |
| 4407 | X | | | |
| 4505* | | | | X |
| 4506 | | | | X |
| 4604 | X | | X | X |
| 4606 | X | | | |
| 4657 | X | | | |
| 4659 | | | | X |
| 4660* | | | | X |
| 6684 | X | | | |

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*Required only for systems using tape transports Type 7330.

## Component Spares

| Type | Quantity | | | |
|---|---|---|---|---|
| | Tape Control 516 | Interface 520 | Interface 521 | Interface 522A |
| D-668 | 11 | -- | 6 | 7 |
| DEC 2894-1 | 21 | 8 | 8 | 11 |
| DEC 2894-3 | 4 | -- | -- | -- |
| 1N276 | 18 | 13 | 11 | 14 |
| 1N645 | 24 | 12 | 13 | 16 |
| 1N748 - 3.9v | 4 | -- | -- | -- |
| 1N914 | 7 | 5 | 5 | 7 |
| 1N994 | 15 | 2 | 2 | 5 |
| 1N3208 | 6 | -- | -- | -- |
| 1N3605 | 5 | -- | 4 | 5 |
| 1N3606 | 28 | 14 | 12 | 15 |
| 2N393 | -- | -- | 6 | -- |
| 2N599 | 5 | -- | -- | -- |
| 2N1304 | 3 | 4 | 9 | 9 |
| 2N1305 | 10 | 9 | 11 | 12 |
| 2N1309 | 6 | -- | 4 | 8 |
| 2N1499 | 5 | -- | -- | 4 |
| 2N1499A | 12 | 6 | -- | 4 |
| 2N1754 | 4 | -- | -- | -- |
| 2N2451 | 3 | 4 | 4 | -- |
| 2N2714 | 6 | -- | 4 | 4 |
| 2N2904 | 4 | -- | -- | -- |
| 2N3009 | 5 | -- | -- | 4 |
| 16J1 | 24 | 11 | 13 | 16 |

## Mechanical Spares

| Part Number and Description | Quantity |
|---|---|
| 53E168, Type CFG: Rotron fan with #2R blade | 1 |
| X-1431, 10' x 10" x 2" EZ Kleen Filter | 1 |
| Type 418 Super Filter Coat, pints | 1 |

# CHAPTER 11

# INSTALLATION AND
# PREOPERATIONAL CHECK-OUT

## SITE SELECTION

Before installing the tape control and interface, select a suitable location near the PDP-6 arithmetic processor. The tape control and interface should be located within 25 feet of the processor, and the tape transports should be located within 25 feet of the tape control.

The tape control and interface are located in a cabinet 69-1/2 inches high, 22-1/4 inches wide, and 27-1/8 inches deep. A 3-foot clearance should be allowed on all sides of the equipment for access during maintenance. A level floor is required because the equipment frames are mounted on casters. The floor should be capable of supporting 150 psf. The system is designed to operate efficiently from 50° to 100°F. The plug-in modules are cooled by blowing air out the front of the bay. No additional cooling equipment is required.

The tape control and interface run on ordinary 115-volt, 600 cycle current. A 10-ampere line is sufficient. The tape control power cable is equipped with a Hubble Twist-Loc 3-prong, 30-ampere, 250-volt plug. The same plug and cable also serve the interface. Although the tape control interface combination draws only 5 to 6 amperes in normal operation, turn-on surges may reach 9 amperes, and system power capacity should be planned accordingly.

## UNPACKING

The tape control and interface cabinet is shipped on a skid and may be crated or not, depending on the mode of transportation. For truck shipment, it may be left uncrated. A crate is furnished for air shipment. The crate is approximately 74 inches high, 27 inches wide, and 32 inches deep. The skid upon which it rests is about 6 inches high and 3 feet square. Interconnecting cables are specially made up for each installation and are ordinarily shipped with the equipment.
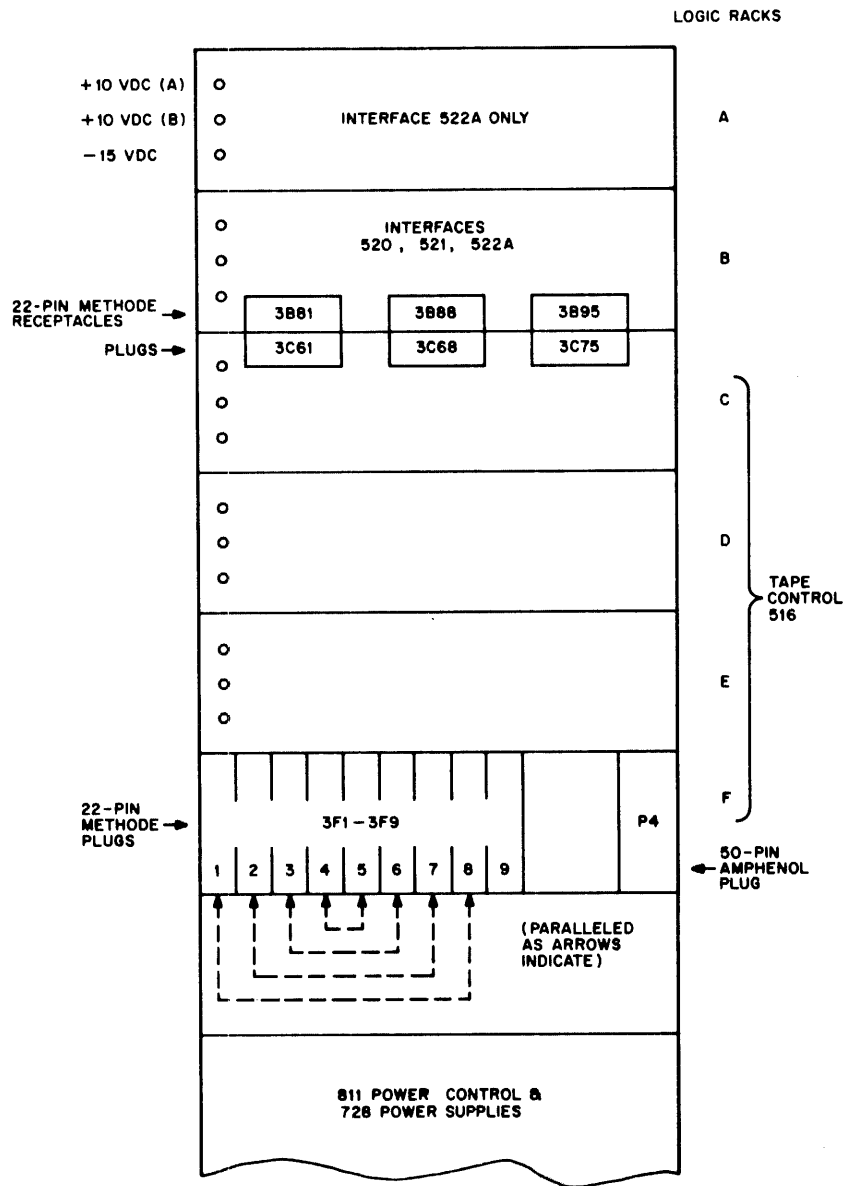
Figure 11-1   Front View Layout, Tape Control 516
and Interface 520, 521, or 522A

1. If the tape control and interface are crated, carefully remove all crating and strapping, and any packing material. If the unit is shipped uncrated, remove the skid and any protective padding.

2. The plenum doors at the rear of the bay have spring catches. To reinforce these doors during shipment, two bolts are used to hold each door shut. Remove these bolts and store them in the plastic loops provided.

3. Remove any packing material, shipping blocks, etc. from the inside of the tape control and interface cabinet.

4. The plug-in modules are taped into the logic panels to prevent damage in shipment. Remove the tape.

> NOTE: If the user plans to reship the equipment (or to move it
> more than a short distance) in the near future, special containers
> and packing materials should be saved for reuse. These items are
> designed especially to accommodate the equipment and are the
> safest means of packing it for reshipment.

## INSPECTION

The tape control and interface are thoroughly tested and checked before they leave the factory. However, both units should be inspected and checked again when installed to make sure that no damage has occurred during shipment. After the equipment is unpacked, check the following:

1. Have all the shipping blocks, packing materials, tape, etc. been removed? If not, remove them.

2. Are all plug-in units inserted firmly in position? Secure any that are loose.

3. Are there any loose nuts or bolts? If so, tighten them.

4. Are there any loose or broken wires? If so, repair them.

## CABLE CONNECTIONS

Complete the inspection procedure as given above before connecting the cables.

    1. Route the four cables from the PDP-6 processor into the cabinet, and connect the Methode receptacles at the ends of the processor cables to the corresponding Methode plugs at the left (viewed from front) of rack F. The four receptacles can be plugged in either to Methode plugs 3F1-3F4, or 3F5-3F8, depending on the layout of the specific installation. The plugs are paralleled as shown in Figure 11-1 and as listed in Table 11-1.

## CAUTION

It is essential that each of the four Methode receptacles be connected to the correct parallel pair of Methode plugs. The receptacles should each be marked with the correct plug position. If they are not so marked, check Table 11-1 to ensure that the correct connections are made.

TABLE 11-1   CABLE CONNECTIONS, METHODE PLUGS 3F1-3F9

| Plug Pair | Processor Signals |
|---|---|
| 3F1-3F8 | IOB2-17 |
| 3F2-3F7 | IOB18-35 |
| 3F3-3F6 | IOB CONO CLR, IOB CONO SET, IOB ⟵ STATUS, PIR0-7 |
| 3F4-3F5 | IOB RESET, DEVICE SELECT IOS3-9 |
| Plug | Data Control 136 Signals |
| 3F9 | RBB0(1)-(RBB5(1), DA0(1)-DA5(1), DA RQ B(1) |

    2. Route the cable from the Data Control 136 into the cabinet, and connect the Methode receptacle at the cable end to Methode plug 3F9.

3. Secure the tie-down brackets over all five Methode receptacles to prevent them from being accidentally loosened or dislodged.

4. Plug in and secure P4, the 50-pin Amphenol receptacle at the end of the cable from the tape transports (the corresponding plug is located at the right of rack F).

5. A coiled ac power cable is taped to the fan at the bottom of the bay. Remove the tape and route the power cable out through the hole in the bottom of the bay, but do not plug it in.

## POWER CONTROLS

To perform the preoperational check-out of the tape control and interface, the operator should be familiar with the controls described below.

### Power Control Type 834-836

There are two controls on this unit, a circuit breaker and a LOCAL/REMOTE switch. When the switch is in the LOCAL position, the processor has no effect on tape control and interface power turnon. Power can then be turned on or off by means of the circuit breaker. The LOCAL position is used primarily for maintenance purposes.

For normal operation, it is usually more convenient to leave the circuit breaker on and the switch in the REMOTE position. Tape control and interface power is then controlled by the processor. When the processor is turned on, power is also applied to the tape control and interface. If the circuit breaker is turned off, no power is applied to the tape control and interface regardless of the position of the LOCAL/REMOTE switch.

### MCV Switches

There are three MCV (Marginal Check Voltage) switches at the left of each logic rack. The top switch in each set governs the +10 vdc (A) power lines, the middle switch governs the +10 vdc (B) power lines, and the bottom switch governs the -15 vdc lines (see Figure 11-1). There are two independent +10 vdc supply lines, A and B; these lines are applied to different

circuits within the same modules. This arrangement is an aid to troubleshooting because it permits selective application of marginal check voltages. In the FIXED position (down), each MCV switch connects the associated logic rack to the fixed supply voltage from the internal 728 Power Supplies. In the MARGINAL position (up), each MCV switch connects the associated logic rack to the variable MCV voltage from the processor. This variable MCV voltage can be adjusted at the MCV controls over the operator's control panel of the PDP-6.

## PREOPERATIONAL CHECK-OUT

Before using the tape control and interface, make sure that the system turns on and off properly and that the correct voltages are present at all logic racks. The following check-out procedure should be carried out after completing the cable connections described under Cable Connections. All voltages are measured from chassis ground with a Multimeter (Simpson Model 260A, Triplett Model 630NA, or equivalent).

1. Put the LOCAL/REMOTE switch in LOCAL position.

2. Turn power circuit breaker OFF.

3. Plug in power cable to 110-volt ac outlet.

4. Put all MCV switches in FIXED position.

5. Turn power circuit breaker ON.

6. Check the fixed (internal) supply voltages at terminals A, B, and C of the module occupying the extreme right (viewed from the front) position of each logic rack.

| Terminal | Voltage |
|----------|---------|
| A | +10 vdc (A) |
| B | +10 vdc (B) |
| C | -15 vdc |

The +10-vdc fixed supply voltages should be between +9.5 vdc and +11.5 vdc. The −15 vdc should be between −14.5 vdc and −16.5 vdc. If either voltage falls outside the specified range, the 728 Power Supply probably needs maintenance.

11-6

7. With the PDP-6 processor turned off, put the LOCAL/REMOTE switch in the REMOTE position. Check each of the three fixed voltages at any of the terminals specified in step 6. No voltage should be present.

8. Turn on the PDP-6 processor. Again check the three fixed voltages. The same voltage noted in step 6 should be present at each of the three terminals checked.

9. Put the LOCAL/REMOTE switch in the LOCAL position.

10. Put the MCV switches that control the +10-vdc (A) lines (upper switch at the left of each logic rack) in the MARGINAL position.

11. Make the following settings at the MCV controls above the PDP-6 operator's control panel:

    a. Set polarity switch to +10-volt position.

    b. Adjust Variac until marginal check voltage meter indicates +5 vdc.

12. Check the +10-vdc (A) voltage at the terminals specified in step 6. It should coincide with the + 5-vdc voltage shown on the marginal check voltage meter.

13. Return the MCV switches for +10 vdc (A) to the FIXED position and set the MCV switches which control the +10-vdc (B) lines (middle switch at the left of each logic rack) to the MARGINAL position.

14. Check the +10-vdc (B) voltage at the terminals specified in step 6. It should coincide with the + 5-vdc voltage shown on the marginal check voltage meter.

15. Return the MCV switches for +10 vdc to the FIXED position.

16. At the PDP-6 MCV controls, set the MCV polarity switch to the −15 volt position and adjust the Variac until the marginal check voltage meter indicates − 8 vdc.

17. Set the MCV switches which control the −15-vdc lines (bottom switch at the left of each logic rack) to the MARGINAL position.

18. Check the −15-vdc voltage at the terminals specified in step 6. It should coincide with the −8-vdc voltage shown on the marginal check voltage meter.

19. Return the MCV switches for −15 vdc to the FIXED position.

20. Return the LOCAL/REMOTE switch to REMOTE.

21. Return the polarity switch at the PDP-6 to the off position.

22. Turn off the PDP-6.