IDENTIFICATION

PRODUCT CODE:	MAINDEC 12-D8CD-D
PRODUCT NAME:	KW12A CLOCK TEST
DATE CREATED:	DECEMBER 1,1971
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	RAYMOND SHOOP

KW12A

ANALOG MODE @ 4 MODE
CLOCK SOURCE TO LINE FREQ
THRESHOLD KNOBS TO MIDRANGE
L SW = 0000 , RSW = 0000
B MODE 10 PRINT START
RSW 06 = 1 INHIBIT TRAP PRINT

1.0 ABSTRACT

1.1 THE KW12 REAL TIME CLOCK TEST IS DESIGNED TO VERIFY THE CORRECT OPERATION OF THE BUFFER PRESET REGISTER, CLOCK COUNTER REGISTER, CLOCK CONTROL REGISTER, CLOCK ENABLE REGISTER, CLOCK I/O INTERFACE, EXTERNAL INPUT CHANNELS, AND FAST SAMPLE MODE (IF THE AD12 OPTION IS CONCURRENTLY INSTALLED.)

1.2 PROGRAM CONTROL IS MAINTAINED BY A MONITOR RESIDENT IN BANK 0, SEVERAL OPTIONS ARE AVAILABLE TO THE OPERATOR FOR ERROR HANDLING.

2.0 REQUIREMENTS:

2.1 EQUIPMENT:

A. A PDP-12 WITH KW12 INSTALLED.
B. AN AD12 ANALOG-TO DIGITAL CONVERTER IF FAST SAMPLE TESTING IS REQUIRED.
C. AN ASR-33 OR EQUIVALENT.

2.2 PRELIMINARY PROGRAMS

A. ALL CENTRAL PROCESSOR AND MEMORY DIAGNOSTIC PROGRAMS FOR A BASIC PDP-12 MUST BE ABLE TO RUN SUCCESSFULLY PRIOR TO TESTING THE KW12.

2.3 STORAGE:

A. 4K MINIMUM CORE.
B. PROGRAM OCCUPIES LOCATIONS 0000 TO 7600.

3.0 LOADING PROCEDURES

3.1 METHOD

LOAD THIS PROGRAM USING THE STANDARD METHOD OF LOADING A BINARY PROGRAM.

4.0 STARTING PROCEDURES

4.1 METHOD

A. SET THE MODE SWITHC TO 8 MODE.
B. SET THE LEFT SWITCHES TO 0000.
C. SET THE RIGHT SWITCHES TO THE DESIRED OPTIONS.
D. DEPRESS I/O PRESET.
E. DEPRESS START 20.
F. THE PROGRAM IS NOW RUNNING. THE TELETYPE BELL WILL RING AT THE END OF EACH PASS. IN ADDITION, THE CONTENTS OF THE PASS COUNTER WILL BY TYPED OUT.

ca 40 seconds

4.2 SWITCH SETTINGS

A. IF FAST SAMPLE TESTING IS TO BE ATTEMPTED, SET KNOB 0 FULLY COUNTERCLOCKWISE AND KNOB 1 FULLY CLOCKWISE.
B. SET THE SELECTOR SWITCHES ON THE FRONT PANEL TO LINE FREQUENCY.
C. SET THE INPUT LEVEL KNOBS TO MID-RANGE.
D. SELECT ANY DESIRED ERROR HANDLER OPTIONS. WITH RSW = 0000, THE FOLLOWING SEQUENCE WILL OCCUR FOR AN ERROR: (MESSAGE TYPEOUT,,ERROR HALT) THE OPERATOR SELECTS ANY FURTHER ERROR OPTIONS AND DEPRESSES CONTINUE.... (MONITOR EXECUTES NEXT SEQUENTIAL TEST)

RSW 00 = 1, INHIBIT ERROR HALT
RSW 01 = 1, INHIBIT ERROR PRINTOUT
RSW 02 = 1, SCOPE LOOP ON ERROR
RSW 03 = 1, SCOPE LOOP ON NON-FAILING TEST
RSW 04 = 1, INHIBIT FASST SAMPLE TESTING
RSW 05 = 1, INHIBIT BELL RINGING
RSW 06 = 1, INHIBIT PASS COUNTER PRINTOUT

5.0 ERROR ROUTINE

5.1 ERROR PRINTOUT

A. THE ERROR MESSAGES HAVE THE FOLLOWING GENERAL FORM:

TEST NO. TEST MESSAGE
REG1 REG2 REG3 ...

B. TEST NO. REFERS TO THE TEST NUMBER AS ORGANIZED IN THE LISTING. THIS IS INCLUDED TO AID THE OPERATOR IN FINDING THE TEST IN THE LISTING.

C. TEST MESSAGE IS THE BODY OF THE TEXT, DESCRIBING WHAT WAS TESTED, AND INDICATING ANY AREAS OF PROBABLE FAILURE.

D. REG1, REG2, REG3, ARE SPECIFIC DATA WORDS PERTAINING TO THE FAILURE.

3.2 ERROR MESSAGES

```
TST10 CLAB CHANGED AC
7741 7020
TST11 CLBA FAILED
0402 7020
TST12 CLAB FAILED
0402 7020
TST13 CLAB FAILED
7741 7020
TST14 CLAB FAILED
0402 7020
TST15 CLBA CHANGED BUFFER
0402 7020
TST16 CLAB <> CLBA FAILED
7741 7020
TST17 CLAB <> CLBA FAILED
0402 7020
TST18 CLAB <> CLBA FAILED
0402 7020
TST19 CLEN CHANGED AC
7741 7020
TST20 CLEN CHANGED BUFFER
7741 7020
TST21 CLCA FAILED
0402 7020
TST22 "CLR CNT" FAILED
0402 7020
TST23 CLEN FAILED
7741 7020
TST24 CLEN FAILED
0402 7020
TST25 CLCA CHANGES COUNT
0402 7020
TST26 BUFFER <> COUNTER FAILED
0402 7020
TST27 "LOAD CNT" FAILS TO "OR"
0402 7020
TST28 "LOAD CNT" LOADED IN ERROR
0402 7020
TST29 "LOAD CNT" LOADED IN ERROR
0402 7020
TST30 MODE REG CAUSES "LOAD CNT"
0402 7020
TST31 MODE REG CAUSES "LOAD CNT" OR "CLR BUF"
0402 7020 0000
TST32 MODE 2:  1>0 CLOCKED CNTR
0402 7020
TST33 MODE 2:  0>1 CLOCKED CNTR
0000 7020
TST34 O'FLO  FAILED TO SET O'FLO FLOP
TST35 CLSA FAILED TO CLEAR O'FLO FLOP
```

```
TST36 CLSK SKIPPED IN ERROR

TST37 ILLEGAL CLOCK INTERRUPT!

TST38 CLSK FAILED TO SKIP

TST39 CLOCK INTERRUPT FAILED

TST40 O'FLO ENABLE WON'T ZERO

TST41 O'FLO FLAG WON'T CLEAR

TST42 CLOCK INTR WON'T CLEAR

TST43 BIT 11 FAILED.
0402 7020
TST44 BIT 10 FAILED.
0402 7020
TST45 BIT 09 FAILED.
0402 7020
TST46 BIT 08 FAILED.
0402 7020
TST47 BIT 07 FAILED.
0402 7020
TST48 BIT 06 FAILED.
0402 7020
TST49 BIT 05 FAILED.
0402 7020
TST50 BIT 04 FAILED.
0402 7020
TST51 BIT 03 FAILED.
0402 7020
TST52 BIT 02 FAILED.
0402 7020
TST53 BIT 01 FAILED.
0402 7020
TST54 BIT 00 FAILED.
0402 7020
TST55 RATE 400KC FAILS

TST56 RATE 100KC FAILS

TST57 RATE 10KC FAILS

TST58 RATE 1KC FAILS

TST59 RATE 100CPS FAILS

TST60
CHAN 1 INPUT LOCKED OUT

TST61 CHAN 3 WON'T TOGGLE
0402 7020
TST62 CHAN 2 WON'T TOGGLE
0402 7020
TST63 CHAN 1 WON'T TOGGLE
0402 7020
TST64 CHAN 1 WON'T TOGGLE
```

TST65 CHAN 1 INTR IN ERROR

TST66 CHAN 2 WON'T INTR.
0402 7020
TST67 CHAN 2 INTR IN ERROR

TST68 CHAN 3 WON'T INTR.
0402 7020
TST69 CHAN 3 INTR IN ERROR

TST70 CHAN 3 INPUT LINE FREQ FAILED
7020
TST71 CHAN 2 INPUT LINE FREQ FAILED
7020
TST72 CHAN 1 INPUT LINE FREQ FAILED
7020
TST73 FAST SAM FAILS
0402 7020
TST74 O'FLO WON'T FAST SAO
0402 7020
TST75 FAST SAM WON'T SET
0402 7020
TST76 MODES 2-1 INHIBIT FAST SAM
0402 7020
TST77 RATE 10KC FAILS
0402
TST78 I/O PRESET WON'T STOP CLOCK
(RATE BITS 1 & 2)

TST79 1KC FAILS
0402

TST80 I/O PRSET WON'T STOP CLOCK
(RATE BIT 0)

TST81 I/O PRESET WON'T CLEAR O'FLO

TST82 I/O PRESET WON'T CLEAR INTERRUPT ENABLE

TST83 I/O PRESET WON'T CLEAR INPUTS

TST83 I/O PRESET WON'T CLEAR MODE 2

TST85 I/O PRESET WON'T CLEAR MODE 0

TST 86 FAST SAM NOT CLEARED

TST 87 CHAN 1 WON'T TRANS CNT TO BUF
0200
TST88 CHAN 2 WON'T TRANS CNT TO BUF
0200
TST89 CHAN 3 WON'T TRANS CNT TO BUF
0200
TST90 CHAN 1 WON'T TRANS CNT TO BUF
0300
TST91 CHAN 2 WON'T TRANS CNT TO BUF
0300
TST92 CHAN 3 WON'T TRANS CNT TO BUF

```
0300
TST93 CHA3 INPUT FAILED TO CLR CNT
7020

TST94 ECO EM12-00034 IS EITHER NOT WORKING OR NOT
      INSTALLED

TST95 ECO EM12-00055 IS EITHER NOT WORKING OR NOT
      INSTALLED PROPERLY

KW12 PASS=0000
```

```
                        /PDP-12 KW12A CLOCK TEST, MAINDEC 12-D8CD-L
                        /COPYRIGHT 1970, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
                        /THIS TEST IS DESIGNED TO VERIFY PROPER OPERATION
                        /OF THE KW-12A REAL TIME CLOCK AND TO DIAGNOSE
                        /MALFUNCTIONS IN REGISTERS, REGISTER TRANSFERS, IO
                        /BUS INTERFACE, AND EXTERNAL INPUT CHANNELS.
                        /
                        /AUTHORS: JAMES KELLY, STEVE TEICHER, HAROLD LONG
                        /RAYMOND SHOOP
                        /MAJOR START
                        /I/O PRESET & MODE
                        /SET LEFT SWITCHES TO 0000
                        /SET RIGHT SWITCHES TO DESIRED OPTIONS
                        /DEPRESS START 20
                        /
                        /SWITCH SETTINGS: (NORMALLY 0000)
                        /RSW 00=1, INHIBIT ERROR HALT
                        /RSW 01=1, INHIBIT ERROR PRINTOUT
                        /RSW 02=1, SCOPE LOOP ON FAILING TEST
                        /RSW 03=1, SCOPE LOOP ON NON-FAILING TEST
                        /RSW 04=1, INHIBIT FAST SAMPLE TESTING.
                        /RSW 05=1, INHIBIT BELL RINGING
                        /RSW 06=1, INHIBIT TEST COMPLETION ALARM
                        /
                        /SOME IOT DEFINITIONS:
                        /
6131    CLSK=6131                       /SKIP ON CLOCK INTERRUPT
6132    CLLR=6132                       /AC TO CLOCK CONTROL REGISTER
6133    CLAB=6133                       /AC TO BUFFER PRESET REGISTER
6134    CLEN=6134                       /AC TO CLOCK ENABLE REGISTER
6135    CLSA=6135                       /CLOCK STATUS TO AC, CLEAR STATUS FLIP-FLOPS
6136    CLBA=6136                       /BUFFER PRESET REGISTER TO AC
6137    CLCA=6137                       /COUNTER TO AC
                        /
0000    EXIT=0000                       /MESSAGE TERMINATOR
7777    EXITA=7777                      /MESSAGE SWITCH
4444    EXITB=4444                      /RESTART SWITCH
                        /
                        /SOME LINC PROGRAMMING DEFINITIONS:
                        /
6141    LINC=6141
0002    PDP=0002
0011    CLR=0011
0004    ESF=0004
0100    SAM0=0100
0101    SAM1=0101
1020    LDAI=1020
```

```
                0001    *1
0001    5451            JMP I   RETURN
                0010    *10
0010    0000    PINT,   0
                0020    *20
0020    5177    JMP     177                     /MAJOR START 8 MODE
                /
                /PAGE 0 REGISTERS AND CROSS-PAGE TAGS
                /
0021    5200    BELL,   BELLS
0022    1561    DN43,   BK43
0023    2362    DN55,   BK55
0024    0000    CNTR,   0000
0025    5020    ERROR,  ERRORS
0026    0000    LSTERR, 0000
0027    5000    NERROR, NERROS
0030    5051    OUTPAS, ASCII
0031    0000    PASS,   0000
0032    1425    PNTA,   LOCA
0033    1457    PNTB,   LOCB
0034    1527    PNTC,   LOCC
0035    2720    PNTD,   LOCD
0036    2742    PNTE,   LOCE
0037    2763    PNTF,   LOCF
0040    3005    PNTG,   LOCG
0041    3027    PNTH,   LOCH
0042    3051    PNTI,   LOCI
0043    4307    PNTJ,   LOCJ
0044    5210    RANDOM, RANDY
0045    0000    REGA,   0000
0046    0000    REGB,   0000
0047    0000    REGC,   0000
0050    0000    REGT,   0000
0051    0000    RETURN, 0000
0052    0000    RXED,   0000
0053    0000    SEND,   0000
0054    5252    SET,    SETN
0055    0000    SPACE,  0000
0056    1342    TST35N, TST35-2
0057    2753    TST66N, TST66
0060    3313    TST75N, TST75
0061    3375    TST77N, TST77
0062    3436    TST79N, TST79
0063    4040    TST90N, TST90
0064    5243    TYPE,   TYPOUT
0065    1572    UP43,   FD43
0066    2201    UP51,   FD51
0067    2372    UP55,   FD55
0070    2617    UP61,   FD61
```

```
                        /
                        /PAGE 0 CONSTANTS
                        /
0071  0000    K0000,  0000
0072  0001    K0001,  0001
0073  0002    K0002,  0002
0074  0003    K0003,  0003
0075  0004    K0004,  0004
0076  0007    K0007,  0007
0077  0010    K0010,  0010
0100  0014    K0014,  0014
0101  0017    K0017,  0017
0102  0020    K0020,  0020
0103  0037    K0037,  0037
0104  0040    K0040,  0040
0105  0060    K0060,  0060
0106  0077    K0077,  0077
0107  0100    K0100,  0100
0110  0177    K0177,  0177
0111  0200    K0200,  0200
0112  0240    K240,   0240
0113  0300    K0300,  0300
0114  0377    K0377,  0377
0115  0400    K0400,  0400
0116  0500    K0500,  0500
0117  0600    K0600,  0600
0120  0700    K0700,  0700
0121  0777    K0777,  0777
0122  1000    K1000,  1000
0123  1026    K1026,  1026
0124  1777    K1777,  1777
0125  2000    K2000,  2000
0126  3000    K3000,  3000
0127  3777    K3777,  3777
0130  4000    K4000,  4000
0131  4100    K4100,  4100
0132  5100    K5100,  5100
0133  5252    K5252,  5252
0134  5555    K5555,  5555
0135  6000    K6000,  6000
0136  7774    K7774,  7774
```

```
                        /
                        /PAGE 0 NEGATIVE CONSTANTS
                        /
0137  7777      M0001,  -1
0140  7776      M0002,  -2
0141  7774      M0004,  -4
0142  7770      M0010,  -10
0143  7760      M0020,  -20
0144  7740      M0040,  -40
0145  7736      M0042,  -42
0146  7700      M0100,  -100
0147  7600      M0200,  -200
0150  7400      M0400,  -400
0151  7000      M1000,  -1000
0152  6400      M1400,  -1400
0153  6000      M2000,  -2000
0154  4000      M4000,  -4000
0155  3334      M4444,  -4444
0156  2400      M5400,  -5400

                        /GENERATE AN PROGRAM I-O POWER CLEAR

0157  0000      CLAR,   0
0160  6141              LINC                    /CHANGE TO LINC MODE
0161  1020              LDAI                    /LOAD AC WITH 20
0162  0020        .     0020                    /
0163  0004              ESF                     /I-O POWER CLEAR
0164  0002              PDP
0165  7200              CLA
0166  5557              JMP I   CLAR            /EXIT

      4157      CLEAR=JMS       CLAR
```

```
                0176    *176
0176  7410              SKP                     /RESTART ADDRESS; DON'T CLEAR COUNTERS
0177  4454              JMS I   SET             /RESET BUFFERS
                0200    *200
                        /MAJOR START 8 MODE, AC=0
                        /TEST BUFFER AND PRESET REGISTER DATA INTERCHANGE
                        /CLAB=6133  AC TO CLOCK PRESET REGISTER
                        /CLBA=6136  CLOCK PRESET REGISTER TO AC
                        /
                        /DOES AC CHANGE AFTER A TRANSFER TO BUFFER REG?
                        /
0200  4421              JMS I   BELL            /RING BELL
0201  7300      TST10,  CLA CLL                 /CLEAR AC
0202  1045              TAD     REGA            /GET A NUMBER=BINARY UPCOUNT SEQUENCE 0 THRU 7777
0203  6133              CLAB                    /LOAD BUFFER
0204  3052              DCA     RXED            /STORE WHAT WAS LEFT IN AC
0205  1052              TAD     RXED            /FETCH IT
0206  7041              CIA                     /INVERT CONTENTS OF AC
0207  1045              TAD     REGA            /SUBTRACT SEND
0210  7650              SNA CLA                 /EQUAL?
0211  4427              JMS I   NERROR          /CHECK MONITOR
0212  4425              JMS I   ERROR           /CLAB CHANGED AC.
0213  5261              TST10M                  /MESSAGE POINTER
0214  7402              HLT                     /ERROR HALT
0215  7610              SKP CLA                 /TO NEXT TEST
0216  0201              TST10                   /ISZ LOOP; SCOPE LOOP
                        /
                        /DOES BUFFER DATA JAM INTO THE AC?
                        /
0217  7300      TST11,  CLA CLL                 /CLEAR AC
0220  3053              DCA     SEND            /0 SEND REG
0221  6133              CLAB                    /SET BUFFER AND PRESET REGISTER TO 0000
0222  7240              CLA CMA                 /SET AC TO 7777
0223  6136              CLBA                    /JAM BUFFER PRESET (0000) OVER AC (7777
0224  3052              DCA     RXED            /SAVE AC
0225  1052              TAD     RXED            /RESTORE AC
0226  7650              SNA CLA                 /DID AC BECOME (0000)?
0227  4427              JMS I   NERROR          /CHECK MONITOR
0230  4425              JMS I   ERROR           /CLBA FAILED TO JAM THE AC
0231  5301              TST11M                  /MESSAGE POINTER
0232  7402              HLT                     /ERROR HALT
0233  7610              SKP CLA                 /TO NEXT TEST
0234  0217              TST11                   /ISZ LOOP; SCOPE LOOP
```

```
                        /
                        /DOES THE AC JAM INTO THE BUFFER?
                        /
0235  7240     TST12,   CLA CMA                 /SET AC=7777
0236  6133              CLAB                    /SET BUFF=7777
0237  7300              CLA CLL                 /CLEAR AC
0240  6133              CLAB                    /LOAD BUFFER TO ALL ZEROS
0241  3053              DCA      SEND           /SAVE AC
0242  6136              CLBA                    /READ BUFFER AND PRESET REGISTER
0243  3052              DCA      RXED           /SAVE TEST VALUE
0244  1052              TAD      RXED           /RESTORE IT
0245  7650              SNA CLA                 /DID BUFFER AND PRESET REGISTER GET CLEARED
0246  4427              JMS I    NERROR         /CHECK MONITOR
0247  4425              JMS I    ERROR          /AC JAM INTO BUFFER FAILED
0250  5317              TST12M                  /MESSAGE POINTER
0251  7402              HLT                     /ERROR HALT
0252  7610              SKP CLA                 /TO NEXT TEST
0253  0235              TST12                   /ISZ LOOP; SCOPE LOOP
                        /
                        /DO ALL NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY?
                        /
0254  7300     TST13,   CLA CLL                 /CLEAR AC
0255  1045              TAD      REGA           /GET TEST NUMBER
0256  6133              CLAB                    /SEND IT
0257  7200              CLA                     /CLEAR AC
0260  6136              CLBA                    /RETRIEVE IT
0261  3052              DCA      RXED           /SAVE IT
0262  1052              TAD      RXED           /RESTORE IT
0263  7041              CIA                     /COMPLEMENT
0264  1045              TAD      REGA           /ADD TEST NUMBER
0265  7650              SNA CLA                 /WERE THEY EQUAL?
0266  4427              JMS I    NERROR         /CHECK MONITOR
0267  4425              JMS I    ERROR          /AC - BUFFER TO AC DATA TRANSFER FAILED
0270  5335              TST13M                  /MESSAGE POINTER
0271  7402              HLT                     /ERROR HALT
0272  7610              SKP CLA                 /TO NEXT TEST
0273  0254              TST13                   /ISZ LOOP; SCOPE LOOP
```

```
                        /
                        /DO RANDOM NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY?
                        /
0274  4444    TST14,    JMS I   RANDOM          /LOAD BUFFER AND PRESET REGISTER WITH A RANDOM NUMBER
0275  3053              DCA     SEND            /SAVE IT
0276  1053              TAD     SEND            /RESTORE IT
0277  6133              CLAB                    /SEND IT
0300  4444              JMS I   RANDOM          /LOAD THE AC WITH A RANDOM NUMBER
0301  6136              CLBA                    /READ BACK RANDOM NUMBER FROM BUFFER PRESET REGISTER
0302  3052              DCA     RXED            /SAVE TEST RETURN
0303  1052              TAD     RXED            /RESTORE IT
0304  7041              CIA                     /COMPLEMENT
0305  1053              TAD     SEND            /SUBTRACT TEST NUMBER
0306  7650              SNA CLA                 /EQUAL?
0307  4427              JMS I   NERROR          /CHECK MONITOR
0310  4425              JMS I   ERROR           /AC - BUFFER - AC DATA INTERCHANGE FAILED
0311  5353              TST14M                  /MESSAGE POINTER
0312  7402              HLT                     /ERROR HALT
0313  7610              SKP CLA                 /TO NEXT TEST
0314  0274              TST14                   /ISZ LOOP; SCOPE LOOP
                        /
                        /DOES READING THE BUFFER CHANGE ITS CONTENTS?
                        /
0315  4444    TST15,    JMS I   RANDOM          /GET RANDOM NUMBER
0316  3053              DCA     SEND            /SAVE IT
0317  1053              TAD     SEND            /RESTORE IT
0320  6133              CLAB                    /SEND IT
0321  4444              JMS I   RANDOM          /LOAD AC WITH A RANDOM NUMBER
0322  6136              CLBA                    /BRING BACK TEST NUMBER
0323  4444              JMS I   RANDOM          /LOAD AC WITH A RANDOM NUMBER
0324  6136              CLBA                    /READ BUFFER AGAIN
0325  3052              DCA     RXED            /SAVE TEST VALUE
0326  1052              TAD     RXED            /RESTORE IT
0327  7041              CIA                     /COMPLEMENT
0330  1053              TAD     SEND            /SUBTRACT TEST NUMBER
0331  7650              SNA CLA                 /EQUAL
0332  4427              JMS I   NERROR          /CHECK MONITOR
0333  4425              JMS I   ERROR           /CLBA CHANGED THE CONTENTS OF THE BUFFER
0334  5371              TST15M                  /MESSAGE POINTER
0335  7402              HLT                     /ERROR HALT
0336  7610              SKP CLA                 /TO NEXT TEST
0337  0315              TST15                   /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /CAN THE GATES FUNCTION AT HIGH SPEED?
                    /
0340  7300  TST16,  CLA CLL                 /CLEAR AC
0341  1045        TAD     REGA            /GET TEST NUMBER
0342  6133        CLAB                    /SEND IT
0343  6136        CLBA                    /GET IT
0344  6133        CLAB
0345  6136        CLBA
0346  6133        CLAB
0347  6136        CLBA
0350  6133        CLAB
0351  6136        CLBA
0352  6133        CLAB
0353  6136        CLBA
0354  6133        CLAB
0355  6136        CLBA
0356  6133        CLAB
0357  6136        CLBA
0360  6133        CLAB
0361  6136        CLBA
0362  6133        CLAB
0363  6136        CLBA
0364  6133        CLAB
0365  6136        CLBA
0366  6133        CLAB                    /SEND IT
0367  6136        CLBA                    /GET IT
0370  3052        DCA     RXED            /SAVE IT
0371  1052        TAD     RXED            /FETCH IT
0372  7041        CIA                     /2'S COMPLEMENT
0373  1045        TAD     REGA            /COMPARE
0374  7650        SNA CLA                 /EQUAL?
0375  4427        JMS I   NERROR         /CHECK MONITOR
0376  4425        JMS I   ERROR          /BUF FAILED TO TOGGLE AT HIGH SPEED
0377  5413        TST16M                  /MESSAGE POINTER
0400  7402        HLT                     /ERROR HALT
0401  7610        SKP CLA                 /TO NEXT TEST
0402  0340        TST16                   /ISZ LOOP; SCOPE LOOP
```

```
                        /
                        /CAN THE BUFFER SURVIVE CHECKERBOARD?
                        /
0403  7300      TST17,  CLA CLL                 /CLEAR AC
0404  1133              TAD     K5252           /GET TEST PATTERN
0405  3053              DCA     SEND            /SAVE TEST PATTERN
0406  1053              TAD     SEND            /RESTORE IT
0407  6133              CLAB                    /SEND IT
0410  6136              CLBA                    /GET IT
0411  7040              CMA
0412  6133              CLAB
0413  6136              CLBA
0414  7040              CMA
0415  6133              CLAB
0416  6136              CLBA
0417  7040              CMA
0420  6133              CLAB
0421  6136              CLBA
0422  7040              CMA
0423  6133              CLAB
0424  6136              CLBA
0425  7040              CMA
0426  6133              CLAB
0427  6136              CLBA
0430  7040              CMA
0431  6133              CLAB
0432  6136              CLBA
0433  7040              CMA
0434  6133              CLAB
0435  6136              CLBA
0436  7040              CMA
0437  6133              CLAB
0440  6136              CLBA
0441  7040              CMA
0442  6133              CLAB
0443  6136              CLBA
0444  7040              CMA
0445  6133              CLAB
0446  6136              CLBA
0447  7040              CMA
0450  6133              CLAB
0451  6136              CLBA                    /SEND IT
0452  7040              CMA                     /GET IT
0453  3052              DCA     RXED            /SAVE FINAL PATTERN
0454  1052              TAD     RXED            /RESTORE IT
0455  7041              CIA                     /COMPLEMENT
0456  1053              TAD     SEND            /SUBTRACT TEST PATTERN
0457  7650              SNA CLA                 /EQUAL?
0460  4427              JMS I   NERROR          /CHECK MONITOR
0461  4425              JMS I   ERROR           /BUFFER FAILED CHECKBOARD TEST
0462  5434              TST17M                  /MESSAGE POINTER
0463  7402              HLT                     /ERROR HALT
0464  7610              SKP CLA                 /TO NEXT TEST
0465  0403              TST17                   /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /CAN THE BUFFER SURVIVE RANDOM COMPLEMENT PATTERNS?
                    /
0466  4444  TST18,  JMS I   RANDOM          /GENERATE A RANDOM NUMBER
0467  3053        DCA      SEND            /SAVE IT
0470  1053        TAD      SEND            /RESTORE IT
0471  6133        CLAB                     /SEND IT
0472  6136        CLBA                     /GET IT
0473  7040        CMA
0474  6133        CLAB
0475  6136        CLBA
0476  7040        CMA
0477  6133        CLAB
0500  6136        CLBA
0501  7040        CMA
0502  6133        CLAB
0503  6136        CLBA
0504  7040        CMA
0505  6133        CLAB
0506  6136        CLBA
0507  7040        CMA
0510  6133        CLAB
0511  6136        CLBA
0512  7040        CMA
0513  6133        CLAB
0514  6136        CLBA
0515  7040        CMA
0516  6133        CLAB
0517  6136        CLBA
0520  7040        CMA
0521  6133        CLAB
0522  6136        CLBA
0523  7040        CMA
0524  6133        CLAB
0525  6136        CLBA
0526  7040        CMA
0527  6133        CLAB
0530  6136        CLBA
0531  7040        CMA
0532  6133        CLAB
0533  6136        CLBA                     /SEND IT
0534  7040        CMA                      /GET IT
0535  3052        DCA      RXED            /SAVE FINAL PATTERN
0536  1052        TAD      RXED            /RESTORE IT
0537  7041        CIA                      /COMPLEMENT
0540  1053        TAD      SEND            /SUBTRACT TEST PATTERN
0541  7650        SNA CLA                  /EQUAL?
0542  4427        JMS I    NERROR          /CHECK MONITOR
0543  4425        JMS I    ERROR           /BUFFER FAILED RANDOM COMPLEMENT PATTERN
0544  5455        TST18M                   /MESSAGE POINTER
0545  7402        HLT                      /ERROR HALT
0546  7610        SKP CLA                  /TO NEXT TEST
0547  0466        TST18                    /ISZ LOOP; SCOPE LOOP
```

```
                        /
                        /CLEN=6134 AC TO CLOCK ENABLE REGISTER
                        /DOES CLEN AFFECT THE AC?
                        /
0550  7300    TST19,    CLL CLA                 /CLEAR AC
0551  1045              TAD     REGA            /RESTORE TEST NUMBER
0552  6134              CLEN                    /DOES CLEN AFFECT AC
0553  3052              DCA     RXED            /SAVE AC
0554  1052              TAD     RXED            /RESTORE IT
0555  7041              CIA                     /COMPLEMENT
0556  1045              TAD     REGA            /SUBTRACT TEST NUMBER
0557  7650              SNA CLA                 /EQUAL?
0560  4427              JMS I   NERROR          /CHECK MONITOR
0561  4425              JMS I   ERROR           /AC TO CLOCK ENABLE REG CHANGED AC
0562  5476              TST19M                  /MESSAGE POINTER
0563  7402              HLT                     /ERROR HALT
0564  7610              SKP CLA                 /TO NEXT TEST
0565  0550              TST19                   /ISZ LOOP; SCOPE LOOP
                        /
                        /PRESET REGISTER AND COUNTER DATA INTERCHANGE
                        /CLSA=6135 STATUS REGISTER TO AC
                        /CLLR=6132 AC TO CLOCK CONTROL REGISTER
                        /
                        /DOES BUFFER CHANGE AFTER A TRANSFER TO THE COUNTER?
                        /
0566  7300    TST20,    CLL CLA                 /CLEAR AC
0567  6135              CLSA                    /CLEAR STATUS
0570  7300              CLA CLL                 /CLEAR AC
0571  1045              TAD     REGA            /RESTORE TEST NUMBER
0572  6133              CLAB                    /LOAD BUFFER PRESET REGISTER WITH A BINARY UPCOUNT NUMBER
0573  7300              CLA CLL                 /CLEAR AC
0574  6132              CLLR                    /STOP CLOCK, SET ALL MODES=0
0575  1107              TAD     K0100           /MODE CONTROL REG BIT 2=1
0576  6132              CLLR                    /SET MODE 2, ENABLING CLR LOAD CNT
0577  7200              CLA                     /CLEAR AC
0600  1111              TAD     K0200           /AC BIT 4=1, SIMULATE CLR OFLOW ON 6134
0601  6134              CLEN                    /TRANSER PRESET COUNT TO CLOCK COUNTER
0602  6136              CLBA                    /READ THE BUFFER
0603  3052              DCA     RXED            /SAVE IT
0604  1052              TAD     RXED            /RESTORE IT
0605  7041              CIA                     /COMPLEMENT
0606  1045              TAD     REGA            /SUBTRACT TEST NUMBER
0607  7650              SNA CLA                 /EQUAL?
0610  4427              JMS I   NERROR          /CHECK MONITOR
0611  4425              JMS I   ERROR           /TRANSFER FROM BUFFER TO COUNTER CHANGES BUFFER
0612  5516              TST20M                  /MESSAGE POINTER
0613  7402              HLT                     /ERROR HALT
0614  7610              SKP CLA                 /TO NEXT TEST
0615  0570              TST20+2                 /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /DOES COUNTER DATA JAM THE BUFFER AND AC?
                    /CLCA=6137 CLOCK COUNTER TO PRESET REGISTER, THEN PRESET REG TO AC
                    /
0616  6135  TST21,  CLSA                    /CLEAR STATUS
0617  7300          CLA CLL                 /CLEAR AC
0620  6133          CLAB                    /LOAD BUFFER TO 0000
0621  6132          CLLR                    /STOP CLOCK, SET ALL MODES=0
0622  1107          TAD     K0100           /SET AC 05=1
0623  6132          CLLR                    /SET MODE 2=1, THEREBY CLEARING CLOCK COUNTER
0624  6134          CLEN                    /ENABLE INTERRUPT ON OVERFLOW
0625  7240          CLA CMA                 /SET AC 7777
0626  3053          DCA     SEND            /SAVE IT
0627  1053          TAD     SEND            /FETCH IT
0630  6133          CLAB                    /SET BUFFER 7777
0631  6137          CLCA                    /READ COUNTER
0632  3052          DCA     RXED            /SAVE COUNT
0633  1052          TAD     RXED            /RESTORE IT
0634  7650          SNA CLA                 /ZERO?
0635  4427          JMS I   NERROR          /CHECK MONITOR
0636  4425          JMS I   ERROR           /COUNTER FAILED TO JAM 0000 INTO 7777
0637  5540          TST21M                  /MESSAGE POINTER
0640  7402          HLT                     /ERROR HALT
0641  7610          SKP CLA                 /TO NEXT TEST
0642  0616          TST21                   /ISZ LOOP; SCOPE LOOP
                    /
                    /DOES SIGNAL CLR CNT WORK
                    /
0643  6135  TST22,  CLSA                    /CLEAR STATUS
0644  7350          CLA CMA CLL RAR         /SET AC=3777
0645  3053          DCA     SEND            /SAVE AC
0646  1053          TAD     SEND            /FETCH IT
0647  6133          CLAB                    /SET BUFFER TO 3777 (USE 3777 SO WE DON'T SET OVERFLOW FLOP)
0650  7300          CLA CLL                 /CLEAR AC
0651  1111          TAD     K0200           /ENABLE LOAD COUNT GATES
0652  6134          CLEN                    /LOAD COUNTER TO 3777 (GENERATE LOAD CNT)
0653  7300          CLA CLL                 /CLEAR AC
0654  6132          CLLR                    /ZERO MODE 2
0655  1107          TAD     K0100           /SET AC 05=1
0656  6132          CLLR                    /SET MODE 2, THEREBY GENERATING "CLC CLR CNT"
0657  7300          CLA CLL                 /CLEAR AC
0660  6137          CLCA                    /READ THE COUNTER
0661  3052          DCA     RXED            /SAVE IT
0662  1052          TAD     RXED            /RESTORE IT
0663  7650          SNA CLA                 /ZERO?
0664  4427          JMS I   NERROR          /CHECK MONITOR
0665  4425          JMS I   ERROR           /CLR CNT FAILED TO CLEAR THE COUNTER FROM 3777 TO 0000
0666  5556          TST22M                  /MESSAGE POINTER
0667  7402          HLT                     /ERROR HALT
0670  7610          SKP CLA                 /TO NEXT TEST
0671  0643          TST22                   /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /DO ALL NUMBERS TRANSFER BETWEEN THE BUFFER AND COUNTER?
                    /
0672  6135    TST23,  CLSA                    /CLEAR STATUS
0673  7300            CLA CLL                 /CLEAR AC
0674  1045            TAD     REGA            /LOAD AC WITH TEST NUMBER
0675  6133            CLAB                    /SET BUFFER TO TEST NUMBER
0676  7300            CLA CLL                 /CLEAR AC
0677  6132            CLLR                    /STOP CLOCK, SET ALL MODES=0
0700  1107            TAD     K0100           /SET AC 05=1
0701  6132            CLLR                    /GENERATE "CLR CNT"
0702  7200            CLA                     /CLEAR AC
0703  1111            TAD     K0200           /SET AC 04=1
0704  6134            CLEN                    /GENERATE "LOAD CNT"
0705  6137            CLCA                    /COUNTER TO AC
0706  3052            DCA     RXED            /SAVE IT
0707  1052            TAD     RXED            /RESTORE IT
0710  7041            CIA                     /COMPLEMENT
0711  1045            TAD     REGA            /SUBTRACT TEST NUMBER
0712  7650            SNA CLA                 /EQUAL?
0713  4427            JMS I   NERROR          /CHECK WITH MONITOR
0714  4425            JMS I   ERROR           /BUFFER TO COUNTER DATA INTERCHANGE FAILED
0715  5576            TST23M                  /MESSAGE POINTER
0716  7402            HLT                     /ERROR HALT
0717  7610            SKP CLA                 /TO NEXT TEST
0720  0672            TST23                   /ISZ LOOP; SCOPE LOOP
```

```
                        /
                        /DO RANDOM NUMBERS TRANSFER BETWEEN BUFFER AND COUNTER?
                        /
0721  4444    TST24,    JMS I   RANDOM          /GET RANDOM NUMBER
0722  6133              CLAB                    /LOAD BUFFER RANDOM
0723  3053              DCA     SEND            /SAVE TEST NUMBER
0724  6135              CLSA                    /CLEAR CLOCK STATUS
0725  7200              CLA                     /CLEAR AC
0726  6132              CLLR                    /STOP CLOCK, SET ALL MODES=0
0727  1107              TAD     K0100           /SET AC 05=1
0730  6132              CLLR                    /GENERATE "CLR CNT"
0731  7200              CLA                     /CLEAR AC
0732  1111              TAD     K0200           /SET AC 04=1
0733  6134              CLEN                    /GENERATE "LOAD CNT"
0734  4444              JMS I   RANDOM          /GET RANDOM NUMBER
0735  6133              CLAB                    /LOAD BUFFER RANDOM
0736  4444              JMS I   RANDOM          /LOAD AC RANDOM
0737  6137              CLCA                    /READ COUNTER
0740  3052              DCA     RXED            /SAVE TEST VALUE
0741  1052              TAD     RXED            /RESTORE IT
0742  7041              CIA                     /COMPLEMENT
0743  1053              TAD     SEND            /SUBTRACT TEST NUMBER
0744  7650              SNA CLA                 /EQUAL?
0745  4427              JMS I   NERROR          /CHECK MONITOR
0746  4425              JMS I   ERROR           /BUFFER TO COUNTER RANDOM DATA INTERCHANGE FAILED
0747  5614              TST24M                  /MESSAGE POINTER
0750  7402              HLT                     /ERROR HALT
0751  7610              SKP CLA                 /TO NEXT TEST
0752  0721              TST24                   /ISZ LOOP; SCOPE LOOP
```

```
                        /
                        /DOES READING THE COUNTER CHANGE ITS STATE?
                        /
0753  4444    TST25,    JMS I   RANDOM          /GET RANDOM TEST NUMBER
0754  6133              CLAB                    /SEND IT TO BUFFER
0755  3053              DCA     SEND            /SAVE IT
0756  6132              CLLR                    /STOP CLOCK, SET ALL MODES=0
0757  1107              TAD     K0100           /SET AC 05=1
0760  6132              CLLR                    /GENERATE "CLR CNT"
0761  6135              CLSA                    /CLEAR CLOCK STATUS
0762  7200              CLA                     /CLEAR AC
0763  1111              TAD     K0200           /SET AC 04=1
0764  6134              CLEN                    /GENERATE "LOAD CNT"
0765  4444              JMS I   RANDOM          /GET RANDOM NUMBER
0766  6133              CLAB                    /SEND IT TO BUFFER
0767  4444              JMS I   RANDOM          /GET RANDOM NUMBER
0770  6137              CLCA                    /READ CLOCK COUNTER
0771  4444              JMS I   RANDOM          /GET RANDOM NUMBER
0772  6133              CLAB                    /SEND IT TO BUFFER
0773  4444              JMS I   RANDOM          /GET RANDOM NUMBER
0774  6137              CLCA                    /READ CLOCK COUNTER
0775  3052              DCA     RXED            /SAVE IT
0776  1052              TAD     RXED            /RESTORE IT
0777  7041              CIA                     /COMPLEMENT
1000  1053              TAD     SEND            /SUBTRACT TEST NUMBER
1001  7650              SNA CLA                 /EQUAL?
1002  4427              JMS I   NERROR          /CHECK MONITOR
1003  4425              JMS I   ERROR           /(CLCA) READ THE COUNTER CHANGES THE COUNTERS STATE
1004  5632              TST25M                  /MESSAGE POINTER
1005  7402              HLT                     /ERROR HALT
1006  7610              SKP CLA                 /TO NEXT TEST
1007  0753              TST25                   /ISZ LOOP; SCOPE LOOP
1010  7340              CLA CLL CMA             /SET AC=7777
1011  3045              DCA     REGA            /PRESET COUNTER FOR NEXT TEST
```

```
                    /
                    /CAN THE BUF TO COUNTER AND COUNTER TO BUF FUNCTION AT HIGH SPEED?
                    /
1012  4444  TST26,  JMS I   RANDOM          /GET RANDOM NUMBER
1013  6133          CLAB                    /SEND IT TO BUFFER
1014  3053          DCA     SEND            /SAVE IT
1015  7200          CLA                     /CLEAR AC
1016  6132          CLLR                    /STOP CLOCK
1017  1107          TAD     K0100           /SET AC 05=1
1020  6132          CLLR                    /GENERATE "CLR CNT"
1021  6135          CLSA                    /CLEAR CLOCK STATUS
1022  7200          CLA                     /CLEAR AC
1023  1111          TAD     K0200           /SET AC 04=1
1024  6134          CLEN                    /GENERATE "LOAD CNT"
1025  6137          CLCA                    /READ COUNTER
1026  2046          ISZ     REGB            /DONE?
1027  5215          JMP     TST26+3         /BACK TO START 4096 TIMES
1030  3052          DCA     RXED            /SAVE FINAL NUMBER
1031  1052          TAD     RXED            /RESTORE IT
1032  7041          CIA                     /COMPLEMENT
1033  1053          TAD     SEND            /SUBTRACT TEST NUMBER
1034  7650          SNA CLA                 /EQUAL?
1035  4427          JMS I   NERROR         /CHECK MONITOR
1036  4425          JMS I   ERROR          /THE BUFFER COUNTER BUFFER DATA INTERCHANGE FAILED AT HIGH SPEED
1037  5653          TST26M                  /MESSAGE POINTER
1040  7402          HLT                     /ERROR HALT
1041  7610          SKP CLA                 /TO NEXT TEST
1042  1012          TST26                   /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /DOES (LOAD CNT) PERFORM LOGIC OR?
                    /
1043  7300  TST27,  CLA CLL                 /CLEAR AC
1044  6132        CLLR                    /STOP CLOCK
1045  1107        TAD     K0100           /SET AC 05=1
1046  6132        CLLR                    /GENERATE "CLR CNT"
1047  6135        CLSA                    /CLEAR CLOCK STATUS
1050  4444        JMS I   RANDOM          /GET RANDOM TEST NUMBER
1051  6133        CLAB                    /LOAD BUFFER WITH A RANDOM NUMBER
1052  3053        DCA     SEND            /SAVE IT
1053  1111        TAD     K0200           /SET AC 04=1
1054  6134        CLEN                    /LOAD COUNTER FROM THE BUFFER REGISTER; GENERATE "LOAD CNT"
1055  7300        CLA CLL                 /CLEAR AC
1056  1053        TAD     SEND            /GET TEST NUMBER
1057  7040        CMA                     /COMPLEMENT
1060  6133        CLAB                    /LOAD BUFFER WITH THE COMPLEMENT OF THE PREVIOUS NUMBER
1061  7300        CLA CLL                 /CLEAR AC
1062  1111        TAD     K0200           /SET AC 04=1
1063  6134        CLEN                    /LOAD COUNTER (OR) IN COMPLEMENT OF THE FIRST NUMBER
1064  6137        CLCA                    /READ COUNTER,
1065  3052        DCA     RXED            /SAVE IT
1066  1052        TAD     RXED            /RESTORE IT
1067  7040        CMA                     /CONVERT TO ALL ZEROS FOR TESTING
1070  7650        SNA CLA                 /ZERO?
1071  4427        JMS I   NERROR          /CHECK MONITOR
1072  4425        JMS I   ERROR           /THE (LOAD CNT) SIGNAL FAILED TO "OR" DATA INTO COUNTER
1073  5676        TST27M                  /MESSAGE POINTER
1074  7402        HLT                     /ERROR HALT
1075  7610        SKP CLA                 /TO NEXT TEST
1076  1043        TST27                   /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 2 (0)
                    /
1077  7300  TST28, CLA CLL                 /CLEAR AC
1100  6133        CLAB                    /CLEAR BUFFER
1101  6132        CLLR                    /CLEAR ALL MODES
1102  1107        TAD     K0100           /SET AC 05=1
1103  6132        CLLR                    /GEN. "CLR CNT"
1104  6135        CLSA                    /CLEAR STATUS
1105  4444        JMS I   RANDOM          /GET RANDOM NUMBER
1106  6133        CLAB                    /SEND IT TO BUFFER
1107  3053        DCA     SEND            /SAVE IT
1110  6132        CLLR                    /STOP CLOCK, SET ALL MODES=0
1111  1107        TAD     K0100           /SET AC 05=1
1112  6132        CLLR                    /GENERATE "CLR CNT"
1113  7200        CLA                     /CLEAR AC
1114  6132        CLLR                    /SET ALL MODES=0
1115  1111        TAD     K0200           /SET AC 04=1
1116  6134        CLEN                    /TRY TO GENERATE "LOAD CNT"
1117  6137        CLCA                    /GET COUNTER
1120  3052        DCA     RXED            /SAVE IT
1121  1052        TAD     RXED            /RESTORE IT
1122  7650        SNA CLA                 /WAS IT ZERO?
1123  4427        JMS I   NERROR         /CHECK MONITOR
1124  4425        JMS I   ERROR          /LOAD CNT GATES FUNCTIONED WITH MODE 2=0 IN ERROR
1125  5722        TST28M                  /MESSAGE POINTER
1126  7402        HLT                     /ERROR HALT
1127  7610        SKP CLA                 /TO NEXT TEST
1130  1077        TST28                   /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 1(1)
                    /
1131  4444  TST29,  JMS I   RANDOM          /GET RANDOM NUMBER
1132  6133          CLAB                    /SEND IT TO BUFFER
1133  3053          DCA     SEND            /SAVE IT
1134  1117          TAD     K0600           /SET AC 04,05=1
1135  6132          CLLR                    /GENERATE "CLR CNT", SET MODE 1 AND 2 =1
1136  6135          CLSA                    /CLEAR CLOCK STATUS
1137  7200          CLA                     /CLEAR AC
1140  1111          TAD     K0200           /SET AC 04=1
1141  6134          CLEN                    /TRY TO GENERATE "LOAD CNT"
1142  6137          CLCA                    /READ COUNTER
1143  3052          DCA     RXED            /SAVE TEST VALUE
1144  1052          TAD     RXED            /RESTORE IT
1145  7650          SNA CLA                 /ZERO?
1146  4427          JMS I   NERROR          /CHECK MONITOR
1147  4425          JMS I   ERROR           /LOAD CNT GATES FUNCTIONED WITH MODE 1=1 IN ERROR
1150  5747          TST29M                  /MESSAGE POINTER
1151  7402          HLT                     /ERROR HALT
1152  7610          SKP CLA                 /TO NEXT TEST
1153  1131          TST29                   /ISZ LOOP; SCOPE LOOP
1154  7340          CLA CLL CMA             /SET AC=7777
1155  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /GLITCH TEST OF LOAD CNT GATES
                    /
1156  4444  TST30,  JMS I   RANDOM          /GET RANDOM NUMBER
1157  6133          CLAB                    /SEND IT TO BUFFER
1160  3053          DCA     SEND            /SAVE IT
1161  1111          TAD     K0200           /SET AC 04=1
1162  6132          CLLR                    /SET MODE 1=1
1163  7200          CLA                     /CLEAR AC
1164  1113          TAD     K0300           /SET AC 04,05=1
1165  6132          CLLR                    /SET MODE 2=1
1166  7200          CLA                     /CLEAR AC
1167  2046          ISZ     REGB            /DONE?
1170  5361          JMP     .-7             /BACK 4096 TIMES
1171  6137          CLCA                    /READ COUNTER
1172  3052          DCA     RXED            /SAVE IT
1173  1052          TAD     RXED            /RESTORE IT
1174  7650          SNA CLA                 /ZERO?
1175  4427          JMS I   NERROR          /CHECK MONITOR
1176  4425          JMS I   ERROR           /THE MODE REGISTER CAUSES ILLEGAL LOAD COUNTER
1177  5774          TST30M                  /MESSAGE POINTER
1200  7402          HLT                     /ERROR HALT
1201  7200          CLA                     /TO NEXT TEST
1202  1156          TST30                   /ISZ LOOP; SCOPE LOOP
1203  7340          CLA CLL CMA             /SET AC=7777
1204  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /GENERAL GATE SHAKING TEST OF THE MODE FLIP FLOPS
                    /
1205  4444  TST31,  JMS I   RANDOM          /GET RANDOM NUMBER
1206  6133          CLAB                    /SEND IT TO BUFFER
1207  3053          DCA     SEND            /SAVE IT
1210  1046          TAD     REGB            /GET TEST COUNTER
1211  7006          RTL                     /ROTATE TWO LEFT
1212  7006          RTL                     /ROTATE TWO LEFT
1213  7006          RTL                     /ROTATE TWO LEFT
1214  0120          AND     K0700           /INSURE THAT MODE 0,1,2=1
1215  6132          CLLR                    /SEND RANDOM NUMBER TO CONTROL REGISTER
1216  7040          CMA                     /COMPLEMENT
1217  0120          AND     K0700           /INSURE THAT MODE 0,1,2=1
1220  6132          CLLR                    /SET TO COMPLEMENT OF THE NUMBER
1221  2046          ISZ     REGB            /DONE?
1222  5210          JMP     TST31+3         /BACK 4096 TIMES
1223  6136          CLBA                    /GET TEST VALUE FROM BUFFER
1224  3052          DCA     RXED            /SAVE IT
1225  1052          TAD     RXED            /RESTORE IT
1226  7041          CIA                     /COMPLEMENT
1227  1053          TAD     SEND            /SUBTRACT TEST NUMBER
1230  7640          SZA CLA                 /EQUAL?
1231  5237          JMP     .+6             /BUFF CHANGED IN ERROR
1232  6137          CLCA                    /READ COUNTER
1233  3046          DCA     REGB            /SAVE IT
1234  1046          TAD     REGB            /RESTORE IT
1235  7650          SNA CLA                 /STILL ZERO?
1236  4427          JMS I   NERROR          /CHECK MONITOR
1237  4425          JMS I   ERROR           /COUNTER CHANGED IN ERROR
1240  6021          TST31M                  /MESSAGE POINTER
1241  7402          HLT                     /ERROR HALT
1242  7200          CLA                     /TO NEXT TEST
1243  1205          TST31                   /ISZ LOOP; SCOPE LOOP
1244  3046          DCA     REGB            /CLEAR FOR NEXT ISZ LOOP
```

```
                        /
                        /DOES MODE 2 1-0 CLK CNT?
                        /
1245  4444  TST32,  JMS I   RANDOM          /GET RANDOM NUMBER
1246  6133           CLAB                   /SEND IT TO BUFFER
1247  3053           DCA     SEND           /SAVE IT
1250  6132           CLLR                   /ZERO MODE 2
1251  1107           TAD     K0100          /AC 05=1
1252  6132           CLLR                   /GENERATE "CLR CNT"
1253  6135           CLSA                   /CLEAR STATUS
1254  7200           CLA                    /CLEAR AC
1255  1111           TAD     K0200          /SET AC 04=1
1256  6134           CLEN                   /GENERATE "LOAD CNT"
1257  7200           CLA                    /CLEAR AC
1260  6132           CLLR                   /0 MODE 2
1261  6137           CLCA                   /READ COUNTER
1262  3052           DCA     RXED           /SAVE IT
1263  6133           CLAB                   /CLEAR BUF OR OVERFLOW WILL RELOAD CNT
1264  1052           TAD     RXED           /RESTORE IT
1265  7041           CIA                    /COMPLEMENT
1266  1053           TAD     SEND           /SUBTRACT TEST NUMBER
1267  7650           SNA CLA                /EQUAL?
1270  4427           JMS I   NERROR         /CHECK MONITOR
1271  4425           JMS I   ERROR          /MODE 2 1-0 DID IT
1272  6056           TST32M                 /MESSAGE POINTER
1273  7402           HLT                    /ERROR HALT
1274  7410           SKP                    /TO NEXT TEST
1275  1245           TST32                  /ISZ LOOP; SCOPE LOOP
                        /
                        /DOES MODE 2 0-1 CLOCK CNT?
                        /
1276  1107  TST33,  TAD     K0100          /SET AC 05=1
1277  6132           CLLR                   /GENERATE "CLR CNT"
1300  6137           CLCA                   /READ COUNTER
1301  3052           DCA     RXED           /SAVE IT
1302  1052           TAD     RXED           /RESTORE IT
1303  7650           SNA CLA                /ZERO?
1304  4427           JMS I   NERROR         /CHECK MONITOR
1305  4425           JMS I   ERROR          /MODE 2 0-1 FAILED
1306  6102           TST33M                 /MESSAGE POINTER
1307  7402           HLT                    /ERROR HALT
1310  7410           SKP                    /TO NEXT TEST
1311  1276           TST33                  /ISZ LOOP; SCOPE LOOP
1312  7340           CLA CLL CMA            /SET AC=7777
1313  3045           DCA     REGA           /PRESET ISZ COUNT
1314  5715           JMP I   .+1
1315  1542           TST43                  /NEXT TEST
```

```
                    /
                    /DOES COUNTER OVERFLOW SET OVERFLOW FLOP?
                    /
1316  7300  TST34,  CLA CLL                  /CLEAR AC
1317  6132         CLLR                     /CLEAR STATUS
1320  1107         TAD      K0100           /SET AC 05=1
1321  6132         CLLR                     /0 TO COUNTER
1322  6135         CLSA                     /CLEAR CLOCK STATUS
1323  7340         CLA CLL CMA              /SET AC=7777
1324  6133         CLAB                     /SET BUFFER TO 7777
1325  7300         CLA CLL                  /CLEAR AC
1326  1111         TAD      K0200           /SET AC 04=1
1327  6134         CLEN                     /LOAD CNT (00)=1
1330  4157         CLEAR                    /GENERATE I-O PRESET
1331  6135         CLSA                     /GET STATUS OF CLOCK
1332  7710         SPA CLA                  /OVERFLOW SET?
1333  4427         JMS I    NERROR          /CHECK MONITOR
1334  4425         JMS I    ERROR           /OVERFLOW NOT SET
1335  6126         TST34M                   /MESSAGE POINTER
1336  7402         HLT                      /ERROR HALT
                                            / OR ECO EM12=55 IS NOT WORKING PROPERLY
1337  7410         SKP                      /TO NEXT TEST
1340  1316         TST34                    /ISZ LOOP; SCOPE LOOP
1341  7340         CLA CLL CMA              /SET AC=7777
1342  3046         DCA      REGB            /PRESET ISZ COUNTER FOR NEXT TEST
1343  3045         DCA      REGA            /RESET REGA
```

```
                    /
                    /DOES CLSA (6135) CLEAR OVERFLOW FLOP?
                    /
1344  7300  TST35, CLA CLL                 /CLEAR AC
1345  6132        CLLR                    /CLEAR ALL MODES
1346  1107        TAD     K0100           /SET AC 05=1
1347  6132        CLLR                    /GEN "CLR CNT"
1350  6135        CLSA                    /CLEAR CLOCK STATUS
1351  7340        CLA CLL CMA             /SET AC=7777
1352  6133        CLAB                    /SET BUF=7777 OCTAL
1353  7300        CLA CLL                 /CLEAR AC
1354  1111        TAD     K0200           /SET AC 04=1
1355  6134        CLEN                    /GEN LOAD CNT
1356  4157        CLEAR                   /GENERATE I-O PRESET
1357  6135        CLSA                    /GET STATUS BIT 0=1
1360  7300        CLA CLL
1361  6135        CLSA                    /GET STATUS BIT 0=0
1362  7700        SMA CLA                 /OVERFLOW SET?
1363  4427        JMS I   NERROR          /CHECK MONITOR
1364  4425        JMS I   ERROR           /CLSA FAILED TO CLEAR OVERFLOW FLOP
1365  6152        TST35M                  /MESSAGE POINTER
1366  7402        HLT                     /ERROR HALT
1367  7410        SKP                     /TO NEXT TEST
1370  1344        TST35                   /ISZ LOOP; SCOPE LOOP
1371  7340        CLA CLL CMA             /SET AC=7777
1372  3045        DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                        /
                        /TEST OVERFLOW SKIP
                        /
1373  7300      TST36,  CLA CLL                 /CLEAR AC
1374  6132              CLLR                    /CLEAR ALL MODES
1375  1107              TAD     K0100           /SET AC 05=1
1376  6132              CLLR                    /GEN "CLR CNT"
1377  6135              CLSA                    /CLEAR CLOCK STATUS
1400  7340              CLA CLL CMA             /SET AC=7777
1401  6133              CLAB                    /SET BUF=7777 OCTAL
1402  7300              CLA CLL                 /CLEAR AC
1403  1111              TAD     K0200           /SET AC 04=1
1404  6134              CLEN                    /GEN LOAD CNT
1405  4157              CLEAR                   /GENERATE I-O PRESET
1406  6131              CLSK                    /OVERFLOW SET?
1407  4427              JMS I   NERROR          /CHECK MONITOR
1410  4425              JMS I   ERROR           /CLOCK PRESET DIDN'T 0 OVERFLOW ENABLE
1411  6177              TST36M                  /MESSAGE POINTER
1412  7402              HLT                     /ERROR HALT
1413  7410              SKP                     /TO NEXT TEST
1414  1373              TST36                   /ISZ LOOP; SCOPE LOOP
1415  7340              CLA CLL CMA             /SET AC=7777
1416  3045              DCA     REGA            /RESET REGA FOR NEXT TEST
                        /
                        /TEST FOR NO INTERRUPT
                        /
1417  1032      TST37,  TAD     PNTA            /GET RETURN POINTER TO LOCA
1420  3051              DCA     RETURN          /PUT IT IN INTERRUPT HANDLER
1421  6001              ION                     /ENABLE INTERRUPTS
1422  7000              NOP                     /WAIT
1423  6002              IOF                     /DISABLE INTERRUPTS
1424  4427              JMS I   NERROR          /CHECK MONTIOR
1425  4425      LOCA,   JMS I   ERROR           /ILLEGAL INTERRUPT OVERFLOW=1 OVERFLOW ENABLE=0
1426  6217              TST37M                  /MESSAGE POINTER
1427  7402              HLT                     /ERROR HALT
1430  7410              SKP                     /TO NEXT TEST
1431  1417              TST37                   /ISZ LOOP; SCOPE LOOP
1432  7340              CLA CLL CMA             /SET AC=7777
1433  3045              DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /SET INT ENABLE
                    /
1434  1107  TST38,  TAD      K0100          /SET AC 05=1
1435  6134         CLEN                    /TURN ON CLOCK OVERFLOW INT
1436  7300         CLA CLL                 /CLEAR AC
1437  6131         CLSK                    /INTERRUPT SET?
1440  7410         SKP                     /TO HERE IF INTERRUPT NOT SET
1441  4427         JMS I    NERROR         /CHECK MONITOR
1442  4425         JMS I    ERROR          /CLSK FAILED TO SKIP OVERFLOW=1 EN OVF INT=1
1443  6240         TST38M                  /MESSAGE POINTER
1444  7402         HLT                     /ERROR HALT
1445  7410         SKP                     /TO NEXT TEST
1446  1434         TST38                   /ISZ LOOP; SCOPE LOOP
1447  7340         CLA CLL CMA             /SET AC=7777
1450  3045         DCA      REGA           /PRESET REGA FOR NEXT TEST
                    /
                    /TEST FOR CLOCK INTERRUPT
                    /
1451  1033  TST39,  TAD      PNTB           /GET RETURN POINTER TO LOCB
1452  3051         DCA      RETURN         /PUT IT IN INTERRUPT HANDLER
1453  6001         ION                     /ENABLE INTERRUPTS
1454  7000         NOP                     /WAIT
1455  6002         IOF                     /DISABLE INTERRUPTS
1456  7410         SKP                     /TO HERE IF NO INTERRUPT
1457  4427  LOCB,  JMS I    NERROR         /CHECK WITH MONITOR
1460  4425         JMS I    ERROR          /CLOCK INT FAILED TO INTERRUPT
1461  6257         TST39M                  /MESSAGE POINTER
1462  7402         HLT                     /ERROR HALT
1463  7410         SKP                     /TO NEXT TEST
1464  1451         TST39                   /ISZ LOOP; SCOPE LOOP
1465  7340         CLA CLL CMA             /SET AC=7777
1466  3045         DCA      REGA           /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /TEST WITH FLAG UP ZERO OVERFLOW INT ENABLE
                    /
1467  7300  TST40,  CLA CLL                  /CLEAR AC
1470  6134          CLEN                    /0 CLOCK ENABLE
1471  6131          CLSK                    /INTERRUPT AVAILABLE?
1472  4427          JMS I   NERROR          /CHECK MONITOR
1473  4425          JMS I   ERROR           /OVERFLOW ENABLE WON'T ZERO
1474  6277          TST40M                  /MESSAGE POINTER
1475  7402          HLT                     /ERROR HALT
1476  7410          SKP                     /TO NEXT TEST
1477  1467          TST40                   /ISZ LOOP; SCOPE LOOP
1500  7340          CLL CLA CMA             /SET AC=7777
1501  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
                    /
                    /TEST WITH FLAG ZERO OVERFLOW SET
                    /
1502  1107  TST41,  TAD     K0100           /SET AC 05=1
1503  6134          CLEN                    /ENABLE INTERRUPTS
1504  7300          CLA CLL                 /CLEAR AC
1505  6132          CLLR                    /STOP THE CLOCK
1506  6135          CLSA                    /READ AND ZERO FLAG
1507  7300          CLA CLL                 /CLEAR AC
1510  6131          CLSK                    /INTERRUPT SET?
1511  4427          JMS I   NERROR          /CHECK MONITOR
1512  4425          JMS I   ERROR           /BAD INTERRUPT CONDITION STILL EXIST'S
1513  6320          TST41M                  /MESSAGE POINTER
1514  7402          HLT                     /ERROR HALT
1515  7410          SKP                     /TO NEXT TEST
1516  1502          TST41                   /ISZ LOOP; SCOPE LOOP
1517  7340          CLA CLL CMA             /SET AC=7777
1520  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
                    /
                    /TEST INT OVERFLOW=0
                    /
1521  1034  TST42,  TAD     PNTC            /GET RETURN POINTER TO LOCC
1522  3051          DCA     RETURN          /PUT IT IN INTERRUPT HANDLER
1523  6001          ION                     /ENABLE INTERRUPTS
1524  7000          NOP                     /WAIT
1525  6002          IOF                     /DISABLE INTERRUPTS
1526  4427          JMS I   NERROR          /CHECK MONITOR
1527  4425  LOCC,   JMS I   ERROR           /ILLEGAL CLOCK INTERRUPT
1530  6340          TST42M                  /MESSAGE POINTER
1531  7402          HLT                     /ERROR HALT
1532  7410          SKP                     /TO NEXT TEST
1533  1521          TST42                   /ISZ LOOP; SCOPE LOOP
1534  2046          ISZ     REGB            /INCREMENT PASS COUNTER
1535  5456          JMP I TST35N            /CROSS-PAGE TO TEST 35 4096 TIMES
1536  7340          CLA CLL CMA             /SET AC=7777
1537  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
1540  5741          JMP I   .+1
1541  2354          TST55                   /NEXT TEST
```

```
                    /
                    /COUNTER CARRY TESTING
                    /COUNTER PRESET SUCH THAT CLOCK CNT RAISES BIT IN QUESTION
                    /
                    /DOES BIT 11 SET UP?
                    /
1542  7200  TST43,  CLA                     /CLEAR AC
1543  6132          CLLR                    /CLEAR ALL MODES
1544  6133          CLAB                    /CLEAR BUF
1545  1107          TAD     K0100           /SET AC 05=1
1546  6132          CLLR                    /GEN "CLR CNT"
1547  6135          CLSA                    /CLEAR STATUS
1550  7200          CLA                     /CLEAR AC
1551  3024          DCA     CNTR            /CLEAR COUNTER
1552  3053          DCA     SEND            /CLEAR SEND
1553  6133          CLAB                    /CLEAR BUFFER
1554  1111          TAD     K0200           /MODE 1
1555  6134          CLEN                    /ENABLE MODE
1556  7300          CLA CLL                 /CLEAR AC
1557  1132          TAD     K5100           /SELECT 100 HZ RATE TO BE USED IN TST 43 TO TST 54
1560  6132          CLLR                    /ENABLE RATE
1561  6137  BK43,   CLCA                    /READ COUNTER
1562  3052          DCA     RXED            /SAVE IT
1563  1052          TAD     RXED            /FETCH IT
1564  1137          TAD     M0001           /BIT 11 AND ONLY BIT 11 SET?
1565  7650          SNA CLA                 /IF NOT, WAIT A WHILE
1566  5465          JMP I   UP43            /SET; GO CHECK MONITOR (.+4)
1567  2024          ISZ     CNTR            /TIMER DONE?
1570  5422          JMP I   DN43            /NO, GO BACK (.-7)
1571  7410          SKP                     /TO HERE IF BAD BIT
1572  4427  FD43,   JMS I   NERROR          /CHECK MONITOR
1573  4425          JMS I   ERROR           /BIT 11 FAILED TO GET SET BY A CLOCK PULSE
1574  6360          TST43M                  /MESSAGE POINTER
1575  7402          HLT                     /ERROR HALT
1576  7410          SKP                     /TO NEXT TEST
1577  1542          TST43                   /ISZ LOOP; SCOPE LOOP
1600  7340          CLA CLL CMA             /SET AC=7777
1601  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 10 SET UP?
                    /
1602  7200  TST44,  CLA
1603  6132         CLLR
1604  6133         CLAB
1605  6132         CLLR
1606  6135         CLSA
1607  7200         CLA
1610  3024         DCA     CNTR
1611  1072         TAD     K0001          /PRESET FOR BIT 10
1612  6133         CLAB
1613  3053         DCA     SEND
1614  1111         TAD     K0200
1615  6134         CLEN
1616  7300         CLA CLL
1617  1132         TAD     K5100
1620  6132         CLLR
1621  6137         CLCA
1622  3052         DCA     RXED
1623  1052         TAD     RXED
1624  1140         TAD     M0002          /BIT 10, AND ONLY BIT 10, SET?
1625  7650         SNA CLA
1626  5232         JMP     .+4
1627  2024         ISZ     CNTR
1630  5221         JMP     .-7
1631  7410         SKP
1632  4427         JMS I   NERROR         /CHECK MONITOR
1633  4425         JMS I   ERROR          /BIT 10 FAILED TO GET SET BY COUNTING
1634  6377         TST44M                 /MESSAGE POINTER
1635  7402         HLT                    /ERROR HALT
1636  7410         SKP                    /TO NEXT TEST
1637  1602         TST44                  /ISZ LOOP; SCOPE LOOP
1640  7340         CLA CLL CMA            /SET AC=7777
1641  3045         DCA     REGA           /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 9 SET UP?
                    /
1642  7200  TST45, CLA
1643  6132        CLLR
1644  6133        CLAB
1645  1107        TAD     K0100
1646  6132        CLLR
1647  6135        CLSA
1650  7200        CLA
1651  3024        DCA     CNTR
1652  1074        TAD     K0003           /PRESET FOR BIT 09
1653  6133        CLAB
1654  3053        DCA     SEND
1655  1111        TAD     K0200
1656  6134        CLEN
1657  7300        CLA CLL
1660  1132        TAD     K5100
1661  6132        CLLR
1662  6137        CLCA
1663  3052        DCA     RXED
1664  1052        TAD     RXED
1665  1141        TAD     M0004           /BIT 09, AND ONLY BIT 09, SET?
1666  7650        SNA CLA
1667  5273        JMP     .+4
1670  2024        ISZ     CNTR
1671  5262        JMP     .-7
1672  7410        SKP
1673  4427        JMS I   NERROR          /CHECK MONITOR
1674  4425        JMS I   ERROR           /BIT 9 FAILED TO GET SET BY COUNTING
1675  6416        TST45M                  /MESSAGE POINTER
1676  7402        HLT                     /ERROR HALT
1677  7410        SKP                     /TO NEXT TEST
1700  1642        TST45                   /ISZ LOOP; SCOPE LOOP
1701  7340        CLA CLL CMA             /SET AC=7777
1702  3045        DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 8 SET UP?
                    /
1703  7200  TST46,   CLA
1704  6132          CLLR
1705  6133          CLAB
1706  1107          TAD     K0100
1707  6132          CLLR
1710  6135          CLSA
1711  7200          CLA
1712  3024          DCA     CNTR
1713  1076          TAD     K0007           /PRESET FOR BIT 08
1714  6133          CLAB
1715  3053          DCA     SEND
1716  1111          TAD     K0200
1717  6134          CLEN
1720  7300          CLA CLL
1721  1132          TAD     K5100
1722  6132          CLLR
1723  6137          CLCA
1724  3052          DCA     RXED
1725  1052          TAD     RXED
1726  1142          TAD     M0010           /BIT 08, AND ONLY BIT 08, SET?
1727  7650          SNA CLA
1730  5334          JMP     .+4
1731  2024          ISZ     CNTR
1732  5323          JMP     .-7
1733  7410          SKP
1734  4427          JMS I   NERROR          /CHECK MONITOR
1735  4425          JMS I   ERROR           /BIT 8 FAILED TO GET SET BY COUNTING
1736  6435          TST46M                  /MESSAGE POINTER
1737  7402          HLT                     /ERROR HALT
1740  7410          SKP                     /TO NEXT TEST
1741  1703          TST46                   /ISZ LOOP; SCOPE LOOP
1742  7340          CLA CLL CMA             /SET AC=7777
1743  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 7 SET UP?
                    /
1744  7200  TST47, CLA
1745  6132        CLLR
1746  6133        CLAB
1747  1107        TAD     K0100
1750  6132        CLLR
1751  6135        CLSA
1752  7200        CLA
1753  3024        DCA     CNTR
1754  1101        TAD     K0017           /PRESET FOR BIT 07
1755  6133        CLAB
1756  3053        DCA     SEND
1757  1111        TAD     K0200
1760  6134        CLEN
1761  7300        CLA CLL
1762  1132        TAD     K5100
1763  6132        CLLR
1764  6137  BK47, CLCA
1765  3052        DCA     RXED
1766  1052        TAD     RXED
1767  1143        TAD     M0020           /BIT 07, AND ONLY BIT 07, SET?
1770  7650        SNA CLA
1771  5375        JMP     .+4
1772  2024        ISZ     CNTR
1773  5364        JMP     .-7
1774  7410        SKP
1775  4427        JMS I   NERROR          /CHECK MONITOR
1776  4425        JMS I   ERROR           /BIT 7 FAILED TO GET SET BY COUNTING
1777  6454        TST47M                  /MESSAGE POINTER
2000  7402        HLT                     /ERROR HALT
2001  7410        SKP                     /TO NEXT TEST
2002  1744        TST47                   /ISZ LOOP; SCOPE LOOP
2003  7340        CLA CLL CMA             /SET AC=7777
2004  3045        DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                        /
                        /DOES BIT 6 SET UP?
                        /
2005  7200    TST48,    CLA
2006  6132              CLLR
2007  6133              CLAB
2010  1107              TAD     K0100
2011  6132              CLLR
2012  6135              CLSA
2013  7200              CLA
2014  3024              DCA     CNTR
2015  1103              TAD     K0037           /PRESET FOR BIT 06
2016  6133              CLAB
2017  3053              DCA     SEND
2020  1111              TAD     K0200
2021  6134              CLEN
2022  7300              CLA CLL
2023  1132              TAD     K5100
2024  6132              CLLR
2025  6137              CLCA
2026  3052              DCA     RXED
2027  1052              TAD     RXED
2030  1144              TAD     M0040           /BIT 06, AND ONLY BIT 06, SET?
2031  7650              SNA CLA
2032  5236              JMP     .+4
2033  2024              ISZ     CNTR
2034  5225              JMP     .-7
2035  7410              SKP
2036  4427              JMS I   NERROR          /CHECK MONITOR
2037  4425              JMS I   ERROR           /BIT 6 FAILED TO GET SET BY COUNTING
2040  6473              TST48M                  /MESSAGE POINTER
2041  7402              HLT                     /ERROR HALT
2042  7410              SKP                     /TO NEXT TEST
2043  2005              TST48                   /ISZ LOOP: SCOPE LOOP
2044  7340              CLA CLL CMA             /SET AC=7777
2045  3045              DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 5 SET UP?
                    /
2046  7200  TST49, CLA
2047  6132        CLLR
2050  6133        CLAB
2051  1107        TAD     K0100
2052  6132        CLLR
2053  6135        CLSA
2054  7200        CLA
2055  3024        DCA     CNTR
2056  1106        TAD     K0077           /PRESET FOR BIT 05
2057  6133        CLAB
2060  3053        DCA     SEND
2061  1111        TAD     K0200
2062  6134        CLEN
2063  7300        CLA CLL
2064  1132        TAD     K5100
2065  6132        CLLR
2066  6137        CLCA
2067  3052        DCA     RXED
2070  1052        TAD     RXED
2071  1146        TAD     M0100           /BIT 05, AND ONLY BIT 05, SET?
2072  7650        SNA CLA
2073  5277        JMP     .+4
2074  2024        ISZ     CNTR
2075  5266        JMP     .-7
2076  7410        SKP
2077  4427        JMS I   NERROR          /CHECK MONITOR
2100  4425        JMS I   ERROR           /BIT 5 FAILED TO GET SET BY COUNTING
2101  6512        TST49M                  /MESSAGE POINTER
2102  7402        HLT                     /ERROR HALT
2103  7410        SKP                     /TO NEXT TEST
2104  2046        TST49                   /ISZ LOOP; SCOPE LOOP
2105  7340        CLA CLL CMA             /SET AC=7777
2106  3045        DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                        /
                        /DOES BIT 4 SET UP?
                        /
2107  7200      TST50,  CLA
2110  6132              CLLR
2111  6133              CLAB
2112  1107              TAD     K0100
2113  6132              CLLR
2114  6135              CLSA
2115  7200              CLA
2116  3024              DCA     CNTR
2117  1110              TAD     K0177           /PRESET FOR BIT 04
2120  6133              CLAB
2121  3053              DCA     SEND
2122  1111              TAD     K0200
2123  6134              CLEN
2124  7300              CLA CLL
2125  1132              TAD     K5100
2126  6132              CLLR
2127  6137              CLCA
2130  3052              DCA     RXED
2131  1052              TAD     RXED
2132  1147              TAD     M0200           /BIT 04, AND ONLY BIT 04, SET?
2133  7650              SNA CLA
2134  5340              JMP     .+4
2135  2024              ISZ     CNTR
2136  5327              JMP     .-7
2137  7410              SKP
2140  4427              JMS I   NERROR          /CHECK MONITOR
2141  4425              JMS I   ERROR           /BIT 4 FAILED TO GET SET BY COUNTING
2142  6531              TST50M                  /MESSAGE POINTER
2143  7402              HLT                     /ERROR HALT
2144  7410              SKP                     /TO NEXT TEST
2145  2107              TST50                   /ISZ LOOP; SCOPE LOOP
2146  7340              CLA CLL CMA             /SET AC=7777
2147  3045              DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 3 SET UP?
                    /
2150  7200  TST51,  CLA
2151  6132          CLLR
2152  6133          CLAB
2153  1107          TAD     K0100
2154  6132          CLLR
2155  6135          CLSA
2156  7200          CLA
2157  3024          DCA     CNTR
2160  1114          TAD     K0377           /PRESET FOR BIT 03
2161  6133          CLAB
2162  3053          DCA     SEND
2163  1111          TAD     K0200
2164  6134          CLEN
2165  7300          CLA CLL
2166  1132          TAD     K5100
2167  6132          CLLR
2170  6137          CLCA
2171  3052          DCA     RXED
2172  1052          TAD     RXED
2173  1150          TAD     M0400           /BIT 03, AND ONLY BIT 03, SET?
2174  7650          SNA CLA
2175  5466          JMP I   UP51            /(.+4)
2176  2024          ISZ     CNTR
2177  5370          JMP     .-7
2200  7410          SKP
2201  4427  FD51,   JMS I   NERROR          /CHECK MONITOR
2202  4425          JMS I   ERROR           /BIT 3 FAILED TO GET SET BY COUNTING
2203  6550          TST51M                  /MESSAGE POINTER
2204  7402          HLT                     /ERROR HALT
2205  7410          SKP                     /TO NEXT TEST
2206  2150          TST51                   /ISZ LOOP; SCOPE LOOP
2207  7340          CLA CLL CMA             /SET AC=7777
2210  3045          DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                        /
                        /DOES BIT 2 SET UP?
                        /
2211  7200      TST52,  CLA
2212  6132              CLLR
2213  6133              CLAB
2214  1107              TAD     K0100
2215  6132              CLLR
2216  6135              CLSA
2217  7200              CLA
2220  3024              DCA     CNTR
2221  1121              TAD     K0777           /PRESET FOR BIT 02
2222  6133              CLAB
2223  3053              DCA     SEND
2224  1111              TAD     K0200
2225  6134              CLEN
2226  7300              CLA CLL
2227  1132              TAD     K5100
2230  6132              CLLR
2231  6137              CLCA
2232  3052              DCA     RXED
2233  1052              TAD     RXED
2234  1151              TAD     M1000           /BIT 02, AND ONLY BIT 02, SET?
2235  7650              SNA CLA
2236  5242              JMP     .+4
2237  2024              ISZ     CNTR
2240  5231              JMP     .-7
2241  7410              SKP
2242  4427              JMS I   NERROR          /CHECK MONITOR
2243  4425              JMS I   ERROR           /BIT 2 FAILED TO GET SET BY COUNTING
2244  6567              TST52M                  /MESSAGE POINTER
2245  7402              HLT                     /ERROR HALT
2246  7410              SKP                     /TO NEXT TEST
2247  2211              TST52                   /ISZ LOOP; SCOPE LOOP
2250  7340              CLA CLL CMA             /SET AC=7777
2251  3045              DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 1 SET UP?
                    /
2252  7200  TST53, CLA
2253  6132        CLLR
2254  6133        CLAB
2255  1107        TAD     K0100
2256  6132        CLLR
2257  6135        CLSA
2260  7200        CLA
2261  3024        DCA     CNTR
2262  1124        TAD     K1777           /PRESET FOR BIT 01
2263  6133        CLAB
2264  3053        DCA     SEND
2265  1111        TAD     K0200
2266  6134        CLEN
2267  7300        CLA CLL
2270  1132        TAD     K5100
2271  6132        CLLR
2272  6137        CLCA
2273  3052        DCA     RXED
2274  1052        TAD     RXED
2275  1153        TAD     M2000           /BIT 01, AND ONLY BIT 01, SET?
2276  7650        SNA CLA
2277  5303        JMP     .+4
2300  2024        ISZ     CNTR
2301  5272        JMP     .-7
2302  7410        SKP
2303  4427        JMS I   NERROR          /CHECK MONITOR
2304  4425        JMS I   ERROR           /BIT 1 FAILED TO GET SET BY COUNTING
2305  6606        TST53M                  /MESSAGE POINTER
2306  7402        HLT                     /ERROR HALT
2307  7410        SKP                     /TO NEXT TEST
2310  2252        TST53                   /ISZ LOOP; SCOPE LOOP
2311  7340        CLA CLL CMA             /SET AC=7777
2312  3045        DCA     REGA            /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /DOES BIT 0 SET UP?
                    /
2313  7200  TST54,  CLA
2314  6132         CLLR
2315  6133         CLAB
2316  1107         TAD     K0100
2317  6132         CLLR
2320  6135         CLSA
2321  7200         CLA
2322  3024         DCA     CNTR
2323  1127         TAD     K3777          /PRESET FOR BIT 00
2324  6133         CLAB
2325  3053         DCA     SEND
2326  1111         TAD     K0200
2327  6134         CLEN
2330  7300         CLA CLL
2331  1132         TAD     K5100
2332  6132         CLLR
2333  6137         CLCA
2334  3052         DCA     RXED
2335  1052         TAD     RXED
2336  1154         TAD     M4000          /BIT 00, AND ONLY BIT 00, SET?
2337  7650         SNA CLA
2340  5344         JMP     .+4
2341  2024         ISZ     CNTR
2342  5333         JMP     .-7
2343  7410         SKP
2344  4427         JMS I   NERROR         /CHECK MONITOR
2345  4425         JMS I   ERROR          /BIT 0 FAILED TO GET SET BY COUNTING
2346  6625         TST54M                 /MESSAGE POINTER
2347  7402         HLT                    /ERROR HALT
2350  7410         SKP                    /TO NEXT TEST
2351  2313         TST54                  /ISZ LOOP; SCOPE LOOP
2352  5753         JMP I   .+1
2353  1316         TST34
```

```
                        /
                        /DOES COUNTER COUNT NORMALLY AND AT ALL RATES?
                        /CHECK 400 KHZ RATE
                        /
2354  7300      TST55,  CLA CLL                 /CLEAR AC
2355  1152              TAD M1400               /GET PRESET
2356  3046              DCA REGB                /SET UP FOR TIMER
2357  1122              TAD     K1000           /GET AC 02
2360  6132              CLLR                    /SET 400KC RATE
2361  7300              CLA CLL
2362  2046      BK55,   ISZ REGB                /INCREMENT COUNT
2363  7410              SKP                     /TIME OK
2364  5467              JMP I UP55              /TIMER NOT OK (,+6)
2365  6135              CLSA                    /GET STATUS
2366  7000              NOP                     /WAIT
2367  7700              SMA CLA                 /OVERFLOW?
2370  5423              JMP I DN55              /TRY AGAIN (,-6)
2371  4427              JMS I NERROR            /CHECK MONITOR
2372  4425      FD55,   JMS I ERROR             /400 KC FAILED
2373  6644              TST55M                  /MESSAGE POINTER
2374  7402              HLT                     /ERROR HALT
2375  7410              SKP                     /TO NEXT TEST
2376  2354              TST55                   /ISZ LOOP; SCOPE LOOP
2377  7340              CLA CLL CMA             /SET AC = 7777
2400  3045              DCA REGA                /PRESET REGA
                        /
                        /CHECK 100 KHZ RATE
                        /
2401  7300      TST56,  CLA CLL                 /CLEAR AC
2402  1156              TAD     M5400           /GET PRESET
2403  3046              DCA     REGB            /SET UP TIMER
2404  1125              TAD     K2000           /GET AC 01
2405  6132              CLLR                    /SET 100 KHZ RATE
2406  7300              CLA CLL
2407  2046              ISZ     REGB            /INCREMENT COUNT
2410  7410              SKP                     /TIMER OK
2411  5217              JMP     .+6             /TIMER NOT OK
2412  6135              CLSA                    /GET STATUS
2413  7000              NOP                     /WAIT
2414  7700              SMA CLA                 /OVERFLOW?
2415  5207              JMP     .-6             /TRY AGAIN
2416  4427              JMS I   NERROR          /CHECK MONITOR
2417  4425              JMS I   ERROR           /100KC FAILED
2420  6661              TST56M                  /MESSAGE POINTER
2421  7402              HLT                     /ERROR HALT
2422  7410              SKP                     /TO NEXT TEST
2423  2401              TST56                   /ISZ LOOP; SCOPE LOOP
2424  7340              CLA CLL CMA             /SET AC = 7777
2425  3045              DCA     REGA            /PRESET REGA
```

```
                        /
                        /CHECK 10 KHZ RATE
                        /
2426  7300      TST57,  CLA CLL                 /CLEAR AC
2427  1142              TAD     M0010           /GET PRESET
2430  3047              DCA     REGC            /SET UP FOR X10
2431  1151              TAD     M1000
2432  3046              DCA     REGB
2433  1126              TAD     K3000
2434  6132              CLLR                    /SET 10KC RATE
2435  7300              CLA CLL
2436  2046              ISZ     REGB            /INCREMENT COUNT
2437  7410              SKP                     /TIMER OK
2440  2047              ISZ     REGC            /INCREMENT MULTIPLIER
2441  7410              SKP                     /MULTIPLIER OK
2442  5250              JMP     .+6             /TIMER NOT OK
2443  6135              CLSA                    /GET STATUS
2444  7000              NOP                     /WAIT
2445  7700              SMA CLA                 /OVERFLOW?
2446  5236              JMP     .-10            /TRY AGAIN
2447  4427              JMS I   NERROR          /CHECK MONITOR
2450  4425              JMS I   ERROR           /10KC FAILED
2451  6676              TST57M                  /MESSAGE POINTER
2452  7402              HLT                     /ERROR HALT
2453  7410              SKP                     /TO NEXT TEST
2454  2426              TST57                   /ISZ LOOP; SCOPE LOOP
2455  7340              CLA CLL CMA             /SET AC = 7777
2456  3045              DCA     REGA            /PRESET REGA
2457  3046              DCA     REGB            /CLEAR REGB
                        /
                        /TEST 1KHZ RATE
                        /
2460  7300      TST58,  CLA CLL                 /CLEAR AC
2461  1146              TAD     M0100           /GET PRESET
2462  3047              DCA     REGC            /SET UP FOR X100
2463  1131              TAD     K4100           /SET 1KC RATE
2464  6132              CLLR
2465  7300              CLA CLL
2466  2046              ISZ     REGB            /INCREMENT COUNT
2467  7410              SKP                     /TIMER OK
2470  2047              ISZ     REGC            /INCREMENT MULTIPLIER
2471  7410              SKP                     /MULTIPLIER OK
2472  5300              JMP     .+6             /TIMER NOT OK
2473  6135              CLSA                    /GET STATUS
2474  7000              NOP                     /WAIT
2475  7700              SMA CLA                 /OVERFLOW?
2476  5266              JMP     .-10            /TRY AGAIN
2477  4427              JMS I   NERROR          /CHECK MONITOR
2500  4425              JMS I   ERROR           /1KC FAILED
2501  6713              TST58M                  /MESSAGE POINTER
2502  7402              HLT                     /ERROR HALT
2503  7410              SKP                     /TO NEXT TEST
2504  2460              TST58                   /ISZ LOOP; SCOPE LOOP
2505  7340              CLA CLL CMA             /SET AC = 7777
2506  3045              DCA     REGA            /PRESET REGA
```

```
                    /
                    /CHECK 100 CPS RATE
                    /
2507  7300  TST59,   CLA CLL                 /CLEAR AC
2510  3046          DCA     REGB            /CLEAR REGB
2511  1146          TAD     M0100           /GET PRESET
2512  3047          DCA     REGC            /SET FOR X100
2513  1150          TAD     M0400           /GET PRESET
2514  6133          CLAB                    /PRESET BUFFER
2515  7300          CLA CLL                 /CLEAR AC
2516  1111          TAD     K0200           /SET AC 05=1
2517  6134          CLEN                    /ENABLE PRESET
2520  7300          CLA CLL
2521  1132          TAD     K5100           /SET 100 CPS RATES
2522  6132          CLLR                    /ENABLE RATE
2523  7300          CLA CLL                 /CLEAR AC
2524  2046          ISZ     REGB            /INCREMENT TIME
2525  7410          SKP
2526  2047          ISZ     REGC            /INCREMENT MULTIPLIER
2527  7410          SKP                     /TIME OK
2530  5336          JMP     .+6             /TIME NOT OK! RATE FAILED
2531  6135          CLSA                    /GET STATUS
2532  7000          NOP                     /WAIT
2533  7700          SMA CLA                 /OVERFLOW?
2534  5324          JMP     .-10            /TRY AGAIN
2535  4427          JMS I   NERROR          /CHECK MONITOR
2536  4425          JMS I   ERROR           /RATE 100 HZ FAILED
2537  6727          TST59M
2540  7402          HLT
2541  7610          SKP CLA
2542  2507          TST59
2543  1146          TAD     M0100
2544  3045          DCA     REGA
2545  3046          DCA     REGB            /CLEAR REGB
```

```
                        /
                        /CHECK CHANNEL 1 INPUT RATE (RATE MUST BE BETWEEN 47 CPS AND 180 KHZ)
                        /(INSURE THAT AN INPUT IS PROVIDED)
                        /
2546  7300      TST60,  CLA CLL                 /CLEAR AC
2547  1102              TAD     K0020         /GET AC 05
2550  6134              CLEN                  /ENABLE CHANNEL 1 INPUT
2551  7200              CLA
2552  1135              TAD     K6000         /GET AC 00, 01
2553  6132              CLLR                  /ENABLE RATE=CHANNEL 1 INPUT
2554  7300      TST60N, CLA CLL                 /CLEAR AC
2555  6137              CLCA                  /GET COUNTER
2556  3053              DCA     SEND          /SAVE IT
2557  2046              ISZ     REGB          /WAIT
2560  5357              JMP     .-1
2561  6137              CLCA                  /GET COUNTER
2562  7041              CIA                   /2'S COMPLEMENT
2563  1053              TAD     SEND          /COMPARE
2564  7640              SZA CLA               /HAS IT CHANGED?
2565  4427              JMS I   NERROR        /CHECK MONITOR
2566  4425              JMS I   ERROR         /CHAN 1 LOCKED UP
2567  6745              TST60M                /MESSAGE POINTER
2570  7402              HLT                   /ERROR HALT
2571  7410              SKP                   /TO NEXT TEST
2572  2554              TST60N                /SCOPE LOOP; ISZ LOOP
```

```
                    /
                    /SIMULATED INPUT TESTS CHANNEL 3
                    /
2573  1072  TST61,  TAD     K0001           /SET AC 11=1
2574  6134          CLEN                    /ENABLE CHANNEL 3
2575  6132          CLLR                    /SET EVENT FLOP
2576  6132          CLLR                    /SET SET PRE-EVENT FLOP
2577  7300          CLA CLL                 /CLEAR AC
2600  6134          CLEN                    /CLEAR ENABLES
2601  6135          CLSA                    /GET STATUS
2602  0127          AND     K3777           /IGNORE O'FLO
2603  3053          DCA     SEND            /SAVE IT
2604  6135          CLSA                    /GET STATUS AGAIN
2605  0074          AND     K0003           /SAVE CHANNEL 3
2606  3052          DCA     RXED            /SAVE IT
2607  1052          TAD     RXED            /FETCH IT
2610  7640          SZA CLA                 /CHANNEL 3 0?
2611  5470          JMP I   UP61           /CLSA DOESN'T 0 INPUT CHANNEL 3 (,+6)
2612  1053          TAD     SEND            /GET STATUS
2613  7041          CIA                     /2'S COMPLEMENT
2614  1074          TAD     K0003           /SUBTRACT SET
2615  7650          SNA CLA                 /EQUAL?
2616  4427          JMS I   NERROR          /CHECK MONITOR
2617  4425  FD61,   JMS I   ERROR           /BOTH PRE-EVENT  AND EVENT NOT SET
2620  6766          TST61M                  /MESSAGE POINTER
2621  7402          HLT                     /ERROR HALT
2622  7410          SKP                     /TO NEXT TEST
2623  2573          TST61                   /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /SIM INPUT TESTS CHAN 2
                    /
2624  1075  TST62,   TAD     K0004          /SET AC 09=1
2625  6134          CLEN                   /ENABLE CHAN 2
2626  6132          CLLR                   /SET EVENT FLOP
2627  6132          CLLR                   /SET PREVENT FLOP
2630  7300          CLA CLL                /CLEAR AC
2631  6134          CLEN                   /CLEAR ENABLES
2632  6135          CLSA                   /GET STATUS
2633  0127          AND     K3777          /IGNORE O'FLO
2634  3053          DCA     SEND           /SAVE IT
2635  6135          CLSA                   /GET STATUS
2636  0100          AND     K0014          /SAVE CHANNEL 2
2637  3052          DCA     RXED           /SAVE IT
2640  1052          TAD     RXED           /FETCH IT
2641  7640          SZA CLA                /0?
2642  5250          JMP     .+6            /CLSA DOESN'T 0 INPUT CHANNEL 2
2643  1053          TAD     SEND           /GET FIRST STATUS
2644  7041          CIA                    /2'S COMPLEMENT
2645  1100          TAD     K0014          /SUBTRACT SET
2646  7650          SNA CLA                /EQUAL?
2647  4427          JMS I   NERROR         /CHECK MONITOR
2650  4425          JMS I   ERROR          /BOTH PRE-EVENT AND EVENT NOT SET
2651  7010          TST62M                 /MESSAGE POINTER
2652  7402          HLT                    /ERROR HALT
2653  7410          SKP                    /TO NEXT TEST
2654  2624          TST62                  /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /SIM INPUT TESTS CHAN 1
                    /
2655  1102  TST63,  TAD     K0020          /SET AC 07=1
2656  6134          CLEN                   /SET ENABLE
2657  6132          CLLR                   /SET EVENT FLOP
2660  6132          CLLR                   /SET PREVENT FLOP
2661  7300          CLA CLL                /CLEAR AC
2662  6134          CLEN                   /CLEAR ENABLES
2663  6135          CLSA                   /GET STATUS
2664  0127          AND     K3777          /IGNORE O'FLO
2665  3053          DCA     SEND           /SAVE IT
2666  6135          CLSA                   /GET STATUS
2667  0105          AND     K0060          /SAVE CHANNEL 1
2670  3052          DCA     RXED           /SAVE IT
2671  1052          TAD     RXED           /FETCH IT
2672  7640          SZA CLA                /ZERO?
2673  5301          JMP     .+6            /CLSA DOESN'T 0 INPUT CHANNEL 1
2674  1053          TAD     SEND           /GET FIRST STATUS
2675  7041          CIA                    /2'S COMPLEMENT
2676  1105          TAD     K0060          /SUBTRACT SET
2677  7650          SNA CLA                /EQUAL?
2700  4427          JMS I   NERROR         /CHECK MONITOR
2701  4425          JMS I    ERROR         /BOTH PRE-EVENT AND EVENT NOT SET
2702  7032          TST63M                 /MESSAGE POINTER
2703  7402          HLT                    /ERROR HALT
2704  7410          SKP                    /TO NEXT TEST
2705  2655          TST63                  /ISZ LOOP; SCOPE LOOP
2706  7340          CLA CLL CMA            /SET AC=7777
2707  3045          DCA     REGA           /PRESET REGA
```

```
                        /
                        /TEST INPUT CHANNEL INTERRUPT CHAN 1
                        /
2710  1035    TST64,    TAD     PNTD            /GET RETURN POINTER TO LOCD
2711  3051              DCA     RETURN          /SET UP INTERRUPT RETURN
2712  1105              TAD     K0060           /ENABLE INPUT AND INTERRUPT
2713  6134              CLEN                    /ENABLE
2714  6132              CLLR                    /SIMULATE INPUT CHANNEL ONE
2715  6001              ION                     /ENABLE INTERRUPTS
2716  7000              NOP                     /WAIT
2717  7410              SKP                     /NO INTERRUPT
2720  4427    LOCD,     JMS I   NERROR          /CHECK MONITOR
2721  4425              JMS I   ERROR           /NO INTERRUPT ERROR
2722  7054              TST64M                  /MESSAGE POINTER
2723  7402              HLT                     /ERROR HALT
2724  7610              SKP CLA                 /TO NEXT TEST
2725  2710              TST64                   /ISZ LOOP
2726  7340              CLA CLL CMA             /SET AC=7777
2727  3045              DCA     REGA            /PRESET REGA
                        /
                        /TEST WITH INTERRUPTS DISABLED
                        /
2730  1102    TST65,    TAD     K0020           /CLEAR INTERRUPT ENABLE SET SIMULATE INPUT
2731  6134              CLEN                    /ENABLE
2732  7300              CLA CLL                 /CLEAR AC
2733  1036              TAD     PNTE            /GET RETURN POINTER TO LOCE
2734  3051              DCA     RETURN          /PUT IT IN INTERRUPT HANDLER
2735  6001              ION                     /ENABLE INTERRUPTS
2736  7000              NOP                     /WAIT
2737  6002              IOF                     /DISABLE INTERRUPTS
2740  6135              CLSA                    /CLEAR CLOCK STATUS
2741  4427              JMS I   NERROR          /CHECK MONITOR
2742  4425    LOCE,     JMS I   ERROR           /INTERRUPT IN ERROR
2743  7072              TST65M                  /MESSAGE POINTER
2744  7402              HLT                     /ERROR HALT
2745  7610              SKP CLA                 /TO NEXT TEST
2746  2730              TST65                   /ISZ LOOP; SCOPE LOOP
2747  7340              CLA CLL CMA             /SET AC=7777
2750  3045              DCA     REGA            /PRESET REGA
2751  2046              ISZ     REGB            /DO THE PAIR OF TESTS 4096 TIMES
2752  5310              JMP     TST64           /BACK
```

```
                    /
                    /TEST INPUT CHANNEL INTERRUPT CHAN 2
                    /
2753  1037  TST66,  TAD     PNTF        /GET RETURN POINTER TO LOCF
2754  3051         DCA     RETURN      /SET UP INTERRUPT RETURN
2755  1100         TAD     K0014       /SET AC 08, 09=1
2756  6134         CLEN                /ENABLE CHANNEL 2
2757  6132         CLLR                /ENABLE RATES
2760  6001         ION                 /ENABLE INTERRUPTS
2761  7000         NOP                 /WAIT
2762  7410         SKP                 /TO HERE IF NO INTERRUPT
2763  4427  LOCF,  JMS I   NERROR      /CHECK MONITOR
2764  4425         JMS I   ERROR       /NO INTERRUPT
2765  7112         TST66M              /MESSAGE POINTER
2766  7402         HLT                 /ERROR HALT
2767  7410         SKP                 /TO NEXT TEST
2770  2753         TST66               /ISZ LOOP; SCOPE LOOP
2771  7340         CLA CLL CMA         /SET AC=7777
2772  3045         DCA     REGA        /PRESET REGA
                    /
                    /TEST WITH INTERRUPTS DISABLED
                    /
2773  1075  TST67,  TAD     K0004       /SET AC 09=1
2774  6134         CLEN                /ENABLE CHANNEL 2
2775  7300         CLA CLL             /CLEAR AC
2776  1040         TAD     PNTG        /GET RETURN POINTER TO LOCG
2777  3051         DCA     RETURN      /PUT IT IN INTERRUPT HANDLER
3000  6001         ION                 /ENABLE INTERRUPTS
3001  7000         NOP                 /WAIT
3002  6002         IOF                 /DISABLE INTERRUPTS
3003  6135         CLSA                /CLEAR CLOCK STATUS
3004  4427         JMS I   NERROR      /CHECK MONITOR
3005  4425  LOCG,  JMS I   ERROR       /INTERRUPT IN ERROR--CLEA EN EVENT 2 INT BAD
3006  7133         TST67M              /MESSAGE POINTER
3007  7402         HLT                 /ERROR HALT
3010  7410         SKP                 /TO NEXT TEST
3011  2773         TST67               /ISZ LOOP; SCOPE LOOP
3012  7340         CLA CLL CMA         /SET AC=7777
3013  3045         DCA     REGA        /PRESET REGA
3014  2046         ISZ     REGB        /DO THIS PAIR OF TESTS 4096 TIMES
3015  5457         JMP I   TST66N      /BACK
```

```
                    /
                    /TEST INPUT CHANNEL INTERRUPT CHAN 3
                    /
3016  1041  TST68,  TAD     PNTH            /GET RETURN POINTER TO LOCH
3017  3051          DCA     RETURN          /SET UP INTERRUPT RETURN
3020  1074          TAD     K0003           /SET AC10,11=1
3021  6134          CLEN                    /ENABLE CHANNEL 3
3022  6132          CLLR                    /ENABLE RATES
3023  6001          ION                     /ENABLE INTERRUPTS
3024  7000          NOP                     /WAIT
3025  6002          IOF                     /DISABLE INTERRUPTS
3026  7410          SKP                     /NO INTERRUPT
3027  4427  LOCH,   JMS I   NERROR          /CHECK MONITOR
3030  4425          JMS I   ERROR           /NO INTERRUPT
3031  7152          TST68M                  /MESSAGE POINTER
3032  7402          HLT                     /ERROR HALT
3033  7410          SKP                     /TO NEXT TEST
3034  3016          TST68                   /ISZ LOOP; SCOPE LOOP
3035  7340          CLA CLL CMA             /SET AC=7777
3036  3045          DCA     REGA            /PRESET REGA
                    /
                    /TEST WITH INTERRUPTS DISABLED
                    /
3037  0072  TST69,  AND     K0001           /SET AC 11=1
3040  6134          CLEN                    /ENABLE CHANNEL 3
3041  7300          CLA CLL                 /CLEAR AC
3042  1042          TAD     PNTI            /GET RETURN POINTER TO LOCI
3043  3051          DCA     RETURN          /PUT IT IN INTERRUPT HANDLER
3044  6001          ION                     /ENABLE INTERRUPTS
3045  7000          NOP                     /WAIT
3046  6002          IOF                     /DISABLE INTERRUPTS
3047  6135          CLSA                    /CLEAR CLOCK STATUS
3050  4427          JMS I   NERROR          /CHECK MONITOR
3051  4425  LOCI,   JMS I   ERROR           /INTERRUPT IN ERROR
3052  7173          TST69M                  /MESSAGE POINTER
3053  7402          HLT                     /ERROR HALT
3054  7410          SKP                     /TO NEXT TEST
3055  3037          TST69                   /ISZ LOOP; SCOPE LOOP
3056  7340          CLA CLL CMA             /SET AC=7777
3057  3045          DCA     REGA            /PRESET REGA
3060  2046          ISZ     REGB            /DO THIS PAIR OF TESTS 4096 TIMES
3061  5216          JMP     TST68           /BACK
3062  1144          TAD     M0040
3063  3045          DCA     REGA            /PRESET REGA IF NEXT TEST IS TO BE EXECUTED
```

```
                    /
                    /TEST OF INPUT CHNNEL 3
                    /KNOBS OF CHAN1,CHAN2,CHAN3 SET TO LINEFREQ, LEVEL IS DISABLED.
                    /
3064  6135  TST70,  CLSA                            /CLEAR STATUS
3065  7300        CLA CLL                           /CLEAR AC
3066  6132        CLLR                              /CLEAR ALL MODES
3067  1074        TAD     K0003                     /SET AC 10, 11=1
3070  6134        CLEN                              /ENABLE CHAN3 INPUT AND INTER.
3071  7200        CLA                               /CLEAR AC
3072  2046        ISZ     REGB                      /INCREMENT TIMER
3073  7410        SKP                               /NOT DONE YET
3074  5277        JMP     .+3                       /TIMER OUT; ERROR CONDITION
3075  6131        CLSK                              /SKIP ON CLOCK INTER.
3076  5272        JMP     .-4                       /WAIT
3077  6135        CLSA                              /GET CLOCK STATUS
3100  3052        DCA     RXED                      /SAVE IT
3101  3046        DCA     REGB                      /CLEAR COUNT
3102  1052        TAD     RXED                      /RESTORE IT
3103  7041        CIA                               /2'S COMPLEMENT
3104  1073        TAD     K0002                     /ADD EVENT 3
3105  7650        SNA CLA                           /EQUAL?
3106  4427        JMS I   NERROR                    /CHECK WITH MONITOR
3107  4425        JMS I   ERROR                     /CHAN 3 EVENT NOT SET, OR PRE-EVENT WAS SET, OR OTHER CHAN UP
3110  7212        TST70M                            /MESSAGE POINTER
3111  7402        HLT                               /ERROR HALT
3112  7410        SKP                               /TO NEXT TEST
3113  3064        TST70                             /ISZ LOOP; SCOPE LOOP
3114  1144        TAD     M0040
3115  3045        DCA     REGA                      /PRESET REGA
```

```
                    /
                    /TEST OF INPUT CHANNEL 2
                    /
3116  6135  TST71,  CLSA                        /CLEAR STATUS
3117  7300          CLA CLL                     /CLEAR AC
3120  6132          CLLR                        /ZERO ALL MODES
3121  1100          TAD     K0014               /ENAB. CHAN. 2 INPUT AND INTERRUPT FLOPS
3122  6134          CLEN                        /ENABLE
3123  7200          CLA                         /CLEAR AC
3124  2046          ISZ     REGB                /INCREMENT TIMER
3125  7410          SKP                         /NOT DONE YET
3126  5331          JMP     .+3                 /TIMER OUT; ERROR CONDITION
3127  6131          CLSK                        /CHECK FOR CLOCK INTER.
3130  5324          JMP     .-4                 /WAIT
3131  6135          CLSA                        /GET STATUS
3132  3052          DCA     RXED                /SAVE IT
3133  3046          DCA     REGB                /CLEAR COUNT
3134  1052          TAD     RXED                /RESTORE IT
3135  7041          CIA                         /2'S COMPLEMENT
3136  1077          TAD     K0010               /ADD EVENT 2
3137  7650          SNA CLA                     /EQUAL?
3140  4427          JMS I   NERROR             /CHECK MONITOR
3141  4425          JMS I   ERROR              /CHAN 2 EVENT NOT SET, OR PRE-EVENT WAS SET, OR OTHER CHAN UP
3142  7240          TST71M                      /MESSAGE POINTER
3143  7402          HLT                         /ERROR HALT
3144  7410          SKP                         /TO NEXT TEST
3145  3116          TST71                       /ISZ LOOP; SCOPE LOOP
3146  1144          TAD     M0040
3147  3045          DCA     REGA                /PRESET REGA
```

```
                        /
                        /TEST OF INPUT CHAN 1
                        /
3150  6135  TST72,  CLSA                        /CLEAR STATUS
3151  7300          CLA CLL                     /CLEAR AC
3152  6132          CLLR                        /CLEAR ALL MODES
3153  1105          TAD     K0060               /SET AC6,7=1
3154  6134          CLEN                        /ENABLE CHAN 1 INPUT AND INTERRUPT
3155  7200          CLA                         /CLEAR AC
3156  2046          ISZ     REGB                /INCREMENT TIMER
3157  7410          SKP                         /NOT DONE YET
3160  5363          JMP     .+3                 /TIMER OUT; ERROR CONDITION
3161  6131          CLSK                        /CHECK FOR CLOCK INTER.
3162  5356          JMP     .-4                 /WAIT
3163  6135          CLSA                        /GET CLOCK STATUS
3164  3052          DCA     RXED                /SAVE IT
3165  3046          DCA     REGB                /CLEAR COUNT
3166  1052          TAD     RXED                /RESTORE IT
3167  7041          CIA                         /COMPLEMENT
3170  1104          TAD     K0040               /ADD INPUT 1
3171  7650          SNA CLA                     /EQUAL?
3172  4427          JMS I   NERROR              /CHECK MONITOR
3173  4425          JMS I   ERROR               / CHAN 1 EVENT NOT SET, OR PREVENT WAS SET, OR OTHER CHAN UP
3174  7266          TST72M                      /MESSAGE POINTER
3175  7402          HLT                         /ERROR HALT
3176  7410          SKP                         /TO NEXT TEST
3177  3150          TST72                       /ISZ LOOP; SCOPE LOOP
3200  7340          CLA CLL CMA                 /SET AC=7777
3201  3045          DCA     REGA                /PRESET REGA
```

```
                    /
                    /TEST FAST SAMPLE MODE IF BIT 04=0
                    /
3202  7404  TST73,  OSR                        /IF RIGHT SW BIT 2(1)
3203  7006        RTL                         /SKIP FAST SAM TEST?
3204  7006        RTL
3205  7004        RAL                         /RSW 04=1?
3206  7710        SPA CLA
3207  5461        JMP I   TST77N              /INDIRECT REF TO TST77
3210  6141        LINC                        /ENTER LINC MODE
3211  0011        CLR                         /CLEAR AC
3212  0004        ESF                         /CLEAR SPEC. IN REG.
3213  0100        SAM0                        /READ KNOB ZERO
3214  0002        PDP                         /BACK TO PMODE
3215  3053        DCA     SEND                /TO PAGE 0
3216  6141        LINC                        /BACK TO LMODE
3217  0101        SAM1                        /READ KNOB 1
3220  0011        CLR                         /CLEAR AC
3221  1020        LDAI                        /PICK UP AC BIT 03
3222  0100        0100
3223  0004        ESF                         /ENABLE FAST SAM
3224  0002        PDP                         /ENTER PDP-8 MODE
3225  6135        CLSA                        /CLEAR CLOCK STATUS
3226  7300        CLA CLL                     /CLEAR AC
3227  1115        TAD     K0400               /SET MODE BIT0=1
3230  6132        CLLR                        /ENABLE COUNT
3231  6141        LINC                        /ENTER LINC MODE
3232  0100        SAM0                        /FAST SAM SET THEREFORE READ IN KNOB 1
3233  0100        SAM0                        /SHOULD STILL READ KNOB1
3234  0002        PDP                         /ENTER PDP-8 MODE
3235  3052        DCA     RXED                /SAVE VALUE
3236  1052        TAD     RXED                /RESTORE IT
3237  7041        CIA                         /2'S COMPLEMENT
3240  1053        TAD     SEND                /COMPARE IT
3241  7640        SZA CLA                     /EQUAL?
3242  4427        JMS I   NERROR              /CHECK MONITOR
3243  4425        JMS I   ERROR               /READING FAST SAM CONVERTED IN ERROR
3244  7314        TST73M                      /MESSAGE POINTER
3245  7402        HLT                         /ERROR HALT
3246  7410        SKP                         /TO NEXT TEST
3247  3202        TST73                       /ISZ LOOP; SCOPE LOOP
3250  7340        CLA CLL CMA                 /SET AC=7777
3251  3045        DCA     REGA                /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /TEST FAST SAMPLE WITH MODE 2=1 (CHECK THAT KNOBS 0 & 1 ARE SET PROPERLY)
                    /
3252  1116  TST74,  TAD     K0500          /SET AC 03,05=1
3253  6132          CLLR                   /MODE 2(1),0(1)
3254  7330          CLA CLL CML RAR        /SET AC=4000
3255  6133          CLAB                   /SET BUFF=4000
3256  7200          CLA                    /CLEAR AC
3257  1111          TAD     K0200          /SET AC 04=1
3260  6134          CLEN                   /LOAD CTN FROM BUF
3261  7200          CLA                    /CLEAR AC
3262  6133          CLAB                   /CLR BUF
3263  7200          CLA                    /CLEAR AC
3264  6132          CLLR                   /CLEAR ALL MODES
3265  1116          TAD     K0500          /SET AC 03,05=1
3266  6132          CLLR                   /SET OVERFLOW MODE 0(1)
3267  6141          LINC                   /ENTER LINC MODE
3270  0100          SAM0                   /SAMPLE KNOB 0
3271  0002          PDP                    /ENTER PDP-8 MODE
3272  3052          DCA     RXED           /STORE
3273  1052          TAD     RXED           /RESTORE
3274  7041          CIA                    /2'S COMPLEMENT
3275  1053          TAD     SEND           /ADD FIRST SAMPLE
3276  7650          SNA CLA                /EQUAL?
3277  4427          JMS I   NERROR         /CHECK MONITOR
3300  4425          JMS I   ERROR          /CONVERSION NOT INITIATED BY OVFLOW
3301  7333          TST74M                 /MESSAGE POINTER
3302  7402          HLT                    /ERROR HALT
3303  7410          SKP                    /TO NEXT TEST
3304  3252          TST74                  /ISZ LOOP; SCOPE LOOP
3305  7340          CLA CLL CMA            /SET AC=7777
3306  3045          DCA     REGA           /REGA FOR NEXT TEST
3307  2046          ISZ     REGB           /DONE?
3310  5202          JMP     TST73          /BACK
3311  1144          TAD     M0040
3312  3046          DCA     REGB
```

```
                    /
                    /CHECK THAT MODE 0(0),1(1),2(1) DO NOT AFFECT SAMPLE
                    /
3313  7200  TST75,  CLA                              /CLEAR AC
3314  6132          CLLR                             /ZERO ALL MODES
3315  1113          TAD     K0300                    /SET AC04,05=1
3316  6132          CLLR                             /MODE 1(1),2(1),0(0)
3317  6141          LINC                             /ENTER LINC MODE
3320  0011          CLR                              /CLEAR AC
3321  0004          ESF                              /ZERO SPEC. IN. REG.
3322  0100          SAM0                             /SAMPLE KNOB 0
3323  0002          PDP                              /TO PMODE
3324  3053          DCA     SEND                     /SAVE KNOB 0
3325  6141          LINC                             /TO LMODE
3326  0101          SAM1                             /SAMPLE KNOB 1
3327  1020          LDAI                             /PICK UP AC 05
3330  0100          0100
3331  0004          ESF                              /SET FAST SAM FLOP
3332  0100          SAM0                             /GET KNOB 1 SETTING
3333  0002          PDP                              /ENTER PDP MODE
3334  3052          DCA     RXED                     /STORE
3335  1052          TAD     RXED                     /RECEIVE
3336  7041          CIA                              /2'S COMPLEMENT
3337  1053          TAD     SEND                     /COMPARE
3340  7640          SZA CLA                          /EQUAL?
3341  4427          JMS I   NERROR                   /CHECK MONITOR
3342  4425          JMS I   ERROR                    /FAST SAM NOT SET
3343  7355          TST75M                           /MESSAGE POINTER
3344  7402          HLT                              /ERROR HALT
3345  7410          SKP                              /TO NEXT TEST
3346  3313          TST75                            /ISZ LOOP; SCOPE LOOP
3347  7340          CLA CLL CMA                      /SET AC=7777
3350  3045          DCA     REGA                     /PRESET REGA FOR NEXT TEST
```

```
                    /
                    /NOW CHECK FOR INHIBITING OF FAST SAM
                    /
3351  6141  TST76,  LINC                        /ENTER LINC MODE
3352  0100        SAM0                         /READ KNOB 0
3353  0002        PDP                          /ENTER PDP MODE
3354  3052        DCA     RXED                 /STORE
3355  1052        TAD     RXED                 /RESTORE
3356  7041        CIA                          /2'S COMPLEMENT
3357  1053        TAD     SEND                 /COMPARE
3360  7650        SNA CLA                      /EQUAL?
3361  4427        JMS I   NERROR               /CHECK MONITOR
3362  4425        JMS I   ERROR                /MODE 2(1),1(1) INHIBIT FAST SAM
3363  7376        TST76M                       /MESSAGE POINTER
3364  7402        HLT                          /ERROR HALT
3365  7410        SKP                          /TO NEXT TEST
3366  3351        TST76                        /ISZ LOOP; SCOPE LOOP
3367  7340        CLA CLL CMA                  /SET AC=7777
3370  3045        DCA     REGA                 /PRESET REGA FOR NEXT TEST
3371  2046        ISZ     REGB                 /DONE?
3372  5460        JMP I   TST75N               /BACK VIA PAGE 0
3373  1144        TAD     M0040
3374  3046        DCA     REGB                 /PRESET REGB
```

```
                    /DOES TO PRESET CLEAR OVFLO, ENABLES, RATES AND MODES
                    /PROGRAMED IO PRESET USED
                    /
3375  7200  TST77,  CLA                              /CLEAR AC
3376  6132          CLLR                             /CLEAR ALL MODES
3377  6134          CLEN                             /CLEAR ALL ENABLES
3400  1126          TAD     K3000                    /SET AC 01,02=1
3401  6132          CLLR                             /SET RATE=10KHZ
3402  7200          CLA
3403  1135          TAD     K6000                    /SET AC 00,01=1
3404  7001          IAC                              /INCREMENT COUNTER
3405  7440          SZA                              /DONE?
3406  5204          JMP     .-2                      /WAIT LOOP 4.92 MSEC
                    /
                    /NOW DO IO PRESET CHECK IF RATE BITS 1,2 CLEAR
                    /
3407  4157          CLEAR                            /GENERATE I-O PRESET
3410  6137          CLCA                             /GET COUNTER
3411  3053          DCA     SEND                     /STORE
3412  1135          TAD     K6000                    /SET UP DELAY
3413  7001          IAC                              /INCREMENT COUNTER
3414  7440          SZA                              /DONE?
3415  5213          JMP     .-2                      /WAIT LOOP 4.92 MSEC
3416  6137          CLCA                             /READ COUNTER AGAIN
3417  7041          CIA                              /2'S COMPLEMENT
3420  1053          TAD     SEND                     /COMPARE
3421  7650          SNA CLA                          /HAS COUNTER CHANGED?
3422  4427          JMS I   NERROR                   /CHECK MONITOR
3423  4425          JMS I   ERROR                    /IO PRESET FAILED TO CLEAR RATE BITS 1 & 2
3424  7423          TST77M                           /MESSAGE POINTER
3425  7402          HLT                              /ERROR HALT
3426  7410          SKP                              /TO NEXT TEST
3427  3375          TST77                            /ISZ LOOP; SCOPE LOOP
3430  7340          CLA CLL CMA                      /SET AC=7777
3431  3045          DCA     REGA                     /PRESET REGA FOR NEXT TEST
3432  2046          ISZ     REGB                     /LOOP BACK
3433  5461          JMP I   TST77N
3434  1144          TAD     M0040                    /
3435  3046          DCA     REGB                     /PRESET REGB
```

```
                    /
                    /NOW ENABLE RATE BIT 0
                    /
3436  7200  TST79, CLA                          /CLEAR AC
3437  6132        CLLR                         /CLEAR ALL MODES
3440  6134        CLEN                         /CLEAR ENABLES
3441  1130        TAD     K4000                /SET AC 00=1
3442  6132        CLLR                         /SET RATE=1KHZ
3443  7200        CLA
3444  7001        IAC                          /INCREMENT COUNTER
3445  7440        SZA                          /DONE?
3446  5244        JMP     .-2                  /WAIT LOOP 16 MSEC
                    /
                    /NOW DO IO PRESET AND SEE IF BIT 0 CLEARED
                    /
3447  4157        CLEAR                        /GENERATE I-O PRESET
3450  6137        CLCA                         /READ COUNTER
3451  3053        DCA     SEND                 /STORE
3452  7001        IAC                          /INCRMENT COUNTER
3453  7440        SZA                          /DONE?
3454  5252        JMP     .-2                  /WAIT 16 MSEC
3455  6137        CLCA                         /READ COUNTER AGAIN
3456  7041        CIA                          /2'S COMPLEMENT
3457  1053        TAD     SEND                 /COMPARE
3460  7650        SNA CLA                      /COUNTER STILL THE SAME
3461  4427        JMS I   NERROR               /CHECK MONITOR
3462  4425        JMS I   ERROR                /RATE BIT 0 SET AFTER IO PRESET
3463  7457        TST79M                       /MESSAGE POINTER
3464  7402        HLT                          /ERROR HALT
3465  7410        SKP                          /TO NEXT TEST
3466  3436        TST79                        /ISZ LOOP; SCOPE LOOP
3467  7340        CLA CLL CMA                  /SET AC=7777
3470  3045        DCA     REGA                 /PRESET REGA
3471  2046        ISZ     REGB                 /LOOP BACK
3472  5462        JMP I   TST79N               /BACK VIA PAGE 0
3473  3045        DCA     REGA                 /CLEAR REGA IF EXECUTING NEXT TEST
```

```
                    /
                    /DOES OVERFLOW AND OVFLO INT. FLOP
                    /CLEAR WITH IO PRESET
                    /
3474  7200  TST81,   CLA                          /CLEAR AC
3475  6132          CLLR                         /CLEAR ALL MODES
3476  1107          TAD     K0100
3477  6132          CLLR                         /SET MODE 2(1)
3500  6135          CLSA                         /CLEAR STATUS
3501  7240          CLA CMA
3502  6133          CLAB                         /SET BUF TO 7777
3503  7200          CLA
3504  1111          TAD     K0200
3505  6134          CLEN                         /LOAD COUNTER
3506  4157          CLEAR                        /GENERATE I-O PRESET THIS ONE WILL SET OVERFLOW
3507  4157          CLEAR                        /THIS ONE WILL CLEAR IT
3510  6135          CLSA                         /GET STATUS
3511  7700          SMA CLA
3512  4427          JMS I   NERROR               /CHECK MONITOR
3513  4425          JMS I   ERROR                /OVFLO STILL SET AFTER IO PRESET
3514  7511          TST81M                       /MESSAGE POINTER
3515  7402          HLT                          /ERROR HALT
3516  7410          SKP                          /TO NEXT TEST
3517  3474          TST81                        /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /TEST OVFLO INT ENABLE
                    /
3520  7200  TST82,  CLA                       /CLEAR AC
3521  1107          TAD     K0100
3522  6132          CLLR                      /SET MODE 2(1)
3523  6135          CLSA                      /CLEAR STATUS
3524  7240          CLA CMA
3525  6133          CLAB                      /SET BUF PRESET REG.
3526  7200          CLA
3527  1111          TAD     K0200
3530  6134          CLEN                      /LOAD CNT WITH 4000
3531  4157          CLEAR                     /GENERATE I-O PRESET, WHIS WILL SET OVERFLOW
3532  6132          CLLR                      /CLEAR ALL MODES
3533  1107          TAD     K0100
3534  6132          CLLR                      /GEN.
3535  6131          CLSK
3536  4427          JMS I   NERROR            /CHECK MONITOR
3537  4425          JMS I   ERROR             /OVFLO INTER. SET AFTER I/O PRESET
3540  7534          TST82M                    /MESSAGE POINTER
3541  7402          HLT                       /ERROR HALT
3542  7610          SKP CLA                   /TO NEXT TEST
3543  3520          TST82                     /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /DOES IO PRESET CLEAR INPUT ENABLE FLOPS
                    /
3544  7200  TST83,   CLA
3545  6132          CLLR                        /CLEAR ALL MODES
3546  1106          TAD     K0077
3547  6134          CLEN                        /ENABLE INPUTS TO ALL CHAN
3550  4157          CLEAR                       /GENERATE I-O PRESET
3551  6135          CLSA                        /CLEAR STATUS
3552  7200          CLA
3553  1106          TAD     K0077
3554  6132          CLLR                        /SIMULATE INPUTS ON ALL CHAN
3555  7200          CLA
3556  6135          CLSA                        /GET STATUS
3557  0127          AND     K3777               /IGNORE O!FLO
3560  7650          SNA CLA
3561  4427          JMS I   NERROR              /CHECK MONITOR
3562  4425          JMS I   ERROR               /STATUS NOT ZERO I/O PRESET FAILED
3563  4310          TST83M                      /MESSAGE POINTER
3564  7402          HLT                         /ERROR HALT
3565  7610          SKP CLA                     /TO NEXT TEST
3566  3544          TST83                       /ISZ LOOP; SCOPE LOOP
```

```
                    /
                    /DOES IO PRESET CLEAR MODE 2
                    /
3567  6133  TST84,  CLAB
3570  6132          CLLR                        /CLEAR MODES
3571  1107          TAD     K0100
3572  6132          CLLR                        /SET MODE 2(1) = CLR CNT
3573  4157          CLEAR                       /GENERATE I-O PRESET
3574  1134          TAD     K5555
3575  6133          CLAB                        /LOAD BUF WITH 5555
3576  7200          CLA
3577  1111          TAD     K0200
3600  6134          CLEN                        /GEN LOAD CNT
3601  6137          CLCA                        /LOAD CNT TO AC
3602  7700          SMA CLA
3603  4427          JMS I   NERROR              /CHECK MONITOR
3604  4425          JMS I   ERROR               /MODE 2 NOT CLEARED BY I/O PRESET
3605  4334          TST84M                      /MESSAGE POINTER
3606  7402          HLT                         /ERROR HALT
3607  7610          SKP CLA                     /TO NEXT TEST
3610  3567          TST84                       /ISZ LOOP; SCOPE LOOP
3611  7340          CLA CLL CMA                 /SET AC = 7777
3612  3045          DCA     REGA                /PRESET REGA
```

```
                    /
                    /DOES IO PRESET CLEAR MODE Ø
                    /
3613  7604  TST85,  LAS                        /IF RIGHT SW BIT 4(1)
3614  7006          RTL                        /SKIP FAST SAM TEST
3615  7006          RTL
3616  7710          SPA CLA
3617  5300          JMP     RESET
3620  7200          CLA
3621  6132          CLLR                       /CLEAR ALL MODES
3622  6141          LINC                       /ENTER LINC MODE
3623  0100          SAMØ                       /READ KNOB Ø
3624  0002          PDP
3625  3053          DCA     SEND
3626  6141          LINC
3627  0101          SAM1                       /READ KNOB 1
3630  0002          PDP                        /ENTER PDP MODE
3631  7200          CLA
3632  1115          TAD     KØ4ØØ
3633  6132          CLLR                       /SET MODE Ø(1)
3634  6141          LINC                       /ENTER LINC MODE
3635  1020          LDAI
3636  0020          ØØ2Ø
3637  0004          ESF                        /DO IO PRESET
3640  1020          LDAI
3641  0100          Ø1ØØ                       /ENABLE FAST SAM
3642  0004          ESF
3643  0100          SAMØ                       /READ KNOB 1=FAST S. MODE
3644  0002          PDP                        /ENTER PDP MODE
3645  7041          CIA
3646  1053          TAD     SEND
3647  7640          SZA CLA
3650  4427          JMS I   NERROR             /CHECK MONITOR
3651  4425          JMS I   ERROR              /FAST SAM NOT SET
3652  4360          TST85M                     /MESSAGE POINTER
3653  7402          HLT                        /ERROR HALT
3654  7410          SKP                        /TO NEXT TAPE
3655  3613          TST85                      /ISZ LOOP; SCOPE LOOP
3656  7340          CLA CLL CMA                /SET AC = 7777
3657  3045          DCA     REGA               /PRESET REGA
```

```
                    /
                    /NOW CHECK FOR MODE 0 CLEARED
                    /
3660  6141  TST86,  LINC                        /ENTER LINC MODE
3661  0100          SAM0                        /READ KNOB 0
3662  0002          PDP                         /ENTER PDP MODE
3663  7041          CIA
3664  1053          TAD     SEND
3665  7650          SNA CLA
3666  4427          JMS I   NERROR              /CHECK MONITOR
3667  4425          JMS I   ERROR               /MODE 0 NOT CLEARED
3670  4405          TST86M                      /MESSAGE POINTER
3671  7402          HLT                         /ERROR HALT
3672  7410          SKP                         /TO NEXT TEST
3673  3660          TST86                       /ISZ LOOP; SCOPE LOOP
3674  7340          CLA CLL CMA                 /SET AC = 7777
3675  3045          DCA     REGA                /PRESET REGA
3676  2046          ISZ     REGB                /LOOP BACK
3677  5213          JMP     TST85
                    /
                    /RESET ANYTHING LEFT HANGING
                    /
3700  4157  RESET,  CLEAR                       /GENERATE I-O PRESET
3701  1144          TAD     M0040
3702  3045          DCA     REGA                /PRESET REGA PRIOR TO NEXT TEST
```

```
                    /
                    /DOES MODE 1(1) WORK CHAN 1
                    /
3703  7200    TST87,  CLA
3704  6132            CLLR                    /CLEAR ALL MODES
3705  6133            CLAB                    /CLEAR BUF
3706  4444            JMS I   RANDOM          /GET RANDOM NUM
3707  3053            DCA     SEND
3710  1053            TAD     SEND
3711  6133            CLAB                    /SEND RANDOM NUM TO BUF
3712  7200            CLA
3713  1107            TAD     K0100
3714  6132            CLLR                    /GEN "CLR CNT"
3715  6135            CLSA                    /CLEAR CLOCK STATUS
3716  7200            CLA                      .
3717  1111            TAD     K0200
3720  6134            CLEN                    /GEN LOAD CNT
3721  6132            CLLR                    /SET MODE BIT 1(1)
3722  7200            CLA
3723  6133            CLAB                    /CLEAR BUFFER
3724  1105            TAD     K0060
3725  6134            CLEN                    /ENABLE INPT 1 AND INT CHAN1
3726  2046            ISZ     REGB            /INCREMENT TIMER
3727  7410            SKP                     /NOT DONE YET
3730  5333            JMP     .+3             /TIME OUT
3731  6131            CLSK                    /SKP ON CLOCK INT
3732  5326            JMP     .-4
3733  6135            CLSA                    /CLEAR STATUS
3734  7200            CLA
3735  3046            DCA     REGB            /CLEAR REGB
3736  6136            CLBA                    /GET BUFFER
3737  7041            CIA
3740  1053            TAD     SEND            /COMPARE
3741  7650            SNA CLA
3742  4427            JMS I   NERROR          /CHECK MONITOR
3743  4425            JMS I   ERROR           /CHAN 1 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3744  4425            TST87M                  /MESSAGE POINTER
3745  7402            HLT                     /ERROR HALT
3746  7410            SKP                     /TO NEXT TEST
3747  3703            TST87                   /ISZ LOOP) SCOPE LOOP
3750  1144            TAD     M0040
3751  3045            DCA     REGA
```

```
                        /
                        /DOES MODE 1 (1) WORK CHAN 2
                        /
3752  6134    TST88,    CLEN                    /CLEAR ENABLES
3753  6135              CLSA                    /CLEAR CLOCK STATUS
3754  7200              CLA
3755  6133              CLAB                    /CLEAR BUFFER
3756  1100              TAD       K0014
3757  6134              CLEN                    /ENABLE CHAN 2 INPUT AND INT
3760  2046              ISZ       REGB          /INCREMENT TIMER
3761  7410              SKP                     /NOT DONE YET
3762  5365              JMP       .+3           /TIME OUT
3763  6131              CLSK                    /SKP ON CLOCK INT
3764  5360              JMP       .-4
3765  6135              CLSA                    /CLEAR STATUS
3766  7200              CLA
3767  3046              DCA       REGB          /CLEAR REGB
3770  6136              CLBA                    /GET BUFFER
3771  7041              CIA
3772  1053              TAD       SEND          /COMPARE
3773  7650              SNA CLA
3774  4427              JMS I     NERROR        /CHECK MONITOR
3775  4425              JMS I     ERROR         /CHAN2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3776  4453              TST88M                  /MESSAGE POINTER
3777  7402              HLT                     /ERROR HALT
4000  7410              SKP                     /TO NEXT TEST
4001  3752              TST88                   /ISZ LOOP; SCOPE LOOP
4002  1144              TAD       M0040
4003  3045              DCA       REGA
```

```
                    /
                    /DOES MODE 1 (1) WORK CHAN 3
                    /
4004  6134    TST89,  CLEN                    /CLEARS ENABLE
4005  6135            CLSA                    /CLEAR STATUS
4006  7200            CLA
4007  6133            CLAB                    /CLEAR BUFFER
4010  1074            TAD     K0003
4011  6134            CLEN                    /ENABLES CHAN 3 INPUT AND INT
4012  2046            ISZ     REGB            /INCREMENT TIMER
4013  7410            SKP                     /NOT DONE YET
4014  5217            JMP     .+3             /TIME OUT
4015  6131            CLSK                    /SKIP ON CK INT
4016  5212            JMP     .-4
4017  6135            CLSA                    /CLEAR CLOCK STATUS
4020  7200            CLA
4021  3046            DCA     REGB            /CLEAR REGB
4022  6136            CLBA                    /GET BUF
4023  7041            CIA
4024  1053            TAD     SEND            /COMPARE
4025  7650            SNA CLA
4026  4427            JMS I   NERROR          /CHECK MONITOR
4027  4425            JMS I   ERROR           /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
4030  4501            TST89M                  /MESSAGE POINTER
4031  7402            HLT                     /ERROR HALT
4032  7410            SKP                     /TO NEXT TEST
4033  4004            TST89                   /ISZ LOOP; SCOPE LOOP
4034  7340            CLA CLL CMA             /SET AC=7777
4035  3045            DCA     REGA            /PRESET REGA
4036  1144            TAD     M0040           /
4037  3046            DCA     REGB            /PRESET REGB
```

```
                    /
                    /TEST MODE 1(1) AND MODE 2(1) CHAN 1
                    /
4040  6134  TST90,  CLEN                    /CLEARS ENABLES
4041  1113          TAD     K0300
4042  1122          TAD     K1000
4043  6132          CLLR                    /START CNT RATE=400KHZ = MODE 1(1) AND 2(1)
4044  7200          CLA
4045  1113          TAD     K0300
4046  6132          CLLR                    /STOP CNT - MODE 1(1) AND 2(1)
4047  6137          CLCA                    /GET CNT
4050  3053          DCA     SEND            /STORE
4051  6135          CLSA
4052  7200          CLA
4053  6133          CLAB                    /CLEAR BUF
4054  1105          TAD     K0060
4055  6134          CLEN                    /ENABLE CHAN1 INPUT AND INT
4056  2050          ISZ     REGT            /INCREMENT TIMER
4057  7410          SKP                     /NOT DONE YET
4060  5263          JMP     .+3             /TIME OUT
4061  6131          CLSK                    /SKP ON CLOCK INT
4062  5256          JMP     .-4
4063  6135          CLSA                    /CLEAR CLOCK STATUS
4064  7200          CLA
4065  3050          DCA     REGT            /CLEAR TIMER
4066  6136          CLBA                    /GET BUF
4067  7041          CIA
4070  1053          TAD     SEND            /COMAPRE
4071  7650          SNA CLA
4072  4427          JMS I   NERROR          /CHECK MONITOR
4073  4425          JMS I   ERROR           /CHAN1 FAILED TO CAUSE CNT TO BUF TRANSFER
4074  4527          TST90M                  /MESSAGE POINTER
4075  7402          HLT                     /ERROR HALT
4076  7410          SKP                     /TO NEXT TEST
4077  4040          TST90                   /ISZ LOOP) SCOPE LOOP
4100  7340          CLA CLL CMA
4101  3045          DCA     REGA
```

```
                    /
                    /TEST MODE 1 (1) AND MODE 2 (1) CHAN 2
                    /
4102  6134  TST91,  CLEN                    /CLEARS ENABLES
4103  6135        CLSA                     /CLEAR STATUS
4104  7200        CLA
4105  6133        CLAB                     /CLEAR BUF
4106  1100        TAD     K0014
4107  6134        CLEN                     /ENABLE CHAN 2 INPUT AND INT
4110  2050        ISZ     REGT             /INCREMENT TIMER
4111  7410        SKP                      /NOT DONE YET
4112  5315        JMP     .+3              /TIME OUT
4113  6131        CLSK                     /SKP ON CLOCK INT
4114  5310        JMP     .-4
4115  6135        CLSA                     /CLEAR STATUS
4116  7200        CLA
4117  3050        DCA     REGT             /CLEAR REGT
4120  7000        NOP
4121  6136        CLBA                     /GET BUF
4122  7041        CIA
4123  1053        TAD     SEND             /COMPARE
4124  7650        SNA CLA
4125  4427        JMS I   NERROR           /CHECK MONITOR
4126  4425        JMS I   ERROR            /CHAN 2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
4127  4555        TST91M
4130  7402        HLT
4131  7610        SKP CLA
4132  4102        TST91
4133  7340        CLA CLL CMA
4134  3045        DCA     REGA             /PRESET REGA
```

```
                    /
                    /TEST MODE 1 (1) AND MODE 2 (1) CHAN 3
                    /
4135  6134  TST92,  CLEN                    /CLEAR ENABLES
4136  6135        CLSA
4137  7200        CLA
4140  6133        CLAB                     /CLEAR BUF
4141  1074        TAD     K0003
4142  6134        CLEN                     /ENABLES CHAN3 INPUT AND INT
4143  2050        ISZ     REGT             /INCREMENT TIMER
4144  7410        SKP                      /NOT DONE YET
4145  5350        JMP     .+3              /TIME OUT
4146  6131        CLSK                     /SKP ON CLOCK INT
4147  5343        JMP     .+4
4150  6135        CLSA                     /CLEAR CLOCK STATUS
4151  7200        CLA
4152  3050        DCA     REGT             /CLEAR REGT
4153  7000        NOP
4154  6136        CLBA                     /GET BUF
4155  7041        CIA
4156  1053        TAD     SEND             /COMPARE
4157  7650        SNA CLA
4160  4427        JMS I   NERROR
4161  4425        JMS I   ERROR            /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
4162  4603        TST92M                   /MESSAGE POINTER
4163  7402        HLT                      /ERROR HALT
4164  7410        SKP                      /TO NEXT TEST
4165  4135        TST92                    /ISZ LOOP; SCOPE LOOP
4166  7340        CLA CLL CMA              /SET AC = 7777
4167  3045        DCA     REGA             /PRESET REGA
```

```
                        /
                        /CHECK THAT CHAN 3 CLEARED COUNTER FROM TEST 92
                        /
4170  6137    TST93,    CLCA                    /GET CNT
4171  3052              DCA     RXED
4172  1052              TAD     RXED
4173  7650              SNA CLA                 /ZERO?
4174  4427              JMS I   NERROR          /CHECK MONITOR
4175  4425              JMS I   ERROR           /CHAN3 INPUT FAILED TO CLEAR CNT
4176  4631              TST93M                  /MESSAGE POINTER
4177  7402              HLT                     /ERROR HALT
4200  7410              SKP                     /TO NEXT TEST
4201  4170              TST93                   /ISZ LOOP; SCOPE LOOP
4202  7340              CLA CLL CMA             /SET AC = 7777
4203  3045              DCA     REGA            /PRESET REGA
4204  2046              ISZ     REGB            /DO TESTS 90-93 40 TIMES
4205  5463              JMP I   TST90N          /TO TEST 90
4206  1144              TAD     M0040
4207  3045              DCA     REGA            /PRESET REGA

                        /
                        /CHECK THAT O'FLO ALWAYS TRANSFERS BUFFER TO COUNTER ON MODE 2(1)
                        /
4210  1135    TST94,    TAD     K6000           /GET 6000
4211  3050              DCA     REGT            /SET UP TIMER
4212  1214              TAD     K7300           /GET PRESET
4213  6133              CLAB                    /PRESET BUFFER
4214  7300    K7300,    CLA CLL
4215  1107              TAD     K0100           /GET RATE
4216  6132              CLLR                    /START CLOCK
4217  6134              CLEN
4220  1125              TAD     K2000           /GET ENABLES
4221  6132              CLLR                    /
4222  6131              CLSK                    /WAIT FOR INTERRUPT
4223  5222              JMP     .-1             /
4224  2050              ISZ     REGT            /WAIT FOR ANOTHER OVERFLOW
4225  5224              JMP     .-1             /22 MSEC DELAY
4226  7200              CLA
4227  6132              CLLR
4230  6134              CLEN
4231  6135              CLSA
4232  6137              CLCA                    /GET THE COUNTER
4233  7440              SZA                     /0 IS OK
4234  7710              SPA CLA                 /COUNTER SHOULD NEVER GO POSITIVE
4235  4427              JMS I   NERROR          /
4236  4425              JMS I   ERROR           /ECO EM12-00034 IS EITHER NOT INSTALLED OR NOT WORKING
4237  4657              TST94M                  /
4240  7402              HLT                     /
4241  7410              SKP                     /
4242  4210              TST94                   /
```

```
                        /
                        /
                        /TEST THAT THE CLOCK COUNTER IS INCREMENTED
                        / BY 1 WITH AN I-O PRESET

4243  7300      TST95,  CLA CLL
4244  3045              DCA     REGA            /CLEAR REGA
4245  3053              DCA     SEND            /PRESET SEND TO 0000
4246  6132              CLLR                    /CLEAR CLOCK
4247  1107              TAD     K0100           /GET 0100
4250  6132              CLLR                    /
4251  6135              CLSA                    /
4252  7300              CLA CLL
4253  6133              CLAB                    /LOAD PRESET BUFFER
4254  7300              CLA CLL
4255  1111              TAD     K0200           /GET 0200
4256  6134              CLEN                    /ENABLE
4257  4157      TST95N, CLEAR                   /GENERATE I-O PRESET
4260  2053              ISZ     SEND            /INCREMENT DATA
4261  7000              NOP
4262  6137              CLCA                    /READ COUNTER
4263  3052              DCA     RXED            /SAVE VALUE
4264  1052              TAD     RXED            /GET IT BACK
4265  7041              CIA                     /NEGATE IT
4266  1053              TAD     SEND            /ADD EXPECTED VALUE
4267  7650              SNA CLA                 /ARE THEY EQUAL ?
4270  4427              JMS I   NERROR          /YES, NO ERROR
4271  4425              JMS I   ERROR           /NO, ECO EM12-00055 IS NOT INSTALLED
                                                / OR NOT WORKING CORRECTLY
4272  4716              TST95M                  /
4273  7402              HLT                     /
4274  7410              SKP                     /
4275  4257              TST95N                  /

                        /
                        /ALERT OPERATOR OF PASS COMPLETION
                        /SUPRESS PRINTOUT IF RSW 06 = 1
                        /
4276  2031      TST96,  ISZ     PASS            /INCREMENT PASS
4277  7000              NOP                     /DON'T SKIP
4300  7604              LAS                     /READ SWITCHES
4301  0104              AND     K0040           /PICK OUT RSW 06
4302  7640              SZA CLA                 /SET?
4303  5176              JMP     176             /YES, NO PRINTOUT
4304  1043              TAD     PNTJ            /GET POINTER
4305  3425              DCA I   ERROR           /CHEAT MONITOR
4306  5430              JMP I   OUTPAS          /GO TYPE ALARM
4307  4755      LOCJ,   TST96M                  /MESSAGE POINTER
                        /
                        /RETURN TO LOC 176 FROM ASCII TYPEOUT (MONITOR WILL HANDLE LINK)
                        /
```

```
                5000    *5000
                        /
                        /NON ERROR MONITOR DETERMINES IF OPERATOR WANTS TO LOOP ON NONFAILING TEST
5000  0000      NERROS, 0                       /RETURN ADDRESS
5001  7307              CLA CLL IAC RTL         /SET AC = 4
5002  1200              TAD     NERROS          /GET RETURN ADDRESS
5003  3200              DCA     NERROS          /UPDATE RETURN ADDRESS
5004  1600              TAD I   NERROS          /GET SCOPE LOOP ADDRESS
5005  3220              DCA     ERRORS          /STORE IT
5006  2045              ISZ     REGA            /UPDATE DATA
5007  5620              JMP I   ERRORS          /EXIT
5010  7604              LAS                     /READ SWITCHES
5011  0115              AND     K0400           /SAVE SR3
5012  7640              SZA CLA                 /TEST AND CLEAR
5013  5620              JMP I   ERRORS          / LOOPING
5014  7040              CMA                     /SET AC=-1
5015  1200              TAD     NERROS          /ADD NERRORS
5016  3200              DCA     NERROS          /STORE IN NERRORS
5017  5600              JMP I   NERROS          /JUMP INDIRECT LOOP
                        /
                        /ERROR PROCESSOR, SCOPE LOOP, HALT, PRINT
5020  0000      ERRORS, 0                       /RETURN ADDRESS STORAGE
5021  7604              LAS                     /READ SWITCHES
5022  7004              RAL                     /MOVE SR1 INTO AC00
5023  7700              SMA CLA                 /IS IT SET
5024  5251              JMP     ASCII           /NO TYPE A MESSAGE
5025  4421              JMS I   BELL            /RING THE BELL
5026  1220      ASCRXT, TAD     ERRORS          /GET CURRENT ERROR ADDRESS
5027  7041              CIA                     /INVERT IT
5030  3026              DCA     LSTERR          /STORE IN LAST ERROR
5031  2220              ISZ     ERRORS          /YES INDEX ESCAPE
5032  7604              LAS                     /READ SWITCHES
5033  7700              SMA CLA                 /IS SR0 SET
5034  7402              HLT                     /NO, ERROR HALT
5035  2220              ISZ     ERRORS          /YES INDEX ESCAPE TO JUMP OUT
5036  2220              ISZ     ERRORS          /INDEX ERRORS TO SCOPE MODE
5037  1620              TAD I   ERRORS          /GET SCOPE ADDRESS
5040  3200              DCA     NERROS          /STORE IN TYPE
5041  7604              LAS                     /READ SWITCHES
5042  7006              RTL                     /MOVE SR02 TO AC0
5043  7710              SPA CLA                 /IS SCOPE MODE SELECTED
5044  5600              JMP I   NERROS          /YES CONTINUE IN SCOPE LOOP
5045  7040              CMA                     /NO SET AC=7777 (-1)
5046  1220              TAD     ERRORS          /SUBTRACT ONE FROM ERRORS
5047  3220              DCA     ERRORS          /STORE SELECTED ADDRESS
5050  5620              JMP I   ERRORS          /EXIT TO NEXT TEST
```

```
5051  7240    ASCII,  CLA CMA                 /SET C(AC)=-1
5052  1620            TAD I   ERRORS          /GET MESSAGE ADDRESS STORAGE
5053  3010            DCA     PINT            /STORE IT IN AUTO INDEX REGISTER
5054  1220            TAD     ERRORS          /GET RETURN ADDRESS
5055  1026            TAD     LSTERR          /SUBTRACT LAST ERROR ADDRESS
5056  7650            SNA CLA                 /TEST
5057  5363            JMP     DATYP           /SAME GO TYPE DATA
5060  1410            TAD I   PINT           /GET FIRST CHARACTER
5061  3200            DCA     NERROS          /SAVE IT
5062  1200            TAD     NERROS          /GET IT
5063  7450            SNA                     /TEST IT
5064  5226            JMP     ASCRXT          /NUMBER=EXIT,
5065  7040            CMA                     /INVERT IT
5066  7450            SNA                     /NUMBER=EXITA
5067  5315            JMP     DATUM           /TYPE OUT DATA ROUTINE
5070  7040            CMA                     /CHANGE IT BACK
5071  7112            RTR CLL                 /SWAP AC TO THE RIGHT
5072  7012            RTR                     /MOVE
5073  7012            RTR                     /MOVE
5074  4300            JMS     TYPECH          /TYPE IT
5075  1200            TAD     NERROS          /GET IT AGAIN
5076  4300            JMS     TYPECH          /TYPE IT
5077  5260            JMP     ASCII+7         /MUST BE MORE WORDS THAT NEED TYPING
5100  0000    TYPECH, 0
5101  0106            AND     K0077           /SAVE SIGNIFICENT PART
5102  3055            DCA     SPACE           /STORE WORD
5103  1055            TAD     SPACE           /FETCH IT
5104  7650            SNA CLA                 /TEST FOR 00 CRLF CODE
5105  4354            JMS     CRLF            /YES IT WAS
5106  1055            TAD     SPACE           /NO TYPE IT
5107  1144            TAD     M0040           /SUBTRACT 40
5110  7510            SPA                     /TEST POLARITY
5111  1107            TAD     K0100           /ADD 340
5112  1112            TAD     K240            /ADD 240
5113  4464            JMS I   TYPE            /TYPE
5114  5700            JMP I   TYPECH          /EXIT
```

```
5115  1410    DATUM,  TAD I   PINT            /GET ADDRESS OF REGISTER
5116  3200            DCA     NERROS          /STORE IN TEMP
5117  1200            TAD     NERROS          /GET TEMP
5120  7650            SNA CLA                 /TEST FOR EXIT
5121  5226            JMP     ASCRXT          /EQUALS 0000 EXIT
5122  1200            TAD     NERROS          /GET TEMP
5123  1155            TAD     M4444           /$$?
5124  7650            SNA CLA                 /TEST
5125  5176            JMP     176             /SPECIAL RESTART
5126  1600            TAD I   NERROS          /GET DATA
5127  4333            JMS     OCTYP           /TYPE IT
5130  1112            TAD     K240            /SPACE
5131  4464            JMS I   TYPE            /TYPE IT
5132  5315            JMP     DATUM           /TYPE NUMERIC DATA
5133  0000    OCTYP,  0                       /RETURN ADDRESS STORAGE
5134  3300            DCA     TYPECH          /STORE DATA TO BE PRINTED
5135  1136            TAD     K7774           /SET UP TALLY
5136  3055            DCA     SPACE           /SET IT
5137  1123    HERE,   TAD     K1026           /GET FLAG NUMBER
5140  3354    REDO,   DCA     CRLF            /STORE
5141  1300            TAD     TYPECH
5142  7004            RAL
5143  3300            DCA     TYPECH
5144  1354            TAD     CRLF
5145  7004            RAL
5146  7420            SNL
5147  5340            JMP     REDO
5150  4464            JMS I   TYPE
5151  2055            ISZ     SPACE
5152  5337            JMP     HERE
5153  5733            JMP I   OCTYP           /EXIT
5154  0000    CRLF,   0                       /RETURN ADDRESS STORAGE
5155  1374            TAD     K0215           /GET CR
5156  4464            JMS I   TYPE            /TYPE IT
5157  1375            TAD     K0212           /GET LF
5160  4464            JMS I   TYPE            /TYPE IT
5161  1110            TAD     K0177           /SET TO RUBOUT
5162  5754            JMP I   CRLF            /EXIT
5163  1410    DATYP,  TAD I   PINT            /GET A TERM OFF OF TYPE LIST
5164  7450            SNA                     /END OF LIST?
5165  5226            JMP     ASCRXT          /YES EXIT
5166  7040            CMA                     /INVERT
5167  7640            SZA CLA                 /BEGINNING OF DATA
5170  5363            JMP     DATYP           /NO
5171  4354            JMS     CRLF            /YES OK RETURN THE TTY CARRIAGE AND LINE FEED
5172  7300            CLA CLL                 /CLEAR AC AND LINK
5173  5315            JMP     DATUM           /GO TYPE THE DATA
5174  0215    K0215,  0215
5175  0212    K0212,  0212
```

```
      5200                *5200
5200  0000    BELLS,      0                       /RING THE BELL
5201  7604                LAS
5202  0107                AND     K0100
5203  7640                SZA CLA
5204  5600                JMP I   BELLS
5205  1076                TAD     K0007
5206  4464                JMS I   TYPE
5207  5600                JMP I   BELLS
5210  0000    RANDY,      0
5211  1240                TAD     RNA             /RANDOM NUMBER GENERATOR
5212  1241                TAD     RNB
5213  1242                TAD     RNC
5214  1133                TAD     K5252
5215  3240                DCA     RNA
5216  7004                RAL
5217  1240                TAD     RNA
5220  1241                TAD     RNB
5221  1242                TAD     RNC
5222  1133                TAD     K5252
5223  3241                DCA     RNB
5224  7004                RAL
5225  1240                TAD     RNA
5226  1241                TAD     RNB
5227  1242                TAD     RNC
5230  1133                TAD     K5252
5231  3242                DCA     RNC
5232  7004                RAL
5233  1240                TAD     RNA
5234  3240                DCA     RNA
5235  1241                TAD     RNB
5236  1242                TAD     RNC
5237  5610                JMP I   RANDY
5240  7601    RNA,        7601
5241  3542    RNB,        3542
5242  3755    RNC,        3755

5243  0000    TYPOUT,     0
5244  6046                TLS
5245  6041                TSF
5246  5245                JMP     .-1
5247  6042                TCF                     /CLEAR FLAG
5250  7300                CLA CLL
5251  5643                JMP I   TYPOUT
5252  0000    SETN,       0                       /RESET PASS COUNTER
5253  7300                CLA CLL
5254  3031                DCA     PASS
5255  3045                DCA     REGA
5256  3046                DCA     REGB
5257  3026                DCA     LSTERR
5260  5652                JMP I   SETN
```

```
                        /
                        /TEXT TEST ERROR MESSAGES
                        /
5261  0024    TST10M, 0024                    /TST10 CLAB CHANGED AC
5262  2324            2324
5263  6160            6160
5264  4003            4003
5265  1401            1401
5266  0240            0240
5267  0310            0310
5270  0116            0116
5271  0705            0705
5272  0440            0440
5273  0103            0103
5274  4000            4000
5275  7777            EXITA
5276  0045            REGA
5277  0052            RXED
5300  0000            EXIT

5301  0024    TST11M, 0024                    /TST11 CLBA FAILED
5302  2324            2324
5303  6161            6161
5304  4003            4003
5305  1402            1402
5306  0140            0140
5307  0601            0601
5310  1114            1114
5311  0504            0504
5312  4000            4000
5313  7777            EXITA
5314  0053            SEND
5315  0052            RXED
5316  0000            EXIT

5317  0024    TST12M, 0024                    /TST12 CLAB FAILED
5320  2324            2324
5321  6162            6162
5322  4003            4003
5323  1401            1401
5324  0240            0240
5325  0601            0601
5326  1114            1114
5327  0504            0504
5330  4000            4000
5331  7777            EXITA
5332  0053            SEND
5333  0052            RXED
5334  0000            EXIT

5335  0024    TST13M, 0024                    /TST13 CLAB FAILED
5336  2324            2324
5337  6163            6163
5340  4003            4003
5341  1401            1401
```

```
5342  0240            0240
5343  0601            0601
5344  1114            1114
5345  0504            0504
5346  4000            4000
5347  7777            EXITA
5350  0045            REGA
5351  0052            RXED
5352  0000            EXIT

5353  0024    TST14M, 0024                    /TST14 CLAB FAILED
5354  2324            2324
5355  6164            6164
5356  4003            4003
5357  1401            1401
5360  0240            0240
5361  0601            0601
5362  1114            1114
5363  0504            0504
5364  4000            4000
5365  7777            EXITA
5366  0053            SEND
5367  0052            RXED
5370  0000            EXIT

5371  0024    TST15M, 0024                    /TST15 CLBA CHANGED BUFFER
5372  2324            2324
5373  6165            6165
5374  4003            4003
5375  1402            1402
5376  0140            0140
5377  0310            0310
5400  0116            0116
5401  0705            0705
5402  0440            0440
5403  0225            0225
5404  0606            0606
5405  0522            0522
5406  4000            4000
5407  7777            EXITA
5410  0053            SEND
5411  0052            RXED
5412  0000            EXIT

5413  0024    TST16M, 0024                    /TST16 CLAB <> CLBA FAILED
5414  2324            2324
5415  6166            6166
5416  4003            4003
5417  1401            1401
5420  0274            0274
5421  7603            7603
5422  1402            1402
5423  0140            0140
5424  0601            0601
5425  1114            1114
```

```
5426  0504            0504
5427  4000            4000
5430  7777            EXITA
5431  0045            REGA
5432  0052            RXED
5433  0000            EXIT

5434  0024    TST17M, 0024                    /TST17 CLAB <> CLBA FAILED
5435  2324            2324
5436  6167            6167
5437  4003            4003
5440  1401            1401
5441  0274            0274
5442  7603            7603
5443  1402            1402
5444  0140            0140
5445  0601            0601
5446  1114            1114
5447  0504            0504
5450  4000            4000
5451  7777            EXITA
5452  0053            SEND
5453  0052            RXED
5454  0000            EXIT

5455  0024    TST18M, 0024                    /TST18 CLAB <> CLBA FAILED
5456  2324            2324
5457  6170            6170
5460  4003            4003
5461  1401            1401
5462  0274            0274
5463  7603            7603
5464  1402            1402
5465  0140            0140
5466  0601            0601
5467  1114            1114
5470  0504            0504
5471  4000            4000
5472  7777            EXITA
5473  0053            SEND
5474  0052            RXED
5475  0000            EXIT

5476  0024    TST19M, 0024                    /TST19 CLEN CHANGED AC
5477  2324            2324
5500  6171            6171
5501  4003            4003
5502  1405            1405
5503  1640            1640
5504  0310            0310
5505  0116            0116
5506  0705            0705
5507  0440            0440
5510  0103            0103
5511  4000            4000
```

```
5512  7777          EXITA
5513  0045          REGA
5514  0052          RXED
5515  0000          EXIT

5516  0024  TST20M, 0024                  /TST20 CLEN CHANGED BUFFER
5517  2324          2324
5520  6260          6260
5521  4003          4003
5522  1405          1405
5523  1640          1640
5524  0310          0310
5525  0116          0116
5526  0705          0705
5527  0440          0440
5530  0225          0225
5531  0606          0606
5532  0522          0522
5533  4000          4000
5534  7777          EXITA
5535  0045          REGA
5536  0052          RXED
5537  0000          EXIT

5540  0024  TST21M, 0024                  /TST21 CLCA FAILED
5541  2324          2324
5542  6261          6261
5543  4003          4003
5544  1403          1403
5545  0140          0140
5546  0601          0601
5547  1114          1114
5550  0504          0504
5551  4000          4000
5552  7777          EXITA
5553  0053          SEND
5554  0052          RXED
5555  0000          EXIT

5556  0024  TST22M, 0024                  /TST22 "CLR CNT" FAILED
5557  2324          2324
5560  6262          6262
5561  4042          4042
5562  0314          0314
5563  2240          2240
5564  0316          0316
5565  2442          2442
5566  4006          4006
5567  0111          0111
5570  1405          1405
5571  0400          0400
5572  7777          EXITA
5573  0053          SEND
5574  0052          RXED
5575  0000          EXIT
```

```
5576  0024    TST23M, 0024                    /TST23 CLEN FAILED
5577  2324            2324
5600  6263            6263
5601  4003            4003
5602  1405            1405
5603  1640            1640
5604  0601            0601
5605  1114            1114
5606  0504            0504
5607  4000            4000
5610  7777            EXITA
5611  0045            REGA
5612  0052            RXED
5613  0000            EXIT

5614  0024    TST24M, 0024                    /TST24 CLEN FAILED
5615  2324            2324
5616  6264            6264
5617  4003            4003
5620  1405            1405
5621  1640            1640
5622  0601            0601
5623  1114            1114
5624  0504            0504
5625  4000            4000
5626  7777            EXITA
5627  0053            SEND
5630  0052            RXED
5631  0000            EXIT

5632  0024    TST25M, 0024                    /TST25 CLCA CHANGES COUNT
5633  2324            2324
5634  6265            6265
5635  4003            4003
5636  1403            1403
5637  0140            0140
5640  0310            0310
5641  0116            0116
5642  0705            0705
5643  2340            2340
5644  0317            0317
5645  2516            2516
5646  2400            2400
5647  7777            EXITA
5650  0053            SEND
5651  0052            RXED
5652  0000            EXIT

5653  0024    TST26M, 0024                    /TST26 BUFFER <> COUNTER FAILED
5654  2324            2324
5655  6266            6266
5656  4002            4002
5657  2506            2506
5660  0605            0605
```

```
5661  2274            2274
5662  7603            7603
5663  1725            1725
5664  1624            1624
5665  0522            0522
5666  4006            4006
5667  0111            0111
5670  1405            1405
5671  0400            0400
5672  7777            EXITA
5673  0053            SEND
5674  0052            RXED
5675  0000            EXIT

5676  0024    TST27M, 0024                    /TST27 "LOAD CNT" FAILS TO "OR"
5677  2324            2324
5700  6267            6267
5701  4042            4042
5702  1417            1417
5703  0104            0104
5704  4003            4003
5705  1624            1624
5706  4240            4240
5707  0601            0601
5710  1114            1114
5711  2340            2340
5712  2417            2417
5713  4042            4042
5714  1722            1722
5715  4200            4200
5716  7777            EXITA
5717  0053            SEND
5720  0052            RXED
5721  0000            EXIT

5722  0024    TST28M, 0024                    /TST28 "LOAD CNT" LOADED IN ERROR
5723  2324            2324
5724  6270            6270
5725  4042            4042
5726  1417            1417
5727  0104            0104
5730  4003            4003
5731  1624            1624
5732  4240            4240
5733  1417            1417
5734  0104            0104
5735  0504            0504
5736  4011            4011
5737  1640            1640
5740  0522            0522
5741  2217            2217
5742  2200            2200
5743  7777            EXITA
5744  0053            SEND
5745  0052            RXED
```

```
5746  0000            EXIT
5747  0024  TST29M,  0024                    /TST29 "LOAD CNT" LOADED IN ERROR
5750  2324            2324
5751  6271            6271
5752  4042            4042
5753  1417            1417
5754  0104            0104
5755  4003            4003
5756  1624            1624
5757  4240            4240
5760  1417            1417
5761  0104            0104
5762  0504            0504
5763  4011            4011
5764  1640            1640
5765  0522            0522
5766  2217            2217
5767  2200            2200
5770  7777            EXITA
5771  0053            SEND
5772  0052            RXED
5773  0000            EXIT

5774  0024  TST30M,  0024                    /TST30 MODE REG CAUSES "LOAD CNT"
5775  2324            2324
5776  6360            6360
5777  4015            4015
6000  1704            1704
6001  0540            0540
6002  2205            2205
6003  0740            0740
6004  0301            0301
6005  2523            2523
6006  0523            0523
6007  4042            4042
6010  1417            1417
6011  0104            0104
6012  4003            4003
6013  1624            1624
6014  4200            4200
6015  7777            EXITA
6016  0053            SEND
6017  0052            RXED
6020  0000            EXIT

6021  0024  TST31M,  0024                    /TST31 MODE REG CAUSES "LOAD CNT" OR "CLR BUF"
6022  2324            2324
6023  6361            6361
6024  4015            4015
6025  1704            1704
6026  0540            0540
6027  2205            2205
6030  0740            0740
6031  0301            0301
6032  2523            2523
```

```
6033  0523            0523
6034  4042            4042
6035  1417            1417
6036  0104            0104
6037  4003            4003
6040  1624            1624
6041  4240            4240
6042  1722            1722
6043  4042            4042
6044  0314            0314
6045  2240            2240
6046  0225            0225
6047  0642            0642
6050  4000            4000
6051  7777            EXITA
6052  0053            SEND
6053  0052            RXED
6054  0046            REGB
6055  0000            EXIT

6056  0024    TST32M, 0024                    /TST32 MODE 2, 1>0 CLOCKED CNTR
6057  2324            2324
6060  6362            6362
6061  4015            4015
6062  1704            1704
6063  0540            0540
6064  6272            6272
6065  4061            4061
6066  7660            7660
6067  4003            4003
6070  1417            1417
6071  0313            0313
6072  0504            0504
6073  4003            4003
6074  1624            1624
6075  2200            2200
6076  7777            EXITA
6077  0053            SEND
6100  0052            RXED
6101  0000            EXIT

6102  0024    TST33M, 0024                    /TST33 MODE 2, 0>1 CLOCKED CNTR
6103  2324            2324
6104  6363            6363
6105  4015            4015
6106  1704            1704
6107  0540            0540
6110  6272            6272
6111  4060            4060
6112  7661            7661
6113  4003            4003
6114  1417            1417
6115  0313            0313
6116  0504            0504
6117  4003            4003
```

```
6120  1624            1624
6121  2200            2200
6122  7777            EXITA
6123  0071            K0000
6124  0052            RXED
6125  0000            EXIT

6126  0024    TST34M, 0024                    /TST34 O'FLO FAILED TO SET O'FLO FLOP
6127  2324            2324
6130  6364            6364
6131  4017            4017
6132  4706            4706
6133  1417            1417
6134  4006            4006
6135  0111            0111
6136  1405            1405
6137  0440            0440
6140  2417            2417
6141  4023            4023
6142  0524            0524
6143  4017            4017
6144  4706            4706
6145  1417            1417
6146  4006            4006
6147  1417            1417
6150  2000            2000
6151  0000            EXIT

6152  0024    TST35M, 0024                    /TST35 CLSA FAILED TO CLEAR O'FLO FLOP
6153  2324            2324
6154  6365            6365
6155  4003            4003
6156  1423            1423
6157  0140            0140
6160  0601            0601
6161  1114            1114
6162  0504            0504
6163  4024            4024
6164  1740            1740
6165  0314            0314
6166  0501            0501
6167  2240            2240
6170  4017            4017
6171  4706            4706
6172  1417            1417
6173  4006            4006
6174  1417            1417
6175  2000            2000
6176  0000            EXIT

6177  0024    TST36M, 0024                    /TST36 CLSK SKIPPED IN ERROR
6200  2324            2324
6201  6366            6366
6202  4003            4003
6203  1423            1423
```

```
6204  1340            1340
6205  2313            2313
6206  1120            1120
6207  2005            2005
6210  0440            0440
6211  1116            1116
6212  4005            4005
6213  2222            2222
6214  1722            1722
6215  4000            4000
6216  0000            EXIT

6217  0024    TST37M, 0024                    /TST37 ILLEGAL CLOCK INTERRUPT!
6220  2324            2324
6221  6367            6367
6222  4011            4011
6223  1414            1414
6224  0507            0507
6225  0114            0114
6226  4003            4003
6227  1417            1417
6230  0313            0313
6231  4011            4011
6232  1624            1624
6233  0522            0522
6234  2225            2225
6235  2024            2024
6236  4100            4100
6237  0000            EXIT

6240  0024    TST38M, 0024                    /TST38 CLSK FAILED TO SKIP
6241  2324            2324
6242  6370            6370
6243  4003            4003
6244  1423            1423
6245  1340            1340
6246  0601            0601
6247  1114            1114
6250  0504            0504
6251  4024            4024
6252  1740            1740
6253  2313            2313
6254  1120            1120
6255  4000            4000
6256  0000            EXIT

6257  0024    TST39M, 0024                    /TST39 CLOCK INTERRUPT FAILED
6260  2324            2324
6261  6371            6371
6262  4003            4003
6263  1417            1417
6264  0313            0313
6265  4011            4011
6266  1624            1624
6267  0522            0522
```

```
6270  2225            2225
6271  2024            2024
6272  4006            4006
6273  0111            0111
6274  1405            1405
6275  0400            0400
6276  0000            EXIT

6277  0024    TST40M, 0024                    /TST40 O'FLO ENABLE WON'T ZERO
6300  2324            2324
6301  6460            6460
6302  4017            4017
6303  4706            4706
6304  1417            1417
6305  4005            4005
6306  1601            1601
6307  0214            0214
6310  0540            0540
6311  2717            2717
6312  1647            1647
6313  2440            2440
6314  3205            3205
6315  2217            2217
6316  4000            4000
6317  0000            EXIT

6320  0024    TST41M, 0024                    /TST41 O'FLO FLAG WON'T CLEAR
6321  2324            2324
6322  6461            6461
6323  4017            4017
6324  4706            4706
6325  1417            1417
6326  4006            4006
6327  1401            1401
6330  0740            0740
6331  2717            2717
6332  1647            1647
6333  2440            2440
6334  0314            0314
6335  0501            0501
6336  2200            2200
6337  0000            EXIT

6340  0024    TST42M, 0024                    /TST42 CLOCK INTR WON'T CLEAR
6341  2324            2324
6342  6462            6462
6343  4003            4003
6344  1417            1417
6345  0313            0313
6346  4011            4011
6347  1624            1624
6350  2240            2240
6351  2717            2717
6352  1647            1647
6353  2440            2440
```

```
6354  0314          0314
6355  0501          0501
6356  2200          2200
6357  0000          EXIT

6360  0024    TST43M, 0024                  /TST43 BIT 11 FAILED,
6361  2324          2324
6362  6463          6463
6363  4002          4002
6364  1124          1124
6365  4061          4061
6366  6140          6140
6367  0601          0601
6370  1114          1114
6371  0504          0504
6372  5600          5600
6373  7777          EXITA
6374  0053          SEND
6375  0052          RXED
6376  0000          EXIT

6377  0024    TST44M, 0024                  /TST44 BIT 10 FAILED,
6400  2324          2324
6401  6464          6464
6402  4002          4002
6403  1124          1124
6404  4061          4061
6405  6040          6040
6406  0601          0601
6407  1114          1114
6410  0504          0504
6411  5600          5600
6412  7777          EXITA
6413  0053          SEND
6414  0052          RXED
6415  0000          EXIT

6416  0024    TST45M, 0024                  /TST45 BIT 09 FAILED,
6417  2324          2324
6420  6465          6465
6421  4002          4002
6422  1124          1124
6423  4060          4060
6424  7140          7140
6425  0601          0601
6426  1114          1114
6427  0504          0504
6430  5600          5600
6431  7777          EXITA
6432  0053          SEND
6433  0052          RXED
6434  0000          EXIT

6435  0024    TST46M, 0024                  /TST46 BIT 08 FAILED,
6436  2324          2324
```

```
6437  6466            6466
6440  4002            4002
6441  1124            1124
6442  4060            4060
6443  7040            7040
6444  0601            0601
6445  1114            1114
6446  0504            0504
6447  5600            5600
6450  7777            EXITA
6451  0053            SEND
6452  0052            RXED
6453  0000            EXIT

6454  0024    TST47M, 0024                    /TST47 BIT 07 FAILED.
6455  2324            2324
6456  6467            6467
6457  4002            4002
6460  1124            1124
6461  4060            4060
6462  6740            6740
6463  0601            0601
6464  1114            1114
6465  0504            0504
6466  5600            5600
6467  7777            EXITA
6470  0053            SEND
6471  0052            RXED
6472  0000            EXIT

6473  0024    TST48M, 0024                    /TST48 BIT 06 FAILED.
6474  2324            2324
6475  6470            6470
6476  4002            4002
6477  1124            1124
6500  4060            4060
6501  6640            6640
6502  0601            0601
6503  1114            1114
6504  0504            0504
6505  5600            5600
6506  7777            EXITA
6507  0053            SEND
6510  0052            RXED
6511  0000            EXIT

6512  0024    TST49M, 0024                    /TST49 BIT 05 FAILED.
6513  2324            2324
6514  6471            6471
6515  4002            4002
6516  1124            1124
6517  4060            4060
6520  6540            6540
6521  0601            0601
6522  1114            1114
```

```
6523  0504            0504
6524  5600            5600
6525  7777            EXITA
6526  0053            SEND
6527  0052            RXED
6530  0000            EXIT

6531  0024    TST50M, 0024                    /TST50 BIT 04 FAILED.
6532  2324            2324
6533  6560            6560
6534  4002            4002
6535  1124            1124
6536  4060            4060
6537  6440            6440
6540  0601            0601
6541  1114            1114
6542  0504            0504
6543  5600            5600
6544  7777            EXITA
6545  0053            SEND
6546  0052            RXED
6547  0000            EXIT

6550  0024    TST51M, 0024                    /TST51 BIT 03 FAILED.
6551  2324            2324
6552  6561            6561
6553  4002            4002
6554  1124            1124
6555  4060            4060
6556  6340            6340
6557  0601            0601
6560  1114            1114
6561  0504            0504
6562  5600            5600
6563  7777            EXITA
6564  0053            SEND
6565  0052            RXED
6566  0000            EXIT

6567  0024    TST52M, 0024                    /TST52 BIT 02 FAILED.
6570  2324            2324
6571  6562            6562
6572  4002            4002
6573  1124            1124
6574  4060            4060
6575  6240            6240
6576  0601            0601
6577  1114            1114
6600  0504            0504
6601  5600            5600
6602  7777            EXITA
6603  0053            SEND
6604  0052            RXED
6605  0000            EXIT
```

```
6606  0024    TST53M, 0024                    /TST53 BIT 01 FAILED.
6607  2324            2324
6610  6563            6563
6611  4002            4002
6612  1124            1124
6613  4060            4060
6614  6140            6140
6615  0601            0601
6616  1114            1114
6617  0504            0504
6620  5600            5600
6621  7777            EXITA
6622  0053            SEND
6623  0052            RXED
6624  0000            EXIT

6625  0024    TST54M, 0024                    /TST54 BIT 00 FAILED
6626  2324            2324
6627  6564            6564
6630  4002            4002
6631  1124            1124
6632  4060            4060
6633  6040            6040
6634  0601            0601
6635  1114            1114
6636  0504            0504
6637  5600            5600
6640  7777            EXITA
6641  0053            SEND
6642  0052            RXED
6643  0000            EXIT

6644  0024    TST55M, 0024                    /TST55 RATE 400KC FAILS
6645  2324            2324
6646  6565            6565
6647  4022            4022
6650  0124            0124
6651  0540            0540
6652  6460            6460
6653  6013            6013
6654  0340            0340
6655  0601            0601
6656  1114            1114
6657  2300            2300
6660  0000            EXIT

6661  0024    TST56M, 0024                    /TST56 RATE 100KC FAILS
6662  2324            2324
6663  6566            6566
6664  4022            4022
6665  0124            0124
6666  0540            0540
6667  6160            6160
6670  6013            6013
6671  0340            0340
```

```
6672  0601            0601
6673  1114            1114
6674  2300            2300
6675  0000            EXIT

6676  0024    TST57M, 0024                    /TST57 RATE 10KC FAILS
6677  2324            2324
6700  6567            6567
6701  4022            4022
6702  0124            0124
6703  0540            0540
6704  6160            6160
6705  1303            1303
6706  4006            4006
6707  0111            0111
6710  1423            1423
6711  4000            4000
6712  0000            EXIT

6713  0024    TST58M, 0024                    /TST58 RATE 1KC FAILS
6714  2324            2324
6715  6570            6570
6716  4022            4022
6717  0124            0124
6720  0540            0540
6721  6113            6113
6722  0340            0340
6723  0601            0601
6724  1114            1114
6725  2300            2300
6726  0000            EXIT

6727  0024    TST59M, 0024                    /TST59 RATE 100CPS FAILS
6730  2324            2324
6731  6570            6570
6732  4022            4022
6733  0124            0124
6734  0540            0540
6735  6160            6160
6736  6003            6003
6737  2023            2023
6740  4006            4006
6741  0111            0111
6742  1423            1423
6743  4000            4000
6744  0000            EXIT

6745  0024    TST60M, 0024                    /TST60 CHAN 1 INPUT LOCKED OUT
6746  2324            2324
6747  6660            6660
6750  0003            0003
6751  1001            1001
6752  1640            1640
6753  6140            6140
6754  1116            1116
```

```
6755  2025            2025
6756  2440            2440
6757  1417            1417
6760  0313            0313
6761  0504            0504
6762  4017            4017
6763  2524            2524
6764  4000            4000
6765  0000            EXIT

6766  0024    TST61M, 0024                    /TST61 CHAN 3 WON'T TOGGLE
6767  2324            2324
6770  6661            6661
6771  4003            4003
6772  1001            1001
6773  1640            1640
6774  6340            6340
6775  2717            2717
6776  1647            1647
6777  2440            2440
7000  2417            2417
7001  0707            0707
7002  1405            1405
7003  4000            4000
7004  7777            EXITA
7005  0053            SEND
7006  0052            RXED
7007  0000            EXIT

7010  0024    TST62M, 0024                    /TST62 CHAN 2 WON'T TOGGLE
7011  2324            2324
7012  6662            6662
7013  4003            4003
7014  1001            1001
7015  1640            1640
7016  6240            6240
7017  2717            2717
7020  1647            1647
7021  2440            2440
7022  2417            2417
7023  0707            0707
7024  1405            1405
7025  4000            4000
7026  7777            EXITA
7027  0053            SEND
7030  0052            RXED
7031  0000            EXIT

7032  0024    TST63M, 0024                    /TST63 CHAN 1 WON'T TOGGLE
7033  2324            2324
7034  6663            6663
7035  4003            4003
7036  1001            1001
7037  1640            1640
7040  6140            6140
```

```
7041  2717            2717
7042  1647            1647
7043  2440            2440
7044  2417            2417
7045  0707            0707
7046  1405            1405
7047  4000            4000
7050  7777            EXITA
7051  0053            SEND
7052  0052            RXED
7053  0000            EXIT

7054  0024    TST64M, 0024                    /TST64 CHAN 1 WON'T INTR
7055  2324            2324
7056  6664            6664
7057  4003            4003
7060  1001            1001
7061  1640            1640
7062  4061            4061
7063  4027            4027
7064  1716            1716
7065  4724            4724
7066  4011            4011
7067  1624            1624
7070  2200            2200
7071  0000            EXIT

7072  0024    TST65M, 0024                    /TST65 CHAN 1 INTR IN ERROR
7073  2324            2324
7074  6665            6665
7075  4003            4003
7076  1001            1001
7077  1640            1640
7100  4061            4061
7101  4011            4011
7102  1624            1624
7103  2240            2240
7104  1116            1116
7105  4005            4005
7106  2222            2222
7107  1722            1722
7110  4000            4000
7111  0000            EXIT

7112  0024    TST66M, 0024                    /TST66 CHAN 2 WON'T INTR.
7113  2324            2324
7114  6666            6666
7115  4003            4003
7116  1001            1001
7117  1640            1640
7120  6240            6240
7121  2717            2717
7122  1647            1647
7123  2440            2440
7124  1116            1116
```

```
7125  2422            2422
7126  5600            5600
7127  7777            EXITA
7130  0053            SEND
7131  0052            RXED
7132  0000            EXIT

7133  0024    TST67M, 0024                    /TST67 CHAN 2 INTR IN ERROR
7134  2324            2324
7135  6667            6667
7136  4003            4003
7137  1001            1001
7140  1640            1640
7141  6240            6240
7142  1116            1116
7143  2422            2422
7144  4011            4011
7145  1640            1640
7146  0522            0522
7147  2217            2217
7150  2200            2200
7151  0000            EXIT

7152  0024    TST68M, 0024                    /TST68 CHAN 3 WON'T INTR.
7153  2324            2324
7154  6670            6670
7155  4003            4003
7156  1001            1001
7157  1640            1640
7160  6340            6340
7161  2717            2717
7162  1647            1647
7163  2440            2440
7164  1116            1116
7165  2422            2422
7166  5600            5600
7167  7777            EXITA
7170  0053            SEND
7171  0052            RXED
7172  0000            EXIT

7173  0024    TST69M, 0024                    /TST69 CHAN 3 INTR IN ERROR
7174  2324            2324
7175  6671            6671
7176  4003            4003
7177  1001            1001
7200  1640            1640
7201  6340            6340
7202  1116            1116
7203  2422            2422
7204  4011            4011
7205  1640            1640
7206  0522            0522
7207  2217            2217
7210  2200            2200
```

```
7211  0000          EXIT

7212  0024  TST70M, 0024                  /TST70 CHAN 3 INPUT LINE FREQ FAILED
7213  2324          2324
7214  6760          6760
7215  4003          4003
7216  1001          1001
7217  1640          1640
7220  6340          6340
7221  1116          1116
7222  2025          2025
7223  2440          2440
7224  1411          1411
7225  1605          1605
7226  4006          4006
7227  2205          2205
7230  2140          2140
7231  0601          0601
7232  1114          1114
7233  0504          0504
7234  4000          4000
7235  7777          EXITA
7236  0052          RXED
7237  0000          EXIT

7240  0024  TST71M, 0024                  /TST71 CHAN 2 INPUT LINE FREQ FAILED
7241  2324          2324
7242  6761          6761
7243  4003          4003
7244  1001          1001
7245  1640          1640
7246  6240          6240
7247  1116          1116
7250  2025          2025
7251  2440          2440
7252  1411          1411
7253  1605          1605
7254  4006          4006
7255  2205          2205
7256  2140          2140
7257  0601          0601
7260  1114          1114
7261  0504          0504
7262  4000          4000
7263  7777          EXITA
7264  0052          RXED
7265  0000          EXIT

7266  0024  TST72M, 0024                  /TST72 CHAN 1 INPUT LINE FREQ FAILED
7267  2324          2324
7270  6762          6762
7271  4003          4003
7272  1001          1001
7273  1640          1640
7274  6140          6140
```

```
7275  1116            1116
7276  2025            2025
7277  2440            2440
7300  1411            1411
7301  1605            1605
7302  4006            4006
7303  2205            2205
7304  2140            2140
7305  0601            0601
7306  1114            1114
7307  0504            0504
7310  4000            4000
7311  7777            EXITA
7312  0052            RXED
7313  0000            EXIT

7314  0024    TST73M, 0024                    /TST73 FAST SAM FAILS
7315  2324            2324
7316  6763            6763
7317  4006            4006
7320  0123            0123
7321  2440            2440
7322  2301            2301
7323  1540            1540
7324  0601            0601
7325  1114            1114
7326  2300            2300
7327  7777            EXITA
7330  0053            SEND
7331  0052            RXED
7332  0000            EXIT

7333  0024    TST74M, 0024                    /TST74 O'FLO WON'T FAST SAM
7334  2324            2324
7335  6764            6764
7336  4017            4017
7337  4706            4706
7340  1417            1417
7341  4027            4027
7342  1716            1716
7343  4724            4724
7344  4006            4006
7345  0123            0123
7346  2440            2440
7347  2301            2301
7350  1500            1500
7351  7777            EXITA
7352  0053            SEND
7353  0052            RXED
7354  0000            EXIT

7355  0024    TST75M, 0024                    /TST75 FAST SAM WON'T SET
7356  2324            2324
7357  6765            6765
7360  4006            4006
```

```
7361  0123            0123
7362  2440            2440
7363  2301            2301
7364  1540            1540
7365  2717            2717
7366  1647            1647
7367  2440            2440
7370  2305            2305
7371  2400            2400
7372  7777            EXITA
7373  0053            SEND
7374  0052            RXED
7375  0000            EXIT

7376  0024    TST76M, 0024                    /TST76 MODES 2,1 INHIBIT FAST SAM
7377  2324            2324
7400  6766            6766
7401  4015            4015
7402  1704            1704
7403  0523            0523
7404  4062            4062
7405  5561            5561
7406  4011            4011
7407  1610            1610
7410  1102            1102
7411  1124            1124
7412  4006            4006
7413  0123            0123
7414  2440            2440
7415  2301            2301
7416  1500            1500
7417  7777            EXITA
7420  0053            SEND
7421  0052            RXED
7422  0000            EXIT

7423  0024    TST77M, 0024                    /TST78 I/O PRESET WON'T STOP CLOCK
7424  2324            2324                    /(RATE BITS 1 & 2)
7425  6770            6770
7426  4011            4011
7427  3417            3417
7430  4020            4020
7431  2205            2205
7432  2305            2305
7433  2440            2440
7434  2717            2717
7435  1647            1647
7436  2440            2440
7437  2324            2324
7440  1720            1720
7441  4003            4003
7442  1417            1417
7443  0313            0313
7444  4000            4000
7445  5022            5022
```

```
7446  0124            0124
7447  0540            0540
7450  0211            0211
7451  2423            2423
7452  4061            4061
7453  4046            4046
7454  4062            4062
7455  5100            5100
7456  0000            EXIT

7457  0024    TST79M, 0024                    /TST80 I/O PRESET WON'T STOP CLOCK
7460  2324            2324                    /(RATE BIT 00)
7461  7060            7060
7462  4011            4011
7463  3417            3417
7464  4020            4020
7465  2205            2205
7466  2305            2305
7467  2440            2440
7470  2717            2717
7471  1647            1647
7472  2440            2440
7473  2324            2324
7474  1720            1720
7475  4003            4003
7476  1417            1417
7477  0313            0313
7500  4000            4000
7501  5022            5022
7502  0124            0124
7503  0540            0540
7504  0211            0211
7505  2440            2440
7506  6051            6051
7507  4000            4000
7510  0000            EXIT

7511  0024    TST81M, 0024                    /TST81 I/O PRESET WON'T CLEAR O'FLO
7512  2324            2324
7513  7061            7061
7514  4011            4011
7515  3417            3417
7516  4020            4020
7517  2205            2205
7520  2305            2305
7521  2440            2440
7522  2717            2717
7523  1647            1647
7524  2440            2440
7525  0314            0314
7526  0501            0501
7527  2240            2240
7530  1747            1747
7531  0614            0614
7532  1700            1700
```

```
7533  0000            EXIT

7534  0024  TST82M, 0024                  /TST82 I/O PRESET WON'T CLEAR INTERRUPT ENABLE
7535  2324            2324
7536  7062            7062
7537  4011            4011
7540  3417            3417
7541  4020            4020
7542  2205            2205
7543  2305            2305
7544  2440            2440
7545  2717            2717
7546  1647            1647
7547  2440            2440
7550  0314            0314
7551  0501            0501
7552  2240            2240
7553  1116            1116
7554  2405            2405
7555  2222            2222
7556  2520            2520
7557  2440            2440
7560  0516            0516
7561  0102            0102
7562  1405            1405
7563  4000            4000
7564  0000            EXIT

      4310  *LOCJ+1                       /FOLD TEXT BACK INTO FREE CORE AREA

4310  0024  TST83M, 0024                  /TST83 I/O PRESET WON'T CLEAR INPUTS
4311  2324            2324
4312  7063            7063
4313  4011            4011
4314  3417            3417
4315  4020            4020
4316  2205            2205
4317  2305            2305
4320  2440            2440
4321  2717            2717
4322  1647            1647
4323  2440            2440
4324  0314            0314
4325  0501            0501
4326  2240            2240
4327  1116            1116
4330  2025            2025
4331  2423            2423
4332  4000            4000
4333  0000            EXIT

4334  0024  TST84M, 0024                  /TST84 I/O PRESET WON'T CLEAR MODE 2
4335  2324            2324
4336  7064            7064
```

```
4337  4011            4011
4340  3417            3417
4341  4020            4020
4342  2205            2205
4343  2305            2305
4344  2440            2440
4345  2717            2717
4346  1647            1647
4347  2440            2440
4350  0314            0314
4351  0501            0501
4352  2240            2240
4353  1517            1517
4354  0405            0405
4355  4062            4062
4356  4000            4000
4357  0000            EXIT

4360  0024    TST85M, 0024                    /TST85 I/O PRESET WON'T CLEAR MODE 0
4361  2324            2324
4362  7065            7065
4363  4011            4011
4364  3417            3417
4365  4020            4020
4366  2205            2205
4367  2305            2305
4370  2440            2440
4371  2717            2717
4372  1647            1647
4373  2440            2440
4374  0314            0314
4375  0501            0501
4376  2240            2240
4377  1517            1517
4400  0405            0405
4401  4060            4060
4402  4000            4000
4403  7777            EXITA
4404  0000            EXIT

4405  0024    TST86M, 0024                    /TST86 FAST SAM NOT CLEARED
4406  2324            2324
4407  7066            7066
4410  4006            4006
4411  0123            0123
4412  2440            2440
4413  2301            2301
4414  1540            1540
4415  1617            1617
4416  2440            2440
4417  0314            0314
4420  0501            0501
4421  2205            2205
4422  0400            0400
4423  7777            EXITA
```

```
4424  0000            EXIT

4425  0024  TST87M, 0024                  /TST87 CHAN 1 WON'T TRANS CNT TO BUF
4426  2324            2324
4427  7067            7067
4430  4003            4003
4431  1001            1001
4432  1640            1640
4433  6140            6140
4434  2717            2717
4435  1647            1647
4436  2440            2440
4437  2422            2422
4440  0116            0116
4441  2340            2340
4442  0316            0316
4443  2440            2440
4444  2417            2417
4445  4002            4002
4446  2506            2506
4447  4000            4000
4450  7777            EXITA
4451  0111            K0200
4452  0000            EXIT

4453  0024  TST88M, 0024                  /TST88 CHAN 2 WON'T TRANS CNT TO BUF
4454  2324            2324
4455  7070            7070
4456  4003            4003
4457  1001            1001
4460  1640            1640
4461  6240            6240
4462  2717            2717
4463  1647            1647
4464  2440            2440
4465  2422            2422
4466  0116            0116
4467  2340            2340
4470  0316            0316
4471  2440            2440
4472  2417            2417
4473  4002            4002
4474  2506            2506
4475  4000            4000
4476  7777            EXITA
4477  0111            K0200
4500  0000            EXIT

4501  0024  TST89M, 0024                  /TST89 CHAN 3 WON'T TRANS CNT TO BUF
4502  2324            2324
4503  7071            7071
4504  4003            4003
4505  1001            1001
4506  1640            1640
4507  6340            6340
```

```
4510  2717            2717
4511  1647            1647
4512  2440            2440
4513  2422            2422
4514  0116            0116
4515  2340            2340
4516  0316            0316
4517  2440            2440
4520  2417            2417
4521  4002            4002
4522  2506            2506
4523  4000            4000
4524  7777            EXITA
4525  0111            K0200
4526  0000            EXIT

4527  0024    TST90M, 0024                    /TST90 CHAN 1 WON'T TRANS CNT TO BUF
4530  2324            2324
4531  7160            7160
4532  4003            4003
4533  1001            1001
4534  1640            1640
4535  6140            6140
4536  2717            2717
4537  1647            1647
4540  2440            2440
4541  2422            2422
4542  0116            0116
4543  2340            2340
4544  0316            0316
4545  2440            2440
4546  2417            2417
4547  4002            4002
4550  2506            2506
4551  4000            4000
4552  7777            EXITA
4553  0113            K0300
4554  0000            EXIT

4555  0024    TST91M, 0024                    /TST91 CHAN 2 WON'T TRANS CNT TO BUF
4556  2324            2324
4557  7161            7161
4560  4003            4003
4561  1001            1001
4562  1640            1640
4563  6240            6240
4564  2717            2717
4565  1647            1647
4566  2440            2440
4567  2422            2422
4570  0116            0116
4571  2340            2340
4572  0316            0316
4573  2440            2440
4574  2417            2417
```

```
4575  4002            4002
4576  2506            2506
4577  4000            4000
4600  7777            EXITA
4601  0113            K0300
4602  0000            EXIT

4603  0024    TST92M, 0024                    /TST92 CHAN 3 WON'T TRANS CNT TO BUF
4604  2324            2324
4605  7162            7162
4606  4003            4003
4607  1001            1001
4610  1640            1640
4611  6340            6340
4612  2717            2717
4613  1647            1647
4614  2440            2440
4615  2422            2422
4616  0116            0116
4617  2340            2340
4620  0316            0316
4621  2440            2440
4622  2417            2417
4623  4002            4002
4624  2506            2506
4625  4000            4000
4626  7777            EXITA
4627  0113            K0300
4630  0000            EXIT

4631  0024    TST93M, 0024                    /TST93 CHAN 3 INPUT FAILED TO CLR CNT
4632  2324            2324
4633  7163            7163
4634  4003            4003
4635  1001            1001
4636  1640            1640
4637  6340            6340
4640  1116            1116
4641  2025            2025
4642  2440            2440
4643  0601            0601
4644  1114            1114
4645  0504            0504
4646  4024            4024
4647  1740            1740
4650  0314            0314
4651  2240            2240
4652  0316            0316
4653  2400            2400
4654  7777            EXITA
4655  0052            RXED
4656  0000            EXIT

4657  0024    TST94M, 0024                    /TST94 ECO EM12-00034 IS EITHER NOT WORKING OR NOT INSTALLED
4660  2324            2324
```

```
4661  7164            7164
4662  4005            4005
4663  0317            0317
4664  4005            4005
4665  1561            1561
4666  6255            6255
4667  6060            6060
4670  6063            6063
4671  6440            6440
4672  1123            1123
4673  4005            4005
4674  1124            1124
4675  1005            1005
4676  2240            2240
4677  1617            1617
4700  2440            2440
4701  2717            2717
4702  2213            2213
4703  1116            1116
4704  0740            0740
4705  1722            1722
4706  4016            4016
4707  1724            1724
4710  4011            4011
4711  1623            1623
4712  2401            2401
4713  1414            1414
4714  0504            0504
4715  0000            EXIT

4716  0024    TST95M, 0024                    /TST95 ECO EM12-00055 IS EITHER NOT WORKING OR IS NOT INSTALLED
4717  2324            2324
4720  7165            7165
4721  4005            4005
4722  0317            0317
4723  4005            4005
4724  1561            1561
4725  6255            6255
4726  6060            6060
4727  6065            6065
4730  6540            6540
4731  1123            1123
4732  4005            4005
4733  1124            1124
4734  1005            1005
4735  2240            2240
4736  1617            1617
4737  2440            2440
4740  2717            2717
4741  2213            2213
4742  1116            1116
4743  0740            0740
4744  1722            1722
4745  4016            4016
4746  1724            1724
```

```
4747  4011              4011
4750  1623              1623
4751  2401              2401
4752  1414              1414
4753  0504              0504
4754  0000              EXIT

4755  0013    TST96M,   0013                    /KW12 PASS-=(PASS)
4756  2761              2761
4757  6240              6240
4760  2001              2001
4761  2323              2323
4762  5555              5555
4763  7777              EXITA
4764  0031              PASS
4765  4444              EXITB                   /EXIT B CAUSES A RETURN TO 0176
                        $
```

```
3000  01000000  10000000  11111111  11111111  11111111  11111111  11111111  11111111
3100  11111111  11111111  11111111  11111111  11111111  11111111  11111110  00000011

3200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
3300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

3400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
3500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

3600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
3700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111


1000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

1200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

1400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

1600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
1700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111


2000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

2200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

2400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

2600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
2700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111


3000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
3100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

3200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
3300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

3400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
3500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

3600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
3700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
```

```
4000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
4100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

4200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
4300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

4400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
4500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

4600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
4700  11111111  11111111  11111111  11111111  11111111  11111111  11111100  00000000


5000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
5100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111100

5200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
5300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

5400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
5500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

5600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
5700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111


6000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
6100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

6200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
6300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

6400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
6500  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

6600  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
6700  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111


7000  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
7100  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

7200  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
7300  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111

7400  11111111  11111111  11111111  11111111  11111111  11111111  11111111  11111111
7500  11111111  11111111  11111111  11111111  11111111  11111111  11111000  00000000

7600
7700
```

ASCII	5051	K0215	5174	NERROR	0027	TST18	0466
ASCRXT	5026	K0300	0113	NERROS	5000	TST18M	5455
BELL	0021	K0377	0114	OCTYP	5133	TST19	0550
BELLS	5200	K0400	0115	OUTPAS	0030	TST19M	5476
BK43	1561	K0500	0116	PASS	0031	TST20	0566
BK47	1764	K0600	0117	PDP	0002	TST20M	5516
BK55	2362	K0700	0120	PINT	0010	TST21	0616
CLAB	6133	K0777	0121	PNTA	0032	TST21M	5540
CLAR	0157	K1000	0122	PNTB	0033	TST22	0643
CLBA	6136	K1026	0123	PNTC	0034	TST22M	5556
CLCA	6137	K1777	0124	PNTD	0035	TST23	0672
CLEAR	4157	K2000	0125	PNTE	0036	TST23M	5576
CLEN	6134	K240	0112	PNTF	0037	TST24	0721
CLLR	6132	K3000	0126	PNTG	0040	TST24M	5614
CLR	0011	K3777	0127	PNTH	0041	TST25	0753
CLSA	6135	K4000	0130	PNTI	0042	TST25M	5632
CLSK	6131	K4100	0131	PNTJ	0043	TST26	1012
CNTR	0024	K5100	0132	RANDOM	0044	TST26M	5653
CRLF	5154	K5252	0133	RANDY	5210	TST27	1043
DATUM	5115	K5555	0134	REDO	5140	TST27M	5676
DATYP	5163	K6000	0135	REGA	0045	TST28	1077
DN43	0022	K7300	4214	REGB	0046	TST28M	5722
DN55	0023	K7774	0136	REGC	0047	TST29	1131
ERROR	0025	LDAI	1020	REGT	0050	TST29M	5747
ERRORS	5020	LINC	6141	RESET	3700	TST30	1156
ESF	0004	LOCA	1425	RETURN	0051	TST30M	5774
EXIT	0000	LOCB	1457	RNA	5240	TST31	1205
EXITA	7777	LOCC	1527	RNB	5241	TST31M	6021
EXITB	4444	LOCD	2720	RNC	5242	TST32	1245
FD43	1572	LOCE	2742	RXED	0052	TST32M	6056
FD51	2201	LOCF	2763	SAM0	0100	TST33	1276
FD55	2372	LOCG	3005	SAM1	0101	TST33M	6102
FD61	2617	LOCH	3027	SEND	0053	TST34	1316
HERE	5137	LOCI	3051	SET	0054	TST34M	6126
K0000	0071	LOCJ	4307	SETN	5252	TST35	1344
K0001	0072	LSTERR	0026	SPACE	0055	TST35M	6152
K0002	0073	M0001	0137	TST10	0201	TST35N	0056
K0003	0074	M0002	0140	TST10M	5261	TST36	1373
K0004	0075	M0004	0141	TST11	0217	TST36M	6177
K0007	0076	M0010	0142	TST11M	5301	TST37	1417
K0010	0077	M0020	0143	TST12	0235	TST37M	6217
K0014	0100	M0040	0144	TST12M	5317	TST38	1434
K0017	0101	M0042	0145	TST13	0254	TST38M	6240
K0020	0102	M0100	0146	TST13M	5335	TST39	1451
K0037	0103	M0200	0147	TST14	0274	TST39M	6257
K0040	0104	M0400	0150	TST14M	5353	TST40	1467
K0060	0105	M1000	0151	TST15	0315	TST40M	6277
K0077	0106	M1400	0152	TST15M	5371	TST41	1502
K0100	0107	M2000	0153	TST16	0340	TST41M	6320
K0177	0110	M4000	0154	TST16M	5413	TST42	1521
K0200	0111	M4444	0155	TST17	0403	TST42M	6340
K0212	5175	M5400	0156	TST17M	5434	TST43	1542

TST43M	6360	TST68M	7152	TST94M	4657
TST44	1602	TST69	3037	TST95	4243
TST44M	6377	TST69M	7173	TST95M	4716
TST45	1642	TST70	3064	TST95N	4257
TST45M	6416	TST70M	7212	TST96	4276
TST46	1703	TST71	3116	TST96M	4755
TST46M	6435	TST71M	7240	TYPE	0064
TST47	1744	TST72	3150	TYPECH	5100
TST47M	6454	TST72M	7266	TYPOUT	5243
TST48	2005	TST73	3202	UP43	0065
TST48M	6473	TST73M	7314	UP51	0066
TST49	2046	TST74	3252	UP55	0067
TST49M	6512	TST74M	7333	UP61	0070
TST50	2107	TST75	3313		
TST50M	6531	TST75M	7355		
TST51	2150	TST75N	0060		
TST51M	6550	TST76	3351		
TST52	2211	TST76M	7376		
TST52M	6567	TST77	3375		
TST53	2252	TST77M	7423		
TST53M	6606	TST77N	0061		
TST54	2313	TST79	3436		
TST54M	6625	TST79M	7457		
TST55	2354	TST79N	0062		
TST55M	6644	TST81	3474		
TST56	2401	TST81M	7511		
TST56M	6661	TST82	3520		
TST57	2426	TST82M	7534		
TST57M	6676	TST83	3544		
TST58	2460	TST83M	4310		
TST58M	6713	TST84	3567		
TST59	2507	TST84M	4334		
TST59M	6727	TST85	3613		
TST60	2546	TST85M	4360		
TST60M	6745	TST86	3660		
TST60N	2554	TST86M	4405		
TST61	2573	TST87	3703		
TST61M	6766	TST87M	4425		
TST62	2624	TST88	3752		
TST62M	7010	TST88M	4453		
TST63	2655	TST89	4004		
TST63M	7032	TST89M	4501		
TST64	2710	TST90	4040		
TST64M	7054	TST90M	4527		
TST65	2730	TST90N	0063		
TST65M	7072	TST91	4102		
TST66	2753	TST91M	4555		
TST66M	7112	TST92	4135		
TST66N	0057	TST92M	4603		
TST67	2773	TST93	4170		
TST67M	7133	TST93M	4631		
TST68	3016	TST94	4210		

ERRORS DETECTED: 0

LINKS GENERATED: 0

RUN-TIME: 43 SECONDS

3K CORE USED

```
0000                    *20
0001                    /
0002                    / KW12A1
0003                    /                   18 JULY 1977
0004                    /                   18 JULY 1977
0005                    /
0006                    /
0007                    / SUPPLEMENT TO THE KW12A DIAGNOSTIC PROGRAM.
0010                    / CHECKS WHETHER, IN MODE 011, EVENT 2 ZERO"S THE
0011                    / CLOCK COUNTER AS WELL AS TRANSFERRING ITS CON-
0012                    / TS TO THE CLOCK BUFFER.
0013                    /
0014                    / ASSUMES KW12A HAS RUN SUCCESSFULLY.
0015                    /
0016                    / DISCONNECT ALL INPUT LINES, AND DESELECT
0017                    / "LINE FREQ" FROM ALL THREE SOURCES.
0020                    / START 8MODE, 0020.
0021                    /
0022                    /
0023                          PMODE
0024                          *0020
0025                    /
0026                    / RATE AND MODE:
0027                    / RATE 110 (COUNT INPUT 1 EVENTS)
0030                    / MODE 011 (ANY EVENT TRANSFERS COUNTER TO BUFFER,
0031                    / & EVENT 3 ZERO"S COUNTER)
0032                    /
0033    0020  7200            CLA
0034    0021  1117            TAD K0025
0035    0022  6134            CLEN                /ENABLE ALL 3 INPUTS
0036    0023  7200            CLA
0037    0024  1120    AGAIN,  TAD K6300
0040    0025  6132            CLLR
0041    0026  7001            IAC
0042    0027  6132            CLLR                /INPUT 3
0043    0030  6135            CLSA                /REENABLE INPUTS
0044    0031  7200            CLA
0045    0032  1121            TAD K6301
0046    0033  6132            CLLR                /AGAIN
0047    0034  6136            CLBA                /BUFFER TO AC
0050    0035  7440            SZA                 /DID IT ZERO COUNTER?
0051    0036  7402            HLT                 /IT SHOULD HAVE.
0052    0037  1123            TAD K6320
0053    0040  6132            CLLR                /INPUT 1
0054    0041  6132            CLLR                /AGAIN
0055    0042  6137            CLCA                /COUNTER TO AC
0056    0043  1124            TAD KM2
0057    0044  7440            SZA                 /WAS IT 2?
0060    0045  7402            HLT                 /IT SHOULD HAVE BEEN.
0061    0046  6133            CLAB                /CLEAR BUFFER PRESET REG.
0062    0047  6135            CLSA                /REENABLE INPUTS
0063    0050  7200            CLA
0064    0051  1121            TAD K6301
0065    0052  6132            CLLR                /INPUT 3
0066    0053  6136            CLBA
0067    0054  1124            TAD KM2
0070    0055  7440            SZA                 /DID THE COUNTER GO TO THE
0071                                              /BUFFER BEFORE IT ZEROED?
0072    0056  7402            HLT                 /NO; IT SHOULD HAVE.
0073    0057  6137            CLCA
0074    0060  7440            SZA                 /DIT IT THEN ZERO?
0075    0061  7402            HLT                 /NO; IT SHOULD HAVE
```

```
0076    0062  1123          TAD K6320
0077    0063  6132          CLLR            /INPUT 1
0100    0064  6132          CLLR            /AGAIN
0101    0065  6132          CLLR            /AND AGAIN
0102    0066  6137          CLCA
0103    0067  7450          SNA             /IS THERE SOMETHING THERE?
0104    0070  7402          HLT             /NO; THERE SHOULD BE.
0105    0071  3116          DCA BUF         /YES; KEEP IT
0106    0072  1122          TAD K6304
0107    0073  6132          CLLR            /INPUT 2
0110    0074  6136          CLBA
0111    0075  7041          CIA
0112    0076  1116          TAD BUF
0113    0077  7440          SZA             /IS THE SAME THING THERE?
0114    0100  7402          HLT             /NO
0115    0101  6135          CLSA
0116    0102  7200          CLA
0117    0103  6133          CLAB            /CLEAR THE BUFFER
0120    0104  1122          TAD K6304       /INPUT 2
0121    0105  6132          CLLR
0122    0106  6136          CLBA
0123    0107  7041          CIA
0124    0110  1116          TAD BUF
0125    0111  7440          SZA             /STILL THERE?
0126    0112  7402          HLT             /OH-OH! INPUT 2 MUST DO
0127                                        /SOMETHING TO THE COUNTER!
0130    0113  6135          CLSA
0131    0114  7200          CLA
0132    0115  5024          JMP AGAIN
0133                /
0134    0116  0000  BUF,     0
0135    0117  0025  K0025,   0025
0136    0120  6300  K6300,   6300
0137    0121  6301  K6301,   6301
0140    0122  6304  K6304,   6304
0141    0123  6320  K6320,   6320
0142    0124  7776  KM2,     -2

NO ERRORS

AGAIN  0024
BUF    0116
KM2    0124
K0025  0117
K6300  0120
K6301  0121
K6304  0122
K6320  0123
```