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MS11-L
MOS memory
user's guide

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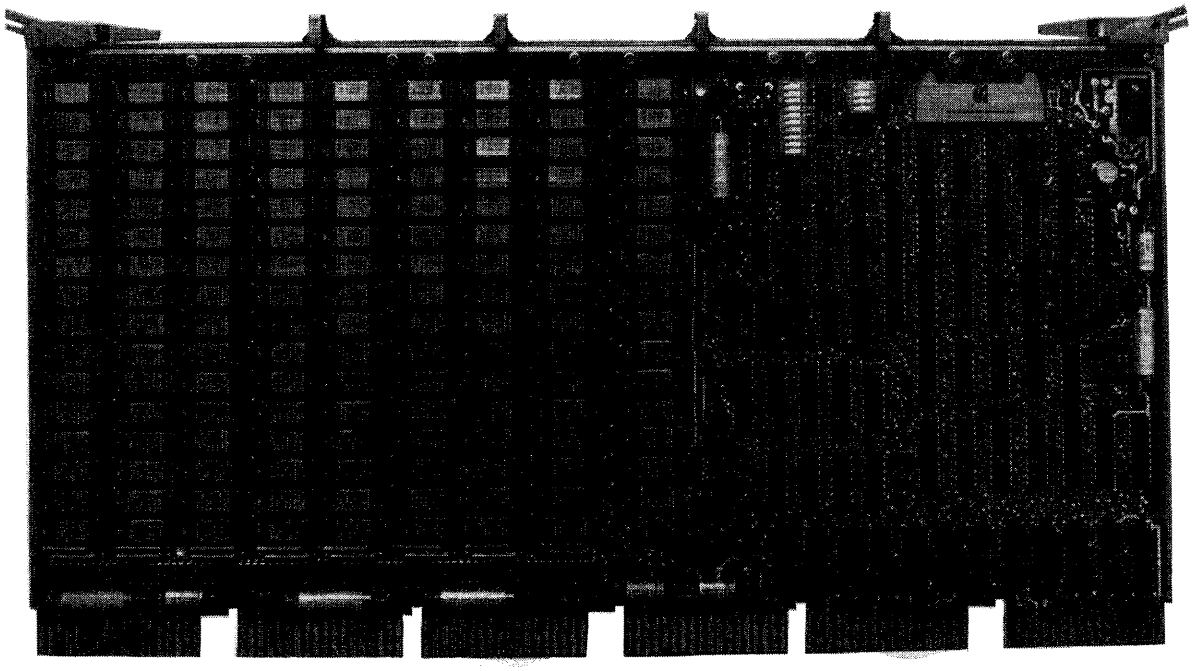

9166-1A0288

MS11-L(D) MOS Memory

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CHAPTER 1
CHARACTERISTICS AND SPECIFICATIONS

1.1 INTRODUCTION

This manual describes the MS11-L, which is a metal oxide semiconductor (MOS), random access memory (RAM), designed to be used with the PDP-11 Unibus or special buses with reserve addressing capability. The memory assumes the role of a slave device to the PDP-11 processor or to any peripheral device that is designated bus master. The MS11-L provides storage for 18-bit words (16 data bits and 2 parity bits) and also contains parity control circuitry and a control and status register (CSR). There are four versions of the MS11-L that are differentiated by the total memory capacity available on the module (Table 1-1). Note that the maximum configuration is 128K (131,072 words).

Table 1-1 MS11-L Versions

Option Designation	Module Designation	Storage Capacity
MS11-LA	M7891-AA	32K × 18-bit
MS11-LB	M7891-BA	64K × 18-bit
MS11-LC	M7891-CA	96K × 18-bit
MS11-LD	M7891-DA	128K × 18-bit

1.2 GENERAL DESCRIPTION

The MS11-L consists of a single, hex-height module (M7891) that contains the Unibus/special bus interface, timing and control logic, refresh circuitry and a MOS storage array. The module also contains circuitry to generate and check parity, and a control and status register (CSR).

The memory starting address can be set at any 4K boundary within the 128K Unibus address space or 2048K special bus address space. (Special buses compatible with the MS11-L contain 22 address lines as opposed to 18 Unibus address lines.) The MS11-L allows the top 2K, 4K or 8K of the Unibus or special bus address space to be reserved for the I/O peripheral page. Note that there is no address interleaving with the MS11-L.

The memory storage elements are 16,384 × 1-bit, MOS dynamic RAM devices. The MOS storage array contains 18 of these devices for each 16K bank of memory; e.g., a 128K memory contains 144 storage devices, a 64K memory contains 72 storage devices. Unlike core memory, the read operation for MOS storage devices is nondestructive; consequently, the write-after-read operation associated with core memory is eliminated. The MOS storage devices must be periodically refreshed so that the data remains valid.

The MS11-L memory uses +5 V and either ±15 V or ±12 V power. Since the MOS storage devices are volatile (data is not retained when power is lost), a battery backup unit is available which supports the MOS power supply regulator(s). Therefore, dc power is available to MOS memory only, for a limited time during an ac power failure. In the battery support mode, power is used only to refresh the MOS storage array so that battery backup time, and therefore, data retention time, are maximized. A green LED on the module stays on as long as +5 V power is supplied to the logic required for memory refresh.

The control and status register (CSR) in the MS11-L contains 11 bits which are used to store information in case of a parity error and control certain parity functions. The CSR has its own address in the top 2K of the Unibus, or special bus address space, and can be read or written into by any device designated as bus master, even during a memory refresh cycle.

The parity control circuitry in the MS11-L generates parity bits based on data being written into memory during a DATO or DATOB bus cycle. One parity bit is assigned to each data byte and is stored with the data in the MOS storage array. When data is retrieved from memory during a DATI or DATIP bus cycle, the parity of the data is recalculated and compared to the stored bits. If the parity bits correspond, the data is assumed to be correct; if the parity bits do not correspond, the data is assumed to be unreliable and the memory initiates the following action:

1. The parity error bit (bit 15) of the CSR is set to a logical 1.
2. A red LED on the module turns on, providing a visual indication of a parity error.
3. If bit 0 in the CSR is set, the memory asserts BUS PB L which warns the processor that a parity error has occurred.
4. Part of the address of the faulty data is recorded in the CSR (Paragraph 2.3).

1.3 SPECIFICATIONS

1.3.1 Functional Specifications

Capacity		
MS11-LA	32,768 (32K) words	18-bit words (16 data bytes with 2 parity bits)
MS11-LB	65,536 (64K) words	
MS11-LC	98,304 (96K) words	
MS11-LD	131,072 (128K) words	
Refresh Timing		
Cycle time	570 ns (typical), 610 ns (maximum)	
Repetition rate	one cycle every 14.5 μs (typical), 13.5 μs (maximum)	

NOTE

Refresh cycle time is defined as the time interval between the assertion of REF REQ L and the negation of BUSY L. These signals are internal to the memory module.

Access and Cycle Times (Table 1-2)

Table 1-2 Access and Cycle Times

Bus Mode	Access Time (ns)		Cycle Time (ns)	
	Typical	Maximum	Typical	Maximum
DATI/DATIP (Memory)	385	415	510	540
DATO/DATOB (Memory)	125	150	510	540
DATI/DATIP (CSR)	60	80	-	-
DATO/DATOB (CSR)	60	80	-	-

NOTES

1. **Access time – The time interval between memory reception of BUS MSYN L (at the input of the receiver) and the assertion of BUS SSYN L on the Unibus or special bus.**

   Cycle time – The time interval between the assertion of MEM REQ L and the negation of BUSY L. These signals are internal to the memory module.

2. **If the memory is accessed by a bus master during a refresh cycle (causing a refresh conflict), the data transfer is delayed until the refresh cycle is completed. In the worst case, memory access and cycle times are increased by the entire refresh time; 570 ns (typical), 610 ns (maximum). Access to the CSR is not affected by a refresh cycle.**

3. **If the memory is accessed by a bus master momentarily before the start of a refresh cycle, memory cycle and access times are increased by the refresh arbitration time; 60 ns (typical), 90 ns (maximum). Access to the CSR is not affected by refresh arbitration.**

1.3.2 Electrical Specifications

Voltage Requirements

+5 V ±5%, max ripple = 0.2 V p-p
+15 V +10%, -3.3% or +12 V ±5%, max ripple = 1 V p-p
-15 V ±10% or -12 V ±10%, max ripple = 1 V p-p

Current and Power Requirements

Tables 1-3 and 1-4

Table 1-3 Current and Power Requirements

Memory Option	+5 V		+5 VBBU		-12 V/-15 V		+12 V/+15 V Standby		+12 V/+15 V Active	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
MS11-LA (32K X 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	9 mA (0.108/0.135 W)	11 mA (0.145/0.182 W)	85 mA (1.02/1.28 W)	105 mA (1.32/1.73 W)	485 mA (5.82/7.28 W)	540 mA (6.8/8.91 W)
MS11-LB (64K X 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	12 mA (0.144/0.18 W)	14 mA (0.185/0.231 W)	140 mA (1.68/2.1 W)	160 mA (2.02/2.64 W)	535 mA (6.42/8.03 W)	595 mA (7.5/9.82 W)
MS11-LC (96K X 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	15 mA (0.180/0.225 W)	17 mA (0.224/0.281 W)	190 mA (2.28/2.85 W)	215 mA (2.71/3.55 W)	590 mA (7.08/8.85 W)	650 mA (8.19/10.73 W)
MS11-LD (128K X 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	18 mA (0.216/0.27 W)	20 mA (0.264/0.33 W)	240 mA (2.88/3.6 W)	265 mA (3.34/4.37 W)	640 mA (7.68/9.6 W)	700 mA (8.82/11.55 W)

NOTES

1. **The module has inputs for two sources of +5 V power, designated +5 VBBU (optionally battery supported) and +5 V (not battery supported). The voltage tolerances required for the +5 V and +5 VBBU inputs are the same. The total module consumption of +5 V power during normal operation is equal to the sum of the +5 V and +5 VBBU ratings (Paragraph 2.2.1.4).**

2. **The standby and active ratings for +5 V, +5 VBBU and -12 V/-15 V are the same.**

3. **The maximum power ratings have been calculated using the worst case voltage tolerances.**

Table 1-4 Total Module Power Requirements

Memory Option	Standby		Active		Battery Backup Mode	
	Typ	Max	Typ	Max	Typ	Max
MS11-LA (32K X 18)	13.6/13.9 W	17.8/18.2 W	18.4/19.9 W	23.3/25.4 W	6.1/6.4 W	8.3/8.7 W
MS11-LB (64K X 18)	14.3/14.8 W	18.5/19.2 W	19.1/20.7 W	24/26.4 W	6.8/7.3 W	9/9.7 W
MS11-LC (96K X 18)	15/15.6 W	19.2/20.1 W	19.8/21.6 W	24.7/27.3 W	7.5/8.1 W	9.7/10.6 W
MS11-LD (128K X 18)	15.6/16.4 W	19.9/21 W	20.4/22.4 W	25.4/28.2 W	8.1/8.9 W	10.4/11.5 W

NOTES

1. XX/YY = rating when ±12 V/±15 V power is used.
2. The maximum power ratings have been calculated using the worst case voltage tolerances.

1.3.3 Physical and Environmental Specifications

Module Designation

MS11-LA	M7891-AA	All versions are hex-height multilayer, 21.6 × 38.1 cm (8.5 × 15 in)
MS11-LB	M7891-BA	
MS11-LC	M7891-CA	
MS11-LD	M7891-DA	

Operating Temperature	5° to 50° C (41° to 122° F)
Humidity	10 to 95 percent (non-condensing)

1.4 RELATED DOCUMENTS

Additional reference information can be found in the documents listed below.

Title	Document No.	Availability
PDP-11 Peripherals Handbook	EB-05961	Hardcopy only
PDP-11/04/34/45/55/60 Processor Handbook	EB-09340	Hardcopy only

These documents can be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532

Attn: Communication Services (NR2/M15)
Customer Services Section

For information concerning Microfiche Libraries, contact:

Digital Equipment Corporation
Micropublishing Group

PK3-2/T12
Maynard, MA 01754

CHAPTER 2
INSTALLATION AND PROGRAMMING

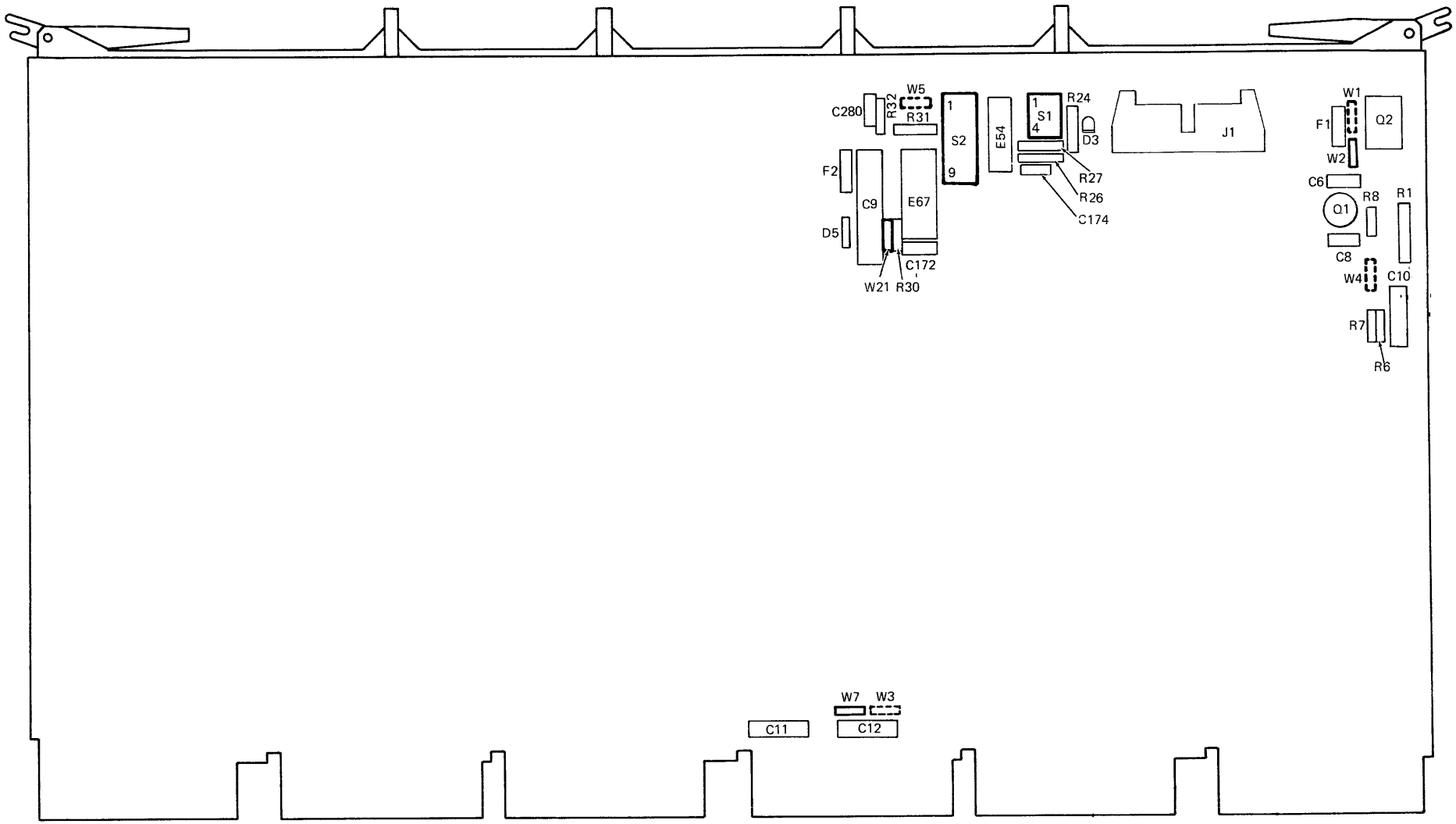
2.1 GENERAL

This chapter presents the information necessary for installation and programming of the MS11-L and applies to all versions of the memory. Installation procedures include: switch/jumper settings, backplane placement, power voltage checks and MAINDEC testing. Programming information includes a discussion of bit assignments in the control and status register (CSR). Power voltage regulation on the module is also discussed in this chapter.

2.2 INSTALLATION

2.2.1 Switch and Jumper Configurations

The MS11-L contains fifteen jumpers and two switchpacks; one switchpack contains four switches (S1-1 to S1-4) and the other contains nine switches (S2-1 to S2-9). The location of the jumpers and switches is shown in Figure 2-1. In normal operation, jumpers W10–W16 and W20 should be IN. The other jumpers are used to specify Unibus or special bus operation, I/O peripheral page size, and the dc power inputs available to the module. The memory starting address and CSR address are specified by the switches.



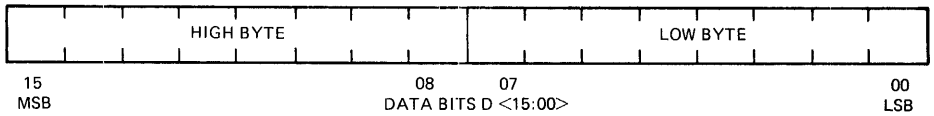
NOTES:

1. JUMPERS W10 – W16 AND W20 ARE NOT SHOWN SINCE THEY SHOULD NOT BE TAMPERED WITH IN THE FIELD.
2. THE JUMPERS SHOWN ARE ZERO OHM RESISTORS:
   ▭ = JUMPER IN
   ⬚ = JUMPER OUT
   THE JUMPER CONFIGURATION IN THE FIGURE IS THE MOST COMMON.

Figure 2-1 Switch and Jumper Locations

2.2.1.1 Memory Addressing

PDP-11 Memory Conventions – The MS11-L can be used with the PDP-11 Unibus or special buses with reserve addressing capability. Memory in these computer systems is organized into 16-bit data words, each containing two 8-bit bytes. These bytes are identified as low or high, as shown below.



Each byte is addressable and has its own address location; low bytes are even-numbered and high bytes are odd-numbered. Words are addressed by even numbered locations only, and the high (odd) byte for each word is automatically included.

Via the Unibus, 131,072 (128K) words or 262,144 (256K) bytes can be addressed; 2,097,152 (2048K) words or 4,194,034 (4096K) bytes can be addressed via a special bus. Each byte location in Unibus memory is specified by a 6-digit octal number, but with a special bus, 8-digit octal numbers are used. The address range is 000000-777777 on the Unibus and 00000000-17777777 on a special bus (Figure 2-2).

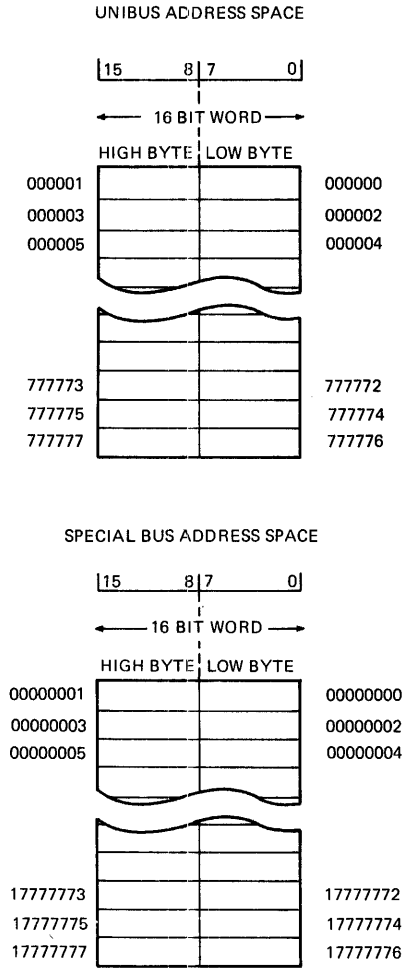
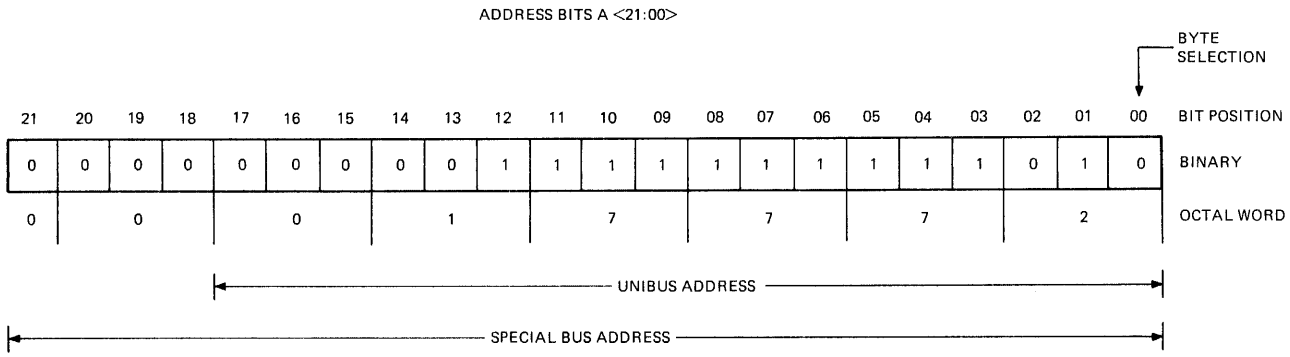


Figure 2-2 Bus Accessible Data Locations

The memory address decoding logic responds to the binary equivalent of the octal address. The binary equivalent of 00017772 is shown below. The MS11-L decodes an 18-bit address (A17-A00) on the Unibus or a 22-bit address (A21-A00) on a special bus.



The address space on a bus occupied by a memory module is determined by the memory starting address and address range. A unique starting address is selected by switches on the MS11-L which correspond to address bits A17-A13 on the Unibus or A21-A13 on a special bus. Table 2-1 lists the octal address ranges of the MS11-L versions and the associated address bits which determine the word location within the module. Address bit A00 is used to select a data byte during a DATOB bus cycle.

Table 2-1 MS11-L Address Ranges

Memory Designation	Storage Capacity	Octal Address Range	Associated Address Bits
MS11-LA	32,768 words (65,536 bytes)	00000000-00177777	A15-A00
MS11-LB	65,536 words (131,072 bytes)	00000000-00377777	A16-A00
MS11-LC	98,304 words (196,608 bytes)	00000000-00577777	A17-A00
MS11-LD	131,072 words (262,144 bytes)	00000000-00777777	A17-A00

Memory Starting Address Selection – The lowest bus address which the MS11-L responds to is the memory starting address. The starting address must be assigned to a 4K boundary within the 128K Unibus address space or 2048K special bus address space. The starting address is assigned by manually setting nine switches, S2-1 through S2-9, to the appropriate positions for the desired location (Tables 2-2 and 2-3).

Switches S2-1 to S2-9 correspond to address bits A21-A13 respectively on a special bus; a switch in the OFF position corresponds to a logical 1. The positions of S2-1 to S2-4 specify the starting address to a 128K range; S2-5 to S2-9 specify the starting address to a 4K boundary within a 128K range.

NOTE
Switches S2-1 to S2-4 should be set to the ON position if the MS11-L is used with the PDP-11 Unibus.

Unibus or special bus operation of the MS11-L is selected by jumper W4:

W4 OUT	Specifies Unibus operation
W4 IN	Specifies special bus operation

Table 2-2 Starting Address Configurations (Part 1)

Partial Starting Address		Switch Positions			
Decimal	Octal	S2-1 (A21)	S2-2 (A20)	S2-3 (A19)	S2-4 (A18)
0K	00RR0000	ON	ON	ON	ON
128K	01RR0000	ON	ON	ON	OFF
256K	02RR0000	ON	ON	OFF	ON
384K	03RR0000	ON	ON	OFF	OFF
512K	04RR0000	ON	OFF	ON	ON
640K	05RR0000	ON	OFF	ON	OFF
768K	06RR0000	ON	OFF	OFF	ON
896K	07RR0000	ON	OFF	OFF	OFF
1024K	10RR0000	OFF	ON	ON	ON
1152K	11RR0000	OFF	ON	ON	OFF
1280K	12RR0000	OFF	ON	OFF	ON
1408K	13RR0000	OFF	ON	OFF	OFF
1536K	14RR0000	OFF	OFF	ON	ON
1664K	15RR0000	OFF	OFF	ON	OFF
1792K	16RR0000	OFF	OFF	OFF	ON
1920K	17RR0000	OFF	OFF	OFF	OFF

NOTES

1. **RR = octal digits determined by switches S2-5 to S2-9**

2. **The decimal addresses listed are equivalent to the associated octal addresses if RR = 00**

Table 2-3 Starting Address Configurations (Part 2)

Partial Starting Address		Switch Positions				
Decimal	Octal	S2-5 (A17)	S2-6 (A16)	S2-7 (A15)	S2-8 (A14)	S2-9 (A13)
0K	SS000000	ON	ON	ON	ON	ON
4K	SS020000	ON	ON	ON	ON	OFF
8K	SS040000	ON	ON	ON	OFF	ON
12K	SS060000	ON	ON	ON	OFF	OFF
16K	SS100000	ON	ON	OFF	ON	ON
20K	SS120000	ON	ON	OFF	ON	OFF
24K	SS140000	ON	ON	OFF	OFF	ON
28K	SS160000	ON	ON	OFF	OFF	OFF
32K	SS200000	ON	OFF	ON	ON	ON
36K	SS220000	ON	OFF	ON	ON	OFF
40K	SS240000	ON	OFF	ON	OFF	ON
44K	SS260000	ON	OFF	ON	OFF	OFF
48K	SS300000	ON	OFF	OFF	ON	ON
52K	SS320000	ON	OFF	OFF	ON	OFF
56K	SS340000	ON	OFF	OFF	OFF	ON
60K	SS360000	ON	OFF	OFF	OFF	OFF
64K	SS400000	OFF	ON	ON	ON	ON
68K	SS420000	OFF	ON	ON	ON	OFF
72K	SS440000	OFF	ON	ON	OFF	ON
76K	SS460000	OFF	ON	ON	OFF	OFF
80K	SS500000	OFF	ON	OFF	ON	ON
84K	SS520000	OFF	ON	OFF	ON	OFF
88K	SS540000	OFF	ON	OFF	OFF	ON
92K	SS560000	OFF	ON	OFF	OFF	OFF
96K	SS600000	OFF	OFF	ON	ON	ON
100K	SS620000	OFF	OFF	ON	ON	OFF
104K	SS640000	OFF	OFF	ON	OFF	ON
108K	SS660000	OFF	OFF	ON	OFF	OFF
112K	SS700000	OFF	OFF	OFF	ON	ON
116K	SS720000	OFF	OFF	OFF	ON	OFF
120K	SS740000	OFF	OFF	OFF	OFF	ON
124K	SS760000	OFF	OFF	OFF	OFF	OFF

NOTES

1. **SS = octal digits determined by switches S2-1 to S2-4**

2. **The decimal addresses listed are equivalent to the associated octal addresses if SS = 00**

2.2.1.2 I/O Peripheral Page Size Selection – The I/O peripheral page is the address space reserved for CPU and peripheral registers. The MS11-L allows the top 2K, 4K or 8K of the Unibus or special bus address space to be reserved for the I/O peripheral page. The peripheral page size is specified by jumpers W5 and W21 as shown in Table 2-4.

Table 2-4 Peripheral Page Size Selection

Peripheral Page Size	Unibus Location	Special Bus Location	Jumpers	
			W5	W21
2K	126K–128K	2046K–2048K	IN	IN
4K	124K–128K	2044K–2048K	OUT	IN
8K	120K–128K	2040K–2048K	OUT	OUT

NOTES

1. **The remaining jumper configuration, W5 IN and W21 OUT, should never be used since it results in a peripheral page which is not continuous.**

2. **Memory diagnostics are not compatible with a 2K or 8K peripheral page (Paragraph 2.2.4).**

2.2.1.3 CSR Address Selection – The control and status register (CSR) can be read or written into via the Unibus or special bus, even during a memory refresh cycle. Address decoding logic in the MS11-L specifies the CSR address in the range of 772100–772136 for Unibus operation or 17772100–17772136 for special bus operation. Four switches, S1-1 to S1-4, are used to select the exact CSR address (Table 2-5). Switches S1-1 through S1-4 correspond to address bits A04–A01 respectively; a switch in the OFF position corresponds to a logical 1. The CSR is always accessed as an entire data word since bit A00 is not decoded by the CSR address logic. The Unibus or special bus address of the CSR is in the top 2K of the available address space.

NOTE

The CSR address has no relevance to the memory starting address or storage capacity of the MS11-L.

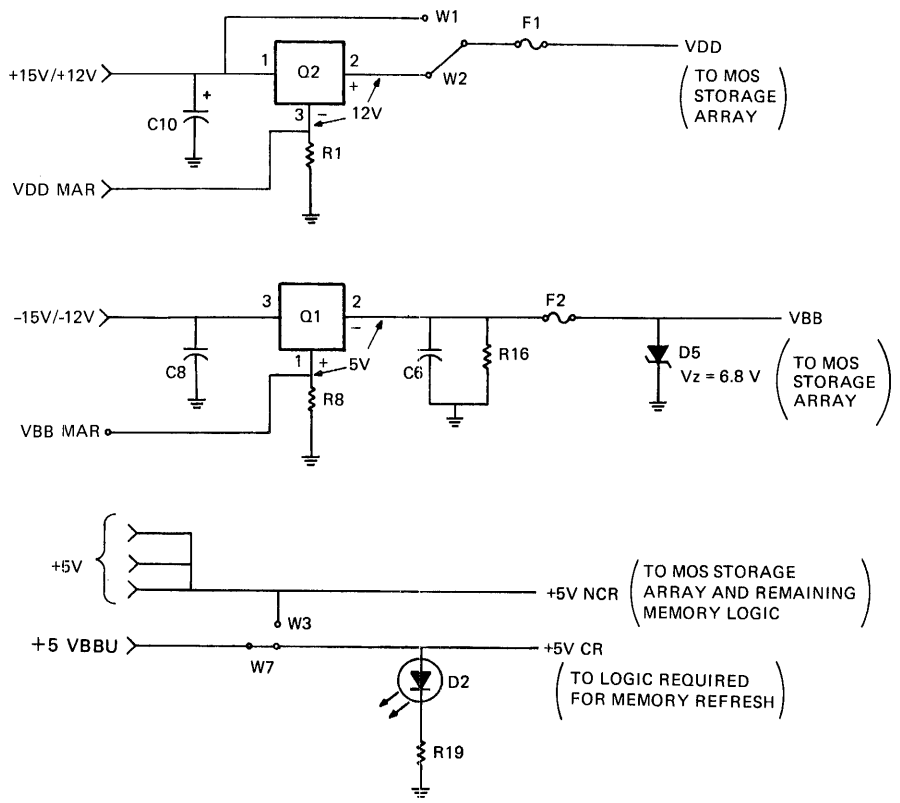
Table 2-5 CSR Address Selection

Unibus Address	Special Bus Address	Switch Positions			
		S1-1 (A04)	S1-2 (A03)	S1-3 (A02)	S1-4 (A01)
772100	17772100	ON	ON	ON	ON
772102	17772102	ON	ON	ON	OFF
772104	17772104	ON	ON	OFF	ON
772106	17772106	ON	ON	OFF	OFF
772110	17772110	ON	OFF	ON	ON
772112	17772112	ON	OFF	ON	OFF
772114	17772114	ON	OFF	OFF	ON
722116	17772116	ON	OFF	OFF	OFF
772120	17772120	OFF	ON	ON	ON
772122	17772122	OFF	ON	ON	OFF
772124	17772124	OFF	ON	OFF	ON
772126	17772126	OFF	ON	OFF	OFF
772130	17772130	OFF	OFF	ON	ON
772132	17772132	OFF	OFF	ON	OFF
772134	17772134	OFF	OFF	OFF	ON
772136	17772136	OFF	OFF	OFF	OFF

2.2.1.4 Power Voltages – The MS11-L uses +5 V and either ±15 V or ±12 V power. Jumpers W1 and W2 are used as listed below to specify ±15 V or ±12 V operation.

Power Voltage	Jumpers W1	W2
±15 V	OUT	IN
±12 V	IN	OUT

The circuit shown in Figure 2-3 yields +12 V and -5 V which are designated VDD and VBB respectively and are routed to the MOS storage array. The major components of the circuit are Q1 and Q2 which are three-terminal voltage regulators. Regulator Q2 produces +12 V from a +15 V module input and Q1 produces -5 V from a -15 V or -12 V module input. In normal operation, voltage drops across R1 and R8 are negligible. Fuses F1 and F2 provide current overload protection and zener diode D5 provides overvoltage protection. If an overvoltage condition occurs, D5 conducts so that VBB is clamped to -6.8 V. Note that if the module operates with ±12 V inputs, the output of Q2 is not used but current flows from the module input via W1. The ±15 V/±12 V module inputs are battery supported during an ac power failure if a battery backup unit is present.



NOTES:

1. AS SHOWN, W1 AND W2 INDICATE ±15V OPERATION AND W3 AND W7 INDICATE MODULE USAGE OF +5V AND +5VBBU. JUMPERS W3 AND W7 SHARE A HOLE ON THE MODULE SO THAT BOTH JUMPERS CAN NOT BE IN AT THE SAME TIME.
2. INPUTS VDD MAR AND VBB MAR ARE USED AT THE FACTORY TO MARGIN THE MEMORY (IN ±15V OPERATION ONLY).

Figure 2-3 Power Voltages

The module has inputs for two sources of +5 V power, designated +5 VBBU and +5 V. Jumpers W3 and W7 are associated with the +5 VBBU and +5V inputs and are configured as follows.

Power Voltages	Jumpers W3	Jumpers W7	Comments
+5 V and +5 VBBU	OUT	IN	Normal configuration.
+5 V only	IN	OUT	Used if power is available at the +5 V input only.

With W3 OUT and W7 IN, power is routed from the +5 VBBU input to the logic required for memory refresh; power from the +5 V input is routed to the MOS storage array and the remaining memory logic. The +5 VBBU input is battery supported during an ac power failure if a battery backup unit is present. In the battery support mode, power is used only to refresh the MOS storage array so that battery backup time and therefore data retention time are maximized. (The MOS storage devices do not require +5 V power during a refresh cycle.) Note that in most systems, power is supplied to the +5 V and +5 VBBU inputs even if the battery backup unit is not used. With W3 IN and W7 OUT, the power distribution lines on the module for +5 V and +5 VBBU are jumpered together and the +5 VBBU module input is disconnected.

A green LED (D2) stays on as long as the logic required for refresh receives power from either the +5 V or +5 VBBU input. The MS11-L should not be extracted from the backplane when the green LED is ON, even in battery support mode.

2.2.2 Backplane Placement (Unibus Operation Only)

The MS11-L should be inserted into any slot in a backplane which contains modified Unibus connectors in sections A and B. For example:

DD11-PK	Slots 3–8
DD11-DK	Slots 2–8
DD11-CK	Slots 2 and 3

The MS11-L is compatible with all modified Unibus parity or non-parity memories. The MS11-L does not require an M7850 Parity Controller; however, an M7850 is required for other parity memories that may be in the same backplane. The presence of the M7850 does not affect the MS11-L. The backplane connections used by the MS11-L are listed in Table 2-6.

Table 2-6 MS11-L Pin Out

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
A	INIT L	+5 V	–	+5 V	NPG IN H]	+5 V	–	–	–	–	–	–
B	–	–	–	–	NPG OUT H]	–	–	–	–	–	–	–
C	D00 L	GND	–	GND	–	GND	–	GND	–	GND	–	GND
D	D02 L	D01 L	+5 V Battery	–	–	–	–	–	–	–	–	–
E	D04 L	D03 L	A19 L	A18 L	–	–	–	–	–	–	–	–
F	D06 L	D05 L	–	DC LO L	VDD MAR	–	–	–	–	–	–	–
H	D08 L	D07 L	A01 L	A00 L	–	–	–	–	–	–	–	–
J	D10 L	D09 L	A03 L	A02 L	–	–	–	–	–	–	–	–
K	D12 L	D11 L	A05 L	A04 L	–	–	–	BUS G7 SO H]	–	–	–	–
L	D14 L	D13 L	A07 L	A06 L	–	–	–	BUS G7 OUT H]	–	–	–	–
M	–	D15 L	A09 L	A08 L	–	–	–	BUS G6 SO H]	–	–	–	–
N	A21 L	PB L	A11 L	A10 L	–	–	–	BUS G6 OUT H]	–	–	–	–
P	A20 L	–	A13 L	A12 L	–	–	–	BUS G5 SO H]	–	–	–	–
R	+15 V/+12 V Battery	–	A15 L	A14 L	–	–	–	BUS G5 OUT H]	–	–	–	–
S	-15 V/-12 V Battery	–	A17 L	A16 L	–	–	–	BUS G4 SO H]	–	–	–	–
T	GND	–	GND	C1 L	GND	–	GND	BUS G4 OUT H]	GND	–	GND	–
U	–	–	SSYN L	C0 L	–	–	–	–	–	–	–	–
V	–	–	MSYN L	–	–	–	–	–	–	–	–	–

NOTES

1. Pins AN1, AP1, BE1 and BE2 are used for address lines A21 L - A18 L in special bus operation. In Unibus operation, the signals on these pins are ignored by the MS11-L (receivers disabled). In Unibus operation, AN1, AP1, BE1 and BE2 contain the internal bus used by the M7850 Parity Controller.
2. Pins marked by] are tied together on the module to provide grant continuity.

2.2.3 Power Voltage Check

Once primary power has been turned on, the dc power voltages listed below should be checked at the backplane.

Voltage and Tolerance	Backplane Pin(s)
+5 V ±5%, max ripple = 0.2 V p-p	AA2, BA2, CA2
+5 VBBU ±5%, max ripple = 0.2 V p-p (only if jumper W7 is IN and W3 is OUT on the module)	BD1
+15 V +10%, -3.3% or +12 V ±5%, max ripple = 1 V p-p	AR1
-15 V ±10% or -12 V ±10%, max ripple = 1 V p-p	AS1

2.2.4 MAINDEC Testing

The following diagnostic program should be used with the MS11-L: 0–128K Memory and Memory Parity Exerciser (MAINDEC-11-CZQMC). To verify proper operation of the memory, run two passes of the diagnostic. No errors are permitted. Also, verify that the program printout agrees with the total memory in the system.

NOTE

The MAINDEC-11-CZQMC diagnostic is compatible with a 4K I/O peripheral page only (Paragraph 2.2.1.2)

2.3 CSR BIT ASSIGNMENTS

The control and status register (CSR) in the MS11-L allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the Unibus or a special bus, even during a memory refresh cycle. Some CSR bits are cleared by the assertion of BUS INIT L. This signal is asserted for a short time by the processor after system power has come up or in response to a reset instruction. The CSR bit assignments are illustrated in Figure 2-4 and are described as follows:

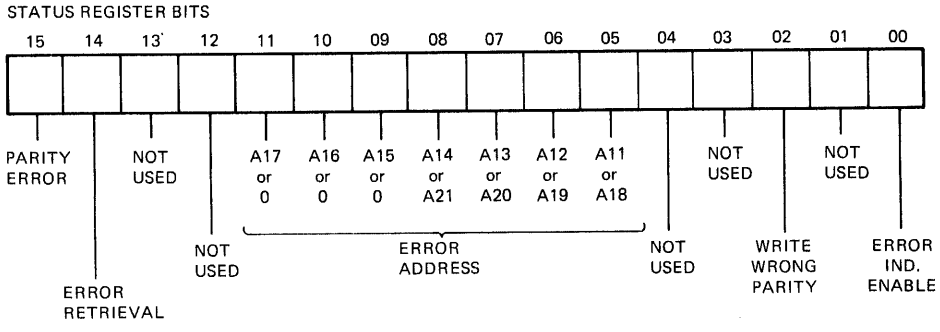


Figure 2-4 CSR Bit Allocation

Bits 1, 3, 4, 12 and 13 — These bits are not used and are always read as logical 0's. Writing into these bits has no effect on the CSR.

Bit 0 — Error Indication Enable – This bit, when set (logical 1), allows the MS11-L to assert BUS PB L when data is retrieved from memory if a parity error has been detected. This bit can be read or loaded by the program (read/write bit) and is cleared by BUS INIT L.

Bit 2 — Write Wrong Parity – This bit, when set, causes the MS11-L to generate the wrong (incorrect) parity when data is written into memory during a DATO or DATOB bus cycle. A parity error should then be detected when this data is read during a DATI or DATIP bus cycle. The bit is usually set for diagnostic purposes and should be cleared (logical 0) for normal operation (correct parity generated). Bit 2 is a read/write bit and is cleared by BUS INIT L.

Bits 05–11 — Error Address – Once a parity error has occurred, these bits contain a partial address of the faulty data which caused the parity error. In Unibus operation, address bits A17–A11 are in CSR bits 11–05 respectively, specifying the faulty data location to a 1K segment of memory. In special bus operation, the address bits placed in bits 05–11 are determined by bit 14. Bits 05–11 are read/write bits and are not cleared by BUS INIT L.

Bit 14 — Special Bus Error Retrieval – This bit, when set, causes the MS11-L to place A21–A18 of the faulty data location into CSR bits 08–05; logical 0's are placed in bits 11–09. Address bits A17–A11 are placed in bits 11–05 when bit 14 is cleared. In special bus operation, bit 14 is a read/write bit and is cleared by BUS INIT L. In Unibus operation, bit 14 is a read-only bit and is always a logical 0 (clear).

NOTE

In normal special bus operation, bit 14 should be a logical 0. If a parity error has occurred, the partial address (A21–A11) of the faulty data can be retrieved using the following sequence.

1. **Read the CSR with a DATI bus cycle to obtain A17–A11. Bit 14 should be read as a logical 0.**
2. **Write a logical 1 in bit 14 of the CSR with a DATO bus cycle.**
3. **Read the CSR with a DATI bus cycle to obtain A21–A18. Bit 14 should be read as a logical 1.**

Bit 15 — Parity Error Bit – This bit, when set, indicates that a parity error has occurred and also turns on a red LED on the module, providing a visual indication of a parity error. Bit 15 is a flag, but it does not cause a parity error trap in the processor. This bit is a read/write bit and is cleared by BUS INIT L.

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EK-MS11L-UG-001

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