# KK11-A
## cache memory
## user's guide

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| DECUS | EDUSYSTEM | RSTS |
| UNIBUS | VAX | RSX |
| | VMS | IAS |

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This manual describes the KK11-A Cache Memory option to the KD11-EA central processing unit of the PDP-11/34A system. The user must be familiar with the KD11-EA to completely understand the contents of this manual.

The following documents are useful references:

KD11-EA Central Processor Maintenance Manual (EK-KD1EA-MM-001)
KD11-EA Print Set (MP00043)
KK11-A Print Set (MP00574)
BA11-K Print Set
KY11-LB Programmer's Console/Interface Module Operation and Maintenance Manual (EK-KY1LB-MM-001)

# CHAPTER 1
# INTRODUCTION

## 1.1 OVERVIEW
The KK11-A is a cache memory option to the PDP-11/34A's KD11-EA processor. The cache is a small, high-speed memory that maintains a copy of previously selected portions of main memory; it is designed to decrease central processing unit (CPU) to memory read access time.

## 1.2 PHYSICAL DESCRIPTION
The KK11-A is implemented on a hex multilayer module (M8268) that contains a 1024-word, high-speed random access memory (RAM) organized as a direct mapped cache with write-through compatible with the current version of the PDP-11/34A. The M8268 module interfaces to the KD11-EA processor (M8265 module) via a 40-pin over-the-top connector (H8821 or H8822). The only power required is 5 Vdc at 4 A maximum (Figure 2-2).

## 1.3 SYSTEM ARCHITECTURE
Cache operates as an associative memory in parallel with the Unibus main memory but with its own high-speed data path (AMUX lines that are also used by the FP11-A – a floating-point option). Cache reads by the CPU result in data being transmitted over the AMUX lines. Read misses (desired data is not present in cache) and write hits (bus address and cache location match) which result in cache updates are accomplished by the cache capturing the data from the Unibus as the CPU/main memory transaction occurs. Direct memory access (DMA) transfers to memory are also monitored by the cache (Figure 1-1).

## 1.4 CACHE MEMORY ORGANIZATION
Cache memory consists of twenty-eight 1024 X 1 RAM chips arranged as shown in Figure 1-2. Specific implementation of the cache memory organization for the PDP-11/34A is as follows.

| Cache Characteristics | PDP-11/34A Implementation |
|---|---|
| Address mechanism | Direct mapping – allows each word from main memory only one possible location in cache. Requires only one address comparison (Figure 1-3). |
| Block size | Block size of one – every time a fetch to the backing store (main memory) occurs, only one word is allocated to cache in the event of a miss. |
| Set size | Set size of one – there is one unique location in cache for any given word from backing store. If a miss occurs, only one cache location is available for data to be written into. |
| Write-through | Data from a write operation is written into cache and simultaneously copied into main memory. Maintains main memory (backing store) with a valid copy of all data. |

1-1
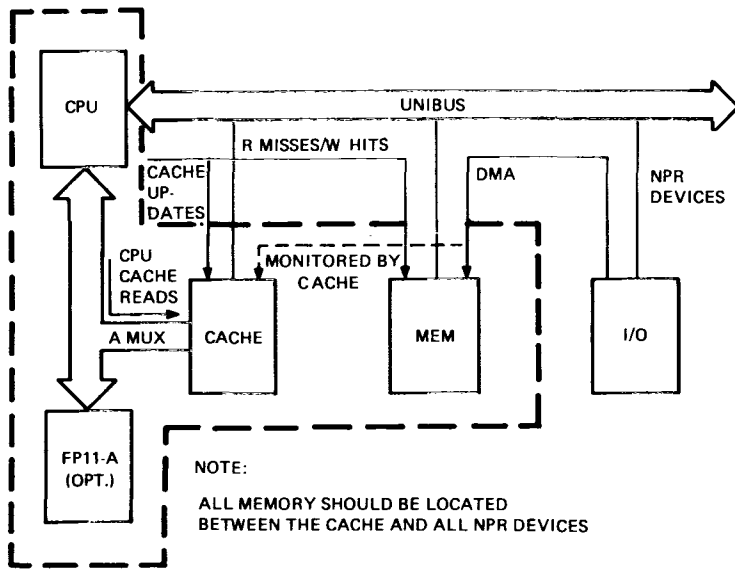
Figure 1-1   General System Architecture
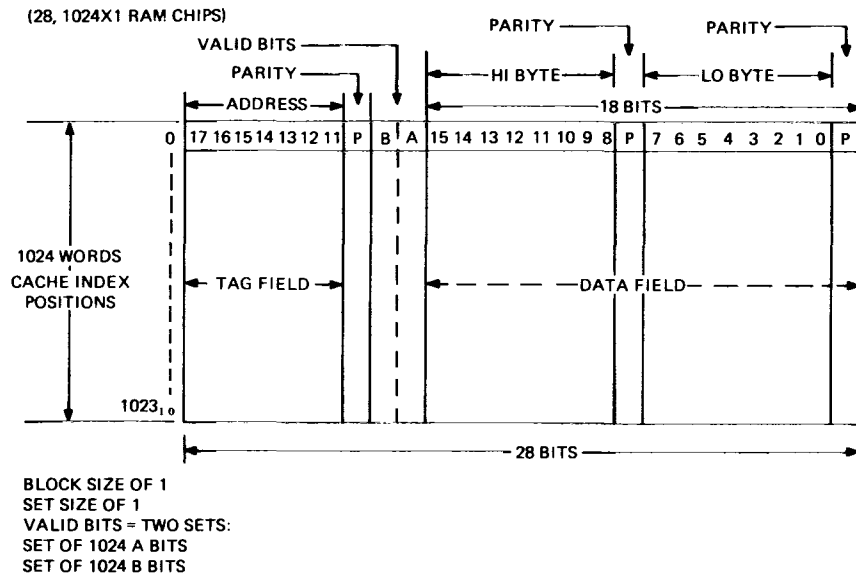


Figure 1-2   Cache Memory Format
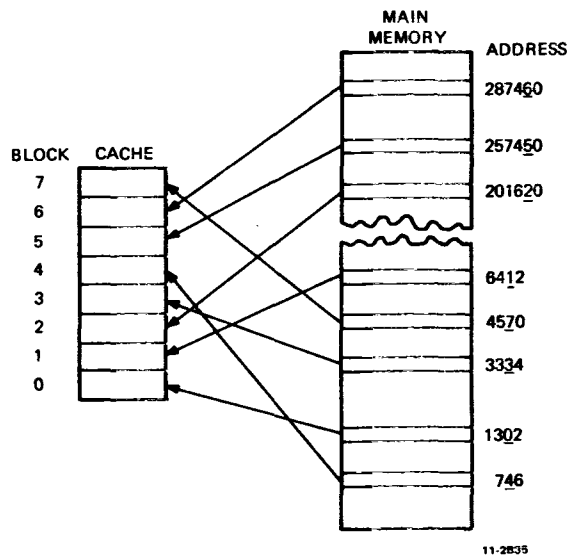
Figure 1-3 Direct Mapping Cache Memory System

The 1024 cache index positions contain 28 bits each. The tag field contains seven address bits. Each position contains a tag parity bit and two valid bits. One valid bit is currently active, allowing the other bit to be cleared concurrently. The use of two sets of valid bits allows the cache to be flushed (cleared) by switching to the second previously cleared bit set and then clearing the first set of valid bits. This method allows the use of one set of valid bits while the other set is being cleared, useful in multi-processing applications. The data field of the index position consists of two 8-bit bytes of data, each with byte parity.

### 1.4.1 Addressing Cache

When addressing cache, the PDP-11/34A uses an 18-bit address formatted as shown below.
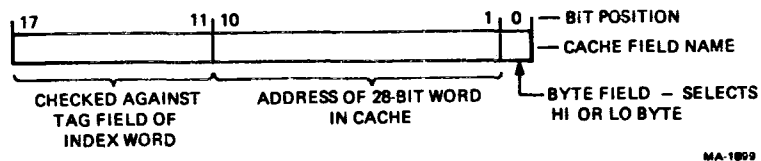


The lower part of the address (10:1) is applied against the 1K cache matrix and the high-order bits (17:11) are checked against the tag field of the index word obtained (data field in cache). If the tag field in the address matches the tag field stored with the data in cache, a hit is designated. If the fields do not match, it is designated as a miss.

The processor always looks for data in the fast cache memory first.

- If a CPU hit occurs during a read non-bypass mode (Table 1-1) data is read from cache; in bypass mode, cache is invalidated.

- If a CPU hit occurs during a write non-bypass mode, data is written into cache; in bypass mode, cache is invalidated.

- If a CPU miss occurs during a read non-bypass mode, data and tag are written into cache; in bypass mode, cache is not affected.

- If a CPU miss occurs during a CPU write non-bypass or bypass mode, cache is not affected.

Table 1-1  Cache Responses to Hit/Miss Operations

| Mode | DMA Miss* | DMA Hit* | CPU Hit | CPU Miss |
|---|---|---|---|---|
| Read<br>Bypass | Not<br>Affected | Not<br>Affected | Cache<br>Read | Write Data<br>Write Tag<br>Write Valid |
| Read<br>Bypass | Not<br>Affected | Invalidate<br>(UCB)† | Invalidate | Not<br>Affected |
| Write<br>Bypass | Not<br>Affected | Invalidate<br>(UCB)† | Invalidate | Not<br>Affected |
| Write<br>Bypass | Not<br>Affected | Invalidate | Write Data<br>Write Valid | Not<br>Affected |

*DMA hit/miss operations are discussed in Paragraph 1.4.3.
†UCB = Unconditional bypass

### 1.4.2  Multiprocessing
Additional functionality is required to perform multiprocessing.

- Unconditional Cache Bypass
  In bypass mode, all memory references are forced to be misses and to invalidate (clear valid bit) on cache hits.

- Conditional Cache Bypass*
  A virtual page can be defined such that all memory references to that page by the CPU result in being bypassed.

- LOCK (ASRB) Instruction*
  Guaranteed ownership of the cache for the duration of the destination operand cycle; must operate in bypass mode.

*Not implemented in the KD11-EA Processor.

1-4

### 1.4.3 NPR Memory References

* If a DMA hit occurs during a read non-bypass mode, the cache is not affected; in bypass mode, cache is invalidated (unconditional cache bypass) Table 1-1.

* If a DMA hit occurs during a write non-bypass mode or bypass mode, cache is invalidated.

* If a DMA miss occurs during a read or write bypass and non-bypass modes, cache is not affected.

### 1.4.4 Unibus Registers

The following hardware registers are implemented in the cache.

* Cache Memory Error Register (CME)
  Address 777 744
  Parity error detection of cache memory, high byte, low byte, and tag.

* Cache Control Register (CCR)
  Address 777 746
  The state of specific CCR bits control (1) valid, UCB, and flush cache, (2) the response of the cache to parity errors, and (3) the occurrence of CPU forced misses.

* Cache Maintenance Register (CMR)
  Address 777 750
  Contains one read/write bit used for memory system maintenance.

* Cache Hit Register (CHR)
  Address 777 752
  Contains the seven bits of the tag store memory of the last valid access and indicates the number of cache hits on the last six CPU accesses to non-I/O page memory.

### 1.4.5 Performance

The cache system is intended to simulate a system having a large amount of moderately fast memory. Therefore, the system contains a small amount of very fast memory (cache) and a large amount of slow memory (backing store). The cache system works because it can successfully predict which words a program will require most of the time. Program behavior is such that cache hits should occur 85 to 90 percent of the time, substantially decreasing average access time.

Unibus Transactions – For a normal memory read (MM11-DP), BUS BUSY is asserted for 1.2 $\mu$s. A cache hit read results in the CPU asserting BUS BUSY for approximately 450 ns. Thus, for every cache hit, about 750 ns are saved.

# CHAPTER 2
# INSTALLATION

## 2.1 SCOPE

Information for installing the KK11-A Cache Memory option and checkout procedures to ensure proper operation of the cache and the system are provided in this chapter.

The following tools are required:

- No. 2 Phillips screwdriver
- Multimeter with ohm capability
- Diagonal cutting pliers
- Soldering iron, 40 watt
- Solder sucker
- Spares kit (Control Distribution)
- Wire-wrap tools

## 2.2 UNPACKING AND INSPECTION

### NOTE
**Customer should not unpack the cache memory option unless a DIGITAL representative is present; to do so voids the warranty.**

### 2.2.1 Unpacking

If the customer's receiving area procedures require it and/or to facilitate inventory, the shipment may be moved to the computer area. Otherwise, unpacking and inventory must be done in the receiving area.

Follow steps 1 through 4 to unpack the shipment.

1. Ensure that the shipping container is sealed. If container is open, notify the customer and record it on the installation report or LARS form.

2. Check the shipment against the packing list to ensure that the correct number of containers has been received and that they are the correct ones. If the shipment is incorrect, notify the customer and the branch service manager or supervisor. The customer should check with the carrier to try and locate the missing item(s).

3. Check all containers for external damage. If any damage is found, notify the customer and record it on the installation report or LARS form.

4. Open containers one at a time, starting with the one marked "OPEN ME FIRST." Inventory the contents of each package with its packing slip and record any missing items on the installation report.

**NOTE**
**Packing materials such as foam fillers and plastic inserts should be retained if reshipment is contemplated.**

### 2.2.2 Inspection
Inspect each component for damage, e.g., scratches, chips, or breaks. Report any damage to the customer and record it on the installation report. Report any damaged components that require replacement immediately to the branch service manager.

### 2.3 PRE-INSTALLATION CHECK
The KK11-A cannot be installed unless the CPU is a PDP-11/34A. Inspect the serial number tag for proper CPU verification. Ensure that the CPU is operating properly by running the following diagnostics.

| | |
|---|---|
| DFKAA | PDP-11/34 basic instruction test |
| DKKTH | KT exerciser (PDP-11/34) |
| CZQMC | 0–124K memory exerciser (16K) |

The KK11-A cache memory option for the PDP-11/34A consists of the following:

| | |
|---|---|
| M8268 | Cache module |
| H8821 | 20-pin over-the-top (OTT) connector |
| H8822 | 20-pin over-the-top (OTT) connector |

### 2.4 BA11-KA MOUNTING BOX INSTALLATION PROCEDURE
The BA11-KA mounting box is capable of delivering 64 A of +5 Vdc, which is supplied by two H7441 regulators. The +5 V is distributed to the backplane in the BA11-KA via five Mate-N-Lok connectors. One H7441 +5 Vdc regulator supplies two Mate-N-Lok connectors; the other H7441 +5 Vdc regulator supplies the remaining three Mate-N-Loks. The PDP-11/34A CPU backplane, DD11-PK, attaches to the BA11-KA power distribution board via connectors J9 and J11, thus allowing the CPU backplane the full capabilities of one H7441 regulator (i.e., 32 A of +5 Vdc). To prevent overloading of the +5 Vdc, the current drain of the modules contained in the DD11-PK should not exceed 32 A (Table 2-1).

If the total current drain used by the devices in the BA11-KA exceeds 61 A without cache, an expander box will be needed (Figure 2-1).

**NOTE**
**To prevent overloading of the +5 Vdc, the current drain should be calculated. The current drain should not exceed 32 A in the DD11-PK backplane.**

**SLOT CONFIGURATION "C"**
SEE NOTES 3 & 4

M8267 OR M8268

SEE NOTE 6

M8265

M8266

A B C D E F

#3 #2 #1

SEE NOTE 1

J2

W9042

J1

M8265

M8268

M8266

A B C D E F

#3 #2 #1

**SLOT CONFIGURATION "D"**
SEE NOTE 5

MA-2277

M8268

SEE NOTE 6

M8267

M8265

M8266

SEE NOTE 6

SEE NOTE 2

#5 #4 #3 #2 #1

**SLOT CONFIGURATION "A"**
SEE NOTE 3

SEE NOTE 6

SEE NOTE 1

M8268

W9042 W9042

M8266

M8265

M8267

#5 #4 #3 #2 #1

**SLOT CONFIGURATION "B"**
SEE NOTE 5
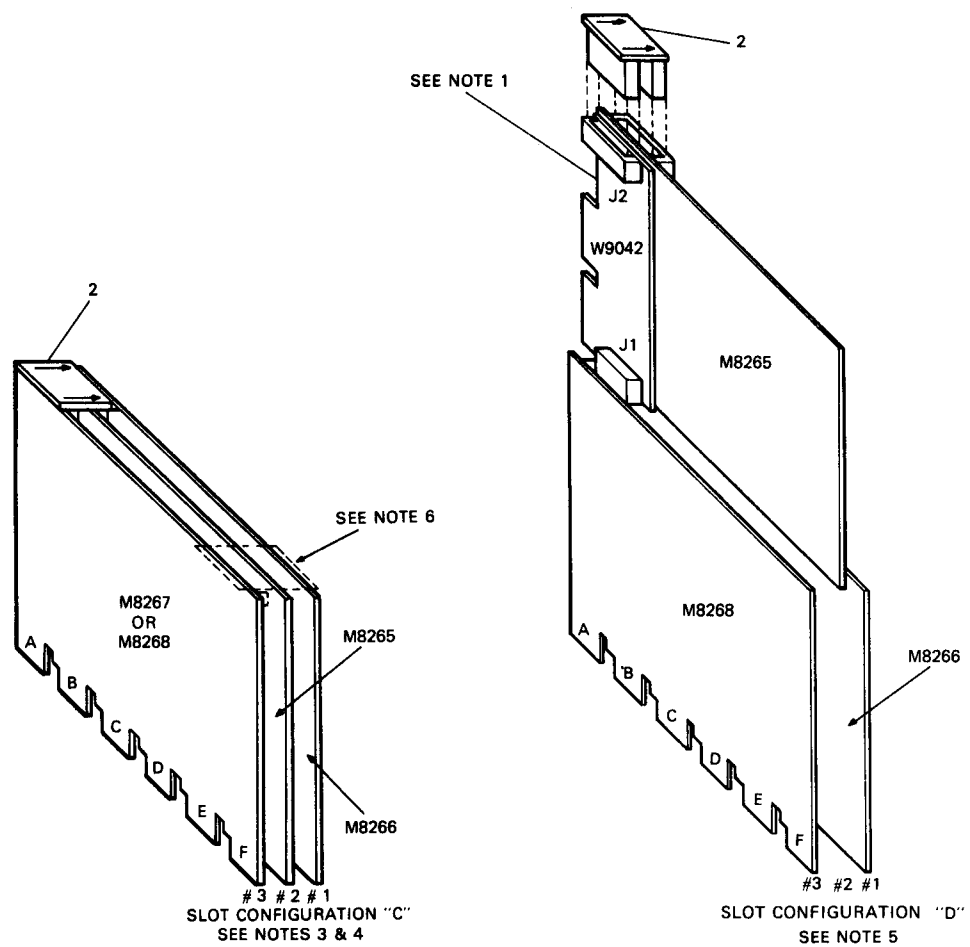
MA-2278
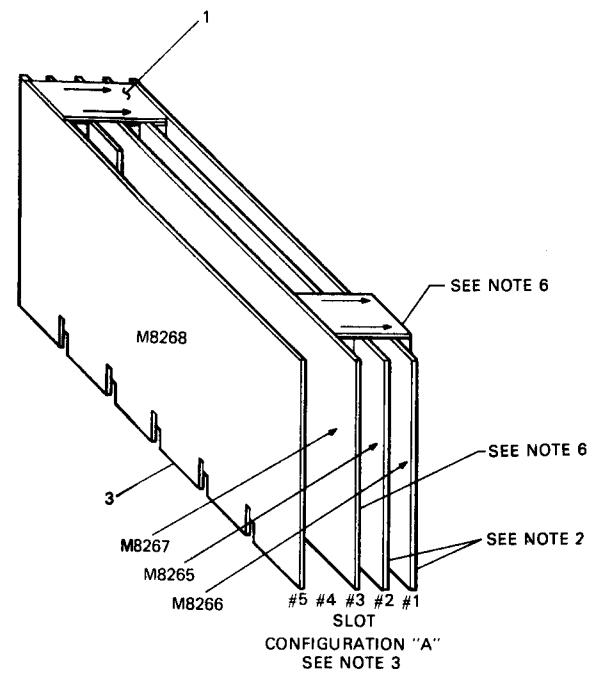
NOTES:

1. THE W9042 EXTENDER BOARD ASSY. IS STORED IN THE BACKPLANE AND IS USED FOR SOME MAINTENANCE OPERATIONS.

2. MODULES M8265 AND M8266 ARE PART OF KD11-EA AND ARE SHOWN FOR REF. ONLY.

3. ALL CONFIGURATIONS SHOWN ARE USED IN THE BA11-K (10.5in. BOX) OR BA11-L (5-1/4 BOX).

4. CONFIGURATION C SHOWS SLOT 3 UTILIZATION FOR EITHER KK11-A OR FP11-A WHEN ONLY ONE IS PRESENT.

5. CONFIGURATIONS B & D SHOW TYPICAL MAINTENANCE SET UP.

6. M8267, 5412416 AND W9042 ARE PART OF FP11-A AND ARE SHOWN FOR REF. ONLY.
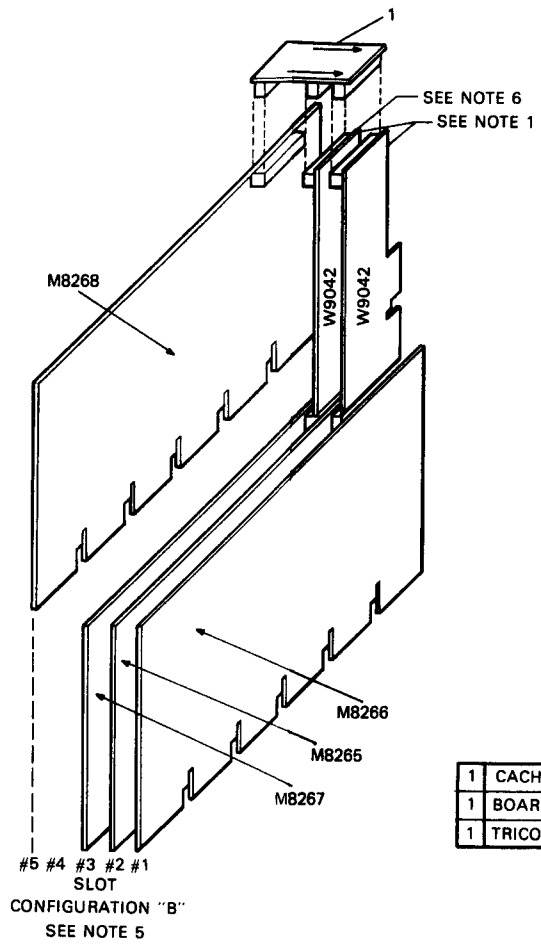
**PARTS LIST**

| | | | |
|---|---|---|---|
| 1 | CACHE MEMORY (KK11-A) | D-UA-M8268-0-0 | 3 |
| 1 | BOARD, INTERCONN 40 PIN | D-UA-H8821-0-0 | 2 |
| 1 | TRICONN BOARD | D-UA-H8822-0-0 | 1 |

Figure 2-1   Cache Installation Diagram

Table 2-1  +5 V Power Consumption
For Some Common Options

| Option Number | Description | +5 VA | Mounting Code |
|---|---|---|---|
| AR11 | 10-bit A/D converter | 4.0 A | Hex |
| DL11-WA/B | Line interface and clock | 2.0 A | Quad |
| DR11-K | Digital I/O | 2.5 A | Quad |
| DUP-11 | Synchronous line interface | 3.6 A | Hex |
| KY11-LB | Programmer's console/interface | 3.0 A | Quad (in PDP-11/34 CPU backplane) |
| LA180 | DECprinter I | 1.5 A | Quad |
| MS11-FP | 8K MOS memory | 2.0 A | Hex |
| MS11-JP | 16K MOS memory | 2.0 A | Hex |
| MM11-CP | 8K core memory | 3.0 A | Hex Quad |
| MM11-DP | 16K core memory | 3.0 A | 2 Hex |
| M7850 | Parity control | 1.0 A | DH* module |
| M9301 | Bootstrap | 2.0 A | DH* module |
| M9302 | Unibus terminator | 1.3 A | DH* module |
| RX11 | Floppy disk | 1.5 A | Quad |
| TMB11 | Tape control | 6.0 A | SU† |
| LP11W,V | Printer | 1.5 A | Quad |
| MM11-YP | 32K core memory | 5.0 A | 2 Hex |
| FP11-A | PDP-11/34 floating-point processor (FPP) | 7.0 A | Hex |
| DL11A-E | Asynchronous line interface | 1.8 A | Quad |
| DU11 | Synchronous line interface | 2.0 A | Quad |
| KG11 | CRC generator | 1.2 A | Quad |
| RK11-D | RK05 controller | 7.5 A | SU† |
| KD11-EA | PDP-11/34 A CPU | 11.5 A | 2 Hex |
| M9312 | Bootstrap | 2.0 A | DH module |
| RK611 | RK06 controller | 15.0 A | 2 SUs† |

*DH = double height.

†SU = single unit.

Perform the following steps when installing KK11-A with the FP11-A present.

1. Turn system power OFF.

2. Extend the BA11-KA mounting box from the system.

3. Remove the top cover by loosening the screw at the side, then slide the cover off.

4. If the KY11-LB is present, remove the two maintenance connectors from the M8266.

5. Remove the 54-12416 OTT connector from the M8266 and M8267 modules.

6. Remove the M8266 module from slot 1.

7. Visually verify that M8266 ECO No. 4 is installed by checking that resistor R2 is 1 kΩ.

NOTE
Where R2 is less than 1 kΩ, install a 1 kΩ resistor
per instructions on M8266 ECO No. 4.

8. Replace M8266 into slot 1 and replace the 54-12416 over-the-top connector.

9. Remove the H8821 connector from the M8265 and M8267 modules.

10. Remove any module in slot five and carefully reconfigure the modules in the DD11-PK backplane (Figure 2-2).

11. Insert the M8268 module into DD11-PK slot 5.

**NOTE**
**To prevent overloading of the +5 Vdc, make sure that the current drain does not exceed 32 A. Calculate power consumptions using 4 A for KK11-A (cache), 7 A for FP11-A, and 11.5 A for KD11-EA.**
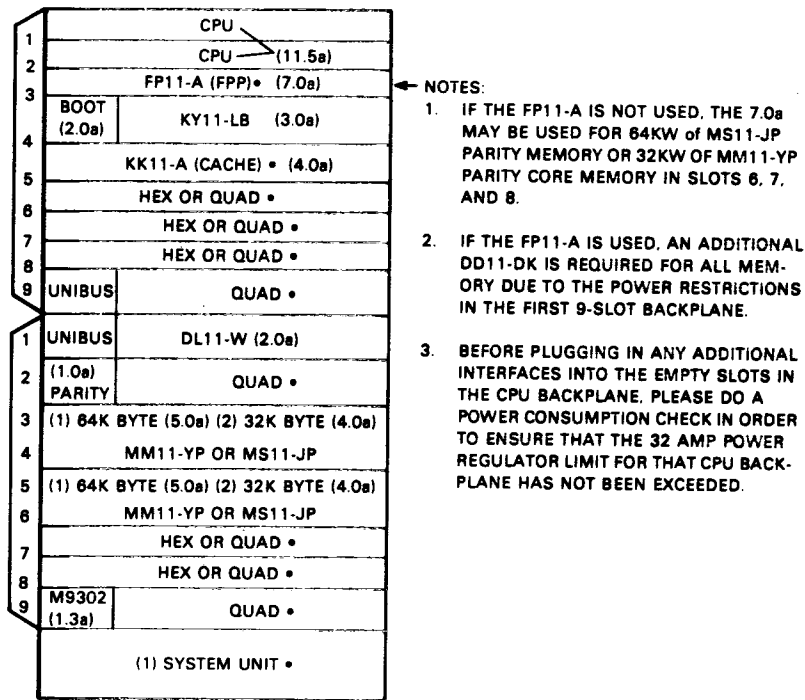


Figure 2-2  Power/Configuration Schematic

12. Install the H8822 connector on the M8265, M8267, and M8268 modules (slots 2, 3, and 5, respectively). Make sure the arrow on this connector points toward slot 1.*

13. Check that both FORCE MISS switches S1 and S2 are on. Have both switch handles pointing toward the console.

14. Loosen both screws on the bottom of the BA11-KA mounting box and remove the cover.

---

*When using other than the M9301-YF bootstrap terminator, the handle of the bootstrap terminator may interfere with the H8822 connector. Therefore, carefully remove that part of the handle which interferes.

15. Check for continuity between backplane connection C01E1 and B02A1. This is the cache hit line; if not present, a jumper (30 gauge wire, DIGITAL P/N 91-05740) should be installed. Then recheck for continuity.

16. Replace the bottom and top covers, and slide the BA11-K into the system chassis.

17. Power-up the system.

18. Verify the CPU, cache, and FP11-A by running the diagnostics listed in Paragraph 2.7.

To install cache when the FP11-A is not present, perform the following steps.

1. Repeat steps 1 through 8.

2. Remove any module in slot 3 and carefully reconfigure the modules in the DD11-PK backplane (Figure 2-2).

3. Insert the M8268 cache module into slot 3 of the DD11-PK.

4. Install the H8821 connector on the M8265 and M8268 modules (slots 2 and 3, respectively). Make sure that the arrow on this connector points toward slot 1.*

5. Check that both FORCE MISS switches S1 and S2 are on. Have both BATT switches pointing toward the console.

6. Complete steps 14–18 in the previous procedure.

## 2.5  BA11-L MOUNTING BOX INSTALLATION PROCEDURE
The 13.3 cm (5 in) BA11-L mounting box can contain a power supply with either a 32 A or 25 A +5 V regulator. Use the following chart in determining whether you have the proper 32 A supply.

| Current | Regulator |
|---------|-----------|
| 25 A | H777-AA |
|  | -AB |
|  | -BA |
|  | -BB |
| 32 A | H777-CB |
|  | -CA |
|  | -DA |
|  | -DB |

### NOTE
To prevent overloading of the +5 Vdc, make sure that the +5 Vdc current consumption does not exceed the capacity of the regulator.

---

*When using other than the M9301-YF bootstrap terminator, the handle of the bootstrap terminator may interfere with the H8822 connector. Therefore, carefully remove that part of the handle which interferes.

Perform the following steps when installing the KK11-A in a BA11-L mounting box.

1. Slide the wire frame out of the wrap-around.

2. Turn CB1 to off first, then turn the DC ON/DC OFF switch to DC OFF.

3. If the KY11-LB is present, remove the two maintenance connectors from the M8266 module.

4. Make sure that the DD11-PK is Rev C or later.

5. Remove the M8266 module from slot 1 and visually verify that ECO M8266 No. 4 (R2 = 1 kΩ) is installed.

**NOTE**
**When R2 is less than 1 kΩ, change this resistor per
instructions on M8266 ECO No. 4.**

6. Replace M8266 into slot 1.

7. Remove any module in slot 3 and carefully reconfigure the system.

8. Insert the M8268 cache module into DD11-PK slot 3 or 5.

9. Install the H8821 or H8822 connector on the M8265 and M8268 modules (slots 2 and 3 or slots 2 and 5, respectively). Make sure arrow points toward slot 1.

10. Check that both FORCE MISS switches S1 and S2 are on. Have both switch handles pointing toward the console.

11. Reconnect the KY11-LB maintenance cable to the M8266 module.

12. Turn CB1 on and slide the wire frame inside the wrap-around carefully.

13. Turn DC OFF to DC ON.

14. Verify CPU, memory, and cache by running the diagnostics listed in Paragraph 2.7.

## 2.6 OPERATION
The cache module is program transparent. The only observable effect while in operation will be reduced program run time.

## 2.7 CHECKOUT PROCEDURES
Run CPU and PDP-11/34A cache diagnostics for verification of the functionality of the options.
  • PDP-11/34 Diagnostics

| DFKAA | PDP-11/34 | Basic instruction test |
|-------|-----------|------------------------|
| DFKAB | PDP-11/34 | Traps test |
| DFKAC | PDP-11/34 | EIS instruction test |
| DKKTH | | KT exerciser (PDP-11/34) |
| CZQMC | | 0–124K memory exerciser (16K) |

- PDP-11/34A FPP Diagnostics

  | | | |
  |---|---|---|
  | DFFPB | PDP-11/34 | FPP Diagnostic Part 1 |
  | DFFPB | PDP-11/34 | FPP Diagnostic Part 2 |
  | DFFPC | PDP-11/34 | FPP Diagnostic Part 3 |

- PDP-11/34 Cache Diagnostics

  | | | |
  |---|---|---|
  | CFKKAA | PDP-11/34 | Cache diagnostics |

  The startup procedure is non-stanard form. A "RUN" command is required in addition to the normal load and go at address 200.

  Procedures are included with the diagnostic media.

- DEC/X11 monitor – the QABM monitor must be patched when the command "CON" for cache on is given.

  The patch for this problem is:

  | | | |
  |---|---|---|
  | MOD | 13136 | 240 |
  | | 13140 | 240 |

## 3.1 MAINTENANCE PHILOSOPHY

The field maintenance and repair philosophy reflects a module replacement approach. Once the cache has been identified as the failing option in the PDP-11/34A system, the module should be replaced. The faulty cache is returned to the Maynard facility in Massachusetts or to European Depots for repair (whichever location is feasible). Because of the complexity of the cache module and its etch width, on-site component level repair is not encouraged. The standalone diagnostics should be run to detect the cache module failure.

## 3.2 SYSTEM MAINTENANCE AND TESTING

For a PDP-11/34A system that is unable to load diagnostics, use procedures in Chapter 6 of the *PDP-11/34A System User Manual* to diagnose the problem. Table 3-1 lists the maintenance equipment required to troubleshoot the cache.

Table 3-1  Maintenance Equipment Required

| Equipment | Manufacturer | Model/Type/Part No. | DEC Part No. |
|---|---|---|---|
| Oscilloscope | Tektronix | 453* | |
| Volt/Ohmmeter (VOM) | Triplett | | 29-13510 |
| Unwrapping Tool | Gardner-Denver DEC Catalog #11812A | 505 244 475 | 29-18387 |
| Hand-Wrap Tool | Gardner-Denver DEC Catalog #11811A | A-20557-29 | 29-18301 |
| Wire Strippers | Miller | 101S | 29-13467 |
| Module Extender Boards (2) | DEC | | W9042 |

*Tektronix type 453 oscilloscope is adequate for most test procedures; Type 454 or equivalent may be required for some measurements.

## 3.3 TROUBLESHOOTING GUIDELINES

The following guidelines are provided for debugging failures in the cache memory module installed in a PDP-11/34A system. Standard PDP-11/34A diagnostics should be run first before attempting to follow the procedures outlined in this section.

To verify the system integrity, run the following diagnostics in the sequence given below.

| | |
|---|---|
| DFKAB | Traps Test (at lease Rev C) |
| DFKAA | PDP-11/34 CPU Test |
| DFKAC | EIS Test |
| CZQMC | 0–124K Memory Exerciser |

If the FP11-A option is included with the system, run the following diagnostics.

| | |
|---|---|
| DFFPB | PDP-11/34 FPP Diagnostic – Part 1 |
| DFFPB | PDP-11/34 FPP Diagnostic – Part 2 |
| DFFPC | PDP-11/34 FPP Diagnostic – Part 3 |

The flowchart in Figure 3-1 is a helpful tool in troubleshooting the system.

3-3

START

1 HAVE ALL DIAGNOSTICS RUN TO COMPLETION

NO → REFER TO CHAPTER 6 OF THE PDP-11/34A USER'S MAN.

YES

VERIFY VIA SYSTEM SERIAL NAME TAG

2 IS THE CPU A PDP-11/34A

NO → CACHE MEM SHOULD NOT BE INSTALLED ON ANY SYS. OTHER THAN AN 11/34A

YES

3 CALCULATE THE +5 VDC CURRENT DRAIN IN THE 11/34A CPU BACKPLANE

4 IS THE THE CPU BOX TYPE 10.5 INCHES

NO → BA11-L

YES → A

IS THE CPU BOX TYPE 5-1/4"

NO → STOP

YES

DOES THE CURRENT DRAIN EXCEED 28 AMPS WITHOUT KK11A INST.

NO → GO TO 11

YES

MUST USE AN EXPANDER BOX

A

DOES CURRENT DRAIN EXCEED 28 AMPS WITHOUT KK11-A

NO →

YES

DOES SPACE ALLOW FOR: EXPANDER BOX & CURRENT AVAILABLE

NO →

YES

5 DOES CURRENT IN BA11-KA MOUNTING BOX EXCEED 61 AMPS (WITHOUT KK11-A INSTALLED)

NO → GO TO 6

YES → MUST USE EXTENDER BOX

DOES CPU BACKPLANE EXCEED 28 AMPS WITHOUT CACHE

NO →

YES → MUST USE AN EXPANDER BOX

MA-2284

Figure 3-1 Troubleshooting Flowchart
(Sheet 1 of 5)

SHEET 1

CACHE SLOT
F03A2
OR
F05A2

(6)

DOES
+5 VDC = 5.0
VDC ± 5% AT
SLOT WHERE
CACHE IS
INSTALLED

NO → ON BA11-KA BOX,
ADJUST +5 VDC
REGULATOR
(H7441) TO
+5.20 VOLTS

YES

(7)

ANY
MOS MEMORY
IN THE SYSTEM

NO → THEN SYSTEM
SHOULD
HAVE CORE

YES

THIS CONCLUDES
THAT BATTERY
BACKUP IS NOT
INSTALLED

(8)

ARE
BATTERY
BACKUP JUMPERS
INSTALLED

NO → BATTERY BACKUP
IS INSTALLED
& NO JUMPERS

GO TO 11

YES

THE CPU
ONLY SHOULD
HAVE JUMPERS
INSTALLED

JUMPER CONFIGURATION
DD11-PK
+5 VB → +5 V JUMPER IN
+15 VB → +15 V JUMPER IN
−15 VB → −15 V JUMPER IN

SEE FIG. 3-2

(9)

ALL OTHER
BACKPLANES
IN THE CPU
BOX SHOULD BE

JUMPER CONFIGURATION
DD11-DK,CK
+5 VB → +5 V JUMPER OUT
+15 VB → +15 V JUMPER IN
−15 VB → −15 V JUMPER IN

(10)

ANY
MOS MEM
IN ANY
BACKPLANE
OTHER THAN
THE CPU
BACKPLANE

NO → GO TO 11

YES

IF THE JUMPER IS IN THE CPU
BACKPLANE:
ADD .5 AMPS OF +5 VDC FOR
EACH MOS MEMORY BOARD
NOT IN THE CPU BACKPLANE
(CPU BOX ONLY) TO CURRENT
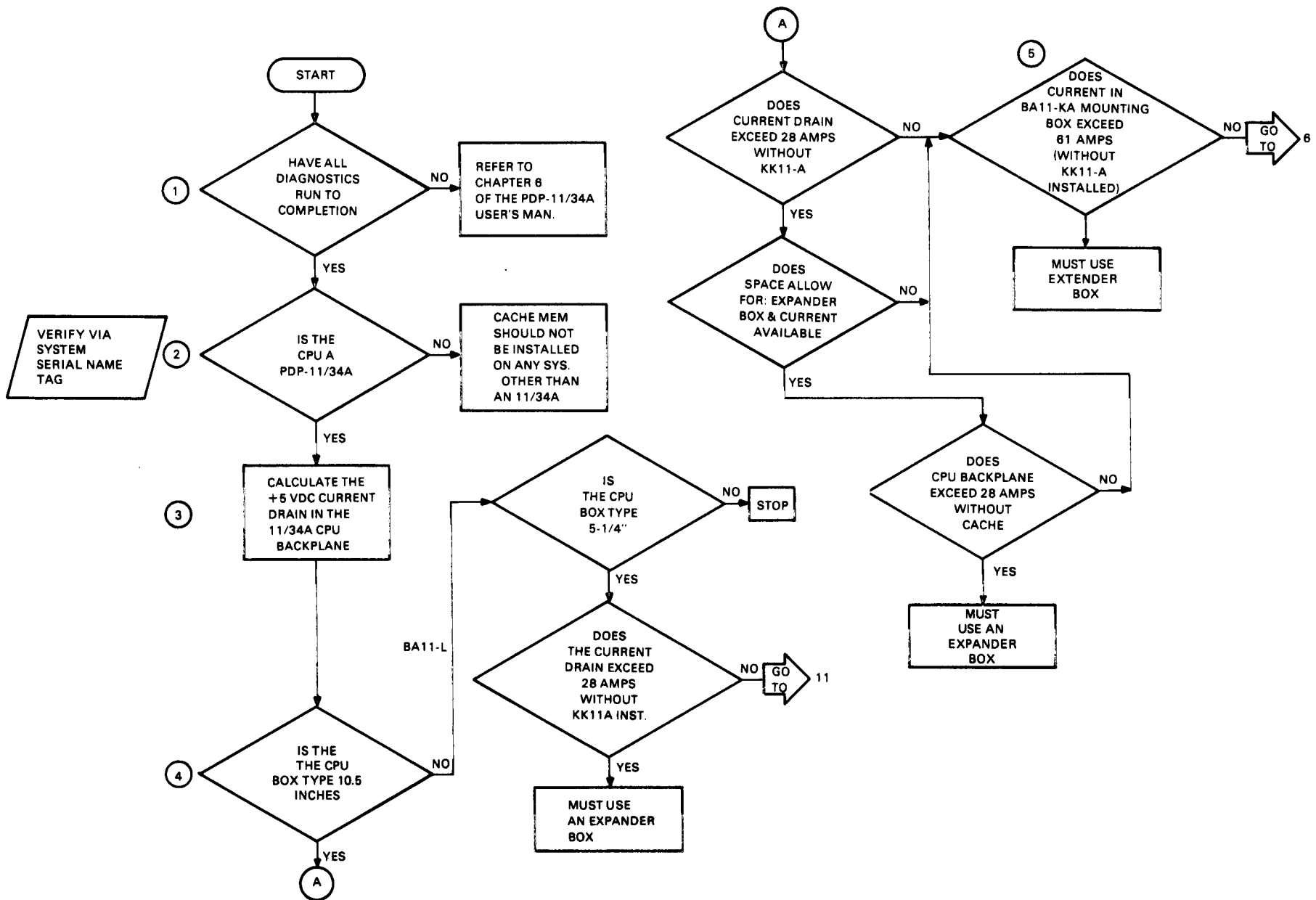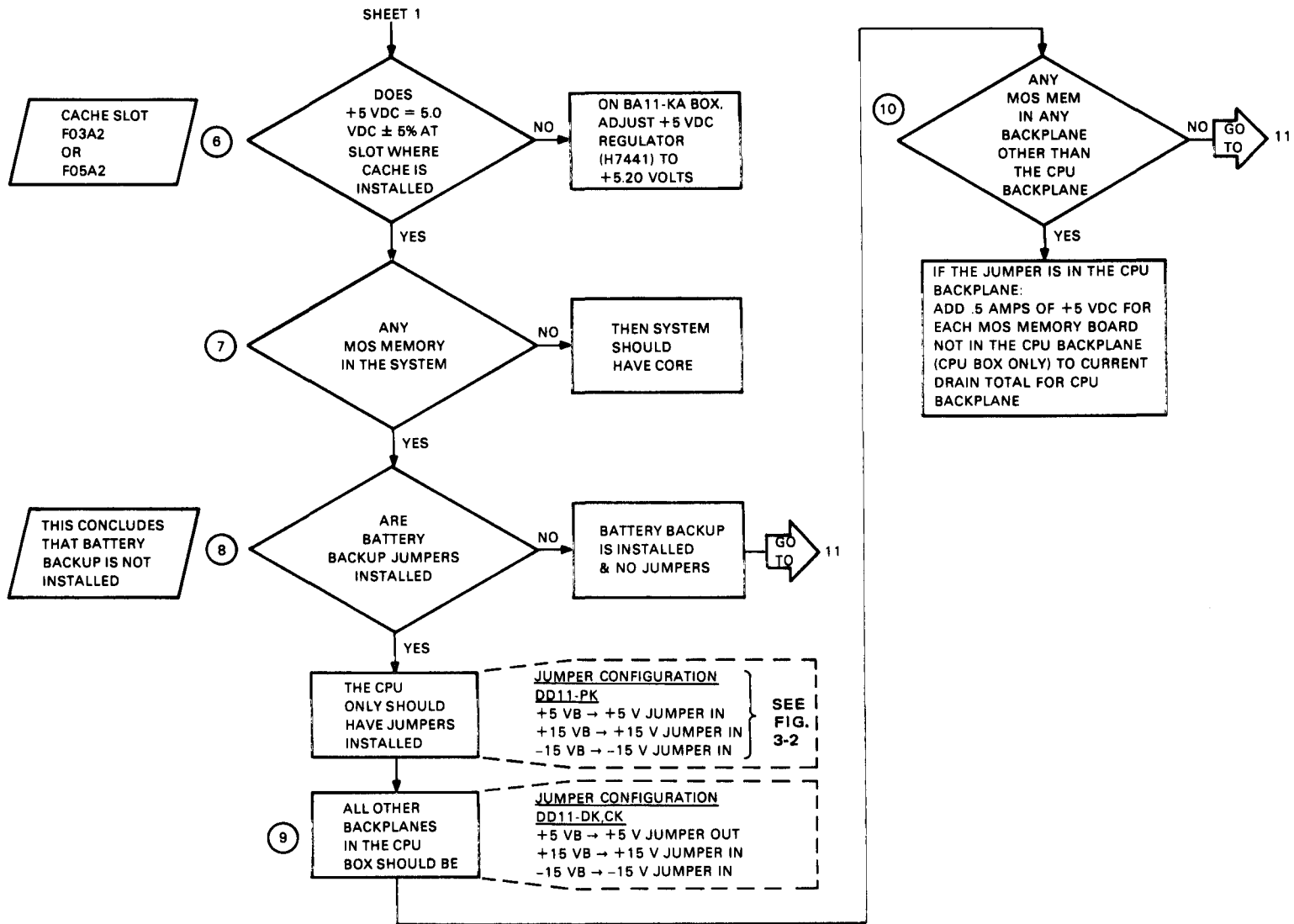DRAIN TOTAL FOR CPU
BACKPLANE

MA-2282

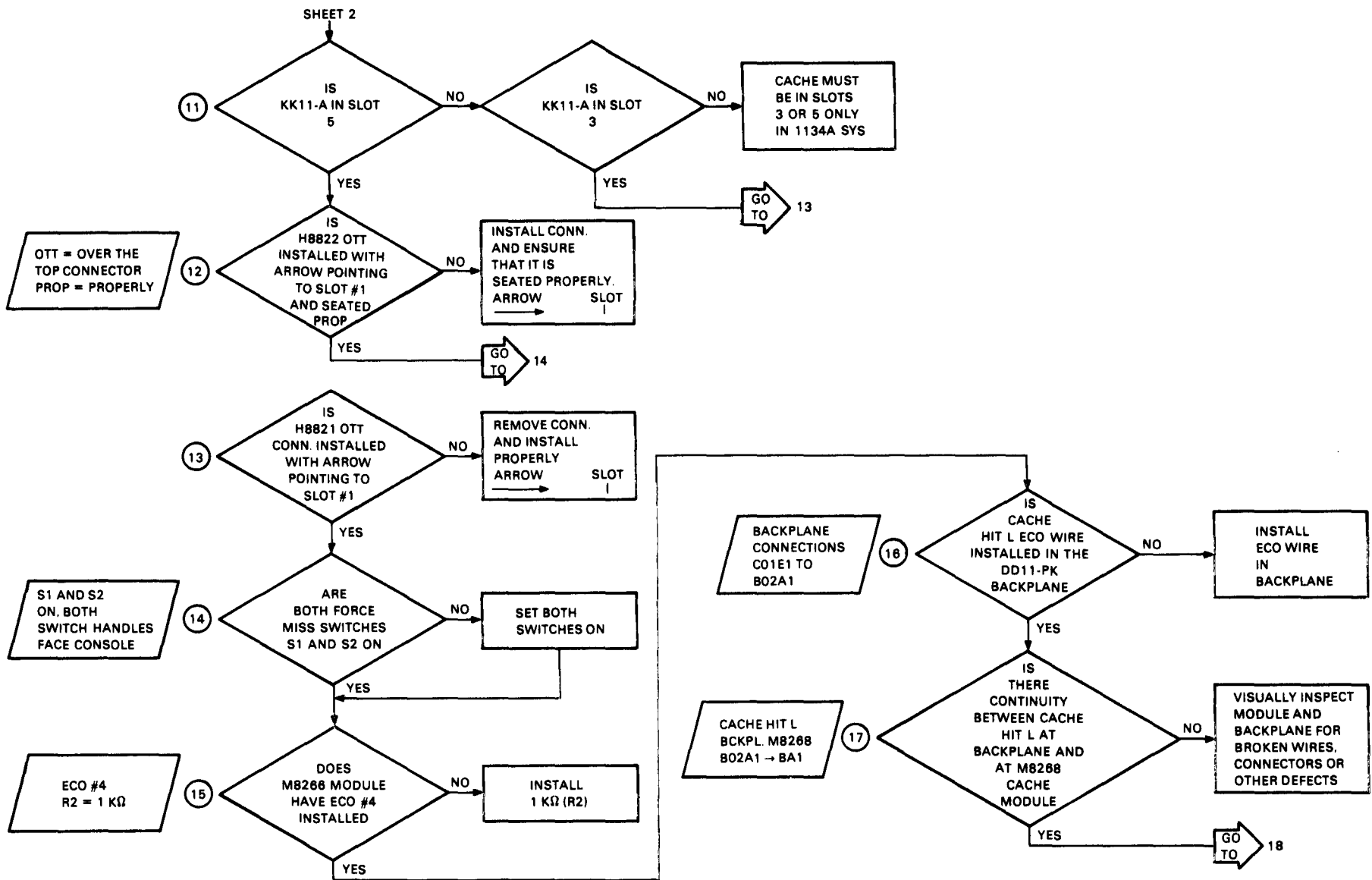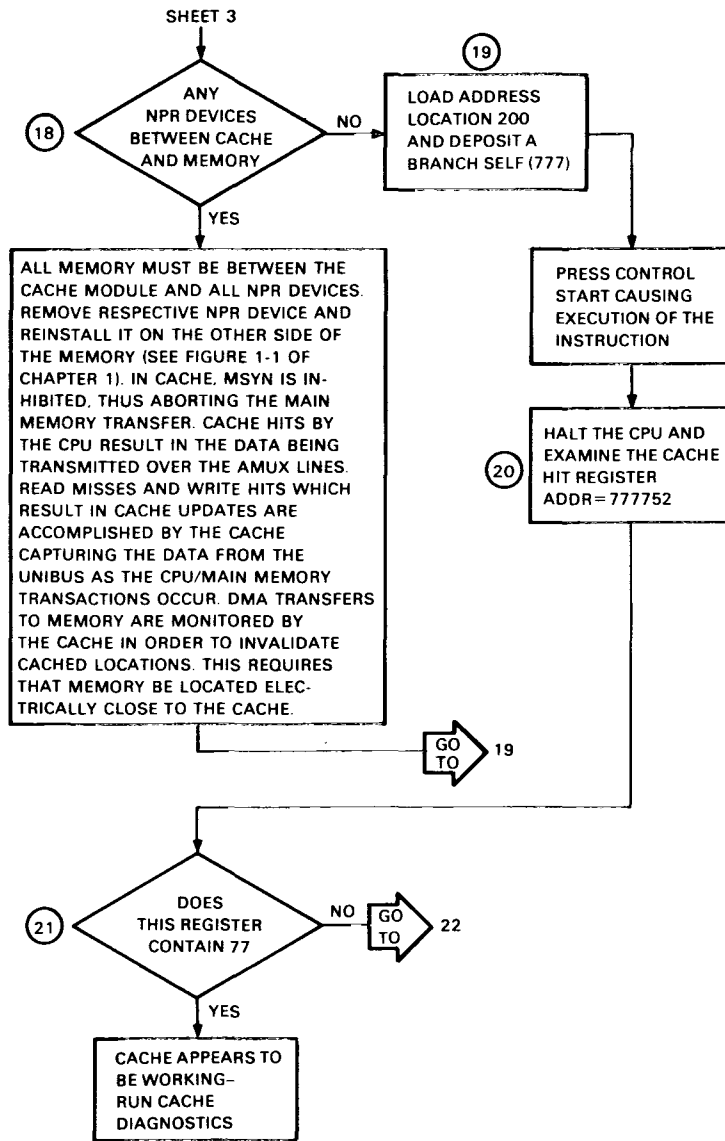Figure 3-1   Troubleshooting Flowchart
(Sheet 2 of 5)

Figure 3-1 Troubleshooting Flowchart
(Sheet 3 of 5)

MA-2263

3-5

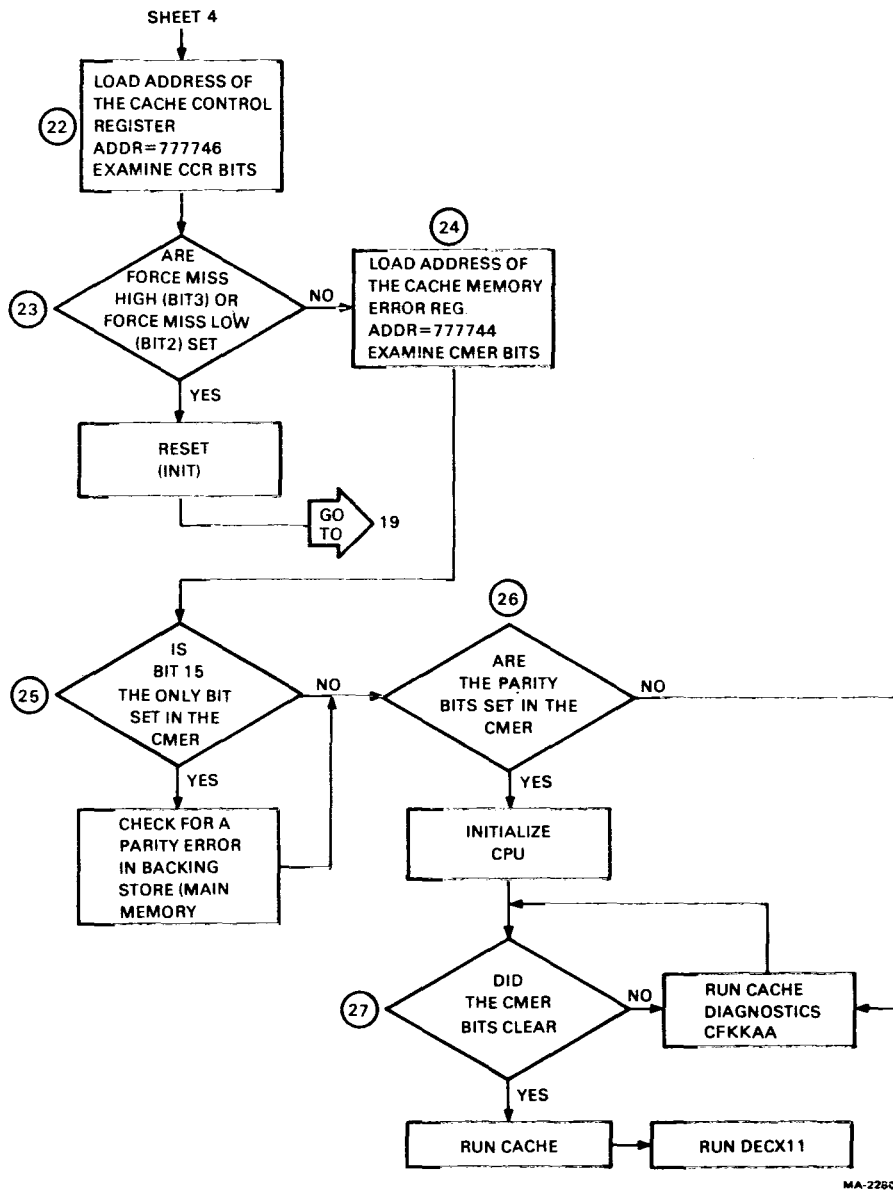Figure 3-1  Troubleshooting Flowchart
(Sheet 4 of 5)

(22) LOAD ADDRESS OF
THE CACHE CONTROL
REGISTER
ADDR=777746
EXAMINE CCR BITS

(23) ARE
FORCE MISS
HIGH (BIT3) OR
FORCE MISS LOW
(BIT2) SET

NO

(24) LOAD ADDRESS OF
THE CACHE MEMORY
ERROR REG.
ADDR=777744
EXAMINE CMER BITS

YES

RESET
(INIT)

GO
TO  19

(25) IS
BIT 15
THE ONLY BIT
SET IN THE
CMER

NO

(26) ARE
THE PARITY
BITS SET IN THE
CMER

NO

YES

CHECK FOR A
PARITY ERROR
IN BACKING
STORE (MAIN
MEMORY

YES

INITIALIZE
CPU

(27) DID
THE CMER
BITS CLEAR

NO

RUN CACHE
DIAGNOSTICS
CFKKAA

YES

RUN CACHE → RUN DECX11

MA-2280

Figure 3-1   Troubleshooting Flowchart
(Sheet 5 of 5)

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**+15V JUMPER**

**-15V JUMPER**

**SEE VIEW A**

**DD11-P**

**P2**

**P3**

**P4**

**+5V JUMPER**

**PIN A01A1**

**GND**

**-15**

**+15**
**+15B**
**-15B**
**+5B**
**-5**

**DC LO**
**AC LO**

**LTC**

**+20**

**+5**

NOTES

1. JUMPERS SHOWN ARE

    -15 TO -15B

    +15 TO +15B

    +5 TO +5B

2. USE #20 INSULATED
    BUS WIRE FOR JUMPERS

**VIEW A**

11-5343

Figure 3-2   Backplane Jumpers

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What features are most useful? _____

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