

KXT11-CA ROM Listing

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INTRODUCTION

This is a general overview of the KXTNT KXT11-CA-macro V05.00 native firmware implementation.

The firmware was written in several modules which were assembled separately and linked to produce the complete native firmware. For purposes of generating a listing for publication, a command procedure was developed which converts these modules into a single module which, when assembled, yields a listing that contains the actual addresses in the address column and the operand field.

The following is a list of each of the modules and a brief description of the function provided by each. A more detailed description proceeds each module:

ABAUD (Auto Baud) - Performs the auto baud function for serial ODT

ACCUM (Accumulate Number) - Accumulates a 16-bit number from octal input

ADDREG (Get Address/Register Number) - Inputs an address or register number for serial ODT

BSUPV (Boot Supervisor) - Controls the boot process

CHKCHR (Check Character) - Polls for input from console line

DATCOM (Data/Command) - Inputs data and commands for serial ODT

DECTST (Decode Test) - Decodes Q-Bus controlled test commands

DEPOS (Deposit) - Performs the deposit function for serial and Q-Bus ODTs

DINIT (Device Initialization) - Initializes all local I/O devices

DISPST (Display String) - Sends a print string to the console serial port

DISPWD (Display Word) - Converts a 16-bit word to an ASCII string and sends the string out to the console serial port

DMALD (DMA Load) - Controls the execution of the DMA load command

ENTRY (Entry Points) - Defines the two entry points to the native firmware (173000, 173004)

EXAMIN (Examine) - Performs the ODT examine function

EXTEST (Execute Test) - Executes each of the self tests

GETIN (Get Input) - Waits for and gets input from console serial line

GOPROC (Go/Proceed) - Performs both the Go and Proceed function of ODT

INIT (Initialization) - Initializes the local I/O

KXTDEF (KXT Definitions) - Defines the KXT specific constants used by the native firmware, KUI and MicroPower

LBTEST (Loop Back Test) - Performs all the self tests executed when in the loop back test mode

NFDEF (Native Firmware Definitions) - Defines all general native firmware related constants

PUTEST (Power-Up Tests) - Performs the appropriate power-up self tests

~ PWRUP (Power-Up Interrupt Handler) - Top level routine entered by Power-Up interrupt (173000)

QCOMIN (Q-Bus Command Interpreter) - Decode Q-Bus commands passed to first word of two-port RAM

QODTM (Q-Bus ODT Monitor) - Controls Q-Bus ODT

RESTRT (Restart Interrupt Handler) - Top level routine entered by Restart interrupt (173004)

SAVERG (Save Registers) - Save the user context of the CPU registers on entry of ODT

SETLED (Set LEDs) - Controls the LED display

SLFTS0 (Self Test Overlay 0) - Normally mapped section of self tests (tests 1 through 7)

~ SLFTS1 (Self Test Overlay 1) - Overlay section of self tests (tests 10 through 13)

SODTM (Serial ODT Monitor) - Controls serial ODT

SPR5SU (Stack Pointer/R5 Setup) - Initializes stack pointer and R5 for particular memory map selection

TNNERR (Test N Error Decoder) - Decodes error from given test

TRAP10 (Trap 10 Emulator) - Emulates trap to 10

TRAP24 (Trap 24 Emulator) - Emulates trap to 24

TRAP4 (Trap 4 Emulator) - Emulates trap to 4

TRAPX (Trap X Emulator) - Emulates trap to address passed in two-port RAM

TU58BT (TU58 Boot) - TU58 primary loader

VERS (Version) - Version code definition

WAITST (Wait State) - Wait for Q-Bus command loop

FIRMWARE MEMORY ORGANIZATION

The native firmware is contained in a 4 K word set of ROMs which are mapped in a 3 K word space with 1 K of overlay. It is organized into five sections in the native ROM. Table 1 describes these sections.

Table 1 Memory Organization

KXT Memory Address	ROM Address	Description
160000 - 163777	0000 - 3777	Normally mapped section of overlay memory (OVL0)
164000 - 172777	4000 - 12777	Permanently mapped section 1 (PERM1)
173000 - 173007	14000 - 14007	Interrupt entries (VECT)
173010 - 173777	14010 - 14777	Permanently mapped section 2 (PERM2)
160000 - 163777	15000 - 17777	Overlay section 1 (OVL1)

IMPORTANT ADDRESSES

The addresses listed in Table 2 are of special interest. Any address specified by symbolic name can be determined by looking that name up in the symbol list at the end of the native firmware listing.

Table 2 Special Addresses

Name	Module	Description
PERV(173000)	ENTRY	Power-up interrupt address
RSTV(173004)	ENTRY	Restart interrupt address
FARSTR	PUTEST	Fatal self test error loop
FAS	BSUPV	Fatal error loop when invalid Boot/Self Test switch position set
FAR	RESTRT	Loop address after Restart interrupt when a fatal error condition exists

REGISTER USE

The only CPU register that has a fixed use throughout the native firmware is R5. This register is used to point to the top of the native RAM (the highest word address) and is referenced throughout the firmware. This register should never be altered while the firmware is executing.

```

5          .SBTTL KXTDEF.MAC - Dual Port RAM definitions on KXT11CA
6          .ident /V1.5/
7          ;
8          ; FUNCTIONAL DESCRIPTION:
9          ;
10         ; This module defines addresses and bit definitions for various registers
11         ; on the KXT11-CA. The following naming conventions are used:
12         ;
13         ; KW.xxx = word addressable register on the KXT11-C
14         ; KL.xxx = Low byte addressable register on the KXT11-C
15         ; KH.xxx = High byte addressable register on the KXT11-C
16         ; KXSxxx = Read/write bit definition for a KXT11-C register
17         ; KWSxxx = Write only bit definition for a KXT11-C register
18         ; KRSxxx = Read only bit definition for the KXT11-C register
19         ; KMSxxx = Multi-bit mask for a KXT11-C register
20         ; KPSxxx = Bit Pattern for Multi-bit fields of KXT11-C registers
21         ;
22         ; These definitions can be used in one of two ways. They can be accessed
23         ; by using the macro KXTDFS which will define each symbol locally in the
24         ; module using the macro. Secondly, this module can be assembled which will
25         ; define each symbol globally in an object that other modules can link to.
26         ; A KXT kernel includes the global definitions so any application merging
27         ; with a KXT kernel need not use the local macro.
28         ;
29         ;-
30         ;
31         ; IF THIS MODULE IS ASSEMBLED, THEN GENERATE THE SYMBOLS IN A GLOBAL MODE
32         ; and show the macro expansions
33         .list me
34         KXTD$$ <==>
35         ;
36         ; KXT11-C CSR A definitions
37
38         177520          KW.CSA ==: 177520          ; KXTCSRA word location
39         177520          KL.CSA ==: 177520          ; KXTCSRA low byte location
40
41         000001          KXSODT ==: 1              ; Sync Mode on channel B enable
42         000002          KXS2EN ==: 2              ; SLU 2 read enable
43         000004          KXSMA ==: 4              ; Sync Mode on channel A enable
44         000010          KXSTC ==: 10             ; Terminal connect
45         000020          KXSTIS ==: 20            ; Terminal in service
46         000040          KXSDPE ==: 40            ; Diagnostic PROM enable
47         000100          KXS RTE ==: 100          ; Real-time clock interrupt enable
48         000200          KXSCTE ==: 200          ; Counter interrupt enable
49
50         ; KXT11 CSR B definitions
51
52         177522          KW.CSB ==: 177522          ; Word address for KXTCSRB
53         177522          KL.CSB ==: 177522          ; Low byte address for KXTCSRB
54
55         000001          KRSTNS ==: 1              ; Terminal in normal service mode
56         000016          KMSMAP ==: 16            ; Memory map configuration
57         000002          KXSMP0 ==: 2              ; Memory map bit 0
58         000004          KXSMP1 ==: 4              ; " " " 1
59         000010          KXSMP2 ==: 10            ; " " " 2
60         000360          KMSWS ==: 360            ; Boot/Self Test switch position

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; KXT11 CSR C definitions

177524	KW.CSC ==:	177524	; Word address for KXTCSR
177524	KL.CSC ==:	177524	; Low byte address for KXTCSR
000001	KX\$LD0 ==:	1	; LED 0
000002	KX\$LD1 ==:	2	; LED 1
000004	KX\$LD2 ==:	4	; LED 2
000010	KX\$LD3 ==:	10	; LED 3
000360	KM\$IDS ==:	360	; KXT11-C ID switch setting

; KXT11 CSR D definitions

177530	KW.CSD ==:	177530	; Word address for KXTCSR
177530	KL.CSD ==:	177530	; Low byte address for KXTCSR
177531	KH.CSD ==:	177531	; High byte address for KXTCSR
000001	KX\$R20 ==:	1	; Dualport RAM interrupt 120 request
000002	KX\$R24 ==:	2	; Dualport RAM interrupt 124 request
000004	KX\$R34 ==:	4	; Dualport RAM interrupt 134 request
000010	KX\$I20 ==:	10	; Dualport RAM interrupt 120 enable
000020	KX\$I24 ==:	20	; Dualport RAM interrupt 124 enable
000040	KX\$I34 ==:	40	; Dualport RAM interrupt 134 enable
000100	KX\$DEN ==:	100	; Dualport RAM enable
000200	KX\$DRT ==:	200	; Dualport RAM non-maskable trap
000400	KX\$BHE ==:	400	; B-halt enable
001000	KX\$BHF ==:	1000	; B-halt flag
002000	KX\$ORE ==:	2000	; Q-bus reset enable
004000	KX\$QRF ==:	4000	; Q-bus reset
010000	KX\$BQI ==:	10000	; Block Q bus interrupt register
020000	KX\$QIE ==:	20000	; QIR interrupt enable
040000	KR\$QRP ==:	40000	; QIR request pending
100000	KX\$NXM ==:	100000	; Non-existent memory flag

; KXT11 I/O Buffer Control definitions

177540	KW.IOC ==:	177540	; Word address for IOBFRC
177540	KL.IOC ==:	177540	; Low byte address for IOBFRC
177541	KR.IOC ==:	177541	; High byte address for IOBFRC
000001	KW\$PB0 ==:	1	; PIO port B byte 0 direction
000002	KW\$PB1 ==:	2	; PIO port B byte 1 direction
000004	KW\$PB2 ==:	4	; PIO port B byte 2 direction
000010	KW\$PB3 ==:	10	; PIO port B byte 3 direction
000020	KW\$PB4 ==:	20	; PIO port B byte 4 direction
000040	KW\$PB5 ==:	40	; PIO port B byte 5 direction
000100	KW\$PB6 ==:	100	; PIO port B byte 6 direction
000200	KW\$PB7 ==:	200	; PIO port B byte 7 direction
000400	KW\$PLD ==:	400	; PIO port A low-byte direction
001000	KW\$PHD ==:	1000	; PIO port A high-byte direction
002000	KW\$P0D ==:	2000	; PIO port C word 0 direction
004000	KW\$P1D ==:	4000	; PIO port C word 1 direction
010000	KW\$P2D ==:	10000	; PIO port C word 2 direction
020000	KW\$P3D ==:	20000	; PIO port C word 3 direction
040000	KW\$PAB ==:	40000	; PIO ports A and B active pull-up

```

100000          KWSPCO ==: 100000          ; PIO port C active pull-up

; DUAL PORT RAM IOP COMMAND REGISTER DEFINITIONS

175000          KW.CMD ==: 175000          ;KXT DPR REGISTER 0 WORD LOC.
175000          KL.CMD ==: 175000          ; " " " " LOW BYTE LOC.
175001          KH.CMD ==: 175001          ; " " " " HIGH BYTE LOC.

;
; SYSTEM COMMAND BIT DEFINITIONS
;
000001          KXSTRC ==: 1              ;TRAP COMMAND
000002          KXSDMC ==: 2              ;DMA LOAD COMMAND
000004          KX$INC ==: 4              ;RE-INITIALIZE COMMAND
000010          KXSODC ==: 10            ;ENTER Q BUS ODT MODE COMMAND
000020          KXSSHCH ==: 20           ;SHOW CONFIGURATION COMMAND
000040          KXSNOP ==: 40            ;NO OPERATION COMMAND
100001          KXST01 ==: 100001         ;CSP TEST COMMAND
100002          KXST02 ==: 100002         ;RAM " "
100004          KXST03 ==: 100004         ;ROM " "
100010          KXST04 ==: 100010         ;CPU " "
100020          KXST05 ==: 100020         ;BEVENT " "
100040          KXST06 ==: 100040         ;SLU1 " "
100100          KXST07 ==: 100100         ;SLU2 " "
100200          KXST10 ==: 100200         ;PARALLEL I/O TEST COMMAND
100400          KXST11 ==: 100400         ;DMA TEST COMMAND
101000          KXST12 ==: 101000         ;QIP " "
102000          KXST13 ==: 102000         ;DPR " "

;
; Q BUS ODT COMMAND DEFINITIONS
;
000001          KXSOMD ==: 1              ;OPEN AND EXAMINE MEMORY COMMAND
000002          KXSORD ==: 2              ;OPEN AND EXAMINE REGISTER COMMAND
000004          KXSDED ==: 4              ;DEPOSIT COMMAND
000010          KXSGOD ==: 10            ;GO COMMAND
000020          KXSPRO ==: 20            ;PROCEED COMMAND
100000          KXSEXO ==: 100000        ;EXIT ODT COMMAND

;
; DUAL PORT RAM IOP STATUS REGISTER DEFINITIONS
;
175002          KW.STA ==: 175002         ;KXT DPR REGISTER 1 WORD LOC.
175002          KL.STA ==: 175002         ; " " " " LOW BYTE LOC.
175003          KH.STA ==: 175003         ; " " " " HIGH BYTE LOC.

000007          KM$STF ==: 7              ;STATE FIELD

000000          KPSINI ==: 0              ;INITIALIZATION STATE
000001          KPSSTS ==: 1              ;POWER UP SELF TEST STATE
000002          KPSOTS ==: 2              ;Q BUS CONTROLLED TEST MODE
000003          KPSQOD ==: 3              ;Q BUS ODT MODE
000004          KPSWST ==: 4              ;WAITING FOR COMMAND STATE
000005          KPSPBS ==: 5              ;PRIMARY BOOTSTRAP STATE
000007          KPSNNC ==: 7              ;EXECUTING NON NATIVE CODE

000010          KX$SEF ==: 10            ;STACK ERROR FLAG

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000020          KX$OHL ==: 20          ;ENTER ODT ON HALT FLAG
000040          KX$FEF ==: 40          ;FATAL ERROR FLAG
000100          KX$SOF ==: 100         ;SERIAL ODT FLAG
000200          KX$QOF ==: 200         ;Q BUS ODT FLAG
001000          KX$PWF ==: 1000        ;POWER UP NO BATTERY BACKUP FLAG
002000          KX$BAT ==: 2000        ;BATTERY BACKUP POWER UP FLAG
004000          KX$SXT ==: 4000        ;STACK POINTER NXM TEST FLAG
010000          KX$NXF ==: 10000       ;NXM HANDLING FLAG
020000          KX$BDF ==: 20000       ;BRFAK DISABLE FLAG
040000          KX$DMF ==: 40000       ;DMA LOAD ERROR FLAG
100000          KX$CME ==: 100000      ;COMMAND ERROR FLAG
;
;
; DUAL PORT RAM SYSTEM CONTROL REGISTER 2
;
175004          KW.SC2 ==: 175004       ;KXT DPR REGISTER 2 WORD LOC.
175004          KL.SC2 ==: 175004       ; " " " " LOW BYTE LOC.
175005          KH.SC2 ==: 175005       ; " " " " HIGH BYTE LOC.
;
; ERROR REPORT BIT DEFINITION OF REGISTER 2
;
000001          KX$F01 ==: 1           ;CSR TEST FAILED
000002          KX$F02 ==: 2           ;RAM " "
000004          KX$F03 ==: 4           ;ROM " "
000010          KX$F04 ==: 10          ;CPU " "
000020          KX$F05 ==: 20          ;REVENT " "
000040          KX$F06 ==: 40          ;SLU1 " "
000100          KX$F07 ==: 100         ;SLU2 " "
000200          KX$F10 ==: 200         ;PARALLEL I/O TEST FAILED
000400          KX$F11 ==: 400         ;DMA TEST FAILED
001000          KX$F12 ==: 1000        ;QIR " "
002000          KX$F13 ==: 2000        ;DPR " "
;
;
; DUAL PORT RAM SYSTEM CONTROL REGISTER 3
;
175006          KW.SC3 ==: 175006       ;KXT DPR REGISTER 3 WORD LOC.
175006          KL.SC3 ==: 175006       ; " " " " LOW BYTE LOC.
175007          KH.SC3 ==: 175007       ; " " " " HIGH BYTE LOC.
;
;
; Data Channel Base addresses (on the KXT side)
;
175010          KW.DC0 ==: 175010       ; CHANNEL 0
175020          KW.DC1 ==: 175020       ; CHANNEL 1
;
;
; Offsets to Data Channel Base address
;
000000          KW.DC0 ==: 0           ; Command word
000002          KW.DST ==: 2           ; Status word
000004          KW.DAT ==: 4           ; beginning of data
;
; Bit definitions within Data Channel Command
;
000036          KC.COM ==: 36          ; Command field
000040          KC.ICC ==: 40          ; Interrupt on command complete
000100          KC.IDA ==: 100         ; Interrupt on DA
000200          KC.IDR ==: 200         ; Interrupt on DR
003400          KC.LEN ==: 3400        ; Length field
004000          KC.EOM ==: 4000        ; End of message

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177400          KC.VEC ==: 177400          ; Vector Number (high byte)
;
; Bit definitions within Data Channel Status
000036          KS.ERC ==: 36             ; Error code
000040          KS.DR  ==: 40             ; Data requested (Write will succeed)
000100          KS.FDM ==: 100            ; End of message
000200          KS.DA  ==: 200            ; Data available (Read will succeed)
003400          KS.ALN ==: 3400           ; Actual length of transfer
020000          KS.DBG ==: 20000          ; Debug available
040000          KS.ON  ==: 40000          ; Interface ready (on)
100000          KS.ERR ==: 100000         ; Error (Cumulative)
;
; Data Channel Command Codes
;
000000          KCSNOP ==: 0.             ; NOP command
000002          KCSRES ==: 2.             ; Reset command
000004          KCSEI  ==: 4.             ; Enable Interrupts command
000006          KCSDI  ==: 6.             ; Disable Interrupts command
000010          KCSGS  ==: 8.             ; Get Status command
000012          KCSSS  ==: 10.            ; Set Status command
000014          KCSRDR ==: 12.            ; Read data command
000016          KCSWD  ==: 14.            ; Write data command
000020          KCSFDR ==: 16.            ; Enable Debug command
000022          KCSDO  ==: 18.            ; Disable Debug command
000022          KCSMAX ==: KCSDO          ; Maximum command code
;
; Data Channel Error Codes
;
000000          KESOK  ==: 0.             ; Success (no)error code
000002          KESNDA ==: 2.             ; No data available (read rejected)
000004          KESNDR ==: 4.             ; No data requested (write rejected)
000006          KESILC ==: 6.             ; Illegal command field
000010          KESILL ==: 8.             ; Illegal length field
000012          KESILV ==: 10.            ; Illegal vector
000014          KESDNA ==: 12.            ; Debug not available
000014          KESMAX ==: KESDNA         ; Maximum error code
;
; .nlist me
;

```

286
287

```
1          .SBTTL NFDEF - Native Firmware definitions
2          .ENABLE LC,GBL
3
4          ;
5          ; Module name: DEF - DEFINITIONS
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ;
17         ; This module defines addresses and bit definitions for various I/O registers
18         ; on the KXT11-CA.
19         ;
```

11

```

1      ;
2      ;
3      ; BIT SYMBOL DEFINITIONS
4      000001      BIT0 == 1
5      000002      BIT1 == 2
6      000004      BIT2 == 4
7      000010      BIT3 == 10
8      000020      BIT4 == 20
9      000040      BIT5 == 40
10     000100      BIT6 == 100
11     000200      BIT7 == 200
12     000400      BIT8 == 400
13     001000      BIT9 == 1000
14     002000      BIT10 == 2000
15     004000      BIT11 == 4000
16     010000      BIT12 == 10000
17     020000      BIT13 == 20000
18     040000      BIT14 == 40000
19     100000      BIT15 == 100000
20     ;
21     ; SLU1 ADDRESS DEFINITIONS
22     ;
23     177560      RCSRIA == 177560
24
25     004000      RCVACB == BIT11
26     000200      RCVDMR == BIT7
27     000100      RCVIEB == BIT6
28
29     177562      RBUF1A == 177562
30
31     100000      ERRB == BIT15
32     040000      ORERRE == BIT14
33     020000      FRERRR == BIT13
34     004000      RCVBKB == BIT11
35
36     177564      XCSRIA == 177564
37
38     000200      XRDYB == BIT7
39     000100      XIEB == BIT6
40     000070      PBRF == BIT5|BIT4|BIT3
41     000004      MAINTB == BIT2
42     000002      PBREB == BIT1
43     000001      XBRKB == BIT0
44
45     177566      XBUF1A == 177566
46
47     ;
48     ; SLU2 Definitions
49     ;
50     175700      SL2SAA == 175700      ;SLU 2 channel A Status register address
51     175710      SL2SBA == 175710      ; " " " B " " "
52     175704      SL2CAA == 175704      ; " " " A Command register "
53     175714      SL2CBA == 175714      ; " " " B " " "
54     ;
55     ; PIO Definitions
56     ;
57     177000      PI0ICA == 177000      ;PIO interrupt control register address

```

```
58          177004          PIOAVA ==      177004          ;PIO Port A interrupt vector register
59          177006          PIOBVA ==      177006          ; " " B " " "
60          177010          PIOTVA ==      177010          ; " Counter timer " " "
61          ;
62          ; DMA Definitions
63          ;
64          174470          DMAMMA ==      174470          ;DMA Master Mode Register
65          174532          DMAOVA ==      174532          ;DMA Channel 0 Interrupt Vector Register
66          174530          DMA1VA ==      174530          ; " " 1 " " "
67          174442          DMA0OA ==      174442          ;DMA Channel 0 Chain Offset Field
68          174446          DMAOSA ==      174446          ; " " " " Segment/Tag Field
69          174454          DMACDA ==      174454          ; " Command Register
70
71          ;
72          ; 8255 Control Register
73          ;
74          177526          C8255 ==      177526
75
```

```
1 .SBTTL SELF TEST OVERLAY 0
2 .LIST ME,MEB,SEQ,LOC,BIN ; NORMAL LISTING MODE
3 .NLIST MC,CND,BEX ; DITTO
4 .FNABL AMA,GBL
5 = 160000
6 ;
7 ; Module name: SELF TEST OVERLAY 0
8 ;
9 ; System: KXT11-CA Native Firmware
10 ;
11 ;
12 ;
13 ;
14 ;
15 ;
16 ; Functional Description:
17 ;
18 ; This module contains overlay 0 of the self test code. The self test
19 ; modules in this overlay are:
20 ;
21 ; I/O register check,
22 ; Native (and user) RAM,
23 ; Native (and user) ROM,
24 ; CPU (a null test),
25 ; Line clock (BEVNT) interrupt,
26 ; Console serial port (DC319), and
27 ; Second serial port (WFC7201).
28 ;
29 ; Overlay 0 physically occupies the first 2 KB of the boot ROM. It
30 ; executes starting at 160000 when the DIAG PROM EN bit, bit 5, in
31 ; KXTCSPA is 0.
32 ;
33 ; RETURNED ERRORS ARE BIT ENCODED IN R0 (TTEEEE)
34 ; WHERE T = TEST NUMBER
35 ; . AND z = 12 DISCRETE ERROR FLAGS.
36 ; . I.E. 010004 = TEST 01, ERROR(BIT) 2.
```



```

1          ; SCRATCH RAM ALLOCATION.
2          ;
3          ; R5 IS ODT'S "TOP-OF-MEM" POINTER, AND IS PRESERVED AS SUCH.
4          ; ALL SCRATCH REFERENCES ARE INDEXED FROM R5 AS FOLLOWS:
5          ;
6          ;
7          ;
8          ;          LO          MID          HI
9          ;          -----          -----          -----
10         000005    $TOP=    &5          ; 077776    137776    157776
11         150002    BUFR1=   -27776          ; 050000    110000    130000    TOP-6KW
12         160002    BUFR2=   -17776          ; 060000    120000    140000    TOP-4KW
13         170002    TMP1=    -07776          ; 070000    130000    150000    TOP-2KW
14         170004    TMP2=    TMP1+2          ;
15         170006    TMP3=    TMP1+4          ;
16         170010    TMP4=    TMP1+6          ;
17         170012    TMP5=    TMP1+10         ;
18         170014    TMP6=    TMP1+12         ;
19         170020    TMP7=    TMP1+14         ;
20         177776    SEF1=    -2              ; LAST 2 WORDS OF NATIVE RAM (BATTERY-BACK-FLAGS)...
21         000005    SEF=     $TOP            ; ...ARE UTILIZED AS OUR ERROR FLAGS.
22         ;
23         ; MISCELLANEOUS STUFF,
24         ;
25         000000    $TN=     0                ; INIT TEST NUMBER SEQUENCE.
26         ;
27         ; A FEW MACROS.
28         ;
29         .MACRO BEGIN NAME,TAG,V1,V2,V3
30             .NLIST
31             $TN=$TN+1                ;; SET TEST NUMBER...
32             $FN=0                    ;;...AND RESET ERROR NUMBER.
33             .LIST
34             .IRP    N,\$TN
35             .SBTTL - T`N NAME
36             ;;*****
37             ;;* TEST N -- NAME
38             ;;*****
39             TST`N:
40             TAG:
41             .ENDR
42             .IF NB <V1>
43                 MOV     V1,-(SP)        ;; SAVE "V1".
44                 MOV     V1+2,-(SP)
45             .IF NB <V2>
46                 MOV     V2,-(SP)        ;; SAVE "V2".
47                 MOV     V2+2,-(SP)
48             .IF NB <V3>
49                 MOV     V3,-(SP)        ;; SAVE "V3".
50                 MOV     V3+2,-(SP)
51             .ENDC
52             .ENDC
53             .ENDC
54             CLR     ($EF)                ;; CLEAR ERROR FLAG.
55             .ENOM BEGIN
56         .MACRO EXIT    V1,V2,V3,?TAG
57

```

> SCRATCH REGISTERS...
 ...AND STACK SPACE.

14

```

58      .IF NB <V1>
59          MOV     (SP)+,V1+2    ;; RESTORE "V1".
60          MOV     (SP)+,V1
61      .IF NB <V2>
62          MOV     (SP)+,V2+2    ;; RESTORE "V2".
63          MOV     (SP)+,V2
64      .IF NB <V3>
65          MOV     (SP)+,V3+2    ;; RESTORE "V3".
66          MOV     (SP)+,V3
67      .ENDC
68      .ENDC
69      .ENDC
70          MOV     (SEF),R0      ;; ERROR BITS => R0<11:00>...
71          BFC     TAG          ;;...AND SKIP IF NONE.
72          .IRP    TN,\STN
73          JIS     #<TN*BIT12>,R0 ;; ELSE, ADD TEST NUM => R0<15:12>...
74          .ENDR
75      TAG:      RETURN         ;;...AND RETURN (NZ).
76          .ENDM    EXIT
77
78      .MACRO    ERROR    TEXT
79          .NLIST  ME
80          .RADIX 10
81          .IRP    N,\SEN
82          BIS     #BIT"N,($FF)  ;; E"N = "TEXT
83          .FNDR
84          SEN=$EN+1
85          .RADIX 8
86          .NLIST
87          .LIST   MF
88          .LIST
89          .ENDM    ERROR
90
91      .MACRO    LRESET
92          SOB    R0,,
93          RESET R0,,          ;; LOCAL RESET.
94          SOB    R0,,
95          .ENDM    LRESET
96
97          .NLIST MD
98

```

```

1          ; A FEW DFFINITIONS
2          ;
3          ; STANDARD STUFF.
4          ;
5          000000      PRO=      000          ; THE PRIORITIES.
6          000040      PR1=      040
7          000100      PR2=      100
8          000140      PR3=      140
9          000200      PR4=      200
10         000240      PR5=      240
11         000300      PR6=      300
12         000340      PR7=      340
13         ;
14         ; PRIMARY CONTROL REGISTERS.
15         ;
16         177560      $SSL1= 177560          ; DEC DC319 (DLART) ASYNC SERIAL PORT.
17         175700      $SSL2= 175700          ; NEC7201 SYNC/ASYNC SERIAL PORT.
18         175720      $I8254= 175720         ; I8254 PROGRAMMABLE BAUD GEN FOR ABOVE.
19         177000      $PIO= 177000          ; Z8036 PIO/PIT.
20         174400      $DMA= 174400          ; AMZ8016 DMA CONTROLLER.
21         177520      $CSRA= 177520         ; \
22         177522      $CSRB= 177522         ; > SECONDARY CSR'S...
23         177524      $CSRC= 177524         ; / ...EMBEDDED IN I8255 CHIP.
24         177526      $CSRCON= 177526       ;
25         177530      $CSR= 177530          ; PRIMARY CSR.
26         177532      $QIR= 177532          ; Q-BUS INTERRUPT REGISTER.
27         175000      $DPR= 175000          ; DUAL-PORT RAM (LOCAL).
28         160000      $QDPR1= 160000        ; DUAL-PORT RAM (GLOBAL BASE ID 0-7...
29         175400      $QDPR2= 175400        ; ...AND ID 8-F).
30         ;
31         175000      $IPV= $DPR            ; IPV INTERRUPTS (VIA DPR WORDS 0, 4, 8, AND 12).
32         177524      $LEDS= $CSRC         ; CSRC<3:0> DRIVE THE LEDS.
33         177524      $UID= $CSRC          ; CSRC<7:4> SHOW THE ID SWITCH SETTING.

```

1		; DEFAULT VECTORS.		
2		;		
3	000024	PWRV= 024	; PWR-UP (BRESET)	(NON-MASKABLE).
4	000060	SL1RV= 060	; CONSOLE (SLU1) RCVR	(PRI 4).
5	000064	SL1XV= 064	; CONSOLE (SLU1) XMTR	(PRI 4).
6	000070	NECV= 070	; SYNC/ASYNC BOTH CHANS	(PRI 4).
7	000100	BEVNT= 100	; LINE CLOCK	(PRI 6).
8	000104	PEVNT= 104	; PROGRAMMABLE CLOCK(S)	(PRI 6).
9		; 110	; OPEN	
10	000114	POTV= 114	; MEMORY PARITY	(PRI 7).
11	000120	DPRV4= 120	; DUAL-PORT RAM WORD 4	(PRI 5).
12	000124	DPRV8= 124	; DUAL-PORT RAM WORD 8	(PRI 5).
13	000130	BIACKV= 130	; Q-BUS "IACK"	(PRI 5).
14	000134	DPRV12= 134	; DUAL-PORT-RAM WORD 12	(PRI 5).
15		; 140	; RESERVED (FALCON).	
16	000144	QIRV= 144	; Q-BUS REQUEST	(ARBITER EXECUTES RTI).
17	000150	QIRV1= 150	; DITTO	(ARBITER EXECUTES RESET,RTI)
18	000154	PIOAV= 154	; PIO PORT A	(PRI 4).
19	000160	PIOBV= 160	; PIO PORT B	(PRI 4).
20	000164	DMAV= 164	; DMA (BOTH CHANNELS)	(PRI 4).

```
1          ; LOW SEGMENT ENTRY BLOCK
2          ;
3          ; CALL: BIC #BITS,CSRA ; ENABLE LO SEGMENT.
4          ; CALL TN          ; CALL TEST 0-7.
5          ; BEQ OK          ; OR BNE ERROR.
6          ;
14         T0==. CLR R0          ;SINCF THERE IS NO TEST BY THIS NAME, SHOW NO ERRORS.
          RETURN
          T1==. JMP TST1          ;; EXECUTE TEST 1.
          T2==. JMP TST2          ;; EXECUTE TEST 2.
          T3==. JMP TST3          ;; EXECUTE TEST 3.
          T4==. JMP TST4          ;; EXECUTE TEST 4.
          T5==. JMP TST5          ;; EXECUTE TEST 5.
          T6==. JMP TST6          ;; EXECUTE TEST 6.
          T7==. JMP TST7          ;; EXECUTE TEST 7.

160000 005000
160002 000207
          160004
160004 000137 160040
          160010
160010 000137 160272
          160014
160014 000137 160700
          160020
160020 000137 161150
          160024
160024 000137 161164
          160030
160030 000137 161344
          160034
160034 000137 161730
```

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```

1          .SBTTL - T1    I/O REGISTER CHECK
          ;;*****
          ;;* TEST 1 -- I/O REGISTER CHECK
          ;;*****
          TST1:
          TIOR:
          CLR      (SEF)          ;; CLEAR ERROR FLAG.
2          ;
3          ; INPUT: NONE.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; VERIFY THAT ALL ASSIGNED I/O ADDRESSES ARE VALID.
7          ;
8          ;
9          ; T1    I/O REGISTER CHECK
10         ;      E0 = BUS-ERROR AT CSR ADDRESS
11         ;      E1 = BUS-ERROR AT QIR ADDRESS
12         ;      E2 = BUS-ERROR AT DPR ADDRESS
13         ;      E3 = BUS-ERROR AT DC319 ADDRESS
14         ;      E4 = BUS-ERROR AT NEC7201 ADDRESS
15         ;      E5 = BUS-ERROR AT I8254 ADDRESS
16         ;      E6 = BUS-ERROR AT Z8036 ADDRESS
17         ;      E7 = BUS-ERROR AT Z8016 ADDRESS
18 160042 012700 177520 1S:  MOV  #SCSR,R0      ; THE CSR SET...
19 160046 012701 000005  MOV  #5,,R1      ;...5 REGISTERS.
20 160052 004737 160254  CALL 10$
21 160056 052715 000001  BIS  #BIT0,(SEF)  ;; E0 = BUS-ERROR AT CSR ADDRESS
22
23 160062 012700 177532 2S:  MOV  #SQIR,R0      ; THE QIR...
24 160066 012701 000001  MOV  #1,R1      ;...ONE-OF-A-KIND.
25 160072 004737 160254  CALL 10$
26 160076 052715 000002  BIS  #BIT1,(SEF)  ;; E1 = BUS-ERROR AT QIR ADDRESS
27
28 160102 012700 175000 3S:  MOV  #SDPR,R0      ; THE 2-PORT-RAM...
29 160106 012701 000020  MOV  #16,,R1    ;...16 REGISTERS.
30 160112 004737 160254  CALL 10$
31 160116 052715 000004  BIS  #BIT2,(SEF)  ;; E2 = BUS-ERROR AT DPR ADDRESS
32
33 160122 012700 177560 4S:  MOV  #SSL1,R0     ; THE CONSOLE PORT...
34 160126 012701 000004  MOV  #4,,R1     ;...4 REGISTERS.
35 160132 004737 160254  CALL 10$
36 160136 052715 000010  BIS  #BIT3,(SEF)  ;; E3 = BUS-ERROR AT DC319 ADDRESS
37
38 160142 012700 175700 5S:  MOV  #SSL2,R0     ; THE SYNC/ASYNCR PORT...
39 160146 012701 000010  MOV  #8,,R1     ;...8 REGISTERS...
40 160152 004737 160254  CALL 10$
41 160156 052715 000020  BIS  #BIT4,(SEF)  ;; E4 = BUS-ERROR AT NEC7201 ADDRESS
42
43 160162 012700 175720 6S:  MOV  #I8254,R0    ;...AND ITS CLOCK GENERATOR...
44 160166 012701 000010  MOV  #9,,R1     ;...HAS 8 MORE.
45 160172 004737 160254  CALL 10$
46 160176 052715 000040  BIS  #BIT5,(SEF)  ;; F5 = BUS-ERROR AT I8254 ADDRESS
47
48 160202 012700 177000 7S:  MOV  #SPIO,R0     ; THE PARALLEL I/O PORT...
49 160206 012701 000060  MOV  #48,,P1    ;...A WHOPPING 48 REGISTERS.
50 160212 004737 160254  CALL 10$
51 160216 052715 000100  BIS  #BIT6,(SEF)  ;; F6 = BUS-ERROR AT Z8036 ADDRESS
  
```

```

52
53 160222 012700 174400      8$:  MOV    #SDMA,R0      ; THE DMA ENGINE...
54 160226 012701 000056      MOV    #46.,R1        ;...A CLOSE SECOND WITH 46.
55 160232 004737 160254      CALL   10$
56 160236 052715 000200      BIS    #BIT7,(SEF)    ;; E7 = BUS-ERROR AT Z8016 ADDRESS
57 160242
   160242 011500
   160244 001402
   160246 052700 010000      9$:  MOV    (SEF),R0    ;; ERROR BITS => R0<11:00>...
   160252 000207      BEQ    30000$        ;;...AND SKIP IF NONE.
   30000$: RETURN      BIS    #<1*BIT12>,R0 ;; ELSE, ADD TEST NUM => R0<15:12>...
   ;;...AND RETURN (WZ).
58
59 160254 005720      10$:  TST    (R0)+      ; TEST AN ADDRESS.
60 160256 000240      NOP
61 160260 103403      BCS    11$          ; TAKE ERROR RETURN IF IT TRAPPED.
62 160262 077104      SOB    R1,10$
63 160264 062716 000004      ADD    #4,(SP)     ; ALL OK, TAKE SKIP RETURN.
64 160270 000207      11$:  RETURN
  
```

```

1          .SETTL - T2  NATIVE (AND USER) RAM
          ;;*****
          ;;* TEST 2 -- NATIVE (AND USER) RAM
          ;;*****
          TST2:
          TRAM:
          CLR      (SEF)          ;; CLEAR ERROR FLAG.
2          ;
3          ; INPUT: R1 = NONE.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; TEST LOCAL RAM FROM BOTTOM UP (NON-DESTRUCTIVE).
7          ; IF SOCKFT "A" CONTAINS USER RAM, TEST IT AS WELL.
8          ;
9          ; 1. WRITE (DATO) EACH LOCATION WITH IT'S OWN ADDRESS.
10         ; 2. READ (DATI) AND VERIFY CORRECT DATA.
11        ; 3. COMPLIMENT WORD (DATIO) AND VERIFY.
12        ; 4. COMPLIMENT LO AND HI BYTES (DATIO(B)) AND VERIFY.
13        ;
14        ;
15        ; T2  NATIVE (AND USER) RAM
16        ; .   E0 = BUS-ERROR AT RAM ADDRESS
17        ; .   E1 = WRITE-READ ERROR
18        ; .   E2 = READ-MOD-WRITE ERROR
19        ; .   E3 = READ-MOD-WRITE(LB) ERROR
20        ; .   E4 = READ-MOD-WRITE(HB) ERROR
21        ; .   E5 TO E9 = SAME AS E0 TO E4 IN USER RAM SPACE
22 160274 020527 137776      CMP      STOP,#137776
23 160300 101007             BHI      MEM3          ; BP IF RAM IS IN HIGH...
24 160302 001403             BEQ      MEM2          ;...OR MID RANGE.
25 160304 012702 000000     MEM1:  MOV      #0,R2          ; SET BOTTOM AT 0.
26 160310 000405             BR       MEM3A
27 160312 012702 040000     MEM2:  MOV      #4000,R2        ; SET BOTTOM AT 8K.
28 160316 000402             BR       MEM3A
29 160320 012702 100000     MEM3:  MOV      #10000,R2       ; SET BOTTOM AT 16K.
30 160324 010504             MEM3A: MOV      $TOP,R4          ; SET TOP.
31 160326 005046             CLR      -(SP)          ; CLEAR NATIVE/USER SWITCH.
32 160330 000241             1$:    CLC
33 160332 011200             MOV      (R2),R0        ; SAVE TARGET DATA.
34 160334 000240             NOP
35 160336 103003             BCC     2$
36 160340 052715 000001     2$:    BIS      #BIT0,(SEF)    ;; E0 = BUS-ERROR AT RAM ADDRESS
37 160344 000444             BR       7$
38
39 160346 010201             2$:    MOV      R2,R1          ; TARGET ADDRESS => R1.
40 160350 010211             MOV      R2,(R1)        ; WRITE (DATO)...
41 160352 011103             MOV      (R1),R3        ;...READ (DATI)...
42 160354 020203             CMP      R2,R3          ;...AND CHECK.
43 160356 001402             BFC     3$
44 160360 052715 000002     3$:    BIS      #BIT1,(SEF)    ;; E1 = WRITE-READ ERROR
45 160364 005102             COM     R2
46 160366 005111             COM     (R1)          ; READ-MOD-WRITE (DATIO)...
47 160370 021102             CMP     (R1),R2        ;...READ AND CHECK.
48 160372 001402             BEQ     4$
49 160374 052715 000004     4$:    BIS      #BIT2,(SEF)    ;; E2 = READ-MOD-WRITE ERROR
50 160400 005102             COM     R2
51 160402 105111             COMB   (R1)          ; READ-MOD-WRITE-LB (DATIO(LB))...

```



```

52 160404 121102          CMPB   (R1),R2      ;...READ AND CHECK.
53 160406 001402          BFQ    5$          ;
54 160410 052715 000010  5$:    BIS    #BIT3,(SEF) ;; E3 = READ-MOD-WRITE(LB) ERROR
55 160414 000302          SWAB   R2          ;
56 160416 105161 000001  5$:    COMB   1(R1)    ; READ-MOD-WRITE-HB (DATIO(HB))...
57 160422 126102 000001  5$:    CMPB   1(R1),R2   ;...READ AND CHECK.
58 160426 001402          BFQ    6$          ;
59 160430 052715 000020  5$:    BIS    #PIT4,(SEF) ;; E4 = READ-MOD-WRITE(HB) ERROR
60
61 160434 000302          SWAB   R2          ;
62 160436 010022          MOV    R0,(R2)+    ; RESTORE AND BUMP TARGET ADDRESS.
63 160440 020227 160330  65$:   CMP    R2,#1$     ; *****
64 160444 001002          BNF   65$         ; *** IF RUNNING IN RAM, DON'T TEST THE "TEST".
65 160446 012702 160456  65$:   MOV    #7$,R2     ; *****
66 160452 020204          CMP    R2,R4      ; REACHED TOP ??
67 160454 101725          BLOS  1$          ; LOOP IF NOT.
68
69 160456 005116          COM    (SP)       ; TOGGLE NATIVE/USER SWITCH...
70 160460 001416          BFQ    8$         ;...AND EXIT IF BOTH DONE.
71 160462 011565 177776  7$:    MOV    (SEF),-2(SEF) ; SAVE NATIVE ERRORS...
72 160466 005015          CLR   (SEF)      ;...AND CLEAR FOR 2ND PASS.
73 160470 004737 160546  7$:    CALL  SKTA      ; GET SOCKET SPECS.
74 160474 020227 000003  7$:    CMP    P2,#3     ; CHECK WHAT'S THERE...
75 160500 001406          BFQ    8$         ;...AND BR IF ROM (OR EMPTY).
76 160502 010002          MOV    R0,R2     ; IT'S RAM, 1ST ADDRESS => R2...
77 160504 010104          MOV    R1,R4     ;...AND SIZE => R4.
78 160506 005304          DEC   R4         ; \
79 160510 006304          ASL   R4         ; > CHANGE SIZE TO LAST ADDRESS...
80 160512 060204          ADD   R2,R4     ; /
81 160514 000705          BR    1$        ;...AND GO 'ROUND ONCE MORE.
82
83 ;
84 ;
85 160516 005726          8$:    TST   (SP)+     ; DONE, POP THE STACK.
86 160520 012700 000005  8$:    MOV    #5,R0     ;
87 160524 006315          9$:    ASL   (SEF)    ; SHIFT USER ERRORS TO BITS<9:5>...
88 160526 077002          SOB   R0,9$     ;
89 160530 056515 177776  9$:    BIS    -2(SEF),(SEF) ;...AND ADD NATIVE ERRORS IN BITS<4:0>.
90 160534 011500          MOV    (SEF),R0  ;; ERROR BITS => R0<11:00>...
    160536 001402          BEQ   30001$    ;;...AND SKIP IF NONE.
    160540 052700 020000  30001$: BIS    #<2*BIT12>,R0 ;; ELSE, ADD TEST NUM => R0<15:12>...
    160544 000207          30001$: RETURN ;;...AND RETURN (NZ).

```

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```

1
2 ; SUBROUTINE TO DETERMINE USER (SOCKET A) ADDRESS AND SIZE.
3 ;
4 ; RETURN R0 = 1ST ADDRESS
5 ; R1 = SIZE (WORDS)
6 ; R2 = 3 IF ROM (OR EMPTY).
7 ;
8 160546 012700 100000 SKTA: MOV #100000,R0 ; ASSUME ROM OVER RAM.
9 160552 005705 TST $STOP
10 160554 100001 bPL 1$ ; BR IF SO...
11 160556 005000 CLR R0 ;...ELSE, SET ROM AT 0.
12 160560 012701 004000 1S: MOV #2048.,R1 ; START SIZING AT 2KW.
13 160564 032737 000006 177522 BIT #<3*BIT1>,$CSRB
14 160572 001417 bFQ 2$ ; BR IF 2KW SELECTED (MAP 0 OR 4).
15 160574 006301 ASL R1 ; RAISE TO 4KW.
16 160576 032737 000004 177522 BIT #<2*BIT1>,$CSRB
17 160604 001412 bFQ 2$ ; BR IF 4KW SELECTED (MAP 1 OR 5).
18 160606 006301 ASL R1 ; RAISE TO 8KW.
19 160610 032737 000010 177522 BIT #<4*BIT1>,$CSRB
20 160616 001405 bFQ 2$ ; BR IF 8KW SELECTED (MAP 2 OR 3).
21 160620 032737 000002 177522 BIT #<1*BIT1>,$CSRB
22 160626 001401 bFQ 2$ ; DITTO (MAP 6).
23 160630 006301 ASL R1 ; RAISE TO 16KW (MAP 7).
24 160632 000401 2S: BR RAMLOA ; EXIT THRU ROM/RAM CHECKER.
25 ;
26 ; SUBROUTINE TO ESTABLISH ROM OR RAM IN VECTOR SPACE.
27 ;
28 ; RETURN R2<00> = 1 IF LO BYTE NON-WRITABLE.
29 ; R2<01> = 1 IF HI BYTE NON-WRITABLE.
30 ;
31 160634 005000 RAMLO: CLR R0
32 160636 005002 RAMLOA: CLR R2
33 160640 011046 MOV (R0),-(SP) ; GET TARGET LOCATION...
34 160642 005116 COM (SP) ;...AND COMPLEMENT IT.
35 160644 005110 COM (R0) ; COMPLEMENT TARGET LOCATION.
36 160646 126066 000001 000001 CMPB 1(R0),1(SP) ; HI PYTE WRITABLE ??
37 160654 001402 bFQ 1$ ; YES
38 160656 052702 000002 BIS #BIT1,R2 ; NO
39 160662 121026 1S: CMPB (R0),(SP)+ ; LO BYTE WRITABLE ??
40 160664 001402 bFQ 2$ ; YES
41 160666 052702 000001 BIS #BIT0,R2 ; NO
42 160672 005110 2S: COM (R0) ; RESTORE TARGET LOCATION.
43 160674 005702 TST R2 ; SET CONDITION FOR CALLER.
44 160676 000207 RETURN

```

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```

1          .SBTTL - T3 NATIVE (AND USER) ROM
          ;;*****
          ;;* TEST 3 -- NATIVE (AND USER) ROM
          ;;*****
          TST3:
          TROM:
          CLR      ($EF)          ;; CLFAR ERROR FLAG.
2          ;
3          ; INPUT: R1<91T0> = INCLUDE USER ROM.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; CHECK SUM BOOT/SELF-TEST ROM (SOCKET B).
7          ; IF SELECTED, DO THE USER ROM (SOCKET A) AS WELL.
8          ;
9          ; T3 NATIVE (AND USER) ROM
10         ; . E0 = LO BYTE CHECK SUM ERROR (NATIVE)
11         ; . E1 = HI BYTE CHECK SUM ERROR (NATIVE)
12         ; . E2 = LO BYTE CHECK SUM ERROR (USER)
13         ; . E3 = HI BYTE CHECK SUM ERROR (USER)
14
15 160702 010104          MOV      R1,R4          ; SAVE OPTION FLAG.
16 160704 012700 161150  MOV      #ACC+2,R0
17 160710 012701 000943  MOV      #<ACC+2-CKSUM>/2,R1
18 160714 014046 15:    MOV      -(R0),-(SP)  ; PUSH CHECK-SUM CODE ONTO THE STACK.
19 160716 077102          SOB      R1,1$
20
21 160720 012700 160000  MOV      #160000,R0
22 160724 012701 010000  MOV      #4096.,R1
23 160730 004766 000000  CALL     0(SP)          ; CHECK SUM (LO BYTE).
24 160734 052715 000001  BIS      #BIT0,($EF)   ;; E0 = LO BYTE CHECK SUM ERROR (NATIVE)
25
26 160740 012700 160001  25:    MOV      #160001,R0
27 160744 012701 010000  MOV      #4096.,R1
28 160750 004766 000000  CALL     0(SP)          ; CHECK SUM (HI BYTE).
29 160754 052715 000002  BIS      #BIT1,($EF)   ;; E1 = HI BYTE CHECK SUM ERROR (NATIVE)
30 160760          35:    ;
31          ; IF ERROR, CHECK FOR OVERLAY PROBLEM ??
32          ;
33 160760 032704 000001  45:    BIT      #BIT0,R4      ; USER ROM SELECTED ??
34 160764 001417          BEQ      6$            ; EXIT IF NOT.
35 160766 004737 160546  CALL     SKTA          ; YES, GET SOCKET SPECS.
36 160772 010046          MOV      R0,-(SP)     ; PUSH START ADDRESS...
37 160774 010146          MOV      R1,-(SP)     ; ...AND SIZE.
38 160776 004766 000004  CALL     4(SP)         ; CHECK SUM (LO BYTE).
39 161002 052715 000004  BIS      #BIT2,($EF)   ;; E2 = LO BYTE CHECK SUM ERROR (USER)
40
41 161006 012601 55:    MOV      (SP)+,R1      ; POP SIZE...
42 161010 012600          MOV      (SP)+,R0     ; ...AND ADDRESS.
43 161012 005200          INC      R0
44 161014 004766 000000  CALL     0(SP)         ; CHECK SUM (HI BYTE).
45 161020 052715 000010  BIS      #BIT3,($EF)   ;; E3 = HI BYTE CHECK SUM ERROR (USER)
46
47 161024 062706 000106  65:    ADD      #ACC+2-CKSUM,SP ; FIX STACK.
48 161030 011500          MOV      ($EF),R0     ;; ERROR BITS => R0<11:00>...
      161032 001402          BEQ      30002$       ;; ...AND SKIP IF NONE.
      161034 052700 030000  BIS      #<3*BIT12>,R0 ;; ELSE, ADD TEST NUM => R0<15:12>...
      161040 000207          30002$: RETURN      ;; ...AND RETURN (NZ).

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1          ;*****
2          ; ROM CHECK SUM ROUTINE.
3          ; THIS STUFF IS COPIED TO AND EXECUTED IN STACK SPACE.
4          ;
5          .DSABL AMA      ; RELATIVE PIC.
6          ;
7          ; ON ENTRY, R0 = STAPT ADDRESS AND R1 = BYTE COUNT.
8          ; ON RETURN, R2 = ACCUMULATED SUM AND R3 = CHECK-SUM.
9          ;
10         161042 005067 000100      CKSUM: CLR     ACC          ; CLEAR ACCUMULATOR...
11         161046 005301              DEC     R1           ;...AND DECR THE BYTE COUNT.
12         161050 111002      1S:    MOVW  (R0),R2       ; 1ST/NEXT ROM LOCATION.
13         161052 042702 177400      BIC     #^C377,R2
14         161056 060267 000064      ADD     R2,ACC          ; \
15         161062 106367 000060      ASLB  ACC           ; > ACCUMULATE BYTE SUM.
16         161066 005567 000054      ADC     ACC           ; /
17         161072 062700 000002      ADD     #2,R0
18         161076 020027 174000      CMP    R0,#174000    ; END OF NATIVE ROM ??
19         161102 103405              BLO    2S           ; BR IF NOT.
20         161104 052737 000040 177520  BIC     #BITS,@#SCSPA ; YES, MAP IN THE OVERLAY...
21         161112 042700 017776      BIC     #^C160001,R0 ;...AND ADJUST SRC POINTER.
22         161116 077124              SOB    R1,1S       ; LOOP 'TIL DONE.
23         161120 116702 000022      MOVW  ACC,R2        ; THEN PUT ACCUMULATED SUM IN R2...
24         161124 111003              MOVW  (R0),R3       ;...AND THE CHECK-SUM IN R3.
25         161126 042737 000040 177520  BIC     #BITS,@#SCSRA ; UNMAP OVERLAY.
26         161134 120203              CMPB  R2,R3         ; ACCUMULATED SUM SHOULD EQUAL CHECK-SUM.
27         161136 001002              HNE   3S           ; ERROR RETURN IF NOT.
28         161140 062716 000004      ADD     #4,(SP)     ; SKIP RETURN IF SO.
29         161144 000207      3S:    RETURN
30         161146 000000      ACC:    0
31          .ENABL AMA
32          ;*****

```

```
1          .Sbttl - T4    T11 CPU INSTRUCTIONS AND TRAPS
          ;;*****
          ;;* TEST 4 -- T11 CPU INSTRUCTIONS AND TRAPS
          ;;*****
          TST4:
          TCPU:
          CLR      ($EF)          ;; CLEAR ERROR FLAG.
2          ;
3          ; INPUT: NONE.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; TEST THE CPU (WHATEVER THAT MEANS) !!
7          ;
8          T4      T11 CPU INSTRUCTIONS AND TRAPS
9          .      NOT INSTALLED.
10
11 161152 011500      MOV      ($EF),R0          ;; ERROR BITS => R0<11:00>...
    161154 001402      BEQ      30003$          ;;...AND SKIP IF NONE.
    161156 052700 040000  BIS      #<4*BIT12>,R0      ;; ELSE, ADD TEST NUM => R0<15:12>...
    161162 000207      30003$: RETURN          ;;...AND RETURN (NZ).
```

27

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1          .SETTL - T5   LINE CLOCK (BEVNT) INTERRUPT
          ;*****
          ;* TEST 5 -- LINE CLOCK (BEVNT) INTERRUPT
          ;*****
          TST5:
          TCLK:
          MOV     BEVNT,-(SP)    ;; SAVE BEVNT.
          MOV     BEVNT+2,-(SP)
          CLR     ($EF)        ;; CLEAR ERROR FLAG.

2          ;
3          ; INPUT: NONE.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; LINE CLOCK IS JUMPERED FROM CONSOLE DC319 OR Q-BUS BEVNT.
7          ; VERIFY THAT WE CAN ENABLE/DISABLE THE CLOCK VIA CSRA<6>,
8          ; AND THAT IT INTERRUPTS THRU VECTOR 100 AT PRI 6.
9          ;
10         ;
11         ; T5   LINE CLOCK (BEVNT) INTERRUPT
12         ; .   E0 = ROM IN VECTOR SPACE -- CAN'T RUN
13         ; .   E1 = CLOCK INTERRUPT NOT MASKED AT LEVEL 6
14         ; .   E2 = CLOCK DOESN'T INTERRUPT
15         ; .   E3 = CAN'T SHUT IT OFF
16 161176 004737 160634          CALL  RAMLO ,      ; VECTOR SPACE USABLE ??
17 161202 001405                BEQ     25          ; PROCEED IF SO.
18 161204 052715 000001          BIS     #BIT0,($EF)  ;; P0 = ROM IN VECTOR SPACE -- CAN'T RUN
19 161210 000444                BR     TCXIT
20          ;
21 161212 005201          15:   INC     R1          ; ON "BEVNT", TICK AND RETURN.
22 161214 000002          RTI
23          ;
24 161216 106427 000300          25:   MTPS   #PR6          ; RAISE CPU.
25 161222 012737 161212 000100  MOV     #1$,BEVNT    ; SET CLOCK VECTOR.
26 161230 012737 000300 000102  MOV     #PR6,BEVNT+2
27 161236 005000                CLR     R0          ; CLEAR LOOP CONTROL...
28 161240 005001                CLR     R1          ; ...AND TICKER.
29 161242 052737 000100 177520  BIS     #BIT6,$CSRA  ; TURN ON CLOCK INTERRUPT.
30 161250 077001                SOB     R0,,         ; DELAY, INTERRUPT SHOULD...
31 161252 005701                TST     R1          ; ...BE MASKED AT THIS LEVEL.
32 161254 001402                BEQ     35          ; BR IF SO.
33 161256 052715 000002          BIS     #BIT1,($EF)  ;; E1 = CLOCK INTERRUPT NOT MASKED AT LEVEL 6
34 161262 106427 000240          35:   MTPS   #PR5          ; NOW, LOWER CPU TO PRI 5.
35 161266 077001                SOB     R0,,         ; DELAY AGAIN, CLOCK SHOULD COME IN...
36 161270 005301                DEC     R1          ; ...AND GIVE US A FEW TICKS (MORE THEN 1).
37 161272 003002                BGT     45          ; BR IF SO.
38 161274 052715 000004          BIS     #BIT2,($EF)  ;; E2 = CLOCK DOESN'T INTERRUPT
39          ;
40 161300 005037 177520          45:   CLR     $CSPA    ; TURN IT OFF.
41 161304 000240                NOP
42 161306 005001                CLR     R1          ; ...FOR HARDWARE LOGIC PUPOSE...
43 161310 077001                SOB     R0,,         ; DELAY ONCE MORE...
44 161312 005701                TST     R1          ; ...CLOCK SHOULD BE SHUT OFF.
45 161314 001402                BEQ     65          ; BR IF SO.
46 161316 052715 000010          BIS     #BIT3,($EF)  ;; E3 = CAN'T SHUT IT OFF
47 161322
48 161322 012637 000102          65:TCXIT:  MOV     (SP)+,BEVNT+2  ;; RESTORE BEVNT.
          161326 012637 000100          MOV     (SP)+,BEVNT
  
```

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161332 011500          MOV    ($EP),R0      ;; ERROR BITS => R0<11:00>...
161334 001402          BEQ    30004$        ;;...AND SKIP IF NONE.
161336 052700 050000   BIS    #<5*BIT12>,R0  ;; ELSE, ADD TEST NUM => R0<15:12>...
161342 000207          30004$: RETURN  ;;...AND RETURN (NZ).
```

29

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1          .SETTL - T6      CONSOLE SERIAL PORT DC319
          ;;*****
          ;;* TEST 6 -- CONSOLE SERIAL PORT DC319
          ;;*****
          TST6:
          TDC:
          MOV     SL1XV,-(SP)      ;; SAVE SL1XV.
          MOV     SL1XV+2,-(SP)
          MOV     SL1RV,-(SP)     ;; SAVE SL1RV.
          MOV     SL1RV+2,-(SP)
          CLR     (SEF)           ;; CLEAR ERROR FLAG.

2          ;
3          ; INPUT: NONE.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; *** REQUIRES EXTERNAL LOOP-BACK ***
7          ;
8          ; TEST THAT THE CONSOLE PORT WORKS AS ADVERTISED.
9          ;
10         ; T6      CONSOLE SERIAL PORT DC319
11         ; .      E0 = ROM IN VECTOR SPACE -- INTERRUPTS NOT TESTED
12         ; .      E1 = XMTR INTERRUPT NOT MASKED AT LEVEL 4
13         ; .      E2 = XMTR INTERRUPT NOT RECEIVED
14         ; .      E3 = RCVR INTERRUPT NOT MASKED AT LEVEL 4
15         ; .      E4 = RCVR INTERRUPT NOT RECEIVED
16         ; .      E5 = RECEIVED DATA INCORRECT
17         ; .      E6 = NO RCVR DONE, LOOP-BACK OPEN
18
19 161366 012704 177560          MOV     #SSL1,R4      ; POINTER => R4.
20 161372 004737 160634          CALL    RAMLO        ; VECTOR SPACE USABLE ??
21 161376 001403                BEQ     DC.XMT       ; PROCEED IF SO.
22 161400 052715 000001          BIS     #BIT0,(SEF)  ;; E0 = ROM IN VECTOR SPACE -- INTERRUPTS NOT TESTED
23 161404 000503                BR      DC.DAT
24
25 161406 106427 000200          DC.XMT: MTPS     #PR4      ; RAISE CPU TO XMTR LEVEL.
26 161412 012737 161440 000064  MOV     #2S,SL1XV    ; SET VECTOR.
27 161420 012737 000200 000066  MOV     #PR4,SL1XV+2
28 161426 052764 000100 000004  BIS     #100,4(R4)   ; SET INTERRUPT ENABLE.
29 161434 000240                NOP
30 161436 000403                BR      3$
31 161440                2$:
32 161440 052715 000002          BIS     #BIT1,(SEF)  ;; E1 = XMTR INTERRUPT NOT MASKED AT LEVEL 4
33 161444 000411                BR      4$
34 161446 012737 161470 000064  3$:  MOV     #4$,SL1XV    ; CHANGE THE VECTOR.
35 161454 106427 000000          MTPS     #PRO        ; LOWER CPU PRIORITY.
36 161460 000240                NOP                ; INTERRUPT SHOULD HAVE COME IN.
37 161462 052715 000004          BIS     #BIT2,(SEF)  ;; E2 = XMTR INTERRUPT NOT RECEIVED
38 161466 000401                BR      5$
39 161470 022626                4$:  CMP     (SP)+,(SP)+  ; ON INTERRUPT, FIX STACK.
40 161472 042764 000100 000004  5$:  BIC     #100,4(R4)   ; CLEAR THE INT ENABLE.
41 161500 016400 000002          DC.RCV: MOV     2(R4),R0  ; ENSURE RCVR DONE IS CLEAR.
42 161504 106427 000200          MTPS     #PR4        ; RAISE CPU LEVEL.
43 161510 005000                CLR     R0
44 161512 110064 000006          MOV     R0,6(R4)    ;...TRANSMIT A NULL CHARACTER...
45 161516 105714                1$:  TSTR    (P4)        ;...WAIT 'TIL RCVR GETS IT...
46 161520 100402                BMI     2$
  
```



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47 161522 077003 SOB R0,1$ ;...(BUT DON'T WAIT FOREVER).
48 161524 000462 BR DC.LBO
49
50 161526 012737 161552 000060 2$: MOV #3$,SL1RV ; OK, SET RCVR VECTOR.
51 161534 012737 000200 000062 MOV #PR4,SL1RV+2
52 161542 052714 00010C BIS #100,(R4) ; SET RCVR INTERRUPT ENABLE.
53 161546 000240 NOP ; INTERRUPT SHOULD BE HELD OFF...
54 161550 000403 BR 4$ ;...BR IF SO.
55 161552 3$:
161552 052715 000010 BIS #BIT3,(SEF) ;; E3 = RCVR INTERRUPT NOT MASKED AT LEVEL 4
56 161556 000411 BR 5$
57 161560 012737 161602 000060 4$: MOV #5$,SL1PV ; CHANGE VECTOR...
58 161566 106427 000000 MTPS #PRO ;...AND LOWER CPU PRIORITY.
59 161572 000240 NOP ; INTERRUPT SHOULD COME IN.
60 161574 052715 000020 BIS #BIT4,(SEF) ;; E4 = RCVR INTERRUPT NOT RECEIVED
61 161600 000401 BR 6$
62 161602 022626 5$: CMP (SP)+,(SP)+ ; ON INTERRUPT, FIX STACK.
63 161604 042714 000100 6$: BIC #100,(R4) ; CLEAR THE INT ENABLE...
64 161610 016400 000002 MOV 2(R4),R0 ;...AND LOWER RCVR DONE FLAG.
65
66 161614 012700 163666 DC.DAT: MOV #FLT10,R0 ; GET DATA TABLE POINTER.
67 161620 005001 CLR R1
68 161622 005002 CLR R2
69 161624 010164 000006 MOV R1,6(R4) ; XMIT A NULL...
70 161630 105714 10$: TSTP (R4) ;...AND SEE IF LOOP IS INTACT.
71 161632 100410 BMI 3$ ; IT IS, PROCEED AT 3$.
72 161634 077203 SOB R2,10$
73 161636 000415 BR DC.LBO ; IT'S NOT, ABORT.
74
75 161640 112001 1$: MOVR (R0)+,R1 ; NOW FLOAT DATA THRU THE LOOP...
76 161642 001415 BEQ DC.XIT ;...UNTIL DONE.
77 161644 010164 000006 MOV R1,6(R4) ; XMIT A BYTE...
78 161650 105714 2$: TSTB (R4) ;...AND WAIT.
79 161652 100376 BPL 2$
80 161654 016402 000002 3$: MOV 2(R4),R2 ; READ...
81 161660 120102 CMPB R1,R2 ;...AND VERIFY.
82 161662 001766 BEQ 1$ ; LOOP IF OK.
83 161664 052715 000040 BIS #BIT5,(SEF) ;; E5 = RECEIVED DATA INCORRECT
84 161670 000402 BR DC.XIT
85 161672 DC.LBO:
161672 052715 000100 BIS #BIT6,(SEF) ;; E6 = NO RCVR DONE, LOOP-BACK OPEN
86 161676 DC.XIT:
161676 012637 000062 MOV (SP)+,SL1RV+2 ;; RESTORE SL1RV.
161702 012637 000060 MOV (SP)+,SL1RV
161706 012637 000066 MOV (SF)+,SL1V+2 ;; RESTORE SL1V.
161712 012637 000064 MOV (SP)+,SL1V
161716 011500 MOV (SEF),R0 ;; ERROR BITS => R0<11:00>...
161720 001402 BEQ 30005$ ;;...AND SKIP IF NONE.
161722 052700 060000 BIS #<6*BIT12>,R0 ;; ELSE, ADD TEST NUM => R0<15:12>...
161726 000207 30005$: RETURN ;;...AND RETURN (NZ).

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1          .SBTTL - T7    SECOND SERIAL PORT NEC7201
          ;;*****
          ;;* TEST 7 -- SECOND SERIAL PORT NEC7201
          ;;*****
          TST7:
          TNEC:
          MOV     PEVNT,-(SP)    ;; SAVE PEVNT.
          MOV     PEVNT+2,-(SP)
          MOV     NECV,-(SP)    ;; SAVE NECV.
          MOV     NECV+2,-(SP)
          CLR     (SEF)        ;; CLFAP ERROR FLAG.

2          ;
3          ; INPUT: R1<BIT0> = RUN CHAN A ONLY (INCLUDES DMA AND MODEM CONTROL).
4          ; R1<BIT1> = RUN CHAN B ONLY.
5          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
6          ;
7          ; NEC7201 SYNC/ASYNC (MULTI-PROTOCOL) SERIAL INTERFACE.
8          ; INCLUDES AN INTEL 8254 TRIPLE PIT FOR BAUD RATE GENERATION.
9          ;
10         ; FIRST, SET UP THE BAUD GENERATOR, AND VERIFY THAT
11         ; GENERAL PURPOSE TIMER 2 (800HZ) WORKS AS ADVERTISED.
12         ;
13         ; T7    SECOND SERIAL PORT NEC7201
14         ; .    E0 = ROM IN VECTOR SPACE -- CAN'T RUN
15         ; .    E1 = I8254 TIMER 2 (800HZ) DOESN'T INTERRUPT
16         ; .    E2 = ASYNC MODE, DATA XFER INCOMPLETE
17         ; .    E3 = SYNC MODE, EOF-SDLC NOT RECEIVED
18         ; .    E4 = SYNC MODE, DATA XFER INCOMPLETE
19         ; .    E5 = SYNC/ASYNC MODES, RECEIVED DATA INCORRECT
20         ;
21         161752 004737 160634    CALL    RAMLO    ; VECTOR SPACE USABLE ??
22         161756 001404          BFC     1$      ; PROCEED IF SO.
23         161760 052715 000001    BIS     #BIT0,(SEF)  ;; E0 = ROM IN VECTOR SPACE -- CAN'T RUN
24         161764 000137 163470    JMP     NECX1T
25         ;
26         161770 012704 175736    1$:    MOV     #SSL2+36,R4    ; GET I8254 CONTROL REG ADDRESS.
27         161774 106427 000300    MTPS   #PR6          ; RAISE CPU.
28         162000 112714 000066    MOVB   #066,(R4)     ; CHAN A <TIMER-012-BYTES/MODE-3IBIN>.
29         162004 112714 000166    MOVB   #166,(R4)     ; CHAN B <TIMER-11 SAME >.
30         162010 112714 000264    MOVB   #264,(R4)     ; 800HZ <TIMER-21 SAME EXCEPT MODE-2>.
31         162014 013744 162124    MOV     HZ800,-(R4)  ; SET 800HZ DIVIDER == 50HZ
32         162020 113714 162125    MOVB   HZ800+1,(R4)
33         162024 013744 162126    MOV     A4800,-(R4)  ; SET CHAN B...
34         162030 113714 162127    MOVB   A4800+1,(R4)
35         162034 013744 162126    MOV     A4800,-(R4)  ;...AND CHAN A FOR ASYNC 4800 (SYNC 76.8K).
36         162040 113714 162127    MOVB   A4800+1,(R4)
37         ;
38         162044 012737 162120 000104    MOV     #3$,PEVNT    ; SET PEVNT VECTOR...
39         162052 012737 000300 000106    MOV     #PR6,PEVNT+2
40         162060 052737 000200 177520    BIS     #BIT7,SCSRA  ;...AND ENABLE IT.
41         162066 005002          CLR     R2
42         162070 005000          CLR     R0
43         162072 106400          MTPS   R0          ; LOWER CPU.
44         162074 077001          SOB    R0,-        ; DELAY, PEVNT SHOULD COME IN...
45         162076 005302          DEC    R2          ;...AND GIVE A FEW TICKS (MORE THAN 1).
46         162100 003002          BGT    2$
47         162102 052715 000002    BIS     #BIT1,(SEF)  ;; E1 = I8254 TIMER 2 (800HZ) DOESN'T INTERRUPT
    
```

```
48 162106 005037 177520      2$: CLR      $CSPA      ; TURN OFF PEVNT...
49 162112 012714 000260      MOV      #260,(R4)    ;...AND TIMER 2 (MODE-0).
50 162116 000434              BR        NEC.DATA    ;...AND MOVE ON.
51
52 162120 005202      3$: INC      R2        ; ON "PEVNT", TICK AND RETURN.
53 162122 000002      RTI
54
55 162124 000020      HZ800: 16.          ; DIVIDER YIELDS == 50HZ
56 162126 000200      A4800: 128.        ; DIVIDER YIELDS ASYNC 4800 AND/OR SYNC 76.8K.
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33

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1
2
3
4
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8
9
10
11
12          000003      ; CHA= R3          ; DEDICATE R3 AS "CHAN-A" AND...
13          000004      ; CHX= R4          ; ...R4 AS "CHAN-IN-TEST" PORT POINTERS.
14          177774      ; STAT= -4        ; INDICES TO CHAN A/B STATUS...
15          177776      ; RDB= -2         ; ...RCVR DATA...
16          000000      ; CTRL= 0         ; ...CONTROL...
17          000002      ; XDB= 2          ; ...AND XMTR DATA PORTS.
18          170002      ; KAT= TMP1       ; EQUATE A KEEP-ALIVE-TIMER...
19          170004      ; MODE= TMP2      ; ...SET-UP/MODE FLAG...
20          170006      ; STATS= TMP3     ; ...STATUS BYTES...
21          170010      ; INHIB= TMP4     ; ...AND INHIBIT (A/B) FLAG IN RAM.
22
23          ; ASYNC SET-UP R CODE          FUNCTION
24          ; -----
25 162130      000      030      A.SET: .BYTE 0, 030 ; COMMAND <CHANNEL RESET>.
26 162132      002      024      .BYTE 2, 024 ; BUS INTERFACE <NON-VECTOREDIPRIINO-DMA>.
27 162134      004      104      .BYTE 4, 104 ; PROTOCOL <X16IASYNC-1-STOPINO-PARITY>.
28 162136      003      301      .BYTE 3, 301 ; RCVR CONTROL <8-BPCIRX-ENAB>.
29 162140      005      152      .BYTE 5, 152 ; XMTR CONTROL <8-BPCITX-ENABIPRTVX-B>.
30 162142      000      020      .BYTE 0, 020 ; COMMAND <RESET-EXT-INTS>.
31 162144      001      036      .BYTE 1, 036 ; INT CONTROL <RXI-ON-ALLICAVITX-IEINO-EXT-IE>.
32 162146      177777      -1
33
34          ; SYNC SET-UP R CODE          FUNCTION
35          ; -----
36 162150      000      030      S.SET: .BYTE 0, 030 ; COMAND <CHANNEL RESET>.
37 162152      002      024      .BYTE 2, 024 ; BUS INTERFACE <NON-VECTOREDIPRIINO-DMA>.
38 162154      004      040      .BYTE 4, 040 ; PROTOCOL <X11SDLCISYNCINO-PARITY>.
39 162156      006      000      .BYTE 6, 000 ; SYNC 1 <SEARCH ADDRESS -- UNUSED>.
40 162160      007      176      .BYTE 7, 176 ; SYNC 2 <FLAG CODE>.
41 162162      003      311      .BYTE 3, 311 ; RCVP CONTROL <8-BPCICRC-ENABIRX-ENAB>.
42 162164      005      153      .BYTE 5, 153 ; XMTR CONTROL <8-BPCITX-ENABICCITTIPRTVX-BICRC-ENAB>.
43 162166      000      200      .BYTE 0, 200 ; COMMAND <RESET TX-CRC-GEN>.
44 162170      000      100      .BYTE 0, 100 ; COMMAND <RESET RX-CRC-GEN>.
45 162172      000      020      .BYTE 0, 020 ; COMMAND <RESET EXT-INT>.
46 162174      001      036      .BYTE 1, 036 ; INT CONTROL <RXI-ON-ALLICAVITX-IEINO-EXT-IE>.
47 162176      177777      -1
48 162200      001      004      C.CLR: .BYTE 1, 004 ; INT CONTROL <KEEP-CAVIDISABLE-ALL-ELSF>
49 162202      003      300      .BYTE 3, 300 ; RCVR <RX-DISABLE>.
50 162204      005      142      .BYTE 5, 142 ; XMTP <TX-DISABLE>.
51 162206      177777      -1
    
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1          ;
2          ; FIRST, SEE IF EITHER CHAN IS INHIBITED.
3          ;
4 162210 005000      NEC.DATA: CLR  R0
5 162212 032701 000003      BIT  #R11BIT0,P1 ; SINGLE CHAN SELECTED ??
6 162216 001407      BEQ  1$ ; PROCEED IF NOT (RUN BOTH).
7 162220 012700      MOV  #SSL2+14,R0 ; YES, ASSUME RUN A, INHIBIT B...
8 162224 032701 000001      BIT  #R10,R1
9 162230 001002      BNE  1$ ;...AND SKIP IF WE GUESSED RIGHT.
10 162232 012700 175704     MOV  #SSL2+4,R0 ; ELSE, SET TO INHIBIT A.
11 162236 010065 170010     1$: MOV  R0,INHIB(STOP) ; SET/CLEAR CHAN INHIBIT FLAG.
12
13          ;
14          ; 1ST 4 PASSES.
15 162242 012700 162130     NEC.ASYNC: MOV #A.SET,R0 ; ASYNC MODE FIRST...
16 162246 000405      BR   NEC.AA
17 162250 012700 162150     NEC.SYNC: MOV  #S.SET,P0 ;...THEN, SYNC (SDLC) MODE...
18 162254 052737 000004 177520     BVS  #4,SCSRA ;...REQUIRES <SYNCA1-SYNB> IN CSRA.
19 162262 010065 170004     NEC.AA: MOV  R0,MODE(STOP) ; SAVE POINTER AS SYNC/ASYNC FLAG.
20 162266 012703 175704     MOV  #SSL2+4,CHA ; SET CHAN-A CONTROL PORT POINTER.
21 162272 012704 175714     MOV  #SSL2+14,CHX ; SET CHAN-B AS CURRENT CHAN-IN-TEST.
22 162276 111013      MOV#P (R0),(CHA)
23 162300 116013 000001     MOV#B 1(R0),(CHA) ; COMMAND <CHAN-A-RESET (INCLUDES INT LOGIC)>.
24 162304 000240      NOP ; WAIT A MOMENT.
25 162306 112014      MOV#B (R0)+,(CHX)
26 162310 112014      MOV#B (R0)+,(CHX) ; COMMAND <CHAN-B-RESET>.
27 162312 000240      NOP ; WAIT AGAIN.
28 162314 106427 000200     1$: MTPS #PR4 ; RAISE CPU.
29 162320 026504 170010     CMP  INHIB(STOP),CHX ; THIS CHANNEL INHIBITED ??
30 162324 001511      BEQ  5$ ; BR IF SO.
31 162326 112013      MOV#B (R0)+,(CHA) ; ELSE, POINT TO...
32 162330 112013      MOV#B (R0)+,(CHA) ;...AND SET BUS-INTERFACE (CR2A ALWAYS).
33 162332 112014      2$: MOV#B (R0)+,(CHX) ; POINT TO...
34 162334 112014      MOV#B (R0)+,(CHX) ;...AND SET-UP THE REST.
35 162336 105710      TSTB (R0)
36 162340 100374      HPL  2$
37 162342 012701 163666     MOV  #FLT10,R1 ; XMT BUFFER POINTER => R1.
38 162346 010502      MOV  STOP,R2
39 162350 062702 150002     ADD  #BUF#1,R2 ; RCV BUFFER POINTER => R2.
40 162354 010246      MOV  R2,-(SP) ; SAVE A COPY OF R2.
41 162356 012700 000020     3$: MOV  #16,,R0
42 162362 005022      CLR  (R2)+ ; CLEAR IT...
43 162364 077002      SOB  R0,3$
44 162366 011602      MOV  (SP),R2 ;...AND RESET POINTER.
45 162370 005065 170006     CLR  STATS(STOP) ; CLEAR SAVED STATUS...
46 162374 005065 170002     CLR  KAT(STOP) ;...AND KEEP-ALIVE-TIMER.
47 162400 012737 163522 000070     MOV  #NEC.I,NECV ; SET VECTOR...
48 162406 012737 000200 000072     MOV  #PR4,NECV+2
49 162414 106427 000000     MTPS #PRO ;...AND LOWER CPU.
50 162420 012700 000001     MOV  #1,R0 ; INIT BYTE COUNTS (RCV=0, XMT=1)...
51 162424 112164 000002     MOV#B (R1)+,XDB(CHX) ;...XMIT 1ST BYTE...
52 162430 112714 000300     MOV#B #<3*BIT6>,(CHX) ;...AND COMMAND <RESET-IDLE/CRC-LATCH>.
53 162434 026527 170004 162150     CMP  MODE(STOP),#S.SET ; SYNC MODE ??
54 162442 001411      BEQ  41$ ; BR IF SO.
55
56 162444 020027 011022     4$: CMP  R0,#<18.*BIT8>#118. ; ASYNC -- 18 BYTES TRANSFERRED ??
57 162450 001423      BEQ  43$ ; BR IF SO.
    
```

```

58 162452 005365 170002          DEC     KAT($STOP)
59 162456 001372                BNE     4$          ; ELSE, HANG-AROUND.
60 162460 052715 000004          BIS     #BIT2,($SEF) ; E2 = ASYNC MODE, DATA XFER INCOMPLETE
61 162464 000415                BR      43$
62
63 162466 005765 170006          41$:   TST     STATS($STOP) ; SYNC -- <EOF> RECEIVED ??
64 162472 100405                BMI     42$          ; BR IF SO.
65 162474 005365 170002          DEC     KAT($STOP)
66 162500 001372                BNE     41$          ; ELSE, SAME-OLF-CRAP.
67 162502 052715 000010          BIS     #BIT3,($SEF) ; E3 = SYNC MODE, EOF-SDLC NOT RECEIVED
68
69 162506 020027 012022          42$:   CMP     R0,#<20.*BIT8118.> ; BYTE COUNTS RIGHT ??
70 162512 001402                BEQ     43$          ; PROCEED IF SO.
71 162514 052715 000020          BIS     #BIT4,($SEF) ; E4 = SYNC MODE, DATA XFER INCOMPLETE
72
73 162520 010065 170002          43$:   MOV     R0,KAT($STOP) ; *** DEBUG SAVE FINAL BYTE COUNTS.
74 162524 012602                MOV     (SP)+,R2      ; GET RCV'D...
75 162526 012701 163666          MOV     #FLT10,R1    ; ...AND XMT'D POINTERS.
76 162532 012700 000022          MOV     #18.,R0
77 162536 122221                44$:   CMPB   (R2)+,(R1)+  ; RCV'D SAME AS THAT XMT'D ??
78 162540 001402                BEQ     45$          ; BR IF SO.
79 162542 052715 000040          BIS     #BIT5,($SEF) ; F5 = SYNC/ASYNC MODES, RECEIVED DATA INCORRECT
80 162546 077005                SOB     R0,44$
81
82 162550 012700 162200          5$:   MOV     #C.CLR,R0   ; DONE, CLEAN-UP TABLE POINTER => R0.
83 162554 112014                6$:   MOVB   (R0)+,(CHX) ; POINT...
84 162556 112014                MOVB   (R0)+,(CHX)  ; ...AND CLEAR (RESET) AS NECESSARY.
85 162560 105710                TSTB   (R0)
86 162562 100374                BPL     6$
87 162564 020403                CMP     CHX,CHA      ; BOTH CHANNELS DONE ??
88 162566 001405                BEQ     7$          ; BR IF SO.
89 162570 010304                MOV     CHA,CHX      ; ELSE, POINT TO CHAN A...
90 162572 016500 170004          MOV     MODE($STOP),R0 ; ...GET SET-UP POINTER => R0...
91 162576 005720                TST     (R0)+        ; ...BUMP PAST THE CHAN-RESET...
92 162600 000645                BR     1$           ; ...AND GO 'ROUND ONCE.
93
94 162602 026527 170004 162150 7$:   CMP     MODE($STOP),#S.SET ; SYNC MODE DONE ??
95 162610 001217                BNE     NFC.SYNC     ; NO, DO IT NOW.
96
97 162612 026503 170010          CMP     INHIB($STOP),CHA ; CHAN A INHIBITED ??
98 162616 001002                BNE     NEC.DMA      ; PROCEED TO DMA AND MODEM TESTS IF NOT...
99 162620 000137 163470          JMP     NECXIT       ; ...ELSE, QUIT HERE.

```

35

36

```

1
2
3
4
5 162624 106427 000200
6 162630 012701 162650
7 162634 012702 000004
8 162640 112113
9 162642 112113
10 162644 077203
11 162646 000404
12 162650 002 025
13 162652 003 311
14 162654 005 151
15 162656 001 016
16
17
18 000070
19 000056
20 000054
21 000046
22 000044
23 000042
24 000040
25 000001
26 020000
27
28 162660 010500
29 162662 062700 150002
30 162666 012701 000020
31 162672 005020
32 162674 077102
33 162676 012737 163632 000070
34 162704 012704 174400
35 162710 005064 000054
36 162714 012764 000115 000070
37 162722 012764 000074 000054
38 162730 012764 000075 000054
39 162736 005064 000046
40 162742 005064 000044
41 162746 012764 163004 000040
42 162754 012764 163024 000042
43 162762 012764 000240 000054
44 162770 060564 000002
45 162774 012764 000241 000054
46 163002 000420
47 163004 001602
48 163006 000000 163666
49 163012 000020 175707
50 163016 000022
51 163020 000020 001201
52 163024 001602
53 163026 000020 175703
54 163032 000000 150002
55 163036 000024
56 163040 000000 001201
57

;
; 5TH PASS USES DMA (ASSUMING THAT 8016 IS ALIVE AND WELL).
; THE 7201 CHIP IS STILL SET-UP FOR "CHAN A SYNC" MODE.
;
NEC.DMA: MTPS #PR4
MOV #2$,R1 ; ADJUST CHAN A SET-UP.
MOV #4,R2
1$: MOV# (R1)+,(CHA) ; POINT TO...
MOV# (R1)+,(CHA) ;...AND CHANGE...
SOB R2,1$ ;...THE FOLLOWING 4 REGISTERS.
BR 3$
2$: .BYTE 2, 025 ; CHANGE BUS-INTERFACE TO <CHAN-A-DMA>
.BYTE 3, 311 ; ENABLE RCVR...
.BYTE 5, 151 ;...AND XMITTR.
.BYTE 1, 016 ; CHANGE INT CONTROL TO <RXI-ON-1ST-CHAR>

;DEFINE THE DMA CHIP REGISTERS THAT ARE USED BELOW.
MMR= 70 ; MASTER MODE REGISTER.
STAT1= 56 ; CHANNEL 1 STATUS.
CMDR= 54 ;...AND COMMAND REGISTER (FOR BOTH).
CHA1H= 46 ; CHAIN ADDRESS REGISTERS HIGH (SEG/TAG)...
CHA2H= 44
CHA1L= 42 ;...AND THE LOW (OFFSET) HALFS.
CHA2L= 40
TC= 1 ; TERMINAL COUNT STATUS BIT (BIT0).
IP= 20000 ; INTERRUPT POSTED (DONE) STATUS BIT (BIT13).

3$: MOV $TOP,R0
ADD #BUF#1,R0 ; GET BUFFER POINTER.
MOV #16,,R1
35$: CLR (R0)+ ; CLEAR RECEIVING BUFFER.
SOB R1,35$
MOV #IXIT+2,NECV ; CHANGE THE VECTOR (IMTS DISMISSED).
MOV #SDMA,R4 ; SET-UP THE DMA ENGINE.
CLR CMDR(R4) ; CHIP RESET.
MOV #115,MMR(R4) ; SET MASTER MODE <V11WAITICPINTLV1ENAB>.
MOV #40134,CMDR(R4) ; CLEAR IE'S...
MOV #41134,CMDR(R4) ;...BOTH CHANNELS.
CLR CHA1H(R4) ; CLEAR HI CHAIN ADDRESS...
CLR CHA2H(R4) ;...BOTH CHANNELS.
MOV #4$,CHA2L(R4) ; SET CHAN 2 (XMT)...
MOV #5$,CHA1L(R4) ;...AND CHAN 1 (RCV) CHAIN ADDRESSES.
MOV #240,CMDR(R4) ; CHAIN-LOAD CHAN 1 (RCVR)...
ADD $TOP,2(R4) ;...AND ADJUST BUF#1 ADDRESS.
MOV #241,CMDR(R4) ; CHAIN-LOAD AND START CHAN 2 (XMT#R).
BR 6$

4$: 1602 ; CHAIN-LOAD ARA, ARB, OPK, AND CH-MODE.
0, FLT10 ; FROM -- DATA TABLE.
20, 175706+1 ; TO ---- 7201 XDB(LB), NO AUTO-INCR.
18. ; OPK --- 18 BYTES.
20, 1201 ; MODE -- SFT-REQ,IP-ON-TCIEOP,SNGL,BYTE-BYTE.

5$: 1602
20, 175702+1 ; FROM -- 7201 ROB(LB), NO AUTO-INCR.
0, BUF#1 ; TO ---- LOCAL BUF#1.
20. ; OPK --- 20 BYTES (18 DATA + 2 CRC).
0, 1201 ; MODE -- SAME AS ABOVE (EXCEPT NO SFT-REQ).
    
```

```

58 163044 112713 000300      6$:  MOVB  #<3*BIT6>,(CHA) ; COMMAND <RESET-IDLE/CRC-LATCH>...
59 163050 005000              CLR  R0
60 163052 106400              MTPS R0 ;...LOWER CPU.
61 163054 032764 020000 000056 7$:  BIT   #IP,STAT1(R4) ;...AND WAIT FOR CHAN1 (RCVR) DONE.
62 163062 001002              BNE  B5
63 163064 077005              SOB  R0,7$
64 163066 000404              BR   9$
65 163070 032764 000001 000056 8$:  BIT   #TC,STAT1(R4) ; GOT <IP>, SHOULD ALSO HAVE <TC>.
66 163076 001002              BNE  11$ ; BR IF SO (ALL RECEIVED).
67 163100              9$:
   163100 052715 000100              BIS   #BIT6,(SEF) ;; E6 = DMA MODE, DATA XFER INCOMPLETE
68
69 163104 012700 163666      11$:  MOV   #FLT10,R0
70 163110 010501              MOV   STOP,R1
71 163112 062701 150002              ADD   #BUFRI,R1
72 163116 012702 000022              MOV   #18,,R2
73 163122 122021      12$:  CMPB  (R0)+,(R1)+ ; CHECK DATA.
74 163124 001402              BEQ  13$ ; BR IF OK.
75 163126 052715 000200              BIS   #BIT7,(SEF) ;; E7 = DMA MODE RECEIVED DATA INCORRECT
76 163132 077205      13$:  SOB  R2,12$ ; LOOP.
77
78 163134 005037 177520              CLR  $CSRA ; ALL DONE, CLEAR CSRA...
79 163140 005064 000054              CLR  CMDR(R4) ;...RESET DMA CHIP AND FALL THRU.

```


38

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1
2 ; FINALLY, TEST ALL THE MODEM CONTROL FUNCTIONS.
3 ;
4     000004      CHB=  R4      ; REDEFINE R4 AS CHAN B POINTER.
9 ;
10 163144 106427 000200  NEC.MDM: MTPS #PR4      ; RAISE CPU.
11 163150 010304      MOV     CHA,CHB
12 163152 062704 000010      ADD     #10,CHB      ; SET CHAN B POINTER.
13 163156 112713 000030 1S:  MOVB  #<3*BIT3>,(CHA) ; <CHAN-RESET>.
14 163162 112714 000030      MOVB  #<3*BIT3>,(CHB)
15 163166 012700 000031      MOV     #100*2/5,R0  ;;DELAY 100 USEC.
163172 077001      SOB     R0,.
16 163174 112713 000021      MOVB  #<2*BIT3>#11,(CHA) ; <RESET-EXT>, POINT TO CR1...
17 163200 112714 000021      MOVB  #<2*BIT3>#11,(CHB)
18 163204 112713 000005      MOVB  #5,(CHA)      ;...AND SET <CAVIINT-ON-EXT>.
19 163210 112714 000005      MOVB  #5,(CHB)
20 163214 012737 163640 000070      MOV     #NEC.EX,NECV ; SET THE VECTOR.
21 163222 005001      CLR     R1          ; CLEAR A SPACE FOR SRO(A)...
22 163224 005002      CLR     R2          ;...AND SRO(B).
23 ;
24 ; TEST REQ-TO-SEND, CLEAR-TO-SEND, AND RCVR-READY BITS.
25 ;
26 163226 005000 3S:  CLR     R0      ,      ; KEEP-ALIVE TIMER.
27 163230 106400      MTPS  R0          ; LOWER CPU.
28 163232 112713 000005      MOVB  #5,(CHA)      ; POINT TO CR5(A)...
29 163236 112713 000002      MOVB  #2,(CHA)      ;...AND SET <REQ-TO-SEND>.
30 163242 105701 4S:  TSTR  R1          ; SHOULD GET SRO(A) STATUS INTERRUPT.
31 163244 001002      BNE   S5          ; BR IF SO.
32 163246 077003      SOB   R0,4S
33 163250 000406      BR    6S          ; INTERRUPT NOT RECEIVED.
34 163252 032701 000040 5S:  BIT   #BIT5,P1      ; SHOULD HAVE <CLR-TO-SEND>...
35 163256 001403      BEQ   6S
36 163260 032701 000010      BIT   #BIT3,R1      ;...AND <RCVR-READY>.
37 163264 001002      BNE   7S
38 163266 052715 000400 6S:  BIS   #BIT8,(SEF)  ;; E8 = STATUS WRONG OR NO INTERRUPT WITH REQ-TO-SEND SET
39 ;
40 ; NEXT, TEST TT108/2 (IN CSRA) AND DATA-MODE BITS.
41 ;
42 163272 005002 7S:  CLR     R2
43 163274 112737 000010 177520  MOVB  #BIT3,$CSRA  ; SET <TT108/2>.
44 163302 105702 8S:  TSTR  R2          ; SHOULD GET SRO(B) STATUS INTERRUPT.
45 163304 001002      BNE   9S          ; BR IF SO.
46 163306 077003      SOB   R0,8S
47 163310 000406      BR    10S         ; INTERRUPT NOT RECEIVED.
48 163312 032702 000010 9S:  BIT   #BIT3,R2      ; SHOULD HAVE <DATA-MODE>...
49 163316 001403      BEQ   10S
50 163320 032702 000040      BIT   #BIT5,R2      ;...AND NOT <INCOMING-CALL>.
51 163324 001402      BEQ   11S
52 163326 052715 001000 10S: BIS   #BIT9,(SEF)  ;; F9 = STATUS WRONG OR NO INTERRUPT WITH TT108/2 SET
53 ;
54 ; NEXT, TEST TERM-IN-SERV (CSRA), TT142 (CSRB), AND INCOMING-CALL BITS.
55 ;
56 163332 005002 11S: CLR     R2
57 163334 052737 000020 177520  BIS   #BIT4,$CSRA  ; SET <TERM-IN-SERV>.
58 163342 105702 12S: TSTR  R2          ; SHOULD GET ANOTHER SRO(B) CHANGE.
    
```

```

59 163344 001002          JNE      13$
60 163346 077003          SOB      R0,12$
61 163350 000407          BR       14$                ; INTERRUPT NOT RECEIVED.
62 163352 032737 000001 177522 13$:  BIT      #BIT0,$CSRB        ; SHOULD HAVE <TT142> IN CSRB...
63 163360 001403          BFQ     14$
64 163362 032702 000040          BIT      #BIT5,R2          ;...AND <INCOMING-CALL>.
65 163366 001002          JNE     15$
66 163370          14$:      BIS      #BIT10,(SEF)    ;; E10 = STATUS WRONG OR NO INTERRUPT WITH TERM-IN-SERV SET
67                                ;
68                                ; FINALLY, TURN ALL THAT STUFF OFF !!!!!
69                                ;
70 163374 042737 000010 177520 15$:  BIC      #BIT3,$CSRA        ; CLEAR <TT108/2>
71 163402 012700 000031          MOV      #100*2/5,R0      ;;DELAY 100 USEC.
72 163406 077001          SOB      R0,.
73 163410 005037 177520          CLR      $CSRA           ; CLEAR <TERM-IN-SERV>.
74 163414 012700 000031          MOV      #100*2/5,R0      ;;DELAY 100 USEC.
75 163420 077001          SOB      R0,.
76 163422 112713 000005          MOVVB   #5,(CHA)         ; POINT TO CR5(A)...
77 163426 112713 000000          MOVVB   #0,(CHA)         ;...AND CLEAR <REQ-TO-SEND>.
78 163432 012700 000031          MOV      #100*2/5,R0      ;;DELAY 100 USEC.
79 163436 077001          SOB      R0,.
80 163440 032701 000050          BIT      #BIT5|BIT3,R1    ; <CSIRR> IN SR0(A) SHOULD BE CLEAR...
81 163444 001003          JNE     16$
82 163446 032702 000050          BIT      #BIT5|BIT3,R2    ;...AND <ICIDM> IN SR0(B) AS WELL.
83 163452 001402          BFQ     17$
84 163454          16$:      BIS      #BIT11,(SEF)    ;; E11 = STATUS WRONG WITH EVERYTHING OFF
85 163454 052715 004000          BIS      #BIT11,(SEF)
86 163460 112713 000030          17$:      MOVVB   #<3*BIT3>,(CHA) ; ALL DONE, RESET THE CHIP.
87 163464 112714 000030          MOVVB   #<3*BIT3>,(CHB)
88 163470          NECXIT:
89 163470 012637 000072          MOV      (SP)+,NECV+2    ;; RESTORE NECV.
90 163474 012637 000070          MOV      (SP)+,NECV
91 163500 012637 000106          MOV      (SP)+,PEVNT+2   ;; RESTORE PEVNT.
92 163504 012637 000104          MOV      (SP)+,PEVNT
93 163510 011500          MOV      ($EF),R0        ;; ERROR BITS => R0<11:00>...
94 163512 001402          BFQ     30006$           ;;...AND SKIP IF NONE.
95 163514 052700 070000          BIS      #<7*BIT12>,R0   ;; ELSE, ADD TEST NUM => R0<15:12>...
96 163520 000207          30006$:  RETURN        ;;...AND RETURN (NZ).

```

40

```

1
2 ; SYNC/ASYNC DATA TEST INTERRUPT HANDLER.
3 ; BYTE COUNTS ARE MAINTAINED IN RO (LO=XMT, HI=RCV).
4 ;
5 163522 112763 000002 000010 NEC.I: MOVB #2,10(CHA) ; POINT TO SR2B...
6 163530 116346 000004 MOVB STAT+10(CHA),-(SP) ;...AND PUSH VECT/COND.
7 163534 006016 ROR (SP) ; BIT 0 => "C"...
8 163536 103420 BCS ISEXT ;...AND BR IF EXT/SPECIAL (1, 3, 5, OR 7)
9 163540 006016 ROR (SP) ; BIT 1 => "C"...
10 163542 103411 BCS IRX ;...AND BR IF RCVR (2 OR 6)...
11 ;...ELSE FALL THRU (0 OR 4).
12
13 163544 105711 ITX: TSTB (R1) ; XMIT -- ANYTHING LEFT ??
14 163546 001404 BEQ 1$ ; BR IF NOT.
15 163550 112164 000002 MOVB (R1)+,XDB(CHX) ; SEND NEXT BYTE...
16 163554 005200 INC RO ;...AND COUNT IT.
17 163556 000424 BR IXIT
18 163560 112714 000050 1$: MOVB #<5*BIT3>,(CHX) ; XMIT DONE, COMMAND <RESET-TXIP>...
19 163564 000421 BR IXIT ;...AND RETURN
20
21 163566 116422 177776 IRX: MOVB RDB(CHX),(R2)+ ; RCVR -- STUFF THE CHAR...
22 163572 062700 000400 ADD #<1*BIT8>,RO ;...AND COUNT IT.
23 163576 000414 BR IXIT
24
25 163600 116465 177774 170006 ISEXT: MOVB STAT(CHX),STATS(STOP) ; EXTERNAL/SPECIAL, GET SRO...
26 163606 112714 000001 MOVB #1,(CHX)
27 163612 116465 177774 170007 MOVB STAT(CHX),STATS+1(STOP) ;...AND SRI.
28 163620 112714 000060 1$: MOVB #<6*BIT3>,(CHX) ; COMMAND <RESET-ERROR>...
29 163624 112714 000020 MOVB #<2*BIT3>,(CHX) ;...AND <RESET-EXTERNAL>.
30
31 163630 005726 IXIT: TST (SP)+ ; FIX STACK.
32 163632 112713 000070 MOVB #<7*BIT3>,(CHA) ; SIGNAL <END-OF-INTERRUPT>.
33 163636 000002 RTI ;...AND RETURN.
34
35 ;
36 ; MODEM CONTROL TEST INTERRUPT HANDLER.
37 ;
37 163640 112713 000020 NEC.EX: MOVB #<2*BIT3>,(CHA) ; COMMAND <RESET-EXTERNAL>.
38 163644 112714 000020 MOVB #<2*BIT3>,(CHB) ; DITTO.
39 163650 116301 177774 MOVB STAT(CHA),R1 ; GET SRO(A)...
40 163654 116402 177774 MOVB STAT(CHB),R2 ;...AND SRO(B).
41 163660 112713 000070 MOVB #<7*BIT3>,(CHA) ; SIGNAL <END-OF-INTERRUPT>.
42 163664 000002 RTI
43
44 ;
45 ; FLOATING 1 AND 0 DATA TABLE.
46 163666 015 012 FLT10: .BYTE 15, 12 ; SYNC PATR.
47 163670 001 002 004 FLT1: .BYTE 001, 002, 004, 010, 020, 040, 100, 200 ; FLOATING 1.
48 163700 376 375 373 FLT0: .BYTE 376, 375, 373, 367, 357, 337, 277, 177 ; FLOATING 0.
49 163710 000000 .WORD 0 ; TERMINATOR.
50
51 .DSABL AMA

```

```
1          .SBTTL LBTEST - LOOP BACK TESTS
2
3          .ENABLE GBL,LC
4          ;
5          ; Module name: LOOP BACK TEST - LBTFST
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ; Functional Description:
13         ;
14         ; This module controls the execution of the loop back tests.
15         ; The tests are:
16         ;
17         ;     SLU1
18         ;     SLU2A
19         ;     SLU2B
20         ;     PIO
21         ;     Power Up Tests
22         ;
23         ;
24         ;
25         ; Input Parameters:
26         ;
27         ;     None
28         ;
29         ; Output Parameters:
30         ;
31         ;     None
32         ;
33         ;
34         ; Routines Used:
35         ;
36         ;     1) Execute Test (EXTEST)
37         ;     2) Power Up Tests (PUTEST)
38         ;
39
```

```
1
2 163712          LBTEST::
3
4 163712          LB100:
5
6 163712 012700 000006      MOV    #CSTMD,R0
7 163716 004767 003256      CALL   SETLED
8
9 163722 012702 000006      MOV    #6,R2
10 163726 004767 006636     CALL   EXTST
11
12 163732 012701 000001     MOV    #PI0,R1
13 163736 012702 000007     MOV    #7,R2
14 163742 004767 006622     CALL   EXTST
15
16 163746 012701 000002     MOV    #BIT1,R1
17 163752 012702 000007     MOV    #7,R2
18 163756 004767 006606     CALL   EXTST
19
20 163762 012702 000010     MOV    #10,R2
21 163766 004767 006576     CALL   EXTST
22
23 163772 004767 006326     CALL   PUTEST
24
25 163776 000745          BR     LB100
26
```

;* PROCEDURE CONTINUOUS SELF TEST
;* * DO UNTIL POWER DOWN
;* * * SET LEDS TO LOOP BACK TEST DISPLAY
;* * * TEST SLU1 LOOP BACK
;* * * TEST SLU2 CHANNEL A
;* * * TEST SLU2 CHANNEL B
;* * * TEST PIO
;* * * PERFORM POWER UP SELF TESTS
;* * END UNTIL
;* END CONTINUOUS SELF TEST

```
1          .SBTTL RESTRT - RESTART HANDLER
2          .ENABLE LC,GBL
3          . = 164000
4
5          ;
6          ; Module name: RESTRT - RESTART
7          ;
8          ; System: KXT11-CA Native Firmware
9          ;
10         ;
11         ;
12         ;
13         ;
14         ;
15         ; Functional Description:
16         ;
17         ; This module handles the restart interrupt at location 173004.
18         ;
19         ; Input Parameters:
20         ;
21         ;     NONE
22         ;
23         ; Output Parameters
24         ;
25         ;     NONE
26         ;
27         ; Data Structures Used
28         ;
29         ; Routines Used
30         ;
31         ;     1. SODTM (jump to)
32         ;
33         ;     2. QCOMIN (jump to)
34         ;
35         ;     3. TRAP4 (jump to)
36         ;
37         ;     4. TRAP10 (jump to)
38         ;
39         ;     5. TRAP24 (jump to)
```

```

1
2 164000                                RESTRT::                                ;* PROCEDURE RESTART HANDLER
3
4 164000 132737 000020 177522          BITB  #BIT4,@#KL.CSB                      ;* * IF BREAK CAUSED RESTART
5 164006 001437                                BEQ   RE400
6 164010 132737 000040 177522          BITB  #BIT5,@#KL.CSB
7 164016 001433                                BEQ   RE400
8 164020 132737 000100 177522          BITB  #BIT6,@#KL.CSB
9 164026 001427                                BEQ   RE400
10
11                                     ;* * THEN
12 164030 042737 100200 177530          BIC   #<KXSDRT I KXSNXM>,@#KW.CSD        ;* * * CLEAR NXM AND DPR INDICATORS
13                                     ;* * * CLEAR BREAK
14 164036 005737 177562                                TST   @#RBUF1A
15                                     ;* * * IF BREAK DISABLE BIT = 0
16 164042 032737 020000 175002          BIT   #KXSBDF,@#KW.STA
17 164050 001015                                BNE   RE250
18                                     ;* * * THEN
19                                     ;* * * IF STATUS REGISTER SERIAL ODT FLAG = 0
20 164052 032737 000100 175002          BIT   #KXSSDF,@#KW.STA
21 164060 001005                                BNE   RF200
22                                     ;* * * * THEN
23                                     ;* * * * * DISABLE BREAKS
24 164062 052737 070000 175002          BIS   #KXSBDF,@#KW.STA
25                                     ;* * * * * PERFORM SERIAL ODT
26 164070 000167 000532                                JMP   SODTM ;(NON STRUCTURED EXIT)
27                                     ;* * * * * ELSE
28 164074                                RE200:
29                                     ;* * * * * REMOVE RETURN ADDR. AND PSW FROM STACK
30 164074 062706 000004                                ADD   #4,SP
31                                     ;* * * * * RETURN TO SERIAL ODT VIA BREAK ENTRY POINT
32 164100 000167 000570                                JMP   @BRKENT ;(NON STRUCTURED EXIT)
33                                     ;* * * * * END IF
34                                     ;* * * * * ELSE
35 164104                                RE250:
36                                     ;* * * * * RETURN FROM INTERRUPT
37 164104 000002                                RTI   ;(NON STRUCTURED EXIT)
38                                     ;* * * * * END IF
39                                     ;* * * * * END IF
40 164106                                RE400:
41                                     ;* * IF FATAL ERROR FLAG OF STATUS REGISTER = 1
42 164106 032737 000040 175002          BIT   #KXSFEP,@#KW.STA
43 164114 001401                                BEQ   RE450
44                                     ;* * THEN
45                                     ;* * * STOP
46 164116 000777                                FAR:: @P
47                                     ;* * * ENF IF
48 164120                                RE450:
49                                     ;* * CASE CAUSE OF RESTART
50                                     ;* * WHEN Q BUS COMMAND RECEIVED
51 164120 032737 000200 177530          BIT   #KXSDRT,@#KW.CSD
52 164126 001405                                BEQ   RF500
53                                     ;* * * CLEAR NXM AND DPR INDICATORS
54 164130 042737 100200 177530          BIC   #<KXSDRT I KXSNXM>,@#KW.CSD
55                                     ;* * * DECODE COMMAND
56 164136 000167 003316                                JMP   QCOMIN ;(NON STRUCTURED EXIT)
57                                     ;* * * WHEN NXM

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44

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58 164142 032737 100000 177530 RE500: BIT   #KXSNXM,@#KW.CSD
59 164150 001500          BEQ   RE1040
60                                     ;* * * CLEAR NXM AND DPR INDICATORS
61 164152 042737 100200 177530          BIC   #<KXSDRT I KXSNXM>,@#KW.CSD
62                                     ;* * * IF STACK NXM TEST FLAG = 1
63 164160 032737 004000 175002          BIT   #KXSSXT,@#KW.STA
64 164166 001442          BEQ   RE900
65                                     ;* * * THEN
66                                     ;* * * * CLEAR STACK NXM TEST FLAG
67 164170 042737 004000 175002          BIC   #KXSSXT,@#KW.STA
68                                     ;* * * * SET STACK ERROR FLAG OF STATUS REG.
69 164176 052737 000010 175002          BIS   #KXSSEF,@#KW.STA
70                                     ;* * * * CASE MAP SELECTION
71                                     ;* * * * WHEN MAP BIT 2 = 0
72 164204 132737 000010 177522          BITB  #KXSMP2,@#KW.CSB
73 164212 001005          BNE   RE600
74                                     ;* * * * * SAVE STACK POINTER VALUE AT TOR 1 - APPLICATION
75                                     ;* * * * * DEFAULT STACK OFFSET
76 164214 010637 077676          MOV   SP,@#PTOP1+ADSTKO
77                                     ;* * * * * SET STACK POINTER TO THAT ADDRESS
78 164220 012706 077676          MOV   #RTOP1+ADSTKO,SP
79 164224 000421          BR    RE800,
80                                     ;* * * * * WHEN MAP BITS 0 AND 1 = 11
81 164226 132737 000002 177524 RE600: BITB  #KXSMP0,@#KW.CSC
82 164234 001411          BEQ   RE700
83 164236 132737 000004 177524          BITB  #KXSMP1,@#KW.CSC
84 164244 001405          BEQ   RE700
85                                     ;* * * * * SAVE STACK POINTER VALUE AT TOR 3 - APPLICATION
86                                     ;* * * * * DEFAULT STACK OFFSET
87 164246 010637 157676          MOV   SP,@#RTOP3+ADSTKO
88                                     ;* * * * * SET STACK POINTER TO THAT ADDRESS
89 164252 012706 157676          MOV   #RTOP3+ADSTKO,SP
90 164256 000404          BR    RE800
91                                     ;* * * * * ELSE
92 164260          RE700:                                     ;* * * * * SAVE STACK POINTER VALUE AT TOR - APPLICATION
93                                     ;* * * * * DEFAULT STACK OFFSET
94                                     ;* * * * * SET STACK POINTER TO THAT ADDRESS
95 164260 010637 137676          MOV   SP,@#RTOP2+ADSTKO
96                                     ;* * * * * SET STACK POINTER TO THAT ADDRESS
97 164264 012706 137676          MOV   #RTOP2+ADSTKO,SP
98                                     ;* * * * * END CASE
99 164270          RE800:                                     ;* * * * * EMULATE TRAP TO 4 (NON STRUCTURED EXIT)
100                                     ;* * * * * ELSE
101 164270 000167 002756          JMP   TRAP4
102                                     ;* * * * * IF NXM FLAG = 1
103 164274          RE900:                                     ;* * * * * THEN
104                                     ;* * * * * SET THE CARRY FLAG OF RETURN PSW
105 164274 032737 010000 175002          BIT   #KXSNXF,@#KW.STA
106 164302 001404          BEQ   RE1000
107                                     ;* * * * * THEN
108                                     ;* * * * * SET THE CARRY FLAG OF RETURN PSW
109 164304 052766 000001 000002          BIS   #1,2(SP)
110 164312 000417          BR    RE1010
111                                     ;* * * * * ELSE
112 164314          RE1000:                                     ;* * * * * CLEAR STACK ERROR FLAG
113                                     ;* * * * *
114 164314 042737 000010 175002          BIC   #KXSSEF,@#KW.STA

```



```

115                                     ;* * * * * SET TEST STACK POINTER NXM FLAG = 1
116 164322 052737 004000 175002      BIS      #KXSSXT,@#KW.STA
117                                     ;* * * * * TEST STACK BEFORE EMULATING TRAP
118 164330 005766 177776              TST      -2(SP) ;(READ NEXT TWO STACK SLOTS, WILL GET RESTART INT. IF STACK BAD)
119 164334 005766 177774              TST      -4(SP)
120                                     ;* * * * * SET TEST STACK POINTER NXM FLAG = 0
121 164340 042737 004000 175002      BIC      #KXSSXT,@#KW.STA
122                                     ;* * * * * EMULATE TRAP TO 4 (NON STRUCTURED EXIT)
123 164346 000167 002700              JMP      TRAP4
124                                     ;* * * * * END IF
125 164352                                RE1010:
126                                     ;* * * * * ENDF
127 164352                                RE1020:
128                                     ;* * * * * WHEN HALT (TEST FOR HALT INSTRUCTION AT
129                                     ;          RETURN PC -2)
130 164352 162716 000002              RE1040: SUB      #2,(SP)
131 164356 005776 000000              TST      @(SP)
132 164362 001403                      BFQ      RE1045
133 164364 062716 000002              ADD      #2,(SP)
134 164370 000412                      BR       RE1070
135 164372 062716 000002              RE1045: ADD     #2,(SP)
136                                     ;* * * * * IF ENTER ODT ON HALT FLAG = 1
137 164376 032737 000020 175002      BIT      #KXSDHL,@#KW.STA
138 164404 001402                      BEQ      RE1050,
139                                     ;* * * * * THEN
140                                     ;* * * * * ENTER SERIAL ODT
141 164406 000167 000214              JMP      SODTM ;(NON STRUCTURED EXIT)
142                                     ;* * * * * FLSE
143 164412                                RE1050:
144                                     ;* * * * * EMULATE TRAP TO 10
145 164412 000167 002676              JMP      TRAP10 ;(NON STRUCTURED EXIT)
146                                     ;* * * * * END IF
147 164416                                RE1060:
148                                     ;* * * * * WHEN BHALT
149 164416                                RE1070:
150 164416 032737 001000 177530      BIT      #KXSBHF,@#KW.CSD
151 164424 001411                      BEQ      RE1080
152                                     ;* * * * * IF SODT OR QODT FLAG NOT SET
153 164426 032737 000300 175002      BIT      #<KXSSOF | KXSQOF>,@#KW.STA
154 164434 001002                      BNE     RE1072
155                                     ;* * * * * THEN
156                                     ;* * * * * EMULATE TRAP TO 24
157 164436 000167 002714              JMP      TRAP24
158                                     ;* * * * * ELSE
159 164442                                RE1072:
160                                     ;* * * * * CLEAR BHALT INDICATOR
161 164442 042737 001000 177530      BIC      #KXSBHF,@#KW.CSD
162                                     ;* * * * * END IF
163 164450                                RE1075:
164                                     ;* * * * * END CASE
165 164450                                RE1080:
166                                     ;* * * * * RETURN FROM INTERRUPT
167 164450 000002                      RTI
168                                     ;* * * * * END RESTART HANDLER

```

```

1          .SBTTL SAVERG - SAVE REGISTERS
2          .ENABLE LC,CBL
3
4          ;
5          ; Module name: SAVERG - SAVE REGISTERS
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ; Functional Description:
12         ;
13         ; This module is used by both the serial and Q bus ODT monitors. It
14         ; saves the contents of the users CPU registers. This module exits
15         ; by jumping back to the ODT monitor which called it. It determines
16         ; which ODT monitor it is to return to by testing the state field of
17         ; the IOP status register. The following table describes the use of the
18         ; native firmware reserved RAM for this purpose.
19         ;
20         ;
21         ;
22         ;
23         ;
24         ;
25         ;
26         ;
27         ;
28         ;
29         ;
30         ;
31         ;
32         ;
33         ;
34         ;
35         ;
36         ;
37         ;
38         ;
39         ;
40         ;
41         ;
42         ;
43         ;
44         ;
45         ;
46         ; Input Parameters:
47         ;
48         ; ALL CPU REGISTERS
49         ;
50         ; Output Parameters
51         ;
52         ; STACK POINTER
53         ;
54         ; Routines Used
55         ;
56         ; NONE
57         ;

```

NATIVE FIRMWARE RESERVED RAM USE

USE	ADDRESS
BATTERY BACKUP FLAG 1	TOP OF NATIVE RAM
" " " 2	TOR - 2
BOOT TYPE FLAG WORD	TOR - 4
NATIVE FIRMWARE FLAG WORD	TOR - 6
APPLICATION STACK POINTER HOLD	TOR - 10
" PS SAVE	TOR - 12
" PC "	TOR - 14
" SP "	TOR - 16
" R5 "	TOR - 20
" R4 "	TOR - 22
" R3 "	TOR - 24
" R2 "	TOR - 26
" R1 "	TOR - 30
" R0 "	TOR - 32
ODT TOP OF WORKING STACK	TOR - 34
ODT STACK GUARD WORD	TOR - 76
APPLICATION DEFAULT STACK	TOR - 100

47

```

1
2
3
4          000000          BBF10 ==: 0          ;BATTERY BACKUP FLAG 1 ADDRESS OFFSET
5          177776          BBF20 ==: BBF10 - 2          ; " " " 2 " "
6          177774          BOOTFO ==: BBF20 - 2          ;BOOT TYPE FLAG, SPECIFIES BOOT DEVICE AND TEST
7          177772          NFFWDO ==: BOOTFO - 2          ;NATIVE FIRMWARE FLAG WORD ADDRESS OFFSET
8
9          177770          APLPSO ==: NFFWDO - 2          ;APPLICATION PS SAVE ADDRESS OFFSET
10         177766          APLPCO ==: APLPSO - 2          ; " " PC " " "
11         177764          APLSPO ==: APLPCO - 2          ; " " SP " " "
12         177762          APLR50 ==: APLSPO - 2          ; " " R5 " " "
13         177760          APLR40 ==: APLR50 - 2          ; " " R4 " " "
14         177756          APLR30 ==: APLR40 - 2          ; " " R3 " " "
15         177754          APLR20 ==: APLR30 - 2          ; " " R2 " " "
16         177752          APLR10 ==: APLR20 - 2          ; " " R1 " " "
17         177750          APLR00 ==: APLR10 - 2          ; " " R0 " " "
18         177746          ODTSTK ==: APLR00 - 2          ;ODT WORKING TOP OF STACK STACK ADDRESS OFFSET
19         177702          ODTSTG ==: -76          ;ODT STACK GUARD WORD ADDRESS OFFSET
20         177700          ADSTKO ==: -100          ;APPLICATION DEFAULT TOP OF STACK OFFSET ADDRESS
21         ;
22         077776          RTOP1 ==: 77776          ;TOP OF RAM 1
23         137776          RTOP2 ==: 137776          ; " " " 2
24         157776          RTOP3 ==: 157776          ; " " " 3
25         000000          RROT1 ==: 0          ;BOTTOM OF RAM 1
26         040000          RROT2 ==: 40000          ; " " " 2
27         100000          RROT3 ==: 100000          ; " " " 3
28         077762          SP1 ==: RTOP1 + APLSPO          ;INITIAL ODT STACK 1 ABSOLUTE ADDRESS
29         137762          SP2 ==: RTOP2 + APLSPO          ; " " " 2 " "
30         157762          SP3 ==: RTOP3 + APLSPO          ; " " " 3 " "
31         000014          SPOPF ==: -APLSPO          ;OFFSET OF STACK POINTER FROM TOP OF RAM
    
```

```

1                                     ;* PROCEDURE SAVE REGISTERS
2 164452                                SAVERG::
3
4                                     ;* * CASE MAP BITS
5 164452 032737 000010 177522          BIT   #KXSMP2,@#KW.CSB
6 164460 001005                                BNE   SR100
7                                     ;* * WHEN MAP BIT 2 = 0
8 164462 010637 077762                MOV   SP,@#SP1
9                                     ;* * * SAVE USERS STACK POINTER AT ODT STACK 1
10 164466 012706 077762                MOV   #SP1,SP
11 164472 000421                                BR    SR300
12                                     ;* * * SET STACK POINTER = ODT STACK 1
13 164474 032737 000002 177522  SR100: BIT   #KXSMP0,@#KW.CSB
14 164502 001411                                BFQ   SR200
15 164504 032737 000004 177522          BIT   #KXSMP1,@#KW.CSB
16 164512 001405                                BFQ   SR200
17                                     ;* * * WHEN MAP BITS 0 AND 1 = 11
18 164514 010637 157762                MOV   SP,@#SP3
19                                     ;* * * SAVE USERS STACK POINTER AT ODT STACK 3
20 164520 012706 157762                MOV   #SP3,SP
21 164524 000404                                BR    SR300
22                                     ;* * * SET STACK POINTER TO ODT STACK 3
23 164526                                SR200:
24                                     ;* * * ELSE
25 164526 010637 137762                MOV   SP,@#SP2
26                                     ;* * * SAVE USERS STACK POINTER AT ODT STACK 2
27 164532 012706 137762                MOV   #SP2,SP
28                                     ;* * * SET STACK POINTER TO ODT STACK 2
29 164536                                SR300:
30                                     ;* * * END CASE
31 164536 010546                                MOV   R5,-(SP)
32 164540 010446                                MOV   R4,-(SP)
33 164542 010346                                MOV   R3,-(SP)
34 164544 010246                                MOV   R2,-(SP)
35 164546 010146                                MOV   R1,-(SP)
36 164550 010046                                MOV   R0,-(SP)
37                                     ;* * * SAVE USER REGISTERS 5 THROUGH 0
38 164552 010605                                MOV   SP,R5
39 164554 162705 177750                SUB   #APLRO0,R5
40                                     ;* * SET R5 = TOP OF RAM ADDRESS
41 164560 016500 177764                MOV   APLSP0(R5),R0
42 164564 012065 177766                MOV   (R0)+,APLPC0(R5)
43 164570 012065 177770                MOV   (R0)+,APLPS0(R5)
44                                     ;* * SAVE USER PC AND PS
45 164574 010065 177764                MOV   R0,APLSP0(R5)
46                                     ;* * REMOVE USER PS AND PC FROM USER STACK
47 164600 012765 123456 177702          MOV   #123456,ODTSTG(R5)
48                                     ;* * WRITE GUARD WORD = 123456
49 164606 032767 000200 010166          BIT   #KXSQ0F,KW.STA
50 164614 001402                                BFQ   SR400
51                                     ;* * IF STATUS REGISTER Q BUS ODT MODE FLAG SET
52                                     ;* * THEN
53 164616 000167 004622                JMP   QSRET
54                                     ;* * * RETURN TO Q BUS ODT MONITOR (NON STRUCTURED JUMP TO Q
55 164622                                SR400:
56                                     ;* * * ELSE
57 164622 000167 000026                JMP   SSRFT

```

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SAVERG - SAVE REGISTERS

58
59

;* * END IF
/* * END SAVE REGISTERS

51

```

1          .SBTTL SODTM - SERIAL ODT MONITOR
2
3          .ENABL LC,GBL
4          ;
5          ; Module name: SODTM - SERIAL ODT MONITOR
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This is the main controlling module for the serial ODT mode.
17         ; It supervises the ODT function and on completion returns
18         ; control back to the application software.
19         ; There is a secondary entry point to this module. This
20         ; entry point is used by the RESTART module when it determines
21         ; a BREAK was received on the console serial line and the IOP
22         ; was executing serial ODT. This entry causes the ODT to
23         ; start with a fresh command prompt without effecting the
24         ; contents of the application register storage area.
25         ;
26         ; The valid ODT commands are as follows:
27         ;
28         ; Kn/ - Open register n (n = 0 through 7 and S)
29         ; n/ - Open location n
30         ; / - Re-open previous location or register
31         ; m,n/ - Examine locations m through n, leaving location n open
32         ; Rm,n/ - Examine registers m through n, leaving location n open
33         ; n - Deposit n in open register or location
34         ; <LF> - Close last location or register, open next +
35         ; ~ - Close last location or register, open next -
36         ; <CR> - Close location or register
37         ; P - Proceed with execution of application
38         ; Gn - Execute application at location n
39         ;
40         ; NOTE: A range examine can be aborted by pressing BREAK key.
41         ;
42         ; Input Parameters:
43         ;
44         ; NONE
45         ;
46         ; Output Parameters:
47         ;
48         ; NONE
49         ;
50         ; Routines Used:
51         ;
52         ; SAVERG
53         ; SETL&D
54         ; ADDR&G
55         ; EXAMIN
56         ; DISPST
57         ; DATCOM

```

58 ; DEPOS
59 ; GOPROC
60

52

1 ;REGISTER 3 IS USED AS THE FLAG REGISTER FOR ALL ODT ROUTINES
2 ;THE FOLLOWING ARE THE BIT DEFINITIONS FOR THIS REGISTER
3
4 000001 DCDFGB === 1 ;DATA/COMMAND ROUTINE - DONE FLAG
5 000002 DARFGB === 2 ;DATA/COMMAND ROUTINE - DATA RECV'D WITH COMM. FLAG
6 000004 APDFGB === 4 ;ADDRESS/REGISTER ROUTINE - DONE FLAG
7 000010 FCHFGB === 10 ;ADDRESS/REGISTER ROUTINE - FIRST CHAR. RECV'D FLAG
8 000020 CNDFGB === 20 ;SERIAL ODT MONITOR ROUTINE - CONDITION FLAG
9 000040 XOFFGB === 40 ;GENERAL - XOFF FLAG
10 000200 RECFGB === 200 ;GENERAL - REGISTER FLAG
11 100000 ERRFGB === 100000 ;GENERAL - ERROR FLAG
12

```

1                                     ;* PROCEDURE SERIAL ODT MONITOR
2 164626                               SODTM::
3                                     ;* * DISABLE DUAL PORT RAM
4 164626 042737 000100 177530         BIC  #KXSDEN,@#KW.CSD
5                                     ;* * DISABLE BREAKS
6                                     ;* * DISABLE NXM TRAP TO 4
7                                     ;* * SET SERIAL ODT FLAG
8 164634 052737 030100 175002         BIS  #<KXSBDF I KXSNXF I KXSSOF>,@#KW.STA
9                                     ;* * CLEAR Q BUS ODT FLAG
10 164642 042737 000200 175002        BIC  #KXSQOF,@#KW.STA
11                                     ;* * SET SERIAL ODT FLAG
12                                     ;* * SAVE REGISTERS (JUMP TO AND BACK FROM
13                                     ;* * SAVE REGISTERS MODULE)
14 164650 000167 177576               JMP   SAVERG
15 164654                               SSRPT::
16                                     ;* * SET LEDS TO SERIAL ODT MODE DISPLAY
17 164654 012700 000004               MOV   #SODTMD,R0
18 164660 004767 002314               CALL  SETLED
19                                     ;* * READ RBUF
20 164664 105737 177562               TSTB @#RBUF1A
21                                     ;* * SET BAUD RATE
22 164670 004767 001762               CALL  ABAUD
23                                     ;* * CLFAR RECEIVE BUFFER
24 164674                               BRKENT::
25                                     ;* * RE-INITIALIZE ODT STACK POINTER
26 164674 012700 177750               MOV   #ODTSTK+2,R0
27 164700 060500                       ADD   R5,R0
28 164702 010006                       MOV   R0,SP
29                                     ;* * ENABLE BREAK
30 164704 042737 020000 175002        BIC  #KXSBDF,@#KW.STA
31                                     ;* * CLEAR ALL ODT FLAG BITS
32 164712 005003                       CLR   R3
33                                     ;* * CLEAR TARGET BUFFER
34 164714 005002                       CLR   R2
35                                     ;* * DISABLE TRAP TO 4
36 164716 052737 010000 175002        BIS  #KXSNXF,@#KW.STA
37                                     ;* * PRINT CR LF
38 164724 004767 000560               CALL  PCRLF ;(LOCAL CALL)
39                                     ;* * DISPLAY PC VALUE
40 164730 016501 177766               MOV   APLPCO(R5),R1
41 164734 004767 001572               CALL  DISPWD
42                                     ;* * ENABLE BREAKS
43 164740 042737 020000 175002        BIC  #KXSBDF,@#KW.STA
44                                     ;* * DO UNTIL PROCEED COMMAND
45 164746                               S0100:
46                                     ;* * OR GO COMMAND
47 164746                               S0200:
48                                     ;* * * DISPLAY ODT PROMPT
49 164746 012701 166266               MOV   #PROMPT,R1
50 164752 004767 001370               CALL  DISPST
51                                     ;* * * CLEAR FIRST CHARACTER FLAG
52 164756 042703 000010               BIC  #FCHFGB,R3
53                                     ;* * * GET ADDRESS OR REGISTER NUMBER
54 164762 004767 000534               CALL  ADDRREG
55                                     ;* * * IF ERROR FLAG = 0
56 164766 005703                       TST  R3
57 164770 100002                       BPL  S0300

```

53

55

115	165110	001014		BNE	S01300	
116						; * * * * AND TARGET IS AN ADDRESS
117	165112	105703		TSTB	R3	
118	165114	100412		BMI	S01300	
119						; * * * * * SET LEOS TO NON NATIVE CODE DISPLAY
120	165116	012700	000000	MOV	#NNCED,R0	
121	165122	004767	002052	CALL	SETLED	
122						; * * * * * EXECUTE AT ADDRESS ENTERED (WILL NOT
123						; RETURN IF NO ERROR)
124	165126	010400		MOV	R4,R0	
125	165130	004767	001636	CALL	GO	
126						; * * * * * SET ERROR FLAG = 1
127	165134	052703	100000	BIS	#ERRFGB,R3	
128	165140	000415		BR	S01450	
129						; * * * * * WHEN "P"
130	165142					
131	165142	122700	000120	CMPE	#*P,R0	
132	165146	001010		BNE	S01400	
133						; * * * * * AND NO DATA PRECEDED COMMAND
134	165150	032703	000002	BIT	#DAPFGB,R3	
135	165154	001005		BNE	S01400	
136						; * * * * * EXECUTE PROCEED (WILL NOT RETURN IF
137						; NO ERROR)
138	165156	004767	001626	CALL	PROC '	
139						; * * * * * SET ERROR FLAG = 1
140	165162	052703	100000	BIS	#ERRFGB,R3	
141	165166	000402		BR	S01450	
142						; * * * * * ELSE (INVALID COMMAND)
143	165170					
144						; * * * * * SET ERROR FLAG
145	165170	052703	100000	BIS	#ERRFGB,R3	
146						; * * * * * END CASE
147	165174					
148						; * * * * * DO WHILE CONDITION FLAG = OPEN
149	165174					
150	165174	032703	000020	BIT	#CNDFGB,R3	
151	165200	001504		BEQ	S01800	
152						; * * * * * AND ERROR FLAG = 0
153	165202	005703		TST	R3	
154	165204	100502		BMI	S01800	
155						; * * * * * PRINT SPACE
156	165206	012701	166272	MOV	#SPACE,R1	
157	165212	004767	001130	CALL	DISPST	
158						; * * * * * GET INPUT DATA
159	165216	004767	001162	CALL	DATCOM	
160						; * * * * * IF VALTD DATA AND COMMAND
161	165222	005703		TST	R3	
162	165224	100467		BMI	S01600	
163						; * * * * * THEN
164						; * * * * * * IF DATA PROCEEDED COMMAND
165	165226	032703	000002	BIT	#DARFGB,R3	
166	165232	001402		BEQ	S01500	
167						; * * * * * * THEN
168						; * * * * * * * DEPOSIT DATA INTO ADDRESS OR REGISTER
169						; (R2=ADDR.)
170						; (R4=DATA)
171	165234	004767	001234	CALL	DEPOS	

56

```

172                                     ; * * * * * END IF
173 165240                               S01500:
174                                     ; * * * * * CASE COMMAND
175                                     ; * * * * * WHEN CR
176 165240 122700 000015                 CMPR  #CR,R0
177 165244 001003                         BNE  S01550
178                                     ; * * * * * SET CONDITION FLAG = CLOSED
179 165246 042703 000020                 BIC  #CNDFGB,R3
180 165252 000453                         BP   S01570
181                                     ; * * * * * WHEN LF
182 165254                               S01550:
183 165254 122700 000012                 CMPB  #LF,R0
184 165260 001023                         BNE  S01560
185                                     ; * * * * * PRINT CR LF
186 165262 004767 000222                 CALL  PCRLF  ;(LOCAL CALL)
187                                     ; * * * * * INCREMENT TARGET
188 165266 005202                         INC  R2
189                                     ; * * * * * IF TYPE IS REGISTER
190 165270 105703                         TSTR  R3
191 165272 100007                         BPL  S01555
192                                     ; * * * * * THEN
193                                     ; * * * * * SET TARGET MOD 10
194 165274 022702 000011                 CMP  #11,R2
195 165300 101001                         BHI  S01552
196 165302 005002                         CLR  R2
197 165304                               S01552:
198                                     ; * * * * * DISPLAY REGISTER NUMBER
199 165304 004767 000140                 CALL  DISPRG ;(LOCAL CALL)
200 165310 000404                         BR   S01557
201                                     ; * * * * * ELSE
202 165312                               S01555:
203                                     ; * * * * * INCREMENT TARGET AGAIN
204 165312 005202                         INC  R2
205                                     ; * * * * * DISPLAY TARGET
206 165314 010201                         MOV  R2,P1
207 165316 004767 001210                 CALL  DISPWD
208                                     ; * * * * * END IF
209 165322                               S01557:
210                                     ; * * * * * EXAMINE
211 165322 004767 000142                 CALL  EXMDIS ;(LOCAL CALL)
212 165326 000425                         BR   S01570
213                                     ; * * * * * WHEN ^
214 165330                               S01560:
215 165330 122700 000136                 CMPB  #^,R0
216 165334 001022                         BNE  S01570
217                                     ; * * * * * PRINT CR LF
218 165336 004767 000146                 CALL  PCRLF  ;(LOCAL CALL)
219                                     ; * * * * * IF TYPE IS REGISTER
220 165342 105703                         TSTR  R3
221 165344 100007                         BPL  S01567
222                                     ; * * * * * THEN
223                                     ; * * * * * DECREMENT TARGET
224 165346 005302                         DEC  R2
225                                     ; * * * * * SET REGISTER NUMBER MOD 10
226 165350 100002                         BPL  S01565
227 165352 012702 000010                 MOV  #10,R2
228 165356                               S01565:

```

```

229                                     ;* * * * * DISPLAY REGISTER NUMBER
230 165356 004767 000066             CALL  DISPRG ;(LOCAL CALL)
231 165362 000405                     BP    SO1569
232                                     ;* * * * * ELSE
233 165364                               SO1567:
234                                     ;* * * * * DECREMENT TARGET BY 2
235 165364 005302                     DEC   R2
236 165366 005302                     DEC   R2
237                                     ;* * * * * DISPLAY TARGET
238 165370 010201                     MOV   R2,R1
239 165372 004767 001134             CALL  DTSPWD
240                                     ;* * * * * END IF
241 165376                               SO1569:
242                                     ;* * * * * EXAMINE
243 165376 004767 000066             CALL  EXMDIS ;(LOCAL CALL)
244                                     ;* * * * * END CASE
245 165402                               SO1570:
246 165402 000402                     BP    SO1700
247                                     ;* * * * * ELSE
248 165404                               SO1600:
249                                     ;* * * * * SET ERROR FLAG
250 165404 052703 100000             BIS   #ERPFGB,R3
251                                     ;* * * * * END IF
252 165410                               SO1700:
253                                     ;* * * * * END WHILE
254 165410 000671                     BR    SO1470
255 165412                               SO1800:
256                                     ;* * * * * END IF
257 165412                               SO1850:
258                                     ;* * * * * IF ERROR FLAG = 1
259 165412 005703                     TST   R3
260 165414 100011                     BPL   SO1900
261                                     ;* * * * * THEN
262                                     ;* * * * * SEND ERROR PROMPT
263 165416 012701 166264             MOV   #ERROR,R1
264 165422 004767 000720             CALL  DISPST
265                                     ;* * * * * CLEAR REGISTER FLAG
266 165426 042703 000200             BIC   #REGFGB,R3
267                                     ;* * * * * SET TARGET2 TO NXM ADDRESS
268                                     ;           (TO CAUSE AN ERROR IF RETURN / ENTERED)
269 165432 012702 177777             MOV   #177777,R2
270                                     ;* * * * * CLEAR TARGET1
271 165436 005004                     CLR   R4
272                                     ;* * * * * END IF
273 165440                               SO1900:
274                                     ;* * * * * CLEAR ALL ODT FLAGS EXCEPT
275                                     ;           REGISTER FLAG
276 165440 042703 177577             BIC   #~C<REGFGB>,R3
277                                     ;* * * * * END UNTIL
278 165444 000167 177276             JMP   SO100
279                                     ;* * * * * END SERIAL ODT MONITOR
280
281

```

57

```
1 ; The following subroutines were created to conserve memory and are only used
2 ; by this module.
3
4 ;* PROCEDURE DISPLAY REGISTER NUMBER
5 165450 DISPRG: ;* * CALCULATE DISPLAY POINTER
6
7 165450 010201 MOV R2,R1
8 165452 006301 ASL K1
9 165454 006301 ASL R1
10 165456 062701 166303 ADD #R&GDIS,R1
11 ;* * DISPLAY STRING
12 165462 004767 000660 CALL DISPST
13 ;* END DISPLAY REGISTER NUMBER
14 165466 000207 RETURN
15
16 ;* PROCEDURE EXAMINE AND DISPLAY
17
18 165470 EXMDIS: ;* * DISPLAY "/"
19
20 165470 012701 166301 MOV #OPENDS,R1
21 165474 004767 000646 CALL DISPST
22 ;* * EXAMINE DATA @ TARGET
23 165500 005000 CLR R0
24 165502 004767 000234 CALL EXAMIN
25 ;* END EXAMINE AND DISPLAY
26 165506 000207 RETURN
27
28 ;* PROCEDURE PRINT CRLF
29
30 165510 PCRLF: ;* * POINT TO STRING
31 ;* * DISPLAY STRING
32 165510 012701 166274 MOV #CRLF,R1
33 ;* * DISPLAY STRING
34 165514 004767 000626 CALL DISPST
35 ;* END PRINT CRLF
36 165520 000207 RETURN
37
```

```
1 .SBTTL ADDRAG - GET ADDRESS/REGISTER
2 .ENABLE LC,GBL
3
4 ;
5 ; Module name: ADDRAG - GET ADDRESS/REGISTER
6 ;
7 ; System: KXT11-CA Native Firmware
8 ;
9 ;
10 ;
11 ;
12 ; Functional Description:
13 ;
14 ; This module is used by the serial ODT monitor. It receives data
15 ; from the console serial line, accumulates a word target delimited
16 ; by a valid command or an error. The valid commands are: ",", CR, LF,
17 ; "/", "G" or "P". It returns the target, the command
18 ; the target type (register or address) and the error status.
19
20 ;Input Parameters:
21
22 ; NONE
23
24 ;Output Parameters
25
26 ; 1) R0 = COMMAND RECEIVED
27 ; 2) R4 = TARGET (ADDRESS OR REGISTER NO.)
28 ; 3) R3, BIT REGFGB - 1 = REGISTER NO., 0 = ADDRESS
29 ; 4) R3, BIT DARFGB - ADDRESS/REGISTER RECEIVED WITH COMMAND FLAG,
30 ; 1 = YES. 0 = NO
31 ; 5) R3, BIT ERRFGB - 1 = ERROR, NOT ALTERED IF NO ERROR
32
33 ;DATA STRUCTURES USED
34
35 ; NONE
36
37 ;Routines Used
38
39 ; 1) CHKCHR
40 ; 2) ACCUM
41
```

60

```

1
2 165522
3
4
5 165522 042703 000006 BIC #<ARDFGB I DARFGB>,R3
6
7 165526 005004 CLR R4
8
9 165530 AD100:
10
11 165530 AD200:
12
13 165530 004767 006016 CALL GETIN
14
15 165534 103417 BCS AD253
16
17 165536 032703 000010 BIT #FCHFGB,R3
18 165542 001002 BNE AD220
19
20
21 165544 042703 000200 BIC #REGFGB,R3
22
23 165550 AD220:
24
25 165550 105703 TSTB R3
26 165552 100002 BPL AD240
27
28
29 165554 010004 MOV R0,R4
30 165556 000402 BP AD250
31
32 165560 AD240:
33
34 165560 004767 005754 CALL ACCUM
35
36 165564 AD250:
37
38 165564 052703 000010 BIS #FCHFGB,R3
39
40 165570 000241 CLC
41 165572 000424 BR AD290
42
43 165574 AD253:
44
45 165574 120027 000141 CMPR R0,#"a
46 165600 103402 BLO AD255
47
48
49 165602 042700 000040 BIC #40,R0
50
51 165606 AD255:
52
53 165606 122700 000123 CMPB #"S,R0
54 165612 001013 BNE AD280
55 165614 AD270:
56
57 165614 105703 TSTB R3

```

```

;* PROCEDURE GET ADDRESS/REGISTER
;* * CLEAR ADDRESS/REGISTER DONE FLAG
;* * CLEAR DATA RECEIVED FLAG
;* * CLEAR ACCUMULATED NUMBER
;* * DO UNTIL DONE FLAG SET
;* * * DO UNTIL NON NUMBER CHARACTER RECEIVED
;* * * * GET INPUT
;* * * * IF INPUT = 0 THRU 7
;* * * * * IF FIRST CHARACTER
;* * * * * THEN
;* * * * * * CLEAR REGISTER FLAG
;* * * * * END IF
;* * * * * IF REGISTER FLAG = 1
;* * * * * THEN
;* * * * * * REPLACE ACCUM VALUE WITH INPUT
;* * * * * ELSE
;* * * * * * ACCUMULATE DATA
;* * * * * END IF
;* * * * * SET FIRST CHARACTER RECEIVED FLAG = 1
;* * * * * CLEAR NON NUMERIC INPUT FLAG
;* * * * * ELSE
;* * * * * IF INPUT => "a"
;* * * * * THEN
;* * * * * * CONVERT TO UPPER CASE
;* * * * * END IF
;* * * * * IF INPUT = "S" OR "s"
;* * * * * AND REGISTER FLAG = 1

```

```

58 165616 100011          LPL      AD280
59
60 165620 032703 000010   BIT      #FCHFGB,R3      ;* * * * * AND NOT FIRST CHARACTER RECEIVED
61 165624 001406          BEQ      AD280
62
63 165626 012704 000010   MOV      #10,R4        ;* * * * * SET ACCUMULATED VALUE = 10
64
65
66 165632 052703 000012   BIS      #<DARFGB I FCHFGB>,R3 ;* * * * * SET DATA RECEIVED FLAG = 1
67
68 165636 000241          CLC
69 165640 000401          BR      AD290        ;* * * * * SET FIRST CHARACTER RECEIVED FLAG = 1
70
71 165642          AD280:          ;* * * * * SET NON NUMERIC FLAG = 0
72
73 165642 000261          SEC
74
75 165644          AD290:          ;* * * * * ELSE
76
77
78 165644 103331          BCC      AD200        ;* * * * * SET NON NUMERIC INPUT FLAG = 1
79 165646          AD300:          ;* * * * * END IF
80
81
82
83
84
85
86
87 165646 012701 165734   MOV      #CHTAB,F1     ;* * * * * END IF
88 165652 122100          AD400:  CMPB     (R1)+,R0   ;* * * * * FND UNTIL
89 165654 001404          BEQ      AD500
90 165656 022701 165742   CMP      #CHEND,R1
91 165662 001404          BEQ      AD600
92 165664 000772          BR      AD400
93 165666          AD500:          ;* * * * * CASE COMMAND RECEIVED
94
95
96 165666 052703 000014   BIS      #<FCHFGB I ARDFGB>,R3 ;* * * * * WHEN ","
97 165672 000414          BR      AD800
98
99 165674          AD600:          ;* * * * * OR CR
100 165674 122700 000122  CMPB     #R,R,R0
101 165700 001007          BNE     AD700
102
103 165702 032703 000010   BIT      #FCHFGB,R3     ;* * * * * OR LF
104 165706 001004          BNE     AD700
105
106
107
108 165710 052703 000212   BIS      #<DARFGB I RECFCB I FCHFGB>,R3 ;* * * * * OR "/"
109
110 165714 005004          CLR     R4
111 165716 000402          BR      AD800        ;* * * * * OR "G"
112
113 165720          AD700:          ;* * * * * OR "p"
114
114

```

61


```
115                                     ;* * * * SET DONE FLAG
116 165720 052703 100004             BIS    #<ERRFCB I ARDFCB>,R3
117                                     ;* * * * END CASE
118 165724                               ADR00:
119                                     ;* * * * END UNTIL
120 165724 032703 000004             BIT    #ARDFCB,R3
121 165730 001677                     BEQ    AD100
122                                     ;* * * * RETURN
123 165732 000207                     RETURN
124                                     ;* * * * END GET ADDRESS/REGISTER
125
126
127                                     ;CHARACTER TABLE
128
129 165734 054 015 012 CHTAB: .ASCII ",,"<15><12>"/GP"
130 165742                                     CHEND:
131                                     .EVEN
```

```
1          .SBTTL EXAMIN - EXAMINE
2          .FNABLE LC,GBL
3
4          ;
5          ; Module name: EXAMIN - EXAMINE
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module performs the memory or register examine function for
17         ; both the Q bus and serial ODT monitors. The output of this module
18         ; is directly to the user (the serial line or the dual port RAM).
19
20         ;Input Parameters:
21
22         ; R0 - FLAGS,
23         ; BIT (RNGFCB) = 1 (RANGE EXAMIN), BIT = 0 (SINGLE EXAMIN)
24         ; R2 - TARGET 1
25         ; BIT 0 - TYPE, BIT = 0 (REGISTER), BIT = 1 (ADDRESS)
26         ; R4 - TARGET 2
27         ; BIT 0 - TYPE, BIT = 0 (REGISTER), BIT = 1 (ADDRESS)
28
29         ;Output Parameters
30
31         ; R3, BIT (ERRFCB) - ERROR FLAG, BIT = 1 (ERROR), NO ERROR BIT NOT ALTERED
32
33         ;DATA STRUCTURES
34
35         ; 1) PRINT STRINGS
36         ; 2) DUAL PORT PAM REGISTER 2
37         ; 3) IOP STATUS REGISTER
38         ; 4) IOP COMMAND REGISTER
39
40         ;Routines Used
41
42         ; 1) DISPLAY STRING (DISPST)
43         ; 2) DISPLAY WORD (DISPWD)
44         ; 3) CHECK CHARACTER (CHKCHR)
45
46         ;
```

64

```

1
2          000002          RNGFGB ==:      2
3
4
5
6
7 165742          EXAMIN::
8
9 165742 032737 000100 175002          BIT      #RNGFGB, @#KW.STA
10 165750 001525          BEQ      EX1000
11
12
13 165752 105703          TSTB     R3
14 165754 100021          BPL      EX300
15
16
17 165756 022702 000011          CMP      #11, R2
18 165762 101001          BHI     EX10
19 165764 005002          CLR     R2
20 165766          EX10:
21
22 165766 022704 000011          CMP      #11, R4
23 165772 101001          BHI     EX20
24 165774 005004          CLR     R4
25 165776          EX20:
26
27
28 165776 006302          ASL     R2
29 166000 062702 177750          ADD     #APLR00, R2
30 166004 060502          ADD     R5, R2
31
32
33 166006 006304          ASL     R4
34 166010 062704 177750          ADD     #APLR00, R4
35 166014 060504          ADD     R5, R4
36 166016 000404          BR     EX400
37
38 166020          EX300:
39
40 166020 042702 000001          BIC     #BIT0, R2
41 166024 042704 000001          JIC     #BIT0, R4
42
43 166030          EX400:
44
45 166030 032700 000007          BIT     #RNGFGB, R0
46 166034 001001          JNE     EX500
47
48
49 166036 010204          MOV     R2, R4
50
51 166040          EX500:
52
53 166040          EX600:
54
55
56
57

```

```

;* PROCEDURE EXAMINE
;* * IF SERIAL ODT MODE
;* * THEN
;* * * IF THE TARGET IS A REGISTER
;* * * THEN
;* * * * SET TARGET 1 TO MOD 10
;* * * * SET TARGET 2 TO MOD 10
;* * * * SET TARGET 1 =
;* * * * (TARGET * 2) 1 + REG 0 SAVE ADDRESS OFFSET
;* * * * SET TARGET 2 =
;* * * * (TARGET 2 * 2) + R&C 0 SAVE ADDRESS OFFSET
;* * * ELSE
;* * * * CLEAR BIT 0 OF TARGET 1 AND TARGET 2
;* * * END IF
;* * * IF NOT RANGE EXAMINE
;* * * THEN
;* * * * SET TARGET 2 = TARGET 1
;* * * END IF
;* * * DO UNTIL TARGET 1 = TARGET 2
;* * * OR ERROR FLAG = 1
;* * * OR INCREMENTED TARGET 1 = 0
;* * * * GET DATA PER TARGET 1 AND INCREMENT
;* * * * TARGET 1 POINTER

```

```

58 166040 000241          CLC
59 166042 012201          MOV      (R2)+,R1
60
61 166044 000240          NOP
62 166046 103003          BCC      EX700
63
64
65 166050 052703 100000    BIS      #ERRFCB,R3
66
67 166054 000502          BR       EX1300
68
69 166056                    EX700:
70
71 166056 004767 000450    CALL    DISPWD
72
73 166062 020204          CMP      R2,R4
74 166064 101402          BLOS    EX750
75
76
77 166066 042700 000002    BIC      #RNGFCB,R0
78
79 166072                    EX750:
80
81 166072 032700 000002    BIT      #RNGFCB,R0
82 166076 001427          BEQ      EX800
83
84
85 166100 012701 166274    MOV      #CRLF,R1
86 166104 004767 000236    CALL    DISPST
87
88 166110 105703          TSTP    R3
89 166112 100012          BPL      EX760
90
91
92 166114 010201          MOV      R2,R1
93 166116 160501          SUB      R5,R1
94 166120 162701 177750    SUB      #APLR00,R1
95 166124 006301          ASL      R1
96 166126 062701 166303    ADD      #REGDIS,R1
97 166132 004767 000210    CALL    DISPST
98 166136 000403          BPL      EX770
99
100 166140                    EX760:
101
102 166140 010201          MOV      R2,R1
103 166142 004767 000364    CALL    DISPWD
104
105 166146                    EX770:
106
107 166146 012701 166301    MOV      #OPENDS,R1
108 166152 004767 000170    CALL    DISPST
109
110 166156                    EX800:
111
112 166156 005703          TST      R3
113 166160 100404          BMI     EX900
114 166162 005702          TST      R2

```

```

; * * * * IF NXH
; * * * * THEN
; * * * * * SET ERROR FLAG
; * * * * * EXIT EXAMINE (NON STRUCTURED EXIT)
; * * * * END IF
; * * * * DISPLAY DATA
; * * * * IF TARGET 1 = TARGET 2
; * * * * THEN
; * * * * * SET RANGE FLAG = 0
; * * * * END IF
; * * * * IF RANGE EXAMINE
; * * * * THEN
; * * * * * DISPLAY CR LF
; * * * * * IF TYPE IS REGISTER
; * * * * * THEN
; * * * * * * DISPLAY REGISTER NUMBER
; * * * * * ELSE
; * * * * * * DISPLAY ADDRESS
; * * * * * END IF
; * * * * * DISPLAY "/"
; * * * * END IF
; * * * * END UNTIL

```

65

66

```

115 166164 001402          BEQ     EX900
116 166166 020204          CMP     R2,R4
117 166170 101723          BLOS   EX600
118 166172                EX900:
119                        ;* * * SET TARGET BACK 2
120 166172 162702 000002    SUB     #2,R2
121                        ;* * * IF TYPE IS REGISTER
122 166176 105703          TSTB   R3
123 166200 100010          BPL    EX970
124                        ;* * * THEN
125                        ;* * * * RESTORE TARGET 1 TO REGISTER NO.
126 166202 160502          SOB    R5,R2
127 166204 162702 177750    SUB    #APLR00,R2
128 166210 006202          ASR    R2
129                        ;* * * * SET TARGET TO MOD 10
130 166212 022702 000011    CMP    #11,R2
131 166216 101001          JHI    EX950
132 166220 005002          CLR    R2
133 166222                EX950:
134                        ;* * * END IF
135 166222                EX970:
136 166222 000417          BR     EX1300
137                        ;* * ELSE
138 166224                EX1000:
139                        ;* * * SAVE TARGET
140 166224 010246          MOV    R2,-(SP)
141                        ;* * * IF TARGET IS REGISTER
142 166226 105703          TSTB   R3
143 166230 100004          BPL    EX1050
144                        ;* * * THEN
145                        ;* * * * SET TARGET =
146                        ; (2*TARGET) + REGISTER 0 SAVE ADDRESS OFFSET
147 166232 006302          ASL    R2
148 166234 062702 177750    ADC    #APLR00,R2
149 166240 060502          ADD    R5,R2
150                        ;* * * END IF
151 166242                EX1050:
152                        ;* * * GET DATA PER TARGET AND PLACE IN DPR 2
153 166242 000241          CLC
154 166244 011237 175004    MOV    (R2),R#KW.SC2
155                        ;* * * IF NXM
156 166250 000240          NOP
157 166252 103002          BCC    EX1200
158                        ;* * * THEN
159                        ;* * * * SET ERROR FLAG
160 166254 052703 100000    BTS    #ERRFCB,R3
161                        ;* * * END IF
162 166260                EX1200:
163                        ;* * * RESTORE TARGET
164 166260 012602          MOV    (SP)+,R2
165                        ;* * END IF
166 166262                EX1300:
167                        ;* * RETURN
168 166262 000207          RETURN
169                        ;* END EXAMINE
    
```

```
1          .SBTTL DISPST - DISPLAY STRING
2          .ENABLE LC,CBL
3
4          ;
5          ; Module name: DISPST - DISPLAY STRING
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module is a general use utility that sends an ASCII string
17         ; out the console serial line. The display string is specified by
18         ; passing the address of the first character to the routine. The
19         ; end of the string is marked by a null character.
20
21         ;INPUT PARAMETERS:
22
23         ; 1) R1 - Start, of string address
24
25         ;OUTPUT PARAMETERS:
26
27         ; NONE
28
29         ;DATA STRUCTURES USED:
30
31         ; 1) SLUI CSRs
```

```
1
2          000015          CR    ==:    15
3          000012          LF    ==:    12
4
5
6 166264    077    000          ERROR:: .ASCIZ "?
7 166266    015    012    100  PROMPT:: .ASCIZ <CR><LF>"@
8 166272    040    000          SPACE:: .ASCIZ "
9 166274    015    012    000  CRLF:: .ASCIZ <CR><LF>
10 166277    015    000          CRDS:: .ASCIZ <CR>
11 166301    057    000          OPENDS:: .ASCIZ "/"
12 166303    122    060    000  REGDIS:: .ASCIZ "R0"
13 166306          .BLKB 1
14 166307    122    061    000          .ASCIZ "R1"
15 166312          .BLKB 1
16 166313    122    062    000          .ASCIZ "R2"
17 166316          .BLKB 1
18 166317    122    063    000          .ASCIZ "R3"
19 166322          .BLKB 1
20 166323    122    064    000          .ASCIZ "R4"
21 166326          .BLKB 1
22 166327    122    065    000          .ASCIZ "R5"
23 166332          .BLKB 1
24 166333    122    066    000          .ASCIZ "R6"
25 166336          .BLKB 1
26 166337    122    067    000          .ASCIZ "R7"
27 166342          .BLKB 1
28 166343    122    123    000          .ASCIZ "RS"
29
30          .EVEN
31
```

```
1
2 166346
3
4 166346
5
6 166346
7
8
9 166346 010046
10 166350 004767 005240
11 166354 012600
12
13 166356 105737 177564
14 166362 100371
15 166364 032703 000040
16 166370 001366
17
18 166372 112137 177566
19
20 166376 105711
21 166400 001362
22
23 166402 000207
24
```

```
DISPST::
DS100:
DS200:
```

```
MOV    R0,-(SP)
CALL   CHKCHR
MOV    (SP)+,R0
TSTB   @#XCSR1A
BPL    DS200
BIT    #XOFFGB,R3
BNE    DS200
MOVB   (R1)+,@#XBUF1A
TSTB   (R1)
BNE    DS100
RETURN
```

```
;* PROCEDURE DISPLAY STRING
;* * DO UNTIL NULL CHARACTER POINTED TO
;* * * DO UNTIL TRANSMIT BUFFER EMPTY
;* * * OR XOFF FLAG = 1
;* * * * TEST FOR INPUT
;* * * END UNTIL
;* * * SEND CHARACTER PER POINTER
;* * END UNTIL
;* * RETURN FROM CALL
;* END DISPLAY STRING
```



```
1          .SBTTL DATCOM - GET DATA/COMMAND
2          .ENABLE LC,GBL
3
4          ;
5          ; Module name: DATCOM - GET DATA/COMMAND
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ; Functional Description:
14         ;
15         ; This module is used by the serial ODT monitor. It poles SLU1
16         ; for valid data and returns when a CR, LF OR ^ are received
17         ; or on an error.
18
19         ;Input Parameters:
20
21         ; NONE
22
23         ;Output Parameters
24
25         ; 1) R0 - COMMAND RECEIVED
26         ; 2) R4 - INPUT DATA
27         ; 3) R3 - BIT ERRFCB, ERROR FLAG: 1 = ON ERROR, NOT ALTERED IF NO ERRORS
28         ; 4) R3 - BIT DARFCB, DATA RECV'D WITH COMMAND FLAG: 1 = YES, 0 = NO
29
30         ;DATA STRUCTURES USED
31
32         ; NONE
33
34         ;Routines Used
35
36         ; 1) ACCUM
37         ; 2) CHKCHR
38
```

```

1
2 166404          DATCOM::          ;* PROCEDURE GET DATA/COMMAND
3
4                ;* * CLEAR DATA RECEIVED FLAG
5 166404 042703 000003          BIC    #<DARFGB I DCDFGB>,R3 ;* * CLEAR DATA/COMMAND DONE FLAG
6                ;* * CLFAR ACCUMULATED NUMBER
7 166410 005004          CLR     R4    ;* * CLFAR ACCUMULATED NUMBER
8
9 166412          DA100:            ;* * DO UNTIL DONE FLAG SET
10               ;* * * DO UNTIL NON NUMERIC INPUT
11 166412          DA200:            ;* * * * GET INPUT
12               ;* * * * * IF NUMERIC INPUT
13 166412 004767 005134          CALL   GFTIN ;* * * * * IF NUMERIC INPUT
14               ;* * * * * ACCUMULATE NUMBER
15 166416 103403          BCS     DA370 ;* * * * * ACCUMULATE NUMBER
16               ;* * * * * SET NON NUMERIC FLAG = 0
17 166420 004767 005114          CALL   ACCUM ;* * * * * SET NON NUMERIC FLAG = 0
18               ;* * * * * END IF
19 166424 000241          CLC
20               ;* * * * * END IF
21 166426          DA370:            ;* * * * * END UNTIL
22               ;* * * * * END UNTIL
23 166426 103371          BCC     DA200 ;* * * * * END UNTIL
24               ;* * * * * CASE CHARACTER INPUT
25               ;* * * * * WHEN CR
26 166430 122700 000015          CMPB   #15,R0
27 166434 001406          BEQ    DA400 ;* * * * * WHEN CR
28               ;* * * * * OR LF
29 166436 122700 000012          CMPB   #12,R0 ;* * * * * OR LF
30 166442 001403          BEW    DA400 ;* * * * * OR LF
31               ;* * * * * OR ^
32 166444 122700 000136          CMPB   #^,R0 ;* * * * * OR ^
33 166450 001003          BNE    DA500 ;* * * * * OR ^
34 166452          DA400:            ;* * * * * SET DONE FLAG
35               ;* * * * * SET DONE FLAG
36 166452 052703 000001          BIS    #DCDFGB,R3 ;* * * * * SET DONE FLAG
37 166456 000402          BR     DA600 ;* * * * * SET DONE FLAG
38               ;* * * * * ELSE
39 166460          DA500:            ;* * * * * ELSE
40               ;* * * * * SET ERROR FLAG
41               ;* * * * * SET DONE FLAG
42 166460 052703 100001          BIS    #<ERRFGB I DCDFGB>,R3 ;* * * * * SET ERROR FLAG
43               ;* * * * * SET DONE FLAG
44 166464          DA600:            ;* * * * * SET DONE FLAG
45               ;* * * * * END CASE
46 166464 032703 000001          BIT    #DCDFGB,R3 ;* * * * * END CASE
47 166470 001750          BEQ    DA100 ;* * * * * END UNTIL
48 166472          DA700:            ;* * * * * END UNTIL
49               ;* * * * * RETURN
50 166472 000207          RETURN ;* * * * * RETURN
51               ;* * * * * END GET DATA/COMMAND
52

```

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```
1          .SBTTL DEPOS - DEPOSITE
2          .ENABLE GBL,LC
3
4          ;
5          ; Module name: DEPOS - DEPOSIT
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module is used by both the Q bus ODT and the serial ODT monitors.
17         ; It deposits the passed data in the register or memory location
18         ; specified.
19
20         ;Input Parameters:
21
22         ; 1) R2 - ADDRESS
23         ; 2) R4 - DATA
24         ; 3) R3 bit REGFGB - Register flag
25
26         ;Output Parameters
27
28         ; 1) R3, BIT (ERRFGB) - ERROR FLAG, BIT = 1 (ERROR), BIT NOT ALTERED IF NO ERROR
29
30         ;DATA STRUCTURES USED
31
32         ; 1) USER REGISTER SAVE AREA
33
34         ;Routines Used
35
36         ; NONE
37
38         ;Global Symbols Defined
39
40         ; NONE
41         ;
```

```
1
2 166474
3 166474 010246
4
5 166476 105703
6 166500 100004
7
8
9 166502 006302
10 166504 060502
11 166506 062702 177750
12
13 166512
14
15 166512 000241
16 166514 010412
17 166516 000240
18
19 166520 103002
20
21
22 166522 052703 100000
23
24 166526
25
26 166526 012602
27 166530 000207
28
```

```
DEPOS::
MOV R2,-(SP)
TSTR R3
BPL DE50
ASL R2
ADD R5,R2
ADD #APLR00,R2
DE50:
CLC
MOV R4,(R2)
NOP
BCC DF200
BIS #ERPFG8,R3
DF200:
MOV (SP)+,R2
RETURN
```

```
;* PROCEDURE
;* * IF TARGET IS A REGISTER
;* * THEN
;* * * CONVERT REGISTER NO. TO ADDRESS
;* * FWD IF
;* * DEPOSIT DATA AT SUPPLIED ADDRESS
;* * IF NXH
;* * THEN
;* * * SET ERROR FLAG
;* * END IF
;* * RETURN FROM CALL
;* END DEPOSIT
```

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```
1          .SBTTL  DISPWD - DISPLAY WORD
2          .FNABLE LC,GBL
3
4          ;
5          ; Module name: DISPWD - DISPLAY WORD
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module is a general use utility that converts an 16 bit
17         ; value to an ASCII string and sends it out the console serial
18         ; line.
19
20         ;INPUT PARAMETERS:
21
22         ; 1) R1 - DATA WORD TO BE DISPLAYED
23
24         ;OUTPUT PARAMETERS:
25
26         ; NONE
27
28         ;DATA STRUCTURES USED:
29
30         ; 1) SLU1 CSRs
```

```

1
2
3 166532          DISPWD::          ;* PROCEDURE DISPLAY WORD
4
5 166532 010046          MOV      R0,-(SP)          ;* * SAVE REGISTERS USED
6 166534 010246          MOV      R2,-(SP)
7
8 166536 012702 000006          MOV      #6,R2          ;* * SET CHARACTER COUNT = 6
9
10
11 166542 005000          CLR      R0          ;* * SHIFT HIGH BIT OF DISPLAY WORD INTO
12 166544 006301          ASL      R1          ;   NEXT NUMBER BUFFER
13 166546 005500          ADC      R0
14
15 166550          DI100:          ;* * DO UNTIL CHARACTER COUNT = 0
16
17 166550 062700 000060          ADD      #60,R0          ;* * * CONVERT NEXT NUMBER BUFFER TO ASCII
18
19 166554          DI200:          ;* * * DO UNTIL TRANSMIT BUFFER EMPTY
20
21
22 166554 010046          MOV      R0,-(SP)          ;* * * OR XOFF FLAG = 1
23 166556 004767 005032          CALL    CHKCHR          ;* * * * CHECK FOR INPUT
24 166562 012600          MOV      (SP)+,R0
25
26 166564 105737 177564          TSTB    @#XCSR1A          ;* * * END UNTIL
27 166570 100371          BPL     DI200
28 166572 032703 000040          BIT     #XOFFGB,R3
29 166576 001366          BNE     DI200
30
31 166600 110037 177566          MOVB    R0,@#XBUF1A          ;* * * DISPLAY NUMBER
32
33 166604 005000          CLR     R0          ;* * * CLEAR NEXT NUMBER BUFFER
34
35
36 166606 006301          ASL     R1          ;* * * SHIFT NEXT THREE HIGH BITS OF DISPLAY
37 166610 005500          ADC     R0          ;   WORD ONTO NEXT NUMBER BUFFER
38 166612 006300          ASL     R0
39 166614 006301          ASL     R1
40 166616 005500          ADC     R0
41 166620 006300          ASL     R0
42 166622 006301          ASL     R1
43 166624 005500          ADC     R0
44
45 166626 005302          DEC     R2          ;* * * DECREMENT CHARACTER COUNT
46
47 166630 001347          BNE     DI100          ;* * END UNTIL
48
49 166632 012602          MOV     (SP)+,R2          ;* * RESTORE REGISTERS
50 166634 012600          MOV     (SP)+,R0
51
52 166636 000207          RETURN          ;* * RETURN FROM CALL
53
;* END DISPLAY WORD

```

```
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43
44
45
46
```

```

                .SBTTL ABAUD - AUTO BAUD
                .ENABLE LC,GBL

;
; Module name: ABAUD - AUTO BAUD
;
; System: KXT11-CA Native Firmware
;
;
; Functional Description:
;
; This module performs the auto baud function on the console serial line.
; It is used by the serial ODT monitor. The decision whether to attempt
; to auto baud is made in this module. If the programmable baud rate
; enable bit of the DLART is set or writing to the baud rate bits
; does not change there value, the auto baud function is not performed.
; If the auto baud function is performed this mode will continue to
; attempt to determine the baud rate until it succeeds.
;
; The auto baud function is performed by setting the baud rate to 2400
; and comparing the input character data to that of a table. This
; character must be a CR and be sent at a baud rate within the range of
; 300 to 9600 (in doubling increments).
;
; The baud rate table has two entries for 4800 baud to eliminate the
; 4800 baud detection problem that exists for the Falcon.
;
; Input Parameters:
;
; NONE
;
; Output Parameters
;
; NONE
;
; DATA STRUCTURES
;
; SLU1 CSR (XCSR1A)
;
; Routines Used
;
; NONE
```

1					
2	000002	B300	=	2	;300 BAUD DLART RATE CODE
3	000012	B600	=	12	;600 " " " "
4	000022	B1200	=	22	;1200 " " " "
5	000032	B2400	=	32	;2400 " " " "
6	000042	B4800	=	42	;4800 " " " "
7	000052	B9600	=	52	;9600 " " " "
8					
9					
10	166640 200	INDATA: .BYTE		200	;RECEIVE DATA AT 300 BAUD/BAUD RATE CODE
11	166641 002	.BYTE		B300	
12	166642 170	.BYTE		170	; " " " 600 " " "
13	166643 012	.BYTE		B600	
14	166644 346	.BYTE		346	; " " " 1200 " " "
15	166645 022	.BYTE		B1200	
16	166646 015	.BYTE		15	; " " " 2400 " " "
17	166647 032	.BYTE		B2400	
18	166650 362	.BYTE		362	; " " " 4800 " " "
19	166651 042	.BYTE		B4800	
20	166652 363	.BYTE		363	; " " " 4800 " " "
21	166653 042	.BYTE		B4800	
22	166654 377	.BYTE		377	; " " " 9600 " " "
23	166655 052	ENDTAB: .BYTE		B9600	
24		.EVEN			

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1


```

2
3 166656                                ABAUD::                                ;* PROCEDURE AUTO BAUD
4                                          ;* * IF DLART XCSR PBRE BIT = 0
5 166656 032737 000002 177564          BIT    #2,@#XCSR1A
6 166664 001041                          BNE    A9600
7                                          ;* * THEN
8                                          ;* * * SET PBE BIT = 1
9 166666 052737 000002 177564          BIS    #2,@#XCSR1A
10                                         ;* * * IF PBE READS BACK AS 1
11 166674 032737 000002 177564          BIT    #2,@#XCSR1A
12 166702 001432                          BEQ    A8500
13                                         ;* * * THEN
14                                         ;* * * * SET BAUD RATE TO 2400
15 166704 012737 000032 177564          MOV    #B2400,@#XCSR1A
16                                         ;* * * * DO UNTIL BAUD RATE FOUND
17 166712                                AB100:                                ;* * * * * DELAY .25 SECONDS
18                                         ;* * * * *
19 166712 005000                          CLR    R0
20 166714 077001                          SOB    R0,.
21                                         ;* * * * * CLEAR RECEIVE BUFFER
22 166716 105737 177562                  TSTB   @#RBUF1A
23                                         ;* * * * * DO UNTIL DATA RECEIVED
24 166722                                AB200:                                ;* * * * * FND UNTIL
25                                         ;* * * * *
26 166722 105737 177560                  TSTB   @#RCSR1A
27 166726 100375                          BPL    A8200
28                                         ;* * * * * GET INPUT DATA
29 166730 113700 177562                  MOVB   @#RBUF1A,R0
30                                         ;* * * * * SET POINTER TO TOP OF TABLE
31 166734 012701 166640                  MOV    #INDATA,R1
32                                         ;* * * * * DO WHILE DATA <> (POINTER) OR LAST VALUE
33 166740 120021                          AB300:  CMPR   R0,(R1)+
34 166742 001405                          BEQ    A8400
35 166744 022701 166655                  CMP    #ENDTAB,R1
36 166750 001760                          B&Q    A8100 ;(NON STRUCTUPED BRANCH FOR CODE OPTIMIZATION)
37                                         ;* * * * * INCREMENT POINTER
38 166752 005201                          INC    R1
39                                         ;* * * * * END WHILE
40 166754 000771                          BR     AB300
41                                         ;* * * * * FND UNTIL (CONDITION TESTED ABOVE TO SAVE CODE)
42 166756                                AB400:                                ;* * * * * SET BAUD RATE PER TABLE
43                                         ;* * * * *
44 166756 111137 177564                  MOVB   (R1),@#XCSR1A
45                                         ;* * * * * DELAY .5 SECONDS
46 166762 005000                          CLR    R0
47 166764 077001                          SOB    R0,.
48 166766 077001                          SOB    R0,.
49                                         ;* * * END IF
50 166770                                AB500:                                ;* * END IF
51                                         ;* *
52 166770                                AB600:                                ;* * RETURN
53                                         ;* *
54 166770 000207                          RETURN
55                                         ;* END AUTO BAUD

```

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```
1  
2          .SBTTL GOPROC - GO/PROCEED  
3          .ENABLE LC,GBL  
4  
5          ;  
6          ; Module name: GOPROC - GO/PROCEED  
7          ;  
8          ; System: KXT11-CA Native Firmware  
9          ;  
10         ;  
11         ;  
12         ;  
13         ;  
14         ;  
15         ; Functional Description:  
16         ;  
17         ; This module performs the go and the proceed functions for both  
18         ; the serial and Q bus ODT. It has separate entry points for  
19         ; each Go and PROCEED. The difference being that a PC value  
20         ; is passed to the module for the GO function. This module  
21         ; tests the user stack area and the user PC value. If a NXH is  
22         ; encountered at the user SP the module returns from the call.  
23         ; If no error is encountered control is passed to the user application.  
24  
25         ;Input Parameters:  
26  
27         ; 1) R0 = USER PC VALUE FOR GO COMMAND  
28  
29         ;Output Parameters  
30  
31         ; NONE  
32  
33         ;Routines Used  
34  
35         ; NONE  
36
```

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08

```

1
2
3 166772          GO::
4
5
6 166772 042700 000001      BIC      #8BIT0,R0      ;* PROCEDURE GO/PROCEED
7                                ;* * IF GO
8 166776 010065 177766      MOV      R0,APLPCO(R5)  ;* * THEN
9                                ;* * * CLEAR ADDRESS BIT0 OF TARGET
10 167002 005065 177770     CLR      APLPSO(R5)    ;* * * SET APPLICATION PC = ADDRESS PASSED
11                                ;* * * SET APPLICATION PSW = 0
12 167006 000005           RESET      ;* * * RESET IOP
13                                ;* * * END IF
14 167010          PROC::
15                                ;* * TEST USER SP FOR NXM AND WRITABLE
16 167010 052737 010000 175002  BIS      #KXSNXF,@#KW.STA
17 167016 016500 177764     MOV      APLSPO(R5),R0
18 167022 012701 052525     MOV      #52525,R1
19 167026 000241           CLC
20                                ;* * IF TEST OF USER SP PASSES
21
22 167030 010160 177776     MOV      R1,-2(R0)
23 167034 000240           NOP
24 167036 103457           BCS     GP300
25 167040 010160 177774     MOV      R1,-4(R0)
26 167044 000240           NOP
27 167046 103453           BCS     GP300
28 167050 020160 177776     CMP      R1,-2(R0)
29 167054 001050           BNE     GP300
30 167056 020160 177774     CMP      R1,-4(R0)
31 167062 001045           BNE     GP300
32                                ;* * THEN
33                                ;* * * SET LEDS TO NON NATIVE CODE STATE
34 167064 012700 000000     MOV      #NNCED,R0
35 167070 004767 000104     CALL    SETLED
36                                ;* * * ENABLE NXM'S TO TRAP TO 4
37 167074 042737 010000 175002  BIC      #KXSNXF,@#KW.STA
38                                ;* * * PUT APPLICATION PC AND PS ON APPLICATION STACK
39 167102 016500 177764     MOV      APLSPO(R5),R0
40 167106 016540 177770     MOV      APLPSO(R5),-(R0)
41 167112 016540 177766     MOV      APLPCO(R5),-(R0)
42 167116 010065 177764     MOV      R0,APLSPO(R5)
43                                ;* * * SET STACK POINTER TO APPL. RO SAVE ADDR.
44 167122 012706 177750     MOV      #APLR00,SP
45 167126 060506           ADD     R5,SP
46                                ;* * * RESORE USER REGISTERS R0 - R5
47 167130 012600           MOV     (SP)+,R0
48 167132 012601           MOV     (SP)+,R1
49 167134 012602           MOV     (SP)+,R2
50 167136 012603           MOV     (SP)+,R3
51 167140 012604           MOV     (SP)+,R4
52 167142 012605           MOV     (SP)+,R5
53                                ;* * * RESTGRE USER SP
54 167144 011606           MOV     (SP),SP
55                                ;* * * ENABLE DUAL PORT RAM
56 167146 052737 000100 177530  BIS      #KXSDEN,@#KW.CSD
57                                ;* * * CLEAR SERIAL ODT, QBUS ODT AND NXM FLAGS OF

```

```

58                                     ; STATUS REGISTER
59 167154 042737 010307 175002      BIC  #<KXSSOF I KXSQOF I KXSHXF I KMSSTF>,@#KW.STA
60                                     ;* * * SET STATUS REGISTER TO NON NATIVE CODE STATE
61 167162 052737 000007 175002      BIS  #KPSNNC,@#KW.STA
62                                     ;* * * CLEAR COMMAND REGISTER
63 167170 005037 175000      CLR  @#KW.CMD
64                                     ;* * * RETURN TO APPLICATION (NON STRUCTURED EXIT)
65 167174 000002      RTI
66                                     ;* * END IF
67 167176                                     GP300:
68                                     ;* * RETURN FROM CALL
69 167176 000207      RETURN
70                                     ;* END GO/PROCEED
  
```

```

1                                     .SBTTL SETLED - SET LEDES
2                                     .ENABLE LC,GBL
3
4                                     ;
5                                     ; Module name: SETLED - SET LEDES
6                                     ;
7                                     ; System: KXT11-CA Native Firmware
8                                     ;
9                                     ;
10                                    ;
11                                    ;
12                                    ;
13                                    ;
14                                    ; Functional Description:
15                                    ;
16                                    ; This mode sets the LED display to the state pass to it as a parameter.
17                                    ; It only changes the state of the LEDs if they are not currently
18                                    ; displaying an error or if the new display is to be Fatal Error.
19                                    ; There are two entry points to this routine. SETLED is the entry
20                                    ; used if the return address is on the stack. SETLDJ is used if there
21                                    ; is not a usable stack and the return address is in R1.
22                                    ;
23                                    ; Input Parameters:
24                                    ;
25                                    ; 1. New LED State (R0)
26                                    ; 2. Return address if SETLDJ entry is used (R1)
27                                    ;
28                                    ; Output Parameters
29                                    ;
30                                    ; NONE
31                                    ;
32                                    ; Data structures used
33                                    ;
34                                    ; 1. LED State (KXTCSR C, bits 3 - 0)
35                                    ;
36                                    ; Routines Used
37                                    ;
38                                    ; NONE
39                                    ;
  
```

1	000017	LS0	==:	17	;LED STATE 0
2	000016	LS1	==:	16	; " " 1
3	000015	LS2	==:	15	; " " 2
4	000014	LS3	==:	14	; " " 3
5	000013	LS4	==:	13	; " " 4
6	000012	LS5	==:	12	; " " 5
7	000011	LS6	==:	11	; " " 6
8	000010	LS7	==:	10	; " " 7
9	000007	LS8	==:	7	; " " 8
10	000006	LS9	==:	6	; " " 9
11	000005	LS10	==:	5	; " " 10
12	000004	LS11	==:	4	; " " 11
13	000003	LS12	==:	3	; " " 12
14	000002	LS13	==:	2	; " " 13
15	000001	LS14	==:	1	; " " 14
16	000000	LS15	==:	0	; " " 15
17					
18	000017	LEDTS0	==:	LS0	;LED TEST DISPLAY
19	000017	FERRD	==:	LS0	;FATAL ERROR DISPLAY
20	000010	NFERRD	==:	LS7	;NON FATAL ERROR DISPLAY
21	000011	UROM0D	==:	LS6	;USER ROM 0 FAILED DISPLAY
22	000012	UROM1D	==:	LS5	;USER ROM 1 FAILED DISPLAY
23	000013	S1LBD	==:	LS4	;SLU1 LOOP BACK TEST FAILED DISPLAY
24	000014	S2ALBD	==:	LS3	;SLU2 CHAN A LOOP BACK TEST FAILED DISPLAY
25	000015	S2BLBD	==:	LS2	;SLU2 CHAN B LOOP BACK TEST FAILED DISPLAY
26	000016	PARLBD	==:	LS1	;PARALLEL LOOP BACK TEST FAILED DISPLAY
27					
28	000007	PUTSDS	==:	LS8	;POWER UP TESTS RUNNING
29	000006	CSTMD	==:	LS9	;CONTINUOUS SELF TEST MODE DISPLAY
30	000005	QODTMD	==:	LS10	;Q BUS ODT MODE DISPLAY
31	000004	SODTMD	==:	LS11	;SERIAL ODT MODE DISPLAY
32	000003	WAITD	==:	LS12	;WAIT MODE DISPLAY
33	000002	DMAED	==:	LS13	;EXECUTING DMA LOAD DISPLAY
34	000001	PRIFD	==:	LS14	;EXECUTING PRIMARY BOOTSTRAP DISPLAY
35	000000	NNCED	==:	LS15	;EXECUTING NON NATIVE CODE DISPLAY

```

1
2
3
4 167200          SETLED::
5
6
7 167200 005001          CLR      R1
8
9 167202          SETLDJ::
10
11 167202 022700 000017          CMP      #FERRD,R0
12 167206 001405          BEQ      SE100
13
14 167210 132737 000010 177524          BITR     #KXSLDJ,@#KW.CSC
15 167216 001401          BEQ      SE100
16 167220 000410          BR       SE200
17
18 167222          SE100:
19
20 167222 110037 177524          MOVR     R0,@#KW.CSC
21
22 167226 122700 000017          CMPB     #FERRD,R0
23 167232 001003          BNE     SE150
24
25
26 167234 052737 000040 175002          BIS     #KX$FEF,@#KW.STA
27
28 167242          SE150:
29
30 167242          SE200:
31
32 167242 005701          TST     R1
33 167244 001001          BNE     SE300
34
35
36 167246 000207          RETURN
37
38 167250          SE300:
39
40 167250 000111          JMP     (R1)
41
42

```

83

```

1          .SBTTL TRAP4 - TRAP 4 EMULATOR
2
3          .ENABLE LC,GBL
4          ;
5          ; Module name: TRAP4 - TRAP 4 EMULATOR MODULE
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module emulates the Trap to 4. This emulation
17         ; is performed by placing PSW and the vector address onto the stack
18         ; and performing an RTI. If the stack pointer is not pointing
19         ; to writeable memory (but not NXM) this routine will force a
20         ; stack NXM situation where the Restart Interrupt handler (RESTRT)
21         ; will re-establish the stack and retry the trap.
22         ;

```

84

```

1
2 167252          TRAP4::
3
4 167252 013746 000006      MOV    @#6,-(SP)
5 167256 013746 000004      MOV    @#4,-(SP)
6
7 167262 023766 000006 000002  CMP    @#6,2(SP)
8 167270 001004          BNE    TR410
9 167272 023716 000004      CMP    @#4,(SP)
10 167276 001001          BNE    TR410
11
12
13 167300 000002          RTI
14
15 167302          TR410:
16
17 167302 052737 004000 175002  BIS    #KXSSXT,@#KW.STA
18 167310 005737 177776      TST    @#177776 ;(FORCE A NXM RESTART INT.)
19
20

```

;* PROCEDURE TRAP4
 ;* * SET UP STACK FOR TRAP TO 4
 ;* * IF STACK IS POINTING TO RAM
 ;* * THEN
 ;* * * EMULATE TRAP (NON STRUCTURED EXIT)
 ;* * ELSE
 ;* * * FAKE A STACK NXM SITUATION (NON STRUCTURED EXIT)
 ;* * END IF
 ;* END TRAP4

```

1          .SBTTL TRAP10 - TRAP 10 EMULATOR
2
3          .FNABLE LC,GBL
4          ;
5          ; Module name: TRAP10 - TRAP 10 EMULATOR MODULE
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module emulates the trap to 10. The trap emulation
17         ; is performed by placing the vector address and PSW on the stack
18         ; and performing an RTI. If the stack pointer is not pointing
19         ; to writable memory (but not NXM) this routines will force a
20         ; stack NXM situation where the Restart Interrupt handler (RESTRT)
21         ; will re-establish the stack and retry the trap.
22

```

85

```

1
2 167314          TRAP10::          ;* PROCEDURE TRAP4
3
4 167314 013746 000012          MOV    @#12,-(SP)          ;* * SET UP STACK FOR TRAP TO 4
5 167320 013746 000010          MOV    @#10,-(SP)
6
7 167324 023766 000012 000002    CMP    @#12,2(SP)          ;* * IF STACK IS POINTING TO RAM
8 167332 001004          BNE    TR1010
9 167334 023716 000010          CMP    @#10,(SP)
10 167340 001001          BNE    TR1010
11
12
13 167342 000002          RTI          ;* * THEN
14
15 167344          TR1010:          ;* * * EMULATE TRAP (NON STRUCTURED EXIT)
16
17 167344 052737 004000 175002    BIS    #KXSSXT,@#KW.STA          ;* * ELSE
18 167352 005737 177776          TST    @#177776 ;(FOPCE A NXM RESTART INT.) ;* * * FAKE A STACK NXM SITUATION (NON STRUCTURED EXIT)
19
20

```



```
1          .SBTTL TRAP24 - TRAP 24 EMULATOR
2
3          .FNABLE LC,GBL
4          ;
5          ; Module name: TRAP24 - TRAP 24 EMULATOR MODULE
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module emulates the Trap to 24. This emulation
17         ; is performed by placing data at locations 26 into the PSW
18         ; and 24 into the PC.
19         ;
```

98

```
1
2 167356          TPAP24::          ;* PROCEDURE TRAP24
3
4 167356 106437 000026          MTPS @#26          ;* * MOVE CONTENTS OF 26 TO PSW
5
6 167362 013707 000024          MOV @#24,PC          ;* * MOVE CONTENTS OF 24 TO PC
7
9          ;* END TRAP24
```

```

1          .SBTTL TRAPX - TRAP COMMAND EMULATOR
2
3          .ENABLE LC,GBL
4          ;
5          ; Module name: TRAPX - TRAP COMMAND EMULATOR MODULE
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ; Functional Description:
14         ;
15         ;
16         ; This module emulates the Trap specified by the DPR. This emulation
17         ; is performed by placing data in DPR register 2 into the PSW
18         ; and DPR register 3 into the PC.
19         ;
20         ;
21         ; * PROCEDURE TRAPX
22         TRAPX::
23         CLR     @*KW.CMD          ; * * CLEAR COMMAND REGISTER
24         ;
25         MTPS   @*KW.SC3         ; * * SET PSW TO DPR REGISTER 3
26         ;
27         MOV    @*KW.SC2,PC      ; * * JUMP TO ADDRESS SPEC. IN DPR REGISTER 2
28         ;
29         ; * END TRAPX

```

```
1
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```

.SBTTL WAITST - WAIT FOR COMMAND STATE
.ENABLE LC,GBL

; Module name: WAITST
; System: KXT11-CA Native Firmware

; Functional Description:
; This module is used to place the IOP in the wait state. In this state
; the IOP waits for a command to be received from the Q bus.
; The LED if not displaying an error will be set to the wait state
; display. The state field of status register of the DPR will be
; set to the wait state if the Root/Self Test Switch is not set to 10.
; If the switch is set to 10 then the state field is set to the Q Bus
; controlled test state. The routine continues to loop setting the LEDs
; and the state field of the status register so that if the serial ODT
; mode is entered via Break, while in this routine and a Proceed
; command is executed the LED display and state field will be correct.

; Input Parameters:
; NONE

; Output Parameters
; NONE

; Routines Used
; NONE

```

1
2 167402
3
4 167402
5
6 167402 012700 000003
7 167406 004767 177566
8
9 167412 013700 175002
10 167416 042700 000007
11
12 167422 113701 177522
13 167426 142701 177417
14 167432 122701 000240
15 167436 001003
16
17
18
19 167440 052700 000002
20 167444 000402
21 167446
22
23
24 167446 052700 000004
25
26 167452
27
28 167452 010037 175002
29
30 167456 000751
31
    WAITST::
    WA100:
        MOV #WAITD,R0
        CALL SETLED
    WA200:
        BIS #MPSQTS,R0
        BR WA300
    WA300:
        MOV R0,@#KW.STA
        BR WA100
; * PROCEDURE WAITST
; * * DO UNTIL INTERRUPTED
; * * * SET LED DISPLAY TO WAIT STATE
; * * * GET STATUS REGISTER
; * * * IF THE BOOT/SELF TEST SWITCH = 10
; * * * THEN
; * * * * SET STATE FIELD OF STATUS REG. TO
; * * * * QBUS CONTROLLED TEST STATE
; * * * ELSE
; * * * * SET STATE FIELD OF STATUS REG. TO WAIT STATE
; * * * END IF
; * * * * WRITE STATUS REGISTER DATA
; * * END UNTIL
; * END WAITST
    
```

68

```
1          .SBTTL QCOMIN - Q BUS COMMAND INTERP.
2          .ENABLE GBL,LC
3
4          ;
5          ; Module name: QCOMIN - Q BUS COMMAND INTERPRITOR
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module decodes the Q bus commands received through the command
17         ; register of the dual port RAM. Once a valid command is recognised
18         ; the appropriate routine is called. If the command received is a test
19         ; command the test command decode routine (DECTST) is jumped to.
20         ;
21         ; Input Parameters:
22         ;
23         ;     NONF
24         ;
25         ; Output Parameters
26         ;
27         ;     NONF
28         ;
29         ; Data Structures Used
30         ;
31         ;     1. IOP COMMAND REGISTER
32         ;
33         ;     2. IOP STATUS REGISTER
34         ;
35         ; Routines Used
36         ;
37         ;     1. REINIT (JMP)
38         ;
39         ;     2. DECTST (JMP)
40         ;
41         ;     3. WAITST (JMP)
```

```

1
2 167460          QCOMIN::          ;* PROCEDURE Q BUS COMMAND INTERPRETER
3
4          ;* * CLEAR COMMAND ERROR AND DMA LOAD ERROR
5 167460 042737 140000 175002      BIC  #<KXSCHE ! KXSDME>,@#KW.STA          ;* * IF IN SERIAL ODT MODE
6          ;* * THEN
7 167466 032737 000100 175002      BIT  #KXSSDF,@#KW.STA
8 167474 001406      BEQ  QC50          ;* * SET COMMAND ERROR BIT OF STATUS REGISTER
9          ;* * *
10         ;* * * CLEAR COMMAND REGISTER
11 167476 052737 100000 175002      BIS  #KXSCME,@#KW.STA
12         ;* * * RETURN FORM INTERRUPT
13 167504 005037 175000      CLR  @#KW.CMD
14         ;* * * END IF
15 167510 000002      RTI  ;(NON STRUCTURED EXIT)
16         ;* * *
17 167512          QC50:          ;* * IF QODT FLAG OF STATUS RFGISTER = 1
18         ;* * THEN
19 167512 032737 000200 175002      BIT  #KXSQDF,@#KW.STA
20 167520 001401      BEQ  QC70          ;* * UNBLOCK QODT WAIT FOR COMMAND
21         ;* * *
22         ;* * * END IF
23 167522 000002      RTI  ;(NON STRUCTURED EXIT)
24         ;* * *
25 167524          QC70:          ;* * IF TEST/COMMAND BIT = 0
26         ;* * THEN
27 167524 032737 100000 175000      BIT  #BIT15,@#KW.CMD
28 167532 001147      BNE  QC500        ;* * CASE COMMAND
29         ;* * * WHEN Q BUS ODT
30         ;* * * AND STATUS REGISTER SERIAL ODT FLAG = 0
31         ;* * * ENTER ODT Q BUS ODT MODE
32 167534 022737 000010 175000      CMP  #KXSODC,@#KW.CMD
33 167542 001006      BNE  QC100        ;* * * WHEN RE-INITIALIZE
34         ;* * * AND DPR REGISTER 3 = 0 THROUGH 6 AND ID
35 167544 032737 000100 175002      BIT  #KXSSDF,@#KW.STA
36 167552 001002      BNE  QC100        ;* * * OR DPR REGISTER 3 = 8
37         ;* * *
38         ;* * *
39 167554 000167 001652      JMP  QODTM          ;* * *
40         ;* * *
41 167560 022737 000004 175000      CMP  #KXSINC,@#KW.CMD
42 167566 001024      BNE  QC200        ;* * *
43         ;* * *
44         ;* * *
45 167570 022737 000006 175006      CMP  #6,@#KW.SC3
46 167576 103407      BLD  QC120
47 167600 013700 177522      MOV  @#KW.CSB,R0
48 167604 042700 177417      BIC  #~C<KXSSWS>,R0
49 167610 022700 000160      CMP  #<7*16.>,R0
50 167614 101004      BHI  QC150
51         ;* * *
52 167616          QC120:          ;* * *
53 167616 022737 000010 175006      CMP  #8,@#KW.SC3
54 167624 001005      BNE  QC200
55 167626          QC150:          ;* * *
56         ;* * *
57 167626 042737 000100 177520      BIC  #KXSDFN,@#KW.CSA

```

```

58                                     ;* * * * RE-INITIALIZ
59                                     ; (NON STRUCTURED JUMP TO POWERUP MODULE RE-INITIALIZE
60 167634 000167 003156                JMP    REINIT
61                                     ;* * * * WHEN DMA LOAD
62 167640 022737 000002 175000 QC200: CMP    #KXSDMC,@#KW.CMD
63 167646 001004                       BNE    QC300
64                                     ;* * * * REMOVE RETURN ADDR. AND PS FROM STACK
65 167650 062706 000004                ADD    #4,SP
66                                     ;* * * * PERFORM DMA TRANSFER
67                                     ; (NON STRUCTURED JUMP TO DMA LOADER MODULE)
68 167654 000167 001152                JMP    DMALD
69                                     ;* * * * WHEN TRAP COMMAND
70 167660 022737 000001 175000 QC300: CMP    #KXSTRC,@#KW.CMD
71 167666 001023                       BNE    QC400
72                                     ;* * * * IF PC VALUE IN DPR REGISTER 2 IS EVEN
73 167670 032737 000001 175004        BIT    #BIT0,@#KW.SC2
74 167676 001016                       BNE    QC380
75                                     ;* * * * THEN
76                                     ;* * * * * SET LEDS TO NON NATIVE CODE STATE
77 167700 012700 000000                MOV    #NNCED,R0
78 167704 012701 167714                MOV    #QC350,R1
79 167710 000167 177266                JMP    SETLQJ
80 167714                               QC350:
81                                     ;* * * * * SET STATUS REGISTER NON NATIVE CODE STATE
82 167714 042737 000007 175002        BIC    #KMSSTF,@#KW.STA
83 167722 052737 000007 175002        BIS    #KPSNNC,@#KW.STA
84                                     ;* * * * * EMULATE TRAP AT ADDRESS
85                                     ; PER DUAL PORT REGISTER 2
86                                     ; SET PSW PER DUAL PORT REGISTER 3
87                                     ; (NON STRUCTURED EXIT)
88 167730 000167 177432                JMP    TRAPX
89                                     ;* * * * END IF
90 167734 000442                       QC380: BR    QC450
91                                     ;* * * * WHEN SHOW STATUS COMMAND
92 167736                               QC400:
93 167736 022767 000020 005034        CMP    #KXSSH,C,KW.CMD
94 167744 001027                       BNE    QC447
95                                     ;* * * * PLACE BOOT SWITCH AND MAP SWITCH
96                                     ; VALUES TO DPR REGISTER 3
97 167746 113737 177522 175006        MOVB  @#KL.CSB,@#KL.SC3
98                                     ;* * * * CLEAR ALL NON RELATED BITS
99 167754 042737 177401 175006        BIC    #^C(KMSMAP | KMSMS),@#KW.SC3
100                                    ;* * * * IF USER SOCKETS MAPPED LOW
101 167762 032737 000010 177522        BIT    #KXSMP2,@#KL.CSB
102 167770 001402                       BEQ    QC420
103                                     ;* * * * THEN
104                                     ;* * * * * TEST FOR RAM AT 0
105 167772 005000                       CLR    R0
106 167774 000402                       BR    QC440
107                                     ;* * * * ELSE
108 167776                               QC420:
109                                     ;* * * * * TEST FOR RAM AT 100000
110 167776 012700 100000                MOV    #100000,R0
111                                     ;* * * * END IF
112 170002                               QC440:
113                                     ;* * * * IF RAM PRESENT
114 170002 011001                MOV    (R0),R1

```

```

115 170004 005110          COM      (R0)
116 170006 020110          CMP      R1,(R0)
117 170010 001404          BEQ      QC445
118
119
120 170012 010110          MOV      R1,(R0)
121
122 170014 052737 000001 175006      BIS      #BIT0,@#KW.SC3
123
124 170022          QC445:
125 170022 000412          BR      QC470
126
127 170024          QC447:
128 170024 022737 000040 175000      CMP      #KASNOP,@#KW.CMD
129 170032 001003          BNE      QC450
130
131 170034 005037 175000          CLR      #KW.CMD
132
133 170040 000002          RTI      ;(NON STRUCTURED EXIT)
134
135 170042          QC450:
136
137 170042 052737 100000 175002      BIS      #KXSCME,@#KW.STA
138
139 170050          QC470:
140 170050 000402          BR      QC600
141
142 170052          QC500:
143
144 170052 000167 000014          JMP      DECTST
145
146 170056          QC600:
147
148 170056 062706 000004          ADD      #4,SP
149
150 170062 005037 175000          CLR      @#KW.CMD
151
152 170066 000167 177310          JMP      WAITST
153

```

```

; * * * * THEN
; * * * * * RESTORE LOCATION
; * * * * * SET PAM PRESENT BIT OF DPR REG. 3
; * * * * * FWD IF
; * * * * * WHEN NOP COMMAND
; * * * * * CLFAR COMMAND REGISTER
; * * * * * RETURN FROM INTERRUPT
; * * * * * ELSE (BAD COMMAND)
; * * * * * SET COMMAND ERROR BIT OF STATUS REGISTER
; * * * * * END CASE
; * * * * * ELSE (TEST/COMMAND BIT = 1)
; * * * * * DECODE TEST COMMAND (NON-STRUCTURED JUMP TO DECTST)
; * * * * * END IF
; * * * * * REMOVE RETURN ADDRESS AND PSW FROM STACK
; * * * * * CLEAR COMMAND REGISTER
; * * * * * ENTER WAIT STATE (NON STRUCTURED EXIT)
; * * * * * END Q BUS COMMAND INTERPRETER

```



```
1          .SBTTL  DECTST - DECODE AND DISPATCH QBUS SELF TEST REQUESTS
2          .ENABL  GRL
3
4
5          ;
6          ; MODULE NAME: DECTST - DECODE AND DISPATCH QBUS SELF TEST REQUESTS
7          ;
8          ;
9          ;
10         ;
11         ;
12         ;
13         ; FUNCTIONAL DESCRIPTION:
14         ;
15         ; THIS MODULE DECODES THE QBUS SELF TEST REQUESTS AND DISPATCHES TO THE
16         ; APPROPRIATE SELF TEST MODULE. ON RETURN FROM THE SELF TEST MODULE,
17         ; DECTST UPDATES THE LED DISPLAY, UPDATES THE ACCUMULATED ERROR WORD,
18         ; AND PERFORMS THE ACKNOWLEDGEMENT PORTION OF THE PROTOCOL TO NOTIFY THE
19         ; ARBITER OF COMPLETION.
20         ;
21         ; INPUTS:
22         ; TPR 0 CONTAINS THE SELF TEST REQUEST CODE.
23         ; TPR 3 CONTAINS AN OPTIONAL CALLING PARAMETER, IF ANY.
24         ;
25         ; CALLING SEQUENCE:
26         ; A SPECIAL CASE JMP TO DECTST FROM QCOMIN.
27         ;
28         ; OUTPUTS:
29         ; TPR 0 IS CLEAR.
30         ; TPR 1 IS THE SAME AS WHEN CALLED UNLESS DECTST SETS THE COMMAND ERROR
31         ; BIT, BIT 15. IF THE BOOT SWITCH SELECTION IS 10 (QBUS
32         ; CONTROLLED TEST), THE STATE FIELD IS SET TO "WAITING FOR
33         ; QBUS TEST COMMAND". ELSE, THE STATE FIELD IS SET TO "WAITING
34         ; FOR QBUS COMMAND".
35         ; TPR 2 HAS ITS APPROPRIATE TEST BIT CLEARED IF NO ERROR OCCURRED
36         ; AND SET IF AN ERROR OCCURRED. TPR 2 IS THE ACCUMULATED SELF
37         ; TEST RESULTS.
38         ; IF TPR 2'S APPROPRIATE ERROR BIT IS SET, TPR 3 CONTAINS THE TEST CODE
39         ; IN BITS <15:12> AND THE DISCRETE ERROR CODE IN BITS <11:00>.
40         ;
41         ; IF AN ERROR OCCURRED, THE LEDS ARE UPDATED WITH A CALL TO INNERR.
42         ;
43         ; ROUTINES USED:
44         ; SPR5SU, INNERR, & THE VARIOUS SELF TEST ROUTINES
45         ;
46         ; OTHER NOTES AND COMMENTS:
47         ;
48         ; 1. THE ARBITER IS RESPONSIBLE FOR CLEARING THE ACCUMULATED VALUE IN
49         ; TPR 2.
50         ;
51         ; 3. ALL REGISTERS ARE USEABLE WITHOUT RESTORATION.
```

95

```

1 170072                                DECTST::
2 170072 012700 170102                MOV    #3$,R0        ;SET UP A RETURN ADDRESS FROM SPR5SU.
3 170076 000137 173706                JMP    @SPRS5U      ;GO SET UP R5 AND A DEFAULT STACK POINTER.
4 170102                                3$:
5 170102 012700 170354                MOV    #STSTAB,R0   ;POINT TO THE SELF TEST DISPATCH TABLE.
6 170106 005710                        5$:    TST    (R0)        ;ARE WE AT THE END OF THE TABLE?
7 170110 001005                        TST    10$          ;NO.
8 170112 013700 175002                MOV    @#KW.STA,R0  ;YES, GET TPR 1.
9 170116 052700 100000                BIS    #KXSCME,R0  ;SET THE COMMAND ERROR BIT IN THE SAVED TPR 1.
10 170122 000465                        BR     45$          ;GO HANDLE THE REST OF UPDATING TPR 1 & TPR 0.
11 170124 021037 175000                10$:  CMP    (R0),@#KW.CMD ;NO, DOES THE TABLE ENTRY MATCH TPR 0?
12 170130 001403                        BEQ    15$          ;YES.
13 170132 062700 000010                ADD    #TSENLE,R0  ;NO, ADD THE LENGTH OF A TABLE ENTRY TO THE
14                                         ;POINTER.
15 170136 000763                        BR     55$          ;GO TRY THE NEXT ENTRY IN THE TABLE.
16 170140                                15$:
17 170140 013746 175002                MOV    @#KW.STA,-(SP) ;TPR 1 (THE STATUS REGISTER),
18 170144 013746 175004                MOV    @#KW.SC2,-(SP) ;TPP 2,
19 170150 012046                        MOV    (R0)+,-(SP)  ;THE COMMAND (WITH BIT 15 CLEARED),
20 170152 042716 100000                BIC    #BIT15,(SP)  ;
21 170156 012046                        MOV    (R0)+,-(SP)  ;THE ERROR CONDITION ROUTINE'S ADDRESS ON
22                                         ;THE STACK,
23 170160 013746 175006                MOV    @#KW.SC3,-(SP) ;TPR 3, AND
24 170164 013746 177524                MOV    @#KW.CSC,-(SP) ;THE LEDS.
25 170170 005001                        CLR    R1           ;CLEAR R1 TO DEFAULT TO NO PARAMETER IN TPR 3.
26 170172 105720                        TSTB   (R0)+        ;NOW, IS THERE A PARAMETER IN TPR 3?
27 170174 001402                        BEQ    20$          ;NO, R1 HAS ALREADY BEEN CLEARED.
28 170176 013701 175006                MOV    @#KW.SC3,R1  ;YES, PUT THE PARAMETER IN R1.
29 170202 105720                        20$:  TSTB   (R0)+        ;IS THE TEST ROUTINE IN OVERLAY 0?
30 170204 001404                        BEQ    25$          ;YES.
31 170206 052737 000040 177520        BIS    #KXSDPE,@#KW.CSA ;NO, IT'S IN OVERLAY 1, SO ENABLE THE
32                                         ;OVERLAY 1 MAP.
33 170214 000403                        BR     30$          ;
34 170216 042737 000040 177520        25$:  BIC    #KXSDPE,@#KW.CSA ;IT'S IN OVERLAY 0, SO DISABLE THE
35                                         ;OVERLAY 1 MAP.
36 170224 052737 010000 175002        30$:  BIS    #KXSNXF,@#KW.STA ;ENABLE C-BIT SETTING ON REFERENCES TO
37                                         ;NON-EXISTENT MEMORY (RATHER THAN A TRAP THRU
38                                         ;4). KXSNXF WILL BE RESTORED WHEN TPR 1 IS
39                                         ;RESTORED.
40 170232 004730                        JSR    PC,@(R0)+    ;CALL THE TEST ROUTINE VIA THE "VECTOR".
41 170234 012637 177524                MOV    (SP)+,@#KW.CSC ;RESTORE THE LEDS.
42 170240 005700                        TST    R0           ;WAS AN ERROR DETECTED?
43 170242 001406                        BEQ    35$          ;NO.
44 170244 010037 175006                MOV    R0,@#KW.SC3  ;YES, SET TPR 3 FOR THIS ERROR.
45 170250 012601                        MOV    (SP)+,R1     ;PUT THE VALUE OF TPR 3, WHEN CALLED, IN R1
46                                         ;(IN CASE THE LED HANDLING ROUTINE NEEDS IT).
47 170252 004736                        JSR    PC,@(SP)+    ;YES, GO TO THE LED UPDATING ROUTINE.
48 170254 052616                        BIS    (SF)+,(SP)   ;SET THE TEST'S ERROR BIT IN THE SAVED TPR 2.
49 170256 000404                        BR     40$          ;GO FINISH UP TPR 2, 1, AND 0 UPDATING.
50 170260 012637 175006                35$:  MOV    (SP)+,@#KW.SC3 ;RESTORE TPR 3.
51 170264 005726                        TST    (SP)+        ;FLUSH THE ERROR HANDLER ADDRESS OFF THE
52                                         ;STACK.
53 170266 042616                        BIC    (SP)+,(SP)   ;CLEAR THE TEST'S ERROR BIT IN THE SAVED
54                                         ;TPR 2.
55 170270 012637 175004                40$:  MOV    (SP)+,@#KW.SC2 ;STORE THE RESULT IN TPR 2.
56 170274 012600                        MOV    (SP)+,R0     ;GET THE SAVED TPR 1.
57 170276 042700 000007                45$:  BIC    #KXSTF,R0    ;CLEAR THE SAVED STATE FIELD.
    
```

```

58 170302 013701 177522      MOV    @#KW.CSB,R1      ;GET THE BOOT SWITCH SETTING FROM KXTCSPB BITS
59                                ;4 *0 7.
60 170306 042701 177417      BIC    #C<KMSSWS>,R1   ;ISOLATE THE SWITCH SETTING BITS.
61 170312 022701 000240      CMP    #10.*20,R1     ;IS THE SWITCH SETTING FOR "QBUS CONTROLLED
62                                ;TESTS"?
63 170316 001003              BNE    47$            ;NO.
64 170320 052700 000002      BIS    #KPSQTS,R0     ;YES, SFT THE STATE TO "QBUS CONTROLLED TEST
65                                ;STATE".
66 170324 000402              BR     50$            ;
67 170326 052700 000004      47$:  BIS    #KPS$ST,R0   ;SET THE STATE TO "WAITING FOR QBUS COMMAND".
68 170332 010037 175002      50$:  MOV    R0,@#KW.STA ;RESTORE THE STATUS REGISTER.
69 170336 005037 175000      CLR    @#KW.CMD       ;CLEAR THE COMMAND REGISTER, TPR 0.
70 170342 052737 000100 177530  BIS    #KXSDEN,@#KW.CSD ;RE-ENABLE THE TWO PORT RAM (SOMETIMES IT'S
71                                ;NEEDED, SOMETIMES IT'S NOT, BUT DO IT
72                                ;ALWAYS).
73 170350 000137 167402      JMP    @#WAITST       ;GO TO THE WAIT STATE AND WAIT FOR THE NEXT
74                                ;QBUS COMMAND.
75
76                                ;STSTAB, THE SELF TEST DISPATCH TABLE, DEFINES THE LEGAL SELF TEST CODES, THE
77                                ;EXISTENCE OF A CALLING PARAMETER IN TPR 3, THE "ROM PAGE" CONTAINING THE TEST
78                                ;CODE, AND THE ADDRESS OF THE CODE.
79                                ;
80                                ; .WORD    TPR 0 VALUE OR 0      ;TPR 0 VALUE IF LEGAL DISPATCH CODE &
81                                ;                      ;0 IF END OF LIST (THUS IMPLYING
82                                ;                      ;COMMAND ERROR)
83                                ;
84                                ; .WORD    TNNERR          ;ADDRESS OF ROUTINE THAT HANDLES LED
85                                ;                      ;UPDATING IF AN ERROR IS INDICATED.
86                                ;
87                                ; .BYTE    0 OR NON-0      ;NON-0 IMPLIES THAT A CALLING
88                                ;                      ;PARAMETER IS IN TPR 3. 0
89                                ;                      ;IMPLIES NO PARAMETER IN TPR 3.
90                                ;
91                                ; .BYTE    0 OR NON-0      ;NON-0 IMPLIES THAT THE TEST ROUTINE
92                                ;                      ;IS IN THE HIGH OVERLAY, OVERLAY 1, OF
93                                ;                      ;ROM, THUS IMPLYING THAT KXTCRA
94                                ;                      ;BIT 5 MUST BE 1 TO MAP THE CODE
95                                ;                      ;TO THE 160000 BASE ADDRESS. 0
96                                ;                      ;IMPLIES THAT THE TEST ROUTINE IS
97                                ;                      ;IN THE LOW OVERLAY, OVERLAY 0,
98                                ;                      ;OF ROM, THUS KXTCRA BIT 05 MUST
99                                ;                      ;BE 0 TO MAP THE CODE TO THE
100                               ;                      ;160000 BASE ADDRESS.
101                               ;
102                               ; .WORD    ADDRESS          ;THE ADDRESS OF THE ROUTINE'S "VECTOR"
103                               ;                      ;IN THE FIRST 32 (DECIMAL) BYTES OF
104                               ;                      ;THE ROM OVERLAY.
105                               ;
106 170354      STSTAB:
107                                ;CSR TEST
108 170354 100001      .WORD    KXST01      ;TPR 0 VALUE
109 170356 170506      .WORD    T1ERR      ;LED UPDATING ROUTINE ON ERROR
110 170360 000      .BYTE    0          ;NO INPUT PARAMETER
111 170361 000      .BYTE    0          ;IN ROM OVERLAY 0
112 170362 160004      .WORD    T1          ;VECTOR ADDRESS
113
114      STSENL =      .-STSTAB      ;DEFINE THE TABLE ENTRY LENGTH
  
```

97

115					
116			;RAM TEST		
117	170364	100002	.WORD	KXST02	;TPR 0 VALUE
118	170366	170546	.WORD	T2ERR	;LED UPDATING ROUTINE ON ERROR
119	170370	000	.BYTE	0	;NO INPUT PARAMETER
120	170371	000	.BYTE	0	;IN ROM OVERLAY 0
121	170372	160010	.WORD	T2	;VECTOR ADDRESS
122			;ROM TEST		
123	170374	100004	.WORD	KXST03	;TPR 0 VALUE
124	170376	170576	.WORD	T3ERR	;LED UPDATING ROUTINE ON ERROR
125	170400	001	.BYTE	1	;TPR 3 CONTAINS PARAMETER
126	170401	000	.BYTE	0	;IN ROM OVERLAY 0
127	170402	160014	.WORD	T3	;VECTOR ADDRESS
128			;CPU TEST		
129	170404	100010	.WORD	KXST04	;TPR 0 VALUE
130	170406	170642	.WORD	T4ERR	;LED UPDATING ROUTINE ON ERROR
131	170410	000	.BYTE	0	;NO INPUT PARAMETER
132	170411	000	.BYTE	0	;IN ROM OVERLAY 0
133	170412	160020	.WORD	T4	;VECTOR ADDRESS
134			;BEVENT TEST		
135	170414	100020	.WORD	KXST05	;TPR 0 VALUE
136	170416	170650	.WORD	T5ERR	;LED UPDATING ROUTINE ON ERROR
137	170420	000	.BYTE	0	;NO INPUT PARAMETER
138	170421	000	.BYTE	0	;IN ROM OVERLAY 0
139	170422	160024	.WORD	T5	;VECTOR ADDRESS
140			;SLU 1 TEST		
141	170424	100040	.WORD	KXST06	;TPR 0 VALUE
142	170426	170656	.WORD	T6ERR	;LED UPDATING ROUTINE ON ERROR
143	170430	000	.BYTE	0	;NO INPUT PARAMETER
144	170431	000	.BYTE	0	;IN ROM OVERLAY 0
145	170432	160030	.WORD	T6	;VECTOR ADDRESS
146			;SLU 2 TEST		
147	170434	100100	.WORD	KXST07	;TPR 0 VALUE
148	170436	170664	.WORD	T7ERR	;LED UPDATING ROUTINE ON ERROR
149	170440	001	.BYTE	1	;TPR 3 CONTAINS PARAMETER, CHANNEL A /
150					;CHANNEL B TEST SELECTION
151	170441	000	.BYTE	0	;IN ROM OVERLAY 0
152	170442	160034	.WORD	T7	;VECTOR ADDRESS
153			;PIO TEST		
154	170444	100200	.WORD	KXST10	;TPR 0 VALUE
155	170446	170720	.WORD	T10ERR	;LED UPDATING ROUTINE ON ERROR
156	170450	000	.BYTE	0	;NO INPUT PARAMETER
157	170451	001	.BYTE	1	;IN ROM OVERLAY 1
158	170452	160000	.WORD	T10	;VECTOR ADDRESS
159			;DMA TEST		
160	170454	100400	.WORD	KXST11	;TPR 0 VALUE
161	170456	170726	.WORD	T11ERR	;LED UPDATING ROUTINE ON ERROR
162	170460	001	.BYTE	1	;TPR 3 CONTAINS PARAMETER, BITS
163					; <21:06> OF A USEABLE QBUS DMA BUFFER
164	170461	001	.BYTE	1	;IN ROM OVERLAY 1
165	170462	160004	.WORD	T11	
166			;QIR TEST		
167	170464	101000	.WORD	KXST12	;TPR 0 VALUE
168	170466	170734	.WORD	T12ERR	;LED UPDATING ROUTINE ON ERROR
169	170470	001	.BYTE	1	;TPR 3 CONTAINS PARAMETER, THE QBUS
170					; INTERRUPT VECTOR ADDRESS
171	170471	001	.BYTE	1	;IN ROM OVERLAY 1

172 170472 160010
173
174 170474 102000
175 170476 170742
176 170500 000
177 170501 001
178 170502 160014
179
180 170504 000000
181

.WORD T12
;Two PORT RAM TEST
.WORD KXST13
.WORD T13ERR
.BYTE 0
.BYTE 1
.WORD T13
;END OF TABLE
.WORD 0

;VECTOR ADDRESS

;TPR 0 VALUE
;LED UPDATING ROUTINE ON ERROR
;NO INPUT PARAMETER
;IN ROM OVERLAY 1
;VECTOR ADDRESS

;IF NO MATCH, THEN COMMAND ERROR.

69

```
1          .SBTTL TNNERR - UPDATE LEDS AFTER SELFTST NN
2          .ENABL GBL
3
4
5          ;
6          ; MODULE NAME: TNNERR - UPDATE LEDS AFTER SELFTST NN
7          ;
8          ;
9          ;
10         ;
11         ;
12         ; FUNCTIONAL DESCRIPTION:
13         ;
14         ; TIERR THROUGH T13ERR HANDLE SETTING THE LEDS DEPENDING ON THE ERROR
15         ; CODE RETURNED IN R0 BY A SELF-TEST ROUTINE. EACH TEST HAS A SET OF
16         ; BITS GIVING "SIGNIFICANT" ERROR CONDITIONS. "INSIGNIFICANT" ERROR
17         ; CONDITIONS ARE SUCH ERROR CODES AS "ROM MAPPED LOW SO INTERRUPT
18         ; TESTS WERE NOT EVEN TRIED". AFTER DECIDING ON AN LED VALUE, THE
19         ; ROUTINE CALLS SETLED TO SET THE VALUE. SETLED PRIORITIZES THE LED
20         ; SETTINGS SUCH THAT A NON-FATAL CODE WILL NOT REPLACE A FATAL CODE,
21         ; FOR EXAMPLE.
22         ;
23         ; INPUTS:
24         ; R0 CONTAINS THE TEST'S DISCPETE ERROR CODE.
25         ; R1 CONTAINS THE VALUE IN R1 WHEN THE SELFTST ROUTINE WAS CALLED. THIS
26         ; VALUE IS OPTIONALLY USED BY TNNERR.
27         ;
28         ; CALLING SEQUENCE:
29         ; JSR PC,TNNERR
30         ;
31         ; OUTPUTS:
32         ; THE LEDS ARE UPDATED VIA A CALL TO SETLED.
33         ;
34         ; R0 CONTAINS 0 IF NO SIGNIFICANT ERROR OCCURRED. R0 CONTAINS THE LED
35         ; VALUE USED IN THE CALL TO SETLED IF A SIGNIFICANT ERROR OCCURRED.
36         ;
37         ; NOTE: A SIGNIFICANT ERROR IS AN ERROR THAT RESULTS IN A REQUEST TO
38         ; UPDATE THE LEDS. WHEN A SELFTST CAN NOT BE RUN (TYPICALLY BECAUSE ROM
39         ; IS MAPPED LOW), THE RESULTING ERROR IS NOT SIGNIFICANT AND, THEREFORE,
40         ; THERE IS NO REQUEST TO UPDATE THE LEDS.
41         ;
42         ; ROUTINES USED:
43         ; SETLED
44         ;
45         ; REGISTERS CHANGED:
46         ; R0,R2
47         ;
```

100

```

1
2 ;THE CSR TEST, TEST 1, IS A SPECIAL CASE BECAUSE WE MUST DIFFERENTIATE BETWEEN
3 170506 032700 000004 TIERR:: BIT #4,R0 ;IS THERE A TPR ERROR?
4 170512 001407 BEQ TIERR1 ;NO.
5 170514 032737 000340 177524 BIT #340,#KMW.CSC ;YES, BUT ARE WE IN STANDALONE MODE (I. E.
6 ;WITH ID EQUAL TO 0 OR 1)? NOTE: THE 340 MASK
7 ;IS A SUBSET OF THE KMSIDS DEFINITON. IF THE
8 ;LOCATION OF KMSIDS CHANGES, THE 340 MUST BE
9 ;CHANGED.
10 170522 001406 BFC TIERR2 ;YES, SO IT'S A NON-FATAL ERROR.
11 170524 012700 000017 MOV #FERRD,R0 ;NO, WE ARE IN NON-STANDALONE MODE SO IT'S A
12 ;FATAL ERROR.
13 170530 000511 BR TNNCM1
14 170532 032700 000373 TIERR1: BIT #373,R0 ;ARE THERE OTHER CSR ERRORS?
15 170536 001511 BFC TNINX ;NO.
16 170540 012700 000010 TIERR2: MOV #NFERD,R0 ;YES, SET UP THE NON-FATAL LED DISPLAY.
17 170544 000503 BR TNNCM1
18 ;
19 ;THE RAM TEST, TEST 2, IS A SPECIAL CASE BECAUSE WE MUST DIFFERENTIATE BETWEEN
20 ;FATAL NATIVE RAM ERRORS AND NON-FATAL USER RAM ERRORS.
21 170546 032700 000037 T2ERR:: BIT #37,R0 ;ARE THERE NATIVE RAM ERRORS?
22 170552 001403 BEQ T2ERR1 ;NO.
23 170554 012700 000017 MOV #FERRD,R0 ;YES, SET UP FATAL LED DISPLAY.
24 170560 000475 BR TNNCM1
25 170562 032700 001740 T2ERR1: BIT #1740,R0 ;ARE THERE USER RAM ERRORS?
26 170566 001475 BEQ TNINX ;NO.
27 170570 012700 000011 MOV #UROMOD,R0 ;YES, SET UP NON-FATAL LED DISPLAY.
28 170574 000467 BR TNNCM1
29 ;
30 ;THE ROM TEST, TEST 3, ERROR HANDLING IS A SPECIAL CASE BECAUSE THERE ARE
31 ;3 POSSIBLE LED SETTINGS THAT MAY RESULT.
32 170576 032700 000003 T3ERR:: BIT #3,R0 ;ARE THERE NATIVE ROM ERRORS?
33 170602 001403 BEQ T3ERR1 ;NO.
34 170604 012700 000017 MOV #FERRD,R0 ;YES.
35 170610 000461 BR TNNCM1
36 170612 032700 000004 T3ERR1: BIT #4,R0 ;IS THERE A LOW BYTE USER ROM ERROR?
37 170616 001403 BFC T3ERR2 ;NO.
38 170620 012700 000011 MOV #UROMOD,R0 ;YES.
39 170624 000453 BR TNNCM1
40 170626 032700 000010 T3ERR2: BIT #10,R0 ;IS THERE A HIGH BYTE USER ROM ERROR?
41 170632 001453 BEQ TNINX ;NO.
42 170634 012700 000012 MOV #UROMID,R0 ;YES.
43 170640 000445 BR TNNCM1
44 170642 012702 170766 T4ERR:: MOV #T4ETB,R2 ;AS ABOVE FOR THE CPU TEST.
45 170646 000437 BR TNNCOM
46 170650 012702 170772 T5ERR:: MOV #T5ETB,R2 ;AS ABOVE FOR THE BEVFNT TEST.
47 170654 000434 BR TNNCOM
48 170656 012702 170776 T6ERR:: MOV #T6ETB,R2 ;AS ABOVE FOR THE DLART TEST.
49 170662 000431 BR TNNCOM
50 ;
51 ;THE 2ND SERIAL LINE UNIT TEST, TEST 7, IS A CODED SPECIAL CASE TO HANDLE
52 ;CHANNEL A / CHANNEL B LED SETTINGS.
53 170664 005701 T7ERR:: TST R1 ;DID WE DO THE "BOTH CHANNELS GO/NO GO" TEST?
54 170666 001403 BEQ T7ERR1 ;YES, USE CHANNEL A'S LED SETTING.
55 170670 032701 000001 BIT #BIT0,R1 ;NO, DID WE SELFTST ONLY CHANNEL A?
56 170674 001403 BEQ T7ERR2 ;NO.
57 170676 012702 171002 T7ERR1: MOV #T7AETB,R2 ;YES.

```

101

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58 170702 000421          BR      TNNCOM
59 170704 032701 000002  T7ERR2: BIT  #BIT1,R1      ;DID WE SELFTEST ONLY CHANNEL B?
60 170710 001424          BEQ    TNNINX          ;NO.
61 170712 012702 171006  MOV    #T7BET0,R2      ;YES.
62 170716 000413          BR      TNNCOM
63 170720          TIGERR::
64 170720 012702 171012  MOV    #T10ETB,R2      ;AS ABOVE FOR THE PIO CHIP TEST.
65 170724 000410          BR      TNNCOM
66 170726          T11ERR::
67 170726 012702 171016  MOV    #T11ETB,R2      ;AS ABOVE FOR THE DMA CHIP TEST.
68 170732 000405          BR      TNNCOM
69 170734          T12ERR::
70 170734 012702 171022  MOV    #T12ETB,R2      ;AS ABOVE FOR THE QIR TEST.
71 170740 000402          BR      TNNCOM
72 170742          T13ERR::
73 170742 012702 171026  MOV    #T13ETB,R2      ;AS ABOVE FOR THE TPR TEST.
74
75          ;
76          ;TNNCOM IS THE COMMON ENTRY TO USE WHEN R2 POINTS TO A TABLE ENTRY OF
77 170746 032200  TNNCOM: BIT  (R2)+,R0      ;ARE ANY OF THE "SIGNIFICANT" ERROR BITS
78          ;SET IN THE RETURNED ERROR CODE?
79 170750 001404          BEQ    TNNINX          ;NO, DON'T EVEN TRY TO UPDATE THE LEDES.
80 170752 011200  MOV    (R2),R0
81          ;
82          ;TNNCM1 IS THE COMMON ENTRY TO USE WHEN R0 CONTAINS AN LED SETTING.
83 170754 004737 167200  TNNCM1: JSK  PC,#SETLED  ;UPDATE THE LEDES USING SETLPD SO THAT A MORE
84          ;IMPORTANT SETTING DOES NOT GET OVERWRITTEN.
85 170760 000401          BR      TNNXIT
86          ;
87          ;TNNINX IS THE EXIT WHEN THERE ARE NO SIGNIFICANT ERRORS.
88 170762 005000  TNNINX: CLR  R0          ;SHOW THAT NO SIGNIFICANT ERROR OCCURRED.
89 170764 000207  TNNXIT: RTS  PC
90
91          ;ERROR TABLES GIVING THE "SIGNIFICANT" ERROR BIT SETTINGS AND THE ASSOCIATED
92          ;LED SETTING FOR THE ERROR. THE SPARSINESS OF THE BITS IS BECAUSE CERTAIN
93          ;TESTS RETURN NON-ZERO ERROR CODES THAT REALLY MEAN "COULDN'T RUN THE TEST".
94          ;THERE ARE SEVERAL TESTS WHERE INTERRUPTS CANNOT BE TESTED BECAUSE ROM IS IN
95          ;LOW MEMORY.
96          ;
97          ;T1, T2, & T3 MUST BE SPECIAL CASED IN CODE.
98 170766 007777 000017  T4ETB: .WORD 7777,FERRD
99 170772 000016 000010  T5ETB: .WORD 16,NFFRPD
100 170776 000176 000013  T6ETB: .WORD 176,S1LRD
101 171002 007476 000014  T7AETR: .WORD 7476,S2ALBD
102
103          ;NOTE: BITS 6 & 7 ARE NOT INCLUDED BECAUSE A
104          ;CONFIGURATION JUMPER ON THE KXT11-CA SWITCHES
105          ;THE DMA CHIP CONNECTION FROM SLU2 CHAN A TO
106          ;THE PIO CHIP. WHEN THE DMA CHIP IS CONNECTED
107          ;TO THE PIO CHIP, BITS 6 & 7 WILL ALWAYS BE 1,
108          ;EVEN THOUGH NO TRUE ERROR OCCURRED.
109          ;THEREFORE, WE DO NOT SET THE LEDES.
110          ;NOTE: DMA (AND THEREFORE BITS 6 & 7) DOES
111          ;NOT APPLY TO CHANNEL B. IF THE BITS COME ON
112          ;WE HAVE A SERIOUS ERROR, SO WE OUGHT TO SET
113          ;THE LEDES.
112 171012 000376 000016  T10ETB: .WORD 376,PAPLBD
113 171016 000074 000010  T11ETB: .WORD 74,NFFRPD
114 171022 000172 000010  T12ETB: .WORD 172,NFERRD
115 171026 007767 000017  T13ETB: .WORD 7767,FERRD
116

```



```

1          .S8TTL DMALD - DMA LOADER
2          .ENABLE LC,GBL
3
4          ;
5          ; Module name: DMALD - DMA LOAD
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ; Functional Description:
13         ;
14         ; This is the module that controls the loading of the IOP's application
15         ; from the Q bus by the DMA controller. It is used by the Q bus command
16         ; interpreter module on reception of a DMA load command. This module
17         ; expects the data which is to be placed into the chain control registers
18         ; of the DMA controller to be in the dual port registers 2 and 3.
19         ; On completion of the load, this module places the IOP in the
20         ; Wait state.
21
22         ;Input Parameters:
23
24         ; NONE
25
26         ;Output Parameters
27
28         ; NONE
29
30         ;DATA STRUCTURES USED
31
32         ; 1) DMA MASTPR MODE REGISTER
33         ; 2) DMA COMMAND REGISTER
34         ; 3) DMA CHANNEL 0 REGISTER
35         ; 4) DUAL PORT RAM REGISTER 2 AND 3
36         ; 5) IOP STATUS REGISTER
37         ; 6) IOP COMMAND REGISTER
38
39         ;Routines Used
40
41         ; 1) WAITST (JUMP TO)
42
43         ;Global Symbols Defined
44

```

102

1	174442	CHNOFO =	174442	;DMA CHAIN OFFSET REGISTER ADDRESS OF CHANNEL 0
2	174446	CHNSTO =	174446	;DMA CHAIN SEGMENT/TAG REGISTER ADDRESS OF CHANNEL 0
3	174470	MMREGA =	174470	;DMA MASTER MODE REGISTER ADDRESS
4	174454	CMREGA =	174454	;DMA COMMAND REGISTER ADDRESS
5	174456	SOREGA =	174456	;DMA CHANNEL 0 STATUS REGISTER ADDRESS
6	010000	CAEIT =	10000	;CHAIN ABORT BIT OF STATUS
7	000002	EOPBIT =	2	;END OF PROCESS BIT OF STATUS
8	004000	NACBIT =	4000	;NAC BIT OF STATUS


```
1          .SBTTL BSUPV - BOOT SUPERVISOR
2          .ENABLE LC,GBL
3
4
5          ;
6          ; Module name: BSUPV - BOOT SUPERVISOR
7          ;
8          ; System: KXT11-CA Native Firmware
9          ;
10         ;
11         ;
12         ;
13         ;
14         ;
15         ; Functional Description:
16         ;
17         ; This module supervises the boot process. It makes the determination
18         ; of which device the application will be loaded from and transfers
19         ; control to the appropriate routines.
20
21         ;Input Parameters:
22         ;
23         ; 1. BOOTFD of FLGWRD
24         ;
25         ;
26         ;Output Parameters
27         ;
28         ; NONE
29         ;
30         ;Data Structures Used
31         ;
32         ; 1. LED DISPLAY
33         ;
34         ; 2. IOP STATUS REGISTER
35         ;
36         ; 3. TCSR, bits of BOOTSW
37         ;
38         ;Routines Used
39         ;
40         ; 1. TU58 Boot (TU58BT)
41         ;
42         ; 2. Loop back tests (LBTEST)
43         ;
44         ; 3. Serial ODT monitor (SODTM)
45         ;
46         ; 4. Set LEDs (SETLED)
47         ;
48         ; 5. Trap 24 emulator (TRAP24)
49         ;
50         ;Global Symbols Defined
51         ;
52         ; NONE
```

105

```

1
2 171170          BSUPV::
3
4 171170 010500          MOV    R5,R0
5 171172 062700 177700  ADD    #ADSTKO,R0
6 171176 010006          MOV    R0,SP
7
8
9
10
11 171200 022765 000002 177774  CMP    #2,BOOTFO(R5)
12 171206 103414          BLD    BS100
13
14 171210 012700 000000          MOV    #NNCED,R0
15 171214 004767 175760  CALL  SETLFD
16
17
18 171220 042737 000007 175002  BIC   #KMSSTF,@#KW.STA
19 171226 052737 000007 175002  BIS   #KPSNNC,@#KW.STA
20
21 171234 000167 176116          JMP   TRAP24
22
23 171240 022765 000003 177774  BS100: CMP   #3,BOOTFO(R5)
24 171246 001014          BNE   BS200
25
26 171250 012700 000001          MOV   #PRIAD,R0
27 171254 004767 175720  CALL  SETLED
28
29 171260 042737 000007 175002  BIC   #KMSSTF,@#KW.STA
30 171266 052737 000005 175002  BIS   #KPSPRS,@#KW.STA
31
32 171274 000167 000434          JMP   TU58BT
33
34 171300 022765 000004 177774  BS200: CMP   #4,BOOTFO(R5)
35 171306 001007          BNE   BS300
36
37 171310 052737 020000 175002  BIS   #KXSBDP,@#KW.STA
38
39 171316 005046          CLR   -(SP)
40 171320 005046          CLR   -(SP)
41
42 171322 000167 173300          JMP   SODTM ;(NON-STRUCTURED EXIT TO SERIAL ODT)
43
44 171326 022765 000005 177774  BS300: CMP   #5,BOOTFO(R5)
45 171334 001404          BEQ   BS400
46
47 171336 022765 000006 177774  CMP   #6,BOOTFO(R5)
48 171344 001002          BNE   BS500
49 171346          BS400:
50
51 171346 000167 176030          JMP   WAITST ;(NON STRUCTURED EXIT)
52
53 171352          BS500:
54 171352 022765 000010 177774  CMP   #8,BOOTFO(R5)
55 171360 001404          BFW   BS550
56
57 171362 022765 000011 177774  CMP   #9,BOOTFO(R5)

```

```

;* PROCEDURE BOOTSTRAP SUPERVISOR
;* * SET SP TO DEFAULT USER STACK
;* * CASE BOOT SELECTION
;* * WHFM 0
;* * OR 1
;* * OR 2
;* * * SET LEDS TO NON NATIVE CODE STATE
;* * * SET STATUS REGISTER TO NON NATIVE
CODE STATE
;* * * EMULATE TRAP TO 24 (NON STRUCTURED EXIT)
;* * WHEN 3
;* * * SET LED TO PRIMARY BOOTSTRAP STATE
;* * * SET STATUS REGISTER PRIMARY BOOTSTRAP STATE
;* * * PERFORM TU58 PRIMARY BOOTSTRAP (JUMP TO TU58 MODULE)
;* * WHEN 4
;* * * DISABLE BREAKS
;* * * PUSH 0 ADDRESS AND PSW ON STACK
;* * * PERFORM SERIAL ODT
;* * WHEN 5
;* * OR 6
;* * * WAIT FOR COMMAND
;* * WHEN 8
;* * OR 9

```

```
58 171370 001005          BNE      BSS70
59 171372          BS550:
60
61 171372 042737 000040 177520  BIC      #KXSDPE,@#KW.CSA      ;* * * ENABLE OVERLAY 0
62
63 171400 000167 172306          JMP      LBTST ;(NON-STRUCTURED EXIT) ;* * * PERFORM LOOP BACK TESTS
64
65 171404          BS570:
66 171404 022765 000012 177774  CMP      #10,,BOOTFO(R5)      ;* * * WHEN 10
67 171412 001002          BNE      BS600
68
69 171414 000167 175762          JMP      WAITST ;(NON-STRUCTURED EXIT) ;* * * WAIT FOR COMMAND
70
71 171420          BS600:
72
73 171420 012700 000017          MOV      #FERRD,R0           ;* * * SET LEDS TO FATAL ERROR
74 171424 004767 175550          CALL   SETTLED
75
76 171430 000777          FAS:: BR      .           ;* * * INVALID SELECTION STOP IOP
77
78
                                ;* * * END CASE
                                ;* * * END BOOTSTRAP SUPERVISOR
```

```
1 .SBTTL QODTM - Q BUS ODT MONITOR
2
3 .FNABLE GBL,LC
4
5 ; Module name: QODTM - Q BUS ODT MONITOR
6 ;
7 ; System: KXT11-CA Native Firmware
8 ;
9 ;
10 ;
11 ;
12 ; Functional Description:
13 ;
14 ; This module is the main controlling module for the Q bus ODT mode.
15 ; It supervises the ODT functions and on completion returns control
16 ; back to the application or places the IOP in the wait state.
17 ;
18 ;Input Parameters:
19
20 ; None
21
22 ;Output Parameters
23
24 ; None
25
26 ;Routines Used
27
28 ; 1) Save Registers (SAVERG)
29 ; 2) Set LEDs (SETLED)
30 ; 3) Wait State (WAITST)
31 ; 4) Go/Proceed (PROC)
32 ; 5) Go/Proceed (GO)
33 ; 6) Deposit (DEPOS)
34 ; 7) Examine (EXAMIN)
35
36 ;Registers Used Outside of Output Parameters:
37
38
```



```

58 171566 013700 175006      MOV     @#KW.SC3,R0
59                               ;* * * * PERFORM GO
60 171572 004767 175174      CALL   GO
61                               ;* * * * IF RETURNED
62                               ;* * * * THEN
63                               ;* * * * * SET ERROR FLAG
64 171576 052703 100000      BIS     #ERRFG0,R3
65                               ;* * * * * RE-ENABLE DUAL PORT PAM (DISABLED
66                               ;           BY THE RESET PERFORMED BY GO ROUTINE)
67 171602 052737 009100 177530  BIS     #KXSDEN,@#KW.CSD
68 171610 000437              BR      QS1000
69                               ;* * * * WHEN DEPOSIT
70 171612              QS500:
71 171612 022700 000004      CMP     #KXSDFO,R0
72 171616 001005              BNE     QS700
73                               ;* * * * SET DATA = DPR 2
74 171620 013704 175004      MOV     @#KW.SC2,R4
75                               ;* * * * PERFORM DEPOSIT
76 171624 004767 174644      CALL   DEPOS
77 171630 000427              BR      QS1000
78                               ;* * * * WHEN OPEN REGISTER
79 171632              QS700:
80 171632 022700 000002      CMP     #KXSORD,R0
81 171636 001007              BNE     QS800
82                               ;* * * * SET TARGET = DPR 3
83 171640 013702 175006      MOV     @#KW.SC3,R2
84                               ;* * * * SET REG/ADDR FLAG = REGISTER
85 171644 052703 000200      BIS     #REGFG0,R3
86                               ;* * * * PERFORM OPEN ON REGISTER
87 171650 004767 174066      CALL   EXAMIN
88 171654 000415              BR      QS1000
89                               ;* * * * WHEN OPEN MEMORY
90 171656              QS800:
91 171656 022700 000001      CMP     #KXSOMO,R0
92 171662 001007              BNE     QS900
93                               ;* * * * SET TARGET = DPR 3
94 171664 013702 175006      MOV     @#KW.SC3,R2
95                               ;* * * * SET REG/ADDR FLAG = ADDRESS
96 171670 042703 000200      BIC     #REGFG0,R3
97                               ;* * * * PERFORM OPEN MEMORY
98 171674 004767 174042      CALL   EXAMIN
99 171700 000403              BR      QS1000
100                              ;* * * * ELSE
101 171702              QS900:
102                              ;* * * * SET COMMAND ERROR BIT
103 171702 052737 100000 175002  BIS     #KXSCME,@#KW.STA
104                              ;* * * * END CASE
105 171710              QS1000:
106                              ;* * * * IF ERROR FLAG SET
107 171710 005703              TST     R3
108 171712 100005              JPL     QS1100
109                              ;* * * * THEN
110                              ;* * * * SET COMMAND ERROR FLAG OF STATUS REGISTER
111 171714 052737 100000 175002  BIS     #KXSCME,@#KW.STA
112                              ;* * * * CLPAR ERROR FLAG
113 171722 042703 100000      BIC     #ERRFG0,R3
114                              ;* * * * END IF

```

109


```
115 171726                                QS1100:
116                                         ;* * * CLEAR COMMAND REGISTER
117 171726 005037 175000                 CLR    @#KW.CMD
118                                         ;* * END UNTIL
119 171732 000661                         BR     QS100
120                                         ;* FND Q BUS ODT MONITOR
```

110

```
1          .SBTTL  TU58BT - TU58 BOOT STRAP
2
3          .ENABLE  GRL,LC
4          ;
5          ; Module name: LJD
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11        ;
12        ;
13        ;
14        ; Functional Description:
15        ;
16        ; This is the primary loader for TU58s. It will attempt to load and transfer
17        ; control to the code in the boot block of a TU58 drive connected to the
18        ; console port (SLU1). If the first word of the block is in the range of
19        ; 240 to 277 it is considered a valid boot block. This routine will
20        ; continue to try to boot until it succeeds.
```

```

1
2
3 171734          TU58BT::          ;* PROCEDURE TU58 BOOT
4
5 171734 012700 000001      MOV      #1,R0          ;* * SET DRIVE FLAG TO 0
6
7 171740          TU100:          ;* * DO UNTIL SUCCESSFUL BOOT
8
9 171740 005100          COM      R0          ;* * * TOGGLE DRIVE FLAG
10 171742 042700 177776     BIC      #^C1,R0
11
12 171746 005004          CLR      R4          ;* * * SET POINTER = 0
13
14 171750 004767 000260     CALL     SNDBRK        ;* * * SEND BREAK
15
16 171754 012702 000002     MOV      #2,R2          ;* * * SEND INIT
17 171760 012701 172320     MOV      #INITST,R1
18 171764 004767 000310     CALL     SEND
19
20 171770 012703 000002     MOV      #2,R3          ;* * * DO UNTIL TIMED OUT OR CONTINUE RECEIVED
21 171774
22 171774 005002          TU120:          CLR      R2
23 171776          TU125:
24 171776 105737 177560     TSTB    @#RCSR1A
25 172002 100403          BMI     TU130
26 172004 077204          SOB     R2,TU125
27 172006 077306          SOB     R3,TU120
28
29 172010 000753          BR      TU100 ;NON STRUCTURED BRANCH
30 172012
31 172012 122737 000020 177562  TU130:          CMPB    #20,@#RBUF1A
32 172020 001365          BNE     TU120
33
34
35 172022 004767 000206     CALL     SNDBRK        ;* * * SEND BREAK
36
37 172026 012702 000002     MOV      #2,R2          ;* * * SEND BOOT COMMAND
38 172032 012701 172322     MOV      #BOOTST,R1
39 172036 004767 000236     CALL     SEND
40
41 172042
42 172042 105737 177564          TU150:          TSTB    @#XCSR1A
43 172046 100375          SPL
44
45
46 172050 110067 005512     MOVB    R0,XBUF1A      ;* * * END UNTIL
47
48 172054 012702 001000     MOV      #512.,R2      ;* * * SEND DRIVE NUMBER
49 172060
50
51 172060 012703 000100     MOV      #100,R3       ;* * * DO UNTIL 512 BYTES RECIEVED
52 172064 005001          TU200:          CLR      R1
53 172066 105737 177560     TU300:          TSTB    @#RCSR1A
54 172072 100403          TU400:          BMI     TU500
55 172074 077104          SOB     R1,TU400
56 172076 077306          SOB     R3,TU300
57
; * * * IF TIMED OUT

```

111

```

58                                     ;* * * * * THEN
59                                     ;* * * * * RETRY
60 172100 000717                       BR      TU100 ;(NON STRUCTURED BRANCH)
61                                     ;* * * * * ELSE
62 172102                               TU500:
63                                     ;* * * * * INPUT DATA
64 172102 113724 177562                MOVB   @#KBUF1A,(R4)+
65                                     ;* * * * * DECREMENT BYTE COUNTER
66 172106 005302                       DEC    R2
67                                     ;* * * * * END IF
68 172110                               TU600:
69                                     ;* * * * * IF 3 BYTES HAVE BEFN RECEIVED
70 172110 022702 000775                CMP    #509.,R2
71 172114 001013                       BNE   TU600
72                                     ;* * * * * AND BYTE 1 = 2
73 172116 005001                       CLR    R1
74 172120 122721 000002                CMPR  #2,(R1)+
75 172124 001007                       BNE   TU800
76                                     ;* * * * * AND BYTE 2 = 12
77 172126 122721 000012                CMPR  #12,(R1)+
78 172132 001004                       BNE   TU800
79                                     ;* * * * * AND BYTE 3 = 100
80 172134 122711 000100                CMPR  #100,(R1)
81 172140 001001                       BNE   TU800
82                                     ;* * * * * THEN
83                                     ;* * * * * RETRY
84 172142 000676                       BR      TU100
85                                     ;* * * * * END IF
86 172144                               TU600:
87                                     ;* * * * * END UNTIL
88 172144                               TU900:
89 172144 005702                       TST   R2
90 172146 001344                       BNE   TU200
91                                     ;* * * * * END UNTIL
92 172150                               TU1000:
93 172150 005002                       CLR    R2
94 172152 021227 000240                CMP   (R2),#240
95 172156 103670                       BLO   TU100
96 172160 021227 000277                CMP   (R2),#277
97 172164 101265                       BHI   TU100
98                                     ;* * * * * SAVE UNIT NO.
99 172166 010004                       MOV   R0,R4
100                                     ;* * * * * SET LED DISPLAY TO NON NATIVE CODE EXECUTING
101 172170 012700 000000                MOV   #NNCED,R0
102 172174 004767 175000                CALL  SETLED
103                                     ;* * * * * SET STATUS REGISTER TO NON NATIVE CODE STATE
104 172200 042737 000007 175002        BIC   #KMSSTP,#KW.STA
105 172206 052737 000007 175002        BIS   #KPSNNC,@#KW.STA
106                                     ;* * * * * SET STACK POINTER TO DEFAULT USER STACK
107 172214 012706 177700                MOV   #ADSTKO,SP
108 172220 060506                       ADD   R5,SP
109                                     ;* * * * * PASS CSR ADDRESS TO SECONDARY LOADER
110 172222 012701 177560                MOV   #RCSR1A,R1
111                                     ;* * * * * PASS UNIT NUMBER TO SECONDARY LOADER
112 172226 010400                       MOV   R4,R0
113                                     ;* * * * * EXECUTE AT 0
114 172230 000137 000000                JMP   @#0

```

115

;* END TU58 BOOT

113

```
1
2 172234          SNDBRK:
3
4 172234 012702 000010          MOV     #R.,R2
5 172240 105737 177564          SN100: TSTB  @XCSR1A
6 172244 100375                BPL     SN10C
7 172246 052737 000001 177564  BIS     #1,@XCSR1A
8 172254 005037 177566          CLR     @XBUF1A
9 172260 077211                SOB     R2,SN100
10
11
12 172262 105737 177564          SN200: TSTB  @XCSR1A
13 172266 100375                BPL     SN200
14
15
16 172270 042737 000001 177564  BIC     #1,@XCSR1A
17
18 172276 000207                RETURN
19
20
21
22
23
24
25
26
27
28 172300          SEND:
29
30
31 172300          SD100:
32 172300 105737 177564          TSTR   @XCSR1A
33 172304 100375                BPL     SD100
34
35
36 172306 112137 177566          MOVP   (R1)+,@XBUF1A
37
38 172312 005302                DFC     R2
39
40 172314 001371                RNE     SD100
41
42 172316 000207                RETURN
43
44
45
```

;* PROCEDURE BREAK
;* * SEND BREAK FOR 8 CHAR. TIMES
;* * END UNTIL
;* * DO UNTIL TRANSMIT BUFFER EMPTY
;* * END UNTIL
;* * CLEAR BREAK
;* * RETURN FROM CALL
;* END BREAK
;* PROCEDURE SEND
;* * DO UNTIL DATA COUNT = 0
;* * * DO UNTIL TRANSMIT BUFFER EMPTY
;* * * END UNTIL
;* * * OUTPUT NEXT CHAR. PER POINTER
;* * * DECREMENT DATA COUNTER
;* * END UNTIL
;* * RETURN FROM CALL
;* END SEND

```
1 172320 004 INITST: .BYTE 4
2 172321 004 .BYTE 4
3
4 172322 004 BOOTST: .BYTE 4
5 172323 010 .BYTE 10
6 .EVEN
7
8
```

```
1 .SBTTL PUTEST - POWER UP SELF TEST
2 .ENABLE GBL,LC
3
4 ;
5 ; Module name: POWER UP SELF TEST - PUTEST
6 ;
7 ; System: KXT11-CA Native Firmware
8 ;
9 ;
10 ;
11 ;
12 ; Functional Description:
13 ;
14 ; This module controls the execution of the Power Up Auto Self Tests.
15 ; It determines which of the test are to be executed per the Boot/Self Test
16 ; selection. This routine also tests the Status Register of the DPR regardless
17 ; of the Boot/Self Test Selection and halts the KXT if the test fails.
18 ;
19 ; Note:
20 ;
21 ; There are two important addresses with regard to the Power Up Self
22 ; Tests. PARSTR (defined in this module) is the address the KXT will be
23 ; looping at if the Status Register is found to be faulty. PTLST (defined
24 ; in the EXTEST module) is the address that the KXT will be looping at if
25 ; any other fatal self test error is found.
26 ;
27 ;
28 ; Input Parameters:
29 ;
30 ; BOOTFD(R5) - Boot selection location
31 ;
32 ; Output Parameters:
33 ;
34 ; None
35 ;
36 ; Routines Used:
37 ;
38 ; 1) Set LEDs (SETLFD)
39 ; 2) Execute Test (EXTEST)
40 ;
41 ;
42 ;
```

```

1 172324          PUTEST::
2
3
4 172324 005037 175004          CLR      @#KW.SC2
5
6
7
8 172330 012702 175002          MOV      #KW.STA,R2
9 172334 011200          MOV      (R2),R0
10 172336 012701 052525         MOV      #52525,R1
11 172342 010112         MOV      R1,(R2)
12 172344 020112         CMP      R1,(R2)
13 172346 001004         BNE     PU20
14 172350 005112         COM     (R2)
15 172352 005101         COM     R1
16 172354 020112         CMP      R1,(R2)
17 172356 001405         BEQ     PU30
18
19 172360          PU20:
20
21
22 172360 012700 000017         MOV      #FERRD,R0
23 172364 004767 174610         CALL   SETTLED
24
25 172370 000777          FARSTR:: BR
26
27 172372          PU30:
28
29 172372 010012         MOV      R0,(R2)
30
31 172374 016500 177774         MOV      BOOTFO(R5),R0
32 172400 005700          TST     R0
33 172402 001414          BEQ     PU50
34 172404 022700 000004         CMP      #4,R0
35 172410 101013         BHI     PU100
36
37 172412 022700 000005         CMF     #5,R0
38 172416 001410         BEQ     PU100
39
40 172420 022700 000010         CMP      #8,R0
41 172424 001405         BEQ     PU100
42
43 172426 022700 000012         CMP      #10,R0
44 172432 001402         BEQ     PU100
45 172434 000167 000126         PU50:  JMP     PU1010
46 172440          PU100:
47
48
49 172440 042712 177770         BIC     #^C<KMSSTF>,(R2)
50 172444 052712 000001         BIS     #KPSSTS,(R2)
51
52 172450 012700 000007         MOV      #PUTSDS,R0
53 172454 004767 174520         CALL   SETTLED
54
55 172460 052767 000100 005042         BIS     #KXSDEN,KW.CST
56
57 172466 012702 000004         MOV      #4,R2

```

```

;* PROCEDURE POWER UP SELF TEST
;* * CLEAR ALL ERROR BITS IN DPR 2
;* * TEST DPR STATUS REGISTER BY WRITING
;* * ALTERNATING 1'S AND 0'S INTO IT AND
;* * COMPARING WHAT IS READ BACK
;* * IF TEST FAILED
;* * THEN
;* * * SET LEDS AND STATUS REGISTER TO FATAL ERROR
;* * * STOP
;* * END IF
;* * RESTORE STATUS REGISTER
;* * IF BOOT/SELF TEST SELECTION = 1,2,3
;* * OR 5
;* * OR 8
;* * OR 10
;* * THEN
;* * * SET STATUS REGISTER TO AUTO TEST MODE STATE
;* * * SET LEDS TO POWER UP TEST DISPLAY
;* * * ENABLE DPR
;* * * TEST CPU

```

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```

58 172472 004767 000072      CALL    EXTEST
59
60 172476 012702 000002      MOV     #2,R2
61 172502 004767 000062      CALL    EXTEST
62
63 172506 022765 000002 177774      CMP     #2,BOOTFO(R5)
64 172514 001404                BFQ     PU400
65
66 172516 022765 000011 177774      CMP     #9,,BOOTFO(R5)
67 172524 001003                BNE     PU500
68 172526                PU400:
69
70
71 172526 012701 000001      MOV     #1,R1
72 172532 000401                BR      PU600
73
74 172534                PU500:
75
76 172534 005001                CLR     R1
77
78 172536                PU600:
79
80 172536 012702 000003      MOV     #3,R2
81 172542 004767 000022      CALL    EXTFST
82
83 172546 012702 000001      MOV     #1,R2
84 172552 004767 000012      CALL    EXTEST
85
86 172556 012702 000011      MOV     #11,R2
87 172562 004767 000002      CALL    EXTEST
88
89 172566                PU1010:
90
91 172566 000207                RETURN
92

```

```

; * * * TEST RAM
; * * * IF BOOT/SELF TEST SELECTION = 2
; * * * OR 9
; * * * THEN
; * * * INCLUDE USER ROM IN TEST
; * * * FLSE
; * * * DO NOT INCLUDE USER ROM IN TEST
; * * * FND IF
; * * * TEST ROM
; * * * TEST CSR
; * * * TEST LOCAL DMA
; * * END IF
; * * RETURN FROM CALL
; * END POWER UP SELF TEST

```

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```

1          .SBTTL  EXTEST - EXECUTE TEST
2
3          .ENABLE  GBL,LC
4
5          ;
6          ; Module name: EXTEST - EXECUTE TEST
7          ;
8          ; System: KXT11-CA Native Firmware
9          ;
10         ;
11        ;
12        ; Functional Description:
13        ;
14        ; This module is used by PUTEST to call a particular self test and display any
15        ; error results in the LEDs and the DPR. It will also halt the KXT if a fatal
16        ; error is found.
17        ;
18        ; Input Parameters:
19        ;
20        ; R1 = TEST PARAMETERS
21        ; R2 = TEST NUMBER

```

```

1
2 172570          EXTEST::          ;* PROCEDURE TEST
3
4 172570 004767 000616          CALL  DINIT          ;* * INITIALIZE IO
5
6 172574 010246          MOV   R2,-(SP)       ;* * SAVE TEST NUMBER
7
8 172576 013746 177524          MOV   @#KW.CSC,-(SP) ;* * SAVE LED STATE
9
10 172602 010146          MOV   R1,-(SP)       ;* * SAVE TEST PARAMETER
11
12 172604 052737 010000 175002    BIS   #KXSNXF,@#KW.STA ;* * SET NXM FLAG OF STATUS REGISTER
13
14 172612 022702 000007          CMP   #7,R2          ;* * IF TEST NUMBER < 7
15 172616 103404          BLO  TF100           ;* * THEN
16
17
18 172620 042737 000040 177520    BIC   #KXSDPE,@#KL.CSA ;* * CLEAR ROM MAP BIT
19 172626 000405          BF   TE200           ;* * ELSE
20
21 172630          TE100:           ;* * SET ROM MAP BIT
22
23 172630 052737 000040 177520    BIS   #KXSDPE,@#KL.CSA ;* * SUBTRACT 8 FROM TEST NUMBER
24
25 172636 162702 000010          SUB   #10,R2         ;* * END IF
26
27 172642          TE200:           ;* * PERFORM TEST
28
29 172642 006302          ASL  R2              ;MULT. TEST NO. BY 4
30 172644 006302          ASL  R2
31 172646 004762 160000          CALL T0(R2)
32
33 172652 042737 010000 175002    BIC   #KXSNXF,@#KW.STA ;* * CLEAR NXM FLAG OF STATUS REGISTER
34
35 172660 012601          MOV   (SP)+,R1       ;* * RETRIEVE TEST PARAMETER
36
37 172662 012637 177524          MOV   (SP)+,@#KW.CSC ;* * RESTORE LED STATE
38
39 172666 011602          MOV   (SP),R2        ;* * RETRIEVE TEST NUMBER (BUT LEAVE ON STACK)
40
41 172670 010003          MOV   R0,R3          ;* * SAVE TEST RESULTS
42
43 172672 006302          ASL  R2              ;* * SET LEDS PFR RESULTS
44 172674 004772 172746          CALL @<<RRT3-2>>(R2) ;* * RETRIEVE TEST NUMBER
45
46 172700 012602          MOV   (SP)+,R2       ;* * IF SIGNIFICANT ERROR
47
48 172702 005700          TST  R0              ;* * THEN
49 172704 001410          BFEQ TE300           ;* * SET ERROR BIT OF TEST IN DPR 2
50
51
52 172706 005000          CLR  R0              ;* *
53 172710 000261          SEC
54 172712 006100          MVL  R0              ;* *
55 172714 077202          SOB  R2,TE250
56 172716 050037 175004          BIS  R0,@#KW.SC2    ;* *
57

```

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;* * * PLACE DISCRETE ERROR DATA IN DPR 3


```

58 172722 010337 175006          MOV    R3,@#KW.SC3          ;* * END IF
59
60 172726                      TE300:          ;* * IF FATAL ERROR
61
62 172726 032737 000040 175002    BIT    #KXSFEF,@#KW.STA    ;* * THEN
63 172734 001401                      BEQ    TE400                ;* * * STOP
64
65
66 172736 000777                      FTLST:: BR    .            ;* * END IF
67
68 172740                      TE400:          ;* * FNABLE OVERLAY 0
69
70 172740 042737 000040 177520    BIC    #KXSDPE,@#KW.CSA    ;* * RETURN FROM CALL
71
72 172746 000207                      RETURN                    ;* END TEST
73
74
75
76
77 172750 170506          ERR3:  .WORD  T1ERR
78 172752 170546          .WORD  T2ERR
79 172754 170576          .WORD  T3ERR
80 172756 170642          .WORD  T4ERR
81 172760 170650          .WORD  T5ERR
82 172762 170656          .WORD  T6ERR
83 172764 170664          .WORD  T7ERR
84 172766 170720          .WORD  T10ERR
85 172770 170726          .WORD  T11ERR
86 172772 170734          .WORD  T12ERR
87 172774 170742          .WORD  T13ERR
  
```

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```

1
2
3          173000          .SBTTL ENTRY POINT
4          .=173000
5          .FNABLE GBL,LC
6          ; Functional Description:
7          ;
8          ; These are the entry points to the native firmware
9
10         ; Power Up entry point
11
12 173000 000167 000006    PERV:: JMP    PWRUP
13
14         ; kestart entry point
15
16 173004 000167 170770    RSTV:: JMP    RESTRT
17
  
```

```
1
2
3
4      173012
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
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53
```

.SBTTL PWRUP - POWER UP HANDLER
.ENABLE GBL,LC
. =173012

; Module name: PWRUP - POWER UP
; System: KXT11-CA Native Firmware
;
;
; Functional Description:
; This routine services the Power Up Interrupt at location 173000.
; Input Parameters:
; NONE
; Output Parameters
; 1. R5 = Top of RAM Pointer
; Data Structures
; 1. BATTERY BACKUP POWER UP FLAG (STATUS REGISTER)
; 2. POWER UP FLAG (STATUS REGISTER)
; 3. BATTERY BACKUP FLAG 1
; 4. BATTERY BACKUP FLAG 2
; 5. Map Selection Bits (KXTCSR B, bits 1-3)
; 6. Boot Flag (BOOTFO)
; Routines Used
; 1. INIT
; 2. PTEST
; 3. BSUPV (jump to)
; 4. SETTLED
; 5. TRAP24 (jump to)

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```

1
2 173012                                PWRUP::                                ;* PROCEDURE POWER UP
3
4
5
6 173012 005004                          CLR      R4                                ;* * IF POWER UP VECTOR ENTRY
7 173014 000404                          BR       PW050                             ;* * THEN
8
9 173016                                REINIT::                                ;* * * SET R4 = 0
10
11 173016 012704 000001                    MOV      #1,R4                             ;* * * ELSE
12
13 173022 013703 175066                    MOV      @#KW.SC3,R3                       ;* * * SET R4 = 1
14
15 173026                                PW050:                                ;* * * SAVE DPR REGISTER 3
16
17 173026 012737 000212 177526            MOV      #212,@#C8255                       ;* * END IF
18
19 173034 005037 177530                    CLR      @#KW.CSD                           ;* * INITIALIZE THE 8255
20
21 173040 012700 000020                    MOV      #20,R0                             ;* * CLEAR ALL KXT CSR'S
22 173044 012701 175000                    MOV      #KW.CMD,R1                         ;* * CLEAR THE DUAL PORT RAM
23 173050 005021                            PW100:  CLR      (R1)+!
24 173052 077002                            SOB      R0,PW100
25
26 173054 005737 177562                    TST      @#RBUF1A                           ;* * READ SLU1 TO CLEAR ANY PENDING BREAKS
27
28 173060 152737 000017 177524            B1SB    #<KXSLD0 ! KXSLD1 ! KXSLD2 ! KXSLD3>,@#KW.CSC ;* * SEQUENCE LEDS (ON-.5 SEC.-OFF)
29 173066 005000                            CLR      R0
30 173070 077001                            SOB      R0,.
31 173072 077001                            SOB      R0,.
32 173074 142737 000017 177524            B1CB    #<KXSLD0 ! KXSLD1 ! KXSLD2 ! KXSLD3>,@#KW.CSC ;* * INITIALIZE STACK POINTER AND SET R5 TO TOP OF RAM
33
34 173102 012700 173112                    MOV      #PW200,R0
35 173106 000167 000574                    JMP      SPR5SU
36 173112                                PW200:
37
38 173112 005704                          TST      R4
39 173114 001403                          BEQ      PW300
40
41 173116 022703 000010                    CMP      #8,,R3
42 173122 001013                          BNE      PW500
43 173124                                PW300:
44
45
46 173124 113700 177522                    MOVB    @#KL.CSB,R0
47 173130 042700 177417                    BIC     #<C<KMSSWS>,R0
48 173134 006200                            ASK     R0
49 173136 006200                            ASR     R0
50 173140 006200                            ASR     R0
51 173142 006200                            ASR     R0
52 173144 010065 177774                    MOV     R0,BOOTFO(R5)
53 173150 000402                            BR      PW600
54
55 173152                                PW500:
56
57 173152 010365 177774                    MOV     R3,BOOTFO(R5)

```

```

58                                     ;* * END IF
59 173156                               PW600:
60                                     ;* * IF POWER UP ENTRY
61 173156 005704                        TST   R4
62 173160 001034                        BNE   PW700
63                                     ;* * AND BATTERY BACKUP FLAG 1 = 125252
64 173162 022765 125252 000000         CMP   #125252, RBF10(R5)
65 173170 001030                        BNE   PW700
66                                     ;* * AND BATTERY BACKUP FLAG 2 = 52525
67 173172 022765 052525 177776         CMP   #52525, RBF20(R5)
68 173200 001024                        BNE   PW700
69                                     ;* * THEN
70                                     ;* * SET BATTERY BACKUP POWER UP FLAG
71                                     ;* * OF STATUS REGISTER = 1
72 173202 052737 002000 175002         BIS   #KX$BAT, @#KW.STA
73 173210 042737 001000 175002         BIC   #KX$PWF, @#KW.STA
74                                     ;* * * INITIALIZE I/O
75 173216 004767 000060                CALL  INIT
76                                     ;* * * SET STATUS REGISTER TO NON NATIVE
77                                     ;* * CODE STATE
78 173222 042737 000007 175002         BIC   #KMSSTF, @#KW.STA
79 173230 052737 000007 175002         BIS   #KPSNNC, @#KW.STA
80                                     ;* * * SET LEDS TO NON NATIVE CODE STATE DISP.
81 173236 012700 000000                MOV   #NNCED, RO
82 173242 004767 173732                CALL  SETTLED
83                                     ;* * * EMULATE TRAP TO 24 (NON STRUCTURED EXIT)
84 173246 000167 174104                JMP   TRAP24
85                                     ;* * FLSE
86 173252                               PW700:
87                                     ;* * * RUN SELF TEST
88 173252 004767 177046                CALL  PTEST
89                                     ;* * * INITIALIZE I/O
90 173256 004767 000020                CALL  INIT
91                                     ;* * * SET POWER UP FLAG OF STATUS REGISTER = 1
92 173262 052737 001000 175002         BIS   #KX$PWF, @#KW.STA
93 173270 042737 002000 175002         BIC   #KX$BAT, @#KW.STA
94                                     ;* * * BOOT IOP (JUMP TO BOOTSTRAP SUPERVISOR)
95 173276 000167 175666                JMP   BSUPV
96                                     ;* * END IF
97                                     ;* END POWER UP

```

```
1 .SBTTL INIT - INITIALIZATION
2 .ENABLE LC,GBL
3
4
5 ;
6 ; Module name: INIT - INITIALIZATION
7 ;
8 ; System: KXT11-CA Native Firmware
9 ;
10 ;
11 ;
12 ;
13 ;
14 ;
15 ; Functional Description:
16 ;
17 ; This module resets and initializes the DMA controller, 7201 and
18 ; PIO. It also places the configuration data in the dual port RAM
19 ; and enables the dual port RAM.
20 ;
21 ;Input Parameters:
22 ;
23 ; NONF
24 ;
25 ;Output Parameters
26 ;
27 ; 1. Reset DMA,7201,PIO
28 ;
29 ; 2. PIO Master Interrupt Register
30 ;
31 ; 3. " Port 1 Intr. Vec. Reg.
32 ;
33 ; 4. " " 2 " " "
34 ;
35 ; 5. " Timer " " "
36 ;
37 ;
```

```

1
2 173302          INIT::          ;* PROCEDURE INITIALIZATION
3
4 173302 004767 000104          CALL  DINIT          ;* * INITIALIZE IO
5
6
7 173306 042737 174770 175002  BIC   #^C<<KMSSTF ! KX$MPF ! KX$BAT>>,@#KW.STA ;* * CLEAR ALL OF STATUS REGISTER EXCEPT STATE FIELD
8
9 173314 005737 175004          TST   @#KW.SC2        ; AND POWER UP FLAGS
10 173320 001030          BNE   IN400          ;* * IF NO AUTO SELF TEST ERRORS FOUND
11
12
13 173322 013700 177522          MOV   @#KW.CSB,R0    ;* * THEN
14 173326 042700 177401          BIC   #^C<<KMSMAP ! KMSSWS>>,R0 ;* * * PLACE IOP MAP & BOOT CONFIGURATION IN DPR REGISTER 3
15 173332 010037 175006          MOV   R0,@#KW.SC3
16
17 173336 032737 000010 177522  BIT   #KX$MP2,@#KL.CSB ;* * * IF USER SOCKETS MAPPED TO 0
18 173344 001402          BFC   IN100
19
20
21 173346 005000          CLR   R0             ;* * * THEN
22 173350 000402          BR    IN200          ;* * * * TEST FOR RAM AT 0
23
24 173352          IN100:          ;* * * ELSE
25
26 173352 012700 100000          MOV   #100000,R0    ;* * * * TEST FOR RAM AT 100000
27
28 173356          IN200:          ;* * * END IF
29
30 173356 011001          MOV   (R0),R1        ;* * * IF RAM PRESENT
31 173360 005101          COM   R1
32 173362 005110          COM   (R0)
33 173364 020110          CMP   R1,(R0)
34 173366 001005          BNE   IN300
35
36
37 173370 005101          COM   R1             ;* * * THEN
38 173372 010110          MOV   R1,(R0)        ;* * * * ReSTORE CONTENTS
39
40 173374 052737 000001 175006  BIS   #BIT0,@#KW.SC2 ;* * * * SET RAM PRESENT BIT OF DPR REG. 3
41
42 173402          IN300:          ;* * * END IF
43
44 173402          IN400:          ;* * END IF
45
46 173402 052737 000100 177530  BIS   #KX$DEN,@#KW.CSD ;* * ENABLE THE DUAL PORT RAM
47
48 173410 000207          RETURN              ;* * RETURN
49
                                     ;* END INITIALIZATION

```

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```

1          .SBTTL DINIT - DEVICE INITIALIZATION
2          .ENABLE LC,GBL
3
4
5          ;
6          ; Module name: DINIT - I/O DEVICE INITIALIZATION
7          ;
8          ; System: KXT11-CA Native Firmware
9          ;
10         ;
11         ;
12         ;
13         ; Functional Description:
14         ;
15         ; Initialize all programmable I/O devices. Disables interrupts and sets
16         ; programable interrupt vector addresses.
17         ;

```

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```

1          ;* PROCEDURE DINIT
2 173412          DINIT::
3
4 173412 005037 174454          CLR          @#DMACDA          ;* * RESET DMA
5
6 173416 113700 175700          MOVB          @#SL2SAA,R0          ;* * RESET 7201
7 173422 112737 000030 175704          MOVB          #30,@#SL2CAA
8 173430 112737 000030 175714          MOVB          #30,@#SL2CBA
9 173436 112737 000002 175704          MOVB          #2,@#SL2CAA
10 173444 112737 000024 175704          MOVB          #24,@#SL2CAA
11 173452 112737 000001 175714          MOVB          #1,@#SL2CBA          ;(SET STATUS EFFECTS VECTOR BIT)
12 173460 112737 000004 175714          MOVB          #4,@#SL2CBA
13
14 173466 112737 000001 177000          MOVB          #01,@#PIOICA          ;* * RESET PIO
15 173474 105037 177000          CLRB          @#PIOICA
16
17 173500 112737 000200 177004          MOVB          #200,@#PIOAVA          ;* * SETUP PIO PORT A INTERRUPT VECTOR REGISTER
18
19 173506 112737 000204 177006          MOVB          #204,@#PIOBVA          ;* * SETUP PIO PORT B INTERRUPT VECTOR REGISTER
20
21 173514 112737 000210 177010          MOVB          #210,@#PIOTVA          ;* * SETUP PIO TIMER INTERRUPT VECTOR REGISTER
22
23 173522 112737 000110 174532          MOVB          #110,@#DMAOVA          ;* * SETUP DMA CHANNEL 0 INTERRUPT VECTOR REGISTER
24
25 173530 112737 000114 174530          MOVB          #114,@#DMA1VA          ;* * SETUP DMA CHANNEL 1 INTERRUPT VECTOR REGISTER
26
27 173536 000207          RETURN          ;* END DINIT

```

```

1          .SBTTL ACCUM - ACCUMULATE NUMBER
2          .ENABLE LC,GBL
3
4          ;
5          ; Module name: ACCUMULATE - ACCUM
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ; Functional Description:
14         ;
15         ; This routine accumulates a 16 bit number by shifting the previous
16         ; accumulation left 3 and "or"ing the new input value (which is a single
17         ; octal digit value) into the accumulation.
18
19
20         ;Input Parameters:
21
22         ; 1) R0 = OCTAL DIGIT INPUT
23         ; 2) R4 = PREVIOUS ACCUMULATED NUMBER
24
25         ;Output Parameters:
26
27         ; 1) R4 = ACCUMULATED NUMBER
28
29         ;Routines Used:
30
31         ; None
  
```

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```

1          ;* PROCEDURE ACCUMULATE
2 173540          ACCUM::
3
4 173540 006304          ASL      R4
5 173542 006304          ASL      R4
6 173544 006304          ASL      R4
7
8 173546 050004          BIS      R0,R4
9
10 173550 000207          RETURN
  
```



```

1          .SBTTL GETIN - GET INPUT
2          .ENABLE LC,GBL
3
4          ;
5          ; Module name: GET INPUT - GETIN
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ; Functional Description:
14         ;
15         ; This routine inputs a character and sets the non numeric flag if the
16         ; input is not a number. If the input is a number it is converted to binary,
17         ; clears the non-numeric flag and sets the data received flag.
18         ;
19         ; Output Parameters:
20         ;
21         ; 1) Data Received flag - DARFGB of R3
22         ; 2) Non Numeric Flag - Carry Flag
23         ; 3) Input Data, - R0
  
```

```

1
2 173552          GETIN::
3
4                                     ;* PROCEDURE GET INPUT
5 173552 004767 000036          GE100: CALL   CHKCHR          ;* * DO UNTIL INPUT
6                                     ;* * END UNTIL
7 173556 103375          BCC     GE100          ;* * IF INPUT = 0 THRU 7
8                                     ;* * THEN
9 173560 122700 000060          CMPB   #*0,R0
10 173564 101011          BHI     GE200
11 173566 122700 000067          CMPB   #*7,R0
12 173572 103406          BLO     GE200
13                                     ;* * * CONVERT TO BINARY
14                                     ;* * * SET DATA RECEIVED FLAG
15 173574 162700 000060          SUB     #60,R0
16                                     ;* * * CLEAR NON NUMERIC FLAG
17 173600 052703 000002          BIS     #DARFGB,R3
18                                     ;* * ELSE
19 173604 000241          CLC
20 173606 090401          BR      GE300
21                                     ;* * * SET NON NUMERIC FLAG
22 173610          GE200:
23                                     ;* * END IF
24 173610 000261          SEC
25                                     ;* * RETURN FROM CALL
26 173612          GE300:
27                                     ;* * END GET INPUT
28 173612 000207          RET'RN
29
30
  
```

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```
1          .SBTTL  CHKCHR - CHECK CHARACTER
2          .ENABLE GBL,LC
3
4          ;
5          ; Module name: CHKCHR - CHECK CHARACTER
6          ;
7          ; System: Micro-PAX RTS
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ; This module tests the console serial line receive buffer for a
17         ; character, signals if one was received, echos the character
18         ; and returns that character to the calling routine.
19         ; This module is to be used for input polling. It
20         ; will handle XON XOFF protocol. This routine will not ecco
21         ; the XON or XOFF characters.
22
23         ;INPUT PARAMETERS
24
25         ;      NONE
26
27         ;OUTPUT PARAMETERS
28
29         ;      1) CARRY BIT = 1 FOR CHARACTER RECEIVED, = 0 FOR NO CHARACTER
30         ;      2) R0 = RECEIVE BUFFER DATA, IF DATA RECEIVED
31
32         ;DATA STRUCTURES USED
33
34         ;      1) SLU1 CSR
35         ;      2) SLU1 RECEIVE BUFFER
36
37         ;ROUTINES USED
38
39         ;      NONE
```

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```
1          000021          XON   =      *Q-100
2          000023          XOFF  =      *S-100
```



```
1          .SBTTL SPR5SU - SP/R5 SETUP
2          .ENABLE LC,GBL
3
4          ;
5          ; Module name: SP AND R5 SETUP - SPR5SU
6          ;
7          ; System: KXT11-CA Native Firmware
8          ;
9          ;
10         ;
11         ;
12         ;
13         ;
14         ; Functional Description:
15         ;
16         ;       This module sets up the SP to the native firmware stack area and
17         ; setting R5 to the address of the last word of native RAM.
18         ;
19         ;
20         ; Input Parameters:
21         ;
22         ;       1) Return address in R0
23         ;
24         ; Output Parameters:
25         ;
26         ;       1) Top of RAM address in R5
27         ;       2) Stack Pointer
28
```

```

1
2
3 173706          SPR5SU::          ;* PROCEDURE SP AND R5 SETUP
4
5                ;* * CASE MAP SELECTION
6 173706 132737 000010 177522      BITB  #KXSMP2,@#KW.CSB ;* * WHEN MAP BIT 2 = 0
7 173714 001003          BNE      SP200
8
9 173716 012706 077762          MOV   #SP1,SP ;* * * SET STACK POINTER TO STACK 1
10 173722 000415          BR     SP400
11
12 173724 132737 000002 177522 SP200: BITB  #KXSMP0,@#KW.CSB ;* * WHEN MAP BITS 0 AND 1 = 11
13 173732 001407          BEQ   SP300
14 173734 132737 000004 177522      BITB  #KXSMP1,@#KW.CSB
15 173742 001403          BEQ   SP300
16
17 173744 012706 157762          MOV   #SP3,SP ;* * * SET STACK POINTER TO STACK 3
18 173750 000402          BR     SP400
19
20 173752          SP300:          ;* * ELSE
21
22 173752 012706 137762          MOV   #SP2,SP ;* * * SET STACK POINTER TO STACK 2
23
24 173756          SP400:          ;* * END CASE
25
26 173756 010605          MOV   SP,R5 ;* * SET R5 = TOP OF RAM (SP + STACK OFFSET)
27 173760 062705 000014          ADD  #SPOFF,R5
28
29 173764 000110          JMP   (R0) ;* * RETURN TO CALLER
30
                ;* END SP AND R5 SETUP

```

```
1 .SBTTL VERS - VERSION NUMBER AND TEST
2 173774 .=173774
3 .FNAELE LC
4
5 ;
6 ; Module name: VERS - VERSION NUMBER
7 ;
8 ; System: KXT11-CA Native Firmware
9 ;
10 ;
11 ;
12 ;
13 ;
14 ;
15 ; Functional Description:
16 ;
17 ; This module places the version number in the last word of the
18 ; permanently mapped native ROM.
19
20 173774 126 061 056 VERS:: .ASCII "V1.0"
```

```
1 .SBTTL SELF TEST OVERLAY 1
2 .LIST ME,MEB,SEQ,LOC,BIN ; NORMAL LISTING MODE
3 .NLIST MC,CND,BEX ; DITTO
4 .ENABL AMA,GBL
5 174000 .=174000
6
7 ;
8 ; Module name: SELF TEST OVERLAY 1
9 ;
10 ; System: KXT11-CA Native Firmware
11 ;
12 ;
13 ;
14 ;
15 ;
16 ;
17 ; Functional Description:
18 ;
19 ; This module contains overlay 1 of the self test code. The self test
20 ; modules in this overlay are:
21 ;
22 ; Parallel I/O port Z8036,
23 ; DMA controller Z8016,
24 ; Q-BUS interrupts, and
25 ; Two-port RAM.
26 ;
27 ; Overlay 1 physically occupies the top 2 KB of the boot ROM. It
28 ; executes starting at 160000 when the DIAG PROM EN bit, bit 5, in
29 ; KXTCSRA is 1.
```

```

1          ;          SCRATCH RAM ALLOCATION.
2          ;
3          ; R5 IS ODT'S "TOP-OF-MEM" POINTER, AND IS PRESERVED AS SUCH.
4          ; ALL SCRATCH REFERENCES ARE INDEXED FROM R5 AS FOLLOWS:
5          ;
6          ;
7          ;
8          000005      $TOP=   %5          ; 077776 137776 157776
9          ;
10         150002      BUFR1= -27776       ; 050000 110000 130000 TOP-6KW
11         160002      BUFR2= -17776       ; 060000 120000 140000 TOP-4KW
12         170002      TMP1=  -07776       ; 070000 130000 150000 TOP-2KW
13         170004      TMP2=  TMP1+2       ;
14         170006      TMP3=  TMP1+4       ;
15         170010      TMP4=  TMP1+6       ;
16         170012      TMP5=  TMP1+10      ;
17         170014      TMP6=  TMP1+12      ;
18         170016      TMP7=  TMP1+14      ;
19         170020      TMP8=  TMP1+16      ;
20         177776      SEF1=  -2           ; LAST 2 WORDS OF NATIVE RAM (BATTERY-BACK-FLAGS)...
21         000005      SEF=   $TOP         ; ...ARE UTILIZED AS OUR ERROR FLAGS.
22         ;
23         ; MISCELLANEOUS STUFF.
24         ;
25         000007      $TN=   7             ; INIT TEST NUMBER SEQUENCE.
26         014000      K3K=  3072.*2      ; HISEG CALLS REQUIRE 3KW OFFSET.
27         ;
28         ; A FEW MACROS.
29         ;
57         ;
78         ;
91         ;
97         ;
98         ;
99         ;
          .NLIST MD
  
```

> SCRATCH REGISTERS...
 ...AND STACK SPACE.

132

```

1          ; A FEW DEFINITIONS
2          ;
3          ; STANDARD STUFF.
4          ;
5          000000      PR0=      000          ; THE PRIORITIES.
6          000040      PR1=      040
7          000100      PR2=      100
8          000140      PR3=      140
9          000200      PR4=      200
10         000240      PR5=      240
11         000300      PR6=      300
12         000340      PR7=      340
13         ;
14         ; PRIMARY CONTROL REGISTERS.
15         ;
16         177560      $SL1= 177560          ; DEC DC319 (DLART) ASYNC SERIAL PORT.
17         175700      $SL2= 175700          ; NFC7201 SYNC/ASYNC SERIAL PORT.
18         175720      $I8254= 175720        ; I8254 PROGRAMMABLE BAUD GEN FOR ABOVE.
19         177000      $PIO= 177000         ; Z8036 PIO/PIT.
20         174400      $DMA= 174400         ; AMZ8016 DMA CONTROLLER.
21         177520      $CSRA= 177520        ; \
22         177522      $CSRB= 177522        ; > SECONDARY CSR'S...
23         177524      $CSPC= 177524        ; / ...EMBEDDED IN I8255,CHIP.
24         177526      $CSRCON= 177526      ;
25         177530      $CSR= 177530         ; PRIMARY CSR.
26         177532      $QIR= 177532         ; Q-BUS INTERRUPT REGISTER.
27         175000      $DPR= 175000         ; DUAL-PORT RAM (LOCAL).
28         160000      $QDPR1= 160000       ; DUAL-PORT RAM (GLOBAL BASE ID 0-7...
29         175400      $QDPR2= 175400       ; ...AND ID 8-F).
30         ;
31         175000      $IPV= $DPR           ; IPV INTERUPTS (VIA DPR WORDS 0, 4, 8, AND 12).
32         177524      $LEDS= $CSRC        ; CSRC<3:0> DRIVE THE LEDS.
33         177524      $UID= $CSRC         ; CSRC<7:4> SHOW THE ID SWITCH SETTING.

```

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```

1          ; DEFAULT VECTORS.
2          ;
3          000024      PWR= 024          ; PWR-UP (BRESET)          (NON-MASKABLE).
4          000060      SL1RV= 060        ; CONSOLE (SLU1) RCVR    (PRI 4).
5          000064      SL1XV= 064        ; CONSOLE (SLU1) XMTR    (PRI 4).
6          000070      NECV= 070        ; SYNC/ASYNC BOTH CHANS (PRI 4).
7          000100      BEVNT= 100        ; LINE CLOCK             (PRI 6).
8          000104      PEVNT= 104        ; PROGRAMMABLE CLOCK(S) (PRI 6).
9          ;
10         000114      PRTYV= 114        ; MEMORY PARITY          (PRI 7).
11         000120      DPRV4= 120        ; DUAL-PORT RAM WORD 4   (PRI 5).
12         000124      DPRV8= 124        ; DUAL-PORT RAM WORD 8   (PRI 5).
13         000130      BIACKV= 130       ; Q-BUS "IACK"           (PRI 5).
14         000134      DPRV12= 134       ; DUAL-PORT-RAM WORD 12 (PRI 5).
15         ;
16         000144      QIRV= 144         ; Q-BUS REQUEST          (ARBITER EXECUTES RTI).
17         000150      QIRV1= 150        ; DITTO                  (ARBITER EXECUTES RESET,RTI)
18         000154      PIOAV= 154        ; PIO PORT A             (PRI 4).
19         000160      PIOBV= 160        ; PIO PORT B             (PRI 4).
20         000164      DMAV= 164         ; DMA (BOTH CHANNELS)    (PRI 4).
  
```

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1          ; HIGH SEGMENT ENTRY BLOCK
2          ;
3          ; CALL: BIS #BIT5,CSRA ; ENABLE HIGH SEGMENT.
4          ; CALL TN          ; CALL TEST 10-17.
5          ; BEQ OK          ; OR BNE ERROR.
13         160000      T10==.-K3F
174000     000137     160040      JMP      TST10-K3K      ;; EXECUTE TEST 10.
160004
174004     000137     161106      JMP      TST11-K3K      ;; EXECUTE TEST 11.
160010
174010     000137     162102      JMP      TST12-K3K      ;; EXECUTE TEST 12.
160014
174014     000137     162432      JMP      TST13-K3K      ;; EXECUTE TEST 13.
160020
174020     005000      CLR      R0          ;SINCE THERE IS NO TEST BY THIS NAME, SHOW NO ERRORS.
174022     000207      RETURN
160024
174024     005000      CLR      R0          ;SINCE THERE IS NO TEST BY THIS NAME, SHOW NO ERRORS.
174026     000207      RETURN
160030
174030     005000      CLR      R0          ;SINCE THERE IS NO TEST BY THIS NAME, SHOW NO ERRORS.
174032     000207      RETURN
160034
174034     005000      CLR      R0          ;SINCE THERE IS NO TEST BY THIS NAME, SHOW NO ERRORS.
174036     000207      RETURN
  
```

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```

1          .SBTTL - T10 PARALLEL I/O PORT Z8036
          ;;*****
          ;;* TEST 10 -- PARALLEL I/O PORT Z8036
          ;;*****
          TST10:
          TP10:
          MOV     PEVNT,-(SP)      ;; SAVE PEVNT.
          MOV     PEVNT+2,-(SP)
          MOV     PIOAV,-(SP)     ;; SAVE PIOAV.
          MOV     PIOAV+2,-(SP)
          MOV     PIORV,-(SP)     ;; SAVE PIORV.
          MOV     PIOBV+2,-(SP)
          CLR     (SEF)           ;; CLEAR ERROR FLAG.

2          ;
3          ; INPUT: NONE.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; ZILOC 8036 CHIP HAS 48 REGISTFRS.
7          ; RESET THE CHIP AND VERIFY THAT ALL REGISTERS RETURN ZERO.
8          ;
9          ;
10         ; T10 PARALLEL I/O PORT Z8036
11         ; E0 = ROM IN VECTOR SPACE -- CAN'T RUN
12         ; E1 = RESET STATE INCORRECT
13         ; E2 = TIMER DIDN'T START
14         ; E3 = TIMER NEVER STOPS.
15         ; E4 = INTERRUPT NOT MASKED AT LEVEL 4
16         ; E5 = INTERRUPT NOT RECEIVED.
17         ; E6 = LOOP TIME-OUT, DATA XFER INCOMPLETE
18         ; E7 = RECEIVED DATA INCORRECT
19 174072 004737 163602          CALL  XRAMLO-K3K      ; VECTOR SPACE USABLE ??
20 174076 001404                  BFC     4$           ; PROCEED IF SO.
21 174100 052715 000001          BIS     #BIT0,(SEF)  ;; E0 = ROM IN VECTOR SPACE -- CAN'T RUN
22 174104 000137 160746          JMP     PTOXIT-K3K
23
24 174110 012703 000060          4$:   MOV     #48,R3      ; CHECK 48 REGISTERS...
25 174114 012704 177000          MOV     #SP10,R4      ; ...STARTING HERE.
26 174120 112714 000001          MOVB   #1,(R4)        ; SET "CHIP-RESET" IN MICR.
27 174124 122714 000001          CMPB   #1,(R4)        ; READ IT, SHOULD SEF THE 1 BIT.
28 174130 000403                  BR     2$             ; CHECK IT AT 2$.
29
30 174132 112714 177777          1$:   MOVB   #-1,(R4)   ; THEN, WRITES SHOULD BE IGNORED...
31 174136 105714                  TSTR   (R4)           ; ...AND READS RETURN ZERO.
32 174140 001402                  2$:   BFC     3$           ; BR IF OK.
33 174142 052715 000002          BIS     #BIT1,(SEF)  ;; E1 = RESET STATE INCORRECT
34 174146 005724                  3$:   TST    (R4)+      ; NEXT ADDRESS...
35 174150 077310                  SOB    R3,1$         ; ...AND LOOP 'TIL DONE.
36
37         ;
38         ; NEXT, SEE THAT EACH TIMER FUNCTIONS AS ADVERTISED.
39
39         000000          MIC=   000           ; MASTER INTERRUPT CONTROL REG.
40         000002          MCC=   002           ; MASTER CONFIGURATION CONTROL REG.
41         000010          CTV=   010           ; TIMER(S) INTERRUPT VECTOR REG.
42         000070          CTMS=  070           ; 1ST (OF 3) TIMER MODE SPEC REG.
43         000024          CTCS=  024           ; 1ST (OF 3) TIMER CMD/STATUS REG.
44         000054          CTTC=  054           ; 1ST (OF 6) TIME CONSTANT REG (3 PAIR).
45         000040          CTCC=  040           ; 1ST (OF 6) CURRENT COUNT REG (3 PAIR).

```

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46
47 174152 012704 177000 ; PIT: MOV #SPI0,R4 ; GET BASE ADDRESS.
48 174156 142714 000001 BICB #1,(R4) ; CLEAR "CHIP-RESET"...
49 174162 012703 000060 MOV #48,,R3
50 174166 005024 2$: CLR (R4)+ ;...AND CLEAR ALL REGISTERS.
51 174170 077302 SOB R3,2$
52 174172 012704 177000 MOV #SPI0,R4 ; GET BASE AGAIN.
53 174176 112714 000200 MOVB #200,(R4) ; SET "MASTER INT ENAB".
54 174202 112764 000104 000010 MOVB #PEVNT,CTV(R4) ; SET TO VECTOR THRU "PEVNT".
55 174210 112764 000160 000002 MOVE #160,MCC(R4) ; ENABLE ALL 3 TIMERS...
56 ;...CTMS = 0 = PULSE-OUT, ONCE-ONLY...
57 ;...CTTC = 0 = TIME K 65536.
58 174216 062704 000024 ADD #CTCS,R4 ; NOW RAISE R4 TO 1ST TIMER CSR.
59
60 174222 106427 000200 PIT1: MTPS #PR4 ; RAISE CPU TO PIO LEVEL.
61 174226 012737 160320 000104 MOV #35-K3K,PEVNT ; SET VECTOR.
62 174234 012737 000300 000106 MOV #PR6,PEVNT+2
63 174242 005000 CLR R0
64 174244 012701 000004 MOV #4,R1 ; SET A 1 SECOND KEEP-ALIVE TIMER.
65 174250 112714 000040 MOVB #40,(R4) ; CLEAR "IUSIIP"...
66 174254 112714 000306 MOVR #306,(R4) ;...AND SET "IEIGCBITCB"...
67 174260 000240 NOP ;...TIMER SHOULD TAKE-OFF !!
68 174262 132714 000001 1$: BITB #1,(R4) ; TIMER RUNNING (CIP=1) ??
69 174266 001004 BNE 2$ ; BR IF SO.
70 174270 077004 SOB R0,1$
71 174272 052715 000004 BIS #BIT2,(SEF) ; E2 = TIMER DIDN'T START
72 174276 000426 BR 7$ ; ABORT.
73 174300 132714 000001 2$: BITB #1,(R4) ; TIMER DONE (CIP=0) ??
74 174304 001411 BEQ 4$ ; BR IF SO.
75 174306 077004 SOB R0,2$
76 174310 077105 SOB R1,2$
77 174312 052715 000010 BIS #BIT3,(SEF) ; E3 = TIMER NEVER STOPS.
78 174316 000416 BR 7$ ; ABORT.
79
80 174320 000240 3$: NOP ; INTERRUPT -- SHOULD HAVE BEEN MASKED.
81 174322 052715 000020 BIS #BIT4,(SEF) ; E4 = INTERRUPT NOT MASKED AT LEVEL 4
82 174326 000411 BR 6$
83
84 174330 062737 000032 000104 4$:5$: ADD #65-3$,PEVNT ; NOW CHANGE THE VECTOR...
85 174336 106427 000000 MTPS #PK0 ;...LOWER THE CPU...
86 174342 000240 NOP ;...AND LET INTERRUPT COME IN.
87 174344 052715 000040 BIS #BIT5,(SEF) ; E5 = INTERRUPT NOT RECEIVED.
88 174350 000401 BR 7$
89
90 174352 022626 6$: CMP (SP)+,(SP)+ ; INTERRUPT -- FIX THE STACK.
91 174354 012714 000040 7$: MOV #40,(R4) ; CLEAR "IUSIPIGCB"...
92 174360 012714 000160 MOV #160,(R4) ;...AND "IE" (TIMER OFF).
93 174364 005724 TST (R4)+ ; BUMP TO NEXT TIMER CMD/STAT...
94 174366 020427 177032 CMP R4,#SPI0+CTCS+6
95 174372 103713 BLO PIT1 ;...AND LOOP 'TIL ALL 3 DONE.
96
97 174374 112737 000001 177000 MOVB #1,SPI0 ; THEN, RESET THE CHIP.
98 174402 000240 NOP ; FALL THRU TO DATA TEST.

```

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```

1
2 ; DATA PORT(S) TEST.
3 ;
4 ; *** REQUIRES EXTERNAL LOOP-BACK ***
5 ;
6 000004 PAV= 004 ; PORT A VECTOR...
7 000020 PACS= 020 ;...CMD/STATUS...
8 000032 PADB= 032 ;...DATA BUFFER...
9 000100 PAMS= 100 ;...MODE...
10 000102 PAHS= 102 ;...AND HANDSHAKE SPEC.
11 000006 PRV= 006 ; PORT B VECTOR...
12 000022 PBCS= 022 ;...CMD/STATUS...
13 000034 PBDB= 034 ;...DATA BUFFER...
14 000120 PBMS= 120 ;...MODE...
15 000122 PBHS= 122 ;...AND HANDSHAKE SPEC.
16 000014 PCDD= 014 ; PORT C DATA DIRECTION...
17 000036 PCDB= 036 ;...AND BUFFER (HANDSHAKE BITS).
18 000140 XCVR= 140 ; 1ST WORD ABOVE THE CHIP HOLDS...
19 164377 AI.BO= <350*400>1377 ;...XCVR CONTROL BITS TTL/A(IN)IB(OUT).
20 165400 AO.BI= <353*400>10 ; DITTO TTL/A(OUT)IB(IN).
21 ;
22 170002 BYTES= TMF1 ; DEFINE A SCRATCH LOCATION.
23 ;
24 174404 012704 177000 PIOD: MOV #SPIO,R4 ; GET BASE ADDRESS.
25 174410 142714 000001 BICR #1,(R4) ; CLEAR "CHIP-RESET".
26 174414 012701 000154 MOV #PIODV,R1
27 174420 010164 000004 MOV R1,PAV(R4) ; SET PORT A VECTORS.
28 174424 012721 161010 MOV #AI-K3K,(R1)+
29 174430 012721 000200 MOV #PK4,(R1)+
30 174434 010164 000006 MOV R1,PBV(R4) ; SET PORT B VECTORS.
31 174440 012721 161024 MOV #BI-K3K,(R1)+
32 174444 012721 000200 MOV #PR4,(R1)+
33 174450 112764 000100 000100 PIOD1: MOVB #100,PAMS(R4) ; SET PORT A INPUT...
34 174456 112764 000000 000102 MOVB #000,PAHS(R4) ;...INTERLOCKED HS...
35 174464 112764 000300 000020 MOVB #300,PACS(R4) ;...INT ENABLED.
36 174472 112764 000200 000120 MOVB #200,PBMS(R4) ; SET PORT B OUTPUT...
37 174500 112764 000000 000122 MOVB #000,PBHS(R4) ;...INTFRLOCKED HS...
38 174506 112764 000300 000022 MOVB #300,PBCS(R4) ;...INT ENABLED.
39 174514 112764 000200 000022 MOVB #200,PBCS(R4) ; SET OUT "IP" TO PRIME THE LOOP.
40 174522 012764 164377 000140 MOV #AI.BO,XCVR(R4) ; SET XCVR CONTROL BITS.
41 174530 000414 BR PIOD3
42 174532 112764 000200 000100 PIOD2: MOVB #200,PAMS(R4) ; CHANGE PORT A TO OUTPUT...
43 174540 112764 000200 000020 MOVB #200,PACS(R4) ;...AND SET OUT "IP".
44 174546 112764 000100 000120 MOVB #100,PBMS(R4) ; CHANGE PORT B TO INPUT.
45 174554 012764 165400 000140 MOV #AO.BI,XCVR(R4) ; CHANGE XCVR CONTROLS.
46 174562 106427 000200 PIOD3: MTPS #PR4 ; RAISE CPU.
47 174566 112764 000377 000014 MOVB #377,PCDD(R4) ; PORT C DIRECTION ALWAYS "IN".
48 174574 012702 163646 MOV #XFLT10-K3K,R2 ; XMT BUFFER POINTER => R2.
49 174600 010503 MOV $TOP,R3
50 174602 062703 150002 ADD #BUFRI,R3 ; RCV BUFFER POINTER => R3.
51 174606 010346 MOV R3,-(SP) ; SAVE A COPY OF R3.
52 174610 012700 000020 MOV #16.,R0
53 174614 005023 1S: CLR (R3)+ ; CLEAR IT...
54 174616 077002 SOB R0,1S
55 174620 011603 MOV (SP),P3 ;...AND RESET POINTER.
56 174622 005001 CLR R1
57 174624 005065 170002 CLK BYTES($TOP) ; CLEAR BYTE COUNTERS.

```

```

58 174630 112714 000200          MOVW  #200,(R4)      ; SFT "MIF"...
59 174634 112764 000224 000002    MOVW  #224,MCC(R4)   ;...AND ENABLE ALL THREE PORTS.
60 174642 116400 000032          MOVW  PADB(R4),R0    ; DUMMY READ (FLUSH)...
61 174646 116400 000034          MOVW  PBDB(R4),R0    ;...BOTH DB'S.
62 174652 106427 000000          MTPS  #PRO          ; LOWER CPU...
63                                ;...DATA SHOULD BEGIN TO FLOW.
64 174656 026527 170002 011022 2$: CMP   BYTES(STOP),#<18.*BITR>118. ; 18 BYTES TRANSFERRED ??
65 174664 001403                  BEQ   3$             ; BR IF SO.
66 174666 077105                  SOB   R1,2$         ; HANG-AROUND FOR A WHILE.
67 174670 052715 000100          BIS   #BIT6,($EF)   ;; E6 = LOOP TIME-OUT, DATA XFER INCOMPLETE
68
69 174674 012603                  3$:  MOV   (SP)+,R3      ; GET RCV'D...
70 174676 012702 163646          MOV   #XFLT10-K3K,R2 ;...AND XMT'D POINTERS...
71 174702 012701 000022          MOV   #18.,R1
72 174706 122223                  4$:  CMPW  (P2)+,(R3)+  ;...AND COMPARE XMTD/RCVD DATA.
73 174710 001402                  BEQ   5$
74 174712 052715 000200          BIS   #BIT7,($EF)   ;; E7 = RECEIVED DATA INCORRECT
75 174716 077105                  5$:  SOB   R1,4$
76
77 174720 105764 000100          6$:  TSTB  PAMS(R4)    ; CHECK PORT A DIRECTION.
78 174724 100404                  BMI   7$            ; BR IF OUTPUT.
79 174726 105014                  CLRW  (R4)          ; ELSE, CLEAR MASTER...
80 174730 105064 000002          CLRW  MCC(R4)       ;...CONTROL REGISTERS...
81 174734 000676                  BR    PIOD2         ;...AND GO 'ROUND ONCE MORE.
82
83 174736 112714 000001          7$:  MOVW  #1,(R4)     ; THEN, RESET THE CHIP...
84 174742 005064 000140          CLR   XCVR(R4)     ;...AND TRANSMITTER CONTROLS.
85 174746
86 174746 012637 000162          PIOXIT: MOV   (SP)+,PIOBV+2  ;; RESTORE PIOBV.
      174752 012637 000160          MOV   (SP)+,PIOBV
      174756 012637 000156          MOV   (SP)+,PIOAV+2  ;; RESTORE PIOAV.
      174762 012637 000154          MOV   (SP)+,PIOAV
      174766 012637 000106          MOV   (SP)+,PEVNT+2  ;; RESTORE PEVNT.
      174772 012637 000104          MOV   (SP)+,PEVNT
      174776 011500          MOV   ($EF),R0     ;; ERROR BITS => R0<11:00>...
      175000 001402          BEQ   30007$       ;;...AND SKIP IF NONE.
      175002 052700 100000          BIS   #<10*BIT12>,R0 ;; ELSE, ADD TEST NUM => R0<15:12>...
      175006 000207          30007$: RETURN    ;;...AND RETURN (NZ).

```

```

1
2 ;
3 ; PORT INTERRUPT HANDLER(S).
4 ;
5 175010 012700 000032 AI: .ENABL LSB
6 175014 105764 000100 MOV #PA0B,R0 ; PORT A -- GET DB INDEX.
7 175020 100407 TSTB PAMS(R4) ; CHECK DIRECTION.
8 175022 000421 BMI 1$ ; OUTPUT
9 BR 3$ ; INPUT
10 175024 012700 000034 BI: MOV #PB0B,R0 ; PORT B -- DITTO.
11 175030 105764 000120 TSTB PAMS(P4)
12 175034 100401 BMI 1$ ; OUTPUT
13 175036 000413 BR 3$ ; INPUT
14
15 175040 060400 1$: ADD R4,R0 ; OUTPUT -- POINT TO DATA BUFFER.
16 175042 105712 TSTB (R2) ; ANY BYTES LEFT ??
17 175044 001404 BEQ 2$ ; BR IF NOT.
18 175046 112210 MOVB (R2)+,(R0) ; ELSE, SEND NEXT BYTE...
19 175050 105265 170002 INCB BYTES($TOP) ;...BUMP THE COUNT...
20 175054 000410 BR 4$ ;...AND RETURN.
21 175056 112760 000240 177766 2$: MOVB #240,-12(R0) ; WHEN XMIT DONE, CLEAR "IP"...
22 175064 000404 BR 4$ ;...AND RETURN.
23
24 175066 060400 3$: ADD R4,R0 ; INPUT -- POINT TO DATA BUFFER.
25 175070 111023 MOVB (R0),(R3)+ ; STORE THE BYTE...
26 175072 105265 170003 INCB BYTES+1($TOP) ;...AND BUMP THE COUNT.
27 175076 112760 000140 177766 4$: MOVB #140,-12(R0) ; COMMON EXIT -- CLEAR "IUS"...
28 175104 000002 RTI ;...AND RETURN.
29 .DSABL LSB

```

140

```

1
    175106
    175106
    175106 013746 000164
    175112 013746 000166
    175116 005015
2
3
4
5
6
7
8
9
10
11
12
13
14      170002
15      170004
16      170006
17      170010
18      170012
19
20 175120 004737 163602
21 175124 001402
22 175126 052715 000001
23
24 175132 010102
25 175134 001002
26 175136 052715 000002
27
28 175142 012700 000006
29 175146 005001
30 175150 006302
31 175152 006101
32 175154 077003
33 175156 000301
34 175160 052701 100000
35 175164 010165 170002
36 175170 010265 170004
37
38
39
40
41 175174 012700 162102
42 175200 012701 000052
43 175204 014046
44 175206 021627 150002
45 175212 001002
46 175214 060516
47 175216 000426
48 175220 021627 160002
49 175224 001002

.SBTTL - T11 DMA CONTROLLER AMZ8016
;*****
;* TEST 11 -- DMA CONTROLLER AMZ8016
;*****
TST11:
TDMA:
    MOV    DMAV,-(SP)      ;; SAVE DMAV.
    MOV    DMAV+2,-(SP)
    CLR    ($EF)          ;; CLEAR ERROR FLAG.
;
; INPUT: R1 = Q-BUS ADDRESS BITS<21:6> OR ZERO.
; OUTPUT: R0 = ERROR FLAGS OR ZERO.
;
;
; T11 DMA CONTROLLER AMZ8016
; . E0 = ROM IN VECTOR SPACE -- INTERRUPTS NOT TESTED
; . E1 = Q-BUS ADDRESS UNDEFINED -- Q-BUS ACCESS NOT TESTED
; . E2 = CHAN INTERRUPT NOT RECEIVED
; . E3 = DMA CHANNEL HUNG (TCIEOP BOTH CLEAR)
; . E4 = DMA ABORTED (EOP = 1 = NXM)
; . E5 = DMA DATA ERROR
;
QAHI= TMP1      ; SAVERS FOR A TWO WORD Q-BUS ADDRESS...
QALO= TMP2
CLISP= TMP3     ;...THREE VARIABLE (CH1/CH2) COMMANDS...
SETIE= TMP4
STACHN= TMP5
;
; CALL XRAMLO-K3K ; VECTOR SPACE USABLE ??
; BEQ 1$ ; SKIP IF SO.
; BIS #BIT0,($EF) ;; E0 = ROM IN VECTOR SPACE -- INTERRUPTS NOT TESTED
;
1$: MOV R1,R2 ; Q-ADDR<21:6> DEFINED ??
; BNE 2$ ; SKIP IF SO.
; BIS #BIT1,($EF) ;; E1 = Q-BUS ADDRESS UNDEFINED -- Q-BUS ACCESS NOT TESTED
;
2$: MOV #6,R0
; CLR R1
;
3$: ASL R2 ; \
; ROL R1 ; > ADDR<21:16> => R1<6:0>
; SOB R0,3$ ; /
; SWAB R1 ; REPOSITION TO DMA FORMAT <13:8>...
; BIS #BIT15,R1 ;...SET "Q-BUS" BIT...
; MOV R1,QAHI($TOP) ;...AND SAVE Q-BUS HIGH (SEG/TAG)...
; MOV R2,QALO($TOP) ;...AND LOW (OFFSET) ADDRESS.
;
; NOW PUSH THE 6-LINK CHAIN SCRIPT ONTO THE STACK
; FILLING IN THE CORRECTED ADDRESSES AS WE GO.
;
TDMA1: MOV #CHAINX+2-K3K,R0 ; CHAIN (TOP) ADDRESS...
; MOV #<CHAINX+2-CHAIN1>/2,R1 ;...AND SIZE.
3$: MOV -(R0),-(SP) ; PUSH A WORD.
; CMP (SP),#BUF1 ; LOCAL BUF1 ??
; BNE 4$ ; NO.
; ADD $TOP,(SP) ; YES, ADJUST IT.
; BR 8$
;
4$: CMP (SP),#BUF2 ; LOCAL BUF2 ??
; BNE 5$ ; NO.

```

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50 175226 060516          ADD     $TOP,(SP)      ; YES, ADJUST IT.
51 175230 000421          BR      8$
52 175232 021627 120000   5$:    CMP     (SP),#120000 ; Q-BUS 20K ??
53 175236 001003          BNE    6$             ; NO.
54 175240 016516 170004   MOV     QALO($TOP),(SP) ; YES, SUBSTITUTE IT.
55 175244 000407          BR      7$
56 175246 021627 130000   6$:    CMP     (SP),#130000 ; Q-BUS 22K ??
57 175252 001010          BNE    8$             ; NO.
58 175254 016516 170004   MOV     QALO($TOP),(SP) ; YES, SUBSTITUTE IT...
59 175260 062716 010000   ADD     #4096,(SP)     ;...AND BUMP UP 2KW.
60 175264 014046          7$:    MOV     -(R0),-(SP)   ; ON EITHER Q-BUS ADDRESS, PUSH...
61 175266 016516 170002   MOV     QAH1($TOP),(SP) ;...AND SUBSTITUTE THE HIGH PART...
62 175272 005301          DEC     R1             ;...AND TWEAK THE COUNT ACCORDINGLY.
63 175274 077135          8$:    SOB     R1,3$     ; LOOP 'TIL DONE...
64                          ;...($P) IS THE CHIP'S CHAIN ADDRESS.
65                          ;
66                          ; NOW, EXECUTE AND ERROR CHECK 5 DMA CHAINS AS FOLLOWS:
67                          ; LOCAL => LOCAL, 2KW.
68                          ; LOCAL I/O PAGE => LOCAL, 1KW.
69                          ; LOCAL => Q-BUS 20K, 2KW.
70                          ; Q-BUS 20K => Q-BUS 22K, 2KW.
71                          ; Q-BUS 22K => LOCAL, 2KW.
72                          ;
73                          ; MMR= 70 ; MASTER MODE REGISTER.
74                          ; STAT1= 56 ; CHANNEL 1 STATUS.
75                          ; STAT2= 54 ; CHANNEL 2 STATUS...
76                          ; CMDR= 54 ;...AND COMMAND REGISTER (FOR BOTH).
77                          ; CHA1H= 46 ; CHAIN ADDRESS REGISTERS HIGH (SEG/TAG)...
78                          ; CHA2H= 44
79                          ; CHA1L= 42 ;...AND THE LOW (OFFSET) HALFS.
80                          ; CHA2L= 40
81                          ; TC= 1 ; TERMINAL COUNT STATUS BIT (BIT0).
82                          ; EOP= 2 ; END-OF-PROCESS (MXM) STATUS BIT (BIT2).
83                          ; IP= 20000 ; INTERRUPT POSTED (DONE) STATUS BIT (BIT13).
84                          ;
85 175276 106427 000200   TDMA2: MTPS    #PR4      ; RAISE TO CHIP LEVEL.
86 175302 012700 174400   MOV     #SDMA,R0      ; BASE ADDRESS.
87 175306 012701 000056   MOV     #46,R1
88 175312 005060 000054   CLR     CMDR(R0)      ; COMMAND "RESET"...
89 175316 005020          1$:    CLR     (R0)+      ;...AND CLEAR ALL REGISTERS.
90 175320 077102          SOB     R1,1$
91 175322 012701 150002   MOV     #BUF1,R1
92 175326 060501          ADD     $TOP,R1      ; GET BUF1 ADDRESS.
93 175330 012702 004000   MOV     #2048,R2
94 175334 010100          2$:    MOV     R1,R0
95 175336 005061 010000   CLR     4096.(R1)    ; CLEAR BUF2...
96 175342 010021          MOV     R0,(R1)+     ;...AND PUT ADDRESSES IN BUF1.
97 175344 077205          SOB     R2,2$
98                          ;
99 175346 012704 174400   TDMA3: MOV     #SDMA,R4      ; GET BASE POINTER.
100 175352 012737 161500 000164 MOV     #21$-K3K,DMAV ; INT SERVICE CHAN 1 (AND 2).
101 175360 012737 000200 000166 MOV     #PR4,DMAV+2
102 175366 012765 170006   MOV     #40114,CLISP($TOP) ; SET "CLEAR IUSIP"...
103 175374 012765 000062 170010 MOV     #42120,SETIE($TOP) ;...SET IE...
104 175402 012765 000240 170012 MOV     #240,STACHN($TOP) ;...AND "START CHAIN" COMMANDS FOR CH 1.
105 175410 012764 000115 000070 MOV     #115,MNR(R4)   ; SET MODE = VI, WAIT, CPINTLV, ENABLE.
106 175416 010664 000042   MOV     SP,CHAIL(R4)  ; SET CHAIN ADDRESS(ES)...
    
```



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107 175422 010664 000040      MOV    SP,CHA2L(R4)    ;... = 1ST LINK.
108 175426 012703 161742      1$:   MOV    #WCTBL-K3K,R3  ; SET WC TABLE POINTER IN R3.
109 175432 005000      2$:   CLR    R0              ; SET A KEEP-ALIVE TIMER.
110 175434 032715 000001      BIT    #BIT0,(SEF)    ; INTERRUPTS USEABLE ??
111 175440 001001      BNE   25$             ; SKIP NEXT IF NOT.
112 175442 106400      MTPS  R0              ; YES, LOWER CPU.
113 175444 016564 170010 000054 25$:   MOV    SFTIE(STOP),CMDB(R4) ; SET "CIE"...
114 175452 016564 170012 000054  MOV    STACHN(STOP),CMDB(R4) ;...AND START CHAIN CHAN 1(2).
115 175460 077001      SOB   R0, .           ; TC (OR EOP) INTERRUPT SHOULD...
116                                     ; ...HAPPEN BEFORE THIS TIMES OUT.
117 175462 052715 000004      BIS   #BIT2,(SEF)    ;; E2 = CHAN INTERRUPT NOT RECEIVED
118 175466 024646      CMP   -(SP),-(SP)    ; FAKE IT...
119 175470 026527 170012 000240  CMP   STACHN(STOP),#240 ;...AND SERVICE CHAN 1...
120 175476 001003      BNE   22$             ;...OR CHAN 2.
121                                     ;
122                                     ; PROCESS DMA CHANNEL INTERRUPTS.
123                                     ;
124 175500 016400 000056      21$:  MOV    STAT1(R4),R0   ; GET CHAN 1 STATUS.
125 175504 000402      BR   27$             ; OR
126 175506 016400 000054      22$:  MOV    STAT2(R4),R0   ; GET CHAN 2 STATUS.
127 175512 022626      27$:  CMP   (SP)+,(SP)+    ; ADJUST STACK.
128 175514 032700 000001      BIT   #TC,R0
129 175520 001010      BNE   24$             ; BR IF TC IS SET.
130 175522 032700 000002      BIT   #EOP,R0
131 175526 001003      BNE   23$             ; BR IF EOP (NXM) IS SET.
132 175530 052715 000010      BIS   #BIT3,(SEF)    ;; E3 = DMA CHANNEL HUNG (TCIEOP BOTH CLEAR)
133 175534 000402      BR   24$
134 175536      23$:
135 175536 052715 000020      BIS   #BIT4,(SEF)    ;; E4 = DMA ABORTED (EOP = 1 = NXM)
136 175542 016564 170006 000054 24$:  MOV    CLISP(STOP),CMDB(R4) ; INT SERVICE COMPLETE, CLEAR "IUSIIP".
137 175550 012300      3$:   MOV    (R3)+,R0       ; GET WORD COUNT FROM "WCTBL"...
138 175552 001423      BEQ   6$             ;...AND SKIP IF DATA CHECK INHIBITED.
139 175554 012701 150002      MOV   #BUF1,R1
140 175560 060501      ADD   STOP,R1        ; ASSUME SRC WAS BUF1...
141 175562 012702 160002      MOV   #BUF2,R2
142 175566 060502      ADD   STOP,R2        ;...AND DEST BUF2.
143 175570 020027 004000      CMP   R0,#2048.     ; WC = 2KW ??
144 175574 001404      BEQ   4$             ; SKIP IF SO...
145 175576 012701 164000      MOV   #164000,R1    ;...ELSE, SRC WAS ODTROM...
146 175602 162702 010000      SUB   #4096.,R2     ;...AND DST BUF1.
147 175606 022122      4$:   CMP   (R1)+,(R2)+   ; COMPARE SRC/DST DATA.
148 175610 001403      BEQ   5$             ; BR IF OK.
149 175612 052715 000040      BIS   #BIT5,(SEF)    ;; E5 = DMA DATA ERROR
150 175616 000401      BR   6$             ; ESCAPE ON 1ST DATA ERROR.
151 175620 077006      5$:   SOB   R0,4$
152
153 175622 005713      6$:   TST   (R3)          ; NEXT LINK INVOLVE Q-BUS ??
154 175624 001003      BNE   7$             ; BR IF NOT.
155 175626 032715 000002      BIT   #BIT1,(SEF)    ; YES, Q-BUS ACCESS PERMITTED ??
156 175632 001003      BNE   8$             ; NO, QUIT WHILE YOU'RE AHEAD.
157 175634 021327 177777      7$:   CMP   (R3),#-1      ; CHECK FOR END OF TABLE...
158 175640 001274      BNE   2$             ;...AND LOOP 'TIL ALL LINKS DONE.
159
160 175642 032765 000001 170012 8$:   BIT   #1,STACHN(STOP) ; NOW, CHECK THE CHANNEL SELECT BIT...
161 175650 001012      BNE   9$             ;...AND EXIT IF BOTH DONE.
162 175652 062737 000006 000164  ADD   #22$-21$,DMAV   ; ELSE, CHANGE VECTOR...

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163 175660 005265 170006          INC      CLISP($TOP)
164 175664 005265 170010          INC      SETIE($TOP)          ;...AND COMMANDS FOR CHAN 2...
165 175670 005265 170012          INC      STACHN($TOP)
166 175674 000654                   BR       1$                  ;...AND GO *ROUND ONCE MORE.
167
168 175676 005064 000054          9$: CLR      CMDR(R4)          ; ALL DONE RESET CHIP.
169 175702 062706 000124          ADD     #CHAINX+2-CHAIN1,SP ; POP CHAIN OFF THE STACK.
170 175706 032715 000001          BIT     #BIT0,(SEF)          ; DID WE RUN WITH INTERRUPTS ??
171 175712 001402                   BEQ     10$                  ; SKIP IF SO.
172 175714 042715 000004          BIC     #BIT2,(SEF)          ; NO, DISCARD INTERRUPT ERROR BIT.
173 175720
173 175720 012637 000166          10$:DMAXIT:
173 175720 012637 000164          MOV     (SP)+,DMAV+2        ;; RESTORE DMAV.
173 175724 012637 000164          MOV     (SP)+,DMAV
173 175730 011500                   MOV     (SEF),RO            ;; ERROR BITS => RO<11:00>...
173 175732 001402                   BEQ     30008$              ;;...AND SKIP IF NONE.
173 175734 052700 110000          BIS     #<11*BIT12>,RO     ;; ELSE, ADD TEST WUM => RO<15:12>...
173 175740 000207                   30008$: RTURN              ;;...AND RETURN (WZ).
174
175
176
177
178 175742 004000                   ; WORD COUNT TABLE FOR POST-DMA DATA CHECKS.
179 175744 002000                   ; FINAL CPECK (5.) VERIFIES THE RESULTS OF CHAINS 2, 3, 4, AND 5.
180 175746 000000                   ;
181 175750 000000                   ;
182 175752 004000                   WCTBL: 2048.                ; 1. 2KW, BUFR1 => BUFR2.
183 175754 177777                   1024.                        ; 2. 1KW, ODTROM => BUFR1.
184
185
186
187
188
189
190 175756 001606                   0                               ; 3. Q-BUS INVOLVED, NO DATA CHECK.
191 175760 000000 150002           0                               ; 4. Q-BUS INVOLVED, NO DATA CHECK.
192 175764 000000 160002           0                               ; 5. 2KW, BUFR1 => Q1 => Q2 => BUFR2.
193 175770 004000                   -1                             ; TABLE TERMINATOR.
194 175772 000164
195 175774 000030 001340
196
197 176000 001602
198 176002 000000 164000
199 176006 000000 150002
200 176012 002000
201 176014 000030 001340
202
203
204
205
206
207 176020 001602
208 176022 000000 150002
209 176026 100000 120000
210 176032 004000
211 176034 000030 001340
212
213 176040 001602

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; AND THIS IS THE 6 LINK DMA CHAIN.
;
; THIS GETS PUSHED ONTO THE STACK WHERE LOCAL AND Q-BUS ADDRESSES
; ARE ADJUSTED ACCORDING TO RAM CONFIG AND ENTRY OPTION (R2).
;
CHAIN1: 1606          ; LOAD ARA, ARB, OPK, VECT, AND CHAN MODE.
0, BUFR1            ; FROM LOCAL BUFR1...
0, BUFR2            ; ...TO LOCAL BUFR2...
2048.                ; ...2K WORDS.
DMAV                ; VECTOR.
30, 1340            ; SFTREQ, HDMSK, INT TCIEOP, INTLV, WORD-WORD.

CHAIN2: 1602          ; RE-LOAD ARA, ARB, OPK, AND CHAN MODE ONLY.
0, 164000           ; FROM LOCAL ODTROM...
0, BUFR1            ; ...TO LOCAL BUFR1...
1024.                ; ...1K WORDS...
30, 1340            ; ...SAME MODE AND TERMINATION.

;Previously, CHAIN3 read the arbiter's boot ROM using the QBUS. However, the
;Boot ROM of a KDF11-B does not respond on the QBUS. Therefore, CHAIN3 was
;removed.

CHAIN4: 1602          ; DITTO.
0, BUFR1            ; FROM LOCAL BUFR1...
100000, 120000      ; ...TO Q-BUS 20K...
2048.                ; ...2K WORDS.
30, 1340            ; DITTO.

CHAINS: 1602          ; DITTO.

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214	176042	100000	120000	100000, 120000	; FROM Q-BUS 20K...
215	176046	100000	130000	100000, 130000	;...TO Q-BUS 22K...
216	176052	004000		2048.	;...2K WORDS.
217	176054	000030	001340	30, 1340	; DITTO.
218					
219	176060	001602		CHAIN6: 1602	; DITTO.
220	176062	100000	130000	100000, 130000	; FROM Q-BUS 22K...
221	176066	000000	160002	0, BUFR2	;...TO LOCAL BUFR2...
222	176072	004000		2048.	;...2K WORDS.
223	176074	000030	001340	30, 1340	; DITTO.
224	176100	000000		CHAINX: 0	; TERMINATOR.

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```

1          .SBTTL - T12 Q-BUS INTERRUPT
          ;;*****
          ;;* TEST 12 -- Q-BUS INTERRUPT
          ;;*****
          TST12:
          TQIR:
          MOV     BIACKV,-(SP)    ;; SAVE BIACKV.
          MOV     BIACKV+2,-(SP)
          MOV     PWRV,-(SP)    ;; SAVE PWRV.
          MOV     PWRV+2,-(SP)
          CLR     ($EF)        ;; CLEAR ERROR FLAG.

2          ;
3          ; INPUT: R1 = 1ST OF 2 CONSECUTIVE Q-BUS VECTORS.
4          ; OUTPUT: R0 = ERROR FLAGS OR ZERO.
5          ;
6          ; *** REQUIRES A RUNNING ARBITER CPU ***
7          ;
8          ; VERIFY THAT THE QIR CAN INTERRUPT THE ARBITER, AND THAT
9          ; THE POST-INTERRUPT PROCESS WORKS AS ADVERTISED.
10         ;
11         ; T12 Q-BUS INTERRUPT
12         ; E0 = Q-BUS VECTOR UNDEFINED -- CAN'T RUN
13         ; E1 = BREQ (CSR<14>) NEVER GOT SET
14         ; E2 = ROM IN VECTOR SPACE -- RESPONSE INTERRUPTS NOT TESTED
15         ; E3 = INT-ON-BIACK NOT MASKED AT PR5
16         ; E4 = INT-ON-BIACK NOT RECEIVED
17         ; E5 = BIACK DIDN'T CLEAR BREQ (CSR<14>)
18         ; E6 = BRESET TRAP THRU 24 DIDN'T HAPPEN
19
20 176124 005701          TST     R1          ; Q VECTOR DEFINED ??
21 176126 001003          BNE     1$          ; PROCEED IF SO.
22 176130 052715 000001  BIS     #BIT0,($EF)    ;; E0 = Q-BUS VECTOR UNDEFINED -- CAN'T RUN
23 176134 000516          BR      QIXIT
24
25 176136 106427 000240  1$: MTPS   #PR5          ; RAISE CPU.
26 176142 042737 177677 177530 BIC     #~CBIT6,$CSR    ; ENSURE EVERYTHING OFF (EXCEPT DPR).
27 176150 010137 177532          MOV     R1,$QIR        ; WRITE A VECTOR IN QIR<9:2>.
28 176154 032737 040000 177530 BIT     #BIT14,$CSR    ; REQUEST SHOULD BE SET.
29 176162 001002          BNE     2$          ; SKIP IF SO.
30 176164 052715 000002  BIS     #BIT1,($EF)    ;; E1 = BREQ (CSR<14>) NEVER GOT SET
31
32 176170 004737 163602  2$: CALL   XRAMLO-K3K    ; VECTOR SPACE USABLE ??
33 176174 001403          BEQ     3$          ; PROCEED IF SO.
34 176176 052715 000004  BIS     #BIT2,($EF)    ;; E2 = ROM IN VECTOR SPACE -- RESPONSE INTERRUPTS NOT TESTE
35 176202 000473          BR      QIXIT
36
37 176204 012737 162232 000130 3$: MOV     #4$-K3K,BIACKV ; SET RESPONSE VECTOR.
38 176212 012737 000240 000132 MOV     #PR5,BIACKV+2
39 176220 052737 030000 177530 BIS     #BIT13|BIT12,$CSR ; SET ENABLES.
40 176226 077001          SOB     R0,.          ; RESPONSE SHOULD BE MASKED AT THIS LEVEL.
41 176230 000403          BR      5$
42 176232
43 176232 052715 000010  4$: BIS     #BIT3,($EF)    ;; E3 = INT-ON-BIACK NOT MASKED AT PR5
44 176236 000411          BR      6$
45 176240 062737 000030 000130 5$: ADD     #6$-4$,BIACKV  ; CHANGE RESPONSE VECTOR.
46 176246 106427 000000          MTPS   #PRO          ; LOWER CPU...
47 176252 077001          SOB     R0,.          ;...INT SHOULD COME IN.
  
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47 176254 052715 000020      BIS    #BIT4,(SEF)    ;; E4 = INT-ON-BIACK NOT RECEIVED
48 176260 000401              BR     65$
49 176262 022626              6$:   CMP    (SP)+,(SP)+    ; OK, FIX STACK.
50 176264 032737 040000 177530 65$:   BIT    #BIT14,SCSR    ; REQUEST SHOULD BE CLEAR.
51 176272 001405              BEQ    7$
52 176274 052715 000040      BIS    #BIT5,(SEF)    ;; E5 = BIACK DIDN'T CLEAR BREQ (CSR<14>)
53 176300 077001              SOB    R0,,
      RESET
      SOB    R0,,    ;; LOCAL RESET.
54
55      ;
56      ; NOW ONCE MORE USING THE ALTERNATE VECTOR (IN ARBITER)
57      ; TO CAUSE A "BUS-INIT" AND LOCAL TRAP THRU VECTOR 24.
58 176306 022121              7$:   CMP    (R1)+,(R1)+    ; BUMP UP (+4) TO SECOND VECTOR.
59 176310 012737 162370 000024  MOV    #8$-K3K,PWRV    ; SET PWR-UP VECTOR.
60 176316 012737 000340 000026  MOV    #PR7,PWRV+2
61 176324 106427 000340      MTPS   #PR7          ; SHOULD BE NON-MASKABLE.
62 176330 042737 020000 177530  BIC    #BIT13,SCSR    ; CLEAR IACK ENABLE.
63 176336 052737 002000 177530  BIS    #BIT10,SCSR    ; ARM BRESET TRAP.
64 176344 010137 177532      MOV    R1,SQIR       ; POST Q-BUS REQUEST.
65 176350 005000      CLR    R0           ; ARBITER EXECUTES A BUS-RESET...
66 176352 077001              SOB    R0,,         ; ...AND A TRAP THRU 24 SHOULD OCCUR.
67 176354 052715 000100      BIS    #BIT6,(SEF)    ;; F6 = BRESET TRAP THRU 24 DIDN'T HAPPEN
68 176360 077001              SOB    R0,,
      RESET
      SOB    R0,,    ;; LOCAL RESET.
69 176366 000401      BR     QIXIT
70 176370 022626              8$:   CMP    (SP)+,(SP)+    ; PWR-UP TRAPPED TO HERE, FIX STACK.
71 176372 042737 177677 177530  QIXIT: BIC    #^CBIT6,SCSR    ; CLEAR CSR.
72 176400 012637 000026      MOV    (SP)+,PWRV+2    ;; RESTORE PWRV.
      MOV    (SP)+,PWRV
      MOV    (SP)+,BIACKV+2    ;; RESTORE BIACKV.
      MOV    (SP)+,BIACKV
      MOV    (SEF),R0        ;; ERROR BITS => R0<11:00>...
      BEQ    30009$         ;; ...AND SKIP IF NONE.
      BIS    #<12*BIT12>,R0    ;; ELSE, ADD TEST NUM => R0<15:12>...
      30009$: RETURN      ;; ...AND RETURN (NZ).

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176432
176432 013746 000120
176436 013746 000122
176442 013746 000124
176446 013746 000126
176452 013746 000134
176456 013746 000136
176462 005015

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23 176464 005037 177530
24 176470 012702 175000
25 176474 012701 125252
26 176500 012700 000020
27 176504 010112
28 176506 022201
29 176510 001402
30 176512 052715 000001
31 176516 077006
32
33
34
35
36
37 170004
38 170006
39 000000
40 000010
41 000062
42
43 176520 013700 177524
44 176524 042700 177617
45 176530 006300

.SBTTL - T13 DUAL-PORT RAM AND IPV
;*****
; * TEST 13 -- DUAL-PORT RAM AND IPV
;*****
TST13:
T0PR:
MOV DPRV4,-(SP) ;; SAVE DPRV4.
MOV DPRV4+2,-(SP)
MOV DPRV8,-(SP) ;; SAVE DPRV8.
MOV DPRV8+2,-(SP)
MOV DPRV12,-(SP) ;; SAVE DPRV12.
MOV DPRV12+2,-(SP)
CLR (SEF) ;; CLEAR ERROR FLAG.

;
; INPUT: NONE.
; OUTPUT: R0 = ERROR FLAGS OR ZERO.
;
; FIRST, DISABLE THE DPR AND VERIFY WRITE/READ
; FROM THE LOCAL (II) SIDE.
;
; T13 DUAL-PORT RAM AND IPV
; . E0 = LOCAL DPR WRITE-READ ERROR
; . E1 = BUS-ERROR ON Q-BUS DPR READ
; . E2 = NON-ZERO DATA RETURNED ON Q-BUS READ
; . E3 = ROM IN VECTOR SPACE -- Q-WRITE AND INTERRUPT NOT TESTED
; . E4 = BUS ERROR ON WRITE TO DPR WORD 0
; . E5 = COMMAND INTERRUPT DIDN'T HAPPEN (OR DOESN'T WORK)
; . E6 = Q-BUS WRITE AND/OR INTERRUPT WITH DPR DISABLED
; . E7 = Q-BUS WRITE DIDN'T TIME-OUT
; . E8 = Q-BUS WRITE TIMED-OUT
; . E9 = DPR INTERRUPT 4 NOT RECEIVED
; . E10 = DPR INTERRUPT 8 NOT RECEIVED
; . E11 = DPR INTERRUPT 12 NOT RECEIVED
;
CLR $CSR ; ENSURE EVERYTHING OFF.
MOV #SDPR,R2 ; DPR BASE ADDRESS (LOCAL).
MOV #125252,R1 ; USE ALTERNATING 1'S AND 0'S.
MOV #16,,R0
1$: MOV R1,(R2) ; WRITE...
CMP (R2)+,R1 ;...AND CHECK A WORD.
BEQ 2$ ; SKIP IF RIGHT.
BIS #BIT0,(SEF) ;; E0 = LOCAL DPR WRITE-READ ERROR
2$: SOB R0,1$ ; LOOP 'TIL DONE.
;
; NOW THE DPR IS FULL OF ALTERNATING 1'S AND 0'S.
; READ ALL WORDS FROM THE Q-BUS SIDE USING THE DMA ENGINE.
; EXPECT ALL ADDRESSES TO RESPOND (NO EOP), BUT DATA = 0'S.
;
QADR= TMP2 ; SAVE Q-BUS...
LADR= TMP3 ;...AND LOCAL ADDRESSES.
RD= 0 ; DMA DRIVER READ...
WRT= WQIO-RQIO ;...WRITE...
CNTNU= CQIO-RQIO ;...AND CONTINUE (AFTER EOP) ENTRIES.
;
T0PR2: MOV SUID,R0 ; GET CPU ID NUM (CSRC<7:4>).
BIC #~C160,R0 ; STRIP <6:4> = NUM*16...
ASL R0 ;...TIMES 2 = NUM*32...

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46 176532 062700 160000          ADD    #SQDPR1,RO    ;...PLUS LO BASE = GLOBAL ADDRESS.
47 176536 032737 000200 177524    BIT    #BIT7,SUID   ; ID >= 8. ??
48 176544 001402                BEQ    1$          ; SKIP IF NOT.
49 176546 062700 015400          ADD    #<SQDPR2-$QDPR1>,RO ; YES, ADJUST TO HIGH RANGE.
50 176552 010065 170004          1$:    MOV    RO,QADR(STOP) ; SAVE IT IN RAM.
51 176556 010500                MOV    STOP,RO
52 176560 062700 150002          ADD    #BUFPR1,RO   ; CALCULATE BUFFER ADDRESS...
53 176564 010065 170006          MOV    RO,LADR(STOP) ;...AND SAVE IT AS WELL.
54 176570 012700 163602          MOV    #QIOC+2-K3K,RO ; GET DRIVER ADDRESS...
55 176574 012701 000101          MOV    #<QIOC+2-RQIO>/2,R1 ;...AND SIZE...
56 176600 014046                2$:    MOV    -(RO),-(SP)   ;...AND PUSH IT ONTO THE STACK.
57 176602 077102                SOB    R1,2$
58 176604 000403                BR     35$         ; SKIP NEXT.
59 176606 052765 002000 170004    3$:    BIS    #2000,QADR(STOP) ; ALTERNATE BASE ADDRESS.
60 176614 016500 170004    35$:   MOV    QADR(STOP),RO ; SET Q-BUS ADDRESS...
61 176620 016501 170006          MOV    LADR(STOP),R1 ;...LOCAL ADDRESS...
62 176624 012702 000020          MOV    #16,,R2      ;...AND WORD COUNT.
63 176630 004766 000000          CALL   RD(SP)       ; READ FROM Q-BUS SIDE VIA DMA.
64 176634 102007                BVC    4$          ; BR IF OK (NOT "EOP").
65 176636 032765 002000 170004    BIT    #2000,QADR(STOP) ; NOT THERE, BOTH BASES TRIED ??
66 176644 001760                BEQ    3$          ; NO, GO "ROUND ONCE.
67 176646 052715 000002          BIS    #BIT1,(SEF)  ;; E1 = BUS-ERROR ON Q-BUS DPR READ
68 176652 000411                BR     TIPV1
69 176654 016500 170006          4$:    MOV    LADR(STOP),RO ; GET BUFFER ADDRESS.
70 176660 012701 000020          MOV    #16,,R1
71 176664 005720                5$:    TST    (RO)+       ; OBSERVED DATA SHOULD BE ZERO.
72 176666 001402                BEQ    6$          ; BR IF SO.
73 176670 052715 000004          BIS    #BIT2,(SEF)  ;; E2 = NON-ZERO DATA RETURNED ON Q-BUS READ
74 176674 077105                6$:    SOB    R1,5$
75                                ;
76                                ; SO FAR, SO GOOD -- NOW WRITE ALL FROM THE Q-BUS SIDE.
77                                ; 1ST WRITE SHOULD FORCE A NON-MASKABLE RESTART TRAP (COMMAND).
78                                ; ALL OTHERS SHOULD APPEAR NON-EXISTANT (EOP)..
79                                ;
80 176676 004737 163602          TIPV1: CALL   XRAMLO-K3K ; VECTOR SPACE USABLE ??
81 176702 001403                BEQ    1$          ; PROCEED IF SO.
82 176704 052715 000010          BIS    #BIT3,(SEF)  ;; E3 = ROM IN VECTOR SPACE -- Q-WRITE AND INTERRUPT NOT TES
83 176710 000563                BR     TIPXIT
84
85 176712 012700 175000          1$:    MOV    #SDPR,RO
86 176716 016501 170006          MOV    LADR(STOP),R1
87 176722 012702 000020          MOV    #16,,R2
88 176726 005020                11$:   CLR    (RO)+       ; CLEAR DPR...
89 176730 005021                CLR    (R1)+       ;...AND BUFFER.
90 176732 077203                SOB    R2,11$
91
92 176734 012701 000120          MOV    #DPRV4,R1
93 176740 012721 163350          MOV    #IPV4-K3K,(R1)+ ; SET DPRV4...
94 176744 012721 000240          MOV    #PR5,(R1)+
95 176750 012721 163356          MOV    #IPV8-K3K,(R1)+ ;...DPRV8...
96 176754 012721 000240          MOV    #PR5,(R1)+
97 176760 022121                CMP    (R1)+,(R1)+
98 176762 012721 163364          MOV    #IPV12-K3K,(R1)+ ;...AND DPRV12 VECTORS.
99 176766 012721 000240          MOV    #PR5,(R1)+
100 176772 106427 000340         MTPS   #PR7        ; RAISE CPU, COMMAND INTERRUPT...
101                                ;...SHOULD BE NON-MASKABLE.
102 176776 016500 170004          MOV    QADR(STOP),RO ; GET GLOBAL ADDRESS...
    
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103 177002 016501 170006      MOV     LADR($TOP),R1    ;...LOCAL ADDRESS...
104 177006 012702 000001      MOV     #1,R2           ;...AND WORD COUNT.
105 177012 012711 000040      MOV     #40,(R1)        ; SFT 1ST WORD = "NOP" COMMAND.
106 177016 004766 000010      CALL    WRT(SP)         ; WRITE DPR WORD 0...
107 177022 102002                BVC     2$              ;...SHOULD NOT HAVE ABORTED.
108 177024 052715 000020      BIS     #BIT4,(SEF)     ;; E4 = BUS ERROR ON WRITE TO DPR WORD 0
109 177030 005737 175000      2$:    TST     $DPR      ; COMMAND SHOULD HAVE BEEN CLEARED.
110 177034 001402                BEQ     3$
111 177036 052715 000040      BIS     #BIT5,(SEF)     ;; E5 = COMMAND INTERRUPT DIDN'T HAPPEN (OR DOESN'T WORK)
112 177042                3$:
113 177042 005004                4$:    CLR     R4           ; CLEAR INT RECEIVED FLAG...
114 177044 106427 000000      MTPS   #PRO            ;...AND LOWER CPU.
115 177050 012703 000017      MOV     #15,,R3        ; SET LOOP FOR 15 MORE WRITES.
116 177054 012702 000001      5$:    MOV     #1,R2        ; SET WORD COUNT.
117 177060 004766 000010      CALL    WRT(SP)        ; WRITE NEXT FROM Q-BUS SIDE...
118 177064 102002                BVC     6$              ;... SHOULD GET "EOP"...
119 177066 005704                TST     R4              ;... AND ...
120 177070 001402                BEQ     7$              ;...NO INTERRUPT.
121 177072                6$:
122 177072 052715 000100      BIS     #BIT6,(SEF)     ;; E6 = Q-BUS WRITE AND/OR INTERRUPT WITH DPR DISABLED
123 177076 077312                7$:    SOB     R3,5$
124                ;
125                ; NOW, ENABLE THE DPR, AND WRITE WORDS 1-15 AGAIN.
126                ; EXPECT LEVEL 5 INTERRUPTS AT WORDS 4, 8, AND 12,
127                ; AND EOP AT WORDS 1, 5, AND 9.
128 177100 052737 000170 177530 TIPV2: BIS     #170,$CSR      ; SET ALL ENABLES.
129 177106 016500 170004      MOV     QADR($TOP),R0   ; SET Q ADDRESS...
130 177112 062700 000002      ADD     #2,R0           ;...FOR DPR1...
131 177116 016501 170006      MOV     LADR($TOP),R1   ;...AND LOCAL ADDRESS.
132 177122 062701 000002      ADD     #2,R1           ;...DITTO.
133 177126 012703 000002      MOV     #BIT1,R3        ; BIT = CURRENT WORD UNDER TEST.
134 177132 005004                1$:    CLR     R4           ; CLEAR "INT RECVD" FLAG.
135 177134 012702 000001      MOV     #1,R2           ; SET WC...
136 177140 004766 000010      CALL    WRT(SP)        ;...AND WRITE 1ST WORD.
137 177144 102406                BVS     3$              ; BR IF IT TIMED-OUT.
138
139 177146 030327 001042      2$:    BIT     R3,#BIT1|BIT5|BIT9 ; DIDN'T TIME-OUT, SHOULD IT HAVE ??
140 177152 001410                BEQ     4$              ; NO, PROCEED.
141 177154 052715 000200      BIS     #BIT7,(SEF)     ;; E7 = Q-BUS WRITE DIDN'T TIME-OUT
142 177160 000405                BR     4$
143 177162 030327 001042      3$:    BIT     R3,#BIT1|BIT5|BIT9 ; DID TIME-OUT, SHOULD IT HAVE ??
144 177166 001002                BNE     4$              ; YES, PROCEED.
145 177170 052715 000400      BIS     #BIT8,(SEF)     ;; E8 = Q-BUS WRITE TIMED-OUT
146
147 177174 030327 000020      4$:    BIT     R3,#BIT4      ; INTERRUPT 4 EXPECTED ??
148 177200 001405                BEQ     5$              ; NO
149 177202 020427 000004      CMP     R4,#4.          ; YES, RECEIVED ??
150 177206 001402                BEQ     5$              ; YES.
151 177210 052715 001000      BIS     #BIT9,(SEF)     ;; E9 = DPR INTERRUPT 4 NOT RECEIVED
152 177214 030327 000400      5$:    BIT     R3,#BIT8      ; INTERRUPT 8 EXPECTED ??
153 177220 001405                BEQ     6$              ; NO.
154 177222 020427 000010      CMP     R4,#8.          ; YFS, RECEIVED ??
155 177226 001402                BEQ     6$              ; YES.
156 177230 052715 002000      BIS     #BIT10,(SEF)    ;; E10 = DPR INTERRUPT 8 NOT RECEIVED
157 177234 030327 010000      6$:    BIT     R3,#BIT12     ; INTERRUPT 12 EXPECTED ??
158 177240 001405                BEQ     7$              ; NO

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159 177242 020427 000014          CMP    R4,#12.          ; YES, RECEIVED ??
160 177246 001402                BEQ    7$              ; YES.
161 177250 052715 004000          BIS    #BIT11,(SEF)    ;; E11 = DPR INTERRUPT 12 NOT RECEIVED
162 177254 006303                ASL    R3              ; SHIFT UP TO NEXT WORD (BIT)...
163 177256 001325                BNE    1$              ;...AND LOOP 'TIL ALL DONE.
164
165 177260 062706 000202          TIPXIT: ADD    #<QIOC+2-RQIO>,SP ; DONE, POP DRIVER OFF THE STACK.
166 177264 042737 177677 177530  BIC    #^C8IT6,$CSR    ; CLEAR ALL EXCEPT "DPREN".
167 177272 012700 175000          MOV    #SDPR,R0       ; GET LOCAL ADDRESS...
168 177276 012701 000020          MOV    #16.,R1
169 177302 005020                1$: CLR    (R0)+        ;...AND FLUSH ANY CRAP.
170 177304 077102                SOB    R1,1$
171 177306 012637 000136          MOV    (SP)+,DPRV12+2 ;; RESTORE DPRV12.
171 177312 012637 000134          MOV    (SP)+,DPRV12
171 177316 012637 000126          MOV    (SP)+,DPRV8+2  ;; RESTORE DPRV8.
171 177322 012637 000124          MOV    (SP)+,DPRV8
171 177326 012637 000122          MOV    (SP)+,DPRV4+2  ;; RESTORE DPRV4.
171 177332 012637 000120          MOV    (SP)+,DPRV4
171 177336 011500                MOV    (SEF),R0       ;; ERROR BITS => R0<11:00>...
171 177340 001402                BEQ    30010$         ;;...AND SKIP IF NONE.
171 177342 052700 130000          BIS    #<13*BIT12>,R0 ;; ELSE, ADD TEST NUM => R0<15:12>...
171 177346 000207                30010$: RETURN        ;;...AND RETURN (NZ).
172
173 177350 012704 000004          IPV4: MOV    #4.,R4    ; DPRV4 INTERRUPT RECEIVED.
174 177354 000405                BR     IPVXIT
175 177356 012704 000010          IPV8: MOV    #8.,R4    ; DITTO DPRV8.
176 177362 000402                BR     IPVXIT
177 177364 012704 000014          IPV12: MOV   #12.,R4   ; DITTO DPRV12.
178 177370 042737 000007 177530  IPVXIT: BIC   #7,$CSR   ; *** TEMP, ENSURE REQ'S ARE CLEAR. ***
179 177376 000002                RTI

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1                                     ;*****
2                                     ; SUBROUTINE TO ACCESS THE Q-BUS I/O PAGE USING THE DMA ENGINE.
3                                     ; THIS CODE IS PUSHED ONTO AND EXECUTED IN STACK SPACE.
4                                     ;
5                                     ;.DSABL AMA      ; RELATIVE PIC.
6                                     ;
7                                     ; ON CALL, R0 = QIO ADDRESS, R1 = LOCAL ADDRESS, R2 = WORD COUNT.
8                                     ; ON RETURN, THEY CONTAIN UPDATED (TERMINAL) VALUES.
9                                     ; IF EOP TERMINATION, "V" BIT IS SET.
10                                    ;
11          174400                    DM=    SDMA      ; DMA CHIP BASE.
12                                    ;
13 177400 042767 000020 000170  RQIO:  BIC    #BIT4,CM+2    ; READ -- CLEAR "FLIP" BIT.
14 177406 000403                    BR      #QIOA
15 177410 052767 000020 000160  WQIO:  BIS    #BIT4,CM+2    ; WRITE -- SET "FLIP" BIT.
16 177416 010067 000142                    #QIOA:  MOV    R0,QA+2      ; SET Q-BUS I/O ADDRESS.
17 177422 010167 000142                    MOV    R1,LA+2      ; SET LOCAL ADDRESS.
18 177426 010267 000140                    MOV    R2,WC       ; SET WORD COUNT.
19 177432 012737 000115 174470  MOV    #115,@#DM+MMR ; MODE = VI, WAIT, CPINTLV, ENABLE.
20 177440 012737 000074 174454  MOV    #40134,@#DM+CMDR ; CLEAR INTERRUPT ENABLES.
21 177446 005037 174446                    CLR    @#DM+CHAIH
22 177452 012700 000100                    MOV    #QIO--6,R0   ; GET (PIC) CHAIN START ADDRESS.
23 177456 060700                    ADD    PC,R0
24 177460 000403                    BR      CQIOA
25 177462 012700 000110  CQIO:  MOV    #QIOC--6,R0   ; GET (PIC) CHAIN CONTINUE (DUMMY).
26 177466 060700                    ADD    PC,R0
27 177470 010037 174442  CQIOA:  MOV    R0,@#DM+CHAIL ; SET CHAIN ADDRESS.
28 177474 012737 000240 174454  MOV    #240,@#DM+CMDR ; CHAIN-LOAD (OR RELOAD 0) REGISTERS.
29 177502 012737 000102 174454  MOV    #102,@#DM+CMDR ; SET SOFT-REQ (START/CONTINUE DMA)...
30 177510 000240                    NOP
31 177512 032737 020000 174456 1$:   BIT    #IP,@#DM+STAT1 ; ...AND WAIT FOR DONE/ABORT (IP=1).
32 177520 001774                    BEQ    1$
33 177522 012737 000054 174454  MOV    #40114,@#DM+CMDR ; OK, CLEAR IUS AND IP.
34 177530 013700 174412  MOV    @#DM+12,R0   ; GET FINAL Q ADDR (ARAL)...
35 177534 013701 174402  MOV    @#DM+2,R1    ; ...LOCAL ADDR (ARBL)...
36 177540 013702 174462  MOV    @#DM+62,R2   ; ...AND WORD COUNT (OPK).
37 177544 032737 000002 174456  BIT    #EOP,@#DM+STAT1 ; "EOP" TERMINATION ??
38 177552 001401                    BEQ    2$
39 177554 000262                    SEV
40 177556 000207                    2$:   RETURN
41
42 177560 001602                    QIO:   1602          ; LOAD CARA, CARB, COPK, AND CR MODE.
43 177562 177400 000000  QA:     177400, 0      ; Q-BUS I/O ADDRESS (CARA)
44 177566 000000 000000  LA:     0, 0        ; LOCAL ADDRESS (CARB)
45 177572 000000                    WC:     0           ; WORD COUNT (COPK)
46 177574 000010 001340  CM:     10, 1340    ; CHAN MODE (1360 IF "FLIP" = 1).
47 177600 000000                    QIOC:  0           ; DUMMY RELOAD TO CLEAR "NAC" AND CONTINUE.
48          .ENABL AMA
49                                     ;*****

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```

1
2
3
4
5
6
7 177602 005000
8 177604 005002
9 177606 011046
10 177610 005116
11 177612 005110
12 177614 126066 000001 000001
13 177622 001402
14 177624 052702 000002
15 177630 121026
16 177632 001402
17 177634 052702 000001
18 177640 005110
19 177642 005702
20 177644 000207
21
22
23
24 177646 015 012
25 177650 001 002 004
26 177660 376 375 373
27 177670 000000
28
29

```

```

;
; HI SEGMENT COPY OF ROM/RAM IN VECTOR SPACE ROUTINE.
;
; RETURN R2<00> = 1 IF LO BYTE NON-WRITABLE.
; R2<01> = 1 IF HI BYTE NON-WRITABLE.
;
XRAMLO: CLR R0
        CLR R2
        MOV (R0),-(SP) ; GET TARGET LOCATION...
        COM (SP) ; ...AND COMPLIMENT IT.
        COM (R0) ; COMPLIMENT TARGET LOCATION.
        CMPB 1(R0),1(SP) ; HI BYTE WRITABLE ??
        BEQ 1$ ; YES
        ; NO
        BIS #BIT1,R2 ;
        1$: CMPB (R0),(SP)+ ; LO BYTE WRITABLE ??
        BEQ 2$ ; YES
        ; NO
        BIS #BIT0,R2 ;
        2$: COM (R0) ; RESTORE TARGET LOCATION.
        TST R2 ; SET CONDITION FOR CALLER.
        RETURN
;
; HIGH SEGMENT COPY OF THE FLOATING I/O DATA TABLE.
;
XFLT10: .BYTE 15, 12 ; SYNC PAIR.
        .BYTE 001, 002, 004, 010, 020, 040, 100, 200 ; FLOATING 1.
        .BYTE 376, 375, 373, 367, 357, 337, 277, 177 ; FLOATING 0.
        .WORD 0 ; TERMINATOR.
        .DSABL AMA

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1 000001 .end

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ABAUD	166656	G	BIT4	=	000020	G	CNTNU	=	000062	DMA600	171160	IN300	173402						
AB100	166712		BIT5	=	000040	G	CQIO	=	177462	DPRV12=	000134	IN400	173402						
AB200	166722		BIT6	=	000100	G	CQIOA	=	177470	DPRV4	=	000120	IP	=	020000				
AB300	166740		BIT7	=	000200	G	CR	=	000015	G	DPRV8	=	000124	IPVXIT	177370				
AB400	166756		BIT8	=	000400	G	CRDS	=	166277	G	DS100	=	166346	IPW12	177364				
AB500	166770		BIT9	=	001000	G	CRLF	=	166274	G	DS200	=	166346	IPW4	177350				
AB600	166770		BOOTFO	=	177774	G	CSTMD	=	000006	G	ENDTAB	=	166655	IPV8	177356				
ACC	161146		BOOTST	=	172322		CTCC	=	000040		EOP	=	000002	IRX	163566				
ACCUM	173540	G	BRKENT	=	164674	G	CTCS	=	000024		EOPBIT=	=	000002	ISEXT	163600				
ADDRREG	165522	G	BSUPV	=	171170	G	CTMS	=	000070		ERRR	=	100000	G	ITX	163544			
ADSTKO	177700	G	BS100	=	171240		CTRL	=	000000		ERRFGB	=	100000	G	IXIT	163630			
AD100	165530		BS200	=	171300		CTTC	=	000054		ERROR	=	166264	G	KAT	=	170002		
AD200	165530		BS300	=	171326		CTV	=	000010		ERRTB	=	172750		KC\$DD	=	000022	G	
AD220	165550		BS400	=	171346		C.CLR	=	162200		EXAMIN	=	165742	G	KC\$DI	=	000006	G	
AD240	165560		BS500	=	171352		CB255	=	177526	G	EXMDS	=	165470		KC\$ED	=	000020	G	
AD250	165564		BS550	=	171372		DARFGB	=	000002	G	EXTEST	=	172570	G	KC\$EI	=	000004	G	
AD253	165574		BS570	=	171404		DATCOM	=	166404	G	EX10	=	165766		KC\$GS	=	000010	G	
AD255	165606		BS600	=	171420		DA100	=	166412		EX1000	=	166224		KC\$MAX	=	000022	G	
AD270	165614		BUFR1	=	150002		DA200	=	166412		EX1050	=	166242		KC\$NOP	=	000000	G	
AD280	165642		BUFR2	=	160002		DA370	=	166426		EX1200	=	166260		KC\$RD	=	000014	G	
AD290	165644		BYTES	=	170002		DA400	=	166452		EX1300	=	166262		KC\$RES	=	000002	G	
AD300	165646		B1200	=	000022		DA500	=	166460		EX20	=	165776		KC\$SS	=	000012	G	
AD400	165652		B2400	=	000032		DA600	=	166464		EX300	=	166020		KC\$WD	=	000016	G	
AD500	165666		B300	=	000002		DA700	=	166472		EX400	=	166030		KC.COM	=	000036	G	
AD600	165674		B4800	=	000042		DCDFGB	=	000001	G	EX500	=	166040		KC.EOM	=	004000	G	
AD700	165720		B600	=	000012		DC.DAT	=	161614		EX600	=	166040		KC.ICC	=	000040	G	
AD800	165724		B9600	=	000052		DC.LBO	=	161672		EX700	=	166056		KC.IDA	=	000100	G	
AI	175010		CABIT	=	010000		DC.RCV	=	161500		EX750	=	166072		KC.IDR	=	000200	G	
AI.BO	=	164377	CHA	=	0000003		DC.XIT	=	161676		EX760	=	166140		KC.LEW	=	003400	G	
AO.BI	=	165400	CHAINX	=	176100		DC.XMT	=	161406		EX770	=	166146		KC.VEC	=	177400	G	
APLPCO	177766	G	CHAIN1	=	175756		DECTST	=	170072	G	EX800	=	166156		KE\$DNA	=	000014	G	
APLPSO	177770	G	CHAIN2	=	176000		DEPOS	=	166474	G	EX900	=	166172		KE\$ILC	=	000006	G	
APLR00	177750	G	CHAIN4	=	176020		DE200	=	166526		EX950	=	166222		KE\$ILL	=	000010	G	
APLR10	177752	G	CHAIN5	=	176040		DE50	=	166512		EX970	=	166222		KE\$ILV	=	000012	G	
APLR20	177754	G	CHAIN6	=	176060		DINIT	=	173412	G	FAR	=	164116	G	KE\$MAX	=	000014	G	
APLR30	177756	G	CHAIH	=	000046		DISPRG	=	165450		FARSTR	=	172370	G	KE\$NDA	=	000002	G	
APLR40	177760	G	CHAIL	=	000042		DISPST	=	166346	G	FAS	=	171430	G	KE\$NDR	=	000004	G	
APLR50	177762	G	CHA2H	=	000044		DISPWD	=	166532	G	FCHPGB	=	000010	G	KE\$OK	=	000000	G	
APLSPO	177764	G	CHA2L	=	000040		DI100	=	166550		FERRD	=	000017	G	KH.CMD	=	175001	G	
ARDFGB	000004	G	CHB	=	0000004		DI200	=	166554		FLTO	=	163700		KH.CSD	=	177531	G	
A.SET	162130		CHEND	=	165742		DM	=	174400		FLT1	=	163670		KH.IOC	=	177541	G	
A4800	162126		CHKCHR	=	173614	G	DMACDA=	=	174454	G	FLT10	=	163666		KH.SC2	=	175005	G	
BBF10	000000	G	CHNOFO=	=	174442		DMAED	=	000002	G	FRERRB=	=	020000	G	KH.SC3	=	175007	G	
BBF20	177776	G	CHNSTO=	=	174446		DMALD	=	171032	G	FTLST	=	172736	G	KH.STA	=	175003	G	
BEVNT	=	000100	CHTAB	=	165734		DMAMMA=	=	174470	G	GETIN	=	173552	G	KL.CMD	=	175000	G	
BI	175024		CHX	=	0000004		DMAV	=	000164		GE100	=	173552		KL.CSA	=	177520	G	
BIACKV=	=	000130	CH100	=	173652		DMAXIT	=	175720		GE200	=	173610		KL.CSB	=	177522	G	
BIT0	=	000001	G	CH200	=	173670		DMA00A=	=	174442	G	GE300	=	173612		KL.CSC	=	177524	G
BIT1	=	000002	G	CH250	=	173702		DMA0SA=	=	174446	G	GO	=	166772	G	KL.CSD	=	177530	G
BIT10	=	002000	G	CH300	=	173704		DMA0VA=	=	174532	G	GP300	=	167176		KL.IOC	=	177540	G
BIT11	=	004000	G	CH400	=	173704		DMA1VA=	=	174530	G	HZ800	=	162124		KL.SC2	=	175004	G
BIT12	=	010000	G	CKSUM	=	161042		DMA100	=	171104		INDATA	=	166640		KL.SC3	=	175006	G
BIT13	=	020000	G	CLISP	=	170006		DMA200	=	171114		INHIB	=	170010		KL.STA	=	175002	G
BIT14	=	040000	G	CM	=	177574		DMA300	=	171142		INIT	=	173302	G	KM\$IDS	=	000360	G
BIT15	=	100000	G	CMDR	=	000054		DMA400	=	171150		INITST	=	172320		KM\$MAP	=	000016	G
BIT2	=	000004	G	CMREGA=	=	174454		DMA50	=	171046		IN100	=	173352		KM\$STF	=	000007	G
BIT3	=	000010	G	CNDPGB	=	000020	G	DMA500	=	171150		IN200	=	173356		KM\$SMS	=	000360	G

KPSINI	000000	G	KXSDME	040000	G	KXST04	100010	G	ODTSTK	177746	G	PWRV	=	000024
KPSWNC	000007	G	KXSDPE	000040	G	KXST05	100020	G	OPENDS	166301	G	PW050	173026	
KPSPBS	000005	G	KXSDRT	000200	G	KXST06	100040	G	ORERRB=	040000	G	PW100	173050	
KPSQOD	000003	G	KXSEXO	100000	G	KXST07	100100	G	PACS	=	000020	PW200	173112	
KPSQTS	000002	G	KXSFEP	000040	G	KXST10	100200	G	PADB	=	000032	PW300	173124	
KPSSTS	000001	G	KXSF01	000001	G	KXST11	100400	G	PAHS	=	000102	PW500	173152	
KPSWST	000004	G	KXSF02	000002	G	KXST12	101000	G	PAMS	=	000100	PW600	173156	
KRSQRP	040000	G	KXSF03	000004	G	KXST13	102000	G	PARLBD	000016	G	PW700	173252	
KRSTMS	000001	G	KXSF04	000010	G	KXS2EM	000002	G	PAV	=	000004	QA	177562	
KS.ALN	003400	G	KXSF05	000020	G	K3K	=	014000	PRCS	=	000022	QADR	=	170004
KS.DA	000200	G	KXSF06	000040	G	LA	177566		PBDB	=	000034	QAHI	=	170002
KS.DBG	020000	G	KXSF07	000100	G	LADR	=	170006	PBHS	=	000122	QALO	=	170004
KS.DR	000040	G	KXSF10	000200	G	LRTEST	163712	G	PBMS	=	000120	QCOMIN	167460	G
KS.EOM	000100	G	KXSF11	000400	G	LB100	163712		PBRFB	=	000002	QC100	167560	
KS.ERC	000036	G	KXSF12	001000	G	LEDTSO	000017	G	PBRF	=	000070	QC120	167616	
KS.ERR	100000	G	KXSF13	002000	G	LF	000012	G	PRV	=	000006	QC150	167626	
KS.ON	040000	G	KXSG00	000010	G	LS0	000017	G	PCDB	=	000036	QC200	167640	
KWSPAB	040000	G	KXSINC	000004	G	LS1	000016	G	PCDD	=	000014	QC300	167660	
KWSPB0	000001	G	KXSI20	000010	G	LS10	000005	G	PCRLF	165510		QC350	167714	
KWSPB1	000002	G	KXSI24	000020	G	LS11	000004	G	PERV	173000	G	QC380	167734	
KWSPB2	000004	G	KXSI34	000040	G	LS12	000003	G	PEVNT	=	000104	QC400	167736	
KWSPB3	000010	G	KXSLD0	000001	G	LS13	000002	G	PIOAV	=	000154	QC420	167776	
KWSPB4	000020	G	KXSLD1	000002	G	LS14	000001	G	PIOAVA=	177004	G	QC440	170002	
KWSPB5	000040	G	KXSLD2	000004	G	LS15	000000	G	PIOBV	=	000160	QC445	170022	
KWSPB6	000100	G	KXSLD3	000010	G	LS2	000015	G	PIOBVA=	177006	G	QC447	170024	
KWSPB7	000200	G	KXSMP0	000002	G	LS3	000014	G	PIOD	174404		QC450	170042	
KWSPCO	100000	G	KXSMP1	000004	G	LS4	000013	G	PIOD1	174450		QC470	170050	
KWSPHD	001000	G	KXSMP2	000010	G	LS5	000012	G	PIOD2	174532		QC50	167512	
KWSPLD	000400	G	KXSNOP	000040	G	LS6	000011	G	PIOD3	174562		QC500	170052	
KWSPOD	002000	G	KXSNXF	010000	G	LS7	000010	G	PIOICA=	177000	G	QC600	170056	
KWSPID	004000	G	KXSNXM	100000	G	LS8	000007	G	PIOTVA=	177010	G	QC70	167524	
KWSP2D	010000	G	KXSODC	000010	G	LS9	000006	G	PIOXIT	174746		QIO	177560	
KWSP3D	020000	G	KXSODT	000001	G	MAINTB=	000004	G	PIT	174152		QIOC	177600	
KW.CMD	175000	G	KXSOHL	000020	G	HCC	=	000002	PIT1	174222		QIRV	=	000144
KW.CSA	177520	G	KXSOMO	000001	G	MEM1	160304		PRIBD	000001	G	QIRV1	=	000150
KW.CSB	177522	G	KXSORO	000002	G	MEM2	160312		PROC	167010	G	QIXIT	176372	
KW.CSC	177524	G	KXSPRO	000020	G	MEM3	160320		PROMPT	166266	G	QODTM	171432	G
KW.CSD	177530	G	KXSPWF	001000	G	MEM3A	160324		PRTYV	=	000114	QODTMD	000005	G
KW.DAT	000004	G	KXSQIE	020000	G	MIC	=	000000	PRO	=	000000	QSRET	171444	G
KW.DCO	000000	G	KXSQOF	000200	G	HMR	=	000070	PR1	=	000040	QS100	171476	
KW.DCO	175010	G	KXSQRE	002000	G	MMRPGA=	174470		PR2	=	000100	QS1000	171710	
KW.DC1	175020	G	KXSQRF	004000	G	MODE	=	170004	PR3	=	000140	QS1100	171726	
KW.DST	000002	G	KXSRTE	000100	G	NACBIT=	004000		PR4	=	000200	QS200	171476	
KW.IOC	177540	G	KXSR20	000001	G	NECV	=	000070	PR5	=	000240	QS300	171536	
KW.SC2	175004	G	KXSR24	000002	G	NECXIT	163470		PR6	=	000300	QS400	171560	
KW.SC3	175006	G	KXSR34	000004	G	NEC.AA	162262		PR7	=	000340	QS500	171612	
KW.STA	175002	G	KXSSEF	000010	G	NEC.AS	162242		PUTEST	172324	G	QS700	171632	
KXSBAT	002000	G	KXSSHC	000020	G	NEC.DA	162210		PUTSDS	000007	G	QS800	171656	
KXSBDF	020000	G	KXSSMA	000004	G	NEC.DM	162624		PUI00	172440		QS900	171702	
KXSBHE	000400	G	KXSSOF	000100	G	NEC.EX	163640		PUI010	172566		RAMLO	160634	
KXSBHF	001000	G	KXSSXT	004000	G	NEC.I	163522		PU20	172360		RAMLOA	160636	
KXSBQI	010000	G	KXSTIS	000020	G	NEC.MD	163144		PU30	172372		RBOT1	000000	G
KXSCHE	100000	G	KXSTRC	000001	G	NEC.SY	162250		PU400	172526		RBOT2	040000	G
KXSCTE	000200	G	KXSTTC	000010	G	NFERRD	000010	G	PUS0	172434		RBOT3	100000	G
KXSDEN	000100	G	KXST01	100001	G	NFFWDO	177772	G	PUS00	172534		RBUF1A=	177562	G
KXSDOD	000004	G	KXST02	100002	G	NNCED	000000	G	PUG00	172536		RCSR1A=	177560	G
KXSDMC	000002	G	KXST03	100004	G	ODTSTG	177702	G	PWRUP	173012	G	RCVACB=	004000	G

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RCVBKB= 004000 G	SN200 172262	S2ALBD 000014 G	TST6 161344	T7 - 160034 G
RCVONB= 000200 G	SODTM 164626 G	S2BLBD 000015 G	TST7 161730	T7AETB 171002
RCVIEB= 000100 G	SODTMD 000004 G	TC = 000001	TU100 171740	T7BETB 171006
RD = 000000	SO100 164746	TCLK 161164	TU1000 172150	T7ERR 170664 G
RDB = 177776	SO1000 165104	TCPU 161150	TU120 171774	T7ERR1 170676
REGDIS 166303 G	SO1300 165142	TCXIT 161322	TU125 171776	T7ERR2 170704
REGFGB 000200 G	SO1400 165170	TDC 161344	TU130 172012	UROMOD 000011 G
REINIT 173016 G	SO1450 165174	TDMA 175106	TU150 172042	UROMID 000012 G
RESTRT 164000 G	SO1470 165174	TDMA1 175174	TU200 172060	VERS 173774 G
RE1000 164314	SO1500 165240	TDMA2 175276	TU300 172064	WAITD 000003 G
RE1010 164352	SO1550 165254	TDMA3 175346	TU400 172066	WAITST 167402 G
RE1020 164352	SO1552 165304	TDPR 176432	TU500 172102	WA100 167402
RE1040 164352	SO1555 165312	TDPR2 176520	TU58BT 171734 G	WA200 167446
RE1045 164372	SO1557 165322	TE100 172630	TU600 172110	WA300 167452
RE1050 164412	SO1560 165330	TE200 172642	TU800 172144	WC 177572
RE1060 164416	SO1565 165356	TE250 172712	TU900 172144	WCTBL 175742
RE1070 164416	SO1567 165364	TE300 172726	TO = 160000 G	WQIO 177410
RE1072 164442	SO1569 165376	TE400 172740	T1 = 160004 G	WQIOA 177416
RE1075 164450	SO1570 165402	TE500 160040	T1ERR 170506 G	WRT = 000010
RE1080 164450	SO1600 165404	TIDR 160040	T1ERR1 170532	XBRKB = 000001 G
RE200 164074	SO1700 165410	TIPV1 176676	T1ERR2 170540	XBUF1A= 177566 G
RE250 164104	SO1800 165412	TIPV2 177100	T10 = 160000 G	XCSR1A= 177564 G
RE400 164106	SO1850 165412	TIPXIT 177260	T10ERR 170720 G	XCVR = 000140
RE450 164120	SO1900 165440	TMP1 = 170002	T10ETB 171012	XDB = 000002
RE500 164142	SO200 164746	TMP2 = 170004	T11 = 160004 G	XFLT10 177646
RE600 164226	SO300 164776	TMP3 = 170006	T11ERR 170726 G	XIEB = 000100 G
RE700 164260	SO400 165006	TMP4 = 170010	T11ETB 171016	XOFF = 000023
RE800 164270	SO700 165054	TMP5 = 170012	T12 = 160010 G	XOFFGB 000040 G
RE900 164274	SO800 165060	TMP6 = 170014	T12ERR 170734 G	XON = 000021
RNGFGB 000002 G	SO900 165062	TMP7 = 170016	T12ETB 171022	XRAMLO 177602
RQIO 177400	SPACE 166272 G	TMP8 = 170020	T13 = 160014 G	XRDYB = 000200 G
RSTV 173004 G	SPOFF 000014 G	TNEC 161730	T13ERR 170742 G	XSCSR = 177530
RTOP1 077776 G	SPR5SU 173706 G	TNNCM1 170754	T13ETB 171026	XSCSRA = 177520
RTOP2 137776 G	SP1 077762 G	TNNCOM 170746	T14 = 160020 G	XSCSRB = 177522
RTOP3 157776 G	SP2 137762 G	TNNINX 170762	T15 = 160024 G	XSCSRC = 177524
SAVERG 164452 G	SP200 173724	TNNXIT 170764	T16 = 160030 G	XSCRCO= 177526
SD100 172300	SP3 157762 G	TPI0 174040	T17 = 160034 G	SDMA = 174400
SEND 172300	SP300 173752	TQIR 176102	T2 = 160010 G	SDPR = 175000
SETIE = 170010	SP400 173756	TRAM 160272	T2ERR 170546 G	SEF = 000005
SETLDJ 167202 G	SR100 164474	TRAPX 167366 G	T2ERR1 170562	SEF1 = 177776
SETLED 167200 G	SR200 164526	TRAP10 167314 G	T3 = 160014 G	SEN = 000014
SE100 167222	SR300 164536	TPAP24 167356 G	T3ERR 170576 G	SIPV = 175000
SE150 167242	SR400 164622	TRAP4 167252 G	T3ERR1 170612	SI8254= 175720
SE200 167242	SSRET 164654 G	TPOM 160700	T3ERR2 170626	SLEDS = 177524
SE300 167250	STACHN= 170012	TR1010 167344	T4 = 160020 G	SPIO = 177000
SKTA 160546	STAT = 177774	TR410 167302	T4ERR 170642 G	SDQPR1= 160000
SL1RV = 000060	STATS = 170006	TST1 160040	T4ETB 170766	SDQPR2= 175400
SL1XV = 000064	STAT1 = 000056	TST10 174040	T5 = 160024 G	SQIR = 177532
SL2CAA= 175704 G	STAT2 = 000054	TST11 175106	T5ERR 170650 G	SSL1 = 177560
SL2CBA= 175714 G	STAT3 = 000054	TST12 176102	T5ETB 170772	SSL2 = 175700
SL2SAA= 175700 G	STSENL= 000010	TST13 176432	T6 = 160030 G	STN = 000013
SL2SBA= 175710 G	STSTAB 170354	TST2 160272	T6ERR 170656 G	STOP = 000005
SNDBRK 172234	S.SET 162150	TST3 160700	T6ETB 170776	SUID = 177524
SN100 172240	SORRGA= 174456	TST4 161150		
	SILBD 000013 G	TST5 161164		
. ABS. 177672 000 (RW,I,GBL,ABS,OVR)				
000000 001 (RW,I,LCL,REL,COM)				