digital

DF10 DATA CHANNEL

PDP-10

DF10

DATA CHANNEL

MAINTENANCE MANUAL

June 1968

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CHAPTER 1

INTRODUCTION

This manual and the documents referenced herein provide the information necessary for the installation, operation and maintenance of the DF10 Data Channel Unit. The DF10 Data Channel is an optional unit available with the PDP-10 System, manufactured by Digital Equipment Corporation (DEC) Maynard, Massachusetts. The unit is a transfer device that provides data transfers between an I/O device and PDP-10 core memory. The DF10 allows up to eight I/O devices to be connected to the memory bus, but only one device can communicate at a time. The I/O device initiates communications on a first-come first-served basis. Once enabled the DF10 functions as an I/O processor, transferring data operations independently of the program running. The initial link is established by the program when it initializes the I/O device. The I/O device requires access to the data channel and when access is granted, the device sets up the data channel to transfer data.

The channel provides control and data lines to and from the device, and supplies address, data, and control information to and from the PDP-10 memory. An RC10 Synchronizer-Adapter can also be incorporated into this system.

The level of discussion in this manual assumes that the reader is familiar with the logic symbology used by DEC, and the general operations of the PDP-10 processors and devices connected to the DF10 Data Channel.

1.1   REFERENCED DOCUMENTATION

The documents which are available to supplement the information in this manual can be obtained from the nearest DEC regional office or by writing to:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

1.1.1   Available Documentation

Title	Document No.	Description
Digital Logic Handbook	C-105	Description and specifications of the standard FLIP CHIP modules. Simplified explanation of the selection and use of the modules.

Available Documentation (Cont)

Title	Document No.	Description
PDP-10 Maintenance Manuals		
Volume I	DEC-10-HMAA-D	Complete information on the internal operation of the KA10 Processor Memory, basic I/O, and options.
Volume II	DEC-10-HMBA-D	Engineering drawings associated with the KA10 Processor.
Volume III	DEC-10-HMCA-D	Description, schematics and specifications of the special modules used in the PDP-10 System.
PDP-10 Peripheral Device Engineering Drawing Set (Volume III)	DEC-10-I6CA-D	Logic block diagrams and pertinent engineering drawings for the DF10, RC10 and TM10 options.
RC10 Disk Synchronizer-Adapter Instruction Manual	DEC-10-I5AA-D	Installation, operation and maintenance instructions for the RC10 Unit.
PDP-10 Installation Manual		Detailed information on the planning and installation of a PDP-10 System.
PDP-10 System Reference Manual	DEC-10-HGAA-D	Programming and operating information for the PDP-10 Processor and options.

1.2 EQUIPMENT SPECIFICATIONS

The DF10 Unit consists of a standard 19 in. cabinet Type CAB9-B which is constructed with welded steel frames and sheet aluminum covering. Access doors are mounted on the front and rear of the cabinet and are held closed by magnetic latches. The power control and dc power supply are mounted inside the rear access door on a plenum door that is latched at the top by a spring-loaded pin. Module mounting panels are located behind the front door with the wiring side facing outward. Access to the modules for removal, replacement and/or adjustment is gained through the rear of the cabinet. A fan at the bottom of the cabinet draws cooling air into the cabinet through a dust filter, and a fan assembly mounted in the logic rack passes the cooling air over the modules. The air is exhausted through an opening at the top of the cabinet.

The DF10 logic receives power from 2 Type 728 Power Supplies which are controlled by a Type 844 Power Control Unit. Two convenience receptacles are located on the front panel.

Figure 1-1 shows the assemblies mounted in the front and rear of the DF10 Unit. If the RC10 Synchronizer-Adapter is required, it can be mounted within the same cabinet.
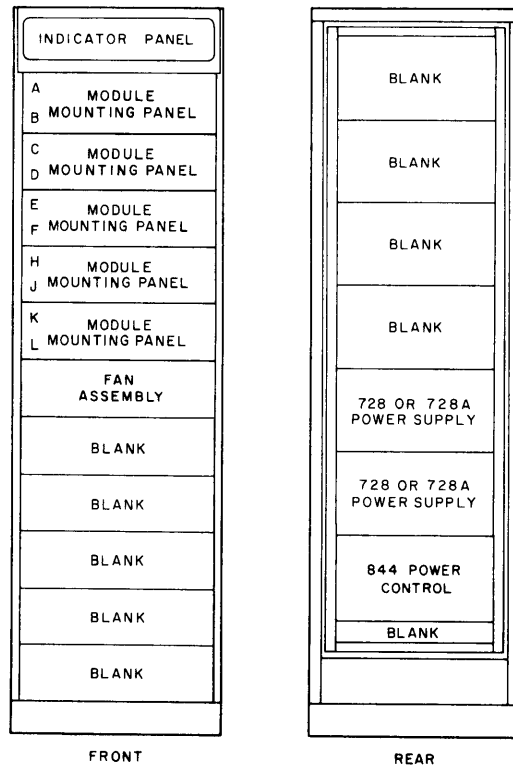
Figure 1-1 DF10 Data Channel, Assembly Locations

1.3   PHYSICAL SPECIFICATIONS

Physical Dimensions:	69 in. high, 19-3/4 in. wide, 27 in. deep
Weight:	200 lbs.
Power Requirement:	115V, 60 Hz, 1 phase primary power Type 728 Power Supply (2) Type 844 Power Control (1) Also 230V 50 Hz, 1 phase
Transfer Rate:	10^6 words per second maximum
Environmental Condition:	Thermal Dissipation – 682 BTU Operating Temperature -60° to 100°F Relative Humidity – 20% to 80%

CHAPTER 2

OPERATION AND PROGRAMMING

Operation of the data channel is initiated by the I/O device that has gained access to it. For an I/O device to transfer data, the program must first insure that the critical words for the data channel are appropriately placed in memory, the data block to be transferred (or to be filled) appropriately reserved or set up, and the I/O device enabled. When the program enables the device with desired parameters, it also sends the initial control word address to the I/O device. The device requires access to the data channel and when access is gained, the I/O device sends the initial control word address to the data channel. The data channel then fetches the initial control word from memory and starts transferring data based upon parameters specified by the control word. Normally, the control contains the DA (data address) and WC (word count). The WC and DA are stored in registers within the data channel. As each data transfer is processed, both the WC and DA are updated. When block transfer is complete, as signified by WC going to zero, the next control word is fetched from memory and if it is zero, the data transfer cycle is terminated.

2.1   INDICATOR PANEL

Figure 2-1 shows the configuration of indicator lights on the indicator panel. These lights display the condition of all major elements of the DF10 Data Channel. Table 2-1 lists the indicators and their function.
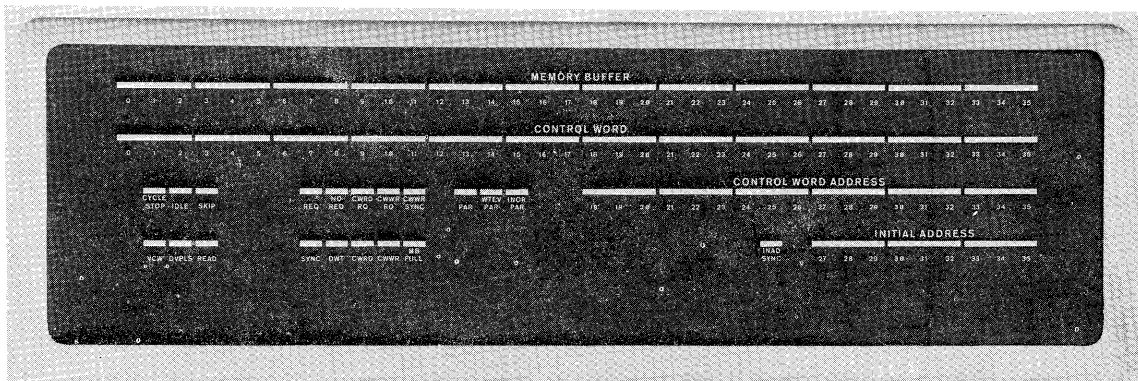

Figure 2-1 DF10 Indicator Panel Configuration

Table 2-1
DF10 INDICATOR PANEL

Indicator	Function
MEMORY BUFFER (Indicators 0-35)	Indicates the contents of the Memory Buffer Register, bits 0 through 35.
CONTROL WORD (Indicators 0-35)	Indicates the content of the Control Word, bits 0 through 35.
CONTROL WORD ADDRESS (Indicators 18-35)	Indicates the content of the Control Word Address Register bits 18 through 35.
INITIAL ADDRESS (Indicators 27-35)	Indicates the content of the Initial Address Register, bits 27 through 35.
CYCLE STOP	Lights to indicate the data channel is ready to terminate operations.
IDLE	Lights to indicate the data channel is in an idle status.
SKIP	Lights to indicate that the control word fetched has a zero data address portion.
REQ	Lights to indicate that a Request Cycle signal is sent to memory provided NO REQ indicator is off.
NO REQ	Lights to indicate that the Request Cycle signal is being suppressed.
CWRD RQ	Lights to indicate a control word read request has been initiated.
CWWR RQ	Lights to indicate a control word write request has been initiated.
CWWR SYNC	Lights to indicate that a write control word request is being held until required by the normal control sequence.
PAR	Lights to indicate a parity bit is sent from memory.
WTEV PAR	Lights to indicate the data transfers to memory will have even parity.
INOR PAR	Lights where a pulse from a memory or memory-like device indicates that the device contains no parity (37th) bit.
VCW	Lights to indicate the control word is valid (non-zero word count).
DVPLS	Lights to indicate that a device pulse has been received by the data channel. It normally goes off when the memory buffer is emptied.
READ	Lights to indicate that the channel is performing data transfer into memory and that the device connected to the channel did not generate a SAWRITE signal at the beginning of the cycle.
SYNC	Lights to indicate that a memory cycle has been initiated and remains "on" until all memory control flip-flops return to their normal state.

Table 2-1 (cont)
DF10 Indicator Panel

Indicator	Function
	These lights indicate the processing of data to and from memory.
DWT	Lights to indicate a data word memory transfer.
CWRD	Lights to indicate a control word read operation.
CWWR	Lights to indicate a control word write operation.
MB FULL	Lights to indicate the memory buffer is loaded.
(INAD SYNC)	Lights to indicate the INAD SYNC flip-flop is set which locks the initial control word address into the Initial Address Register (INAD 27-34).

2.2 CONTROL WORD FORMAT

During the initializing phase, the I/O device which has gained access to the data channel sends the initial control word address to the data channel. The control word is fetched from memory and evaluated to determine the ensuing operation. The format of the control word contains the data address (DA) and the word count (WC) of the data transfer as shown below. It is the WC and DA position of the control word that is evaluated. The format of the control word has the following meaning.

WC	DA	Function
$= 0$	$= 0$	Terminate the data channel operation with the I/O device. Set CHANNEL BUSY = 0 and IDLE = 1.
$= 0$	$\neq 0$	DA is sent to the control word address register and a new control word is fetched from that location in memory.
$\neq 0$	$= 0$	If SAWRITE is not asserted (writing memory), the channel will receive the number of words specified by WC from the device, but will not put them into memory. This feature is useful for tape and disk applications (see examples).
$\neq 0$	$\neq 0$	Transfer the number of words indicated by WC. Transfer the first word into or from the address specified by DA + 1. After each transfer, increment the DA register by 1 and transfer the next word to or from the incremented address.

If the evaluation of the control word specifies a data transfer, the DA and WC are stored in their respective registers. The DA is incremented before the first transfer.

The initial control word address, B, an even number, is supplied by the device. Immediately upon receiving the CHANNEL BUSY signal from the channel, the device should send 8 bits of initial address (bits 27 through 34) on the data bus and the DEVICE PULSE. There is no latest-time for sending these signals, the channel will wait indefinitely to receive them. Bits 0 through 17 and 35 must be zero to insure proper operation.

If a control word with WC = 0 is stored in B, the channel will load DA into the control word address register and fetch another control word from the location specified in the DA.

The control word address register is incremented by 1 after each control word fetch. Thus, when the number of words specified by the word count of a particular control word has been transferred, a new control word is fetched from the next address.

2.2.1 Typical Program Examples

All numbers are in octal representation.

Memory Location	Contents	
	WC	DA
B	0	001000
1000	777700	001777
1001	0	0

If SAWRITE is not asserted by the device, the channel will accept up to 100 words from the device, and store them sequentially in memory locations 2000 through 2077. The channel will then reset the CHANNEL BUSY signal. Note that 1001 must contain zero to stop the channel.

Memory Location	Contents	
	WC	DA
B	776000	004777
B + 1	0	0

If SAWRITE is asserted, the channel will deliver up to 2000 words to the device. The first word will come from 5000 and the others sequentially. The channel user should understand that if the device sends a WRITE CONTROL WORD REQUEST pulse while the CHANNEL BUSY signal is asserted, the contents of B + 1 will change, and may cause undersirable consequences.

Memory Location	Contents	
	WC	DA
B	0	000500
500	777700	000777
501	777000	004777
502	777300	0
503	777000	005777
504	0	0

If SAWRITE is not asserted, and this program runs to completion, the first 100 words delivered by (or from) the device (for example a file header) will go to 1000 through 1077, the next 1000 words will go to 5000 through 5777, the next 500 words will be skipped and the next 1000 words will go to 6000 through 6777. In the case of disk or tape operations, skipping saves memory space, and allows this type of transfer without reinitiating the device.

If SAWRITE had been asserted, the first 100 words delivered to the device would have come from 1000 through 1077, the next 1000 words from 5000 through 5777, the next 500 from 0 through 477, and the next 1000 words from 6000 through 6777.

2.3   WRITE CONTROL WORD

The write control word facility permits the device using the data channel to initiate a control word write. The device accomplishes this by asserting the WRITE CONTROL REQUEST signal and the data channel responds immediately by writing the control word into memory. Furthermore when the data channel terminates the data transfer operation, it automatically writes the control word into memory. The memory address for the control word write is the initial control word address + 1. The control word written into memory contains the contents of the control word address register in bits 0 through 17 and the contents of the data address register in bits 18 through 35.

2.4   WRITE EVEN PARITY

Normally, the parity for data transfer between data channel and core memory is odd parity since the central processor and other devices using memory, check for odd parity. As a maintenance check of the parity circuits, even parity can be specified by the device, by asserting the WRITE EVEN PARITY signal. Data written into memory from the data channel now contains even parity. Any device accessing this data from memory would expect to find a parity error since the device checks for odd parity.

CHAPTER 3
PRINCIPLES OF OPERATION

This chapter describes the principles of operation of the DF10 Data Channel. The detailed logic descriptions make reference to the logic drawings listed in Chapter 6. Reference to logic drawings is by mnemonic signal names, since all signal names reflect their logic drawing origination. For example, signal CCB CLEAR MB originates on drawing P-BS-DF10-0-CCB.

Before describing the detailed logic of the data channel, a general description and a block diagram is presented.

3.1   DF10 DATA CHANNEL DESCRIPTION

Operation is first initiated by an I/O device that is connected to the data channel. The PDP-10 program initiates operation when it issues an I/O instruction to the device to start operation and provide the initial control word address. The control word address is stored by the I/O device until it gains access to the data channel.

When the I/O device gains access to the data channel, it sends the initial control word address to the data channel which stores this address in the control word address register. The data channel then fetches the control word, normally consisting of WC (word count) and DA (data address). The WC and DA are stored in their respective data channel registers. The WC register specifies the number of data words to transfer and the DA specifies the core memory location. After a word transfer between core memory and the device communicating with the data channel, the WC is decremented (i.e., WC contains 2's complement and is incremented) and the DA is incremented. When the WC overflows, the number of words initially specified have been transferred and the next control word is fetched from core memory. If the control word contains all 0s, the end of communications is specified and the data channel terminates operation.

A number of devices can be connected to the data channel; however, the data channel comunicates with only one at a time. To establish, maintain, and terminate communications, the following signals are exchanged to between device and data channel.

<u>Data Bus</u>	This incorporates 36 bidirectional data pulse lines. These signals are 100 ns negative-going pulses swinging from ground to -3V.
<u>Channel Pulse</u>	This 100 ns negative-going pulse is sent from the channel. It accompanies the data pulses when the channel is sending data to the device. It also signifies a readiness to receive data when the device is trying to send data to memory.

<u>Device Pulse</u>	This signal is similar in function to the channel pulse signal. It accompanies the data when the device is sending, and signifies readiness to receive when data flow is toward the device.
<u>Channel Start</u>	This is a level (-3V for true) which is sent from the device to the channel. It will start the channel into operation when asserted.
<u>Sawrite</u>	This signal controls the direction of data transfer. When true, it signifies the device is writing some medium (reading memory). The timing is the same as that for CHANNEL START.
<u>Channel Busy</u>	This signal comes from the channel and is asserted (-3V) sometime after CHANNEL START is asserted from the device. The device must not put anything on the bus until this signal is asserted. When this signal goes false after having been true, the channel has terminated for one reason or another. CHANNEL START and CHANNEL BUSY must all be false for at least 400 ns prior to re-assertion of CHANNEL START.
<u>Write Control Word Request</u>	This negative 100 ns pulse from the device causes the channel to store the current contents of the data address register and the control word address register into memory location B + 1 where B (an even number) is the channel initial control word address. The contents of the control word address register go into bit positions 0 through 17 and the contents of the data address register into bits 18 through 35. Upon any channel termination, the control word as specified above, is written into memory at B + 1 (as above) automatically.
<u>Write Control Word Complete</u>	This pulse from the channel signals the completion of the operation requested above. This pulse does not occur on the automatic transfer.
<u>Channel Reset</u>	Forces the data channel to its clear state.
<u>Write Even Parity</u>	Causes data channel to write even parity into memory.
<u>No Such Memory</u>	This pulse is sent from the channel as CHANNEL BUSY goes off and indicates that the memory addressed failed to respond.
<u>Control Word Parity Error</u>	If a control word is fetched from the memory by the channel and the word has a parity error, CHANNEL BUSY is reset and this pulse is sent to the device from the channel.
<u>Data Word Parity Error</u>	This pulse accompanies the data and the CHANNEL PULSE when a data word, which was read from memory with a parity error, is sent to the device.

The I/O devices attached to a data channel are arranged as shown in Figure 3-1 (only the pertinent signals are shown). In order for a device to gain access to the data channel, it must generate a CHANNEL START and receive a CHANNEL BUSY. If a device is not actively engaged with the data channel, it relays the CHANNEL START and CHANNEL BUSY. A device that is relaying CHANNEL START is prevented from generating its own CHANNEL START. A device that is busy with the data channel does not relay CHANNEL BUSY.
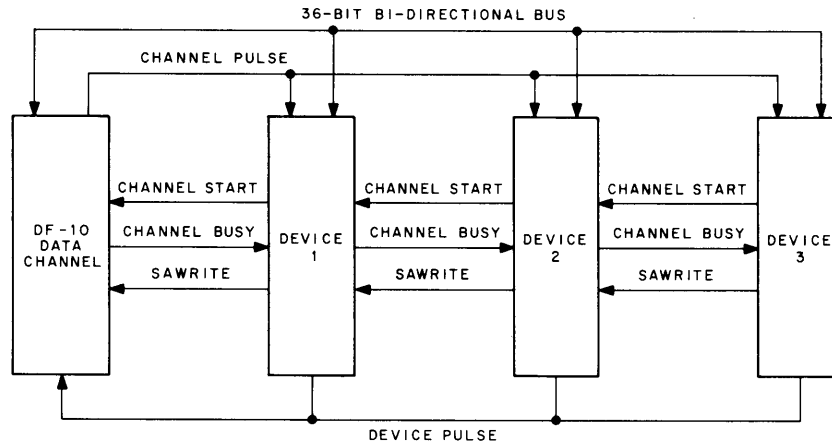

Figure 3-1   Data Channel Communication

To further pursue data channel communication, assume that devices 1 and 2 are not busy and device 3 initiates communication by asserting its CHANNEL START signal. It is applied to device 2 and since device 2 is not busy, it relays the CHANNEL START. Similarly, device 1 relays CHANNEL START. The data channel acknowledges the CHANNEL START by asserting the CHANNEL BUSY. The data channel does not know which device requested access; the only thing it knows is that it received a CHANNEL START and it responds by asserting CHANNEL BUSY. Furthermore, the data channel responds only to stimulus of the control signals by transferring data to and from the data bus or starting and stopping operation. It is the responsibility of the devices to determine which has access.

Since devices 1 and 2 are not busy, they relay the CHANNEL BUSY signal to device 3. Upon receipt of CHANNEL BUSY, device 3 has access to the data channel and can communicate via use of data bus. A device requires two things to gain access to the data channel; the assertion of its own CHANNEL START and the receipt of CHANNEL BUSY.

To demonstrate this dual requirement, assume that device 2 is communicating with the data channel. It has asserted its CHANNEL START and received a CHANNEL BUSY. It does not relay CHANNEL BUSY to device 3. If now, device 3 attempts communication, it can assert its CHANNEL

START since it is not relaying CHANNEL START, however, since device 2 is already generating a CHANNEL START, it essentially ignores the CHANNEL START from device 3. The CHANNEL BUSY is not relayed to device 3; therefore, device 3 does not gain access to the data channel because of the two requirements, assertion of CHANNEL START and receipt of CHANNEL BUSY. Device 3 now must wait until device 2 has finished with the data channel.

Either device 2 or data channel can terminate operation. The data channel terminates operation by removing CHANNEL BUSY and the device responds by negating CHANNEL START. The device terminates operation by removing CHANNEL START and the data channel responds by negating CHANNEL BUSY. After termination, device 3 is now free to communicate; however, the data channel requires at least 400 ns between the negation of CHANNEL BUSY and CHANNEL START and the assertion CHANNEL START. In this case, requirement is imposed upon device 2 (or any other device that is generating or relaying CHANNEL START and receives the on-to-off transition of CHANNEL BUSY). When termination occurs, the device must inhibit the generation or relaying of CHANNEL START for 400 ns.

3.2   BLOCK DIAGRAM DESCRIPTION

Assuming initial operation, a device requests access to the data channel by generating CHANNEL START (refer to Figure 3-2). The data channel responds by resetting it IDLE flip-flop and asserting CHANNEL BUSY which is acknowledgement to the device that it has access to the data channel. The data channel now prepares to receive the initial control word address.

The device responds to receiving CHANNEL BUSY by generating the DEVICE PULSE and transferring the initial control word to the data channel (into CWAD – control word address register via MB, the memory buffer). The data channel now fetches the control word from memory. The memory transfers the control word to the MB (memory buffer) where it is evaluated. The left half of MB corresponds to the WC(word count) portion of the control word and the right half corresponds to the DA (data address) portion.

When both the WC and DA are not equal to 0, the data transfer starts. The direction of transfer is specified by SAWRITE. The address that the data is either written into or read from is contained in the DA. The number of words transferred is determined by the 2's complement number in the WC. On each data transfer, the WC and DA are incremented by 1 count. When the WC overflows, a new control word is fetched (read) from memory.

When the WC is not equal to 0 and the DA is equal to 0 and the SAWRITE signal indicates writing into memory, the channel receives the number of words specified by the WC from the device, but does not write them into memory. This allows the channel to skip certain data.
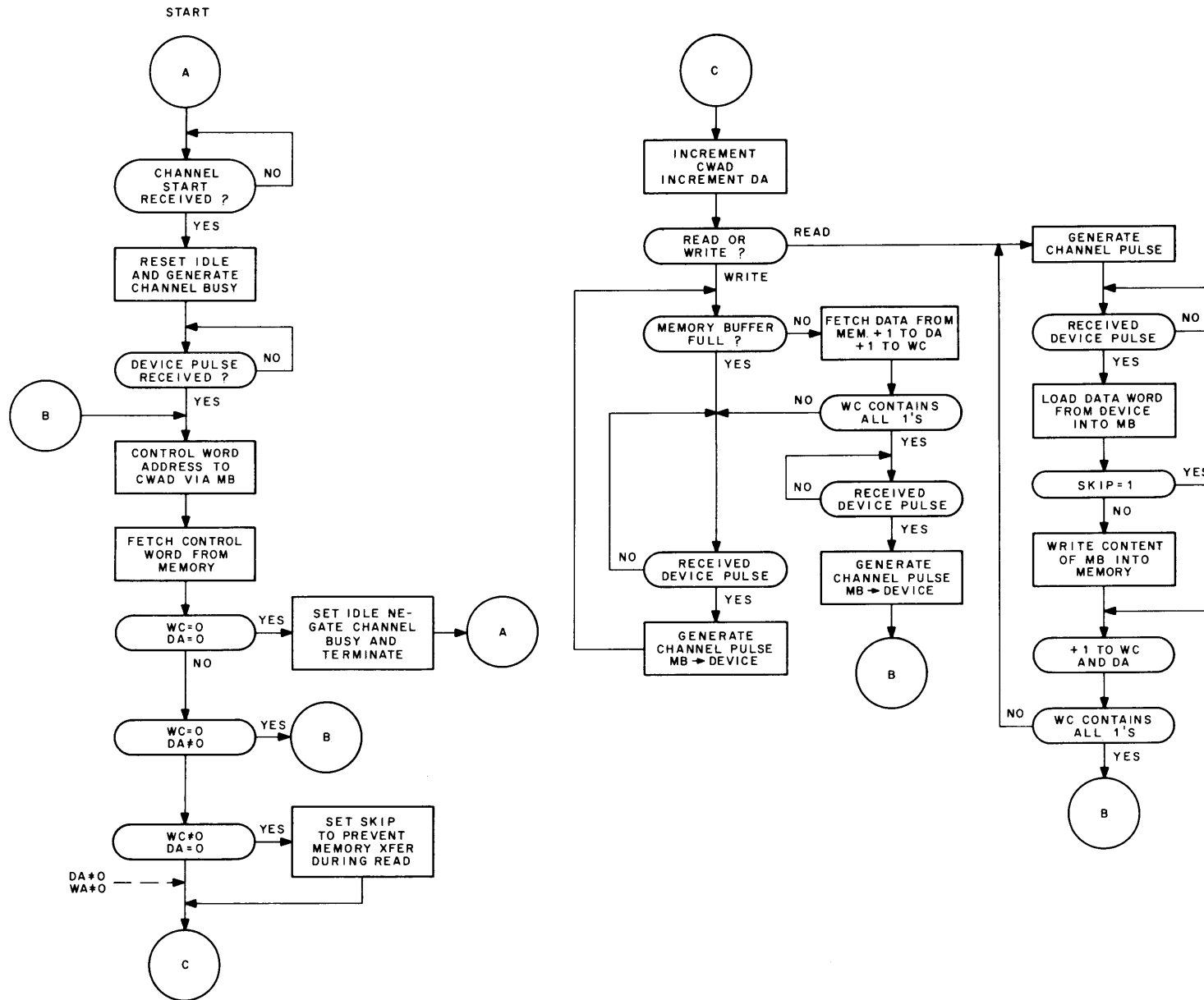
Figure 3-2 DF10 Flow Diagram

3-5

When the WC is equal to 0 and the DA is not equal to 0, the address currently contained in the DA is transferred to the control word address register (CWAD). This becomes the address of the next control word (WC and DA) and a control word fetch cycle is initiated. This capability is similar to a jump instruction.

If both the WC and DA are 0, the data channel terminates operation by setting IDLE and removing CHANNEL BUSY.

After control word evaluation, assuming a data transfer cycle, the CWAD is incremented. For a write operation, a data word is obtained from memory at the earliest possible time. The data word is transferred to the data channel MB. For the first data word obtained, it is immediately transferred to the device, since the device signified that it was ready with the initial DEVICE PULSE. When the MB is empty a memory cycle is initiated to load MB. When MB is full it waits for the DEVICE PULSE from the device. During each memory fetch, the DA and WC are incremented.

When the WC contains all 0's and the MB is empty, then a control word fetch is executed to obtain the next control word.

For a read operation, the device sends the data to the MB and generates DEVICE PULSE. The data channel transfers the data word to memory, increments the DA and WC and then generates the CHANNEL PULSE. This operation is repeated until the WC contains all 1's, at which time the next control word is fetched and evaluated.

3.3   DETAILED LOGIC DESCRIPTION

For the following description refer to the flow charts and logic diagram referenced in Chapter 6. The state of control circuits are assumed to be as shown in Flow Chart A, drawing D-DF10-0-00A.

3.3.1   Initial Operation

For the initial operation, assume that a device is going to read an I/O medium and transfer data to memory via data channel.

Operation starts when the device generates CHANNEL START. It comes in on the channel bus (drawing CBC) and generates CBC CHANNEL START (refer also to Flow Chart A, referenced in Chapter 6.) CBC CHANNEL START resets CYCLE STOP and generates CCA START which turns off CCA IDLE and generates CCB CLEAR MB which clears the MB (memory buffer) in preparation for the initial control word address from the device. CCA IDLE (0) generates CCC CHANNEL BUSY which goes back to the device to acknowledge access to the data channel.

The device also negates or asserts the SAWRITE signal to signify the read or write mode respectively, which either sets or resets CCA DEV READ. The CIA INAD SYNC (0) is true at this time.

In response to CHANNEL BUSY, the device sends the control word initial address data strobes (via channel bus, CBC CHND 27 through 34) which strobes the data into the MB. (The CCC WRITE MEM GATE 1, 2, 3 signals are on at this time due to CCA INAD SYNC (0) being true). The device also generates the CBC DEVICE PULSE, which after a delay generates CCA XFER CW (transfer control word).

CCB DEVPULS is not generated because CIA INAD SYNC (1) and the DVPLS flip-flop remains clear. Since the left half of MB is 0 (CCA MBL EQ ZERO true), CCA XFER CW generates CCA LOAD CWAD 1, 2, 3. (The device must insure that bits 0 through 18 are 0 when it transfers the initial control word address control word.) The right half of MB now contains the control word initial address. The CCA LOAD CWAD pulses jam transfers the right half of MB into the CWAD (control word address) register (drawing CCW). Simultaneously, CCA LOAD CW generates CCB CLEAR MB to clear the memory buffer.

Up to this point, a device has requested access to the data channel via CHANNEL START; the data channel has acknowledged CHANNEL START by asserting CHANNEL BUSY, and the device has responded by sending the initial control word address which is now in the CWAD. The next operation is to fetch the control word from memory.

3.3.2   Control Word Fetch

The CCC CWRDRQ (control word read request) flip-flop is set to request a control word read to obtain the initial control word from memory. The CCA LOAD CWAD pulse sets this flip-flop since CCA MBR EQ ZERO and CPG ODD PARITY are both true at this time. (Parity is forced odd by CIA INAD SYNC being false.) CCC CWRDRQ turns on CCC CWRD (control word read). CCC CWRD (1) generates CCC CLCWR (drawing CCC sheet 2) which clears the word count register (drawing WCR) and (2) turns on CCC SYNC the memory cycle sync flip-flop.

Signal CCC SYNC generates CCC REQN which requests access to the multiplexer. The multiplexer responds by generating CBC ACKN. (This signal is generated by a W990 module in the data channel if it is connected directly to the memory bus(see the CBC print). CBC ACKN generates CAD ACKN 1, 2, 3 which turns on the memory address gates to the address bus (drawing CAD). Since CCC CWRD is true, the CWAD (control word address) data is gated to the memory address bus (drawing CAD). Signal CCC CWRD also generates CCC MCRD (memory cycle read) to signal the direction of transfer (drawing CBC) to the PDP-10 memory.

Shortly thereafter, CCC REQ turns on and generates CCC REQ CYC to request a memory cycle. At this time, the CCC REQ PULSE sets the CIA INAD SYNC flip-flop which latches the initial control word address in CIA INAD 27 through 34.

The memory now responds with CBC ADDR ACK (address acknowledge) to acknowledge receipt of address and this generates CCB GTD ADDRACK (gated address acknowledge) which turns on CCC NOREQ. CCC REQ CYC now turns off.

The memory now sends the control word data and signal CBC RDRS. The CCC READ MEM GATE turns on the bus to the memory buffers enabling the control word data to enter the memory buffer. CBC RDRS generates CCA END RD DY (end read delay). The delay allows time for the parity and zero-detection circuits to settle. CCA ENDRDDY generates CCC END MC (end memory cycle) and CCA XFR CW since this is a control word transfer (-CCC RDDW being true). The CCC END MC signal strobes the delayed reset input of CCC CWRD and after a delay, turns off CCC SYNC. The delay insures that DWT, CWRD, and CWWT are all off when SYNC turn off, otherwise SYNC might retrigger.

3.3.3   Control Word Evaluation

For a control word fetch, bad parity is catastrophic. Therefore, CCA LOAD CW with CPG EVEN PARITY turns on CCA IDLE which will terminate the cycle and generate CPG CON PAR ERR.

The newly fetched control word is now examined to determine the ensuing action. If all the word is 0, then a termination is specified. If WC = 0 (i.e., MBL = 0) and DA $\neq$ 0 (i.e., MBR $\neq$ 0), then the DA data is transferred to the CWAD and another control word read is requested. If WC $\neq$ 0 and DA = 0, then the ensuing read cycle will perform all operations of reading the device, however, no data transfer to memory occurs. When WC $\neq$ 0 and DA $\neq$ 0, then the normal data transfer is requested.

When both the WC and the DA portion of the control word are 0, both the CCA MBL EQ ZERO and CCA MBR EQ ZERO signals are true and thus enable CCA LOAD CW to set the IDLE flip-flop to terminate operation.

When the WC portion is 0 (MBL EQ ZERO is true) and the DA portion not 0 (-MBR EQ ZERO is true), the CCA LOAD CWAD 1, 2, and 3 signal is generated and loads MB 18 through 35 into the CWAD (drawing CCW). CCA LOAD CWAD3 then sets CWRDRQ (control word read request) and the next control word is fetched from memory as described previously.

When DA $\neq$ 0, CCA LOAD WCDA (1, 2, and 3) is generated and the content of MB is transferred to the control word register WCR WCT 0 through 17 and CDA 18 through 35. It should be noted that the control word register was cleared when CCC CWRD turned on.

The DA portion determines if the ensuing read cycle is to transfer data to memory. If DA = 0, then CCA SKIP is set to prevent a memory transfer. If DA $\neq$ 0, then CCA SKIP is cleared to permit a normal transfer.

3.3.4   Data Transfer (Read)

Currently, the data channel has been initialized, a control word has been obtained and evaluated. Assuming that the control word specifies a normal transfer (that is WC $\neq$ 0 and DA $\neq$ 0), the read operation continues.

The CCA LOAD WCDA 1 signal triggers a 450 ns delay which, when it times out, generates CCB COUNT ADR1 and 2. (The delay allows time for the data address to settle before stepping it from DA-1 to DA.)

CCB SET VCW turns on CCB VCW (valid control word) which signifies the readiness of the channel to transfer data. CCB VCW (1) then generates CCB COUNT CWAD1 and 2 to increment the control word address register (drawing CCW). The MB has been cleared for sometime, hence it is safe for the device to transmit the first word to the channel. Therefore, VCW turning on, generates CCB INT CHN PLS (the internal channel pulse) which in turn generates CBC CHANNEL PULSE for the device (via drawing CBC).

Upon receiving CBC DEVICE PULSE from the device, the data channel generates CCB DEVPULS which turns on CCB DVPLS (the device pulse flip-flop) and CCB MB FULL. With CCB DVPLS true, CCC DWT (data word transfer) flip-flop turns on, causing CCC SYNC to turn on a short time later. CCC SYNC generates CCC REQN, to request access to the multiplexer. As previously described, signal CBC ACKN (acknowledgement from either the jumper or multiplexer) generates CCC REQ CYCLE. This will start a memory write cycle (CCC MCWR asserted) since CCC WTDW (write data word) is asserted. REQ and NO REQ behave as for control word fetch.

The memory responds with CCB GTD ADDR ACK which now does the following:

a. Turns off CCB DVPLS.

b. Generates CCB COUNT WC 1 and 2 and CCB COUNT ADR 1 and 2 to increment the control word.

c. Generates CCB WRIT MEM STROBE 1 and 2 to fire the data off to memory. CCB WRITE MEM STROBE 1 generates CCC WRRS (the write restart to memory), CCC END MC and after a delay, CCB CLEAR MB which clears the CCB MB FULL flip-flop and the MB.

With CCB MB FULL going off, it generates CCB INT CHN PLS (internal channel pulse) which generates CCC CHANNEL PULSE to complete one cycle.

When CCA SKIP is on, DVPLS will not turn on, thus preventing a memory cycle. However, the control word must still be counted, the channel pulse generated, and the MB cleared. The CCB SKIP PULSE accomplishes all this.

If, when the CCC REQ PULSE is generated (the time when CCC REQ CYC is asserted to memory) the contents of the WC register is all 1's, WCR WCT OVFLO (word count overflow) will be true thus causing CCB VCW to turn off and CCC CWRDRQ to turn on. At the completion of the current

write cycle, the channel will fetch another control word as described previously. Note also that the CCB SKIP PULSE can cause the same action.

3.3.5 Data Transfer (Write)

The initial write cycle is identical to that of read with one exception; CCB DVPLS is turned on by the device pulse that accompanies the initial address. This informs the channel that the device is ready to receive the first data word as soon as the channel has it.

When CCB VCW becomes true, CCC DWT will become true also, since CCB MB FULL is 0 and CCA READ is 0. A memory read cycle will now occur. This time however, CCB GTD ADDR ACK will only count the control word. CCA ENDRDDY will turn on CCB MB FULL and CCB AUX MB FULL. Since CCB DVPLS is on, CCB READ MEM STROBE 1 and 2 is now generated which will:

    a.   Transmit the contents of MB to the device.

    b.   Generate CCB INT CHN PLS which generates CCC CHANNEL PULSE for the device.

    c.   Through a delay, turns off CCB DVPLS.

    d.   Through a delay, generates CCB CLEAR MB which turns off MB FULL and AUX MB FULL.

With MB FULL equal to 0, CCC DWT will turn on, generating another memory cycle and filling the memory buffer. When AUX MB FULL turns on, if the device pulse has not been received, the cycle will stop and not generate CCB READ MEM STROBE and CHANNEL PULSE. The data channel will wait until CCB DVPLS becomes true which will occur when the device is ready for the next word.

If WCR WCT OVFLO is true at CCC REQ PULSE time, CCB VCW will turn off and CCC CWRDRQ will turn on so that when the next memory buffer is emptied, a new control word can be fetched.

If there is a parity error in the data at the time READ MEM STROBE occurs, CPG DATA PAR ER is sent to the device to signal the error.

3.3.6 Write Control Word

The device may request to have the control word written into memory. To accomplish this, it sends the WT CONT WD RQ pulse which generates CBC WRCON WD REQUEST which, if the channel is not IDLE, will turn on CCC CWWT SYNC. The next data transfer which does not call for an immediate control word fetch will turn on CCC CWWTRQ. This will cause CCC CWWT to come on as soon as the memory buffer is clear, and prevent CCB MB FULL from going off. (If READ = 1, this will inhibit CCB INT CHN PLS and the device will not know the MB is empty. If READ = 0 CCC DWT will not turn on to reload MB.) With CCC CWWT on, CCC START CW WRITE triggers, which after a delay, to allow the MB to settle, generates CCC CW to MB 1 and 2. These pulses load the MB, the contents of CCW

CWAD 18 through 35 going into MB 0 through 17 and CDA ADDR 18 through 35 going into MB 18 through 35. CCC SYNC is now turned on to cause a memory cycle.

The address used for this transfer is the initial control word address +1. This was initially stored in INAD 27 through 34, and it is assumed that the initial address transferred was even. (If the initial address sent was odd, this transfer goes into that location.) This is done by forcing memory address bit 35 equal to 1 for this transfer.

START CW WRITE turns off CCC CWWR SYNC and CCC CWWTRQ. Thus, when CCB WRIT MEM STROBE generates CCB CLEAR MB, MB FULL will go off allowing the normal cycle to resume.

CCB GTD ADDR ACK, in addition to generating CCB WRIT MEM STROBE, also generates CCC CONT WRD WRITE COMP to the device.

3.3.7   Cycle Termination

Normal termination occurs when CCA IDLE goes on prior to CCA CYCLE STOP coming on. With IDLE changing state, the device is obliged to remove CBC CHANNEL START which, after a delay, generates CCA CYCLE TERMINATE to turn on CCA CYCLE STOP and CC CWWR SYNC. (The need for the delay which will be explained later, is not necessary here.) With CWWR SYNC and IDLE on, CCC CWWT will turn on. After a delay, CCC START CW WRITE will be generated, which will generate CCB CLEAR MB and after another delay CCC CW TO MB to load MB and turn on SYNC forcing a memory cycle to store information as described in Paragraphs 5.1 through 5.3.

For an abnormal termination, the device removes CBC CHANNEL START prior to the channel going IDLE. This immediately inhibits the inputs to CCC SYNC, and after a delay, turns on CCA CYCLE STOP. (This delay allows SYNC to turn on if the inhibit arrived too late.) With CYCLE STOP on, as soon as the current memory cycle is completed (that is if SYNC was caught on) IDLE will come on. CCA CYCLE TERMINATE, the pulse which turned on CCA CYCLE STOP, has also turned on CCC CWWT SYNC. Thus when IDLE goes on, CCC CWWT will go on also. This causes CCC START CW WRITE to fire after a delay (the delay to allow MB to settle) clearing MB and proceeding as described in Paragraphs 5.1 and 5.3.

3.3.8   Memory Hang-Up

When CCC SYNC turns on, it releases the retriggerable one-shot CCB NONEXMEM. If this one-shot times out, it will generate CCB NO MEM. If SYNC turns off before it times out, the one-shot is caught in the one-state and held until next time.

This circuit presumes that the multiplexor, if used, can always service a channel in 100 μs. If this is not the case, and the multiplexor is servicing higher priority inputs and is not hung-up, it will receive a clear pulse anyway which will cause spurious actions elsewhere.

CHAPTER 4

MAINTENANCE

4.1   GENERAL

The DF10 Data Channel maintenance procedures are grouped into two major catagories; preventive maintenance and corrective maintenance. Preventive maintenance procedures are repeated periodically to ensure system performance is not degrading. Corrective maintenance procedures are performed in the event of equipment malfunctions. For a list of suggested maintenance equipment refer to the PDP-10 Maintenance Manual.

4.2   PREVENTIVE MAINTENANCE

The preventive maintenance procedures forestall possible equipment failures by correcting minor damage and discovering progressive deterioration at an early stage. A log book should be used to record data found during the performance of each preventive maintenance task to indicate the rate of circuit operation deterioration and provide information to determine when components should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks, which include cleaning and visual inspections; checks of specific elements such as the power supplies, and marginal checks which aggravate border-line conditions or intermittent failure. All preventive maintenance tasks should be performed as a function of conditions at the installation site and the downtime limitations of equipment use. Perform the mechanical checks at least once each month or as often as required to allow efficient functioning of the air filters. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. For a typical application, a schedule of every four months or 700 equipment operating hours, whichever occurs first, is suggested.

4.2.1   Mechanical Checks

To check the mechanical operation of the equipment, perform the following steps and indicated corrective action for any substandard conditions found:

a.   Clean the exterior and the interior of the equipment cabinet housing the DF10 Data Channel by using a vacuum cleaner or clean cloths moistened with a nonflammable solvent.

b.   Clean the air filter at the bottom of the cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filters in soapy water, dry in an oven or spray with compressed gas, and spray with Filter-Kote (Research Products Corporation, Madison, Wisconsin) before replacing them in the cabinets.

c.   Lubricate door hinges and casters with a light machine oil, wiping off excessive oil.

d.   Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas with DEC enamel.

e. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

f. Inspect all mounting panels of logic to insure that each module is securely seated in its connector.

g. Verify that all bus cables are firmly seated in their respective connectors.

h. Inspect power supply capacitors for leaks, bulges, or discolorations. Replace any capacitors giving these signs of malfunction.

4.2.2   Power Supply Checks

Check the output voltage and ripple content of the Type 728 and 728A power Supplies and assure that they are within tolerance. Use the multimeter to make the output voltage measurements without disconnecting the load. Use the oscilloscope to measure the peak-to-peak ripple content on dc outputs of the supplies. These supplies are not adjustable; if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be undertaken.

Check the +10V output between the black (-) and the red (+) terminals to assure that it is between 9.5V and 11.0V with less than 800 mV ripple. Check the -15V output between the black (+) and blue (-) terminals to assure that it is between 14.5V and 16.0V with less than 400 mV ripple. Note that the black terminals are common with the power supply chassis.

4.3   CORRECTIVE MAINTENANCE

Corrective maintenance procedures are performed to correct a malfunction within the DF10 Data Channel. Test equipment suggested is a broadband oscilloscope and a standard multimeter. A suggested approach for localizing any fault and method for correcting it is as follows:

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the drum system.

b. System troubleshooting to locate the fault to within a module through the use of signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of a malfunction.

e. Validation test to assure that the fault has been corrected.

f. Log entry to record pertinent data.

4.3.1   Preliminary Investigation

If a fault is evident, the first area to be examined is generally the electrical-mechanical device to which the data channel is associated, however, before proceeding into any detailed trouble-shooting procedure, check for all possible simple faults, such as, cables and modules secured, test jumpers removed, and switches placed in correct position. The programmer should also check the program on which the malfunction occurred. Assure that the power supplies are working properly and that there are no power short circuits by performing the power supply checks as described under Preventive Maintenance.

4.3.2   System Troubleshooting

Troubleshooting the data channel should not be attempted without gathering all information concerning the fault.

Troubleshooting is begun by performing the operation using the same program in which the malfunction was initially observed. The program should be checked for proper control settings, and indicator light operations before, and at the time of the error. Checks should be made to assure that the system is actually at fault before continuing with corrective maintenance procedures. Loose or faulty cable connections often give indications similar to those caused by internal malfunctions. Faulty ground connections between pieces of equipment are a common source of trouble.

If the fault has been determined to be within the data channel, but cannot be localized to a specific logic function, perform the diagnostic program procedure specified for the device used. When the fault has been determined to be a logic element, the defective module or component should be tested by means of signal tracing. If the fault is intermittent, a form of aggravation tests should be employed to locate the source of the fault.

4.3.3   Signal Tracing

If the fault is located within a functional logic element, the PDP-10 can be programmed to repeat an instruction in which all functions of that logic element are utilized. If the test is to be performed without the use of the computer, the control flip-flops or register flip-flops can be cleared or set manually by momentarily supplying a ground potential to the appropriate flip-flop output terminals. Counting operations of registers can be checked by supplying count pulses to the register from the output of a variable clock. Under these conditions, the oscilloscope is used to trace signal flow through the suspected logic element. Oscilloscope sweep may be synchronized with any control signal by connecting the trigger input to the appropriate module terminal on the wiring side (front) of the equipment. Output

signals should be traced from the connector, back to the origin, and input signals from the connector to its final destination. The signal-tracing method can be used to determine the quality of pulse amplitude, duration, rise time, and the correct timing sequence of this signal. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

4.3.4   Intermittent Failures

Intermittent failures caused by poor wiring connections can often be revealed by vibrating the modules while running a repetitive routine, such as the diagnostic program. Moving the handle of a screwdriver across the back of a suspect row of modules is a useful technique. By repeatedly starting the program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After the malfunction is isolated, the seating of the modules in the connector, the module connector for wear and misalignment, and the module wiring for cold solder joints or wiring kinks should be checked.

4.3.5   Module Circuits

Circuit schematics of each module are supplied with the equipment and are contained in the PDP-10 Maintenance Manual, Volume III. The basic functions and specifications for standard modules are presented in the DEC FLIP CHIP Modules Catalog (C-105).

4.3.6   Module List

Drawing A-PL-DF10-0-3 referenced in Chapter 6 lists the modules used in the DF10.
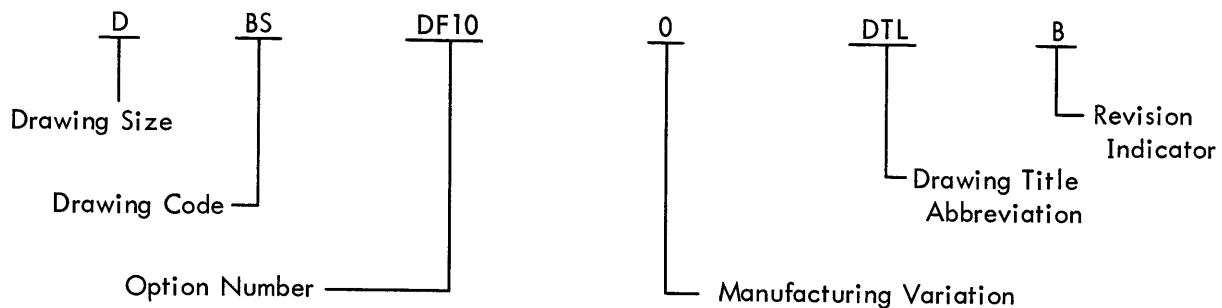
CHAPTER 5
INSTALLATION

The detailed installation information for the DF10 Unit is contained in the PDP-10 Installation Manual.

CHAPTER 6
ENGINEERING DRAWINGS

The engineering drawings for the DF10 Data Channel are contained in Volume III of the PDP-10 Peripheral Device Engineering Drawing Set and are supplied in addition to a complete set of drawings with each system. Should any discrepancy exist between the drawings in Volume III and those supplied with the equipment, assume the latter drawings are correct.

6.1 DRAWING TERMINOLOGY

The engineering drawing number for the DF10 contain six fields of information, separated by hyphens. A typical example of a drawing number is shown below.

```
    D        BS        DF10        0        DTL        B
    |         |          |         |         |         |
Drawing Size  |          |         |         |         └─ Revision
              |          |         |         |             Indicator
Drawing Code ─┘          |         |         └─ Drawing Title
                         |         |              Abbreviation
Option Number ───────────┘         └─ Manufacturing Variation
```
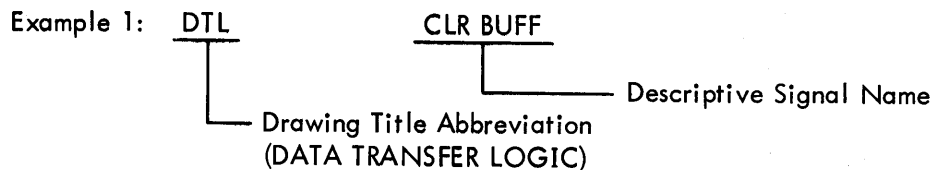
The drawing size, option number, and the drawing title abbreviation are self-explanatory. The manufacturing variation letter identifies the variation that the drawings reflect. For example: 0 reflects drawing applicable to all variations; A reflects the 60 Hz equipment; etc. The drawing code identifies the type of drawing. A list of the common drawing codes follows.

1. BS – Block Schematic or Logic Diagram
2. CL – Cable List
3. CS – Circuit Schematic
4. FD – Flow Diagram
5. IC – Interconnection Drawing
6. KS – Key Sheet
7. MU – Module Utilization
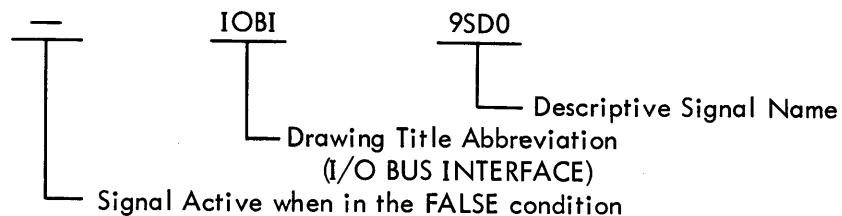8. RS – Replacement Schematic

9. SD – System Diagram

10. PL – Parts List

Signal names on the drawings cross reference the signal to the drawing where the signal originates. Two typical examples of signal names are shown below.

Example 1:   DTL   CLR BUFF

└─── Drawing Title Abbreviation
(DATA TRANSFER LOGIC)

└───── Descriptive Signal Name

Example 2:

─   IOBI   9SDO

└─ Descriptive Signal Name

└─ Drawing Title Abbreviation
(I/O BUS INTERFACE)

└─ Signal Active when in the FALSE condition

6.2   LOGIC SYMBOLS

The DEC standard logic symbols are shown at the input of most circuits to specify enabling condition required to produce a desired output. These symbols represent either standard DEC logic levels or standard DEC pulses.

Typical engineering symbols are shown in Figure 6-1.

6.3   LOGIC LEVELS

All logic signals are either standard DEC logic levels or standard DEC pulses. A standard DEC logic level is either a ground (0 to -0.5V or -3V (-2.5 to -4.0V). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (──◇) indicates that the signal is a level and that ground presents assertion; a solid diamond (──◆) indicates that the signal is a level and that -3V represents assertion.

All logic levels applied to the conditioning-level inputs of capacitor-diode gates must be present either 100 or 400 ns (depending upon the module used) before an input triggering pulse is applied to the gate.

The standard DEC negative pulse is indicated by a solid triangle (──▶) and goes

———————➤	NON-STANDARD SIGNAL
———————▷	POSITIVE PULSE OR LEADING EDGE OF A POSITIVE LEVEL
———————▶	NEGATIVE PULSE OR LEADING EDGE OF A NEGATIVE LEVEL
———————◇	POSITIVE LEVEL
———————◆	NEGATIVE LEVEL
———————◆▷	TRIGGERING ON THE TRAILING EDGE OF A NEGATIVE LEVEL
●——〜〜〜——	−15V LOAD RESISTOR CLAMPED AT −3V

POSITIVE NAND, NEGATIVE NOR DIODE GATE

POSITIVE NOR, NEGATIVE NAND DIODE GATE

CAPACITOR − DIODE GATE, POSITIVE OR NEGATIVE INDICATED BY POLARITY OF THE INPUTS.

1. PULSE INPUT
2. CONDITIONING LEVEL INPUT
3. PULSE OUTPUT

FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING.)

1. DIRECT-CLEAR INPUT
2. GATED-CLEAR INPUT
3. DIRECT-SET INPUT
4. GATED-SET INPUT
5. OUTPUT LEVEL, −3V IF 0, OV IF 1
6. OUTPUT

DELAY (ONE SHOT MULTIVIBRATOR)

1. CONDITIONING LEVEL INPUT
2. PULSE INPUT
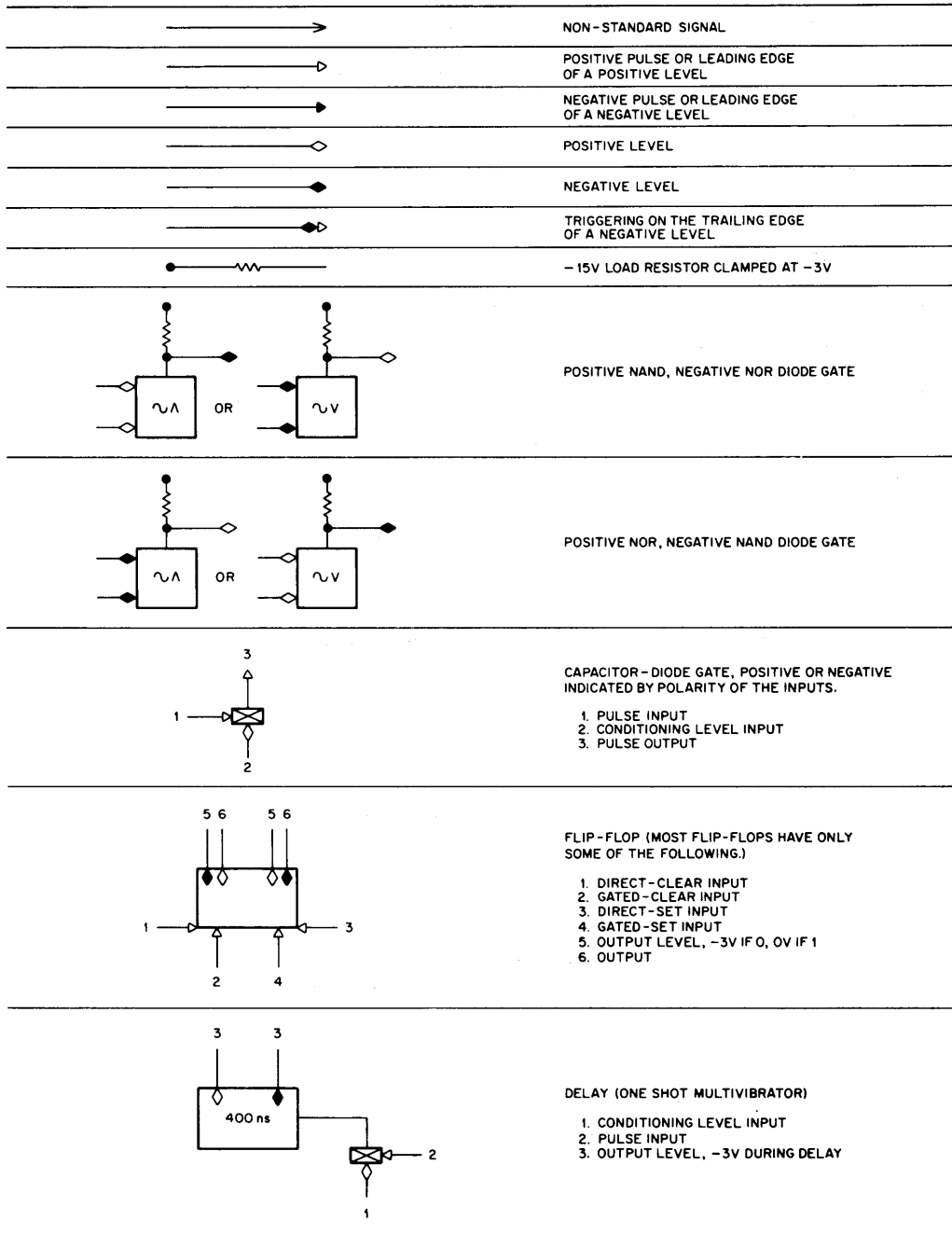3. OUTPUT LEVEL, −3V DURING DELAY

400 ns

Figure 6-1   DEC Standard Logic Symbols

6-3

from ground (0 to -0.5) to -3V (-2.5 to -4.0V). The standard DEC positive pulse, indicated by an open triangle (———▷), goes from -3V to ground. The width of the standard pulses used in this equipment is either 100 or 400 ns, depending upon the module and application.

Occasionally, the trailing edge transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (———◆▷) is drawn to indicate this fact. The triangle is drawn solid if the negative (ground to -3V) transition triggers circuit action. The shading of the diamond is opposite that of the triangle to indicate triggering on the trailing edge.

Any other signal is nonstandard and is indicated by an arrowhead(———▷) pointing in the direction of signal flow.

6.4   FLIP-CHIP PULSES

FLIP-CHIP circuit operation in the DF10 uses the DEC R-, S-, and B-series pulses. The pulse produced by the R-series or S-series modules start at -3V, goes to ground (-0.2V) for 100 or 400 ns, then returns to -3V. The rise time of the leading edge from 10% to 90% should be less than 60 ns. An idealized pulse is shown in Figure 6-2.
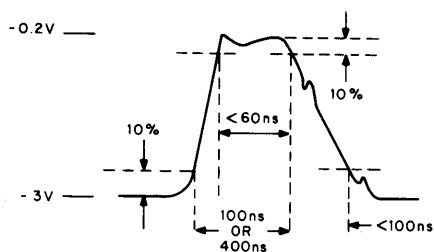

Figure 6-2 R-Series and S-Series Pulses

The B-series pulse starts at 0V, goes to -3V and returns to 0V. The pulse width must be between 30 and 40 ns at the -1V level and greater than 15 ns at the -2V level. Glitches on the bottom of the pulse should not be more positive than -2.5V, overshot should not exceed +4.0V, and no ring should be below -0.5V. The B-series pulse is idealized in Figure 6-3.
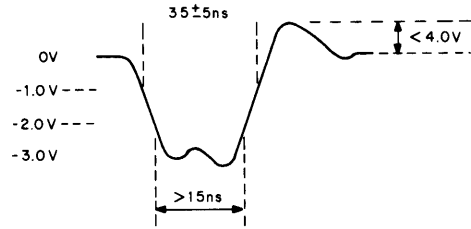
Figure 6-3 B-Series Pulse

6.5   ENGINEERING DRAWING LIST

The engineering drawings that are supplied with the DF10 will be found in Volume IV of the PDP-10 Peripheral Engineering Set.

Drawing Number	Rev.	Title
D-MU-DF10-0-3	B	Module Utilization
A-PL-DF10-03	B	Module Utilization
D-BS-DF10-0-CAD		Address Drivers Cad
D-BS-DF10-0-CBC		Channel Bus Conn's and Terms
D-BS-DF10-0-CBL		Data Display Connectors
D-BS-DF10-0-CCA		Data Channel Control A
D-BS-DF10-0-CCB	A	Data Channel Control B
D-BS-DF10-0-CCC	A	Data Channel Control C
D-BS-DF10-0-CCW		Control Word Address Register (CCW)
D-BS-DF10-0-CDA		Data Address Register
D-BS-DF10-0-CIA		Initial Address Register
D-BS-DF10-0-CPG	A	Data Chan Par Gen
D-BS-DF10-0-MBL	A	Memory Buffer 0-17
D-BS-DF10-0-MBR	A	Memory Buffer 18-35
D-BS-DF10-0-WCR		Word Count Register
D-BS-DF10-0-TERM		Signal Terminations
D-FD-DF10-0-00A	B	Flow Chart A
D-FD-DF10-0-00B	A	Flow Chart B Memory Cycle
D-FD-DF10-0-00C	A	Flow Chart C
A-WL-DF10-0-5		DF10 Channel Twisted Pair
A-CP-DF10-0-6	A	DF10 Channel
D-IC-DF10-0-4		Wiring Power Dc and Ac

digital