Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-10
Maintenance Manual

DK10
REAL TIME CLOCK

DEC-10-HDKB-D

decsystem10

DK10 REAL TIME CLOCK MAINTENANCE MANUAL

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CHAPTER 1
GENERAL DESCRIPTION

1.1 GENERAL DESCRIPTION

The DK10 Real Time Clock is a DECsystem-10 option designed to provide the user with an accurate time measurement in either the Executive mode or the User mode. It is a combination interval timer, Non-PI in-progress timer, and a time-of-day clock. It contains an internal 100-kHZ ±0.01% crystal clock with provisions for utilizing an external clock of up to 400 kHZ. Of general interest here is the fact that an error of 0.01% amounts to 8.64 seconds in 24 hours.

1.2 PERFORMANCE SPECIFICATIONS

The DK10 has a frequency counter which counts the pulses of an internal 100-kHZ ±0.01% clock, or an external clock having a maximum frequency of 400 kHZ. It also incorporates a comparator network, to indicate a comparison between the clock register (frequency counter) and the interval register. When using the internal clock source, the interval register may be set to any integral number of 10 μs, up to a maximum of approximately 2.6s. At the time of equal comparison, a program interrupt is generated and the frequency counter is reset to start timing the next interval. The clock is synchronized to the DATAI instructions so that it may be read by the PDP-10, at any time, without missing a clock pulse. The Real Time Clock can be used to time either Real Time Executive mode functions or User mode functions. Therefore, it is necessary to have two device codes available for those applications that incorporate two DK10's for timing both modes of operation. Device code 070_8 has been assigned to the first DK10. Device code 074_8 has been assigned to the second DK10. The DK10 Real Time Clock has a standard PDP-10 I/O Bus interface used as the communications media between it and the PDP-10.

1.3 ENVIRONMENTAL SPECIFICATIONS

Operating Ambient
Temperature = 60° - 95°F (15° - 35°C)

Relative Humidity = 20% - 80%
Storage Temperature = 40° - 110°F (5° - 45°C)

1.4 POWER SPECIFICATIONS

+10 Vdc @ 0.5A
-15 Vdc @ 5.0A

Power dissipation = 75W
Heat dissipation = 250 BTU/Hr

Dc voltages are provided by the TD10 Power Supplies. If a second DK10 is installed, an additional power supply must be mounted, in parallel, with the TD10 Power Supplies.

1.5 EXTERNAL CLOCK SPECIFICATIONS

Pulses:

Width = 100 ns min
Level = -3V to gnd
Frequency = 400 kHZ max

Level Changes:

Level change = -3V to gnd at a maximum of 400 kHZ
Rise time = 60 ns min
Duration = 40 ns min
Input must be at -3V for a minimum of 400 ns before positive change

The external clock transmission cable must be a 100-ohm coaxial cable with a BNC connector to mate to the DK10.

1.6 MECHANICAL PACKAGING (Refer to Figure 1-1)

The DK10 is contained within two 1943 mounting panels. The upper panel contains a small Indicator/Control panel.

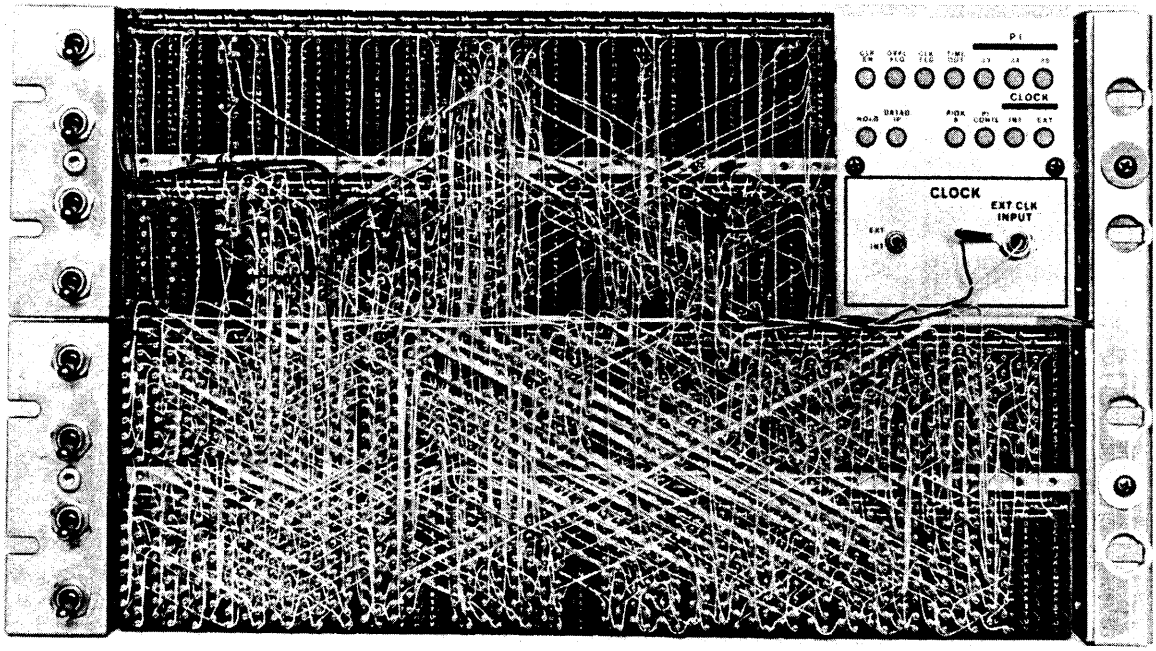


Figure 1-1 DK10 Real Time Clock

CHAPTER 2

THEORY OF OPERATION

2.1 GENERAL THEORY

The DK10 Real-Time Clock is an accurate, high-speed timer. It contains a frequency counter (clock register), an interval register, and a comparator network, as well as associated control logic for all three.

The frequency counter (clock register) counts the pulses of an internal 100-kHZ ±0.01% crystal clock or an external clock having a maximum frequency of 400 kHZ. The comparator network continually monitors the contents of the clock register and the interval register. An interrupt is generated, by the DK10, each time an equal comparison is detected.

The DK10 has four modes of operation. Three of these modes are operating modes and the remaining mode is a diagnostic mode. The modes are as follows:

a. Interval Clock - In this mode, the user is capable of counting up blocks of time (intervals). At the end of each interval, the DK10 generates an interrupt request to the PDP-10.

b. Time-of-Day Clock - The Time-of-Day Clock is actually a software clock, not a hardware clock. Each time the PDP-10 is interrupted, the content of the interval register is added to an initially cleared memory location. When the actual time of day is required, the contents of the initially cleared memory location must be read into a temporary memory location. The contents of the DK10 Clock Register must then be added to the contents of the temporary location. The sum of this location, multiplied by the time duration between clock pulses, represents the actual time of day.

c. Non-PI In Progress Timer - In this mode of operation, the clock pulses, in the DK10, are enabled only while the PDP-10 is not servicing an interrupt and has no request for an interrupt. Thus, the total time spent in other than PI In Progress time, can be accumulated.

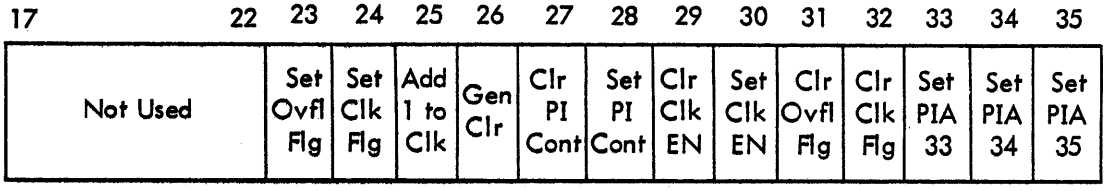
d. Diagnostic Mode - This mode of operation allows diagnostic checkout of the DK10 and the PDP-10 I/O Bus.

2.2 PDP-10 INSTRUCTIONS

PDP-10 Instruction Bit Assignments are illustrated in Figure 2-1.

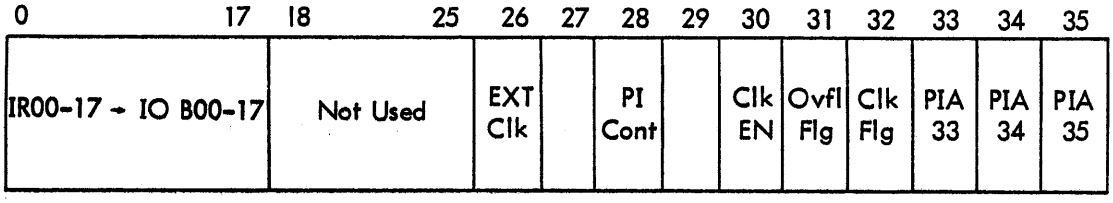
CONO:

Instruction Bits



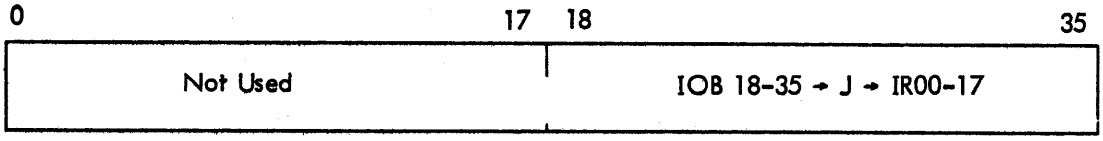
CONI:

Status Word



DATAO:

Data Word



DATAI:

Data Word

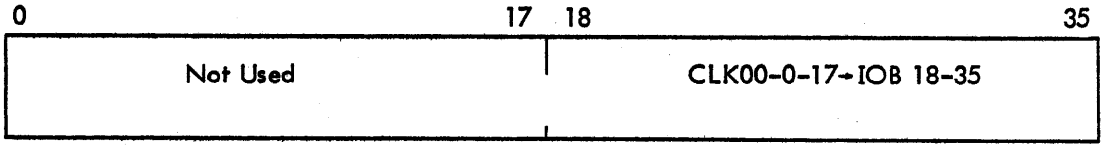


Figure 2-1 PDP-10 Instruction Bit Assignments

The CONO instruction bits have the following significance:

Bit 23	Sets the IOC OVFL flag.
Bit 24	Sets the IOC CLOCK flag.
Bit 25	If the CLOCK ENABLE flip-flop is off, the clock register is incremented by a count of one. (Used for diagnostic programming.)
Bit 26	Clears the control registers and the clock register.
Bit 27	Clears the PI CONTROL flip-flop.

Bit 28	Sets the PI CONTROL flip-flop. This enables the DK10 to count clock pulses only when the PDP-10 is not servicing an interrupt and has no request for an interrupt. (Clock Enable must be set.)
Bit 29	Clears the CLOCK ENABLE flip-flop which disables the DK10 Clock.
Bit 30	Sets the CLOCK ENABLE flip-flop which enables the DK10 Clock.
Bit 31	Clears the IOC OVFL flag.
Bit 32	Clears the IOC CLOCK flag.
Bits 33-35	Set up the priority interrupt level at which the DK10 will interrupt the PDP-10.

The CONI status word bits have the following significance:

Bits 0-17	Contain the contents of the interval register.
Bit 26	When true, indicates the DK10 is using an external clock source. When false, indicates the DK10 is using its internal clock source.
Bit 28	Indicates the DK10 is being used as a Non-PI In Progress Timer.
Bit 30	Indicates that the DK10 Clock is enabled.
Bit 31	Indicates that the clock register has overflowed.
Bit 32	Indicates that the contents of the clock register and the interval register are equal.
Bits 33-35	Indicate the priority interrupt level assignment of the DK10.

The DATAO data word bits have the following significance:

Bits 0-17	Not used.
Bits 18-35	Contain the number to be loaded into the DK10 Interval Register.

The DATAI data word bits have the following significance:

Bits 0-17	Not used.
Bits 18-35	Contain the contents of the clock register within the DK10.

2.3 I/O BUS GLOSSARY

The PDP-10 I/O Bus serves as the communications link between the DK10 and the PDP-10 processor. The following signals are transmitted over the I/O Bus:

IOB 00-35	a. Bi-directional data word transfers. b. Transfer control information to the DK10. c. Transfer DK10 status information to the PDP-10.
IOB Reset	Initializes all I/O devices.

IOS 3-9	Used to select the I/O device.
IOB PI 01-07	Seven levels at which the I/O device may interrupt the PDP-10.
IOB RDI PULSE	Not used in the DK10.
IOB RDI DATA	Not used in the DK10.
IOB CONO CLR	During a CONO instruction, this pulse clears all the specified control registers within the DK10.
IOB CONO SET	During a CONO instruction, this pulse gates the information on the I/O Bus into the DK10 control registers.
IOB DATAO CLR	During a DATAO instruction, this pulse is used to synchronize the DK10 to the DATAO instruction.
IOB DATAO SET	During a DATAO instruction, this pulse gates the information on the I/O Bus into the DK10 interval register.
IOB DATAI	During a DATAI instruction, this pulse gates the contents of the DK10 clock register onto the I/O Bus to the PDP-10.
IOB CONI	During a CONI instruction, this pulse gates the contents of the DK10 control registers (as well as the interval register) onto the I/O Bus to the PDP-10.
IOB DR SPLIT	Not used in the DK10.

2.4 INDICATOR/CONTROL PANEL

The Indicator/Control Panel is mounted in module locations AB25-32 (see Figure 2-2). The panel contains 13 indicators, one switch, and one BNC connector. Their functions are described in Table 2-1.

Table 2-1
Indicator/Control Panel Functions

Mnemonic	Function
CLK EN	Indicates that the DK10 clock register is enabled to count clock pulses.
OVFL FLAG	Indicates that the DK10 clock register has overflowed and has started counting up again. This flag interrupts the PDP-10 to inform it that the comparator in the DK10 failed or that the DK10 and the program are out of synchronization.
CLK FLG	Indicates the clock counter has reached the specified interval.
TIME OUT	Indicates the contents of the interval register and the clock counter are identical. This light goes out as soon as either changes state.
PI 33, 34, 35	Indicate the priority level assignment of the DK10.
HOLD	Indicates that the PDP-10 is reading the contents of the DK10 clock register.
DATAO IP	Indicates the PDP-10 is transferring information into the DK10 interval register.

Table 2-1 (Cont)
Indicator/Control Panel Functions

Mnemonic	Function
PIOK8	Indicates that the PDP-10 is not servicing an interrupt and has no interrupt request present.
PI CONTL	Indicates the DK10 is being used as a Non-PI In Progress timer.
CLOCK INT	Indicates the DK10 is using its internal clock source.
CLOCK EXT	Indicates the DK10 is using an external clock source.
INT/EXT (switch)	Used to select the clock source.
BNC Connector	Used to input the external clock source.

2.5 DETAILED THEORY

To operate the DK10 as an interval timer, the PDP-10 must accomplish the following:

a. Set up the interval register via a DATAO instruction.

b. Set the priority interrupt registers (PI 33-35) to the desired priority interrupt level via a CONO instruction.

c. Set the CLOCK ENABLE flip-flop via the same CONO instruction.

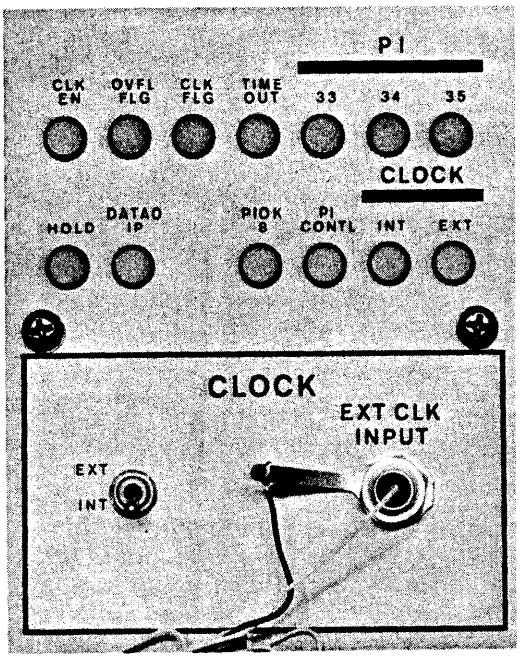


Figure 2-2 Indicator/Control Panel

Refer to the DK10 Engineering Drawings (Paragraph 4.2). Once the CLOCK ENABLE flip-flop is set, a series of TIC CLK1 pulses are generated. The frequency of the TIC CLK1 pulses is identical to that of the selected clock source. A TIC CLK2 pulse is generated on the trailing edge of each TIC CLK1 pulse. TIC CLK2, in turn, is ANDed with TIC HOLD (0) to produce TIC COUNT PLS A and TIC COUNT PLS B. The clock register (CLK00-17) is incremented by one each time these pulses occur. In addition, TIC COUNT PLS A triggers the TIC COUNT DLY multivibrator, which is set for 400 ns to allow the clock register to settle down prior to sampling the output of the comparator.

The trailing edge of TIC COUNT DLY generates TIC SAMPLE PLS. The comparator network, meanwhile, monitors the contents of the interval register (IR00-17) and the clock register (CLK00-17). When they are equal, TOC TIME OUT is true. TIC SAMPLE PLS is now gated with TOC TIME OUT. If TOC TIME OUT is false, the TIC SAMPLE PLS is ignored and the clock register continues to count clock pulses. Conversely, if TOC TIME OUT is true, the Clock FLG is set, the clock register is cleared, and the DK10 generates a priority interrupt on the assigned level to the PDP-10.

The comparison interrupt is disabled during a DATAO instruction (as the interval register is changing). This is accomplished via the TIC DATAO IP flip-flop. Assume a DATAO instruction is issued. When IOC DATAO CLR is generated, TIC DATAO IP is set. TIC DATAO IP (1) inhibits TIC SAMPLE PLS (which is necessary to set the CLOCK FLG and generate an interrupt). IOC DATAO SET occurs 1 μs after IOC DATAO CLR. This clears TIC DATAO IP. TIC SAMPLE PLS can now be generated to cause an interrupt whenever the Clock Register is equal to the new setting of the interval register.

The DK10 must be synchronized to a DATAI instruction to prevent the loss of a clock pulse which may occur during a DATAI instruction. This is accomplished by delaying the clock pulse until after the DATAI instruction is completed. During a DATAI instruction IOC DATAI is true. When TIC CLK 1 occurs, TIC HOLD is set. On the trailing edge of TIC CLK1, TIC CLK2 is generated. However, TIC COUNT PLS A and TIC COUNT PLS B are not generated because TIC HOLD is set. TIC CLK2 triggers a 2.0 μs multivibrator TIC HOLD CLK. The PDP-10 reads the contents of the Clock Register during the 2.0 μs. On the trailing edge of TIC HOLD CLK, TIC CLK3 is generated. TIC CLK3 generates TIC COUNT PLS A and TIC COUNT PLS B which increment the clock register.

The output of the comparator is sampled 400 ns later by TIC SAMPLE PLS. If the clock register and the interval register are equal, the CLOCK FLG is set causing an interrupt to the PDP-10 on the assigned level.

2.5.1 Time of Day Feature

To use the DK10 as a Time-of-Day clock, the DK10 is set up to run as an interval timer. At the end of each interval of time (determined by the contents of the interval register), the DK10 transmits an interrupt request to the PDP-10. As the PDP-10 receives each interrupt request, it adds the number which was stored in the DK10 interval register to a time-of-day core location which was initially cleared. The number may be obtained by reading in the contents of the DK10 interval register with a CONI instruction or by reading it from core. The total accumulated sum of this location, multiplied by the time duration between clock pulses, is the time of day after the time-of-day core location was cleared.

To obtain the time of day between interrupts, the contents of the time-of-day core location must first be transferred into a temporary core location. Next, a DATAI instruction is issued to read the contents of the DK10 clock

register, which is then added to the contents of the temporary core location. The resultant sum may be used to calculate the present time of day (taking the current clock frequency into consideration).

If, at any time, the frequency of the external clock source is changed, via the program, (assume the DK10 is using an external clock) the contents of the time-of-day core location must be modified at that time to concide with the new clock frequency.

2.5.2 Operation as a Non-PI In Progress Timer

Upon setting the PI CONTROL and CLOCK ENABLE flip-flops in the DK10, the clock register will increment only while the PIOK8 level from the PDP-10 is true. This mode allows the user to accumulate the total time spent in other than PI In Progress time. The PIOK8 level is generated by a modification to the PDP-10. It signifies that the PDP-10 is not servicing any interrupts and has no interrupt requests.

2.5.3 Diagnostic Feature

The operation of the DK10 and the PDP-10 I/O Bus connections may be tested by using the diagnostic feature of the DK10. This is accomplished by clearing the CLOCK ENABLE flip-flop in the DK10. The program may then issue a CONO instruction, with bit 25 on a 1, each time it wishes to increment the DK10 Clock Register.

2.5.4 Power Loss Protection

If for any reason, power is removed from the DK10 power source, the 844 Power Control causes TIC CROBAR to go to ground. (Refer to the DK10 prints.) This level triggers the Power On multivibrator for 150 ms which generates TIC GEN CLR and IOC PI CLR. These pulses clear all the registers within the DK10. TIC CROBAR inhibits the DK10 from responding to a DATAI or CONI instruction and inhibits the DK10 from generating a Priority Interrupt request by holding PI33-35 cleared. The preceding action prevents the PDP-10 program from receiving false information from the DK10 upon loss of power.

CHAPTER 3

INSTALLATION AND MAINTENANCE

3.1 INSTALLATION

3.1.1 Inspection

Upon receipt inspect the equipment for visible signs of damage in transit, such as dents, and abrasions. Inspect the logic modules for foreign matter which may have become lodged in them during shipment. Any damage observed should be reported immediately to both the carrier and Digital Equipment Corporation. Check the contents of each carton with the items listed on the shipping document and report any omissions or incorrect parts immediately to Digital Equipment Corporation. Installation is not recommended until all materials are in hand.

3.1.2 Installation Procedure

a. Turn off system power.

b. Install the DK10 in place of a TU55 DECtape unit directly above the TD10 logic, if there are four or less TU55's in the system. Otherwise install the DK10 in the lower half of the TD10B expander cabinet along with its cooling fans.

c. Connect the +10Vdc, -15Vdc, and ground terminals from the TD10 Power Supplies to the DK10 power in tabs. Connect the marginal check voltages. Also, connect the CROBAR line to the DK10.

d. Connect ac power to the cooling fans, if required.

e. Insure that all the margin check switches are in the OFF (down) position.

f. Connect the DK10 to the PDP-10 I/O Bus as follows:

(1) Insert I/O Bus cable 1 IN and OUT into module locations CD 1, 2, and CD 5, 6 respectively.

(2) Insert I/O Bus cable 2 IN and OUT into module locations CD 3, 4, and CD 7, 8 respectively.

g. Connect the PIOK8 level from PDP-10.

h. Turn on system power.

i. Run the DK10 diagnostic programs (MAINDEC-10-DCDKA) to insure proper operation.

3.2 DK10 ADJUSTMENTS

a. Switch the clock source to EXT CLK, but do not connect an external clock to the DK10. Disconnect

the I/O Bus connections to the DK10. Install a jumper between B11H and B11C to disable the I/O Reset line. Sync negative and monitor PWR ON (A04D). Turn power on and check for a 150 ms, -3V level. To set the output for 150 ms, turn the power on and off and adjust the trim pot on the R303 in A04. After 150 ms, TIC GEN CLR (B17K) should be produced. The combination of PWR ON and TIC GEN CLR will clear all the flip-flops, except the interval register, within the DK10. Remove the jumper between pins B11H and B11G.

b. Install a jumper between B01D and B01C. Install another jumper between B10N and B10C. Leave these jumpers in place until told to remove them. Turn on the dc power. The only indicator that should be illuminated is CLOCK EXT. Set IOC PI CONTL and IOC CLK EN by momentarily connecting pins A12H and A12S to ground. The indicators for these flip-flops should become illuminated as they are set. When both are set, the PI0K8 indicator should illuminate.

c. Switch the clock source to INT clock on the Indicator/Control panel. The CLOCK EXT indicator should go off and the CLOCK INT indicator should come on. Sync (-) the scope on the internal clock (A23D). Monitor TIC CLK 1 (B19K). There should be a 400 ns pulse every 10 μs. If a pulse is not present, trace back through the logic to locate the problem. The CLK FLG and the OVFL FLG may come on, at some point, indicating that the DK10 is functioning properly further along the timing chain.

d. Monitor TIC CLK 1 (B19K) and TIC CLK 2 (B18F). TIC CLK 2 should be a 100 ns pulse occuring on the trailing edge of each TIC CLK 1 pulse. (Move the probe from TIC CLK 1 (B19K) and check that a TIC CONT PLS A (B19U) and a TIC COUNT PLS B (B17U) are generated at each TIC CLK 2 time. They should be 100 ns wide.)

e. Sync the scope positive on TIC CLK 2 (B18F). Monitor TIC COUNT DLY (A18V). Adjust the lower trim pot in A18 for a 400 ns, -3V level output. (Remove the probe from A18V and monitor TIC SAMPLE PLS (B18T). A 100 ns pulse should be generated at the end of the 400 ns.)

f. Monitor TIC CLK 2 (B18F) and TIC HOLD CLK (A18M). Adjust the upper trim pot on A18 for 2.0 μs, -3V level. Verify that there are no TIC CLK 3 pulses present at B18M.

g. Remove the jumper between B10N and B10C. The HOLD indicator should come on. Monitor TIC CLK 2 (B18F) and TIC CLK 3 (B18M). A 100 ns TIC CLK 3 pulse should occur 2.0 μs after each TIC CLK 2 pulse. A TIC COUNT PLS A (B19U) and a TIC COUNT PLS B (B17U) should be generated at the same time TIC CLK 3 is generated.

h. Remove the jumper between B01D and B01C. All clock pulses should cease. Clear the IOC PI CONTL flip-flop by momentarily grounding A12J. The clock pulses should start again.

i. Monitor the outputs of the clock register (refer to drawing DK10-0-IR) to insure that they are incrementing at a 10 μs rate.

j. Turn power off and remove any jumpers that were left connected in the previous steps. Reconnect the I/O Bus. Turn power back on.

3.3 MARGIN CHECK SPECIFICATIONS

	+10 VOLT RANGE		-15 VOLT RANGE	
RACK	LOW	HIGH	LOW	HIGH
1A	2.5	17.5	-12	-18
1B	2.5	17.5	-12	-18
1C	2.5	17.5	-12	-18
1D	2.5	17.5	-12	-18

CHAPTER 4
ENGINEERING DRAWINGS

4.1 INTRODUCTION TO DEC LOGIC

Logic schematics (called block schematics at DEC) are usually drawn with DEC pre-MIL-STD-806B logic symbols. Except for shape representation, these logic symbols conform to MIL-STD-806B, with additional features added for clarity. Both of these logic symbol standards are discussed below.

The most striking feature of DEC logic (and most puzzling to those not accustomed to it) is that a logic signal may be true (logical 1) either when it is high or when it is low, depending on the logic designer's preference. In any given logic network, signals which are high-when-true and signals which are low-when-true will ordinarily exist. Not infrequently, the same logic signal will have two electrical representations, one high-when-true and the other low-when-true. In addition, the logic designer has the freedom of using the logic negation of a signal. This usage is indicated by a not sign (~), and over bar ($\overline{XXXX}$), or by a minus sign preceding the signal name (Figure 4-1). Whether a signal is true-when-high or true-when-low is indicated by the type of diamond or arrow (open or solid) in DEC logic symbols or by the presence or absence of a small circle in MIL-STD-806B logic. This convention permits logic design without regard to the inversion properties of most DEC logic. It also permits assignment of logic packages to the realization of the design without requiring undue redesign to account for gate inversions.

Frequently, in larger logic networks, it is convenient to show a named signal's source without a connection to its load which is located elsewhere (Figure 4-2). To facilitate this, a small circle may be drawn at the end of the source line when using MIL-STD-806 logic symbols in order to show that the signal is true-when-low.

In DEC logic symbols, wired ANDs and wired ORs are not explicitly marked (Figure 4-3 and 4-4); they must be recognized. Due to the electrical properties of DEC's below ground logic (ground and -3V logic levels), a wired OR will usually occur at ground (high) and a wired AND at -3V (low).

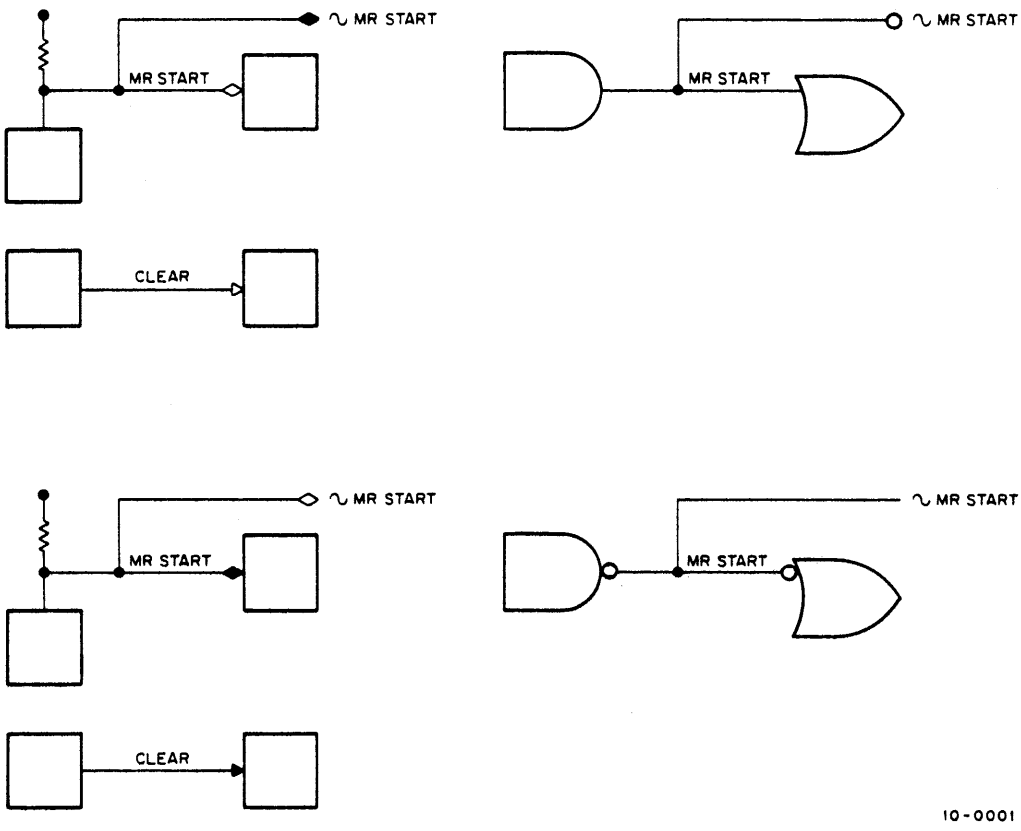


Figure 4-1 Digital Logic Signals

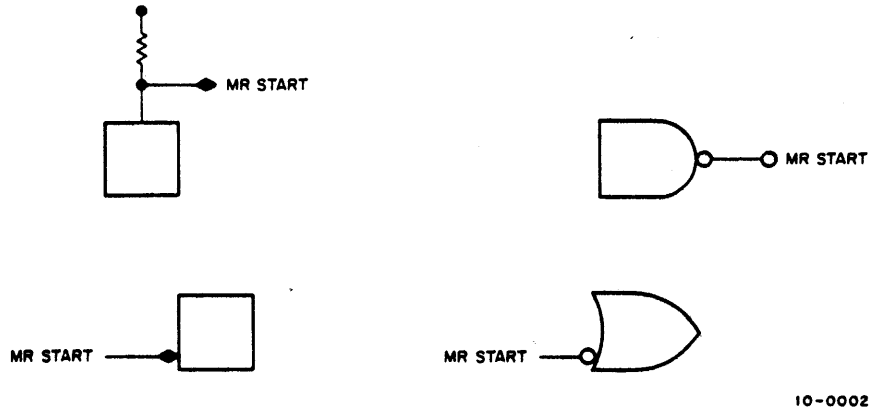


Figure 4-2 Sources and Loads Shown Without Connections

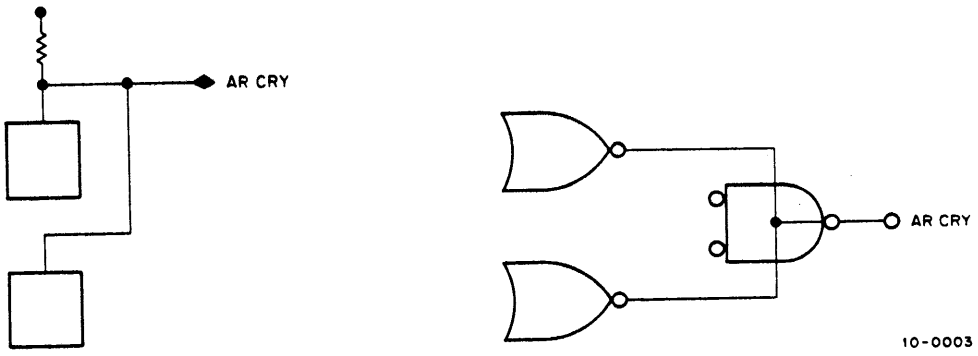


Figure 4-3 Wired AND

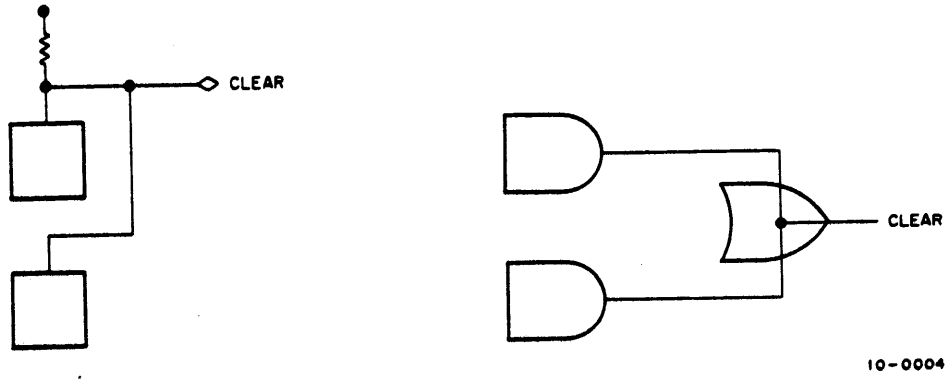


Figure 4-4 Wired OR

In DEC logic, most flip-flops are drawn with four outputs: one which is high when the flip-flop is in the 1 state, one which is low when the flip-flop is in the 1 state, one which is high when the flip-flop is in the 0 state, and one which is low when the flip-flop is in the 0 state. This convention allows the condition "the flip-flop is in the 1 (0) state" to be used with gates that require either high or low inputs without manipulating highs, lows, 1s and 0s. Although a flip-flop has four logical outputs, as noted above, it has only two electrical output connections, as the 1-high and 0-low connections are electrically equivalent (same output pin), as are the 1-low and 0-high connections. Except when the lines are quite short, connections to flip-flop outputs are not usually shown explicitly (Figure 4-5).

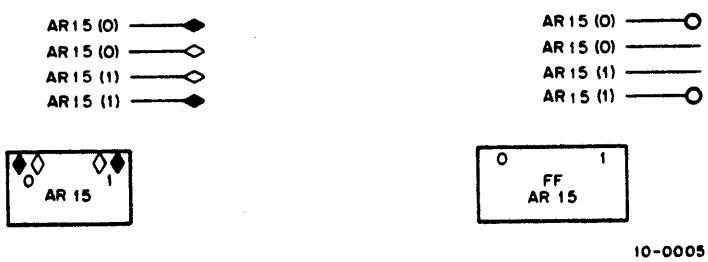


Figure 4-5 Flip-Flop Representation

In MIL-STD-806B logic drawings, DEC shows only the 1-high and 0-high output of a flip-flop, although all outputs are considered present for the purpose of logic design.

Mention should be made of the DEC diode-capacitor-diode (DCD) gate which is both an AND gate and a logic delay (Figure 4-6). This gate allows the output of a flip-flop to be sampled (with a DCD gate) at the same time the flip-flops state is changed. The flip-flop state seen by the DCD gate is the state prior to the change. The DCD gate generates an output pulse when the "level" input has been true (high) for approximately 400 ns and the "pulse" input has a 100 ns positive pulse or a positive-going (ground-going) level change with a rise time of less than 600 ns applied to it.

It is recommended that the DEC rectangular symbol for the DCD gate be used, either with the older DEC logic symbols or with the MIL-STD-806B logic symbols, in order to distinguish the quite different properties of the two inputs and to indicate the logic delay properties of the DCD gate. DEC logic symbols are all rectangular in shape. The function of the symbol is indicated by a descriptive notation within the rectangle. Examples of the more common symbols are shown in Figure 4-7 through 4-15.

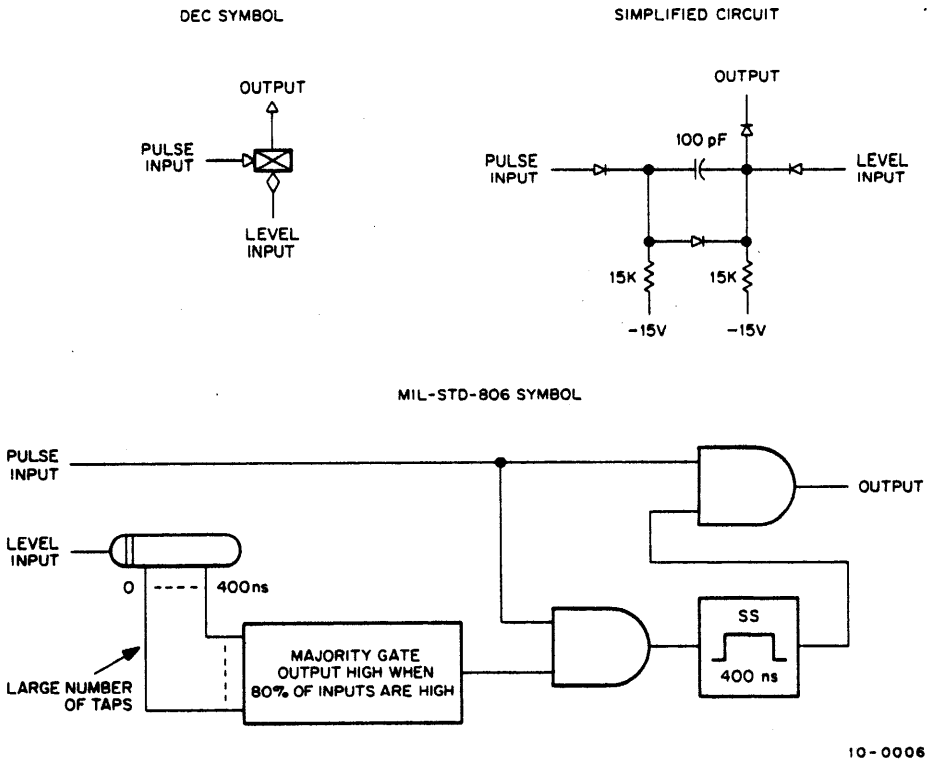


Figure 4-6 DCD Gate

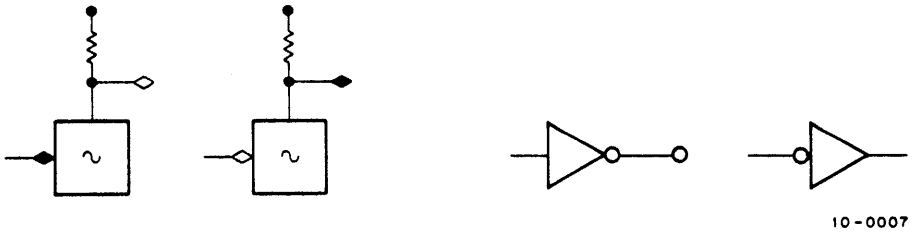


Figure 4-7 Inverter (NOT Gate)

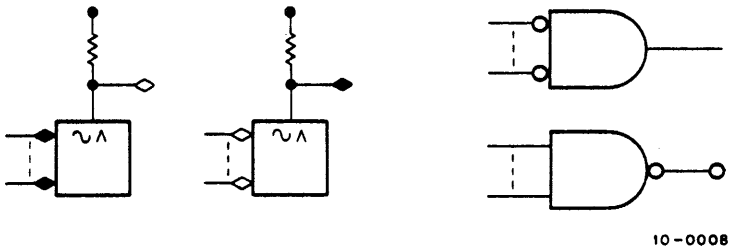


Figure 4-8 AND Gate

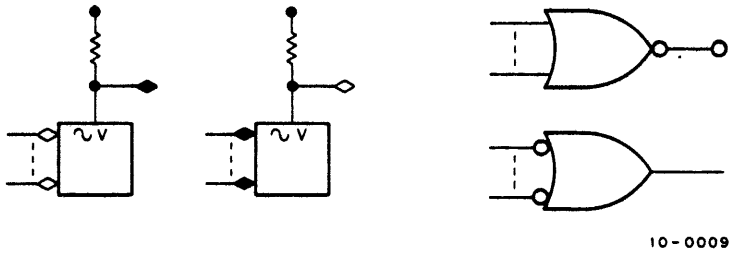


Figure 4-9 OR Gate

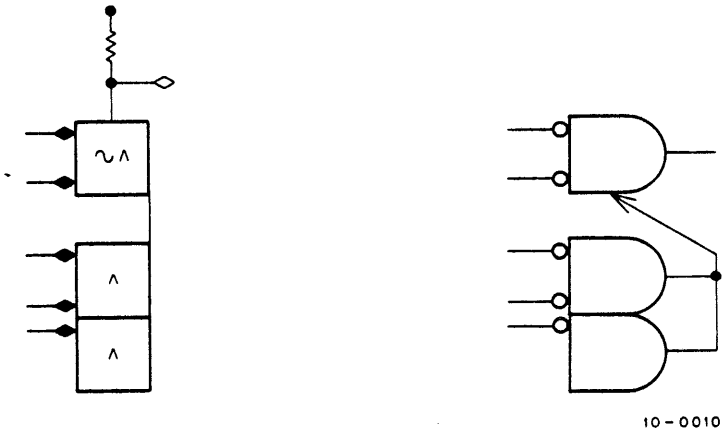


Figure 4-10 Expanded Gate

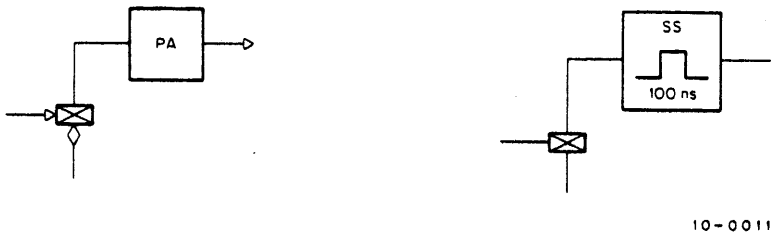


Figure 4-11 Pulse Amplifier

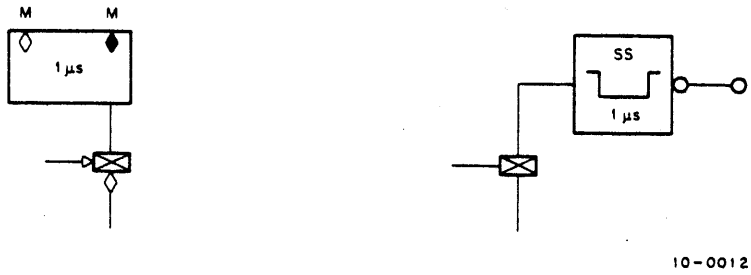


Figure 4-12 Monostable Multivibrator (Single Shot)

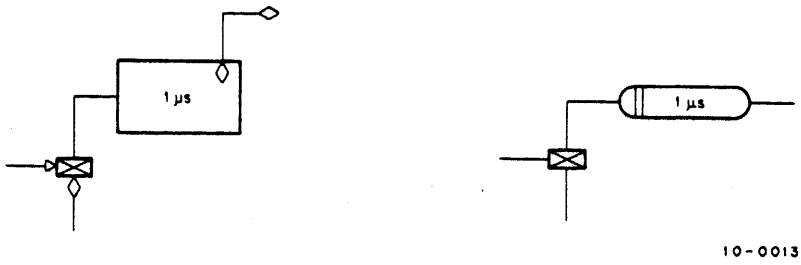


Figure 4-13 Monostable Multivibrator (Delay)

Figure 4-14 Delay

Figure 4-15 Clamped Load

DEC makes use of the electrical equivalence of various logic configurations. As an aid to understanding, symbols are drawn to represent the logic function intended by the designer rather than as a single standard symbol for each module type. Thus, a particular module type may appear as several different symbols. (See Figure 4-16.)

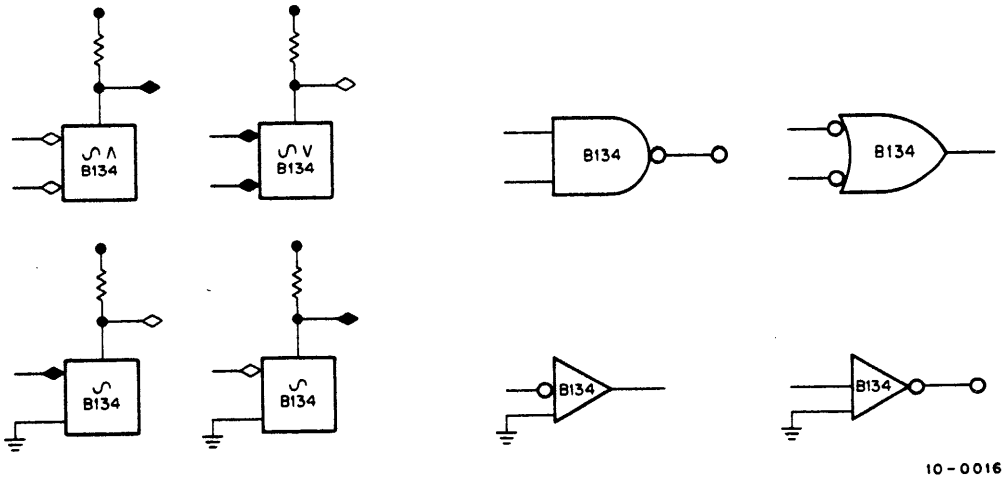


Figure 4-16 Different Uses of a Particular Module

Occasionally, the trailing edge of a signal will be used to cause some action, usually by triggering a DCD gate. This usage is illustrated in Figure 4-17. For additional details on the types of logic modules available, see the DEC Logic Handbook (C-105).

Figure 4-17 DCD Usage

4.2 ENGINEERING DRAWINGS LIST

The following Engineering Drawings are included in this manual for reference purposes.

Drawing Number	Title	Page No.
D-DI-DK10-0-1	Drawing Index List	4-9
D-UA-DK10-0-0	DK10 Real-Time Clock	4-11
A-PL-DK10-0-0	DK10 Unit Assembly, Parts List	4-13
D-FD-DK10-0-FD	Flow Diagram	4-15
D-BS-DK10-0-CLK	Clock Counter	4-17
D-BS-DK10-0-JOB	I/O Bus and Indicator Cables	4-19
D-BS-DK10-0-JOBD	I/O Bus Drivers	4-21
D-BS-DK10-0-JOBI	I/O Bus Interface	4-23
D-BS-DK10-0-IOC	I/O and Clock Control	4-25
D-BS-DK10-0-IR	Interval Register	4-29
D-BS-DK10-0-MOD	Modification to KA10	4-31
D-BS-DK10-0-TIC	Timing Control	4-33
D-BS-DK10-0-TOC	Time Out Comparator	4-35
D-IC-DK10-0-PWR	Power Wiring AC and DC	4-37

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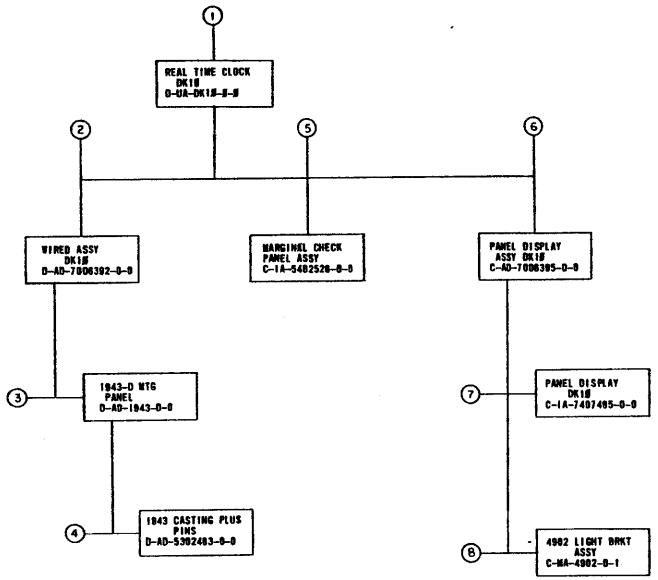

MECHANICAL			DEPT USAGE		
FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C
1.	REAL TIME CLOCK DKIØ REAL TIME CLOCK DKIØ (PL) RIGHT END PANEL DISPLAY CABLE DKIØ BCIØA CABLE (ASSY) CABLE TRANSPORT BUS RET BLOCK (W950)	D-UA-DKIØ-B-B A-PL-DKIØ-B-B C-WD-5302406-B-0 C-IA-7005895-B-0 D-UA-BCIØA-B-B C-IA-7005292-0-0 C-IA-7405575-0-0			
2.	WIRED ASSY DKIØ WIRED ASSY DKIØ (PL) LOGIC FRAME DECALS	D-AD-7006392-0-0 A-PL-7006392-0-0 A-DC-7406371-B-0			
3.	19430 MTG PANEL 1943 MTG PANEL (PL)	D-AD-1943-0-0 A-PL-1943-0-0			
4.	1943 CASTING PLUS PINS 1943 CASTING PLUS PINS (PL) 1943 FRAME CASTING	D-AD-5302483-0-0 A-PL-5302483-0-0 E-MD-1202695-0-0			
5.	MARGINAL CHECK PANEL ASSY MARGINAL CHECK PANEL	C-IA-5402528-0-0 C-WD-5302484-0-0			
6.	PANEL DISPLAY ASSY DKIØ PANEL DISPLAY ASSY DKIØ (PL)	C-AD-7006395-0-0 A-PL-7006395-0-0			
7.	PANEL DISPLAY DKIØ SILK SCREEN	C-IA-7407485-0-0 A-SS-7407485-0-1			
8.	4902 LIGHT BRKT ASSY 4902 LIGHT BRKT ASSY (PL) LIGHT BRKT ETCH BOARD INSTALLATION DWG	C-MA-4902-0-1 A-PL-4902-0-1 C-MD-4902-0-1-0-1 B-MD-4902-0-1-0-2 D-S-4902-0-1-0-3			

ELECTRICAL			DEPT USAGE		
FIND NO.	DESCRIPTION	PART NO.	PROD	CUST	F/C
1.	REAL TIME CLOCK DKIØ MODULE UTILIZATION MODULE UTILIZATION (PL) TIMING CONTROL MODIFICATION TO KAIØ INTERVAL REGISTER I/O BUS INDICATOR CABLES CLOCK COUNTER TIME OUT COMPARITOR I/O AND CLOCK CONTROL I/O BUS DRIVERS I/O BUS INTERFACE FLOW DIAGRAM DKIØ ARRANGEMENT DWG AC/DC POWER WIRING SPECIFICATION SHEET	A-ML-DKIØ-B D-MU-DKIØ-MU A-PL-DKIØ-MU D-BS-DKIØ-B-TIC D-BS-DKIØ-B-WOD D-BS-DKIØ-B-IR D-BS-DKIØ-B-IOB D-BS-DKIØ-B-CLK D-BS-DKIØ-B-TOC D-BS-DKIØ-B-IOC D-BS-DKIØ-B-IOBD D-BS-CKIØ-B-IOBI D-FD-DKIØ-B-FD D-AR-DKIØ-B-AR D-IC-DKIØ-B-PWR A-SP-DKIØ-Ø-2
2.	WIRED ASSY DKIØ WIRED ASSY DKIØ (PL) WIRE LIST	D-AD-7006392-0-0 A-PL-7006392-0-0 K-WL-DKIØ-B-WL
5.	MOUNTING PANEL 1943	B-CS-1943-0-1
8.	CIRCUIT SCHEMATIC	B-CS-4902

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: DKIØ

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY 7
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL —
FINISH —

DRN. J. Marin	DATE 6/6/69	
CHK'D. D. Bonelli	DATE 6/23/69	
ENG. Ronald Adams	DATE 9/10/69	
PROJ. ENG. Russell Evans	DATE 9/12/69	
PROD. M. Mahon	DATE 9-15-69	

NEXT HIGHER ASSY: A-ML-DKIØ-Ø
SCALE: NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DRAWING INDEX LIST

SIZE	CODE	NUMBER	REV.
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DIST.

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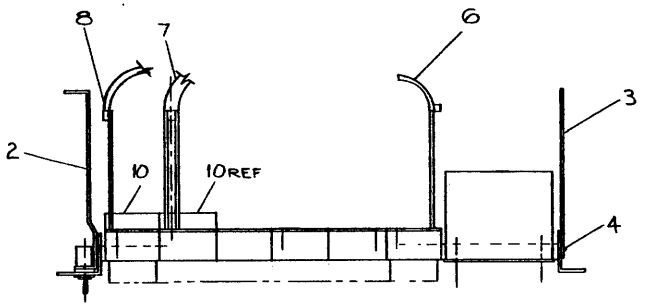
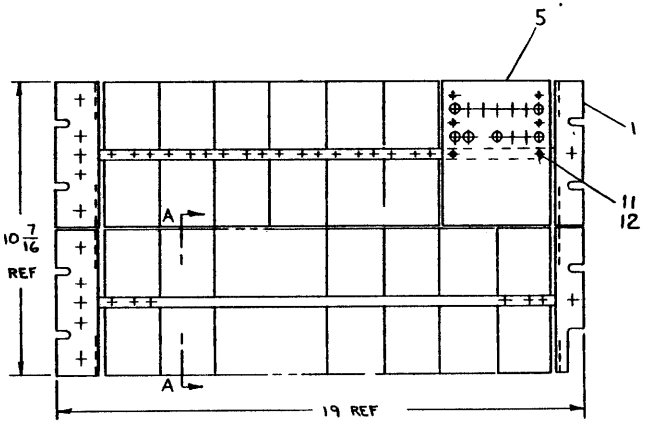
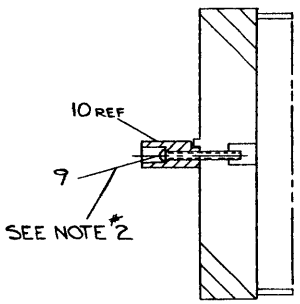
DEC FORM NO DRD 100

1-Ø-ØIKDIQ 3003 3276







SECTION A-A
SCALE: 1/1
2 PLACES

NOTES:

1. REMOVE 2 CONN. BLOCKS FROM 1943D MTG PANEL AND REPLACE WITH ITEM #5 AS SHOWN.
2. REMOVE EXISTING 8-32 SCREW & INSTALL # 9 & 10 AS SHOWN.
3. FOR DRAWING INDEX LIST REFER TO D-DI-DKIØ-Ø-1
4. FOR LOCATIONS OF ITEM'S # 9 & 10 REFER TO MODULE UTILIZATION LIST SPECIFIED ON MASTER DRAWING LIST. USED AT ALL W851 PLACES.
5. LENGTH OF ITEM # 7 TO BE DETERMINED BY SYSTEM CONFIGURATION.

REVISIONS			
CHK	CHANGE NO.	REV.	
FV	MISC DWG 1-C-DK-10-12-70	A	
KENT			

FIRST USE ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DKIØ		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINISH SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

DRN	L.F. Mercier	DATE 5/3/67
CHK'D	R.E. Farrell	DATE 6/16/69
ENGR	R.E. Adams	DATE 8/10/69
ENGR MGR	R.E. Adams	DATE 9/6/69
PROJ LDR	D.M. Lane	DATE 12-19-69

NEXT HIGHER ASSY
A-ML - DKIØ-Ø

SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD MASSACHUSETTS

TITLE
REAL TIME CLOCK
DKIØ

SIZE	CODE	NUMBER	REV.
D	UA	DKIØ - Ø-Ø	A

DIST. G

DEC FORM NO. DRD 500

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

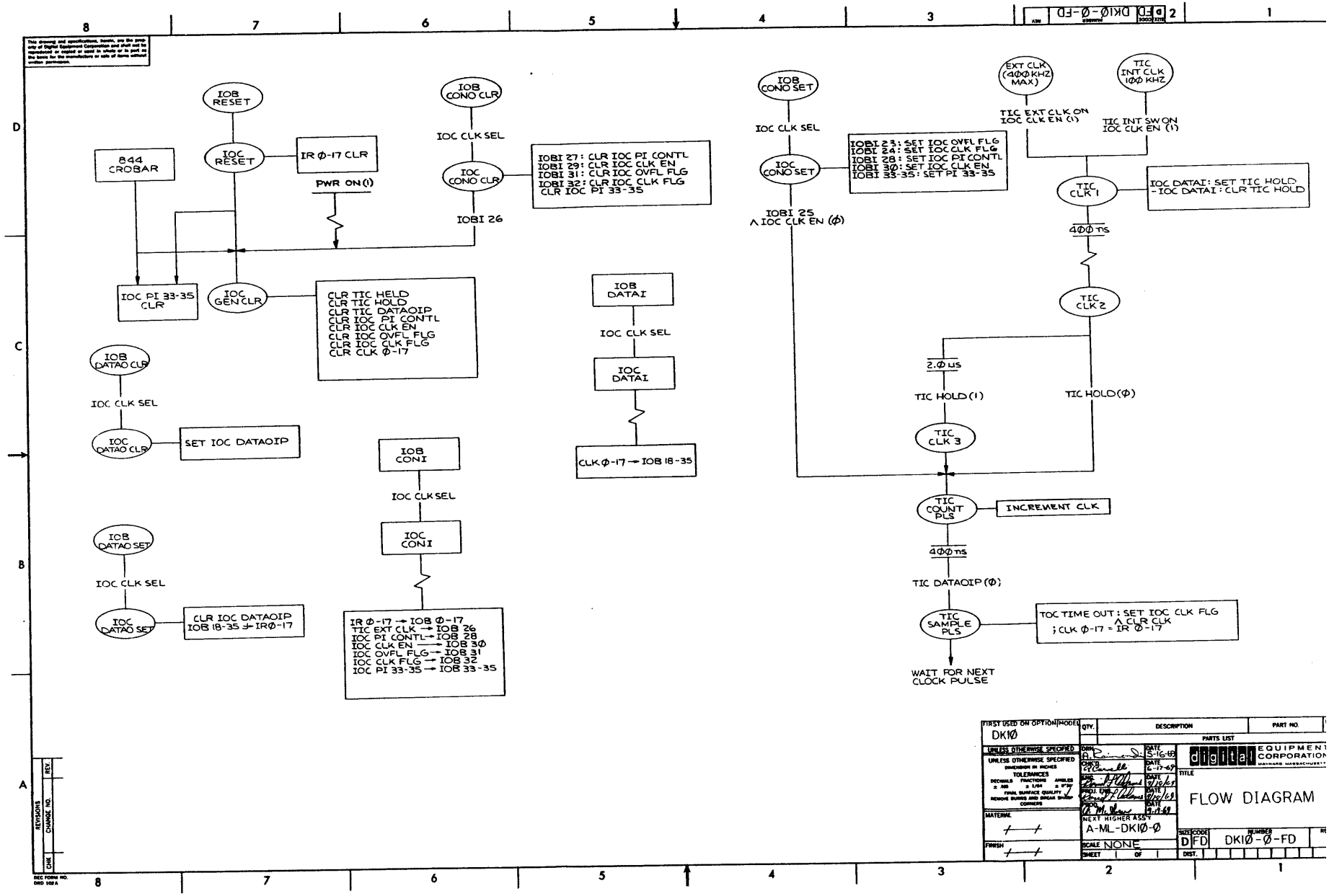
PARTS LIST

MADE BY G. MARINI DATE 6/9/69	CHECKED D. Read DATE 7-11-69	SECTION
ENG David F. Adams DATE 9/18/69	PROD G. McIlveen DATE 9-19-69	ISSUED SECT.

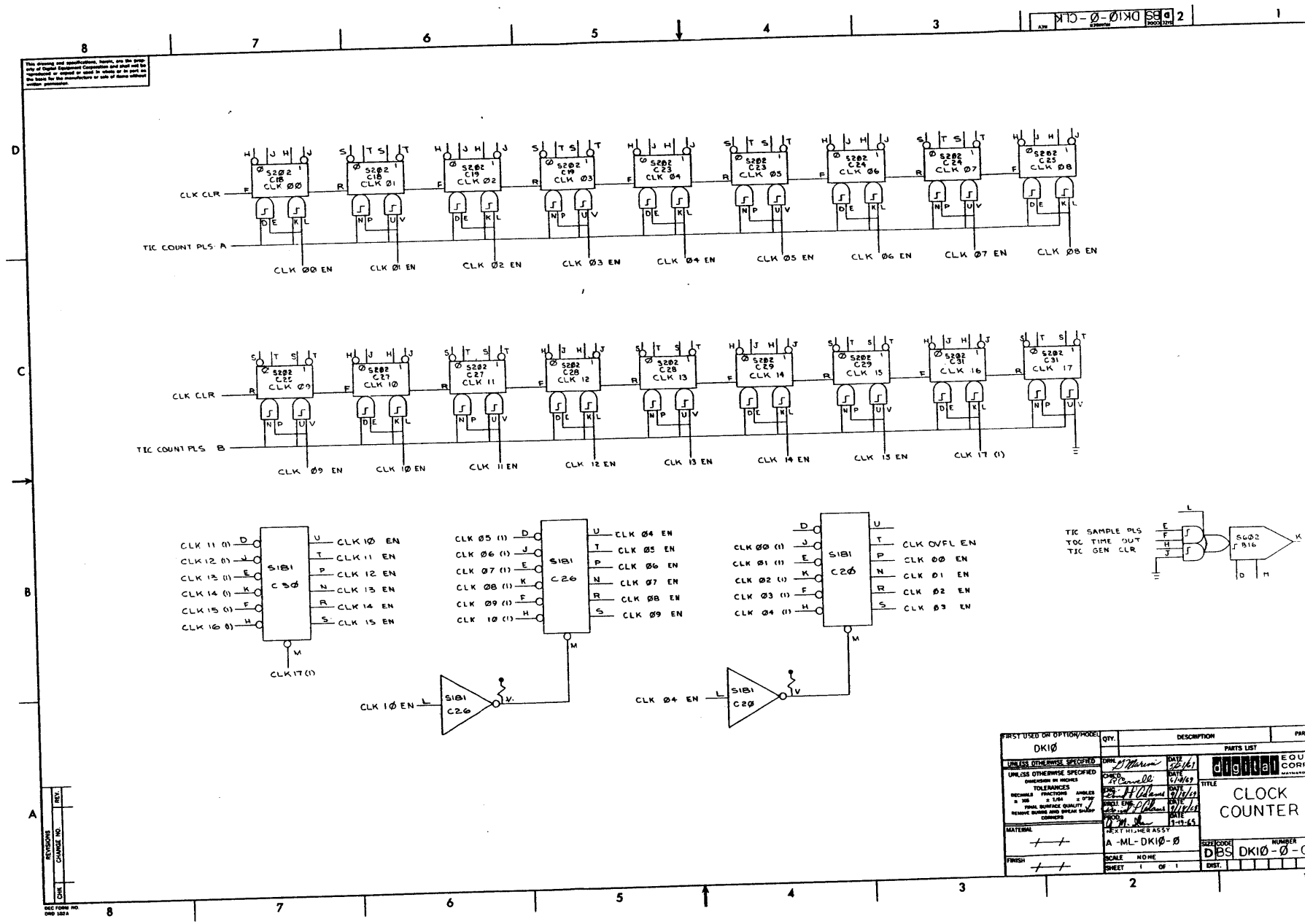
ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION
1	D-AD-7006392-0-0	WIRED ASSY DK1Ø	1
2	C-IA-5402526-0-0	MARGINAL CHECK PANEL	2
3	C-MD-5302486-0-0	RIGHT END PANEL	2
4	9006507	POP RIVET 1/8 DIA x 23/64 LG	16
5	C-AD-7006395-0-0	PANEL DISPLAY DK1Ø ASSY	1
6	C-IA-7005695-0-0	DISPLAY CABLE	2
7	D-UA-BC10A-0-0	BC10/A CABLE ASSY	2
8	C-IA-7005797-0-0	CABLE, TRANSPORT BUS	1
9	9007958	SCR PHL FIL HD 8-32 x 1¼ LG	2
10	D-SC-1209850-0-0	BLOCK RET UNIVERSAL	2
11	9006634	WASH LOCK #8	2
12	9006039	SCR PHIL H PAN #8-32 x ½ LG SST	4

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
REAL TIME CLOCK DK1Ø	D-UA-DK1Ø-Ø-Ø	A	PL	DK1Ø-Ø-Ø	A	MISC-00079
	SHEET 1 OF 1	DIST.	G			

DEC FORM NO.
DRA 110



Flow Diagram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CLK ØØ EN
CLK Ø1 EN
CLK Ø2 EN
CLK Ø3 EN
CLK Ø4 EN
CLK Ø5 EN
CLK Ø6 EN
CLK Ø7 EN
CLK Ø8 EN
CLK CLR
TIC COUNT PLS B
CLK Ø9 EN
CLK 1Ø EN
CLK 11 EN
CLK 12 EN
CLK 13 EN
CLK 14 EN
CLK 15 EN
CLK 17 (1)
S181 C 5Ø
CLK 11 (1)
CLK 12 (1)
CLK 13 (1)
CLK 14 (1)
CLK 15 (1)
CLK 16 (1)
CLK 1Ø EN
CLK 11 EN
CLK 12 EN
CLK 13 EN
CLK 14 EN
CLK 15 EN
CLK 17 (1)
S181 C 26
CLK Ø5 (1)
CLK Ø6 (1)
CLK Ø7 (1)
CLK Ø8 (1)
CLK Ø9 (1)
CLK 1Ø (1)
CLK Ø4 EN
CLK Ø5 EN
CLK Ø6 EN
CLK Ø7 EN
CLK Ø8 EN
CLK Ø9 EN
S181 C 2Ø
CLK Ø4 EN
S181 C 2Ø
CLK ØØ (1)
CLK Ø1 (1)
CLK Ø2 (1)
CLK Ø3 (1)
CLK Ø4 (1)
CLK OVFL EN
CLK ØØ EN
CLK Ø1 EN
CLK Ø2 EN
CLK Ø3 EN
TIC SAMPLE PLS
TOC TIME OUT
TIC GEN CLR
S402 816
DKIØ-Ø-CLK
DKIØ
CLOCK COUNTER
DBS DKIØ-Ø-C
A -ML-DKIØ-Ø
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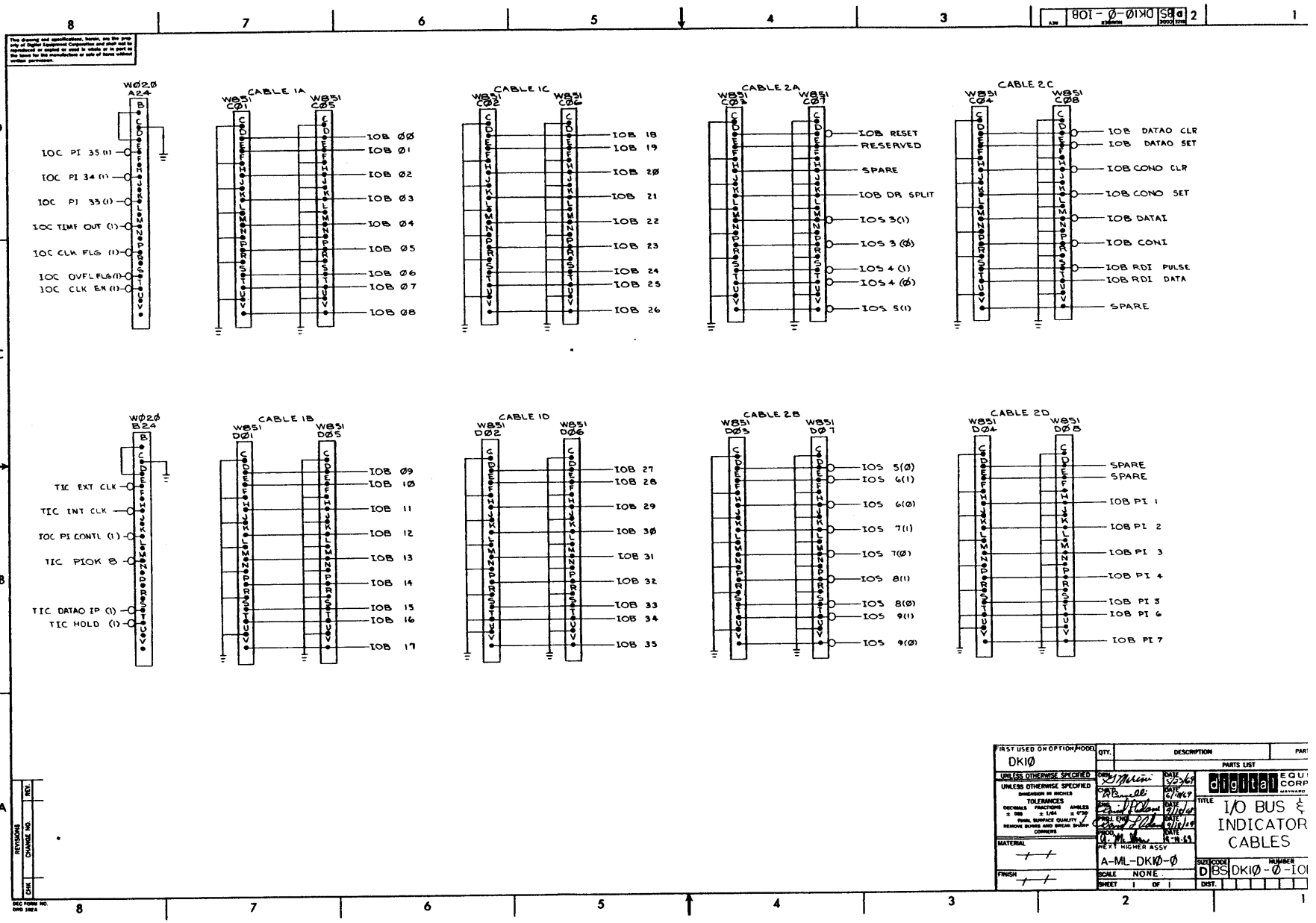
SHEET 1 OF 1
REVISIONS
REV.
CHANGE NO.
CHK.
DEC FORM NO. DRD 102 A


W02Ø A24
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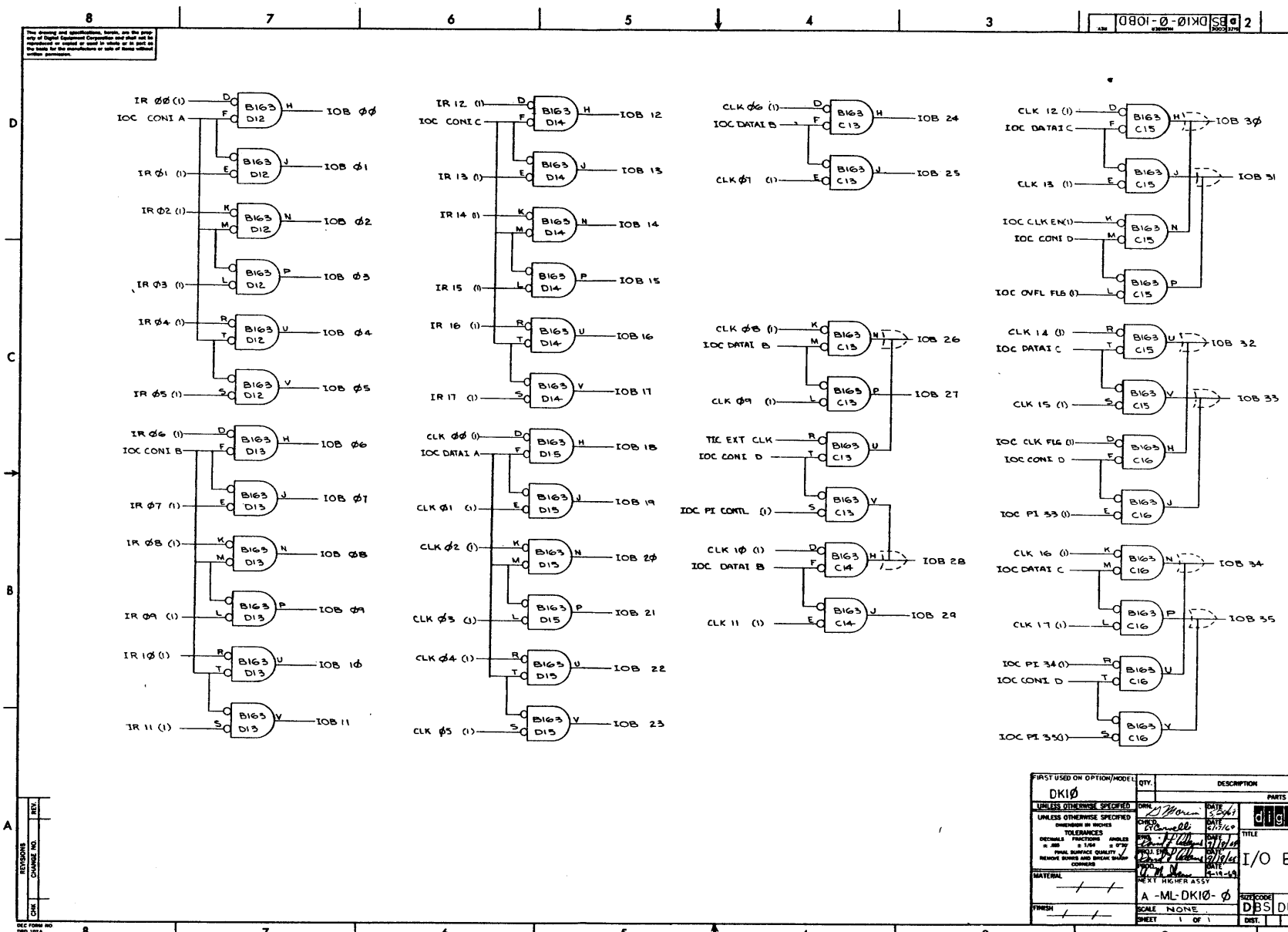
IOC PI 34 (1)
IOC PI 33 (1)
IOC TIME OUT (1)
IOC CLK FLG (1)
IOC OVFL FLG (1)
IOC CLK EN (1)
CABLE 1A
W851 C01
W851 C05
IOB ØØ
IOB Ø1
IOB Ø2
IOB Ø3
IOB Ø4
IOB Ø5
IOB Ø6
IOB Ø7
IOB Ø8
CABLE 1C
W851 C02
W851 C06
IOB 18
IOB 19
IOB 2Ø
IOB 21
IOB 22
IOB 23
IOB 24
IOB 25
IOB 26
CABLE 2A
W851 C03
W851 C07
IOB RESET
RESERVED
SPARE
IOB DR SPLIT
IOS 3(1)
IOS 3 (Ø)
IOS 4 (1)
IOS 4 (Ø)
IOS 5(1)
CABLE 2C
W851 C04
W851 C08
IOB DATAO CLR
IOB DATAO SET
IOB CONO CLR
IOB CONO SET
IOB DATAI
IOB CONI
IOB RDI PULSE
IOB RDI DATA
SPARE
W02Ø B24
TIC EXT CLK
TIC INT CLK
IOC PI CONTL (1)
TIC PIOK B
TIC DATAO IP (1)
TIC HOLD (1)
CABLE 1B
W851 D01
W851 D05
IOB Ø9
IOB 1Ø
IOB 11
IOB 12
IOB 13
IOB 14
IOB 15
IOB 16
IOB 17
CABLE 1D
W851 D02
W851 D06
IOB 27
IOB 28
IOB 29
IOB 3Ø
IOB 31
IOB 32
IOB 33
IOB 34
IOB 35
CABLE 2B
W851 D03
W851 D07
IOS 5(Ø)
IOS 6(1)
IOS 6(Ø)
IOS 7(1)
IOS 7(Ø)
IOS 8(1)
IOS 8(Ø)
IOS 9(1)
IOS 9(Ø)
CABLE 2D
W851 D04
W851 D08
SPARE
SPARE
IOB PI 1
IOB PI 2
IOB PI 3
IOB PI 4
IOB PI 5
IOB PI 6
IOB PI 7
FIRST USED ON OPTION/MODEL
DKIØ
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
MATERIAL
FINISH
QTY.
DESCRIPTION
PARTS LIST
DRN
CHK
ENG
PROJ
NEXT HIGHER ASSY
A-ML-DKIØ-Ø
SCALE NONE
SHEET 1 OF 1
digital EQUIPMENT CORPORATION
TITLE
I/O BUS & INDICATOR CABLES
SIZE CODE
D BS
NUMBER
DKIØ-Ø-IOB
DIST.
REVISIONS
REV.
CHANGE NO.
CHK
DEC FORM NO. DMD 1987 A


IR ØØ (1)
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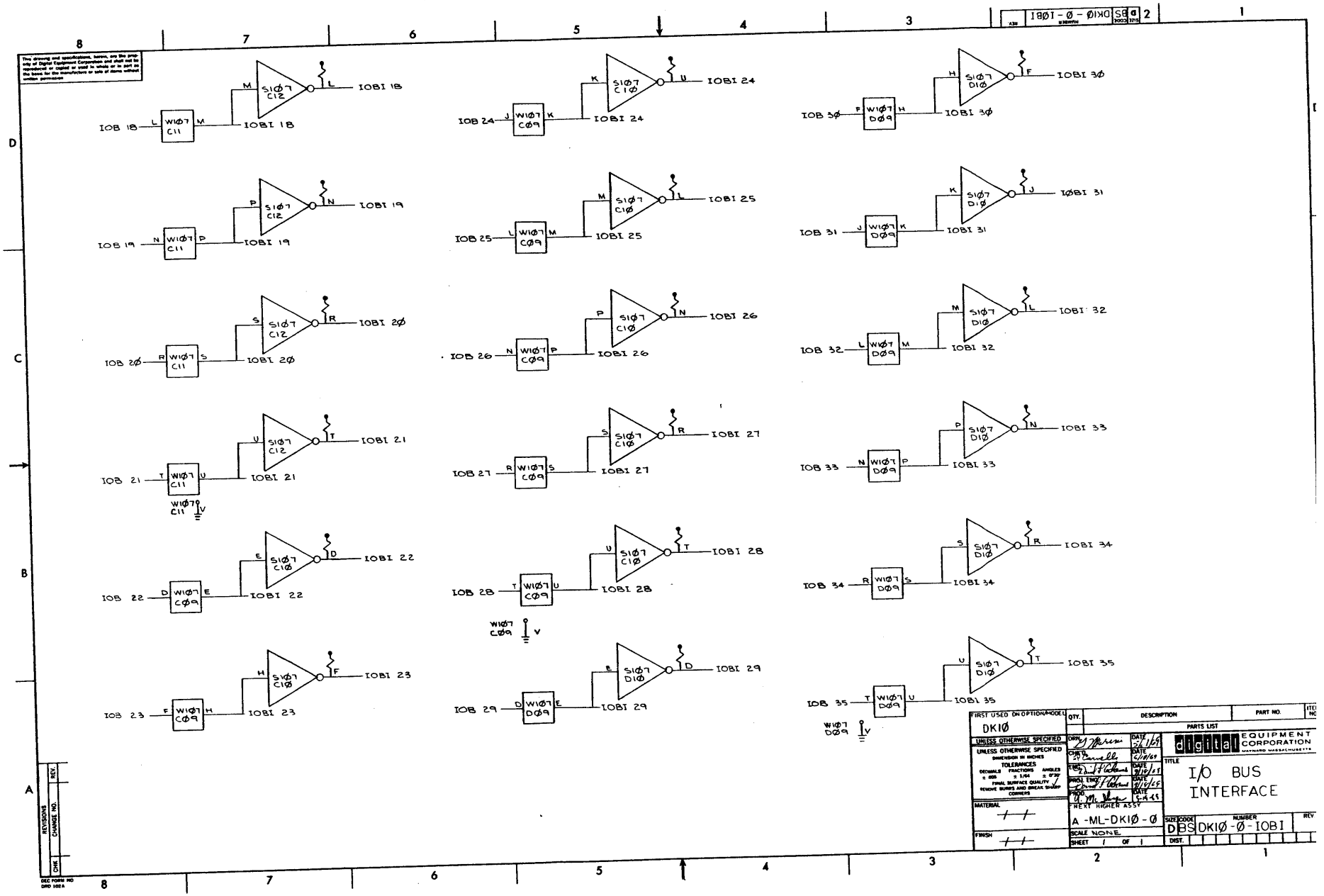
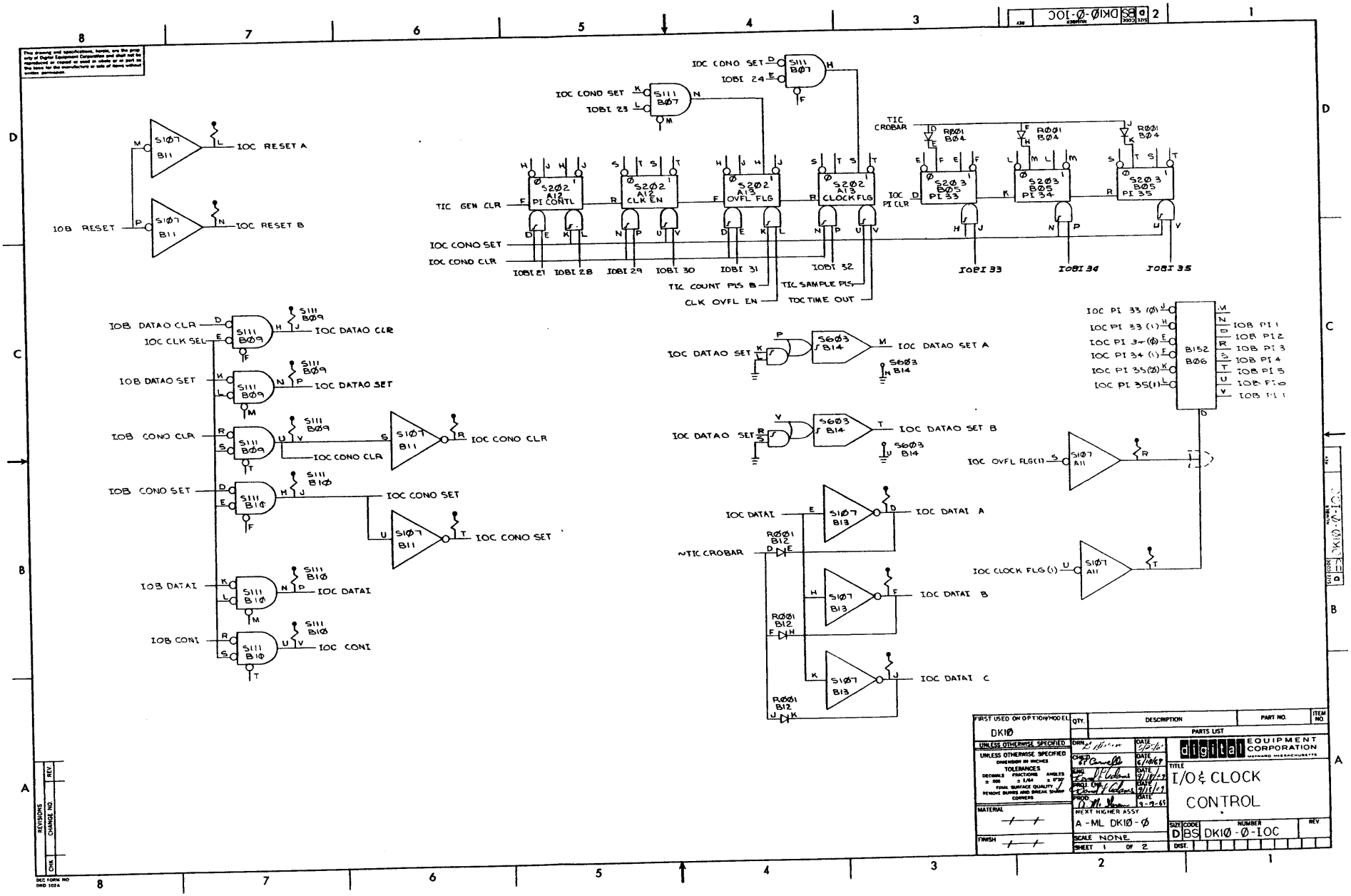
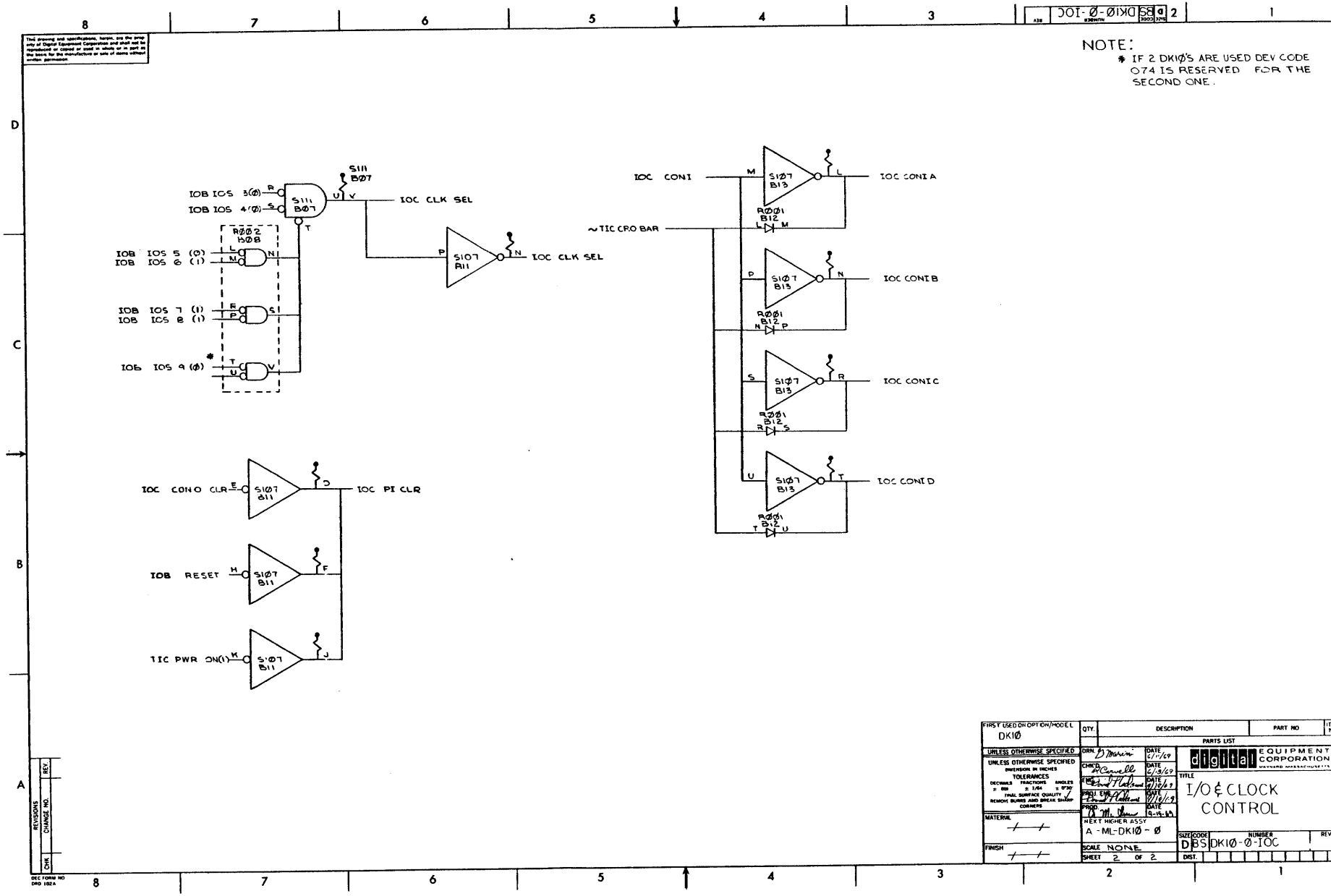
IOB ØØ
IR Ø1 (1)
IOB Ø1
IR Ø2 (1)
IOB Ø2
IR Ø3 (1)
IOB Ø3
IR Ø4 (1)
IOB Ø4
IR Ø5 (1)
IOB Ø5
IR Ø6 (1)
IOC CONI B
IOB Ø6
IR Ø7 (1)
IOB Ø7
IR Ø8 (1)
IOB Ø8
IR Ø9 (1)
IOB Ø9
IR 1Ø (1)
IOB 1Ø
IR 11 (1)
IOB 11
IR 12 (1)
IOC CONI C
IOB 12
IR 13 (1)
IOB 13
IR 14 (1)
IOB 14
IR 15 (1)
IOB 15
IR 16 (1)
IOB 16
IR 17 (1)
IOB 17
CLK ØØ (1)
IOC DATAI A
IOB 18
CLK Ø1 (1)
IOB 19
CLK Ø2 (1)
IOB 2Ø
CLK Ø3 (1)
IOB 21
CLK Ø4 (1)
IOB 22
CLK Ø5 (1)
IOB 23
CLK Ø6 (1)
IOC DATAI B
IOB 24
CLK Ø7 (1)
IOB 25
CLK Ø8 (1)
IOC DATAI B
IOB 26
CLK Ø9 (1)
IOB 27
TIC EXT CLK
IOC CONI D
IOC PI CONTL (1)
CLK 1Ø (1)
IOC DATAI B
IOB 28
CLK 11 (1)
IOB 29
CLK 12 (1)
IOC DATAI C
IOB 3Ø
CLK 13 (1)
IOB 31
IOC CLK EN (1)
IOC CONI D
IOC OVFL FLG (1)
CLK 14 (1)
IOC DATAI C
IOB 32
CLK 15 (1)
IOB 33
IOC CLK FLG (1)
IOC CONI D
IOC PI 33 (1)
CLK 16 (1)
IOC DATAI C
IOB 34
CLK 17 (1)
IOB 35
IOC PI 34 (1)
IOC CONI D
IOC PI 35 (1)
B163 D12
B163 D13
B163 D14
B163 D15
B163 C13
B163 C14
B163 C15
B163 C16
DKIØ
DIGITAL EQUIPMENT CORPORATION
I/O BUS DRIVERS
A-ML-DKIØ-Ø
DBS DKIØ-Ø-IOBD
SCALE NONE
SHEET 1 OF 1



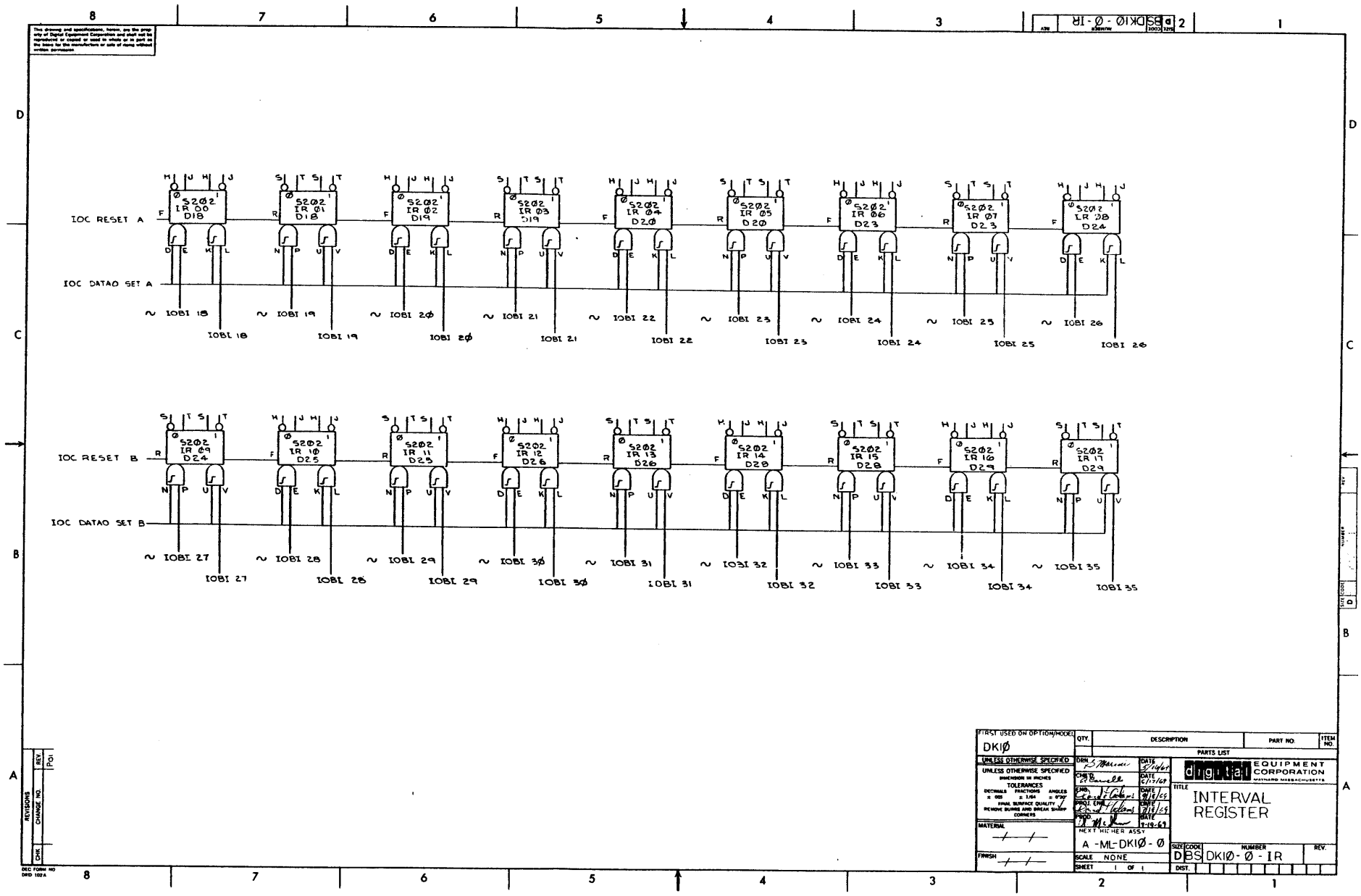
I/O Bus Interface



I/O and Clock Control (Sheet 1 of 2)



I/O and Clock Control (Sheet 2 of



Interval Register

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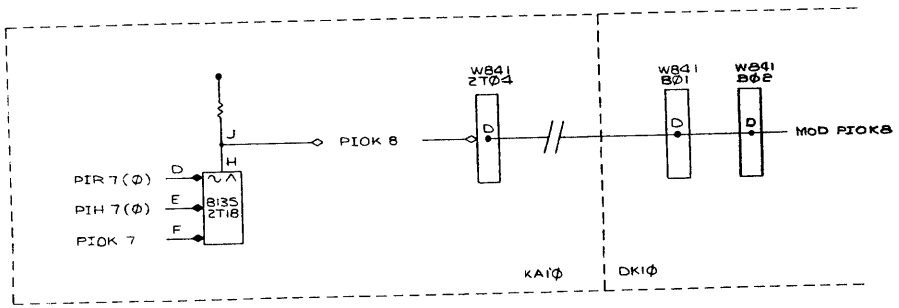
WIRE LIST

SIG NAME	FROM	TO	LEVEL	ADD	DEL
PIR 7(Ø)-	2S19P	2T18D	2	X	
PIH 7(Ø)-	2S13E	2T18E	2	X	
PIOK 7-	2S1ØE	2T18F	2	X	
PIOK 8	2T18H	2T18J	1	X	
PIOK 8	2T18H	2TØ4D	2	X	
GND	2TØ4F	2TØ4J	1	X	
GND	2TØ4L	2TØ4N	1	X	
GND	2TØ4R	2TØ4U	1	X	
GND	2TØ4C	2TØ4F	2	X	
GND	2TØ4J	2TØ4L	2	X	
GND	2TØ4N	2TØ4R	2	X	

NOTES:

1. ADD THE FOLLOWING TO KA1Ø BAY 2
   A. B135 TO LOCATION 2T18
   B. W841 (CABLE PART NO. 7ØØ5797) TO LOCATION 2TØ4



FIRST USED ON OPTION/MODE	QTY.	DESCRIPTION	PART NO.
DK1Ø		PARTS LIST	

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —/—/—
FINISH —/—/—

DRN. A. [signature] DATE 5-16-69
CHK'D. [signature] DATE 6-16-69
ENG. [signature] DATE 9/19/69
PROJ. ENG. [signature] DATE 9/19/69
PROD. [signature] DATE 9-19-69

NEXT HIGHER ASS'Y A-ML-DK1Ø-Ø
SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

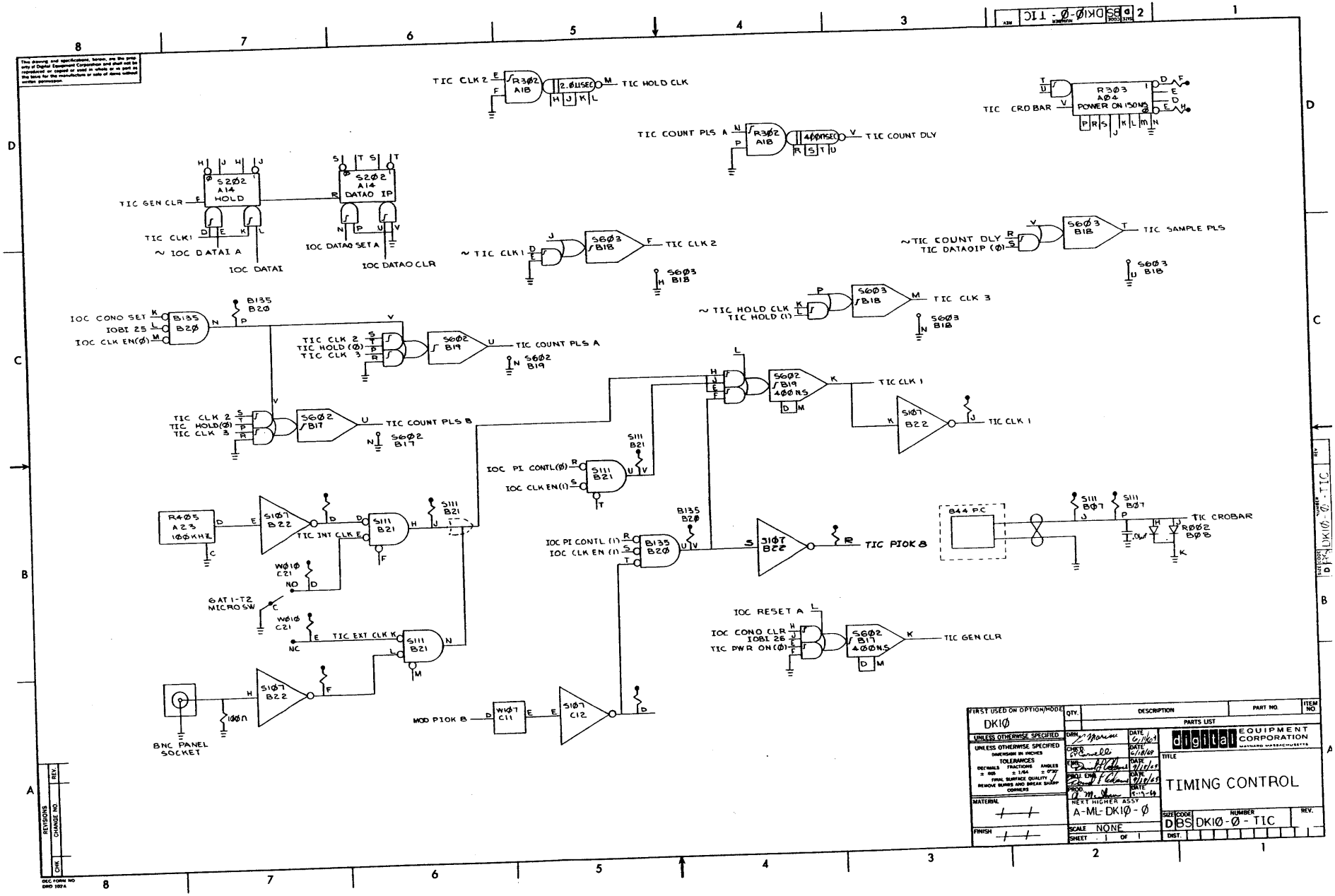
TITLE MODIFICATION TO KA1Ø FOR DK1Ø (OPTION)

SIZE D CODE BS NUMBER DK1Ø-Ø-MOD REV
DIST.

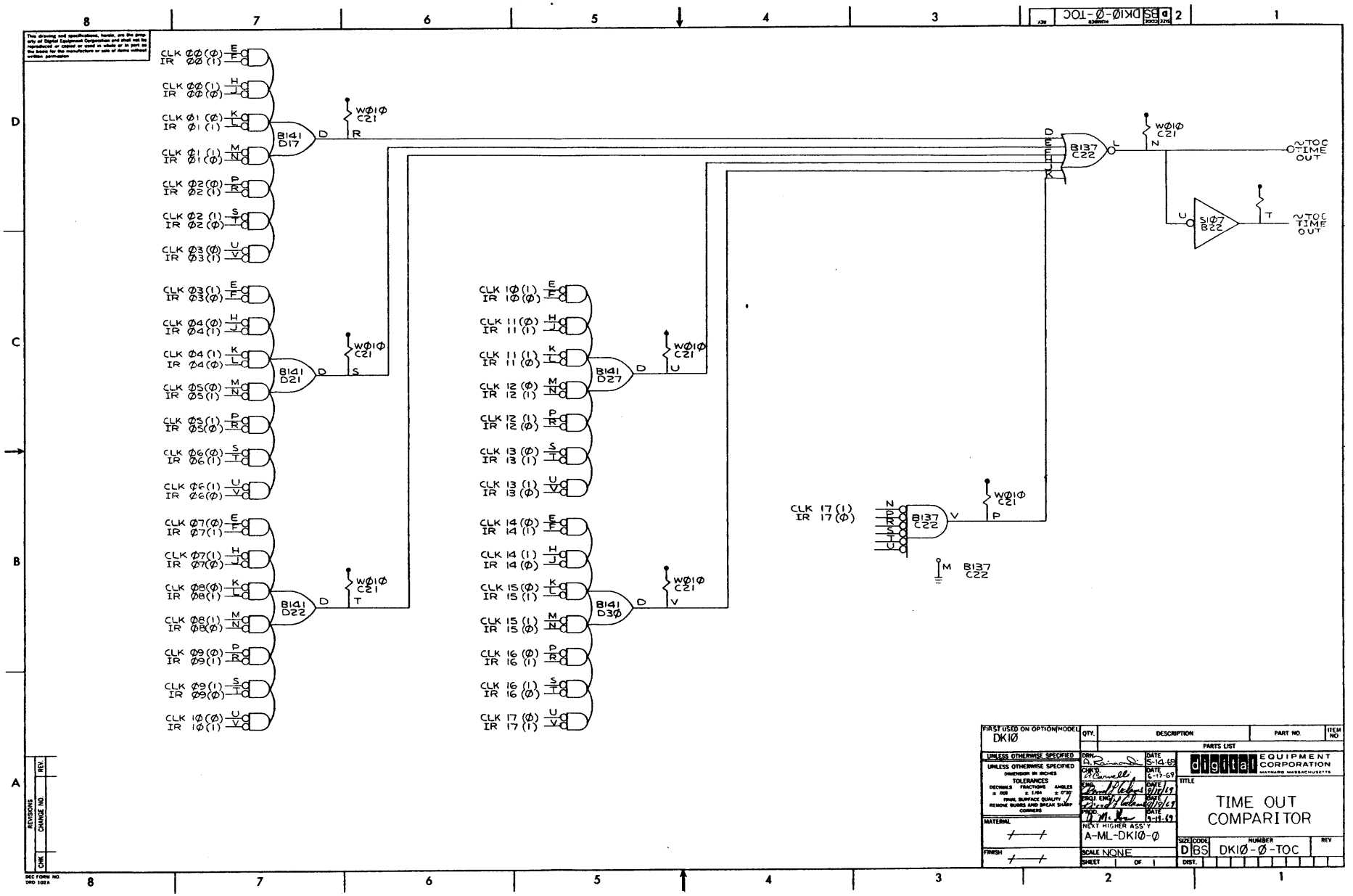
REVISIONS: CHK | CHANGE NO. | REV

DEC FORM NO DRD 102A

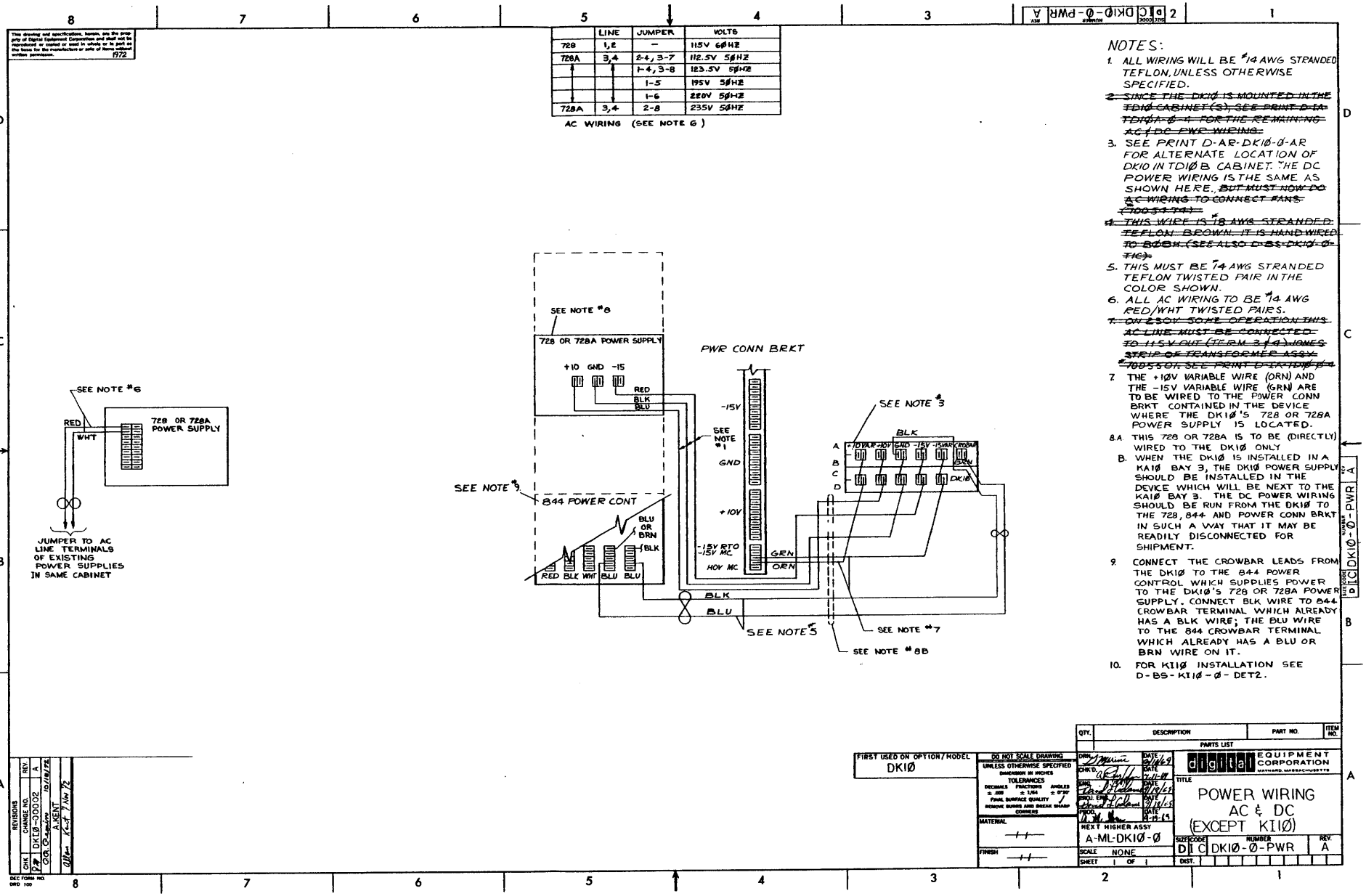
Modification to KA10



Timing Control



Time Out Comparator



	LINE	JUMPER	VOLTS
728	1,2	—	115V 6ØHZ
728A	3,4	2-4, 3-7	112.5V 5ØHZ
		1-4, 3-8	123.5V 5ØHZ
		1-5	195V 5ØHZ
		1-6	220V 5ØHZ
728A	3,4	2-8	235V 5ØHZ

AC WIRING (SEE NOTE 6)

NOTES:

1. ALL WIRING WILL BE #14 AWG STRANDED TEFLON, UNLESS OTHERWISE SPECIFIED.
2. ~~SINCE THE DKIØ IS MOUNTED IN THE TDIØ CABINET(S), SEE PRINT D-IA-TDIØA-Ø-4 FOR THE REMAINING AC & DC PWR WIRING.~~
3. SEE PRINT D-AR-DKIØ-Ø-AR FOR ALTERNATE LOCATION OF DKIO IN TDIØ B CABINET. THE DC POWER WIRING IS THE SAME AS SHOWN HERE. ~~BUT MUST NOW DO AC WIRING TO CONNECT FANS (700534-74).~~
4. ~~THIS WIRE IS #18 AWG STRANDED TEFLON BROWN. IT IS HAND WIRED TO BØBH (SEE ALSO D-BS-DKIØ-Ø-TIC).~~
5. THIS MUST BE #14 AWG STRANDED TEFLON TWISTED PAIR IN THE COLOR SHOWN.
6. ALL AC WIRING TO BE #14 AWG RED/WHT TWISTED PAIRS.
7. ~~ON 230V 50HZ OPERATION THIS AC LINE MUST BE CONNECTED TO 115V OUT (TERM 3 & 4) JONES STRIP OF TRANSFORMER ASSY #700550. SEE PRINT D-IA-TDIØ-Ø-4.~~
7. THE +10V VARIABLE WIRE (ORN) AND THE -15V VARIABLE WIRE (GRN) ARE TO BE WIRED TO THE POWER CONN BRKT CONTAINED IN THE DEVICE WHERE THE DKIØ'S 728 OR 728A POWER SUPPLY IS LOCATED.
8. A. THIS 728 OR 728A IS TO BE (DIRECTLY) WIRED TO THE DKIØ ONLY
   B. WHEN THE DKIØ IS INSTALLED IN A KAIØ BAY 3, THE DKIØ POWER SUPPLY SHOULD BE INSTALLED IN THE DEVICE WHICH WILL BE NEXT TO THE KAIØ BAY 3. THE DC POWER WIRING SHOULD BE RUN FROM THE DKIØ TO THE 728, 844 AND POWER CONN BRKT IN SUCH A WAY THAT IT MAY BE READILY DISCONNECTED FOR SHIPMENT.
9. CONNECT THE CROWBAR LEADS FROM THE DKIØ TO THE 844 POWER CONTROL WHICH SUPPLIES POWER TO THE DKIØ'S 728 OR 728A POWER SUPPLY. CONNECT BLK WIRE TO 844 CROWBAR TERMINAL WHICH ALREADY HAS A BLK WIRE; THE BLU WIRE TO THE 844 CROWBAR TERMINAL WHICH ALREADY HAS A BLU OR BRN WIRE ON IT.
10. FOR KIIØ INSTALLATION SEE D-BS-KIIØ-Ø-DET2.

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

FIRST USED ON OPTION/MODEL: DKIØ

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —/—
FINISH —/—

DRN. [signature] DATE 9/18/69
CHK'D. [signature] DATE 9-11-69
ENG. [signature] DATE 9/19/69
PROJ. ENG. [signature] DATE 9/18/69
PROD. [signature] DATE 9-19-69

NEXT HIGHER ASSY: A-ML-DKIØ-Ø
SCALE: NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: POWER WIRING AC & DC (EXCEPT KIIØ)

SIZE D | CODE C | NUMBER DKIØ-Ø-PWR | REV. A
DIST.

REVISIONS

CHK	CHANGE NO.	REV.
[signature]	DKIØ-00002	A
[signature]	[signature]	10/18/72

A. KENT
[signature] Kent 7 Nov 72

DEC FORM NO. DRD 100

Power Wiring AC and DC