DOLPHIN CLOCKING - CONTROL AND DISTRIBUTION SPECIFICATION

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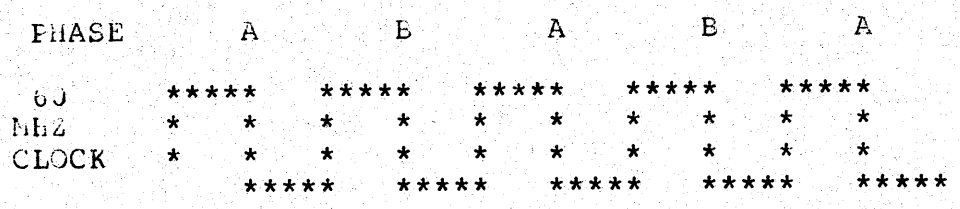
Oct 22,1978
REV 1 - DEC.19,1978

A diagram showning the clock distribution scheme in a single Dolphin processor is shown in figure 1. There are two possible sources of clocks.

Single processor systems will normally use the internal VFO oscillator which is located on the console.

In a multiprocessor system an external oscillator will be used which will be located somewhere in the system but not on the console. In either case the nominal clock frequency is 60 MHZ. The Dolphin bus operates with a 30MHZ clock which is derived by dividing the 60 MHZ clock by two. When two Dolphin buses are connected together with a bus repeater, it is necessary that the two different bus clocks have their true going edges occur at the same time. Without phasing information it would be possible for the two bus clocks to be 180 degrees out between the two systems. Therefore phase information is supplied by the external oscillator and maintained by the clock distribution logic. The 60 MHZ clock stream is alternately labled phase a, phase b as shown below.



The master oscillator is a VFO type with a nominal center frequency of 60 MHZ. Thru a control register on the console, the oscillator's frequency can be varied from 50 to 70 MHZ in .5 MHZ steps (this corresponds to loading 100 to 140 in the VFO control register). The oscillator's output connects to the clock control MCA. The clock control MCA provides the basic clock control functions which affects all the clocks within a single backplane assembly. The clock control functions are: SELECT OSCILLATOR SOURCE (external or internal oscillator), CLOCK ON, CLOCK OFF, HALF STEP, and BURST THE CLOCK. The hardware will automaticaly prevent selection off the external oscillator if external clocks are not being received.

The clock control chip, together with the clock distribution chips provide the capability to establish the correct phasing of clocks within a backplane and between CPU clusters in multi-processor configurations. The Dolphin backplane bus is operated at 30 MHZ. The phase information is used to insure that both ends of a bus repeater always clock on the same edge of the 60MHZ clock source. Bus repeaters always clock on the A phase (phase information is always supplied by an external oscillator).

CLOCK INITIALIZATION - The clocks should first be turned off. Then the IIL logic should be used to assert RESET in all chips which are to be initialized. The clocks should then be turned on. The clocks must then be turned off and then RESET deasserted. The distribution chips will declare the first clock after reset to be an A phase clock.

CLOCK CONTROL - The CLOCK OFF function simply turns off the clocks. The CLOCK ON function turns the clocks on. The control chip remembers which clock phase was output last and insures that the next clock produced will be of the opposite phase. This distinction of phases at the control chip is only necessary on multi processor configurations. The BURST function outputs a specified number of clocks, always ending with the clock false. The number of cycles to be produced must be first loaded (how is not specified yet). The BURST function also remembers which phase was produced last and insures that the next falling edge is of opposite phase. The clock half step cause the clock to advance 1/2 of a clock cycle. The clock must be in the false state before the clock can turned on or bursted.

DISTRIBUTION -The clock distribution MCAs are used in a tree structure to provide sufficient fan out to reach every MCA chip(see diagram). The output of the clock control MCA is feed to a clock distribution MCA. The distribution MCA in turn feeds a second level of distribution MCA's. The second level distribution MCA outputs are the "clocks on a module". The distribution MCAs contain the logic to support different module requirements.

CLOCK STOPPING AND ERROR REPORTING - The level I clocks are normally 60 MHZ. The frequency of these clocks can be modified for diagnostic and margining purposes. The frequency can be altered by changing the main oscillator's frequency (50 to 70 MHZ) or by dividing the oscillators frequency by 2, 4, or 6. The clock stop, clock rate, burst, start, etc. operations affect all clocks in the system. Clock error stops are only allowed on individual module clock distribution chips (i.e only on level 2 clocks). For normal operation no clocks are allowed to be stopped for which the clock stop could cause a bus message to be munged or lost. Presently the only clocks which are allowed to be stopped are in the the P-BOX. The M-BOX will not be stopped since it talks directly to the bus. Instead errors

information will be recorded in error registers in the M-Box.

DISTRIBUTION CHIP FUNCTIONS - The clock distribution MCA is used to distribute clocks from the console to each module and from each module to each chip. There is only one clock input pin per clock distribution chip. During normal operation the clock input frequency will be 60MHZ. The first level clock distribution MCA's can be varied to control the overall clocking rate of the machine. The second level MCA's timing control is used to suplly individual clocking rates for each section of logic. The distribution MCA provide 3 separately controllable clocking units on each MCA with 8 outputs per unit.

Phase information is no transmitted from the console to each MCA. Instead, the initial phase information is established by reseting the clock MCA's thru the IIL logic. Phase information can be feed into the chip from an external source. The IIL status bits control the source of phase information.

Each clocking unit within the clock distribution MCA has the following:

1. Symmetrical clocks for 60 or 30 MHZ clocks. All clocks slower than 30 MHZ will be on for only 16 ns.

2. A three bit clock rate input is provided. If N is loaded, then the next clock will be output in (N*16) + 16 n.s. Clock rates for the next cycle are sampled on the falling edge of output clocks (this is not exactly true they are sample slightly before the output clock - more details to follow).

3. The clock rate lines are parity checked. If the parity is incorrect the clock rate (n) is forced to 7.

4. The clocks can be specified as either A phase, B phase or next. The phase information is sampled on every input clock tic (nominally 60 MHZ).

CLOCK ON A PHASE	CLOCK ON B PHASE	RESULT
FALSE	FALSE	CLOCKS TURNED OFF (used for wait state -i.e. KL10 MB wait)
FALSE	TRUE	WAIT FOR TIME SPECIED BY CLOCK RATE TO EXPIRE - THEN OUTPUT CLOCK ON NEXT B PHASE
TRUE	FALSE	WAIT FOR TIME SPECIED BY CLOCK RATE TO EXPIRE - THEN OUTPUT CLOCK ON NEXT B PHASE
TRUE	TRUE	WAIT FOR TIME SPECIED BY CLOCK RATE TO EXPIRE - THEN OUTPUT CLOCK

5. There are four ways to stop clocks. The first method was described above , that is declaring the clock to be output on neither A or B phase. The second is thru a EXT"N" STROBED STOP H input. This signal is sampled approximately 8 n.s. before the output clock. If true when sampled this signal will prevent clocks from being output. The third method is thru EXT"N" FIELD INPUT 1 or 2 H. This signal is tied directly to the combinational output gating. This signal must be stable whenever an input clock is true or the output clocks will be distorted. This signal must be asserted approximately 3 n.s. before the clock is to be output to stop the clock. The fourth method is thru the IIL logic . The IIL logic can turn off each clock section independently by asserting the appropriate INHIBIT SECTION bit.

In addition each MCA has an input clock counter. The counter is four bits in length and readable only by the IIL logic. All second level distribution chips should always have the same value in the counter after reset.

IF a parity error is detected in any section of a clock distribution chip an error flag is asserted. This error flag remains set until the IIL CLEAR ERROR signal is asserted. The error flag is not cleared by a RESET.

SKEW - The the processor and all devices connecting to the bus receive their clocks from one first level distribution chip. The memory array modules receive their clocks from a second distribution chip. The skew for modules is as follows.

SAME BOARD SKEW (1 CLOCK LOAD PER OUTPUT)

DIST CHIP OUTPUT SKEW	550 N.S.
CLOCK BUFFER SKEW	700 N.S.
CLOCK LOAD VARIANCE	260 N.S.
CLOCK ETCH TOLERANCE	50 N.S.
	1.560 N.S.

SAME BOARD SKEW (2 CLOCK LOADS PER OUTPUT)

SAME BOARD SKEW (1 LOAD)	1.560 N.S.
DUAL CONNECTION SKEW	.400 N.S.
	1.960 N.S.

DIFFERENT MODULE SKEW

SAME BOARD SKEW (2 LOADS)	1.960 N.S.
FIRST LEVEL OUTPUT SKEW	.550 N.S.
DESKEW ACCURACY	.100 N.S.
COAX ACCURACY	.050 N.S.
	2.660 N.S.

DIFFERENT FIRST LEVEL SOURCES
(MEMORY ARRAYS)

DIFFERENT MODULE SKEW	2.660 N.S.
DESKEW ACCURACY	.100 N.S.
	2.710 N.S.

CLOCK DISTRIBUTION MCA INPUTS AND OUTPUTS - The inputs and outputs are labled ext"N". The "N" refers to the clock section numbers. All signals are inputs unless otherwise stated.

U102	EXT1 FIELD INPUT 1 H	
U100	EXT1 FIELD INPUT 2 H	
U119	EXT2 FIELD INPUT 1 H	
U117	EXT2 FIELD INPUT 2 H	
U136	EXT3 FIELD INPUT 1 H	
U134	EXT3 FIELD INPUT 2 H	- When either INPUT 1 or 2 is high the output clocks will be prevented from occurring. This signal must be asserted within 3 n.s. before the clock was to occur. This signal cannot prevent clocks from being output when the input clock rate has a parity error.
U101	EXT1 STROBED STOP H	
U118	EXT2 STROBED STOP H	
U135	EXT3 STROBED STOP H	- This input is sampled approximately 8 n.s. before every 60 MHZ clock edge. If high when sampled the output clock will be inhibited during the next 60 MHZ clock cycle.
U103	-EXT1 CLOCK ON B PHASE H	
U120	-EXT2 CLOCK ON B PHASE H	
U137	-EXT3 CLOCK ON B PHASE H	- When true, an output clock is allowed to be output on the B phase. If false no clocks are allowed to be output on the B phase.
U104	-EXT1 CLOCK ON A PHASE H	
U121	-EXT2 CLOCK ON A PHASE H	
U138	-EXT3 CLOCK ON A PHASE H	- When true, an output clock is allowed to be output on the A phase. If false no clocks are allowed to be output on the A phase.

U105	EXT1 PARITY H
U106	EXT1 CLOCK RATE IN 4 H
U107	EXT1 CLOCK RATE IN 2 H
U108	EXT1 CLOCK RATE IN 1 H
U122	EXT2 PARITY H
U123	EXT2 CLOCK RATE IN 4 H
U124	EXT2 CLOCK RATE IN 2 H
U125	EXT2 CLOCK RATE IN 1 H
U139	EXT3 PARITY H
U140	EXT3 CLOCK RATE IN 4 H
U141	EXT3 CLOCK RATE IN 2 H
U142	EXT3 CLOCK RATE IN 1 H

- These groups of signals supplies the minimum amount of time to occur before an clock is output.

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U109	-EXT1 CLOCK OUT 8 H
U110	-EXT1 CLOCK OUT 7 H
U111	-EXT1 CLOCK OUT 6 H
U112	-EXT1 CLOCK OUT 5 H
U113	-EXT1 CLOCK OUT 4 H
U114	-EXT1 CLOCK OUT 3 H
U115	-EXT1 CLOCK OUT 2 H
U116	-EXT1 CLOCK OUT 1 H
U126	-EXT2 CLOCK OUT 8 H
U127	-EXT2 CLOCK OUT 7 H
U128	-EXT2 CLOCK OUT 6 H
U129	-EXT2 CLOCK OUT 5 H
U130	-EXT2 CLOCK OUT 4 H
U131	-EXT2 CLOCK OUT 3 H
U132	-EXT2 CLOCK OUT 2 H
U133	-EXT2 CLOCK OUT 1 H
U143	-EXT3 CLOCK OUT 8 H
U144	-EXT3 CLOCK OUT 7 H
U145	-EXT3 CLOCK OUT 6 H
U146	-EXT3 CLOCK OUT 5 H
U147	-EXT3 CLOCK OUT 4 H
U148	-EXT3 CLOCK OUT 3 H
U149	-EXT3 CLOCK OUT 2 H
U150	-EXT3 CLOCK OUT 1 H

- OUTPUT SIGNAL - These are the output clocks.

U151	-CLOCK IN H	- This is the common clock input for all sections.
U152	CLOCK ERROR H	- OUTPUT SIGNAL - When true this signal indicates that a parity error was detected on one of the sections clock rate input lines.
U153	DIAG DATA OUT H	
U154	DIAG DATA IN H	
U155	DIAG CLOCK H	- Standard IIL diagnostic lines.
U157	EXT PHASE A NEXT H	- External phase information input. IIL status bit CLK7 EXT PHASE L must be true or this signal will be ignored.

IIL DIAGNOSTIC STATUS BITS

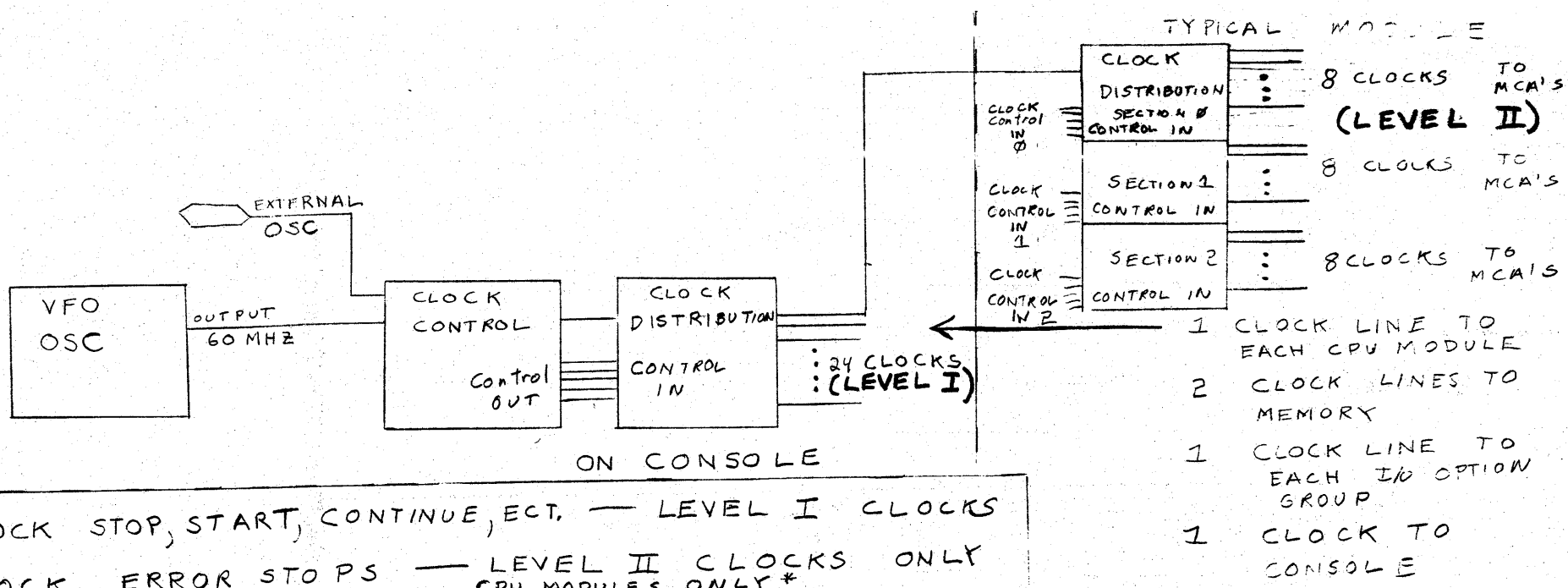
BIT 00 - CLK7 INHIBIT SECTION 0 H - Disables clock outputs from section 0.

BIT 01 - CLK7 INHIBIT SECTION 1 H - Disables clock outputs from section 1.

BIT 02 - CLK7 INHIBIT SECTION 2 H - Disables clock outputs from section 2.

BIT 03 - CLK7 EXT PHASE L - When low the EXT PHASE A NEXT H signal will be used for phase information rather than the MCA determining the phase information internally.

BIT 04 - CLK7 CLEAR ERROR H - Assertion of this bit while clocks are runnin will clear the CLOCK ERROR FLAG H.



CLOCK STOP, START, CONTINUE, ECT. — LEVEL I CLOCKS

CLOCK ERROR STOPS — LEVEL II CLOCKS ONLY
CPU MODULES ONLY*

Nominal Frequency - LEVEL I - 60 MHZ
LEVEL II - Selectable

CLOCK RATE SELECT — LEVEL I

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* CAN BE DONE ON ANY CLOCK FOR F.S. support — Could destroy files.