MAINDEC 3

ADDRESS TEST PROGRAM

Abstract: Address test is a utility program designed to test the performance of the Type 12 memory module address selection. The program comes in two parts, a high and low test.

Although not specifically designed to test the Type 15 memory extend switch, it is compatible with multi memory machines in the sense that it can be read into any memory bank.

The program detects both multiple addressing and failure to address in all 4096 locations of each memory tested.

The high part checks from address 0000 of memory "0" to 7747 of the memory into which it was read and the program occupies register 7750 to 7777.

The low part checks from address 25 to address 7777 of the memory in which it was read and occupies register 0 - 24.

CHAPTER 1

CONSOLE OPERATING PROCEDURE

The five tables below describe the console operating procedure to be used when running the Address Test program.

TABLE 1-1 TAPE REQUIRED

Address Test Tape

TABLE 1-2 SWITCH

a) No sense switches or T.W. switches are used.

b) Set Test Address Switches to appropriate memory field.

TABLE 1-3 LOAD SEQUENCE

a) Place tape in Reader and depress read-in -- the jmp is performed automatically to location 7750.

b) If part one runs, load part 2 by depressing read-in -- the jmp is performed automatically to register 0. The cycle time is approximately 385MS.

TABLE 1-4 ERROR HALTS

Error No.	Contents of MA	Cause of Error
Errhlt 1	7772	There has been an address failure. The AC contains the memory field and address of the register being tested. The IO register contains the contents of the register shown in the AC. If IO = O it is probable the X and Y lines for the address specified were not activated.

TABLE 1-4 ERROR HALTS (continued)

Error No.	Contents of MA	Cause of Error
		If IO = AC the error occured after the load IO instruction; that is, in the actual testing. Manually examine the contents of memory, if they are unchanged it indicates a failure of the SAS inst. at location 7771 - any other address in the IO suggest multiple addressing.
Errhlt 2	0017	Memory failure. AC Bits 6 - 17 contain the address being tested. AC Bits 0 - 5 should = 0, if other probable cause is a bad sense amplifier or inhibit driver. If IO = O Errhlt 1. If IO = AC see Errhlt 1. If any IO Bits between 0 - 5 are on a one probable failure of sense amplifier or inhibit driver.

TABLE 1-5 POST ERROR RESTART PROCEDURES

The operator should record all pertinent information about the error, AC and IO contents.

Depressing continue will resume checking from the error location. Restarting will start checking at the lowest memory location. In either case the pattern will be restored.

CHAPTER 2

SUGGESTED APPLICATION OF THE ADDRESS TEST PROGRAM

MODIFICATION OF PROGRAM FOR TROUBLE SHOOTING PURPOSES

If the high portion is started at 7751 instead of 7750 the extend will be off and checking will occur in only one memory.

If it is desirable to check only a portion of memory, this may be accomplished by modification of the start and stop address. Start address is the number N-1 stop address is the number N.

Example: To test only register 100.

Start = LAW 77

Stop = 100

High Test Start location = 7755

High Test Stop location = 7777

Low Test Start location = 2

Low Test Stop location = 24

CHAPTER 3

PROGRAM DESCRIPTION

Address test is a utility program to test the address selection of Type 12 memory module. Depressing READ-IN will load the high part into the memory specified by the TEST ADDRESS switches. The program is then executed by the computer.

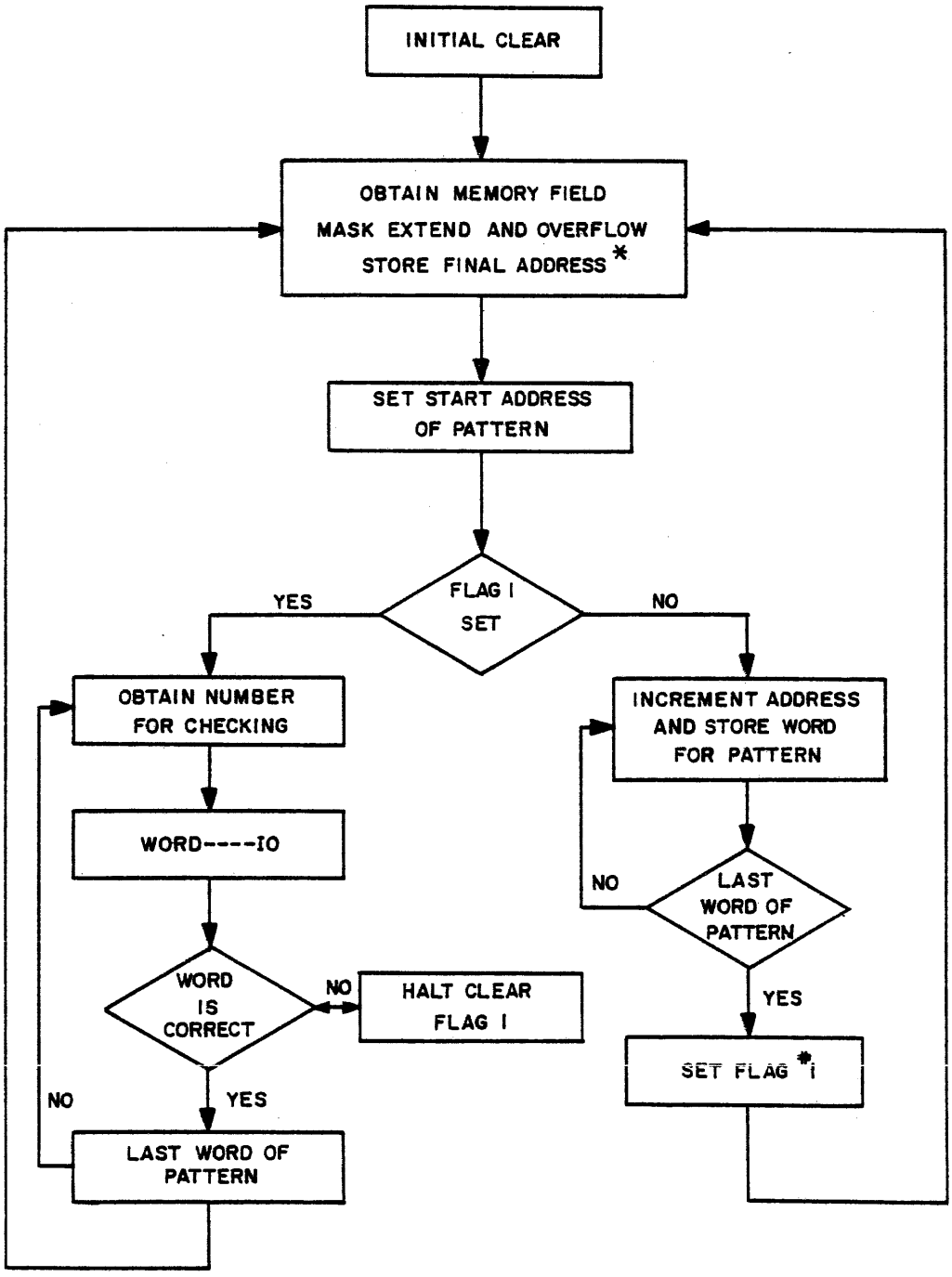
The program sets the extend mode and clears all flag. A PC to AC transfer determines what memory the program has been read into. It then stores a start address of location 0 memory 0, a stop address of 7747 in the memory into which it was read.

Program flag one is tested for "0" and the program goes into a loop that makes the contents of each word between the start and stop address equal to the address of the word.

Flag one is set, start and stop address are initialized. The program now compares the contents of each word against a counter in location 7747. The program remains in the checking routine until an error or manual intervention stops it.

Upon finding an error the AC contains the location of the register being checked, the IO is equal to the contents of the register. Depressing continue will resume checking and generate the pattern again when the start and stop address are equal.

The low portion of address test is very similar to the high, the primary difference is that it checks only the memory into which it has been read.



*THESE STEPS USED WITH HIGH ADDRESS TEST ONLY

Figure 3-1 Address Test diagram

PROGRAM LISTING

MAINDEC 3 HIGH ADDRESS TEST PROGRAM

Location	Contents	Mnemonic Code	Remarks
7750		7777	Set extend to one
7750	724074	lem	Set extend to one
7751	760007	clf	~~Set extend to one~~ clear all flags
7752	764300	opr 4300	
7753	027776	and 7776	Clear IO, PC to AC transfer
7754	307777	dip 7777	Mask OV and EXT
7755	710001	law i 0001	Start Stop address
7756	247747	dac 7747	Store start address
7757	640001	szf 1	If flag set go to checking
7760	607767	jmp 7767	
7761	447747	idx 7747	Pattern generator
7762	257747	dac i 7747	Store word for pattern
7763	527777	sas 7777	Test for end of pattern
7764	607761	jmp 7761	Return to generate next word
7765	760011	stf 1	End of generating pattern
7766	607752	jmp 7752	And initialize for checking
7767	447747	idx 7747	
7770	237747	lio i 7747	Contents of word for operator
7771	537747	sas i 7747	Test for accuracy
7772	760401	hlt 1	Errhlt 1 AC = Register IO = error content
7773	527777	sas 7777	Test for end of pattern
7774	607767	jmp 7767	Check next word
7775	607752	jmp 7752	Repeat test
7776	177777		Address of the word written or checked
7777	007747		Final address of program

PROGRAM LISTING

MAINDEC 3 LOW ADDRESS TEST PROGRAM

Location	Contents	Mnemonic Code	Remarks
0000	720074	lem	Initial clear
0001	760007	clf 7	
0002	700024	law 24	
0003	240023	dac 23	Store start address
0004	640001	skp 1	If set go to checking
0005	600014	jmp 14	
0006	440023	idx 23	Increment
0007	250023	dac i 23	Store word
0010	520024	sas 24	Test for last word
0011	600006	jmp 6	
0012	760011	stf 1	Initialize for checking
0013	600002	jmp 2	
0014	440023	idx 23	Obtain number and increment word
0015	230023	lio i 23	Load word for operator
0016	530023	sas i 23	Test word for accuracy
0017	760401	hlt 1	Errhlt 2 AC = Register IO = contents
0020	520024	sas 24	Test for final address
0021	600014	jmp 14	Check next word
0022	600002	jmp 2	Repeat program
0023	0		
0024	7777		