digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

EC DEC-O-LOG Engineering Change Order Log

M7236

KT11-D Memory Management

PROCESSOR TYPE PDP-11/40

M7236-00001 CODE: D CS: A ETCH: B

NOV-72 - PROBLEM 1: KD11-A signal **K2-3 BUPP8 H** has a loading problem.
CORRECTION 1: Eliminate one load of **K2-3 BUPP8 H** in KT ROM logic.
PROBLEM 2: Etch board has etch errors and pinning errors.
CORRECTION 2: Rework module as indicated by description of change.
PROBLEM 3: Clocking of **KT-2 PS 15:12 DATA** may be late.
CORRECTION 3: Gate **KT-6 P CLK MSYN H** with explicit clocking logic.
PROBLEM 4: Incorrect stack selection during KT instruction.
CORRECTION 4: Select appropriate stack using multiplexed signal.
PROBLEM 5: Incorrect disable of W BIT clocking.
CORRECTION 5: Disable clocking of W BIT on PAR or PDR access before **MSYN** is asserted.
PROBLEM 6: Physical bus access, **DATI** from console not made.
CORRECTION 6: Store SBC EQUALS 10 for appropriate time to enable **DATI** from console switch register in CONSOLE MODE .
PROBLEM 7: Incorrect resistor pull-ups for 8881 on KT-6.
CORRECTION 7: Replace resistors R3 and R4 with 10K ohm, 1/4W resistors; update print KT-6 and Parts List accordingly.
PROBLEM 8: Internal register clocking logic one-shot delays incorrect.
CORRECTION 8: Replace capacitors C111, C112, and C113 with 33 pfd 100V 5% capacitors; update Parts List accordingly.
PROBLEM 9: Processor VIRTUAL PAGE 7 always hardware mapped to external peripheral bank.
CORRECTION 9: Inhibit VIRTUAL PAGE 7 being mapped to external bank by disabling **BA 17:16 MUX** when memory management enabled, **KT-3 RELOCATE 1 H** .

NOTE: This ECO creates M7236 DD revision "A ".
In-plant effectivity -03 rework immediately

M7236-B0002 CODE: DF CS: B ETCH: C

JAN-73 - PROBLEM 1: Incorrect KT B14A2 ROM word.
CORRECTION 1: Replace KT ROM B14A2 with B38A2.
PROBLEM 2: Trap caused by MEMORY MANAGE on power-up.
CORRECTION 2: Inhibit **KT-3 FAULT H** when MEMORY MANAGE not enabled.
PROBLEM 3: KT11-D Parts List doesn't include capacitors to extend KD11, K4, **BUS MSYN L** and **MSYNA H** .
CORRECTION 3: Add capacitors C106 and C107 to KT11-D Parts List.
PROBLEM 4: Print errors in IC pin designations.
CORRECTION 4: Correct prints as detailed in this FCO.
CORRECTION 5: Add device truth tables 74153, 74157 and 1311003-02 to prints.

NOTE 1: See correction supplement FCO M7236-B002A.

NOTE 2: This FCO creates M7236 DD revision "B ".
In-plant effectivity -03 rework immediately
Field effectivity -Rework all M7236's
(Time To Install And Test 3.0 Hours.) (Kit Contents -FCO/Prints And Parts) Supplement M7236-B002A will also be included in the kit.

M7236-B002A CODE: DF

JAN-73 - PROBLEM: Incorrect chip location given in FCO M7236-B0002 rework procedure.
CORRECTION: Change chip number designation in description of change in rework procedure from E75 to E53.
In-plant effectivity -Unchanged
Field effectivity -Unchanged

M7236-B0003 CODE: F CS: C

MAR-73 - PROBLEM: A bus error trap in USER MODE results in the vector PSW being taken from user space and not kernel; incorrect B38A2 ROM word.
CORRECTION: Install new ROM, B39A2, with correct control patterns to enable trap vector to always be accessed in kernel space.

NOTE: This FCO creates M7236 DD revision "C ".
In-plant effectivity -03 * install immediately on machines for RSX11-D test installations. Phase-in: All machines into Acceptance 4/15.
Field effectivity -Rework all M7236's in KT11-D's
(Time To Install And Test 1.0 Hour.) (Kit Contents -FCO/Prints And Parts)

M7236-B0004 CODE: F CS: D ETCH: D

OCT-73 - PROBLEM: When doing a CMP B or BIS B instruction with the "T " bit set, the PDP-11/35 and PDP-11/40 CPU's will execute a false Memory Management Trap before the Trace Trap. This is due to the signal **KT-3 FAULT L** being true when microword TRP04, ROM word 010 in the CPU, is executed, causing the microprogram to branch to TRP05 instead of TRP02.
CORRECTION: Disable the signal **KT-3 FAULT L** unless one of the memory management error flags is set. The rework procedure is as follows: Cut etch on side 1 running from E63 pin 5 to E61 pin 6. Cut etch on side 1 running from E63 pin 6 to module pin C08R1. Add wire from E75 pin 3 to etch running to module pin C08R1. Add wire from E75 pin 2 to E61 pin 6. Add wire from E75 pin 1 to E73 pin 13.

NOTE: This FCO creates M7236 DD revision "D ".
In-plant effectivity -Rework all M7236's immediately.
Field effectivity -Rework all M7236's in all PDP-11/35's and PDP-11/40's with memory management.
(Time To Install And Test 1.0 Hour.) (Kit Contents -F1070 -FCO/Prints)