DATASYSTEMS™

DLP-11 LINE PRINTER CONTROLLER

REV. C

TECHNICAL MANUAL

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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The DATASYSTEMS DLP-11 Line Printer Controller provides an interface between Digital Equipment Corporation (DEC) PDP-11 Series or VAX Series machines and any Centronics, Dataproducts, or LA180 compatible line printer. Among the unique features of the DATASYSTEMS DLP-11 is self test capability which aids installation and trouble shooting by verifying the proper operation of the DLP-11, cable, and printer. The DLP-11 is also switch configurable, eliminating the need to cut trace and jumper wires to alter the controller's address, and most options. The DLP-11 also has an optional Long Lines (LL) capability which is compatible with the Dataproducts long lines standard for cable lengths in excess of 50 feet.

1.2 FUNCTIONAL DESCRIPTION

The DATASYSTEMS DLP-11 Line Printer Controller is LP-11/LS11 compatible and completely software transparent. In the self-test mode, the DLP 11 generates a 96-character ASC11 code set and sends it to the printer. The DLP-11 controller

will output all characters received to the line printer without requiring software or hardware modifications to the host PDP-11.

1.3 PHYSICAL DESCRIPTION

The DATASYSTEMS DLP-11 Line Printer Controller is a double size (10.5"x8.5") module and occupies one position in the quad size H9270 and DDV11-B type backplane or the double size H9281 type backplane. For the standard Centronics or Dataproducts interface, a 15 foot cable is provided for the specified line printer type. The connector type used on Centronics compatible cable is an AMPHENOL 57-30360. The connector types used on the Dataproducts compatible cable are either a WINCHESTER MRACP50P or an AMP 205212-1. For Dataproducts long lines interface, a 6 foot internal cable is provided as well as a 37 pin male D-subminiature connector and a Winchester MRACP50P connector to facilitate customer cabling. All cables mate with the header connector on the controller board, a 3M 3431-1202.

1.4 SYSTEM SPECIFICATIONS

The following specifications describe the DLP-11 Line Printer Controller.

1.4.1 Bus Interface

Compatible with any Digital Equipment Corporation PDP-11 Series or VAX Series CPU, except PDP-11/03.

1.4.2 Printer Interface

Compatible with Centronics, Dataproducts, LA180, or any printer emulating one of these. Also, as an option, compatible with the Dataproducts long lines interface.

1.4.3 Parallel Data Transfer Rate

400,000 Bytes per second

1.4.4 Logic

Low Power Schottky TTL/MSI

1.4.5 Power

5 volts at 1.0 amperes

1.4.6 Size

One quad board

1.4.7 Weight

10 ounces (not including cable)

1.4.8 Environment

A. Operational at 0° to 55° C.

B. Storage -65° to 100° C

C. Humidity 10% to 90% (non-condensing)

SECTION II

INSTALLATION AND OPERATION

2.1 CONFIGURATION

The DATASYSTEMS DLP-11 Line Printer Controller is shipped with the DIP switches set to the configuration specified by the user. Check to insure that the controller is configured as desired (refer to Section III for configuration details).

CAUTION: IF THERE IS ANY EVIDENCE OF PHYSICAL DAMAGE, DO NOT INSTALL THE BOARD.

2.2 BOARD PLACEMENT

CAUTION: TURN OFF THE POWER TO THE PROCESSOR BEFORE INSTALLING THE BOARD.

1. Select the slot position in which the DLP-11 controller is to be installed. (Line Printer Controllers are usually located near the end of the interrupt chain.) Check to insure that the slot chosen is an SPC Slot (Small Peripheral Controller) in the chassis.
2. Remove the G727 Grant Continuity module from Slot D of the selected slot.
3. Insert the DLP-11 board into slots C, D, E, and F at the desired location. Always replace the Grant Continuity Module, G727, when the DLP-11 board is removed.

2.3 PRINTER CONNECTION

The DLP-11 will support standard Centronics, Dataproducts, and LA180 compatible printers. As an option, the DLP-11 will support the Dataproducts long lines interface. The method of connection is different for printers using the long lines interface. Follow the appropriate procedure below.

2.3.1 Standard Centronics, Dataproducts, LA180 Interface

1. Plug the printer cable supplied with the controller into connector P1 on the front of the DLP-11 board. Align arrow on cable connector with arrow on printer circuit board connector before attempting to insert.

2. Connect the opposite end of the cable to the line printer. (Refer to the printer manufacturer's instructions for unpacking and installing the line printer.)

3. Apply power to the computer and line printer.

4. Place the printer ON-LINE and set the DLP-11 self test switch (SW1) to ON. The line printer should operate and repeatedly print a 96-character ASCII pattern followed by carriage return and line feed.

In the event the printer does not respond, check the strap options in the printer and recheck the configuration of the

DLP-11. Failures may be due to a malfunctioning controller, line printer, or cable.

2.3.2. Dataproducts Long Lines Interface

1. Add a capacitor (C25) in location 8A. The proper value will be found in Dwg. No. 46-000011 "LONG LINES OPTION SPECIFICATION".

2. Plug the short internal cable into P2 on the DLP-11. Note: The cable assembly is keyed. Align arrow on cable connector with arrow on printed circuit board connector before attempting to insert.

3. Observe that the free end of the internal cable is a 37 pin male D subminiature connector. Its mate was included with the DLP-11 along with a printer connector to facilitate customer cabling. (Note: Most long lines applications require cable to be routed through conduit prior to assembling connectors.) Route long cable, assemble connectors, and attach long cable between printer and short internal cable.

4. Apply power to the computer and line printer.

5. Place the printer ON-LINE and set the DLP-11 self test switch (SWI) to ON. The line printer should operate and repeatedly print a 96-character ASCII pattern followed by a carriage return and line feed.

In the event the printer does not respond, check the strap options in the printer and re-check the configuration of the DLP-11. Failures may be due to a malfunctioning controller, line printer, or cable.

2.4 OPERATION

The DLP-11 operates completely under software control except when in the self-test mode. For normal operation, the self-test switch (SWI) should be OFF. The DLP-11 is shipped with default values set for both Addressing and Vector locations. The default values for the controller are as follows:

Status Register = 177514_8
Data Register = 177516_8
Vector Location = 200_8

These values are set to the standard addresses used by DEC. Refer to Section III for non-standard addressing.

SECTION III

CONFIGURATION

3.1 ADDRESSING SWITCHES

There are three 8-position switch packs on the DLP-11. These are located at locations D4, E4, and F4. A switch in the "ON" position represents a binary 0 and a switch in the "OFF" position represents a binary 1. (See Figure 3.2 for switch assignments.)

3.2 PRINTER SELECTION

The DLP-11 will support Centronics, Dataproducts, and LA-180 printer interfaces. There are 3 switches at location F4 which control printer selection (F4-3, F4-4, F4-5). Figure 3.1, below, shows proper setting of switches for specific printer. (Note: F4-2 "ON" for Long Lines ONLY.)

PRINTER INTERFACE	SWITCH #: LABEL:	F4-3 DR	F4-4 C/DSEL	F4-5 LA-180
Centronics		OFF	OFF	ON
Dataproducts		OFF	ON	ON
LA-180		OFF	OFF	OFF
Printronix Dataproducts		OFF	ON	ON
Printronix Centronics		OFF	OFF	ON

Figure 3.1 Printer Selection

SECTION III

CONFIGURATION

3.1 ADDRESSING SWITCHES

There are three 8-position switch packs on the DLP-11. These are located at locations D4, E4, and F4. A switch in the "ON" position represents a binary 0 and a switch in the "OFF" position represents a binary 1. (See Figure 3.2 for switch assignments.)

3.2 PRINTER SELECTION

The DLP-11 will support Centronics, Dataproducts, and LA-180 printer interfaces. There are 2 switches at location F4 which control printer selection (F4-4 and F4-5.) Figure 3.1, below, shows proper setting of switches for specific printer. (Note: F4-2 "ON" for long lines ONLY.)

PRINTER INTERFACE	SWITCH #: LABEL:	F4-4 C/DSEL	F4-5 LA-180
Centronics		OFF	ON
Dataproducts		ON	ON
LA-180		OFF	OFF

3.3 STATUS REGISTER ADDRESS SELECTION

Switches 1 through 8 at D4 together with switches 1, 2, and 3 at E4 perform the status register address selection. Switch number 1 at D4 selects the 12th address bit. This is the most significant selectable address bit. Bits 13 through 17 of the status register address are assumed to be 1's. Switch number 3 at E4 selects the 2nd address bit. This is the least significant selectable address bit. Bits 1 and 0 of the status register address are assumed to be 0's. (See Section 3.6 for configuration example.)

3.4 DATA REGISTER ADDRESS SELECTION

The data register address is assumed to be the status register address plus 2.

3.5 VECTOR ADDRESS SELECTION

Switches 4 through 8 at E4 together with Switch 1 at F4 perform the vector address selection. Switch Number 4 at E4 selects the 7th address bit. This is the most significant selectable address bit. Bits 8 through 15 of the vector address are assumed to be 0's. Switch Number 1 at F4 selects the 2nd address bit. This is the least significant selectable address bit. Bits 1 and 0 are assumed to be 0's. (See next section for configuration example.)

D4	1	Status Address Bit 12	(Most Significant Bit)
	2	Status Address Bit 11	
	3	Status Address Bit 10	
	4	Status Address Bit 9	
	5	Status Address Bit 8	
	6	Status Address Bit 7	
	7	Status Address Bit 6	
	8	Status Address Bit 5	
E4	1	Status Address Bit 4	
	2	Status Address Bit 3	
	3	Status Address Bit 2	(Least Significant Bit)
	4	Vector Address Bit 7	(Most Significant Bit)
	5	Vector Address Bit 6	
	6	Vector Address Bit 5	
	7	Vector Address Bit 4	
	8	Vector Address Bit 3	
F4	1	Vector Address Bit 2	(Least Significant Bit)
	2	Long lines Enable	
	3	***NOT USED***MUST BE OFF***	
	4	Centronics/Dataproducts Selection	
	5	LA-180 Selection	
	6	***NOT USED***	
	7	On for UNIX for operating system only	
	8	Data Bit 8 Disable	

3.6 CONFIGURATION EXAMPLE

The standard addresses expected by the DEC software are:

Status Register Address : 177514 (base 8)

Data Register Address : 177516 (base 8)

Vector Address : 200 (base)

The switch settings to select these addresses are as follows:

3.6.1 STATUS REGISTER ADDRESS

SWITCH LOCATION	SWITCH NUMBER	SWITCH SETTING	ADDRESS BIT	BIT VALUE	OCTAL
NOT SELECTABLE		--	0	0	
NOT SELECTABLE		--	1	0	4
E4	3	OFF	2	1	
E4	2	OFF	3	1	
E4	1	ON	4	0	1
D4	8	ON	5	0	
D4	7	OFF	6	1	
D4	6	ON	7	0	5
D4	5	OFF	8	1	
D4	4	OFF	9	1	
D4	3	OFF	10	1	7
D4	2	OFF	11	1	
D4	1	OFF	12	1	
NOT SELECTABLE		--	13	1	7
NOT SELECTABLE		--	14	1	
NOT SELECTABLE		--	15	1	
NOT SELECTABLE		--	16	1	7
NOT SELECTABLE		--	17	1	

3.6.2 DATA REGISTER ADDRESS

The Data Register Address is equal to the Status Register Address, 177514, plus 2 or 177516.

3.6.3 VECTOR ADDRESS

SWITCH LOCATION	SWITCH NUMBER	SWITCH SETTING	ADDRESS BIT	BIT VALUE	OCTAL
NOT SELECTABLE		--	0	0	
NOT SELECTABLE		--	1	0	0
F4	1	ON	2	0	
E4	8	ON	3	0	
E4	7	ON	4	0	0
E4	6	ON	5	0	
E4	5	ON	6	0	
E4	4	OFF	7	1	2
NOT SELECTABLE		--	8	0	
NOT SELECTABLE		--	9-15	0	0

3.7 LONG LINES

Switch Number 2 at F4 performs the selection of long lines operation. This switch functions only if the long lines option is installed on the DLP-11. If the option is NOT installed, the switch should be in the "OFF" position.

This switch in the "ON" position enables the long lines option allowing communications with printers using differential receiver/drivers. (See also Section 2.3.2.)

3.8 DATA BIT 8 DISABLE

Switch Number 8 at F4 performs the function of enabling Bit 8 out to the printer. Bit 8 is normally enabled. This is done by setting switch 8 to the "OFF" position. To disable Bit 8, set switch 8 "ON".

3.9 BUS REQUEST PRIORITY SELECTION

The bus request priority jumpers are located at E1 and F1 on the circuit board. The board comes factory set for level 4. To alter this to an arbitrary level X, perform the following procedure:

I. At BGI, BGO, and $\overline{BR}$
   - A. Cut the trace for level 4.
   - B. Jumper a wire for level X.

II. At BGI/O
   - A. Jumper a wire for level 4.
   - B. Cut the trace for level X.

SECTION IV

PROGRAMMING

4.1 GENERAL

The DATASYSTEMS DLP-11 Line Printer Controller is software compatible with the Digital Equipment Corporation LP11 and LS11 line printer options available for the PDP-11 series minicomputers. For additional information on programming refer to the DEC Peripheral Handbook.

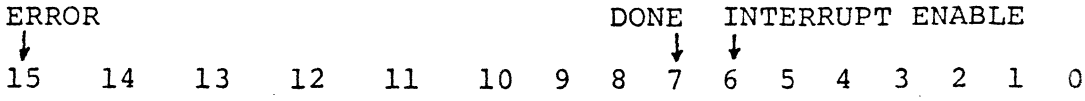
The DLP-11 supports up to eight data lines for communication from the processor to the line printer. This permits full ASC11 code transmission plus either paper instruction or Bit 8 information. The information to be sent to the line printer is loaded into bits 0-7 of the character buffer. The least significant bit is zero. After each character is loaded into the printer buffer, the line printer DONE (Bit 7) appears in the status register.

The maximum data transfer rate between the DLP-11 controller and the line printer is 400 KB per second. If Bit 8 is not used, it may be disabled by a switch on the DLP-11 controller.

4.2 STATUS REGISTER

Address = 777514_8 Default

Address Range = 160000_8 - 777774_8



NAME	BIT	FUNCTION
ERROR	15	Set when one or all of the following conditions exists: 1) Power OFF 2) No Paper 3) Printer Off Line or unavailable.
DONE	7	Set when the printer is ready to receive the next character
INTERRUPT ENABLE	6	Set to allow a DONE or ERROR condition to generate an Interrupt.

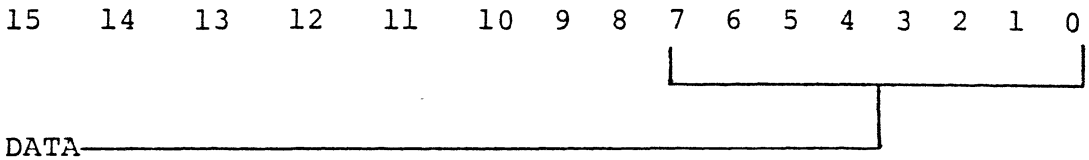
4.3 SYSTEM INITIALIZATION

When the computer performs a hardware reset either by power on or from front panel instructions, bit 6 (Interrupt Enable) is reset and Bit 7 (Done) is set (if no error exists). Bits 15 and 7 are read only information. Interrupt Enable and Done are also reset when self-test is enabled.

4.4 DATA REGISTER

Address = 777516_8 Default

Address Range = 160002_8 - 777776_8



Bits 0-6 contain the character information in ASCll with Bit 0 being the least significant bit. Bit 7 is used as either a Paper Instruction line or as a data line if it is necessary to pass eight bits to the line printer.

4.5 PRIORITY AND INTERRUPT LEVELS

The DLP-11 is set with interrupt vector = 200_8, the standard for DEC software. The Bus Request level is set to four (4), also standard.

SECTION V

THEORY OF OPERATION

5.1 INTRODUCTION

This section describes the DLP-11 Line Printer Controller theory of operation. Refer to Appendix A (sheets 1 through 5) for schematic representation of the DLP-11.

5.2 DEVICE SELECTION

The DLP-11 occupies two consecutive addresses; one for the status register and one for the data register. The Unibus has 18 address lines labeled A0 through A17. They are shown on sheet 1. They are buffered by 26S12A receivers and fed into two 6-Bit Comparators. The address lines are compared against switches A12 through A2, if they match ADDE goes active. ADDE, C1, and A1 feed a 3 to 8 decoder which is enabled at MSYC time. The decoder supplies the read/write commands to the rest of the controller. The command lines are then OR'ed to acknowledge receipt of a command from the CPU.

5.3 INTERRUPT HANDLER

The interrupt circuit (Sheet 3) is enabled by the Interrupt Enable flip-flop (Sheet 2-E2). The clear line or Self-Test Enable clears the flip-flop. Data Bit 6 from the UNIBUS feeds the D input of the flip-flop, so on the positive edge of WTS, the flip-flop loads Bit 6. The output of the Interrupt Enable flip-flop is AND'ed with RDY*ERR to generate an interrupt if either term is active. FI going active starts the interrupt sequence.

When INTR goes active and no interrupt is in progress, Bus Request (BR) goes active. Jumpers E1-E2 prevent interrupt servicing during a direct memory access operation to improve CPU throughput. The function is disabled by jumpering E2-E3. (NOTE: The DLP-11 is shipped with that function disabled.) After BR, the CPU responds with a BGI. BG is delayed by R12, R21, C29 and clocks F2 which sets SACK and disables BR during that time. The CPU acknowledges SACK by clearing BGI.

When BUSY from the current bus master is cleared, H3 is clocked to set BUSY and INTR, making the controller the current bus master. This also enables the current vector information to be loaded on the bus by making INTV active. The vector data is gated by F3 and G3 (Sheet 4) onto the UNIBUS. When the CPU has read the vector information, it returns a SSYC. SSYC is AND'ed with BSY to disable the INTR input, causing H3 to reset, completing the interrupt cycle.

5.4 DATA REGISTER

The 8-bit data word from the CPU is buffered by F3 and G3 (Sheet 4). These buffers first invert the data then feed it into two 4-bit registers, F6 and H6 which latch the data from the UNIBUS. The data is loaded into the latches by the positive edge of WTD, which is derived from the command decoder on Sheet 1. The data is then selectively enabled onto the internal tri-state bus, D1-D7 which functions for self-test and a special character detection circuit. During normal operation, the latches are enabled except when the controller is in the Centronics mode and a line termination is in progress.

5.5 PRINTER BUFFERING

The DLP-11 supports two standards for printer interface. For distances under 50 feet single ended receiver drivers are used. The drivers are 7407 type with 1,000 ohm resistor pullups to +5. The receivers are terminated 220 ohm to +5 and 330 ohm to ground. The receivers are 7414 Schmitt receivers used for improved noise immunity. For distances in excess of 50 feet, the DLP-11 supports an optional long lines differential interface. It is comprised of 75183 differential drivers and 75183 differential receivers with built-in 180 ohm terminations. This method of interface will support Long Lines compatible printers up to 3,000 feet from the host CPU.

5.6 SELF-TEST

Self-test is controlled by enabling two PROM's F7 and H7 onto the internal tri-state data bus (Sheet 4). The PROM's contain a 96-character ASCll set, terminated with a CR, LF. Two 4-bit counters E7 and G7 drive the PROM's to control the loading of the appropriate data onto the bus. While self-test is enabled the two 4-bit latches holding data from the CPU are disabled. The counters driving the PROM's are incremented by ACK which is the acknowledgement from the printer. The counters are cleared by either STE being low or when 134 characters have been sent to the printer. The PROM's also serve to hold a one-character code used by the Special Character Detect circuit.

5.7 SPECIAL CHARACTER DETECT (CENTRONICS ONLY)

As data enters the DLP-ll it is sampled by PROM G6. The PROM checks for FF or LF codes. If either code is detected, B5-9 will go low at WTD time. If the previous character was printable, then B5-8 will have been low, setting D5-2 high so that at WTD time, D5-5 SEL is set. SEL being high releases the CLR of counters E7 and G7. SEL sets the load inputs of the counters low. This addresses the PROM's at F7 and H7 to location 251 (base 10) which contains a "CR" code which is sent out with the current DATASTROBE pulse. On ACK, SEL is

cleared and a false datastrobe is generated by D5-9, which also inhibits the RDY flipflop to prevent an interrupt request.

5.8 STATUS CONTROL

The DLP-11 has 3 bits of status. When the Command Decoder receives a status request, RES goes active, enabling H1 onto the UNIBUS. This places the status information on the bus.

5.9 STROBE GENERATOR

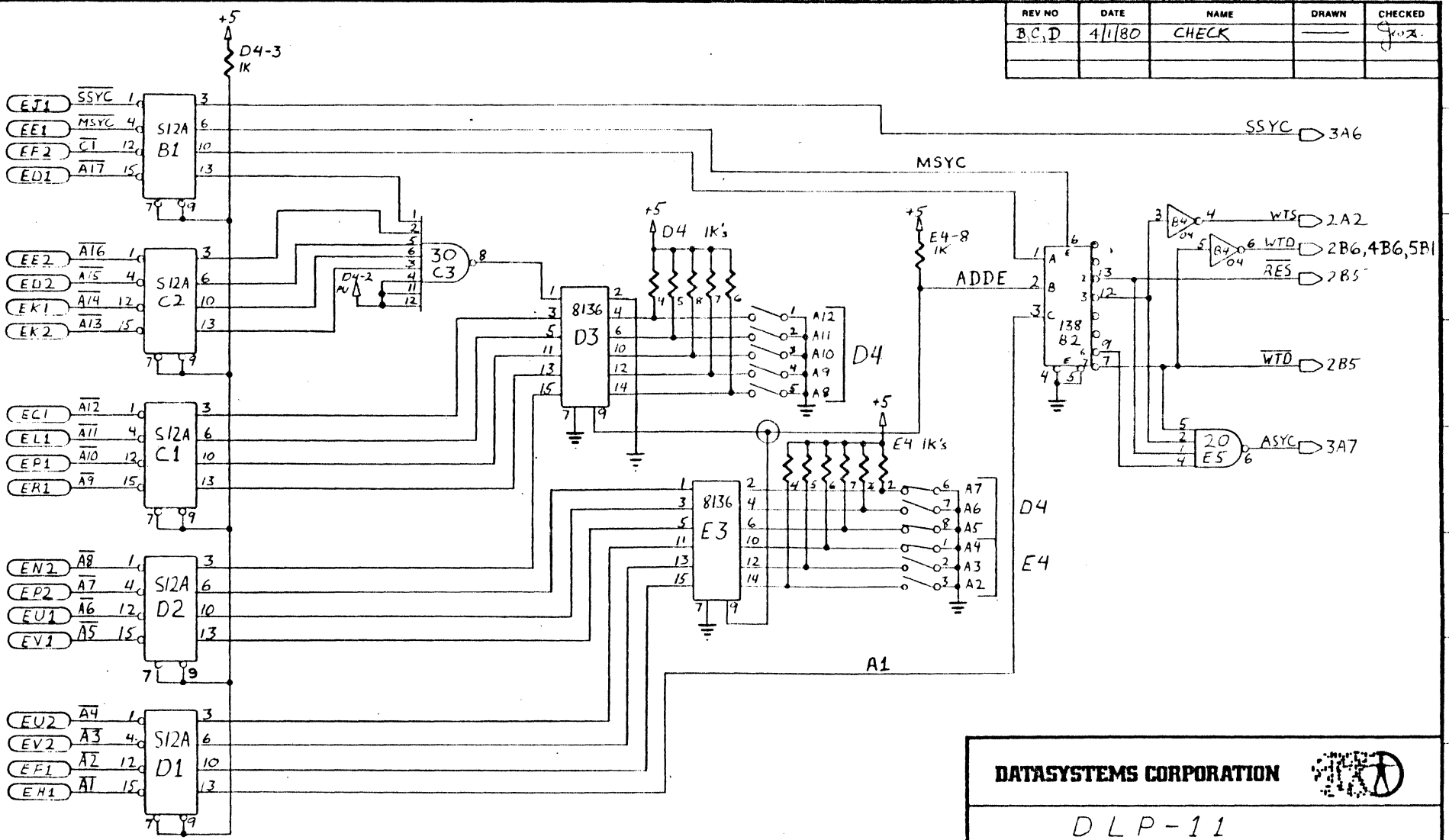
When WTD occurs from the Command Decoder, A8 delays the Data Strobe by 1.5 microsecond to allow data to stabilize on the Data Bus (Sheets 4 and 5). This process is accomplished by coupling two one-shot multivibrators, A8, to delay 1.5 microsecond and generate a 2.0 microsecond strobe pulse which is buffered and routed to the printer, P1-1.

APPENDIX A

SIGNAL MNEMONICS
AND
SCHEMATIC DIAGRAMS
(Sheets 1-5)

SIGNAL MNEMONICS

Name	Description	Location
A17-A1	Address Bus	Sheet 1
ACK	Acknowledge	2H3
ASYC	Acknowledge Sync	1S5
BGI	Bus Grant In	3B3
BGO	Bus Grant Out	3S3
BR	Bus Request	3S2
BSCK	Bus Acknowledge	3S4
C1	Control Write	1B2
CLR	Clear	3D4
D1-D8	Internal Data Bus	Sheet 4
DPS	Dataproducts Select	5N2
DSF	Datastrobe Flag	5M1
DSTB	Datastrobe	5S2
FDST	False Datastrobe	2S6
INIT	Initialize	3A4
INTR	Interrupt Request	2S5
INTV	Interrupt Vector	3S6
MSYC	Master Sync	1B2
NPR	Non Processor Request	3A2
RES	Read Status Command	1S3
SEL	"CR" Select	2S7
STE	Self Test Enable	4J9
SSYC	Slave Sync	1S2
UB0-UB7	UNIBUS Data Lines	Sheet 4
WTD	Write Data Command	1S3
WTS	Write Status Command	1S3



REV NO	DATE	NAME	DRAWN	CHECKED
B,C,D	4/1/80	CHECK	——	

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All resistors 5% ¼W KΩ unless otherwise specified. All capacitors in pf 50V unless otherwise specified.

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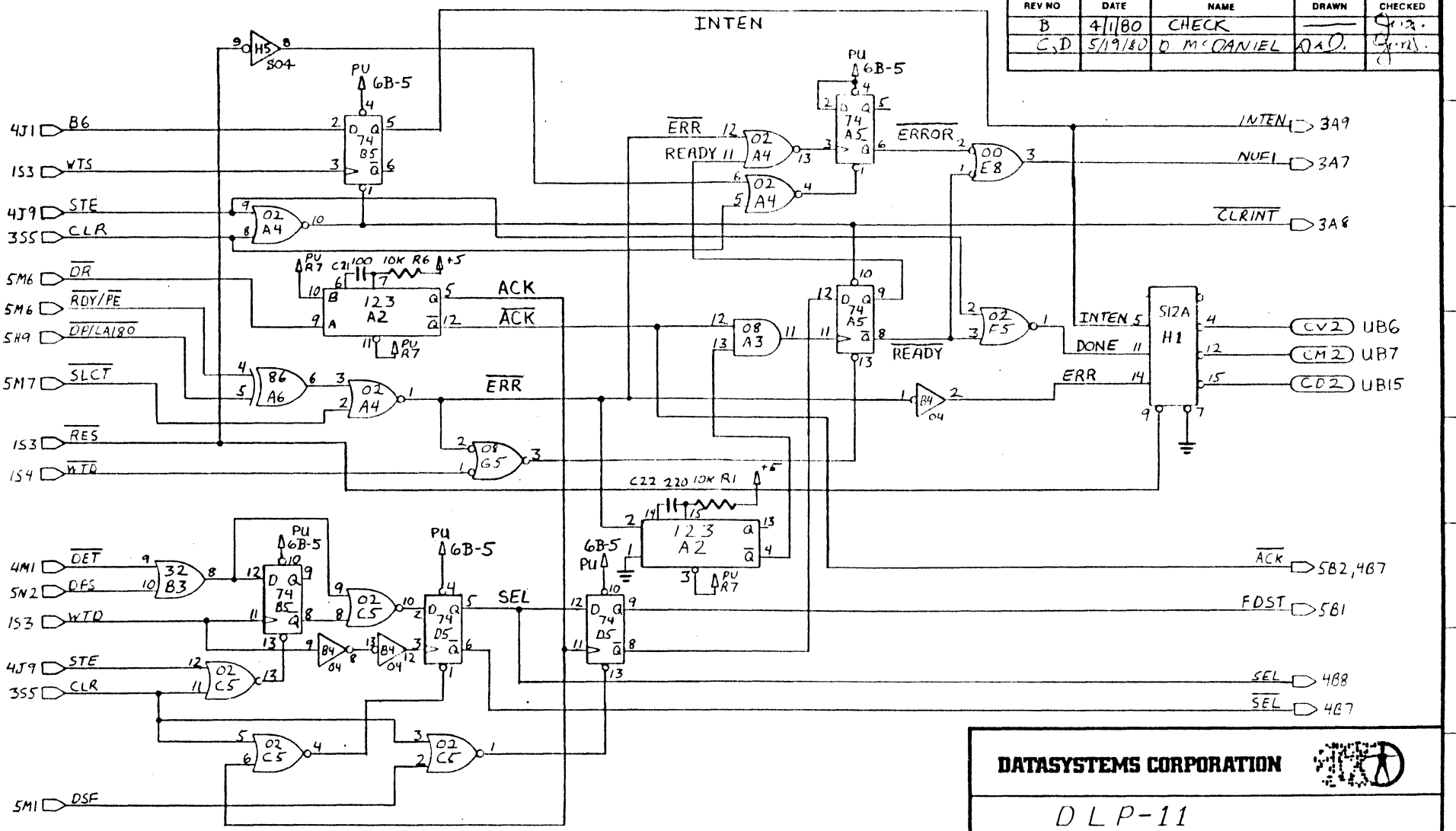
DATASYSTEMS CORPORATION

DLP-11

COMMAND DECODER

DRAWN BY Dean McDaniel	CHECKED J. HACKLANDER		
REV. DATE 4/1/80	DRAWING NO. 51-100000	SHEET 1	OF 5



REV NO	DATE	NAME	DRAWN	CHECKED
B	4/1/80	CHECK	—	
C,D	5/19/80	D McDANIEL	DAD.	

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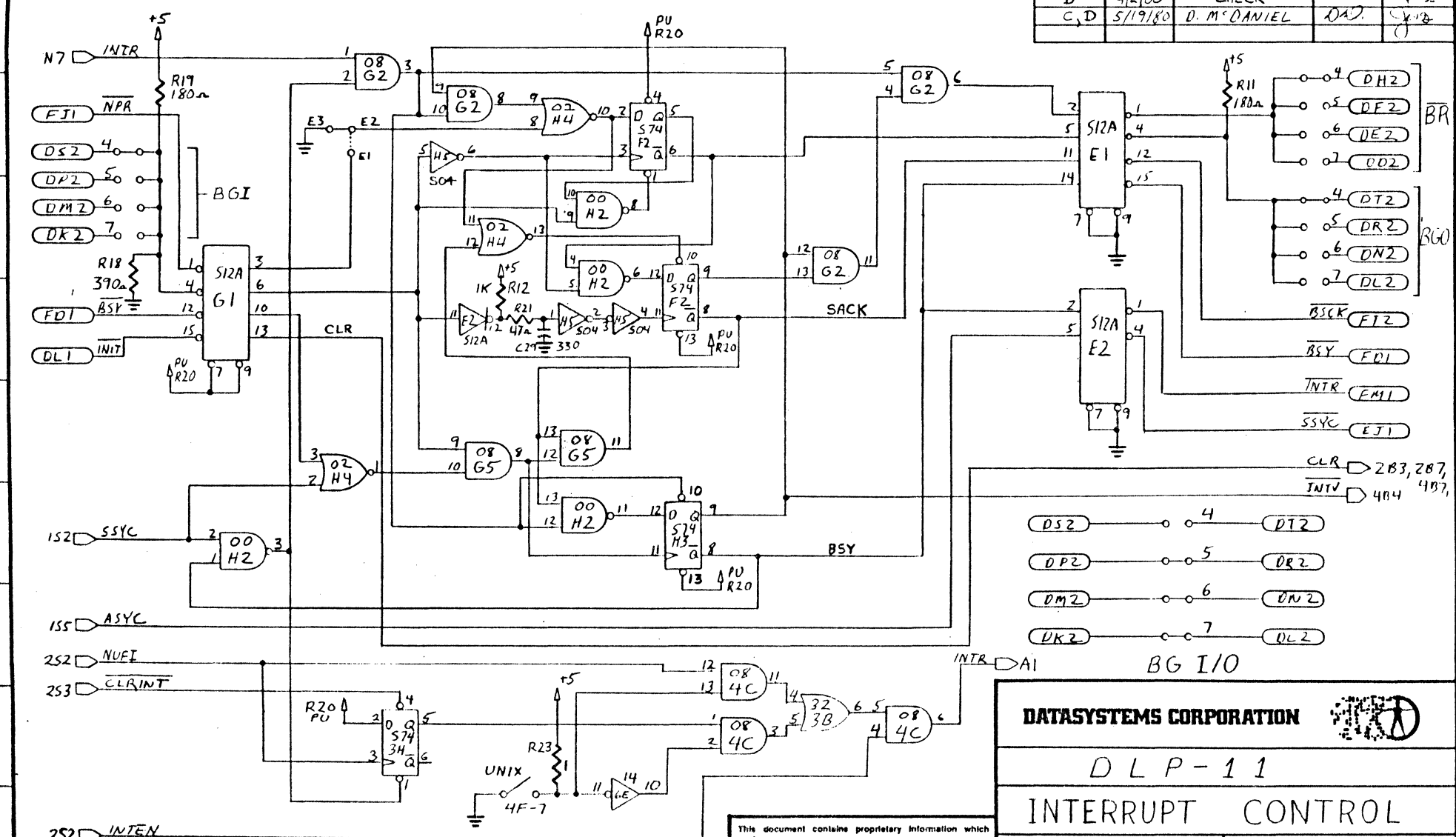
DATASYSTEMS CORPORATION

DLP-11

CONTROL

DRAWN BY	CHECKED	REV. DATE	DRAWING NO	SHEET
Dean McDaniel	J. HACKLANDER	5/19/80	51-100000	2 OF 5

REV NO	DATE	NAME	DRAWN	CHECKED
B	4/2/80	CHECK	—	[illegible]
C, D	5/19/80	D. McDANIEL	DAD	[illegible]



DATASYSTEMS CORPORATION

DLP-11

INTERRUPT CONTROL

DRAWN BY	CHECKED	
Dean McDaniel	J. HACKLANDER	
REV DATE 5/19/80	DRAWING NO 51-100000	SHEET 3 OF 5

All resistors 5% ¼W KΩ unless otherwise specified. All capacitors in pf 50V unless otherwise specified.

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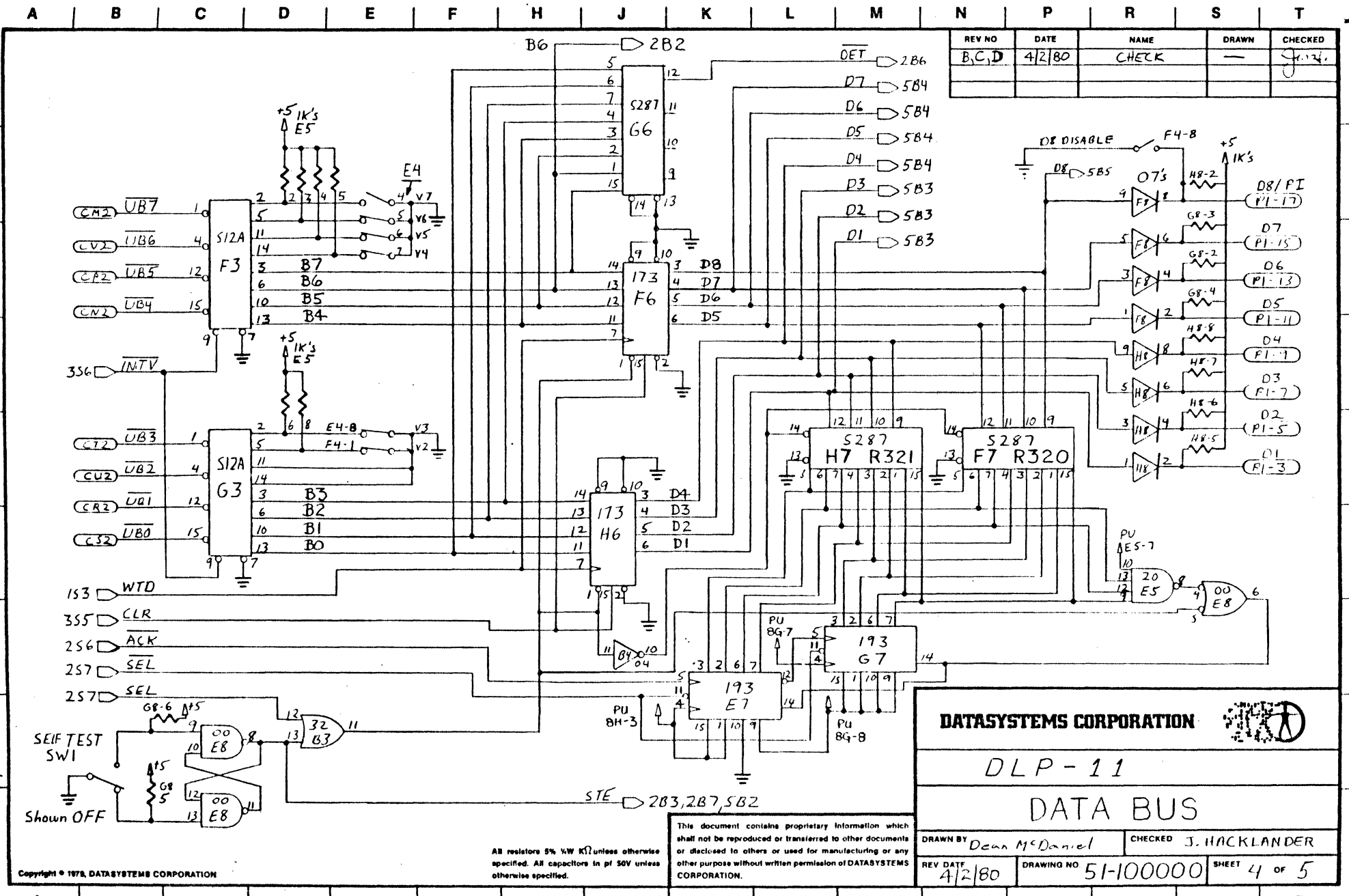

REV NO	DATE	NAME	DRAWN	CHECKED
B,C,D	4/2/80	CHECK	—	J.H.

All resistors 5% ¼W KΩ unless otherwise specified. All capacitors in pf 50V unless otherwise specified.

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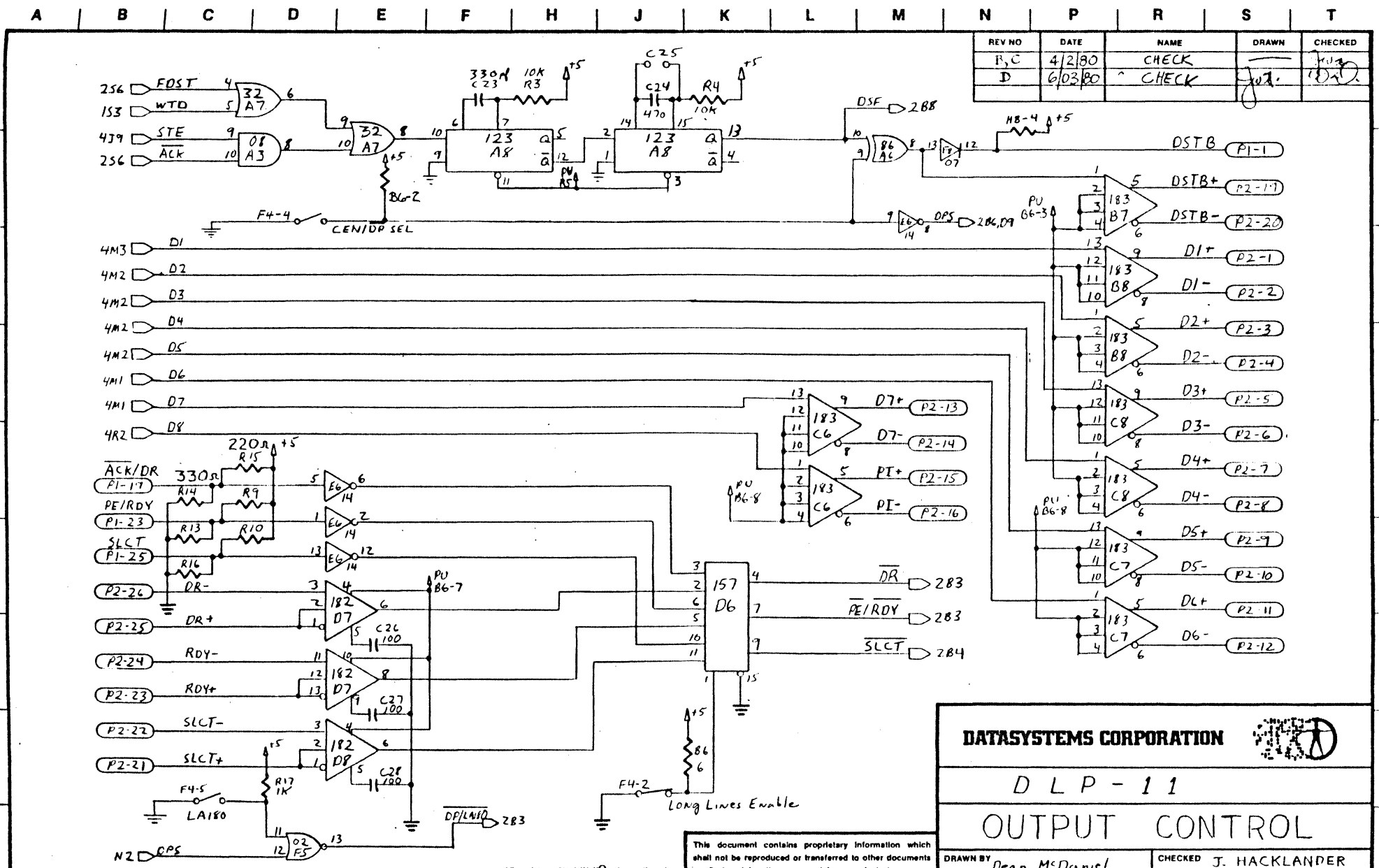
DATA BUS

DRAWN BY	CHECKED	REV DATE	DRAWING NO	SHEET
Dean McDaniel	J. HACKLANDER	4/2/80	51-100000	4 OF 5



REV NO	DATE	NAME	DRAWN	CHECKED
B,C	4/2/80	CHECK	—	
D	6/03/80	CHECK		

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OUTPUT CONTROL

DRAWN BY Dean McDaniel | CHECKED J. HACKLANDER

REV. DATE 5/19/80 | DRAWING NO 51-100000 | SHEET 5 OF 5

All resistors 5% ¼W KΩ unless otherwise specified. All capacitors in pf 50V unless otherwise specified.

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APPENDIX B

CABLE DESCRIPTIONS

CENTRONICS CABLE DESCRIPTION (CCAB-N)

CABLE CONDUCTOR	SIGNAL NAME	AMPHENOL PIN NUMBER
1 (COLORED)	DATA STROBE	1
2	RETURN	19
3	DATA BIT 1	2
4	RETURN	20
5	DATA BIT 2	3
6	RETURN	21
7	DATA BIT 3	4
8	RETURN	22
9	DATA BIT 4	5
10	RETURN	23
11	DATA BIT 5	6
12	RETURN	24
13	DATA BIT 6	7
14	RETURN	25
15	DATA BIT 7	8
16	RETURN	26
17	DATA BIT 8	9
18	RETURN	27
19	ACKNOWLEDGE	10
20	RETURN	28
21	NO CONNECTION	
22	RETURN	29
23	PAPER EMPTY	12
24	NO CONNECTION	
25	SELECT	13
26	NO CONNECTION	
27	RETURN	14
28	NO CONNECTION	
29	NO CONNECTION	
30	NO CONNECTION	
31	RETURN	16
32	NO CONNECTION	
33	NO CONNECTION	
34	NO CONNECTION	

DATAPRODUCTS CABLE DESCRIPTION (DCAB-N)

CABLE CONDUCTOR		SIGNAL NAME	WINCHESTER PIN NUMBER
1	(COLORED)	DATA STROBE	j
2		RETURN	m
3		DATA BIT 1	B
4		RETURN	D
5		DATA BIT 2	F
6		RETURN	J
7		DATA BIT 3	L
8		RETURN	N
9		DATA BIT 4	R
10		RETURN	T
11		DATA BIT 5	V
12		RETURN	X
13		DATA BIT 6	Z
14		RETURN	b
15		DATA BIT 7	n
16		RETURN	k
17		PAPER INSTRUCTION	p
18		RETURN	s
19		DATA REQUEST	E
20		RETURN	H
21		NO CONNECTION	
22		RETURN	EE
23		READY	CC
24		NO CONNECTION	
25		ONLINE	y
26		NO CONNECTION	
27		RETURN	AA
28		NO CONNECTION	
29		NO CONNECTION	
30		NO CONNECTION	
31		RETURN	C
32		NO CONNECTION	
33		NO CONNECTION	
34		NO CONNECTION	