Xerox Sigma Series

The top-of-the-line Sigma 9 system, designed for general-purpose business and scientific applications, offers up to 2 million bytes (524K 32-bit words) of core storage with a 900-nanosecond cycle time.

The Xerox Sigma family of medium-to-large-scale computers has won a small but loyal following in real-time and scientific applications and, to a lesser extent, in business data processing. The Sigma 3, 5, and 6 computer systems have been superseded by newer Xerox systems, leaving the Sigma 9 and Sigma 9 Model 3 as the remaining actively marketed processor models in the series.

MANAGEMENT SUMMARY

Originating with the Sigma 7 computer system, announced in March 1966, the Xerox Sigma series has grown over its eight-year marketing life to include seven processor models, the Sigma 2, 3, 5, 6, 7, 8, and 9. Although all of the processor models remain for sale on an as-available basis, most are no longer actively marketed by Xerox. The small-scale Sigma 2, announced in August 1966, was made obsolete first by the Sigma 3. Both of these 16-bit Sigma systems, in turn, were replaced in the Xerox marketing line-up by the Xerox 530, announced in January 1973. The original Sigma 7 was superseded by the Sigma 6, in 1970, and both the Sigma 5 and the Sigma 6 were finally supplanted by two members of a new Xerox computer family, the Xerox 550 and 560, announced in February 1974.

On the large-scale end of the Xerox family of computers, the Sigma 9 is still actively marketed, and users of the Sigma 8 real-time systems can upgrade to the Sigma 9 Model 3, added to the series in mid-1973. Both the Sigma 9 and the Sigma 9 Model 3 incorporate memory-mapping hardware in their central processor design, thus ➢

CHARACTERISTICS

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MODELS: Sigma 3, 5, 6, 7, 8, and 9.

DATA FORMATS

BASIC UNIT: Although the same 32-bit/word core memory is used in all Sigma processors, the Sigma 3 operates with a 16-bit word (two 8-bit bytes) plus a parity bit, and all the larger models use a 32-bit (four 8-bit bytes) word plus parity bit.

FIXED-POINT OPERANDS: The Sigma 3 uses a 16-bit word, with optional double-precision (32-bit doubleword) arithmetic operations. The larger models all use 32-bit words, with operations performed upon 8-bit bytes, 16-bit halfwords, 64-bit doublewords, and/or immediate operands contained in the instruction words.

FLOATING-POINT OPERANDS: The Sigma 5 and larger models use either a short form, consisting of one word with a 24-bit-plus-sign fraction and 7-bit exponent; or a long form, consisting of two words with a 56-bit-plus-sign fraction and 7-bit exponent. Floating-point hardware is optional on the Sigma 5, 6, and 7, and standard on the 8 and 9. Floating-point hardware is not available for the Sigma 3.

INSTRUCTIONS: The Sigma 3 uses one 16-bit word consisting of a 4-bit Operation Code, 4 bits for Register Designators, and an 8-bit Address Field. The Sigma 5 and larger models use one 32-bit word consisting of a 1-bit code for immediate or indirect addressing, a 7-bit Operations Code, a 4-bit General Register Address Field, and either a 20-bit Value Field Integer (for immediate instructions) or a 3-bit Index Register Address and a 17-bit Reference Address (for indirect address instructions).

INTERNAL CODE: Either 8-bit EBCDIC or 7-bit ASCII is used for internal data representation, with no two printable EBCDIC codes having their seven low-order bits common with one another. ➢

REFERENCE EDITION. This is a mature product line, and no significant further developments are anticipated. Because of its importance, coverage is being continued, but no future update is planned.

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enabling their users to take advantage of the two new virtual-memory operating systems released by Xerox in 1973.

The Sigma 9 Model 3 is a limited version of the Sigma 9 with from 32K to 512K words of storage. Prices of the Sigma 9 Model 3 are substantially lower than those for a Sigma 9 processor, with economies achieved by the selection of features provided in the Model 3 configuration. As a result, the Sigma 9 Model 3 does not include decimal arithmetic facilities, has only two priority interrupt levels instead of the eight priority levels offered on the Sigma 9, and includes as standard only one block of registers. The Sigma Model 3 is designed specifically for real-time processing environments and runs under the Control Program for Real-Time (CP-R).

Market reception of the Sigma series has been good among sophisticated scientific users, but was initially slow in the commercial marketplace. Historically, Xerox (then Scientific Data Systems) introduced the Sigma series as a direct competitor to the IBM System/360, with the promise of "at least two times more computations per dollar than any other machine in the industry." This claim was overly ambitious, but the Sigma 7 did offer about 50 percent more processing power than the System/360 Model 50 at its introduction, and the ratio has increased in Xerox's favor since then with the availability of faster memory. Many of the advanced features of the current Sigma computers are based upon the experience which Scientific Data Systems gained by developing and marketing its very successful 900 and 9000 Series scientific computers between 1961 (when SDS was founded) and 1966.

There are a number of strengths in the Sigma Series, based to a great extent upon excellent hardware designs. Although many of the hardware features were designed for SDS's traditional real-time, time-sharing, and scientific computer markets, a substantial number are also intended for general-purpose and commercial users.

For real-time use, Xerox provides a flexible interrupt system ranging from 112 interrupts on the Sigma 3 to 237 or more on the larger Sigma processors. Watchdog timers are built-in to assure that special real-time sensors or asynchronous devices which do not respond within a reasonable period cannot hang the entire system up, and up to four real-time clocks provide timing information and signals for critical time-dependent processes in real-time environments.

Time-sharing users can benefit from rapid context switching and storing by using multiple register blocks and push-down stack instructions to load entire blocks of registers with a single command. Master and slave modes of operation provide lock-and-key protection to certain memory locations and restricted access to privileged instructions. A memory mapping capability allows ▷

MAIN STORAGE

STORAGE TYPE: Magnetic core for main memory, plus optional high-speed integrated-circuit (IC) memories for storage of a set of memory access and/or write-protection codes or locks for the Sigma 5 and larger models.

CAPACITY: See table.

CYCLE TIME: See table.

CHECKING: Parity bit with each 16-bit word in the Sigma 3 or each 32-bit word in the larger Sigmas is generated during writing and checked during reading.

STORAGE PROTECTION: The Sigma 3 provides 16 optional 1-word registers, each bit of which specifies write protection only for memory blocks or pages of 256 addresses. Each 1-word register, therefore, can protect up to 4,096 16-bit words (8K bytes). The full bank of 16 protection registers can thus protect the full 64K-word Sigma 3 maximum memory size.

The Sigma 5 and all larger models use 256 2-bit write-protect locks to protect 512-word pages of main memory from unauthorized writing only. The keys to these locks can be set up only in the privileged or "master" mode of operation. The Sigma 6, 7, and 9, equipped with the memory map, also provide write-only access or complete denial of access to 512-word pages from programs operating in the "slave" mode, in addition to the read-only access provided by the basic lock-and-key protection feature.

CENTRAL PROCESSORS

CONFIGURATION RULES: The Sigma 5 and larger models are designed to permit the attachment of multiple CPU's and independently functioning I/O processors up to the number of ports available on the memory banks. (Standard Xerox software, however, supports only one CPU). The basic memory bank on the Sigma 5 has one memory port which can be expanded to six. The Sigma 6 through 9 each have two standard ports, which can be expanded to eight on the Sigma 6 or 7 and up to twelve on the Sigma 8 or 9. Bus-sharing MIOP's on the Sigma 5 through 9 allow two I/O processors to be attached to a given memory port.

The Sigma 3 is basically a stand-alone processor. An interface to Sigma 5 or 7 core memory is provided, however, to permit up to 8 banks with 4K to 16K 32-bit words each to be added to the Sigma 3. Thus, the Sigma 3 can effectively have up to 256K 16-bit words of Sigma 5 or 7 memory in addition to the maximum Sigma 3 memory.

REGISTERS: The Sigma 5 and larger models have 32-bit general-purpose registers grouped into blocks of 16 registers each. These fast integrated-circuit registers are activated in 16-register blocks by a 4-bit (on Sigma 5, 8, or 9) or 5-bit (on Sigma 6 and 7) control field in the Program Status Doubleword (PSD) known as the Register Block Pointer. The PSD is kept in the arithmetic and control unit, and is alterable only in the "master" mode. This prevents the register Block Pointer from being altered by any user program, and allows the Operating System Control programs to switch contexts from one user job to another with a different set of index registers assigned to each. Any of the registers in a block can be used as fixed- or floating-point accumulators, temporary storage, or for counters, etc. Registers 1 through 7 in each block can also be used as index registers, and registers 12 ▶

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CHARACTERISTICS OF THE SIGMA SERIES SYSTEMS

	Sigma 3	Sigma 5	Sigma 6	Sigma 7	Sigma 8	Sigma 9
SYSTEM CONFIGURATION						
Max.no. of I/O Processors (excluding CPU) supported by standard software	2	8	8	8	8	8
Max. no. of interactive terminals	None	64	128	128	64	128
Orientation of system	Process control, communications, scientific	Real-time, time-sharing, communications, general-purpose	General-purpose	Time-sharing, real-time, general-purpose	Scientific, real-time	Business, general-purpose
Typical system rental (including maintenance)	$3,500	$12,000	$18,000	$20,000	$20,000	$30,000
Date of first delivery	1969	1967	1970	1966	1971	1971
MAIN STORAGE						
Word length, bits	16	32	32	32	32	32
Cycle time, microseconds	0.975	0.950	0.950	0.950	0.900	0.900
Words accessed per cycle	1	1	1	1	1	1
Minimum capacity, words	8,192	8,192	32,768	8,192	16,384	65,536
Maximum capacity, words	65,536**	131,072	131,072	131,072	131,072	524,288
Increment size, words	8,192	8,192	16,384	8,192	16,384	16,384
Storage interleaving	None	2 or 4-way	2 or 4-way	2 or 4-way	2 or 4-way	2 or 4-way
Memory mapping	No	No	Standard	Optional	No	Standard
CENTRAL PROCESSOR						
No. of hardware instructions	37	90	106	108	101	112
Instruction look-ahead	No	No	1 instruction	1 instruction	2 instructions	2 instructions
Index registers	8	1x16 to 16x16	2x16 to 32x16	1x16 to 32x16	1x16 to 4x16	2x16 to 4x16
Double-precision floating-point	No	Optional	Optional	Optional	Standard	Standard
Decimal instructions	No	No	Standard	Optional	No	Standard
Interrupt service time, microseconds	7 (min.)	6 (min.)	6 (min.)	6 (min.)	6 (min.)	6 (min.)
Max. no. of interrupts—external/internal	96/16	224/13	224/13	224/13	224/14	224/14
Watchdog timer	Optional	Standard	Standard	Standard	Standard	Standard
INSTRUCTION TIMES						
Fixed-point binary, microseconds:						
Add/subtract (32 bits)	3.2	2.0	2.0	2.0	0.7	0.7
Multiply (32 bits)	7.8*	7.2	5.0	5.0	3.3	3.3
Divide (32 bits)	8.1*	15.8	12.6	12.6	9.5	9.5
Load/store (32 bits)	4.2	2.0/2.5	1.8/2.6	1.8/2.6	0.7	0.7
Compare (32 bits)	4.2	2.1	2.0	2.0	0.8	0.8
Floating-point, microseconds:						
Add/subtract (single-precision)	Not avail.	4.8	3.3	3.3	2.1	2.1
Multiply (single-precision)	Not avail.	10.0	6.0	6.0	3.3	3.3
Divide (single-precision)	Not avail.	14.0	12.4	12.4	7.7	7.7
Add/subtract (double-precision)	Not avail.	9.0	4.1	4.1	2.9	2.9
Multiply (double-precision)	Not avail.	16.0	9.1	9.1	6.3	6.3
Divide (double-precision)	Not avail.	25.3	25.4	25.4	17.5	17.5
I/O CONTROL						
SIOP transfer rate, bytes/sec	Not used	4,000,000	4,000,000	4,000,000	Not used	Not used
MIOP/EIOP transfer rate, bytes/sec:						
Standard	500,000	450,000	450,000	450,000	500,000	500,000
With 4-byte option	850,000†	900,000	900,000	900,000	1,000,000	1,000,000
HSRIOP transfer rate, bytes/sec***	Not used	Not used	Not used	Not used	3,200,000	3,200,000
IIOP transfer rate, bytes/sec	450,000	Not used	Not used	Not used	Not used	Not used

*For 16-bit operands.
**The equivalent of 256K 16-bit words can be added through a Sigma 5/7 Memory Adapter.
***HSRIOP includes controller for 7212 RAD.
†Two-byte data transfer path on Sigma 3.

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programs to be swapped into fragmented memory areas, thus reducing the swapping overhead time otherwise required to clear large, contiguous memory areas. A wide variety of fixed-head Rapid Access Data (RAD) storage devices is available for temporary storage of swapped programs.

Scientific users in general benefit from many of the above features, plus the symbiont I/O processors (IOP's) which handle I/O along independent memory access paths to permit heavy number-crunching to continue in the CPU without I/O interference. Floating-point single-precision and extended-precision hardware is also available for scientific users.

Commercial users can take advantage of decimal instructions and comprehensive data manipulation and conversion capabilities, and they can also benefit from many of the above scientific and real-time features.

The complex operating systems required to drive these fine hardware capabilities, however, were slow to be developed. The Universal Time-Sharing System (UTS), announced in 1966 as a multi-purpose system that would, in effect, be all things to all people, encountered numerous delays before its release to the field. When this happened, Xerox went on to develop the Batch Time-Sharing Monitor (BTM) as an interim system.

Most of the problems in implementing and delivering the earlier operating systems have now been resolved. UTS, which was delivered early in 1971 primarily as a time-sharing system, evolved through eight versions and numerous enhancements into a true multi-purpose operating system with batch, remote batch, interactive time-sharing, and terminal-oriented inquiry/response capabilities. A second operating system with multiprogramming and transaction processing capabilities, XOS, was a Xerox variant of the operating system designed by CII of France for systems in the IRIS series (manufactured under license agreement with Xerox) and was usable on the Sigma 6 and Sigma 9.

More recently, in mid-1973, both UTS and XOS were replaced by the Control Program-Five (CP-V), which culminates Xerox's efforts thus far to develop a comprehensive, multi-purpose operating system for the Sigma 6 and Sigma 9 computers. As originally released in August 1973, CP-V was based on the earlier UTS operating system and supported four modes of operation: multi-programmed batch, remote batch, time-sharing, and real-time processing. The fifth operating mode (accounting for the "Five" in the name of the operating system) is transaction processing, scheduled for release late in 1974. With the development of CP-V, Xerox has demonstrated its capability to fully harness the hardware potential of its computer systems and to supply operating system capabilities for both scientific and commercial users.

through 15 in each block are also used as accumulators for decimal arithmetic (optional on the Sigma 5, 6, and 7; standard on Sigma 8 and 9).

The Sigma 3 has one block of 32 16-bit high-speed integrated-circuit registers which is divided into 3 different groups: 8 General-Purpose Registers, 8 I/O Channel Registers, and 16 optional Protection System Registers. The I/O Channel Registers hold control information for the integrated I/O processor (HOP). The Protection System Registers are explained under the "Storage Protection" heading above.

INDEXING: In the Sigma 5 and larger models, operand addresses can be modified by the 32-bit contents of any one of registers 1 through 7 in the current register block. The resulting effective address following an indexing operation is automatically adjusted (scaled) for operands of 1-byte, halfword, fullword, or doubleword length.

In the Sigma 3, the first two general-purpose registers are also used as index registers.

INDIRECT ADDRESSING: In the Sigma 3, one level of indirect addressing is allowed, and this may be indexed.

Larger Sigma systems permit indirect addressing for all instructions except those using immediate addressing, to one level only. Indirect addressing may be combined with indexing, but indirect addressing takes place before indexing. That is, the index displacement modifies the direct reference address obtained from the location pointed to by the indirect reference address, rather than modifying the indirect reference address itself. The 17 low-order bits of the referenced address effectively replace the 17-bit reference address field of the current instruction.

INSTRUCTION REPERTOIRE: In the Sigma 3, a basic complement of 37 hardware instructions, each one word in length, permits direct addressing of up to 1024 memory locations. Neither floating-point hardware nor decimal instructions are available.

Larger Sigma processors have more extensive instruction sets (see table) to provide a full range of computational and data manipulation capabilities. Decimal instructions are available for the Sigma 6, 7, and 9 only to provide improved commercial processing facilities. Floating-point single and double precision hardware is standard in the Sigma 8 and 9, and optional in the Sigma 5, 6, and 7. Extensive facilities are also included for testing, searching, logical, and byte-manipulation operations.

INSTRUCTION TIMES: The table on page 70C-930-01c lists representative minimum instruction execution times for each Sigma processor. All times are in microseconds and are for direct addressing without indexing (i.e., with no effective address calculation).

PROCESSOR MODES: The Sigma 5 through 8 processors operate in either a master mode or a slave mode, and the Sigma 9 operates in master, slave, or master-protected mode. The mode is determined by three control bits in the Program Status Doubleword (PSD). Master mode allows the execution of all instructions in any part of memory except certain protected areas. Under master mode operation, an operating system (in master mode) controls and supports the operation of other programs which may be in master, slave, or master-protected modes (Sigma 9 only). Most user application or "problem solving" programs run in slave mode, in which certain

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For real-time systems, the Control Program for Real-Time (CP-R) is an extended version of the Real-Time Batch Monitor (RBM) originally released for the Sigma 5, 7, and 8 processors. Like its predecessor, CP-R processes real-time tasks in a foreground area of memory along with batch processing in the background. However, CP-R utilizes the Memory Map feature available with the Sigma 9 Model 3 (and the newly announced Xerox 550 system) to add virtual memory addressing capabilities to the operating system. CP-R, therefore, can manage memory in two ways: time-critical real-time programs occupying the foreground area of memory operate in the "real" addressing mode, while secondary tasks including background tasks operate in the virtual addressing mode and can be assigned to noncontiguous 512-word pages in the virtual addressing portion of main memory.

The Xerox computers have had a heritage of scientific system usage. For that marketplace, Xerox has developed one of the industry's most extensive product offerings of system interface units to tie analog and sensor-based special-purpose devices into the computer mainframes. An experienced group of systems engineers has been organized specifically to respond to special user interface requirements for real-time, scientific, and university users.

Until 1969, the company placed only a secondary emphasis upon commercial data processing. At that time (coincident with the acquisition of the former Scientific Data Systems by Xerox Corporation), a business plan was established to focus heavier attention upon commercial activities.

In addition to the ongoing software development, extensive efforts have been directed at supplying a full line of peripheral devices that would make the Sigma line more attractive to commercial computer users. Of paramount importance was the introduction of large-capacity disk drives aimed at promoting the acceptance of the Sigma Series in environments with large data base applications. The 7270 and 7275 Removable Disk Storage Systems, announced early in 1974, provide a maximum of 392 million and 1.3 billion bytes of on-line removable disk storage, respectively, for Sigma systems, thus bringing these systems to a competitive level with most other comparable computer systems in on-line disk storage capacity.

Magnetic tape capabilities were enhanced by the addition of 1600-bit-per-inch capabilities to the 120KB 7332 and 240KB 7333 Magnetic Tape Units. Missing from the Xerox product line, however, are more specialized services such as MICR and OCR input units. A Xerox data systems group specializes in providing hardware and software interfaces for a wide variety of non-Xerox-supplied peripheral services. On the other hand, Xerox scored an industry first with its 1973

privileged operations such as I/O control and alteration of the Program Status Doubleword are prohibited. The master-protected mode of operation is used in Sigma 9 processors with the memory map to protect virtual memory.

INTERRUPT STRUCTURE: All of the Sigma Series processors have extensive prioritized interrupt structures, well suited to on-line and real-time environments. Each Sigma processor has internal and external interrupts. The internal interrupts are divided into 3 main groups: the counter group, the override group, and the I/O group. The counter group interrupts are each associated with override interrupts, and are triggered when the result of a modify and test instruction in the interrupt counter location produces a zero result. Counter interrupts may be inhibited, if desired, by programs operating in the master mode. Override interrupts have the highest priority in a Sigma processor and are used for memory parity errors, power on and off, clock pulse signals, etc. Override interrupt signals cannot be shut off. The Internal I/O interrupt group handles standard I/O device interrupt signals and operator control panel interrupts, and may be inhibited by the Program Status Double Word, which is alterable in the master control mode.

Sigma Series external interrupts are configured into groups of 16 interrupts or levels per group. The priority of each level within a group is fixed, but the priority of each group may be established by the user. The Sigma 5 through 9 processors have 14 groups of external interrupts each, for a total of 224; and the Sigma 3 has 6 groups of interrupts, for a total of 96. External interrupts may be in four basic states–disarmed, armed, waiting, or active–in response to interrupt signals. The processor can stimulate any given external interrupt level, thus permitting the simulation of special device attachments for testing and debugging real-time or on-line configurations.

A trap system is also available on the Sigma 5 and larger models. Traps automatically cause a branch to a predesignated location when a trap condition is encountered. Unimplemented Instruction traps (or Unidentified Operator Handlers) are provided to cause program control to be transferred to user-written or Xerox-supplied routines for execution of certain instructions to aid in software simulation. On the Sigma 5, decimal instructions (available in hardware on the Sigma 6 and larger models) are trapped as unimplemented instructions for execution by software routines.

VIRTUAL MEMORY: The Memory Map feature (standard on the Sigma 6 and 9, and optional on the Sigma 7) permits user programs up to 128K words in length to occupy up to 256 pages of 512 words each that are distributed throughout the main memory. The entire user program being executed must fit into main memory at one time, but it need not occupy one large contiguous area. The memory map permits referencing of addresses in virtual memories of up to 4 million words (8192 pages) by translating (or mapping) the 8 most significant bits of the 17-bit effective virtual address (the page identifier portion) into a 13-bit page address. This 13-bit page address is concatenated with the low-order 9 bits of the effective virtual address to produce a 22-bit memory address (for up to 4 million words).

WATCHDOG TIMER: All Sigma processors have a watchdog timer (optional on the Sigma 3 and standard on the larger models) to ensure that real-time operations will not be hung up because of an improperly functioning sensor or other attached device. The watchdog timer issues a trap

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announcement of the 1200 Computer Printing System as an on-line peripheral device for systems operating under the CP-V operating system. A non-impact "Xerographic" computer printing system, the 1200 can print at speeds of up to 4,000 lines per minute, about twice as fast as today's fastest impact-type printers.

Xerox has a substantial custom communications product line with a number of well-designed and reliable communications system building blocks, including local and remote batch terminal controllers. Missing from the standard product line, however, are numerous commonplace components of commercial communications systems such as a full line of CRT display devices, data collection stations, etc. This product-line gap is also a heritage of the Xerox scientific computer background, where most user communications requirements are for unique, special-purpose subsystems that cannot be satisfied by any standard communications product line. Xerox does, however, have all the interfaces necessary to tie in nearly any communications terminals desired by the user.

Currently, although excellent commercial data manipulation capabilities (decimal arithmetic, conversion instructions, etc.) are available in the Xerox hardware, fully supported applications software is provided only for a small group of scientific programs. For scientific users, however, these programs are among the best of their types available and are in wide use. As a result, the Sigma series presents a very strong alternative to IBM for scientific, real-time, and time-sharing users. Initially Xerox enjoyed much less success with business data processing users, mainly because of a dearth of fully supported commercial software applications packages. However, the company has added business data processing packages to its software product line as part of its ACES package for educational institutions, and COBOL, RPG, and a data base management system are now available.

Compatibility within the Sigma line is very good, with almost complete transferability of most programs across the entire series, especially at the source-language level. Xerox's ANS COBOL (announced in 1971) offers source-language compatibility with numerous COBOL processors supported by a variety of other vendors. FORTRAN is Xerox's strong suit, and the Sigma compilers exhibit a high degree of compatibility with the FORTRAN languages of nearly every popular third-generation computer system. Numerous real-time extensions to the Xerox FORTRAN compilers place them among the most powerful FORTRAN systems in the industry. APL and BASIC language processors can execute in both batch and interactive modes, and an industry-compatible RPG compiler is supported for batch operations.

Excluding the small-scale Sigma 3 computer, a modest range of processing capability is available across the

instruction at user-specified maximum time intervals, and if the currently existing program has not had a normal level of activity by the time this interval has expired, it is aborted and the next user job is activated.

INPUT/OUTPUT CONTROL

I/O CHANNELS: The Sigma Series uses symbiont I/O processors (IOP's) to perform selector and multiplexer data transfer between main memory and peripheral I/O devices. On the Sigma 3, selector operations are done by the Integral I/O Processor (IIOP), and multiplexer operations are handled by the External I/O Processor (EIOP). The basic IIOP shares the CPU memory bus and provides four I/O channels. The IIOP can be expanded to 12 channels. The maximum transfer rate of the IIOP is approximately 450,000 8-bit bytes/second on a 1-byte wide data path. The EIOP, conversely, has its own registers and memory but for independent memory bank access. The basic EIOP contains 8 I/O channels and can be expanded to 16 channels. The EIOP transfer data on a 1-byte-width path at approximately 500,000 bytes/second. With the optional 2-byte interface, maximum data transfer rate is approximately 850,000 bytes/sec. Any combination of two IIOP's or EIOP's can be connected to a Sigma 3.

The Sigma 5, 6, and 7 processors can each have a combined total of eight multiplexer and/or selector I/O processors with independent paths to main memory. From 8 to 24 device controllers can be attached to each MIOP, and up to 32 high-speed devices to each SIOP. The MIOP transfers data between main memory and the attached device controllers at approximately 450,000 bytes/sec. Both the MIOP and SIOP have 1-byte-wide data paths that can be expanded to 4 bytes with an optional interface feature. The Sigma 5 can have an integral IOP as well as fully independent MIOP's, while the Sigma 6 includes one 8-controller MIOP as a standard feature. Bus-sharing MIOP's are available on the Sigma 5 through 9 to permit the attachment of two MIOPS to a single memory port.

The Sigma 8 and 9 have I/O channel characteristics that are identical with one another, including a dual-channel capability for connection of up to 24 device controllers on Channel A and 8 devices on Channel B. Other characteristics are similar to those of the Sigma 5, 6, and 7 MIOP. The high-speed RAD I/O Processor (HSRIOP) differs from the lower Sigma series SIOP only in the standard inclusion of 7211 RAD controller equivalent in the HSRIOP; 7212 RAD storage devices can be attached directly to the HSRIOP without a controller. Up to 11 IOP's in any combination of MIOP's and HSRIOP's can be connected to a Sigma 8 or 9 each with its own memory path. Additional IOP's can be configured through bus-sharing. One MIOP with 8 channels is standard in either the Sigma 8 or 9.

Direct Device I/O (DIO) of a full word (16 bits for Sigma 3, 32 bits for other Sigmas) without use of a channel is possible on all processors to transfer data directly to a general-purpose register from a seldom-activated or low-speed sensor or asynchronous device. High-speed real-time I/O is normally handled through an MIOP, SIOP, or Direct Memory Access through a separate port.

On the Sigma 5 through 9, up to 32,000 output control signals and input test signals can be handled through the DIO channel.

SIMULTANEOUS OPERATIONS: Each controller is capable of transferring data to or from only one of the

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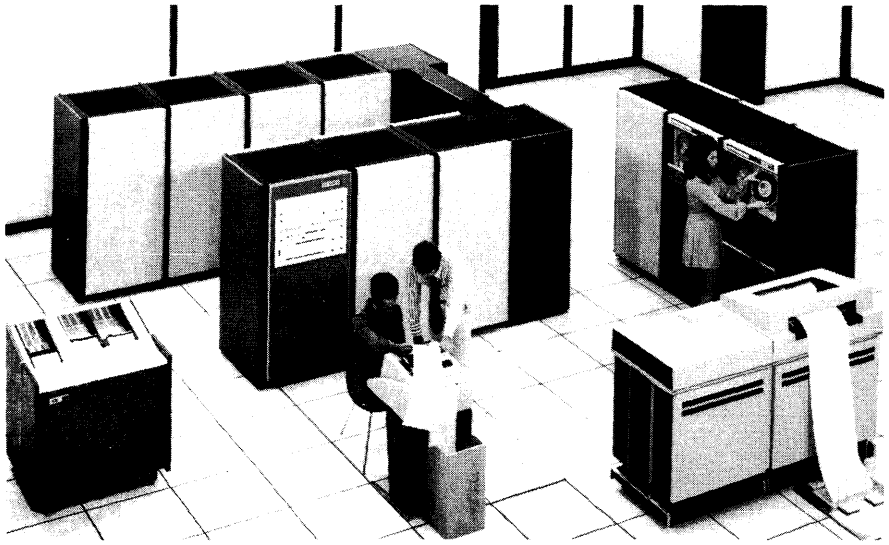

The Sigma 8 computer system is oriented toward real-time and scientific applications. It was developed for use in process control, manufacturing, education, health care, research, and other high-technology environments.

Sigma product line, with the larger models possessing only a little more than four times the internal performance of the smaller systems. The Sigma 6 and 7 processors are nearly identical in performance; each provides approximately 20 percent more throughput in a scientific environment than the Sigma 5, while the commercial processing capabilities of the Sigma 6 or 7 are at least twice those of the Sigma 5. The difference in commercial processing capabilities is due primarily to the lack of decimal hardware and byte-string manipulation instructions in the lower-priced Sigma 5. The top-of-the-line Sigma 8, Sigma 9 Model 3, and Sigma 9 processors also differ from one another primarily in the provision of various features as standard or optional equipment. The Sigma 8 and its upgrade system, the Sigma 9 Model 3, are oriented toward scientific and real-time applications, while the Sigma 9 is intended for business and general-purpose use.

USER REACTION

Major marketing targets for the Xerox Sigma Series have been large-scale university, medical, manufacturing, and governmental installations where multiple-use environments consisting of on-line batch operations are found with extensive, sophisticated in-house programming talent. Although Xerox's share of the overall general-purpose computer market is quite small, in these areas of specialization the Sigma series has earned for Xerox a loyal and satisfied customer base.

In its 1974 subscriber survey of general-purpose computer users, Datapro received a total of six responses from users of Sigma series computer systems. The Sigma series systems represented in the responses included two Sigma 2 systems (in a single installation), one Sigma 3, three Sigma 6 systems, and one Sigma 7 system. Three of these processors were in educational institutions, one was installed in a medical research environment, one was

devices connected to it at a time. The 7204, 7270, and 7275 Disk subsystems, however, can have two-way access, enabling two controllers on different IOP's or different channels on the same IOP to access two disk storage units simultaneously. The IOP's on the Sigma series operate independently of one another through individual memory ports (two bus-sharing IOP's occupy the same path to memory), with simultaneous computing. Sigma 8 and 9 MIOP's permit 32 simultaneous operations, while other Sigma MIOP's permit only 24 concurrent operations.

Two-way or four-way memory interleaving is possible on the Sigma 5 and larger models; consecutive addresses are stored in alternate physical memory banks, permitting overlapped memory accesses. The Sigma 3 has 2-way memory interleaving only. Instruction look-ahead, on the Sigma 6 and larger models, causes the next instruction to be fetched and decoded during execution of any given instruction. The Sigma 6 and 7 have 1-instruction look-ahead, while the Sigma 8 and 9 have 2-instruction look ahead.

MASS STORAGE

7201/7202/7203/7204 RAPID ACCESS DATA (RAD) STORAGE SYSTEM: Consists of 7201 RAD Controller and from one to eight head-per-track 7202, 7203, or 7204 RAD Storage Units in any combination. Each 7202 has a capacity of 737,280 bytes (128 tracks); the 7203 stores up to 1,474,560 bytes (256 tracks); and the 7204 stores up to 2,949,120 bytes (512 tracks). Each single-spindle RAD Storage unit organizes data into tracks of 16 sectors each, with 360 8-bit bytes per sector. Average access time for the 7202, 7203, or 7204 is 17 milliseconds, and data transfer rate for each unit is 187,500 bytes/second when accessing a single sector or an overage of 170,500 bytes/second for multiple-sector accesses. The 7201 RAD System connects to an SIOP or MIOP channel.

7211/7212 HIGH-SPEED RAPID ACCESS DATA (RAD) STORAGE SYSTEM: Consists of a 7211 RAD Controller and from one to four head-per-track 7212 RAD Storage Units. Each 7212 has a capacity of 5,373,952 8-bit bytes, for a maximum 7211 system capacity of 21,495,808 bytes. Data is organized into sectors of 1024 bytes each, with 82 sectors per band and 64 bands per 7212 unit. Average access time is 17 milliseconds, and data transfer

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in manufacturing, and the two Sigma 2 processors were engaged exclusively in real-time control. Their users indicated that four of the Sigma series processors were performing both scientific and business data processing, and two of these were also engaged in data base management operations. These Xerox users expressed a high degree of satisfaction with their systems, as follows:

	Excellent	Good	Fair	Poor	WA*
Ease of operation	2	4	0	0	3.3
Reliability of mainframe	2	3	1	0	3.2
Reliability of peripherals	1	2	3	0	2.7
Maintenance:					
Responsiveness	4	0	2	0	3.6
Effectiveness	2	2	1	0	3.2
Technical support	2	1	3	0	2.8
Operating systems	2	4	0	0	3.3
Compilers and assemblers	3	3	0	0	3.5
Application programs	1	3	0	1	2.8
Ease of conversion	1	2	1	0	3.0
Overall satisfaction	2	4	0	0	3.3

*Weighted Average on a scale of 4.0 for excellent.

The Sigma series' weakest score in comparison to the average ratings achieved by all of the computer systems represented in Datapro's 1974 user survey was in the area of peripheral reliability, where users gave the Sigma series a weighted average of 2.7 compared with an industry average of 3.0. The two other categories in which users gave their Sigma systems a lower-than-good (under 3.0) rating were those in which the overall ratings for all the computer systems in the survey were also less than good, indicating that in the areas of technical support and application programs Xerox was at least as good as the industry average.

Users expressed a high degree of satisfaction with the Xerox software—both the operating systems and the compilers and assemblers. In particular, users cited the flexibility and adaptability of the systems for multi-use environments. The users were also well pleased with both the responsiveness and effectiveness of the Xerox maintenance service.

In terms of overall satisfaction, these users gave their Sigma systems an average rating of 3.3, higher than the overall rating of 3.1 for all computer systems in the Datapro survey. It appears, then, as if Xerox has accomplished some of its goals established for the Sigma series. Although the sample here is very small, those users in the original targeted market areas for the Sigma series who responded to the Datapro survey appear to be very pleased with the Sigma family's capabilities. It remains to be seen whether Xerox can capitalize on these successes and extend its influence into more commercially-oriented environments with its newer 530, 550, and 560 computer systems. □

rate is 3 million bytes/second when accessing a single sector or 2.47 million bytes/second when accessing one or more full bands (82 sectors). The 7211 Controller connects only to a Selector I/O Processor (SIOP) on the Sigma 5 or 7. On the Sigma 8 or 9, the 7212 RAD connects directly to the High-Speed RAD I/O Processor (HSRIOP) without the 7211 Controller.

7231/7232 EXTENDED-PERFORMANCE RAPID ACCESS DATA (RAD) SYSTEM: Consists of a 7231 RAD Controller and from one to four head-per-track 7232 RAD Storage Units. Each 7232 has a capacity of 6,291,456 bytes, for a maximum 7231 system capacity of 25,165,824 bytes. Data is organized into sectors of 1024 bytes each, with 12 sectors per track and 512 tracks per 7232 unit. Average access time is 17 milliseconds, and data transfer rate is 384,000 bytes/second when accessing a single sector or 365,000 bytes/second for multiple-sector accesses. The 7235 Extended Width Interface feature provides a 4-byte data path for increased effective data transfer rates over the standard 1-byte-wide data path. The 7231/7232 RAD system connects to an SIOP or MIOP channel.

7270/7271/7274 REMOVABLE DISK STORAGE SYSTEM: Consists of a 7270 Disk Storage Controller and from two to eight model 7271 Disk Drives with a capacity of 49 million bytes each for an on-line storage capacity of from 98 million to 392 million bytes per controller. The 7270/7271 subsystem uses the 7274 Disk Pack for 49,152,000 bytes of on-line storage per spindle. The 7274 is an 11-disk pack with 20 recording surfaces. Data is organized into sectors of 1024 bytes with 6 sectors per track and 400 tracks (plus 6 spares) per surface. Average head movement time is 35 milliseconds, and average rotational delay is 12.5 milliseconds. Data transfer rate is 312,000 bytes/second for multiple sectors.

The optional use of an additional 1040 controller plus one 1041 Dual Access Feature per disk drive provides dual access to the disk subsystem and allows simultaneous read/read, read/write, and write/write operations on any two spindles in a total subsystem of eight spindles. The 1042 Extended Width Interface permits full-word transfers. An Independent Seek Operation feature allows overlapping of seek operators on multiple-spindle systems, and the Hardware Write-Protect feature provides for file protection of each spindle.

7275/7276/7277 REMOVABLE DISK STORAGE SYSTEM: Provides large-capacity direct-access storage. A minimum configuration consists of a 7275 Disk Controller with three 86-million-byte disk drive units. The 7276 system consists of a 7275 Disk Controller and seven 86 million-byte disk drive units. Both the 7275 and 7276 configurations can be expanded to include up to fifteen 7277 disk drives for a total of 1.3 million bytes of on-line storage. The removable storage medium is the Model 7279 Disk Pack, which contains 19 recording surfaces. Data is organized in 1024-byte sectors, with 11 sectors per track and 404 tracks (plus 7 spares) per surface. Average seek time is 30 milliseconds, and average rotational delay is 8.3 milliseconds. Data transfer rate is 806,000 bytes/second. The use of an additional 1043 Controller plus one 1044 Dual Access Feature per disk drive permits simultaneous read/read, read/write, or write/write operations on any two spindles. Hardware write product and overlapped seek operations are supported.

INPUT/OUTPUT UNITS

7315/7316 MAGNETIC TAPE SYSTEM: Consists of a 7315 Controller combined with one tape drive and one

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optional 7316 Add-on Tape Drive. This 9-track NRZI system has a tape speed of 75 inches/second and a recording density of 800 bpi for a maximum data transfer rate of 60,000 bytes/second. The tape is ½ inch wide and is compatible with the IBM 2400 and 3400 Series Magnetic Tape Units.

7320/7322/7323 MAGNETIC TAPE SYSTEM: Consists of a 7320 Controller and from one to eight 7322 and/or 7323 tape drives that can read either forward or backward. The 7322 9-track NRZI tape drives have a tape speed of 75 inches/second and an 800-bpi recording density for a maximum data transfer rate of 60,000 bytes/second. The 7323 9-track NRZI tape drives have a tape speed of 150 inches/second and a recording density of 800 bpi for a maximum data transfer rate of 120,000 bytes/second. Both cyclic and longitudinal redundancy checks are generated by the 7320. The tape is ½ inch wide and is compatible with the IBM 2400 and 3400 Series Magnetic Tape Units. Patented Push-On-Pull-Off (POPO) tape hubs simplify mounting and removing tape reels.

7261/7362 MAGNETIC TAPE SYSTEM: Consists of a 7361 Controller and one or two 7362 7-track NRZI Magnetic Tape Drives. The drives have a tape speed of 37.5 inches/second and a recording density of 556 bpi for a maximum data transfer rate of 20,850 characters/second. A program-selectable, binrary packing mode of operation permits 8-bit bytes to be recorded on the 7362; this BCD option for the controller allows the 7362 to be used as a low-speed 9-track tape substitute. The tape is ½ inch wide and is compatible with IBM 7-track recording formats. Patended Push-On-Pull-Off (POPO) tape hubs simplify mounting and removing tape reels. The 7362 reads in the forward direction only.

7371/7372 MAGNETIC TAPE SYSTEM: Consists of a 7371 Controller and from one to eight 7372 7-track NRZI Magnetic Tape Drives. The drives have a tape speed of 75 inches/second and recording densities of 200, 556, or 800 bpi for maximum data transfer rates of 15,000, 41,700, and 60,000 characters/second, respectively. A program-selectable, binrary packing mode of operation permits 8-bit bytes to be recorded on the 7372; this BCD option for the controller allows the 7372 to be used as a low-speed 9-track tape substitute. The code conversion operation is performed in the controller. The tape is ½ inch wide and is compatible with IBM 7-track recording formats. Patented Push-On-Pull-Off (POPO) tape hubs simplify mounting and removing tape reels.

7121/7122 CARD READERS: Read 80-column cards serially by column at the rate of 200 or 400 cards per/minute for the 7121 or 7122, respectively. Both tabletop readers accept EBCDIC on binary code. Input hopper capacity for either reader is 1400 cards, and output stacker capacity is 1000 cards. The 7121 or 7122 includes a controller and connects directly to the Multiplexer I/O Processor.

7140 HIGH-SPEED CARD READER: Reads 80-column cards serially by column at the rate of 1500 cards/minute in either EBCDIC or binary code. The input stacker holds 2500 cards, and two output stackers hold a combined total of 2000 cards. The stackers are program-selectable to facilitate the separation of exception or error cords. The 7140 includes a controller and connects directly to the Multiplexer I/O Processor.

7160 CARD PUNCH: Punches 80-column card in row-by-row fashion at 300 cards/minute in either EBCDIC or binary code. Read-after-punch verification is provided. The input hopper holds 1000 cards, and two program-selectable output stackers hold 1000 cards each. The 7160 includes a controller and connects directly to the Multiplexer I/O Processor.

7165 LOW-SPEED CARD PUNCH: Punches 80-column cards in column-by-column fashion in either EBCDIC or binary code. With 80 columns punched, the speed is 100 cards/minute; maximum punch speed is 300 cards/minute with up to 20 columns punched. The input hopper and the output stacker each have a capacity of 1000 cards. Cards in the output stacker can be offset under program control to segregate error cards, etc. The 7165 includes a controller and connects directly to the Multiplexer I/O Processor.

7060 PAPER-TAPE INPUT/OUTPUT SYSTEM: Includes a 7061 Controller and Cabinet, a 7062 Paper-Tape Reader, a 7063 Paper-Tape Punch, and a 7064 Spooler. The 7062 reads paper tape at a speed of 300 characters/second, and is mounted with the 7064 Spooler and the 7061 Controller in a separate cabinet. The 7063 Punch operates at a rate of 120 characters/second. The punched tape may be 5-, 6-, 7-, or 8-level format, and is passed through the 7060 system at a rewind or fast forward rate of 200 inches/second.

7440 LINE PRINTER: Provides full-line buffering of 132 positions for print speeds of 628 to 795 lines/minute, depending upon the number of different characters printed per line. The 7440 uses a 56-character print drum and has an 8-channel vertical format control tape and a print spacing of 6 lines/inch. Among the 8 operator controls are an indicator for low paper supply. The 7440 includes a controller and connects directly to the Multiplexer I/O Processor.

7441 LINE PRINTER: Provides full-line buffering of 132 positions for print speeds of 550 to 1100 lines/minute for the full 96-character drum or a subset consisting of the first 42 characters, respectively. The dum may be ordered with full or partial ASCII or EBCDIC character sets, and prints under operator control at either 6 or 8 lines/inch. A 64-character drum is also available. Forms control is handled by an 8-channel control tape. The 7441 includes a controller and connects directly to the Multiplexer I/O Processor.

7446 LINE PRINTER: Provides full-line buffering of 132 positions for print speeds of 1200 to 1500 lines/minute for the full 64-character drum or a subset consisting of the first 47 characters, respectively. The drum may be ordered with either a 64-character ASCII or EBCDIC set. The 7446 prints 6 or 8 lines/inch under operator control, and uses an 8-channel carriage control tape to handle forms control. The single-line forms feed rate is 16 inches/second, and the multiple-line feed rate for 6 lines or more is 90 inches/second. A motor-operated accoustical cover is used to reduce the noise level. This printer provides operator facilities similar to those of the widely used IBM 1403 Printers. The 7446 includes a controller and connects directly to the Multiplexer I/O Processor.

7450 LINE PRINTER: Offers low-cost, low-speed printing of 128-position lines at 225 to 450 lines/minute, depending upon the number of different characters printed per line. The print drum has 63 EBCDIC characters plus a blank, consisting of the numerals, upper-case letters, and 27 punch marks and symbols. Half-line buffering is provided, and basic forms control is handled

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by a 2-channel control tape which senses bottom-of-page and skips to top-of-page. Vertical spacing is 6 lines per inch. Automatic forms advance is provided under processor control, and inhibition of automatic advance as well as skipping of up to 7 lines per command is provided under program control. The 7450 includes a controller and connects directly to an MIOP channel.

7012/7014 KEYBOARD/PRINTERS: Provide the required operator console interface through an I/O channel. The 7012 is a modified Model 35 KSR Teletypewriter and controller which sends or receives EBCDIC code a rate of 10 characters/second. Print line width is 86 characters at a horizontal spacing of 12 characters/inch. Vertical spacing is 6 lines/inch. The 7014 is a spare print mechanism.

7015/7016/7017 AND 7025/7026/7027 REMOTE COMMUNICATION TELETYPEWRITERS: These units are modified Teletype Model 35's and are ASCII-compatible. Each teletypewriter can operate in a simplex (one-way only), half-duplex (two-way alternate), or full-duplex (two-way simultaneous) mode using Bell System 103 modems. Input/output printing speed is 10 characters/second, with horizontal spacing of 12 characters/inch and vertical spacing of 6 lines/inch. The 7015 (KSR-35), 7017 (ASR-35), 7025 (KSR-35), and 7027 (ASR-35) are keyboard/printers; and the 7016 (RO-35) and 7026 (RO-35) are printers only.

7018 REMOTE KEYBOARD/PRINTER: This unit is a modified Teletype Model 37 and is ASCII-compatible.

7020/7021 KEYBOARD/PRINTERS: The 7020 is a modified Teletype Model 35 ASR with a paper tape reader/punch and controller which provides the required operator console interface to a Sigma operating system through an I/O channel. The 7021 is a replacement print mechanism. Standard EBCDIC code can be sent or received via the keyboard, printer, and/or punch at 10 characters/second, and via the paper tape reader at 19 characters/second on-line and 10 characters/second off-line. Horizontal spacing of the 86-character line is 12 characters/inch, and vertical spacing is 6 lines/inch.

7530/7531 GRAPH PLOTTERS AND 7534 CONTROLLER: These modified Calcomp drum-type plotters produce X-Y plots under computer control on rolls of paper wither 11 inches (7530) or 29.5 inches (7531) in width. Maximum plotting speeds are as follows:

Increment Size	7530 (Modified Calcomp 565)	7531 (Modified Calcomp 563)
0.010 in.	3 in./sec.	2 in./sec.
0.005 in.	1.5 in./sec.	1.5 in./sec.
0.100 mm.	30 mm./sec.	30 mm./sec.

COMMUNICATION CONTROLS

7601 DATA SET CONTROLLER: Enables half-duplex or full-duplex connection (optional feature 7602) of a Bell System 100, 200, or 300 Series modem for communication over common-carrier private lines or switched message networks. Message transmission is provided at rates of 45 to 230,400 bits/second in a variety of standard speeds and formats. Operating synchronously or asynchronously, the 7601 is code-independent. An Automatic Dialing Feature (7603) provides control for the Bell System 800 Series Automatic Calling Unit or its equivalent to perform automatic dialing on a common-carrier switched network under computer control. The 7601 connects to a Sigma MIOP channel. Full-duplex operations use two MIOP channels.

7605 PROCEDURE-ORIENTED DATA SET CONTROLLER: A variation of the 7601 for binary synchronous protocol. This procedure-oriented controller provides an interface to a Xerox IOP for a single device operating at up to 230,400 bits/second via a Bell System 100, 200, or 300 series modem.

7604 LOCAL BATCH TERMINAL CONTROLLER: Provides full-duplex tie-in for either a local batch terminal or a 7670 Remote Batch Terminal. Operating speed is 2400 bits/second.

7611 CHARACTER-ORIENTED COMMUNICATION (COC) SUBSYSTEM: Provides low-to-medium-speed asynchronous communications control for up to 64 remote terminals operating simultaneously at speeds up to 1800 bits/second each. Independent simplex, half-duplex, or full-duplex operation is provided for each line handled. Up to 16 COC Subsystems can be connected to any Sigma Series computer, each through an MIOP channel. Up to five 7612 Timing Modules can be added to each COC Subsystem to control line interfaces. For each group of 8 lines tied to the COC subsystem, a 7613 Line Interface Unit (LIU) is required. A variety of other interface features are available for special-purpose requirements, including commercial modems, DC interfaces, military device interfaces, etc.

7630/7631 COMMUNICATION SUBSYSTEM: Consists of a 7611 COC Subsystem packaged to handle 8 lines.

7650 CHANNEL INTERFACE UNIT: Enables transfer of data and control information between two Sigma Series computers. Transmission is in half-duplex mode at a rate of 900,000 8-bit bytes/second (at 1000-foot distances or less) or over 450,000 8-bit bytes/second (at distances up to 2000 feet) using private-wire communications systems. The 7650 connects to any multiplexer or selector I/O processor in the Sigma Series. With the Sigma 7, interconnection cables are provided at no extra charge; these cables are separately priced for other Sigma processors.

COMMUNICATIONS I/O PROCESSOR: The CIOP is available from Xerox as a special programmable subsystem on an RPQ basis. This subsystem is capable of handling up to 512 voice-grade lines with line speeds of 75 to 9600 bits/second, or multiple wide-band lines with line speeds ranging from 20,000 to 230,400 bits/second, for an aggregate line capacity of more than 500,000 characters per second. The CIOP has a sustained message-switching capacity greater than 50,000 fifty-character messages (or 25,000,000 characters) per hour. The CIOP can operate in three modes—message switching, transaction mode, or a combination of both—to provide most of the communications interface functions in a Sigma communications network, thereby minimizing the communications demand on the central processor.

SWITCHING EQUIPMENT AND SPECIAL INTERFACE UNITS: Xerox offers a number of programmable switches to transfer up to ten peripheral controllers from one channel or I/O processor to another on the same or different Sigma system(s). A wide variety of special System Interface Units is also available to accommodate analog devices, display drivers, counters, frequency sources, etc.

SOFTWARE

OPERATING SYSTEMS: Software support for the Sigma Series is provided at six major levels. Their designations, in order of increasing power and complexity, are: Basic Control Monitor (BCM), Real-Time Batch Monitor

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(RBM), Batch Processing Monitor (BPM), Batch Time-Sharing Monitor (BTM), and the two most recently announced, CP-R (Control Program for Real-Time) and CP-V (Control Program-Five). The facilities provided at each of these support levels are summarized in the following paragraphs. Although multiple CPU connections are possible in hardware configurations, the standard Xerox software provides support for single-CPU configurations only.

BASIC CONTROL MONITOR: BCM is designed for minimal Sigma systems, such as those which do not contain RAD storage devices. BCM runs on the Sigma 3, 5, and 7 processors and provides real-time foreground processing concurrently with general-purpose background batch processing. Availability of operator communication support to the background batch job streams and automatic I/O handling are two of the key features of BCM.

REAL-TIME BATCH MONITOR: RBM was developed to fully utilize the advanced real-time hardware features present on the Sigma 3, 5, 7, and 8 processors to run real-time processing in the foreground concurrently with batch processing in the background. The following capabilities have been designed into RBM: priority scheduling using Sigma's extensive hardware interrupt capabilities; program re-entrancy using both the push-pull stack feature and high speed "context" switching between register blocks; and memory protection. RBM uses RAD or disk files for swapping of non-resident user programs and segments of RBM itself. Toward this end, RBM is extensively segmented, permitting resident operating system memory requirements to be much smaller than the overall RBM size.

Up to 100 real-time tasks can be processed concurrently by RBM, with re-entrant monitor services, use of the public library, and selected dedicated peripheral devices available to the real-time users. Background batch users can take advantage of a job accounting facility that records system utilization by name and account, and can also use a variety of language processors, including a macro assembly language, several versions of FORTRAN, etc. Foreground programs which require more memory than has been reserved for foreground use can temporarily seize all of the Sigma system resources by using a checkpoint capability to dump the background on direct-access storage for subsequent restoration to memory. To complement this variable partitioning capability, the operator can reduce the size of the foreground area from his console if desired, thus making more memory available for background use. Other features of RBM include symbolic I/O device references, allowing specific hardware assignment to be deferred until execution time under program control, and a Real-Time Debug package to assist in debugging foreground or background programs.

BATCH PROCESSING MONITOR: BPM has been designed for general-purpose batch processing on the Sigma 5, 6, 7, 8, and 9; it includes a "symbiont" feature to handle I/O simultaneously with processing. BPM can operate in three modes: local batch, remote batch, and real-time. In local batch processing, input jobs are queued on an RAD or disk unit for subsequent processing according to individual job priority. The operator may suspend or delete a job and may change individual job priorities. Symbiont file processing and language processors are supported in the local batch mode. Symbionts perform a spooling function to permit peripheral operations to occur simultaneously with processing.

BPM remote batch processing supports the 7670 Remote Batch Terminal and provides the same services as the local batch mode. For real-time processing, both resident and non-resident tasks can be assigned to the foreground at SYSGEN time. These tasks can be invoked by the operator and are driven by Sigma hardware interrupts concurrently with local or remote batch processing. The facilities for real-time processing under BPM are very similar to those provided RBM, including use of checkpoint service for the real-time foreground to preempt all system resources temporarily, etc.

BPM supports consecutive (sequential), keyed (indexed sequential), and random file structures for ANS COBOL, 3 versions of FORTRAN including FORTRAN Load And Go (GLAD), Xerox Meta Assembler, and BASIC. A number of standard XDS program products are also supported, including EDMS, MANAGE, SL-1, GPDS, FMPS, CIRC, etc. Other features of BPM include overlay service, a character-oriented communications (COC) system (for support of the 7611 Communications Controller), accounting statistics, debug aids, automatic or manual recovery procedures, and an error log for I/O or parity errors, etc.

BATCH TIME-SHARING MONITOR: BTM supports local, remote, and/or terminal-initiated batch processing simultaneously with real-time operations and up to 64 on-line time-sharing users on Sigma 5, 6, 8 and 9 systems. Swapping of on-line users' programs or segments is overlapped with batch operations, which are located in a dedicates Sigma memory partition. BTM is an extended version of BPM with a time-sharing Terminal Executive program added. Symbiont routines that buffer I/O to high-speed RAD's or disks are provided. On-line users may use Symbol (the Xerox assembler), BASIC, or FORTRAN IV-H with complete compatibility at the source and object language level to the batch processors. Language processors supported under BTM include COBOL, FORTRAN, interactive FORTRAN Debugger (FDP), BASIC, on-line Edit, etc. The structures for data files created on-line are common to those of batch users. A user can develop a program and/or data base interactively, then initiate remote or local batch processing to execute his job.

The BTM scheduling algorithm, as well as other basic parameters used by the time-sharing executive program, can be dynamically modified by the operator during execution to adjust for varying work-load requirements. Basically, a two-level round-robin scheduler (the higher level for conversational users and the lower level for compute-bound users) controls interactive access to the system resources under BTM. An upper limit on total interactive resource use can be set. A Performance Monitor which provides on-going profiles of system and user activity can give the operator on-line feedback as to the system's performance. Although the maximum number of interactive users under BTM is 64, the practical limit depends upon the type of work done by each user and the availability of swapping devices.

The greater the number of time-sharing users, the greater the reduction in potential batch throughput under BTM. Within a basic user-specified parameter guaranteeing a certain percentage of system resources to batch operations, batch throughput and concurrent interactive user response will vary widely with workload fluctuations. Individual time-sharing users can be allocated set percentages of the overall time provided for all time-sharing operations.

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BTM also includes the following on-line subsystems: EDIT–a tool to create and modify data files; FDP and DELTA–interactive debugging packages; FERRET–a program to provide a list of user files and/or reassign their storage locations; and Terminal Oriented MANAGE (TOM)–to permit on-line access to MANAGE files.

CONTROL PROGRAM FOR REAL-TIME: CP–R is an upward extension of the Real-Time Batch Monitor that includes new facilities to use the Memory Map feature available in the Sigma 9, Sigma 9 Model 3, and Xerox 550 computer systems. As a result, CP-R provides both real- and virtual-memory management capabilities for processing both real-time and batch-oriented programs. Multiprogramming support is provided for up to 32 jobs (of which one is a background job). A job is defined as a set of user programs, called tasks, which is allocated peripheral and main memory resources. Multi-tasking support is provided for a maximum of 255 tasks.

CP-R divides main memory into four classes: the CP-R System Memory, the Foreground Private Memory, the Foreground Preferred Memory, and Secondary Task Memory. The CP-R System Memory contains resident and nonresident CP-R routines and job and task management data. Foreground Private Memory is used by highly time-critical programs that are not rolled out to disk storage and for other programs that require direct access to physical memory. User programs also can execute in foreground private areas as primary tasks. CP-R System Memory and the Foreground Private Memory operate in the real memory addressing mode. Primary tasks occupying foreground private areas are scheduled by the hardware priority interrupt system and do not require software scheduling intervention.

The Foreground Preferred Memory areas are used for sharing data between primary tasks and secondary tasks, for data transfers involving peripheral devices with very high transfer rates, and for remote terminal operations. Tasks executing in the Foreground Preferred Memory areas can reside at real or virtual memroy addresses.

Secondary real-time tasks, the background batch task, symbionts, media conversion routines, and secondary tasks initiated from terminals execute in the Secondary Task Memory in a virtual memory addressing mode. Secondary tasks are scheduled by primary tasks or by the CP-R task management routines and are dispatched by software dispatchers. All secondary tasks, unless they request to be "locked" in memory, may be rolled out by CP-R to provide memory space for higher priority tasks.

The CP-R System Area occupies 24K words of main memory, and an additional 8K words of memory are reserved for a Task I/O Buffer Area and tables used by the DEBUG program. The remainder of memory is available for primary and secondary task execution. CP-R uses RAD or disk files for swapping non-resident portions of primary programs and of CP-R itself, and for rolling out portions of mapped secondary tasks. Memory protection for mapped programs is built into the Memory Map for each 512-word page, and provides for free access, read and execute access only, read access only, and denial of access. Programs operating with fixed memory addresses are protected by a two-bit write lock key. Each secondary task has a unique virtual addressing space of 128K words independent of the size of physical memory.

CP-R is heavily segmented, permitting resident operating system memory requirements to be much smaller than the overall CP-R size. The CP-R software segmentation facility also allows virtually addressed tasks to be logically divided into segments. Only the active segments of a task need to be loaded into physical memory for execution. Context switching for virtually addressed tasks is accomplished by reloading the portion of the memory map corresponding to the segments to be activated.

Up to 100 real-time tasks can be processed concurrently by CP-R, with re-entrant monitor services, use of the public library, and selected dedicated peripheral devices available to real-time users. Background batch users can take advantage of a job accounting facility that records system utilization by name and account, and can use FORTRAN, Xerox Assembly Program, and SL-1, a simulation language designed specifically for digital or hybrid simulation. CP-R permits the use of symbolic I/O device references, allowing specific hardware assignment to be deferred until execution time under program control and both shared or exclusive use of peripheral devices.

A Terminal Job Entry (TJE) Facility supports concurrent terminal operations, permitting file creation and editing, batch job entry, real-time job initiation, and real-time job debugging. Up to 16 concurrent users can be supported at local and remote terminals. The CP-R debug facility is available for debugging primary or secondary tasks from a terminal and for the background task and tasks initiated locally.

CP-R incorporates comprehensive reliability, maintainability and availability (RMA) features. An error log of all central processor memory and I/O errors is stored on a disk file and can be retrieved in chronological or sorted orders. An error analysis program provides information on the system status, including CP-R tables and hardware conditions at the time of the error, to aid in error diagnosis. Malfunctioning peripheral devices can be manually removed from the system and subjected to device verification routines for detecting recoverable and non-recoverable errors. Off-line diagnostic software also is provided. In the event of a system failure, CP-R will isolate the malfunctioning system and provide for an orderly shutdown of the affected components. A resident routine loaded by CP-R after the shutdown procedure can be used to terminate real time tasks or initiate application-dependent recovery attempts.

CONTROL PROGRAM-FIVE (CP-V): CP-V is a comprehensive multi-purpose operating system for Sigma 6, Sigma 9, and Xerox 560 computer systems. An outgrowth of the Universal Time-Sharing System (UTS), CP-V provides upward compatibility for UTS language processors and application programs and supports any combination of the following five modes of operation: multiprogrammed batch, remote batch, conversational time-sharing, real-time, and transaction processing. Designed as an "integrated" operating systems, CP-V makes extensive use of common system services such as schedulers, memory management and file management routines, and symbionts, to ensure interchangeability of programs and sharing of data files among the five operating modes. CP-V uses the Memory Map feature to relocate programs into non-contiguous 512-word pages. CP-V, using the Memory Map, manages the swapping of programs between main memory and a high-speed RAD

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and provides for context switching by loading and reloading the 256 Memory Map registers.

The batch processing mode permits multiprogrammed execution of batch jobs from up to 16 batch streams or "partitions." Partitions are described by a set of parameters that establish the minimum and maximum limits for the resources utilized by each partition (such as total job execution time, main memory size, and non-shareable peripherals), and are used for optimizing the job mix being executed by predetermining the mix of I/O and compute-bound jobs. Partition attributes are dynamically alterable to respond to changing job mixes. All batch jobs are queued in a single input queue in priority sequence and are initiated according to priority and resource requirements.

Batch jobs entered from remote batch terminals also are entered in the input queue and scheduled for execution in the batch "partitions." Jobs can be entered from a time-sharing terminal, from a remote batch terminal, from an intelligent remote batch terminal (such as a Xerox 530 or IBM 360/20 computer system), from another Xerox computer system, or from any other computer system operating under IBM HASP multileaving protocol for binary synchronous transmission. Output from remotely entered jobs can be returned to the originating terminal, to another specified terminal, to multiple terminals, or to the central site. Output from locally entered batch programs can also be dispersed to one or more remote terminals. CP-V permits users to control the total number of active batch partitions, to temporarily block execution of a specified partition, or to lock a partition in memory in order to ensure faster execution of these jobs.

Up to 128 on-line time-sharing users can be handled concurrently with local or remote batch processing and real-time operations. A Terminal Execution Language (TEL) is available for submitting requests for time-sharing services by users. Each time-sharing user has the facilities for creation, modification, debugging, and initiation of programs as well as for creation, modification, inquiry into, and deletion of files. In addition to the conversational mode of operation, time-sharing users can use a deferred batch operation to initiate a job through the terminal batch entry facility for execution as a local batch job. Debugging aids are available for assembly language, FORTRAN, and COBOL programs; in addition, programs created in other modes of operation can be debugged from time-sharing terminals. Time-sharing terminals supported by the CP-V Time-Sharing Mode include Teletype terminals and the IBM 2741.

CP-V supports two levels of real-time processing. Highly time-critical real-time programs are assigned to an unmapped area of foreground memory and operate under direct control of the interrupt system without requiring operating system intervention. Centrally connected real-time tasks can be resident in memory or can be assigned to mapped memory. A non-resident real-time program can request to be locked into memory to complete the processing of a task. Centrally connected real-time tasks are connected to the interrupt structure through a central CP-V routine and are processed as normal batch or on-line jobs. Centrally connected real-time programs have access to all normal CP-V facilities and can direct their output to specified remote terminals. Real-time programs operate in a time-slicing mode, with user-determined intervals selected for each task. A "wake-up" facility permits tasks to be activated at predetermined times.

The Transaction Processing Mode provides device-independent access from remote or local terminals through user application programs to shared CP-V-managed central files or a generalized data based organized under the Xerox EDMS data base management system. The Transaction Processing Mode multitasking capability permits concurrent processing of multiple tasks entered from remote terminals or originating from a single terminal entry. Individual terminals can also be limited to entering specific transaction types. An interactive data base processor permits users to query and update files concurrently with other users and batch programs, and provides file protection to prevent simultaneous updating of records by two users. A report-generating capability is supported. All output generated by the system can be routed directly to the originating terminal, to alternate terminals, or to output devices at the central site.

In systems using EDMS, a common journal facility is used to provide a complete audit trail of the flow of transactions through the system, including queued transactions and output. In the event of a system malfunction, utilities are available to restore the data base, including all transactions processed to the point of failure. In case of transaction errors, the transaction can be aborted and the data base restored to its original content before processing of the transaction. User-oriented commands are provided to enable users at remote locations to examine, search, and modify the data base.

Standard CP-V system services that are available to all processing modes include the system scheduler, the file management system and file maintenance utilities, reentrant language processors, spooling symbionts, resource management routines, and accounting routines. Files can be protected from unauthorized access either by passwords or by association with a list of users with authorization to read or to read and update. A performance-monitoring system provides statistical summaries of performance data and enables the user to alter key parameters for "tuning" the system.

A system recovery function is automatically invoked by CP-V upon detection of an unrecoverable hardware or software error. The recovery routines examine all essential system tables for intactness and reload a new copy of CP-V to begin system re-initialization. Errors that can be isolated to a single user cause that user's program to be aborted while the remainder of the system continues processing. A manual entry point is also provided for use in the event of unrecoverable errors. File recovery also is handled automatically by CP-V.

File structures supported by CP-V are consecutive (sequential), keyed (indexed sequential), and random. Secondary storage for virtual storage swapping can be a high-speed RAD or removable disk storage system.

COBOL: Xerox offers an ANS COBOL compiler which is segmented for use on Sigma equipment with memory mapping. Extended COBOL language features include implementation of the Table Handling module, sort/merge linkages, common data storage for independently compiled programs, etc. ANS COBOL is available for the Sigma 5, 6, 8, and 9 systems.

FORTRAN: Xerox offers FORTRAN in a number of different versions. For the Sigma 3, Basic FORTRAN, FORTRAN IV, and ANS FORTRAN IV are available, all of which are upward-compatible with their FORTRAN counterparts on the larger Sigma series processors.

A FORTRAN Load and Go (FLAG) compiler is available for the Sigma 5, 6, 7, 8, and 9. FLAG is designed for

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one-pass operation to compile and execute a small-to-medium-size program without leaving main memory.

Extended FORTRAN IV-H is another one-pass compiler for operation under BCM, BTM, BPM or RBM on the Sigma 5, 6, 7, 8, and 9. This compiler produces re-entrant programs with a number of extensions beyond ANS FORTRAN. Among these are IMPLICIT statements, END and ERROR options on READ statements, an in-line assembly-language option, run-time path-of-flow tracing for debugging, etc. Extended FORTRAN IV-H is intended for use on smaller-configuration systems, and provides a high degree of compatibility with the FORTRAN compilers of numerous other computer vendors.

Extended FORTRAN IV is another superset of ANS FORTRAN for the Sigma 5 through 9. This 3-pass compiler requires more memory for compilation than Extended FORTRAN IV-H, but produces more efficient code along with extensive diagnostics to reduce debug time. Extended FORTRAN IV runs under RBM, BPM, BTM, CP-R, or CP-V. In addition to producing re-entrant object code, this compiler offers mixed-mode expressions, punctuation flexibility, automatic double precision, generalized DO loops and subscripts, bit manipulation, etc.

ASSEMBLERS: Four assemblers are offered for the Sigma Series: Symbol, Extended Symbol, Macro Symbol, and Meta Symbol.

Symbol is the basic assembler under BCM, RBM, BPM, or BTM for the Sigma 3 through 8. It provides essential literal and external referencing capabilities, common area definitions, absolute or relocatable program segments, and conditional assembly.

Extended Symbol, available for the Sigma 3 only, is a 3-pass assembler under RBM that is upward-compatible with basic Symbol on the larger Sigmas. A concordance (cross-reference table that lists the data and/or statement names) and a macro capability are the primary enhancements over basic Symbol. Many of the features of Extended Symbol are found in either Meta Symbol or Macro Symbol on higher-numbered versions of the Sigma Series.

The Xerox Assembly Processor (AP) is a four-phase macro assembler that executes in the background area of CP-R. AP allows recursive procedures, conditional coding to control assembly, arithmetic and Boolean operators, and updating of source programs during assembly.

Meta Symbol is the full-scale Xerox assembler used under BPM, CP-R, and VP-V. It includes provisions for procedure-oriented statements, symbolic references, etc. This 3-pass assembler allows parameter testing during assembly that can vary the generated code. Other features of Meta Symbol include self-defining constants, full use of lists and subscripted elements, automatic alignment of instructions on word boundaries, etc. Meta Symbol runs on all Sigma processors except the Sigma 3.

RPG: A Report Program Generator (RPG II) is available for the Sigma 3 and operates as a background batch job. The generator accepts RPG input that has been coded for the IBM 1800, 1130, or 360/20 computers. Other features include the selective execution of RPG suroutines, printing of multiple lines per input record by dynamically altering the normal RPG logic flow, full user control over spacing, specialized edit codes, and the ability to use indexed sequential files. RPG will operate on a minimum Sigma 3 with 8K words of memory.

An industry-compatible RPG compiler is available for larger Sigma series computer systems operating under the CP-V operating system.

BASIC: A compiler for the BASIC language is usable in either the batch or on-line mode of operation on Sigma 5, 6, 8, and 9 systems under BTM or BPM. An extended version is also available for use under CP-V.

MANAGE: This generalized file management system can be used for developing and updating files as well as for the production of reports based upon data selection criteria specified by the programmer. MANAGE is available for use on 32K-word Sigma 5, 6, 8, and 9 systems under BPM. MANAGE consists of four separate processors: file creation (DICTNARY), file maintenance (FILEUP), data retrieval (RETRIEVE), and report generation (REPORT). The system processes sequential files of fixed or variable-length records, and may produce up to 99 separate reports in a single pass of RETRIEVE. Up to 9 levels of control breaks are provided. MANAGE requires 15K words of main memory and 28K words of RAD storage, plus additional peripheral storage for data bases and communiation files. Basic security provisions are included, and audit trails of data base updates can be maintained. Retrieval requests use AND/OR logic, with up to 20 consecutive AND's permitted in a single data-qualifying statement. The normal range of relational operators and arithmetic associations is provided. A number of basic defaults are included in the REPORT phase, most of which can be overridden by the user. TOM, a terminal-oriented version of MANAGE, is also available.

EXTENDED DATA MANAGEMENT SYSTEMS: EDMS has many similarities to Honeywell's time-proven Integrated Data Store (IDS). As a generalized data management system, EDMS uses the random file facilities of BPM, BTM, or CP-V File Management for batch or on-line operation on the Sigma 5 and larger models. Closed chains or rings of pointers are used to maintain data element relationships, with optional secondary indices for specified fields. This secondary indexing is a form of partial file inversion to greatly speed data retrievals using frequently keyed-upon fields. Extensive security provisions are for various types of data base access make use of passwords. EDMS consists of three basic programs: file definition processor (FDP), data base manager (DBM), and data base utility routines (DUR). The features of EDMS include multi-level, hierarchical (tree structure) data organization using repeating groups, with audit trails, direct (random) storage and retrieval of data, etc.

APL: Full APL is available under CP-V, and does not require that the system be dedicated to APL exclusively.

TEXT: Xerox offers a TEXT publication processor under UTS that is functionally identical with IBM's ATS/360.

UTILITY ROUTINES: Sort/merge programs are offered at all six levels of software support for the Sigma Series. All are generalized programs which are controlled by user-supplied parameters, and all can accommodate either fixed or variable-length records. Each software level also includes an appropriate number of data transcription, diagnostic, mathematical, and other utility routines. IBM

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1400 simulation routines are available for the Sigma 5 and larger models.

APPLICATION PROGRAMS: A number of applications programs are available from Xerox on an unbundled (separately priced) basis.

General Purpose: Discrete Simulaor (GPDS) is a version of IBM's GPSS that runs on a Sigma 5, 6, 7, or 9 under BPM, BTM, or CP-V.

Functional Mathematical Programming System (FMPS) is a linear programming system developed jointly with Bonner and Moore Associates. FMPS operates on a Sigma 5, 6, 7, or 9. GAMMA III is an adjunct to FMPS that formulates linear programming problems into specialized matrix notation to simplify FMPS input.

CIRC is a sophisticated circuit design and analysis tool for electrical engineers that runs under BPM, BTM, or CP-V on the Sigma 5 and larger models. Three versions are available: CIRC-DC (direct current), CIRC-AC (alternating current), and CIRC-TR (transient analysis).

Simulation Language (SL-1) provides digital or hybrid simulation through a superset of IBM's Continuous System Simulation Language (CSSL) under RBM, BPM, or BTM on a Sigma 5, 7, or 9. A version called CSS/3 is available for the Sigma 3.

In addition to the applications supported by Xerox, more than 1,000 programs are listed in the Xerox Users' Group Catalog of Programs.

USERS' GROUP: Xerox has a users' group composed of over 1200 active members. Semiannual meetings are held to coincide with the Joint Computer Conferences, and a newsletter, *User News*, is published monthly. A number of Special Interest Groups have been formed, covering topics such as commercial Sigma applications, real-time operation, educational applications, etc. A comprehensive catalog of the Xerox Users' Group programs is available from Xerox. For further information, contact: Secretary, Xerox Users' Group, Xerox Corporation, 701 South Aviation Blvd., El Segundo, California 90245.

PRICING

EQUIPMENT: All necessary control units, I/O processors, and adapters are included in the indicated prices for the following typical configurations, and the quoted one-year rental prices include equipment maintenance. Note that numerous special interface units and communications controllers for real-time and on-line use have not been included.

SIGMA 3 DISK (EXPANDED RBM) SYSTEM: Consists of a 16K-word (32K-byte) Central Processor, 7203 RAD Storage System (1.5 MB), 8195 Magnetic Tape System, 7122 Card Reader (400 cpm), 7121 Card Punch (200 cpm), 7440 Line Printer (628-795 lpm), and 8192 Printer-Keyboard. Monthly rental and purchase prices are approximately **$4,739** and **$187,759,** respectively, and monthly maintenance (for purchased systems) is **$1,446.**

SIGMA 5 DISK (EXPANDED RBM) SYSTEM: Consists of a 24K-word (96K-byte) Central Processor, 7246 Disk Storage Drive (24.58 MB), 7203 RAD Storage System (1.5 MB), 7122 Card Reader (400 cpm), 7160 Card Punch (300 cpm), 7440 Line Printer (628-795 lpm), and 7012 Printer-Keyboard. Monthly rental and purchase prices are approximatly **$8,557** and **$334,712,** respectively, and monthly maintenance (for purchased systems) is **$2,063.**

SIGMA 7 TAPE/DISK/RAD (BTM) SYSTEM: Consists of a 48K-word (192K-byte) Central Processor, 7242 Disk Storage Unit (49.16 MB), 7204 RAD Storage Unit (1.5 MB), one 7315 Magnetic Tape Control and Magnetic Tape Drive and one additional 7316 Magnetic Tape Drive (60KB), 7122 Card Reader (400 cpm), 7160 Card Punch (300 cpm), 7441 Line Printer (1100 lpm), and 8495 System Supervisory Console. Monthly rental and purchase prices are approximately **$35,369 and $734,429,** respectively, and monthly maintenance (for purchased systems) **is $3,832.**

SIGMA 8 TAPE/DISK/RAD (BPM) SYSTEM: Consists of a 64K-word (256K-byte) Central Processor, one 7242 Disk Storage Unit (49.16 MB), two 7212 RAD Storage Units (11.75 MB), one 7315 Magnetic Tape Control and Tape Drive and one additional 7316 Tape Drive (60KB), 7122 Card Reader (400 cpm), 7160 Card Punch (300 cpm), 7441 Line Printer (1100 lpm), and 7020 Printer-Keyboard. Monthly rental and purchase prices are approximately **$24,085** and **$770,328,** respectively, and monthly maintenance (for purchased systems) is **$4,932.**

SIGMA 9 TAPE/DISK/RAD (CP-V) SYSTEM: Consists of a 256K-word (1024K-byte) Central Processor, four 7242 Disk Storage Units (196.64 MB), four 7212 RAD Storage Units (23.50 MB), four 7332 Magnetic Tape Units (120KB), two 7122 Card Readers (400 cpm), one 7140 Card Reader (1500 cpm), two 7160 Card Punches (300 cpm), two 7446 Line Printers (1500 lpm), and two 7020 Printer-Keyboards. Monthly rental and purchase prices are approximately **$45,283 and $1,598,209,** respectively, and monthly maintenance (for purchased systems) is **$11,156.**

SOFTWARE: Xerox was among the first mainframe vendors to price applications software separately. This policy applies to the major applications systems developed by Xerox or by outside sources under contract to Xerox. Such software is currently limited to a handful of applications-oriented packages. Operating systems, utilities, and language processors are bundled at no additional cost to Sigma users. A number of the separately priced applications packages are provided at no charge to qualified educational institutions.

SUPPORT: Xerox has formed a Commercial Systems Integration Group to provide systems engineering and field support to customers. "Emergency" operating system software support is available from Field Engineers at $25/hour on weekdays and $28/hour on Sundays and holidays. On-site custom software assistance is provided by Systems Engineers at $25/hour for small Sigma 3 systems and $30/hour for more complex systems.

EDUCATION: Xerox maintains an Education Center in Los Angeles at which standard and special courses are taught. These courses cover all aspects of Sigma usage and range in length from 2 to 10 days, at costs ranging from $100 to $300. A training program consisting of a number of courses may be desired, depending upon customer requirements. On-site training can be arranged at negotiated charges.

CONTRACT TERMS: Xerox offers a purchase agreement for Sigma computer systems, and 1, 4, or 6-year lease terms. A 9-hour weekday principal period of maintenance is included at no additional charge for leased Sigma systems. Additional maintenance support is available: Saturday or Sunday coverage is offered at a premium of 20% of the separate maintenance charge; 16-hour maintenance is available for 5, 6, or 7 days per week at premiums of 40%, 70%, or 90%, respectively, of the separate maintenance charge; and 24-hour maintenance is available for 5, 6, or 7 days per week at premiums of 115%, 125%, or 140%, respectively, of the separate maintenance charge. ■

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease)*	Rental (6-year lease)*
SIGMA 3 PROCESSOR AND MAIN STORAGE						
8101**	Sigma 3 CPU including IIOP w/4 Channels, 1 Port, and 8K 16 bit words of Memory	31,482	222	852	730	648
8102**	Sigma 3 CPU including EIOP w/8 Channels, 2 Ports, 8K 16-bit words of Memory, and DIO Interface	40,068	256	1,084	929	825
8105	Integral I/O Processor (IIOP) with 4 I/O Channels	6,868	33	185	159	142
8111	Two Real Time Clocks	572	5	16	13	12
8113	Power Fail-Safe Interrupt	1,145	5	31	27	24
8114	Fault Interrupt & Protect Feature—includes Interface Time & Memory Parity	2,862	16	77	68	59
8119	Extended Arithmetic Unit	2,862	16	77	68	59
8121	Interrupt Control Chassis	2,517	11	89	57	52
8122	Priority Interrupt, 2 Levels (for 8121)	402	0	12	10	8
8123	Two Integral Priority Interrupt Levels (for 8101 or 8102)	917	5	25	22	18
8150	Sigma 5/7 Memory Adapter	8,586	44	232	199	177
8151	Basic Memory Module, 8K 16-bit Words (first and odd-numbered subsequent memory increments)	19,461	95	525	449	400
8152	Memory Increment, 8K 16-bit Words (second and even-numbered subsequent memory increments)	13,738	67	371	318	283
8155	Additional Memory Port	1,717	11	47	40	35
8170	External Interface Feature	1,145	5	30	26	24
8171	External I/O Processor (EIOP) With 8 I/O Channels (requires 8155 and 8170)	13,738	67	371	318	283
8172	Additional 8 I/O Channels (for CPU, IIOP, or EIOP)	4,579	22	124	106	94
8175	Two-Byte Interface (for 8102 or EIOP)	1,717	11	47	40	35
8191	First Keyboard Printer—KSR-35 (Console for Sigma 3 only)	4,579	39	124	106	94
8192	First Keyboard Printer—ASR-35 w/Paper Tape Reader & Punch (Console for Sigma 3 only)	6,869	56	186	159	142
8195	Magnetic Tape Controller plus one Tape Drive (For Sigma 3 only)	15,000	206	562	528	500
8196	Add-On Tape Drive (For 8195)	8,000	155	337	317	300
SIGMA 5 PROCESSOR AND MAIN STORAGE						
8201	Sigma 5 CPU including Integral I/O Processor, two Real-Time Clocks, Control Panel, & Power Supplies	74,200	501	1,855	1,744	1,651
8202	Sigma 5 CPU without Integral I/O Processor	68,900	473	1,723	1,620	1,442
8203	Integral I/O Processor (IIOP)	7,950	27	199	188	178
8211	Two Additional Real-Time Clocks	1,060	6	27	25	24
8213	Power Fail-Safe	1,060	6	27	25	24
8214	Memory Protect	4,240	16	106	100	94
8216	Additional Register Block	2,650	11	67	64	59
8218	Floating-Point Arithmetic	10,600	111	265	249	236
8221	Interrupt Control Chassis (Required for 8270)	2,332	32	58	55	52
8222	Priority Interrupt, 2 Levels (Requires 8270)	371	0	10	10	8
8261	Memory Bank, 8K 32-bit Words (first and odd-numbered subsequent memory modules)	44,520	134	1,113	1,046	991
8262	Memory Increment, 8K 32-bit Words (second and even-numbered subsequent memory modules)	32,860	122	822	773	731
8264	Each Port Expansion (Required for each pair of 8261's in same memory cabinet)	4,240	22	106	100	94
8270	External Interface Feature (Requires 8221)	2,120	11	53	50	48
8273	Multiplexer Input/Output Processor (MIOP); includes eight Multiplexer Channels	21,200	89	530	498	472
8275	4-Byte Interface Feature for MIOP	2,650	16	67	64	59
8276	Additional Eight Multiplexer Channels for MIOP	4,240	16	106	100	94
8277	Bus-Sharing MIOP	15,900	89	398	374	354
8285	Selector Input/Output Processor (SIOP)	31,800	111	795	747	708
SIGMA 6 PROCESSOR AND MAIN STORAGE						
8310A	Sigma 6 CPU including Multiplexer I/O Processor (MIOP) w/8 channels & 4-byte Interface Feature, Decimal	207,760	1,391	8,130	7,643	7,237

*Rental prices include monthly maintenance charges.
**Minimum monthly rental for a Sigma 3 system is $1200.

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		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease)*	Rental (6-year lease)*
SIGMA 6 PROCESSOR AND MAIN STORAGE (Continued)						
	Arithmetic, Memory Map w/Access Protection, Memory Write Protection, Two Register Blocks, Two Real Time Clocks, Power Fail-Safe, External Interface, Dual Access (2 port), and 32K 32-bit words of memory					
8310B	Same as above, with 48K 32-bit words	266,060	1,663	9,922	9,326	8,831
8310C	Same as above, with 64K 32-bit words	303,160	1,935	11,284	10,607	10,042
8310D	Same as above, with 80K 32-bit words	325,420	2,209	13,075	12,291	11,638
8310E	Same as above, with 96K 32-bit words	347,680	2,481	13,769	12,944	12,256
8310F	Same as above, with 112K 32-bit words	369,940	2,753	14,877	13,985	13,242
8310G	Same as above, with 128K 32-bit words	392,200	3,026	15,571	14,638	13,860
8311	Two Additonal Real-Time Clocks	1,060	6	27	25	24
8316	Additional Register Block	2,650	11	67	64	59
8318	Floating-Point Arithmetic Unit	26,500	111	663	623	590
8321	Interrupt Control Chassis (Required for 8322)	2,332	32	58	55	52
8322	Priority Interrupt, 2 Levels (Requires 8321)	371	0	10	10	9
8364A	Each Port Expansion for 8310A	4,240	22	106	100	94
8364B,C	Each Port Expansion for 8310B, C	8,480	44	212	199	189
8364D,E	Each Port Expansion for 8310D, E	12,720	67	318	299	283
8364F,G	Each Port Expansion for 8310F, G	16,960	89	424	399	377
8370	Additional MIOP w/8 Channels and 4-Byte Interface Feature	23,850	106	597	562	532
8375	I/O Processor (IOP) Expansion Feature; 8 Channels, 4-Byte Interface Feature (For MIOP)	18,550	106	464	437	413
8376	Additional 8 Multiplexer Channels (For MIOP)	4,240	16	106	100	94
8385	Selector I/O Processor (SIOP)	31,800	111	795	747	708
SIGMA 7 PROCESSOR AND MAIN STORAGE						
8401	Sigma 7 CPU including two Real-Time Clocks, Control Panel, and Power Supplies	215,180	730	5,380	5,057	4,788
8411	Two Additional Real-Time Clocks	1,060	6	27	25	24
8413	Power Fail-Safe	1,060	6	27	25	23
8414	Memory Protect	5,300	23	133	125	119
8415	Memory Map	34,450	90	862	810	767
8416	Additional Register Block	2,650	11	67	64	59
8418	Floating-Point Arithmetic	26,500	112	663	623	590
8419	Decimal Arithmetic	31,800	135	795	747	708
8421	Interrupt Control Chassis (Required for 8422)	2,332	33	58	55	52
8422	Priority Interrupt, 2 Levels (Requires 8421)	371	0	10	10	9
8461	Memory Bank, 8K 32-bit Words (first and odd-numbered subsequent memory modules)	38,000	151	950	893	846
8462	Memory Increment, 8K 32-bit Words (second and even-numbered subsequent memory modules)	25,069	123	628	589	559
8464	Each Port Expansion (Required for each pair of 8461's in same memory cabinet)	4,240	23	106	100	94
8473	Multiplexer Input/Output Processor (MIOP), including eight Multiplexer Channels	21,200	90	530	498	472
8475	4-Byte Interface Feature for MIOP	2,650	17	67	64	59
8476	Additional Eight Multiplexer Channels for MIOP	4,240	17	106	100	94
8477	Bus-Sharing MIOP	15,900	90	398	374	354
8485	Selector Input/Output Processor (SIOP)	31,800	112	795	747	708
8495	System Supervisory Console (For Sigma 7 only)	26,500	112	663	623	590
SIGMA 8 PROCESSOR AND MAIN STORAGE						
8510A	Sigma 8 CPU including Multiplexer I/O Processor (Channel A), 16 General-Purpose Registers, Floating-Point Arithmetic, Memory Write Protect, two Real-Time Clocks, Power Fail-Safe, External Interface, and 16K 32-bit words of memory	238,500	1,455	10,070	9,466	8,962
8510B	Same as above, with 32K 32-bit words	280,900	1,741	10,759	10,113	9,576
8510C	Same as above, with 48K 32-bit words	325,420	2,044	11,872	11,160	10,566
8510D	Same as above, with 64K 32-bit words	367,820	2,331	12,561	11,807	11,180
8510E	Same as above, with 80K 32-bit words	412,340	2,634	13,674	12,854	12,170
8510F	Same as above, with 96K 32-bit words	454,740	2,920	14,363	13,501	12,784

*Rental prices include monthly maintenance charges.

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		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease)*	Rental (6-year lease)*
SIGMA 8 PROCESSOR AND MAIN STORAGE (Continued)						
8510G	Same as above, with 112K 32-bit words	499,260	3,224	15,496	14,547	13,774
8510H	Same as above, with 128K 32-bit words	541,660	3,510	16,165	15,196	14,387
8511	Two Additional Real-Time Clocks	1,060	6	27	25	24
8516	Additional Register Block	2,650	11	87	64	60
8517	Alternate CPU Bus	3,180	11	80	75	71
8521	Interrupt Control Chassis (Required for 8522)	2,332	33	58	55	52
8522	2 Levels of Priority Interrupt (Requires 8521)	371	0	10	10	9
8560	Memory Reconfiguration Control Unit	4,240	11	106	100	94
8564A,B	Each Port Expansion for 8510A, B	5,088	28	127	120	113
8564C,D	Each Port Expansion for 8510C, D	10,176	56	254	240	227
8564E,F	Each Port Expansion for 8510E, F	15,264	84	382	359	340
8564G,H	Each Port Expansion for 8510G, H	20,352	112	509	479	454
8570	Additional MIOP—Channel A	21,200	174	530	498	472
8571	4-Byte Interface (For MIOP)	3,180	17	80	75	71
8572	8 Additional Subchannels (For MIOP)	4,240	17	106	100	94
8573	Memory-to-Memory Move (For MIOP)	2,968	17	74	70	67
8574	Alternate MIOP Bus (For MIOP—Channel A)	3,180	11	80	75	71
8575	MIOP—Channel B	15,900	174	398	374	354
8580	High Speed RAD IOP (HSRIOP); includes control for 7212 RAD	47,700	225	1,193	1,121	1,062
8584	Alternate HSRIOP Bus (For HSRIOP)	3,180	11	80	75	71
SIGMA 9 PROCESSOR AND MAIN STORAGE						
8610A	Sigma 9 CPU including Decimal Arithmetic Unit, Floating-Point Arithmetic Unit, Memory Map w/Access Protection, Memory Write Protection, two Register Blocks, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Chassis, Eight Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 subchannels), Motor Generator Set, and 64K 32-bit words of memory	450,500	2,516	14,098	13,252	12,547
8610B	Same as above, with 80K 32-bit words	477,000	2,819	14,946	14,050	13,302
8610C	Same as above, with 96K 32-bit words	503,500	3,122	15,794	14,846	14,056
8610D	Same as above, with 112K 32-bit words	530,000	3,426	16,642	15,643	14,811
8610E	Same as above, with 128K 32-bit words	556,500	3,527	17,490	16,440	15,566
8610F	Same as above, with 160K 32-bit words	609,500	4,133	19,186	18,035	17,075
8610G	Same as above, with 192K 32-bit words	662,500	4,538	20,776	19,529	18,490
8610H	Same as above, with 224K 32-bit words	715,500	5,144	22,472	21,123	20,000
8610I	Same as above, with 256K 32-bit words	768,500	5,549	24,062	22,618	21,415
8610J	Same as above, with 320K 32-bit words	874,500	6,560	27,348	25,707	24,340
8610K	Same as above, with 384K 32-bit words	980,500	7,570	30,634	28,796	27,264
8610L	Same as above, with 448K 32-bit words	1,086,500	8,582	33,920	31,884	30,190
8610M	Same as above, with 512K 32-bit words	1,192,500	9,592	37,206	34,973	33,113
8611	Two Additional Real-Time Clocks	1,060	6	24	23	21
8616	Additional Register Block	2,650	11	69	65	61
8617	Alternate CPU Bus	3,180	11	71	67	64
8621	Additional Interrupt Controller	2,332	33	57	54	33
8622	Priority Interrupt, 2 Levels	371	0	11	10	10
8664A	Each Port Expansion for 8610A	8,140	56	204	192	182
8664B,C	Each Port Expansion for 8610B, C	12,211	84	305	288	271
8664D,E	Each Port Expansion for 8610D, E	16,282	112	408	383	363
8664F	Each Port Expansion for 8610F	20,352	140	510	479	454
8664G	Each Port Expansion for 8610G	24,422	138	610	573	544
8664H	Each Port Expansion for 8610H	28,493	197	712	670	634
8664I	Each Port Expansion for 8610I	32,563	225	815	766	725
8664J	Each Port Expansion for 8610J	40,704	280	1,019	957	906
8664K	Each Port Expansion for 8610K	48,844	337	1,221	1,148	1,087
8664L	Each Port Expansion for 8610L	56,985	393	1,425	1,340	1,269
8664M	Each Port Expansion for 8610M	65,126	450	1,629	1,532	1,450
8670	Additional MIOP—Channel A	21,200	174	472	443	420
8671	Four-Byte Interface (For MIOP)	3,180	17	71	67	64
8672	Additional Eight Subchannels (For MIOP)	4,240	17	94	89	84
8673	Memory-to-Memory Move (For MIOP)	2,968	17	67	63	59

*Rental prices include monthly maintenance charges.

Xerox Sigma Series

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease)*	Rental (6-year lease)*
SIGMA 9 PROCESSOR AND MAIN STORAGE (Continued)						
8674	Alternate 8670 Bus (For MIOP)	3,180	11	71	67	64
8675	MIOP—Channel B	15,900	174	354	333	315
8680	High Speed RAD IOP (HSRIOP); includes control for 7212 RAD	47,700	225	1,060	996	943
8684	Alternate HSRIOP Bus (For HSRIOP)	3,180	11	71	67	64
SIGMA 9 MODEL 3 PROCESSOR AND MAIN STORAGE						
8710	Sigma 9 Model 3 CPU including Floating-Point Arithmetic Unit, Memory Map with Access Protection, Register Block, two Real-Time Clocks, Power Fail-Safe, External Interface, Interrupt Control Chassis, two Interrupt Levels, Multiplexer I/O Processor (Channel A w/8 Subchannels), and 32K 32-bit words of memory	285,000	1,650	10,329	9,934	9,340
8711	Two Additional Real-Time Clocks	1,060	6	24	23	21
8716	Additional Register Block	2,650	11	69	65	61
8717	Alternate CPU Bus	3,180	11	71	67	64
8721	Additional Interrupt Controller	2,332	33	57	54	51
8722	Priority Interrupt, 2 Levels	371	0	11	10	10
8760	Memory Reconfiguration Control	4,240	11	106	100	94
8762A	16K Expansion Memory (Basic Memory Cabinet w/2 Ports)	26,500	111	848	797	755
8762B	16K Expansion Memory Increment	26,500	111	848	797	755
8766	Memory Port Expansion	4,070	28	103	95	89
8770	Additional MIOP—Channel A	21,200	174	472	443	420
8771	Four-Byte Interface	3,180	17	71	67	64
8772	Additional 8 Subchannels	4,240	17	94	89	84
8773	Memory-to-Memory Move	2,968	17	67	63	59
8774	Alternate MIOP Bus	3,180	11	71	67	64
8775	MIOP—Channel B	15,900	174	354	333	315
8780	High-Speed RAD IOP	47,700	225	1,060	996	943
8784	Alternate 8780 Bus	3,180	11	71	67	64
CONSOLE INPUT/OUTPUT						
7012	Keyboard/Printer & Controller (KSR-35); 10 cps	6,360	52	159	149	142
7014	Spare Mechanism for 7012 or 8091	3,960	0	99	94	89
7020	Keyboard/Printer (10 cps) w/Paper Tape Punch/Reader (10/19 cps) and Controller (ASR-35)	7,950	57	199	188	178
7021	Spare Mechanism for 7020 or 8092	5,500	0	138	130	123
MASS STORAGE						
7201	Rapid Access Data (RAD) Controller (for up to eight 7202, 7203, or 7204 RAD Storage Units in any combination)	8,480	39	212	199	189
7202	RAD Storage Unit; 0.75MB, 188,000 bytes/sec.	14,300	103	358	336	319
7203	RAD Storage Unit; 1.5MB, 188,000 bytes/sec.	26,400	137	660	620	587
7204	RAD Storage Unit; 3.0MB, 188,000 bytes/sec.	38,500	200	963	905	851
7211	Rapid Access Data (RAD) Controller (connected to Selector I/O Processor for up to four 7212 RAD Storage Units)	19,080	56	477	448	425
7212	RAD Storage Unit; 5.4MB (may be directly connected to Sigma 9 High-Speed RAD IOP)	66,000	286	1,650	1,551	1,469
7231	Extended Performance Rapid Access Data (RAD) Controller (for up to four 7232 RAD Storage Units)	14,840	79	371	349	331
7232	Extended Performance RAD Storage Unit; 6.3 MB	55,000	286	1,375	1,293	1,224
7235	Extended Width Interface Feature for 7231 (provides 4-byte data path through IOP channel)	2,750	17	69	66	62
7236	Extended Width Rapid Access Data (RAD) Controller (for up to four 7232 RAD Storage Units)	28,090	56	703	660	625
7240	Disk Controller (connected to any I/O Channel for up to 8 spindles in 7242 and/or 7246 Disk Storage Units)	21,200	112	530	498	472
7241	Extended Width Interface Feature for 7240 (provides 4-byte data path)	2,750	17	69	66	62

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Xerox Sigma Series

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease)*	Rental (6-year lease)*
MASS STORAGE (Continued)						
7242	Disk Storage Unit; Removable, Dual Spindle, 49.15 MB	27,500	303	880	827	783
7243	Device Pooling Feature (for 7242 to provide dual access by two 7240's)	8,800	56	220	207	196
7244	Disk Pack for 7242 or 7246 Disk Storage Units; 24.58 MB	660	0	34	34	34
7246	Disk Storage Unit; Removable, Single Spindle, 24.58 MB	16,500	229	495	465	440
7247	Device Pooling Feature, Single Spindle (for 7246 to provide dual access by two 7240's)	5,500	45	137	130	122
7260	Disk Controller plus two 7261 Disk Drives (90MB)	91,600	477	2,290	2,153	2,038
7261	Disk Drive (45MB)	19,600	148	490	461	436
1032	Second Controller (for 7260 dual access)	40,000	177	1,000	940	890
1033	Dual Access (for 7261 Disk Drive)	5,000	26	125	117	111
7265	Disk Controller plus three 7266 Disk Drives (273MB)	145,000	625	3,625	3,408	3,226
7266	Disk Drive (91MB)	20,000	150	500	470	445
1034	Second Controller (for 7265 dual access)	45,000	175	1,125	1,058	1,001
1035	Dual Access (for 7266 Disk Drive)	5,000	25	125	117	111
7264	Disk Pack (for 7261 or 7266 Disk Drive)	600	N/A	31	31	31
MAGNETIC TAPE INPUT/OUTPUT						
7315	Magnetic Tape Controller and one Tape Unit	16,960	216	636	583	530
7316	Add-on Tape Drive; 60KB	13,200	194	495	464	440
7322	Tape Unit; 60KB	13,200	194	495	464	440
7330	Magnetic Tape Controller; 1600 bpi	30,104	123	753	707	670
1038	Magnetic Tape Controller, 800 bpi option for 7330	4,240	28	106	99	94
1039	Extended Width Interface for 1600 bpi Controller	2,750	17	69	66	62
7332	Tape Unit; 1600 bpi, 120KB	20,350	172	479	450	426
7333	Tape Unit; 1600 bpi, 240KB	28,435	212	671	630	597
7361	Magnetic Tape Controller; 556 bpi	6,360	45	159	149	142
7362	Tape Unit; 19.7KB	20,900	144	523	492	465
7365	BCD Option	2,200	NC	55	52	51
7371	7-Channel Tape System Controller	23,320	112	583	548	519
7372	7-Channel Tape Unit; 200/556/800 bpi, 15/41.7/60 KB	29,700	212	743	698	661
7374	Binary Packing Option	3,520	NC	88	84	79
OTHER INPUT/OUTPUT UNITS						
7121	Card Reader (including control); 200 cpm	7,950	59	233	219	208
7122	Card Reader (including control); 400 cpm	12,720	137	424	399	377
7140	Card Reader (including control); 1500 cpm	25,440	206	636	598	566
7160	Card Punch (including control); 300 cpm	33,920	286	848	797	755
7165	Card Punch (including control); 100 cpm	20,766	151	519	489	463
7440	Buffered Line (drum) Printer; 628 lpm, 132 positions	37,100	286	928	872	826
7441	Buffered Line (drum) Printer; 1100 lpm, 132 positions	48,760	315	1,219	1,146	1,085
7446	Buffered Line (drum) Printer; 1500 lpm, 132 positions	65,720	378	1,537	1,445	1,368
7450	Buffered Line (drum) Printer; 225 lpm, 128 positions	23,850	160	597	562	532
7060	Paper Tape Reader (7062), Punch (7063), Spooler (7064), w/Controller & Rack (7061)	11,660	97	318	299	283
7061	Paper Tape Equipment Cabinet & Controller	7,420	34	186	175	165
7062	Paper Tape Reader; 300 cps	2,200	17	55	52	51
7063	Paper Tape Punch; 120 cps	2,750	29	69	66	63
7064	Paper Tape Spooler	1,650	12	42	40	37
7530	Incremental Graph Plotter (11-inch)	13,780	86	345	324	307
7531	Incremental Graph Plotter (30-inch)	23,320	114	583	548	519
7534	Graph Plotter Controller (For 7530 or 7531)	3,180	27	101	95	90
COMMUNICATION CONTROLS						
3625	Communications Processor; includes 8K memory and CPU interfaces	36,600	179	1,200	1,125	1,075
3630	Communications Processor Expansion Feature	7,670	30	240	225	215
3635	Send/Receive Unit	5,900	30	215	198	175
3636	4K Data Memory Increment	1,650	9	59	52	46
3650	Dual Multimode Line Interface	1,200	7	43	38	30
7601A-E	Data Set Controller	7,420	39	186	175	165
7602	Full Duplex Feature (for 7601)	880	0	22	21	20
7603	Automatic Dialing Feature (for 7601)	880	0	22	21	20

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Xerox Sigma Series

		Purchase Price	Monthly Maint.	Rental (1-year lease)*	Rental (4-year lease)*	Rental (6-year lease)*
COMMUNICATION CONTROLS (Continued)						
7604	Local Batch Terminal Controller	8,904	39	223	210	198
7605A-E	Procedure-Oriented Data Set Controller	10,070	54	252	237	225
7611	Character-Oriented Communications Subsystem (for up to 64 simultaneous remote devices)	11,130	51	279	263	247
7612	Timing Module for 7615/7616 (a maximum of 5 may be connected to a 7611)	275	0	7	7	7
7613	Line Interface Unit (a maximum of 7 may be connected to a 7611 for up to 64 lines)	1,100	0	28	26	25
7615A-D	Formatted Send Module (one per 7611 line)	275	3	7	7	7
7616A-D	Formatted Receive Module (one per 7611 line)	275	3	7	7	7
7623	DC Power Supply (for 7611)	1,100	6	28	26	25
7618	Automatic Dialing Unit (controls 1 Bell System 800 Series Automatic Call Unit)	6,050	45	152	143	135
7619	Additional Dialing Position (up to 15 may be added to a 7618 for a total of 16 dialers)	550	0	14	14	13
7630	Communications Controller Plus 8 Lines	14,840	51	371	349	331
7631	8-Line Expansion Unit	6,380	33	160	151	143
7650	Channel Interface Unit for inter-processor data transmission	8,250	56	207	195	185

*Rental prices include monthly maintenance charges.

SOFTWARE PRICES

Program Product	Monthly Use Fee	Prepaid Use Fee
SL-1	200	10,000
FMPS	Not avail.	15,000
GAMMA III	Not avail.	7,500
GPDS	72	3,600
CIRC-DC	78	3,900
CIRC-AC	24	1,200
CIRC-TR	59	2,950
ACES (Administrative and Classroom Education System):		
Control Program	30	1,500
Financial Accounting	17	850
Payroll and Personnel	33	1,650
Stores Inventory	17	850
Accounts Payable	33	1,650
Student Work Continuation Program	50	2,500
Attendance Accounting	16	800
Student Scheduling	16	800
Mark Reporting, Education Planning, and Guidance Reporting	26	1,300
Test Reporting	32	1,600

Xerox Sigma Series

NEW PRODUCT ANNOUNCEMENT

During the month of April 1975, Xerox added two new features for its large-scale processor models. The first, a multiprocessing capability, was announced for the Sigma 9, the most powerful computer system in the Xerox product line and the only remaining Sigma Series system that is now being actively marketed. The second important enhancement, announced for both the Sigma 9 and the newer Xerox 560 computers, is a programmable front-end communications processor that allows a single-line interface module to handle a variety of data transmission modes and communications terminals.

The Sigma 9 multiprocessing capability executes under the Xerox Control Program Five (CP-V) operating system and allows from two to four central processors to operate in a "tightly coupled" configuration, sharing main memory and peripherals equally among all central processors. One central processor is designated as the primary processor and handles the scheduling of user programs and input/output operations performed by secondary central processors in the configuration. A system fail-soft capability enables control to be passed to a secondary processor in the event of a failure of the primary processor. The new multiprocessing capability requires an additional 2,048 words of main memory for the resident portion of the operating system and is compatible with user programs and data files developed under earlier releases of CP-V. Purchase prices for Sigma 9 multiprocessing systems are estimated to range from $1 million to $3 million, and delivery is scheduled for the fourth quarter of 1975.

The Xerox 3625 Communications Processor, available for both the Sigma 9 and Xerox 560 systems, is based on a special-purpose Xerox processor that includes from 8K to 32K words of memory, has an instruction cycle time of 350 nanoseconds, and can handle up to 128 communications lines with an aggregate bandwidth of 10,000 characters per second. All standard character lengths of from 5 to 8 bits and 19 asynchronous line speeds ranging from 37.5 to 19,200 bits per second can be accommodated, with a maximum combination of up to 16 different asynchronous line speeds supported by a single system. The new 3650 Dual Multimode Line Interface Module can handle synchronous, asynchronous, and isochronous transmission in a single interface. ("Isochronous" can be defined as the asynchronous transmission of messages whose characters are transmitted synchronously with respect to each other.)

The 3625 currently can support the following terminals: Teletype Models 33, 35, and 38; the IBM 2741; the IBM 360/20, the Xerox 530 Satellite Processor, and other HASP Version 3.1 terminals; and the IBM 3270 or its equivalent operating as a transaction processing terminal.

The 3625 is scheduled for delivery in the fourth quarter of 1975. Purchase price for a typical 3625 system with 32 synchronous and asynchronous communications lines is estimated at $55,800, and one-, four-, and six-year lease terms are also offered. Detailed prices are included in the newly updated Xerox price lists in Reports 70C-931-01 and 70C-931-02.