DEC PDP-11 Family
New Product Announcement: PDP-11/60

In March 1977, Digital Equipment Corporation announced a new mid-range member of its extensive PDP-11 minicomputer line. The new PDP-11/60 offers performance levels between those of the PDP-11/34 and the PDP-11/70. Designed as a FORTRAN machine, the PDP-11/60 is oriented toward high-performance real-time applications and medium-performance, multi-user, multi-task, time-shared applications. Memory is expandable to 256K bytes, and memory relocation and protection are built in. Hardware multiply, divide, and 32- and 64-bit single- and double-precision floating-point arithmetic are standard. The new model is targeted specifically for real-time laboratory, scientific engineering, and educational environments.

The 11/60 CPU represents a new design and incorporates a combination of features found in the smaller PDP-11's and the high-end PDP-11/70, plus a few features that represent innovations for the company. From the PDP-11/70 have come the 11/60's cache memory feature and floating-point instruction set. From the other PDP-11 models, the 11/60 draws the fundamental 16-bit architecture, with none of the 32-bit busses found in the 11/70. Innovations in the new CPU include user-accessible microprogramming, error-correcting memory, and a special firmware diagnostic module for improved availability.

The cache memory in the PDP-11/60 is based on the same 2048-byte, 240-nanosecond cache system used in the PDP-11/70, but is organized into a single field instead of two 1024-byte fields as in the 11/70. According to DEC, this different configuration reduces the average cache "hit rate" to about 87 percent, compared to the 95 percent rate in the PDP-11/70, and produces an effective memory cycle time of about 532 nanoseconds.

A portion of the control store is available for customer use in the PDP-11/60. 2.5K words of this address space are reserved for the base machine. The remaining 1.5K words of address space are used for three immediately available firmware products that offer a high degree of flexibility and provide for future enhancements. Two of the products are User Control Store (UCS—1K address space) and Extended Control Store (ECS—1.5K address space). These products are general-purpose options for use in the development of specific microcode routines for critical applications. The third product is Diagnostic Control Store (DCS—2K address space) and represents a specific, hardware-supported application of ECS. DCS is a fault isolator which facilitates fault isolation in the central processor to the module level.

In particular, the User Control Store, which permits users to develop their own microprograms for specialized functions, is a significant addition to the PDP-11 capabilities. This is the first time DEC has allowed users this capability; and, although only 1024 words of control storage are currently available for user developments, it marks an important new direction for the world's largest minicomputer manufacturer. DEC had long been a holdout against permitting user microprogramming of its products, but increasing user understanding of this previously "black magic" technology has increased the demand for the capability. DEC is still barring extensive incursions into the inner machine by limiting the amount of control storage available to the users. In comparison, the Hewlett-Packard 21 MX-E can accommodate up to 8.5K words of user control storage, and the Data General microNova allows up to 4K words.

The 11/60 offers two different types of floating-point processors, both having the same 46-instruction set found in the PDP-11/70. The integral floating-processor is a firmware implementation added to the standard PDP-11 instruction set. The second version is a new auxiliary floating-point processor, designated the FP11-E, that is capable of performing a 64-bit, register-to-register multiply in 3.74 microseconds. Using this faster floating-point unit, the PDP-11/60 is said to be capable of performance levels between 85 and 90 percent of the 11/70 level.

The 11/60 does not have the high-speed mass-bus used in the PDP-11/45 and 11/70 CPU's, but instead features a Unibus with a broader bandwidth than that of the PDP-11/34 and 11/40 CPU's. With its unique combination of the Unibus and processor cache memory, the PDP-11/60 allows I/O transfers to memory to occur simultaneously with central processor accesses from cache memory. I/O transfers do not cause the CPU to halt, and multi-port memories with a more complex bus structure are not necessary.

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The cache/Unibus arrangement results in a system-oriented computer that can handle high I/O rates without significant degradation of processor speed.

The 11/60 is software-compatible with the other members of the PDP-11 line. It supports the RSX-11M, RSX-11D, RT-11, and IAS operating systems and the FORTRAN IV, FORTRAN IV-PLUS, BASIC-11, and COBOL languages, as well as a great number of optional and applications-oriented products.

Pricing for the PDP-11/60 starts at $35,700 for a single processor for OEM use, and at $44,700 for a packaged end-user system consisting of a CPU with 256K bytes of either core or MOS memory, two 14-megabyte RK06 disk drives, and an LA36 30-cps hard-copy terminal.□

EQUIPMENT PRICES

PACKAGED SYSTEMS		Purchase Price
11 x 60-BA	32K-word CPU in short cabinet; core memory with parity	$31,700
11 x 60-CA	32K-word CPU in short cabinet; ECC MOS memory	25,700
11T60-BA	32K words of core memory; RK05F and RK05J and LA36	50,700
11T60-CA	32K ECC MOS memory; RK05F and RK05J and LA36	44,700
11S60-BA	32K core memory; two RK06 and LA36	67,300
11S60-CA	32K ECC MOS memory; two RK06 and LA36	62,700
MEMORY AND PROCESSOR OPTIONS		
MM11-WP	32K words core memory with parity (11/45 memory)	6,600
MM11-KA	32K words ECC MOS memory	5,000
FP11-E	High-speed floating-point	5,600
KU116-AA	User Control Store (UCS)	5,000
KU116-AB	Extended Control Store (ECS)	1,200
KU116-BB	Diagnostic Control Store (DCS)	3,800

