Computervision

CGP-100/200 Graphics Processor Conversion Module

Logic Diagrams

Document control number: 48-00558

Name: _____

CGP-100/200 Graphics Processor Conversion Module

Logic Diagrams

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Order No. 001-00548-001

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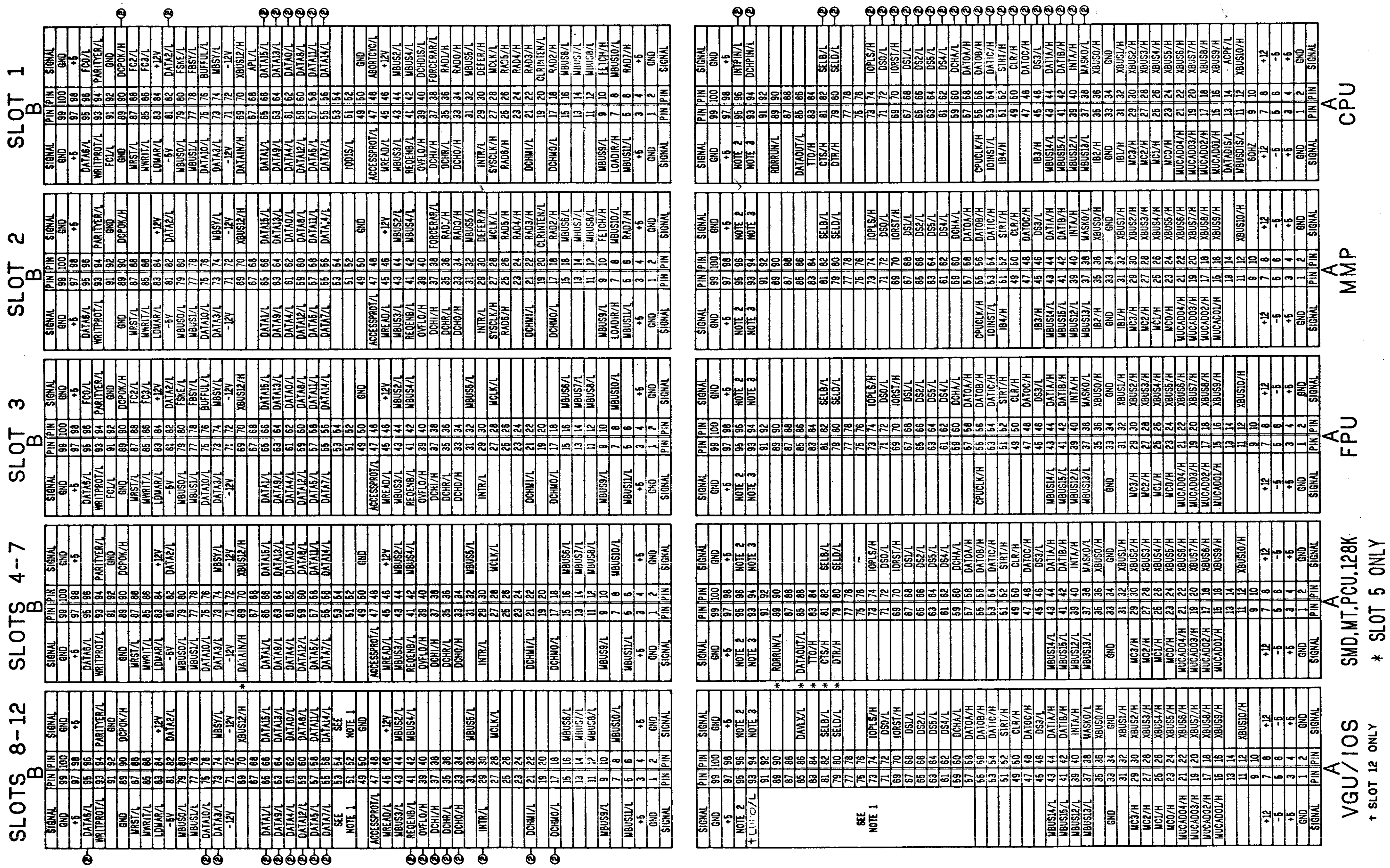
12 Slot Backplane



NOTE 1:

SLOTS 8, 9, 10, 11, AND 12 HAVE PROVISIONS FOR EITHER VGU OR IOS INTERFACES. BOTH USE THE CORRESPONDING 26 PIN CONNECTORS J27, J30, J33, J36, AND J39. CONNECTORS J28, J29, J31, J32, J34, J35, J37, J38, J40, AND J41 ARE USED WITH VGU INTERFACES ONLY.

NOTE 2:

INTERUPT PRIORITY PASSING CONNECTIONS

FROM A95 OF SLOT:	TO A96 OF SLOT:
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
10	11
11	12

NOTE 3:

DATA CHANNEL PRIORITY PASSING CONNECTIONS

FROM A93 OF SLOT:	TO A94 OF SLOT:
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	9
9	10
10	11
11	12

J28, J31, J34, J37, J40
(VGU ONLY)

1	OUTVID(-)	B53
2	OUTVID(+)	B51

CONN	SLOT
J28	8
J31	9
J34	10
J37	11
J40	12

J29, J32, J35, J38, J41
(VGU ONLY)

1	INVID(-)	B54
2	INVID(+)	B52

CONN	SLOT
J29	8
J32	9
J35	10
J38	11
J41	12

HIGH POWER CONNECTOR

J25

GND	(+5VOLTS RETURN)	2	1	(+5VOLTS OUTPUT) +5

LOW POWER CONNECTOR

J26

	2	1	(+5V OUT SEN) +5V
	4	3	(+5V RET SEN) GND
+12V (+12V OUTPUT)	6	5	(+12V OUT SEN) +12V
GND (+12V RETURN)	8	7	(+12V RET SEN) GND
GND (-12V RETURN)	10	9	(-12V RET SEN) GND
-12V (-12V OUTPUT)	12	11	(-12V OUT SEN) -12V
GND (-5V RETURN)	14	13	ACPF/L
-5V (-5V OUTPUT)	16	15	DCPOK/H

TTY CONNECTORS

J42, J45

SLOTS 1 AND 5	SIGNAL NAME	PIN	PIN	SIGNAL NAME	SLOTS 1 AND 5
	GND	9	5		NC
NC		8	4	-5V	
A83	TTO/H	7	3	DATAIN/H	B69
A85	DATAOUT/L	6	2	RDRRUN/L	A89
			1	DTR/H	A79

CONN	SLOT
J42	1
J45	5

DS21E1026

C

VGU/IOS CONNECTORS

J27, J30, J33, J36, 39

SLOTS 8-12	IOS SIGNAL	VGU SIGNAL	PIN	PIN	VGU SIGNAL	IOS SIGNAL	SLOTS 8-12
			1	14	TURNO2/H	IODTA1/L	A61
A63	IODTA1/H	TURNO4/H	2	15			
A65	IOBSY/L	TURNO1/H	3	16	TURNO3/H	IOBSY/H	A67
			4	17		YSIGN1/L	A69
A71	YSIGN1/H	TURN13/H	5	18	TURN11/H		A57
A73	YSTEP1/L		6	19	TURN14/H	YSTEP1/H	A75
A59		TURN12/H	7	20	RCVDAT/H	XSIGN1/L	A77
A79	XSIGN1/H	RCVDAT/L	8	21			
A81	XSTEP1/L	URBSY/H	9	22	URBSY/L	XSTEP1/H	A83
			10	23	GND	GND	
A85	TBLBSY/L	IAMBUSY/L	11	24	IAMBUSY/H	TBLBSY/H	A87
	GND	GND	12	25	TRDATA/L	TBLDATA/L	A89
A91	TBLDTA/H	TRDATA/H	13	26	GND	GND	

CONN	SLOT
J27	8
J30	9
J33	10
J36	11
J39	12

MATERIAL	PART NUMBER	NEXT ASSEMBLY	QTY
— // —		DA21E1024	1
FINISH — // —			

TOLERANCES
DECIMAL
.XX =±.01
.XXX =±.005
.XXXX =±.0010
FRACTIONAL=±1/64
ANGULAR=±.100

	SIGNATURE	DATE
DRN	P. MAGEE	8-10
CHK	C. Standish	9/74
ENGR	N TIDD	8-10
PROJ	R.T.M.	9/74
MFG	R. Gr...	9/74

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
C	ECO 3303	RB		12/77
B	ECO 3270	RB		11/77
A	REL ECO 3163	RB		8/7?

TITLE 12 SLOT BACKPLANE SCHEMATIC DIAGRAM

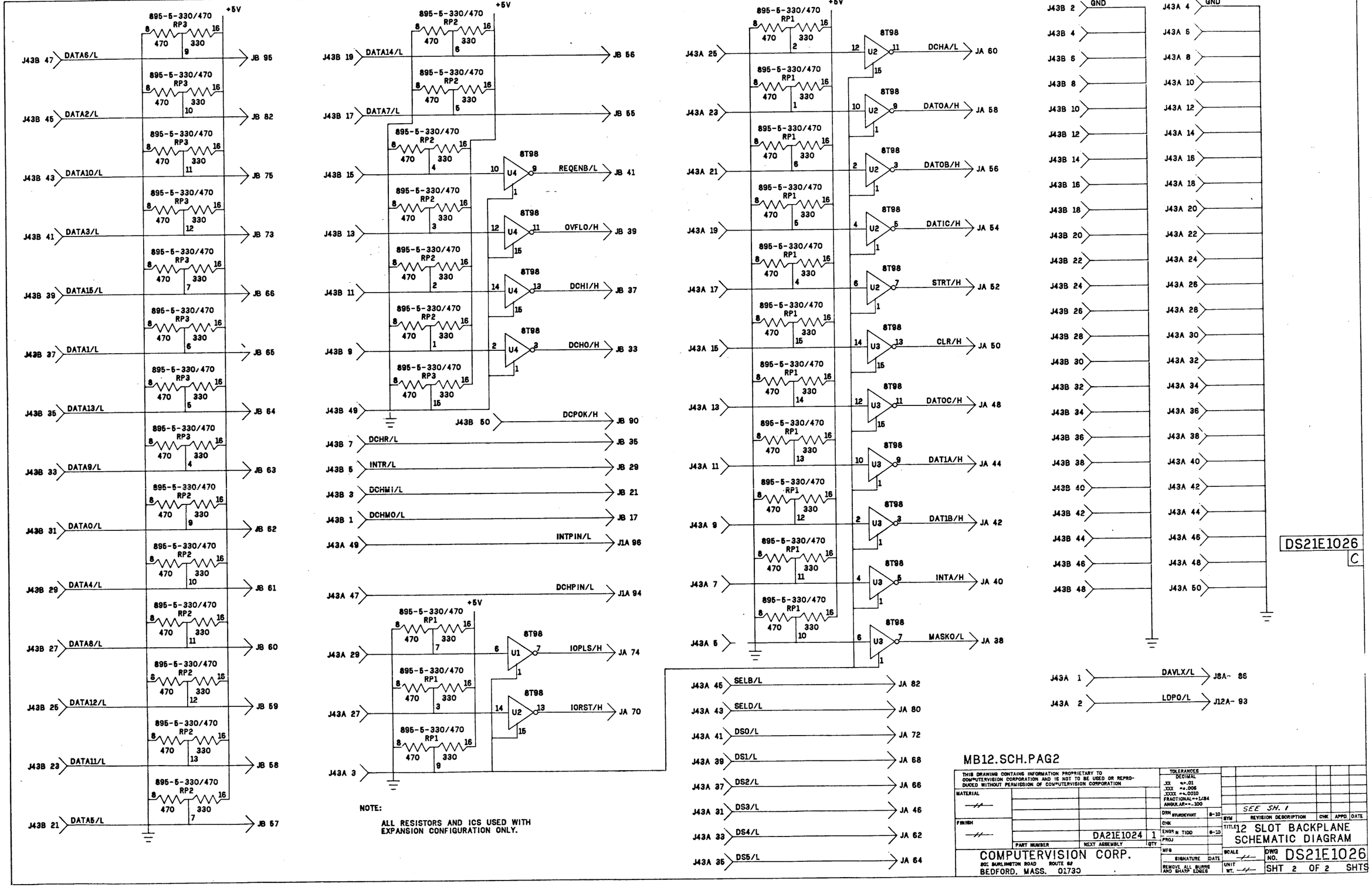
SCALE — // —

UNIT WT. — // —

DWG NO. DS21E1026

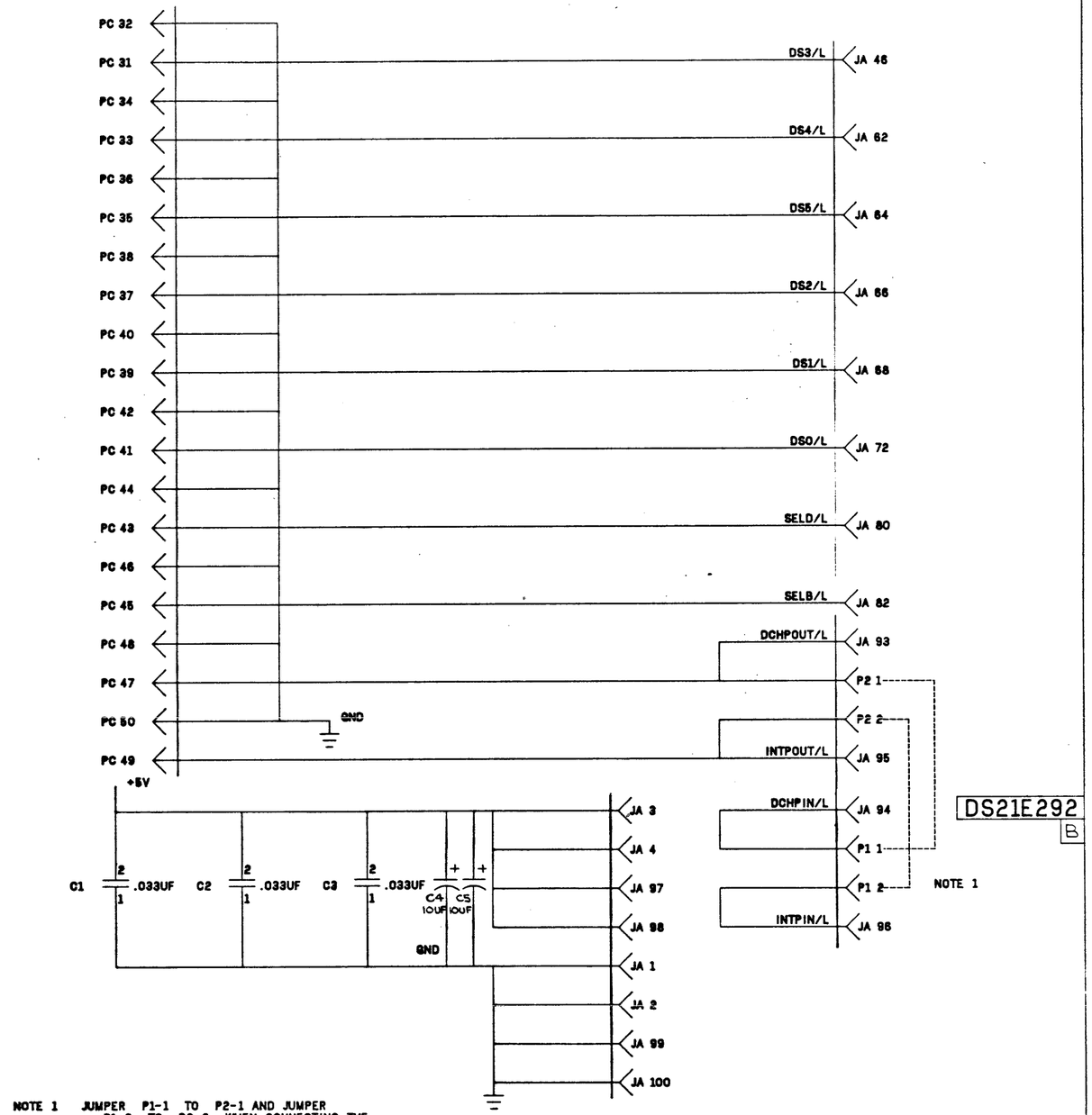
SHT 1 OF 2 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730


+5V
895-5-330/470
RP3
RP2
RP1
470
330
J43B 47 DATA6/L JB 95
J43B 45 DATA2/L JB 82
J43B 43 DATA10/L JB 75
J43B 41 DATA3/L JB 73
J43B 39 DATA15/L JB 66
J43B 37 DATA1/L JB 65
J43B 35 DATA13/L JB 64
J43B 33 DATA9/L JB 63
J43B 31 DATA0/L JB 62
J43B 29 DATA4/L JB 61
J43B 27 DATA8/L JB 60
J43B 25 DATA12/L JB 59
J43B 23 DATA11/L JB 58
J43B 21 DATA5/L JB 57
J43B 19 DATA14/L JB 56
J43B 17 DATA7/L JB 55
J43B 15 REQENB/L JB 41
J43B 13 OVFLO/H JB 39
J43B 11 DCH1/H JB 37
J43B 9 DCHO/H JB 33
J43B 49
J43B 50 DCPOK/H JB 90
J43B 7 DCHR/L JB 35
J43B 5 INTR/L JB 29
J43B 3 DCHWI/L JB 21
J43B 1 DCHWO/L JB 17
J43A 49 INTPIN/L J1A 96
J43A 47 DCHPIN/L J1A 94
8T98
U4
U1
U2
U3
J43A 29 IOPLS/H JA 74
J43A 27 IORST/H JA 70
J43A 3
NOTE:
ALL RESISTORS AND ICS USED WITH EXPANSION CONFIGURATION ONLY.
J43A 25 DCHA/L JA 60
J43A 23 DATOA/H JA 58
J43A 21 DATOB/H JA 56
J43A 19 DATIC/H JA 54
J43A 17 STRT/H JA 52
J43A 15 CLR/H JA 50
J43A 13 DATOC/H JA 48
J43A 11 DAT1A/H JA 44
J43A 9 DAT1B/H JA 42
J43A 7 INTA/H JA 40
J43A 5 MASKO/L JA 38
J43A 45 SELB/L JA 82
J43A 43 SELD/L JA 80
J43A 41 DSO/L JA 72
J43A 39 DS1/L JA 68
J43A 37 DS2/L JA 66
J43A 31 DS3/L JA 46
J43A 33 DS4/L JA 62
J43A 35 DS5/L JA 64
J43B 2 GND
J43A 4 GND
J43A 1 DAVLX/L J8A- 86
J43A 2 LDPO/L J12A- 93
DS21E1026
C
MB12.SCH.PAG2
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION
MATERIAL
FINISH
DA21E1024 1
PART NUMBER NEXT ASSEMBLY QTY
COMPUTERVISION CORP.
900 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
TOLERANCES
DECIMAL
.XX +-.01
.XXX +-.005
.XXXX +-.0010
FRACTIONAL +-1/64
ANGULAR +-.100
DRN STURDEVANT 8-10
CHK
ENGR N TIDD 6-20
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES
SEE SH. 1
SYM REVISION DESCRIPTION CHK APPD DATE
TITLE 12 SLOT BACKPLANE SCHEMATIC DIAGRAM
SCALE
DWG NO. DS21E1026
UNIT
WT.
SHT 2 OF 2 SHTS

Paddleboards

A Schematic
B Schematic



DS21E292

B

NOTE 1 JUMPER P1-1 TO P2-1 AND JUMPER P1-2 TO P2-2 WHEN CONNECTING THE I/O BUS DRIVER-A BD TO AN UNUSED SLOT.

TOLERANCES DECIMAL .XX +-.01 .XXX +-.005 .XXXX +-.0010 FRACTIONAL +-1/64 ANGULAR +-.100

MATERIAL —

FINISH —

DRN STURDEVANT 8-78

CHK RB 10/78

ENGR — —

PROJ n/a —

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
B	ECO# 3384			4/82
A	REL. ECO #3233			

PART NUMBER DT21E191 NEXT ASSEMBLY 1 QTY

TITLE I/O BUS DRIVER-A SCHEMATIC

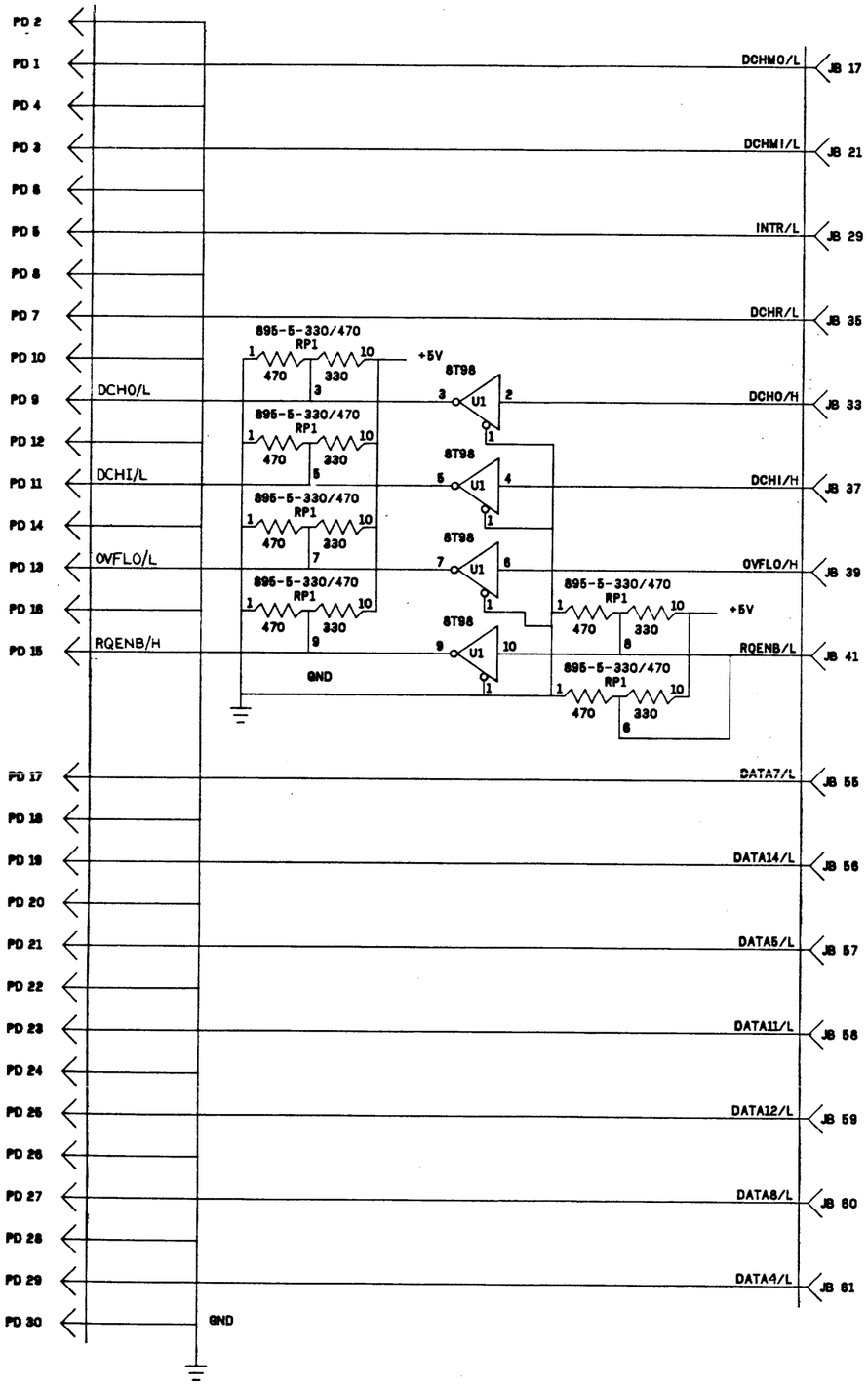
SCALE —

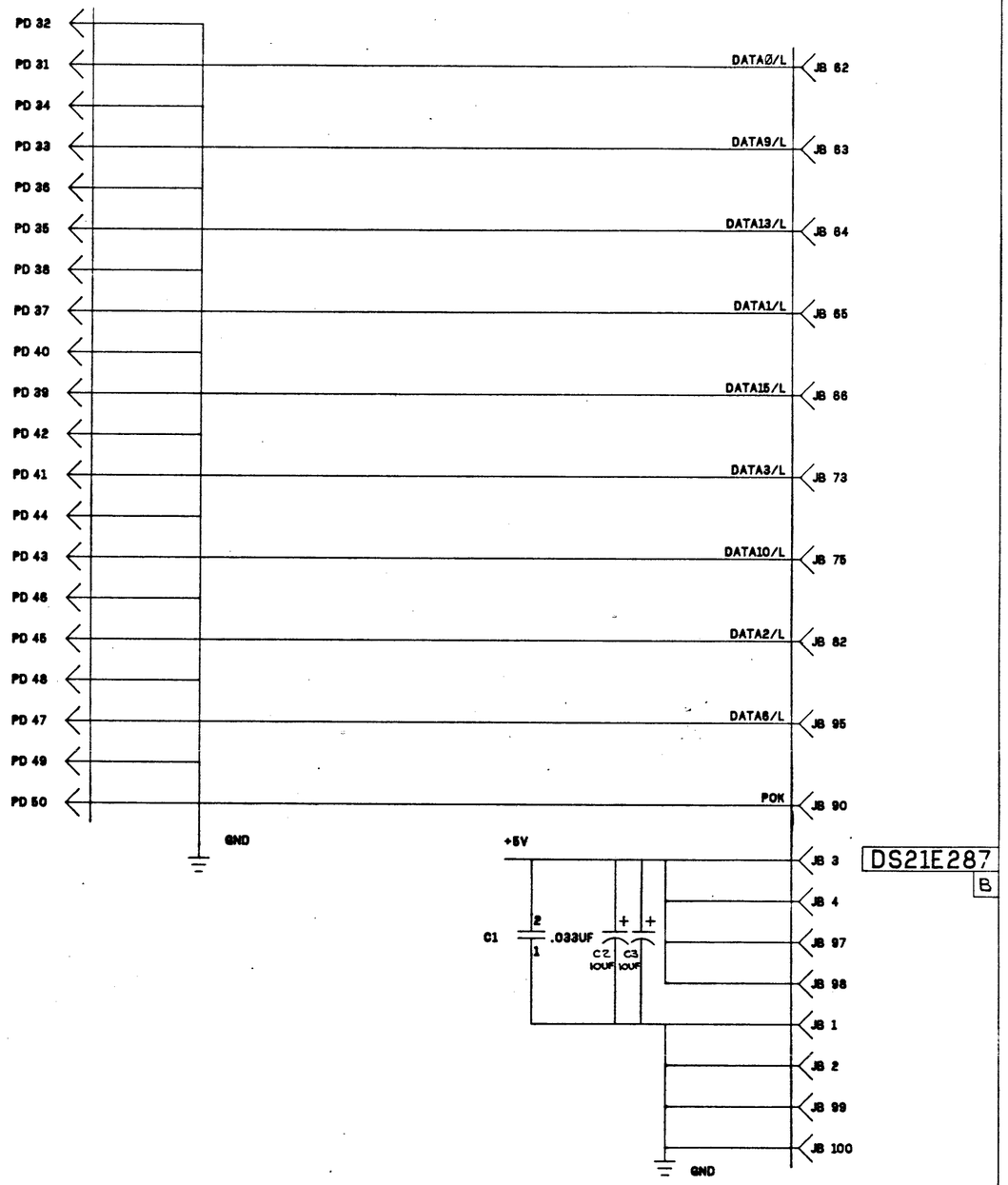
DWG NO. DS21E292

UNIT WT. —

SHT 1 OF 1 SHTS

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730





DS21E287

B

TOLERANCES
DECIMAL
XX +-.01
XXX +-.005
XXXX +-.0030
FRACTIONAL +-1/64
ANGULAR +-.100

MATERIAL —

FINISH —

DRN STURDEVANT 8-78
CHK [illegible] 10/78
ENGR [illegible] 11/78
PROJ [illegible] 10/78
MFR
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
B	ECO# 3384	LP	MAT	9/80
A	REL. ECO #3233	KS	JPM	11/79

PART NUMBER DT21E196 NEXT ASSEMBLY QTY 1

TITLE I/O BUS DRIVER-B SCHEMATIC

SCALE —

DWG NO. DS21E287

UNIT WT. —

SHT 1 OF 1 SHTS

COMPUTERVISION CORP.
896 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

128/32K A/B-Port Memory Unit

DA21E250-X CONFIGURATION TABLE

	SINGLE PORT	DUAL PORT. DISTRIBUTED MODE	DUAL PORT. GPU MODE	SINGLE PORT 32K
POPULATED WITH 4K RAMS (MK 4027-3)	USE CONFIGURATION BLOCKS A.A1.B	USE CONFIGURATION BLOCKS A.A1.C.D.E	USE CONFIGURATION BLOCKS A.C.D.E	
POPULATED WITH 16K RAMS (MK 4116-3)	DA21E250-02 USE CONFIGURATION BLOCKS B.F	DA21E250-01 USE CONFIGURATION BLOCKS D.E.F.G	DA21E250-01 USE CONFIGURATION BLOCKS E.F.H	DA21E250-03 USE CONFIGURATION BLOCKS A1.I

CONFIGURATION BLOCK A) 32K HARDWARE CONFIGURATION (USING 4K RAMS)

1) REMOVE R22
2) ADJUST POT R31 SUCH THAT TP HAS A 29 µS REP RATE
3) INSERT JUMPERS: JP9-2 . JP11-2 . JP13-2
4) POPULATE MEMORY ARRAY WITH MK4027-3 MEMORY CHIPS

CONFIGURATION BLOCK A1) APORT 32K ADDRESSING CHART

*APORT FIELD	AMC0	AMC1	AMC2	AMC3	**CLOSED CONTACTS ON SWITCH PACK 1V
0	H	H	H	H	8
1	H	H	H	L	7.8
2	H	H	L	H	6.8
3	H	H	L	L	6.7.8
4	H	L	H	H	5.8
5	H	L	H	L	5.7.8
6	H	L	L	H	5.6.8
7	H	L	L	L	5.6.7.8
8	L	H	H	H	4.8
9	L	H	H	L	4.7.8
10	L	H	L	H	4.6.8
11	L	H	L	L	4.6.7.8
12	L	L	H	H	4.5.8
13	L	L	H	L	4.5.7.8
14	L	L	L	H	4.5.6.8
15	L	L	L	L	4.5.6.7.8

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK 1V OPEN

CONFIGURATION BLOCK B) SINGLEPORT CONFIGURATION

1) DEPOPULATE PC BOARD AS PER BM21E250-02
2) ADD JUMPERS JP3 . JP5 . JP7

CONFIGURATION BLOCK C) BPORT 32K MEMORY ROW SELECT

1) INSERT JUMPERS: JP10-2 . JP12-2 . JP14-2

CONFIGURATION BLOCK D) BPORT 32K ADDRESSING AND I/O DEVICE CODE CHART

*BPORT FIELD OR I/O DEVICE CODE	$\overline{BMC0}$ OR $\overline{BDS0}$	$\overline{BMC1}$ OR $\overline{BDS1}$	$\overline{BMC2}$ OR $\overline{BDS2}$	$\overline{BMC3}$ OR $\overline{BDS3}$	**CLOSED CONTACTS ON SWITCH PACK 12S
0	H	H	H	H	6
1	H	H	H	L	4.6
2	H	H	L	H	3.6
3	H	H	L	L	3.4.6
4	H	L	H	H	2.6
5	H	L	H	L	2.4.6
6	H	L	L	H	2.3.6
7	H	L	L	L	2.3.4.6
8	L	H	H	H	1.6
9	L	H	H	L	1.4.6
10	L	H	L	H	1.3.6
11	L	H	L	L	1.3.4.6
12	L	L	H	H	1.2.6
13	L	L	H	L	1.2.4.6
14	L	L	L	H	1.2.3.6
15	L	L	L	L	1.2.3.4.6

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
** ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN

CONFIGURATION BLOCK E) LAST BOARD IN DAISY CHAIN

THE LAST DUAL PORT MEMORY BOARD IN A DAISY CHAIN MUST TERMINATE BPORT BUS SIGNALS. THE LAST DUAL PORT MEMORY IN A DAISY CHAIN ONLY MUST HAVE THE FOLLOWING RESISTORS: RP6.RP7.RP8. RP12 . RES PACK 12F

CONFIGURATION BLOCK F) 128K HARDWARE CONFIGURATION/APORT 128K ADDRESSING M

1) R20 AND R22 INSERTED
2) INSERT JIMPER JP4
3) ADJUST POT R31 SUCH THAT TP HAS A 14.5 µS REP RATE
4) INSERT JUMPERS JP9 . JP11 . JP13
5) POPULATE MEMORY ARRAY WITH MK4116-3 MEMORY CHIPS
6) APORT 128K ADDRESSING CHART

*APORT FIELD NO.	$\overline{AMC0}$	$\overline{AMC1}$	$\overline{AMC2}$	$\overline{AMC3}$	$\overline{AMC3}$	**CLOSED CONTACTS ON SWITCH PACK 1V
0.1.2.3	H	H	H	H	H	
4.5.6.7	H	H	H	H	L	5
8.9.10.11	H	H	H	L	H	4
12.13.14.15	H	H	H	L	L	4.5
16.17.18.19	H	H	L	H	H	3
20.21.22.23	H	H	L	H	L	3.5
24.25.26.27	H	H	L	L	H	3.4
28.29.30.31	H	H	L	L	L	3.4.5
32.33.34.35	H	L	H	H	H	2
36.37.38.39	H	L	H	H	L	2.5
40.41.42.43	H	L	H	L	H	2.4
44.45.46.47	H	L	H	L	L	2.4.5
48.49.50.51	H	L	L	H	H	2.3
52.53.54.55	H	L	L	H	L	2.3.5
56.57.58.59	H	L	L	L	H	2.3.4
60.61.62.63	H	L	L	L	L	2.3.4.5
64.65.66.67	L	H	H	H	H	1
68.69.70.71	L	H	H	H	L	1.5
72.73.74.75	L	H	H	L	H	1.4
76.77.78.79	L	H	H	L	L	1.4.5
80.81.82.83	L	H	L	H	H	1.3
84.85.86.87	L	H	L	H	L	1.3.5
88.89.90.91	L	H	L	L	H	1.3.4
92.93.94.95	L	H	L	L	L	1.3.4.5
96.97.98.99	L	L	H	H	H	1.2
100.101.102.103	L	L	H	H	L	1.2.5
104.105.106.107	L	L	H	L	H	1.2.4
108.109.110.111	L	L	H	L	L	1.2.4.5
112.113.114.115	L	L	L	H	H	1.2.3
116.117.118.119	L	L	L	H	L	1.2.3.5
120.121.122.123	L	L	L	L	H	1.2.3.4
124.125.126.127	L	L	L	L	L	1.2.3.4.5

* EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY (TO EXPAND BEYOND 15 FIELDS . IC 2X AND 2V . SHT.7 . MUST BE ADDED)
** ALL OTHER SWITCH CONTACTS ON SWITCH 1V ARE OPEN

CONFIGURATION BLOCK G) 128K APORT/32K BPORT COMMON MEMORY

WITH JUMPERS JP10. JP12. JP14. INSERTED

BMC2	BMC3	COMMON SEGMENT OF APORT 128K MEMORY
H	H	1ST 32K
H	L	2ND 32K
L	H	3RD 32K
L	L	4TH 32K

2) TO FORCE COMMON APORT/BPORT MEMORY INDEPENDENT OF BMC2 AND BMC3

BMC2	BMC3	COMMON SEGMENT OF APORT 128K MEMORY	JUMPERS INSERTED
X	X	1ST 32K	JP10. JP15. JP16
X	X	2ND 32K	JP10. JP16
X	X	3RD 32K	JP10. JP15
X	X	4TH 32K	JP10

WHERE X = DONT CARE

CONFIGURATION BLOCK H) BPORT 128K ADDRESSING CONFIGURATION

1) INSERT JUMPERS JP10. JP12. JP14
2) BPORT 128K ADDRESSING CHART

BPORT FIELD NO.	BMAD0	BMAD1	BMAD2	BMC0	BMC1	**CLOSED CONTACTS ON SWITCH PACKS 9C	12S
0.1.2.3	H	H	H	H	H		8
4.5.6.7	H	H	H	H	L		2.8
8.9.10.11	H	H	H	L	H		1.8
12.13.14.15	H	H	H	L	L		1.2.8
16.17.18.19	H	H	L	H	H	7	8
20.21.22.23	H	H	L	H	L	7	2.8
24.25.26.27	H	H	L	L	H	7	1.8
28.29.30.31	H	H	L	L	L	7	1.2.8
32.33.34.35	H	L	H	H	H	6	8
36.37.38.39	H	L	H	H	L	6	2.8
40.41.42.43	H	L	H	L	H	6	1.8
44.45.46.47	H	L	H	L	L	6	1.2.8
48.49.50.51	H	L	L	H	H	6.7	8
52.53.54.55	H	L	L	H	L	6.7	2.8
56.57.58.59	H	L	L	L	H	6.7	1.8
60.61.62.63	H	L	L	L	L	6.7	1.2.8
64.65.66.67	L	H	H	H	H	5	8
68.69.70.71	L	H	H	H	L	5	2.8
72.73.74.75	L	H	H	L	H	5	1.8
76.77.78.79	L	H	H	L	L	5	1.2.8
80.81.82.83	L	H	L	H	H	5.7	8
84.85.86.87	L	H	L	H	L	5.7	2.8
88.89.90.91	L	H	L	L	H	5.7	1.8
92.93.94.95	L	H	L	L	L	5.7	1.2.8
96.97.98.99	L	L	H	H	H	5.6	8
100.101.102.103	L	L	H	H	L	5.6	2.8
104.105.106.107	L	L	H	L	H	5.6	1.8
108.109.110.111	L	L	H	L	L	5.6	1.2.8
112.113.114.115	L	L	L	H	H	5.6.7	8
116.117.118.119	L	L	L	H	L	5.6.7	2.8
120.121.122.123	L	L	L	L	H	5.6.7	1.8
124.125.126.127	L	L	L	L	L	5.6.7	1.2.8

EACH FIELD NO. REPRESENTS ONE 32K SEGMENT OF MEMORY
ALL OTHER CONTACTS ON SWITCH PACK 12S AND 9C OPEN
(9C-2 MAY BE CLOSED TO DISABLE APORT)

CONFIGURATION BLOCK I) 32K SINGLE PORT CONFIGURATION (USING 16K RAMS)

1) DEPOPULATE BOARDS AS PER ASSEMBLY DA21E250-03

DS21E252
E

MISCELLANEOUS JUMPERS

1) FOR LDMAR STARTING APORT MEMORY CYCLE INSERT JP-2
2) FOR MEMREAD STARTING APORT MEMORY CYCLE INSERT JP-1
3) FOR GPU MODE REQUIRING DISABLED APORT . CLOSE SWITCH 9C-2
4) APORT MUC/NON MUC OPERATION

JUMPER PLUG 4D	
MUC OPERATION	1-16 2-15 3-14 4-13
NON MUC OPERATION	5-12 6-11 7-10 8-9

5) APORT I/O DEVICE CODE

1) STANDARD 24_8. INSERT JP8 FOR 25_8

MATERIAL —
FINISH —

PART NUMBER	NEXT ASSEMBLY	QTY
	DA21E250	1

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.100

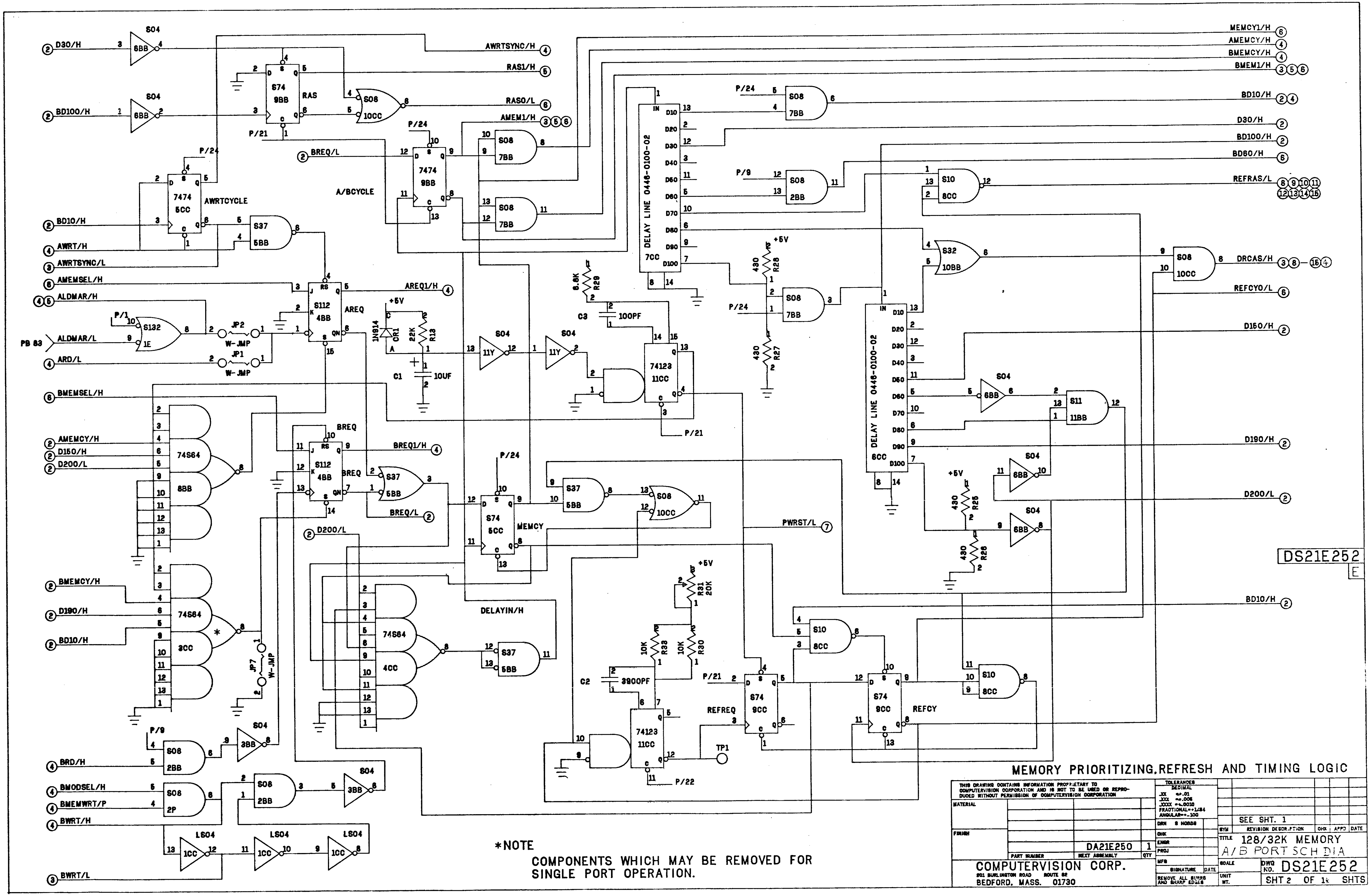
DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SYM	REVISION DESCRIPTION	CHK	APPD	DATE
E	ECO 3423			
D	ECO 33 3			

TITLE 128/32K MEMORY A/B PORT SCH. DIAGRAM

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 1 OF 16 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730



MEMORY PRIORITIZING,REFRESH AND TIMING LOGIC
*NOTE
COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.
DS21E252
E
D30/H
BD100/H
BD10/H
AWRT/H
AWRTSYNC/L
AMEMSEL/H
ALDMAR/H
ALDMAR/L
PB 83
ARD/L
BMEMSEL/H
AMEMCY/H
D150/H
D200/L
BMEMCY/H
D190/H
BRD/H
BMODSEL/H
BMEMWRT/P
BWRT/H
BWRT/L
BREQ/L
AWRTSYNC/H
RAS1/H
RAS0/L
AMEM1/H
MEMCY1/H
BMEMCY/H
BMEM1/H
BD80/H
REFRAS/L
DRCAS/H
REFCY0/L
PWRST/L
AREQ1/H
BREQ1/H
DELAYIN/H
AWRTCYCLE
A/BCYCLE
AREQ
BREQ
MEMCY
REFREQ
REFCY
DELAY LINE 0446-0100-02
TP1
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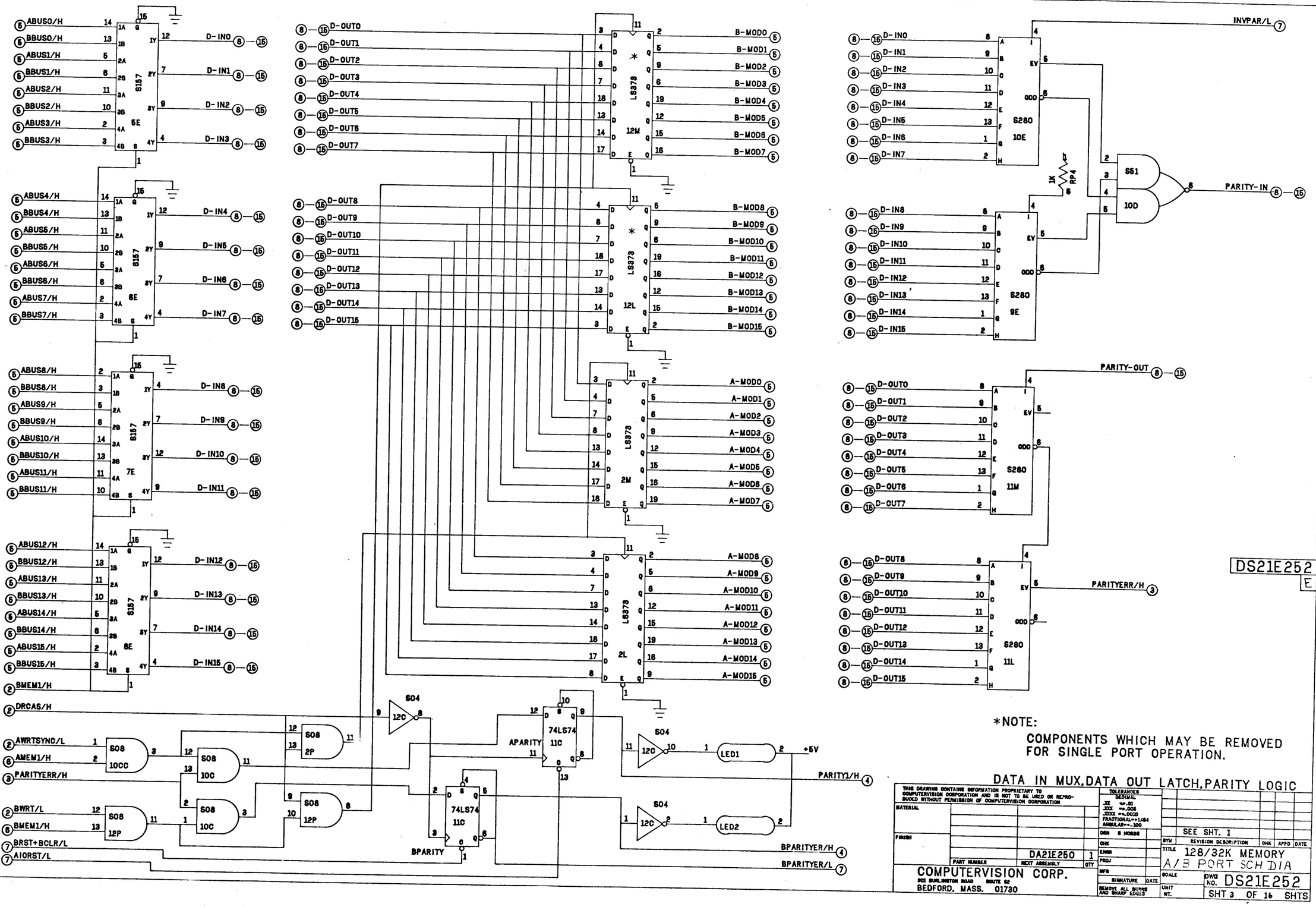
DA21E250
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
SEE SHT. 1
TITLE 128/32K MEMORY
A/B PORT SCH DIA
DWG NO. DS21E252
SHT 2 OF 14 SHTS



DS21E252 E

*NOTE:
COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

DATA IN MUX.DATA OUT LATCH.PARITY LOGIC

MATERIAL
FINISH
PART NUMBER DA21E250 1
NEXT ASSEMBLY QTY

COMPUTERVISION CORP.
901 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL
.XX +-.01
.XXX +-.005
.XXXX +-.0010
FRACTIONAL +-1/64
ANGULAR +-.100

DRN G HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

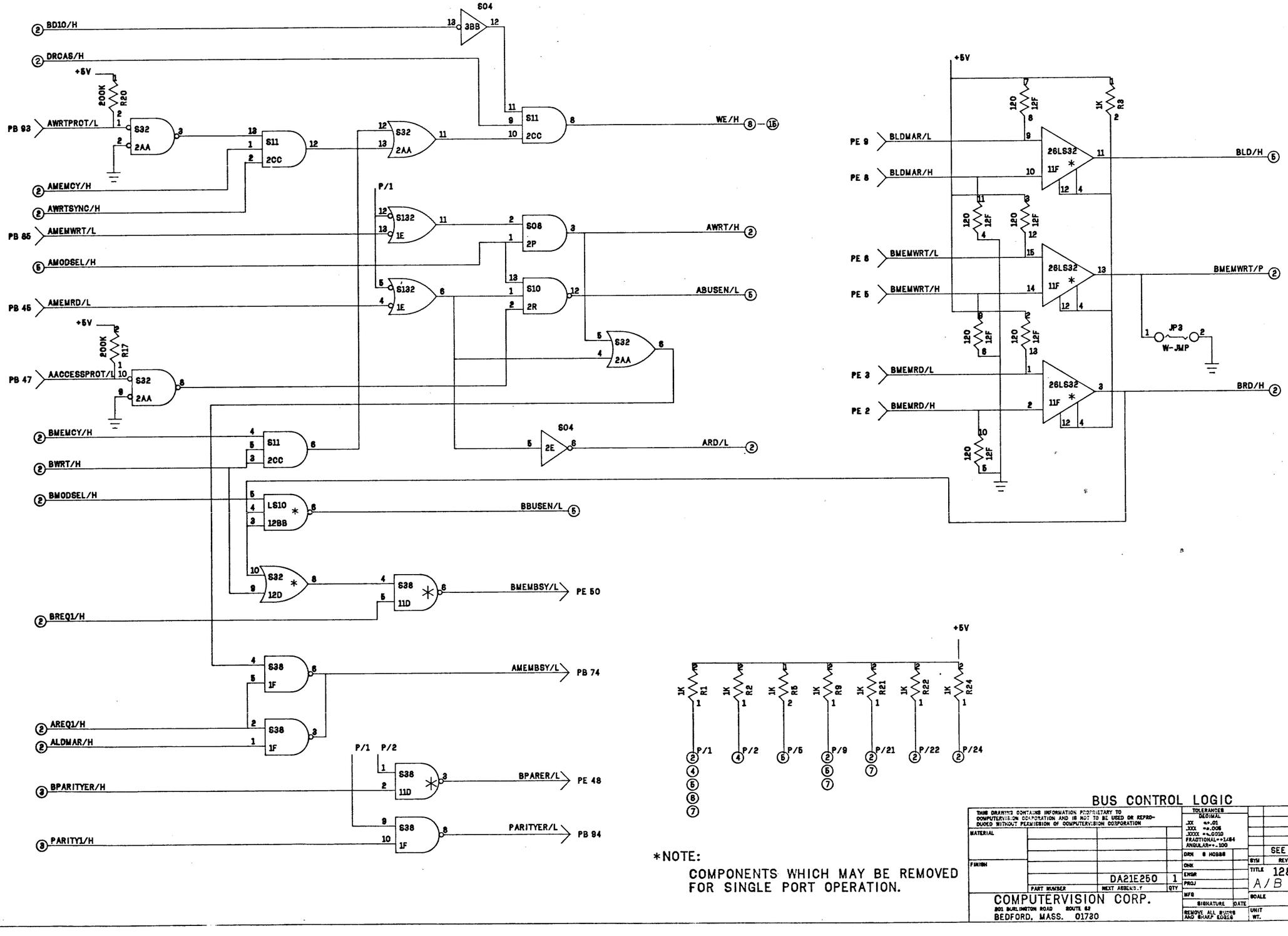
SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY A/B PORT SCH DIA

SCALE DWG NO. DS21E252

UNIT WT. SHT 3 OF 16 SHTS



DS21E252
E

*NOTE:
COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

BUS CONTROL LOGIC

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±.100

MATERIAL

FINISH

DRN B HOBBS

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

PART NUMBER DA21E250 NEXT ASSEMB. 1 QTY

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
801 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

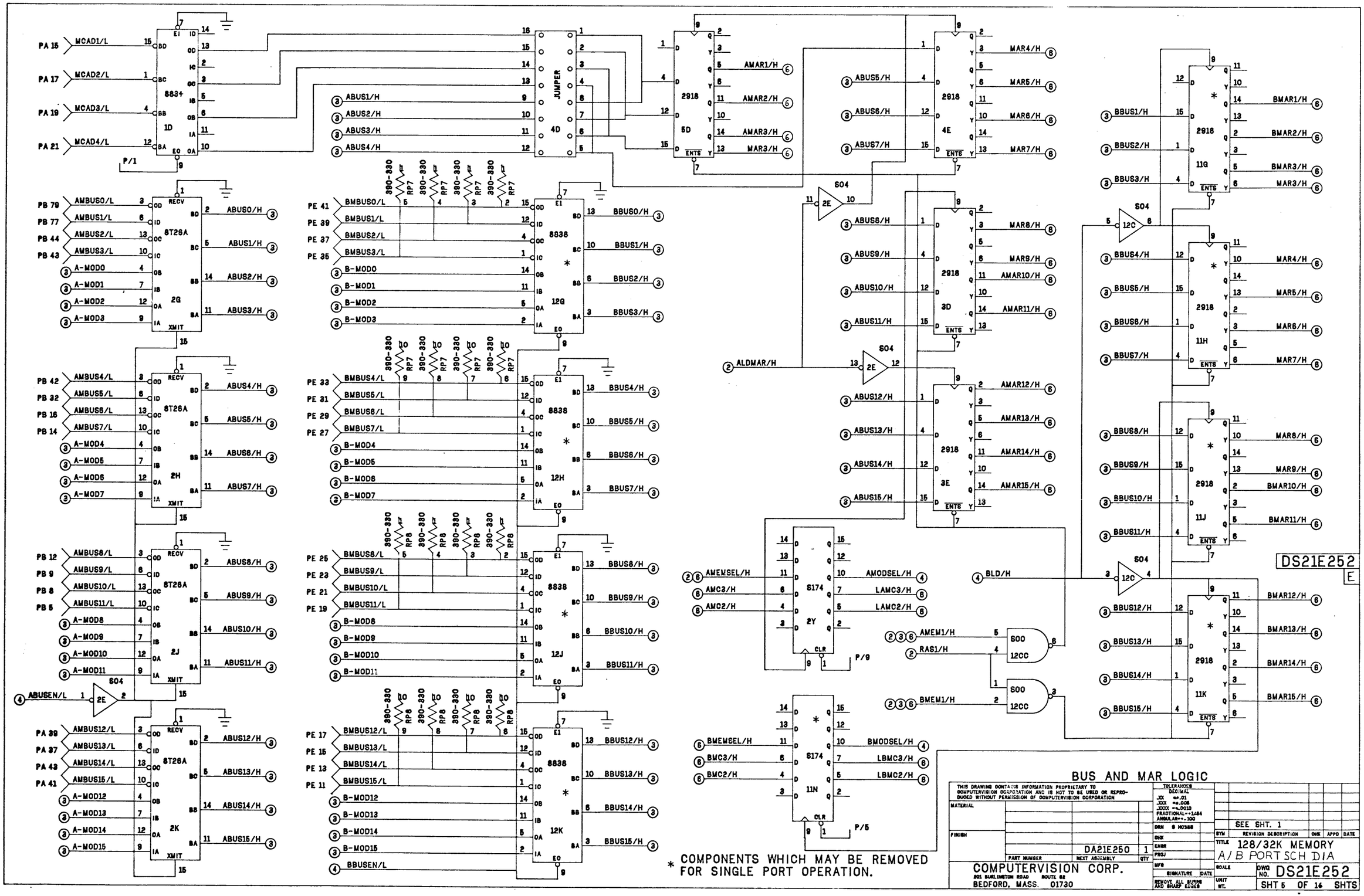
TITLE 128/32K MEMORY A/B PORT SCH DIA

SCALE

DWG NO. DS21E252

UNIT WT.

SHT 4 OF 16 SHTS



DS21E252 E

* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

BUS AND MAR LOGIC

TOLERANCES DECIMAL .XX ±.01 .XXX ±.005 .XXXX ±.0010 FRACTIONAL ±1/64 ANGULAR ±1°

MATERIAL

FINISH

DRN S MOSES

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

PART NUMBER DA21E250 NEXT ASSEMBLY QTY 1

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY A/B PORT SCH DIA

SCALE

DWG NO. DS21E252

UNIT WT.

SHT 5 OF 16 SHTS

COMPUTERVISION CORP.
801 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

STANDARD JUMPERS (FOR OTHER CONFIGS. SEE SHT. 1)

128K MEM . GPU JP9, JP10, JP11, JP12, JP13, JP14

128K MEM . DIST MODE - JP9, JP10, JP11, JP13, JP15, JP18

ADDR MUX CONTROL		
A	B	RAM ADDR
L	L	CAS ADDR
H	L	APORT RAS ADDR
L	H	BPORT RAS ADDR
H	H	REFRESH ADDR

2X AND 2Y TO BE ADDED FOR FUTURE EXPANSION

APORT/BPORT SELECT, ADDR MUX, REFRESH CNTR, RAS CLOCK

* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.

DS21E252

E

SEE SHT. 1

REVISION DESCRIPTION	CHK	APPD	DATE

TITLE: 128/32K MEMORY A/B PORT SCH DIA

SCALE:

DWG NO. DS21E252

SHT 6 OF 16 SHTS

DRN: B HOBBS

CHK:

ENGR:

PROJ:

MFG:

DA21E250 1

PART NUMBER / NEXT ASSEMBLY / QTY

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES DECIMAL: XX ±.01, XXX ±.005, XXXX ±.0050; FRACTIONAL ±1/64; ANGULAR ±.100

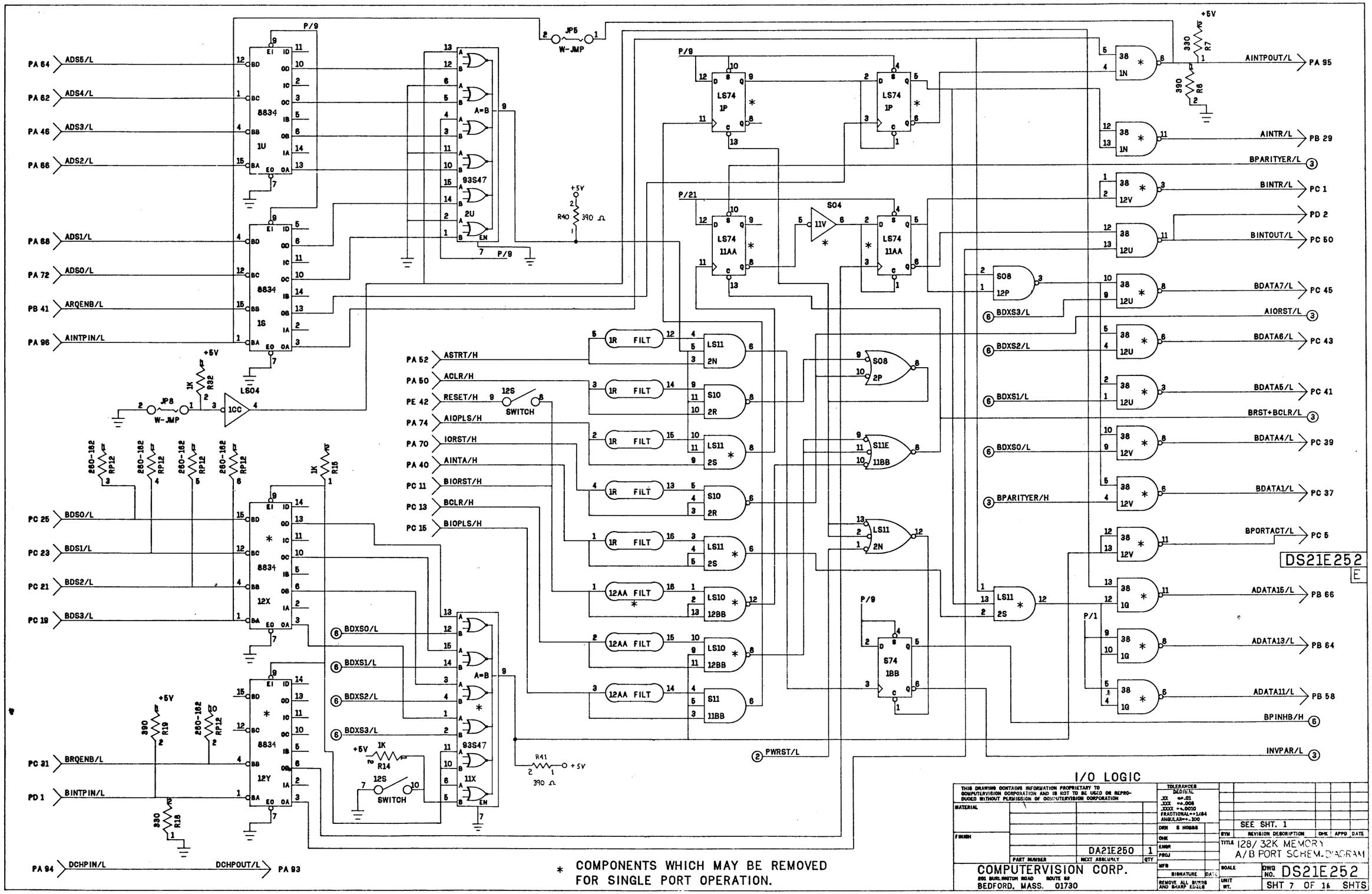
MATERIAL

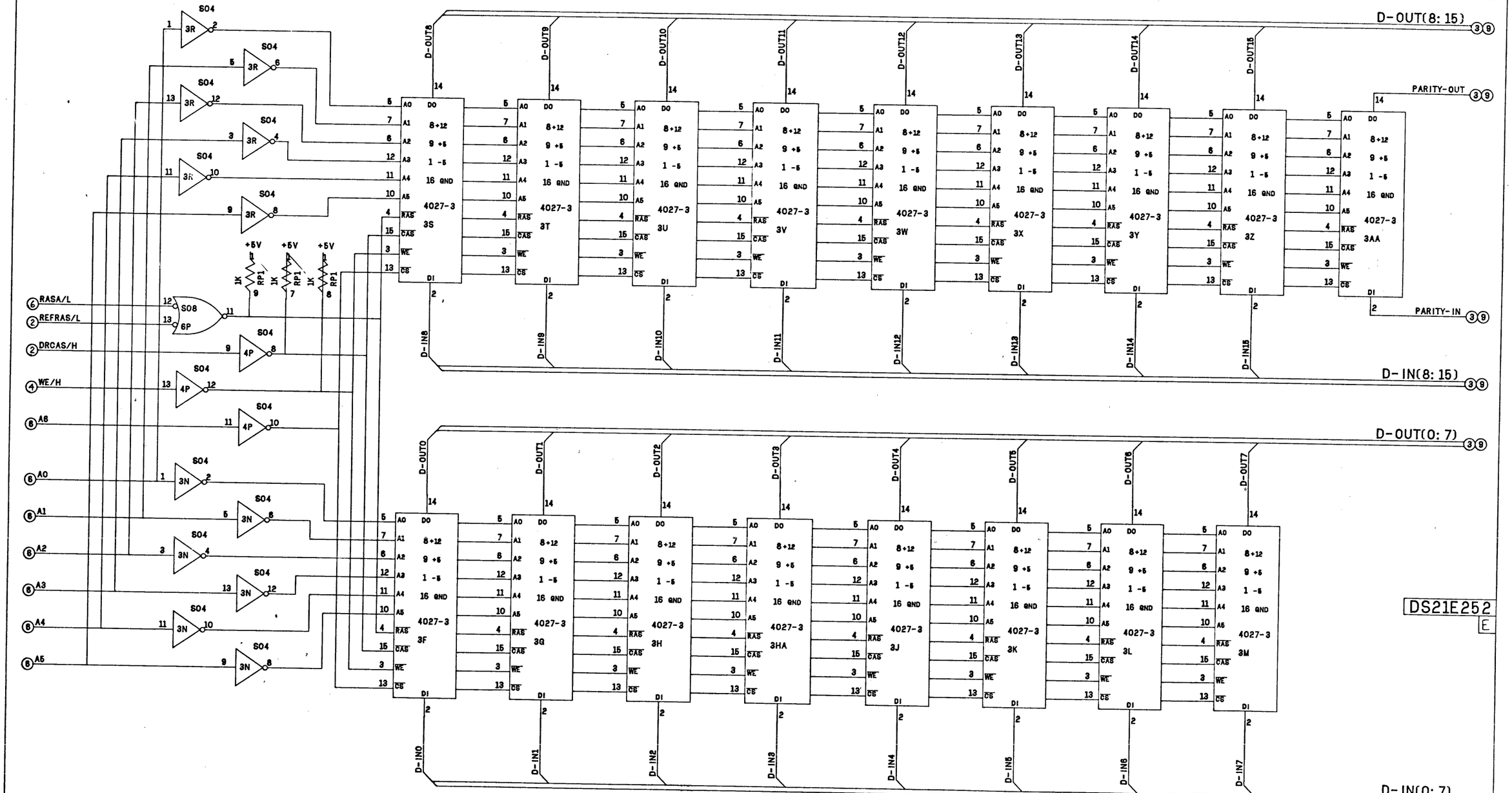
FINISH

REMOVE ALL BURRS AND SHARP EDGES

SIGNATURE / DATE

UNIT WT.


PA 64 ADS5/L
PA 62 ADS4/L
PA 46 ADS3/L
PA 66 ADS2/L
PA 68 ADS1/L
PA 72 ADS0/L
PB 41 ARQENB/L
PA 96 AINTPIN/L
8834
1U
1S
LS04
JP8
W-JMP
2K R32
1CC
P/9
JP5
W-JMP
93S47
A=B
2U
+5V
R40 390 Ω
PA 52 ASTRT/H
PA 50 ACLR/H
PE 42 RESET/H
PA 74 AIOPLS/H
PA 70 IORST/H
PA 40 AINTA/H
PC 11 BIORST/H
PC 13 BCLR/H
PC 15 BIOPLS/H
1R FILT
LS11 2N
LS11 2S
S10 2R
12AA FILT
LS10 12BB
S11 11BB
12S SWITCH
11X
P/21
LS74 1P
LS74 11AA
S04 11V
S08 2P
S11E 11BB
S08 12P
LS11 2S
S74 1BB
38 1N
38 12V
38 12U
38 1Q
+5V R7 390
R6 390
AINTPOUT/L PA 95
AINTR/L PB 29
BPARITYER/L 3
BINTR/L PC 1
PD 2
BINTOUT/L PC 50
BDATA7/L PC 45
AIORST/L 3
BDATA6/L PC 43
BDATA5/L PC 41
BRST+BCLR/L 3
BDATA4/L PC 39
BDATA1/L PC 37
BPORTACT/L PC 5
ADATA15/L PB 66
ADATA13/L PB 64
ADATA11/L PB 58
BPINHB/H 6
INVPAR/L 3
BDXS3/L 6
BDXS2/L 6
BDXS1/L 6
BDXS0/L 6
BPARITYER/H 3
PWRST/L 2
P/1
260-182 RP12
1K R15
PC 25 BDS0/L
PC 23 BDS1/L
PC 21 BDS2/L
PC 19 BDS3/L
12X
BDXS0/L 6
BDXS1/L 6
BDXS2/L 6
BDXS3/L 6
390 R19
260-182 RP12
PC 21 BRQENB/L
PD 1 BINTPIN/L
330 R18
1K R14
12S SWITCH
11X
R41 390 Ω +5V
PA 94 DCHPIN/L
DCHPOUT/L PA 93
* COMPONENTS WHICH MAY BE REMOVED FOR SINGLE PORT OPERATION.
I/O LOGIC
DS21E252
E
SEE SHT. 1
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
DA21E250
128/ 32K MEMORY
A/B PORT SCHEM. DIAGRAM
DWG NO. DS21E252
SHT 7 OF 16 SHTS



MEMORY CHIPS 3S THRU 3AA
AND 3F THRU 3M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY QTY 1

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.30

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

MEMORY ROW A

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE

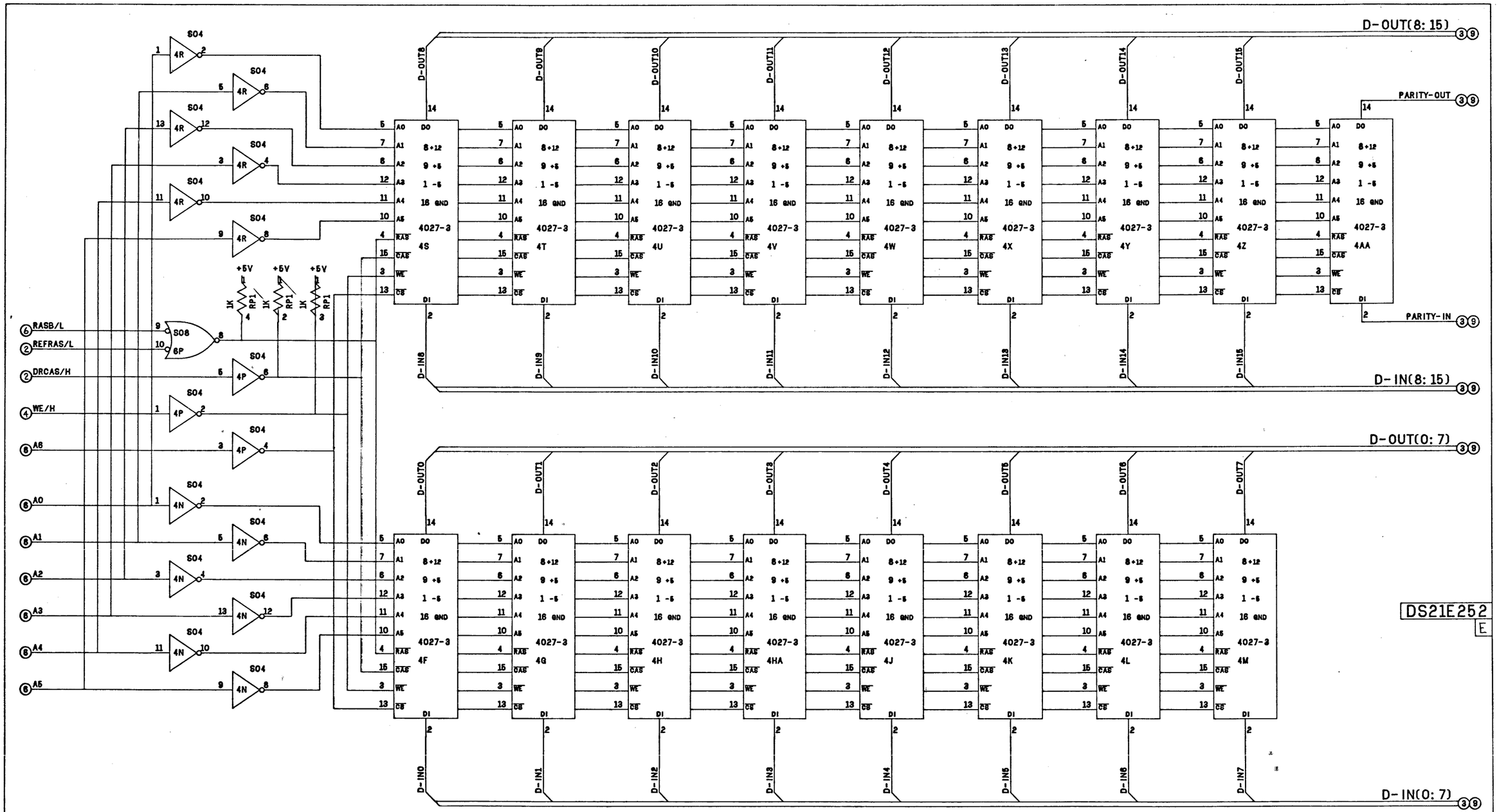
DWG NO. DS21E252

UNIT

WT.

SHT 8 OF 16 SHTS

DS21E252
E



MEMORY CHIPS 4S THRU 4AA
AND 4F THRU 4M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MATERIAL

FINISH

DA21E250 | 1
PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±2°-.100

DRN G MOSS8
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
200 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

MEMORY ROW B

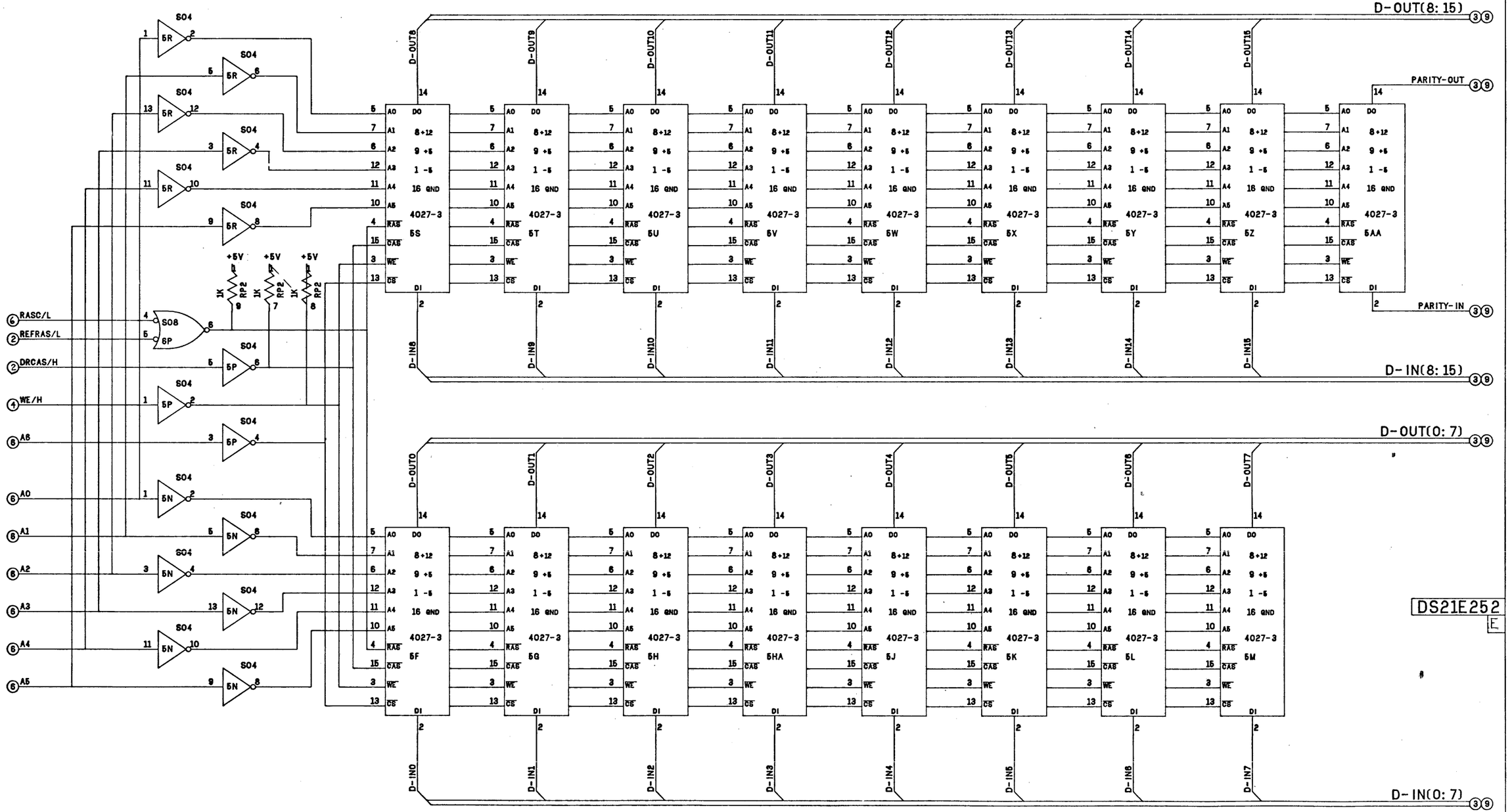
SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 9 OF 16 SHTS

DS21E252
E



MEMORY CHIPS 5S THRU 5AA
AND 5F THRU 5M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

MEMORY ROW C

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY QTY 1

REMOVE ALL BURRS AND SHARP EDGES

TOLERANCES DECIMAL
XX ±.01
XXX ±.005
XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.100

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

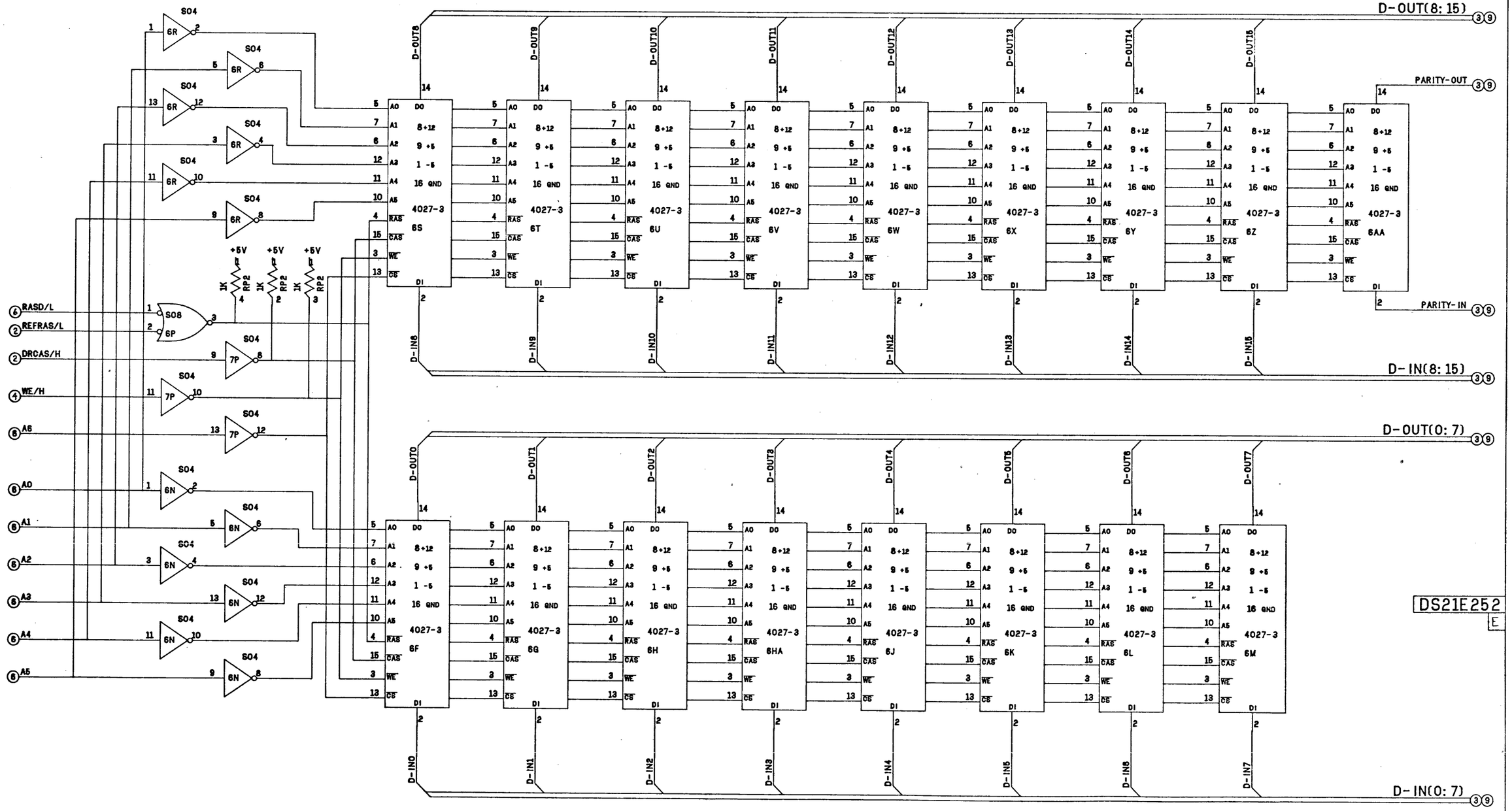
TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

SCALE

DWG NO. DS21E252

UNIT WT.

SHT 10 OF 16 SHTS



MEMORY CHIPS 6S THRU 6AA
AND 6F THRU 6M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MATERIAL

FINISH

PART NUMBER DA21E250 1 NEXT ASSEMBLY QTY

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.100

DRN S HOSSE
CHK
ENGR
PROJ
MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

MEMORY ROW D

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCHEM. DIAGRAM

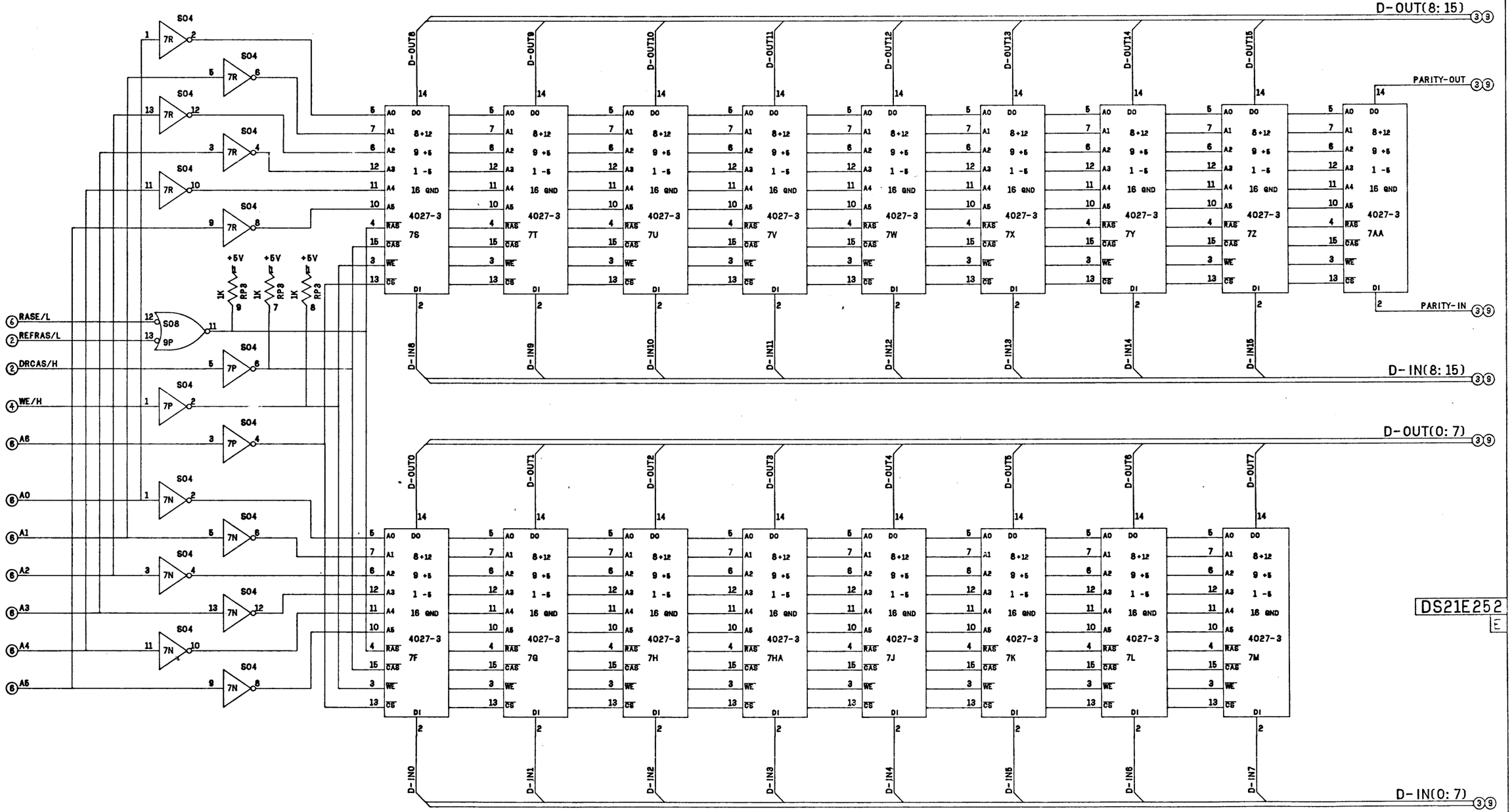
SCALE

DWG NO. DS21E252

UNIT WT.

SHT 11 OF 16 SHTS

DS21E252
E



DS21E252
E

MEMORY CHIPS 7S THRU 7AA
AND 7F THRU 7M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW E

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.30

MATERIAL
FINISH
PART NUMBER DA21E250 1
NEXT ASSEMBLY QTY

DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

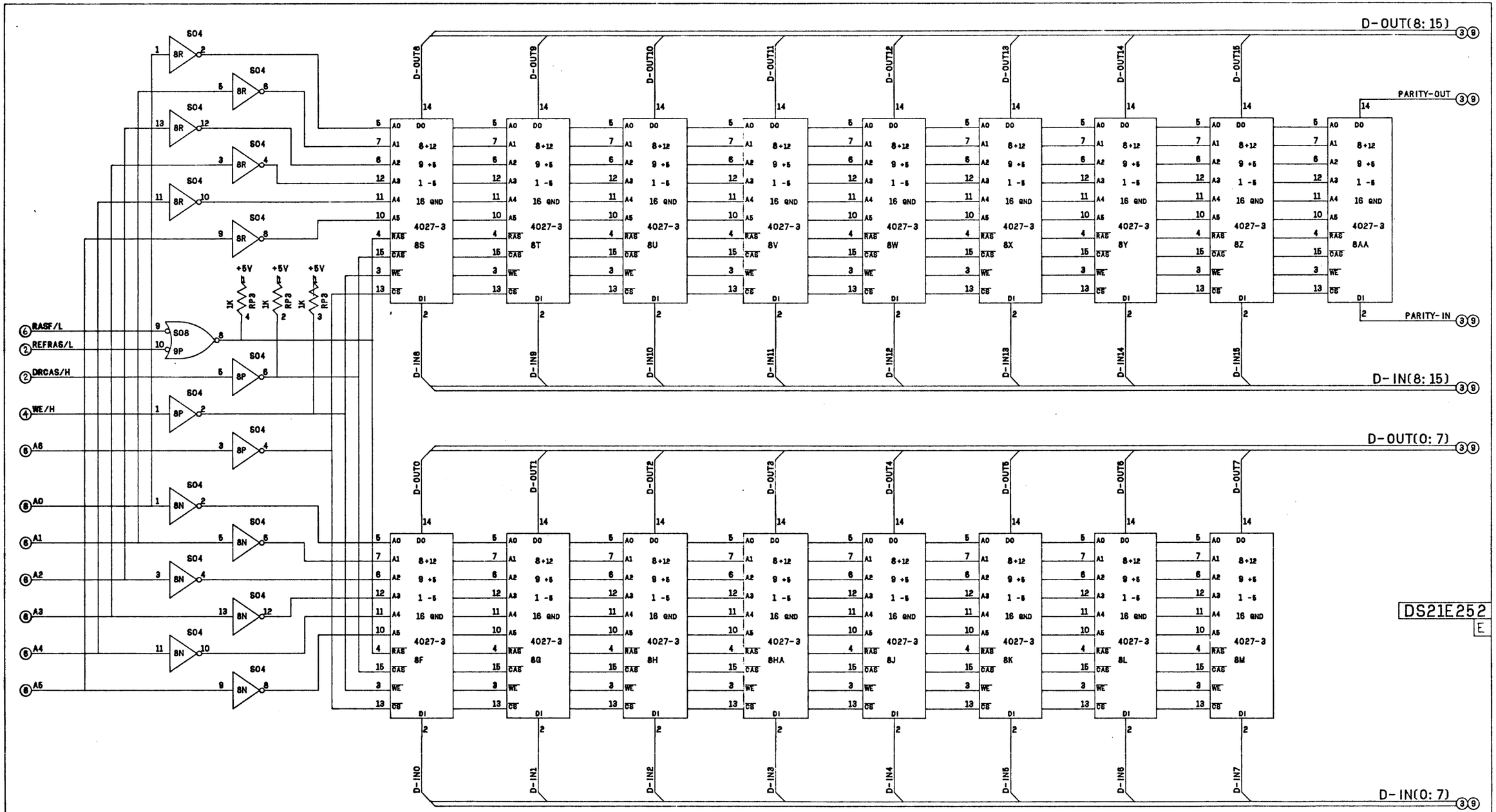
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
UNIT WT.
DWG NO. DS21E252
SHT 12 OF 16 SHTS



DS21E252
E

MEMORY CHIPS 8S THRU 8AA
AND 8F THRU 8M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW F

TOLERANCES UNLESS SPECIFIED
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0050
FRACTIONAL ±1/64
ANGULAR ±.100

MATERIAL
FINISH
DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

PART NUMBER DA21E250 | NEXT ASSEMBLY | QTY 1

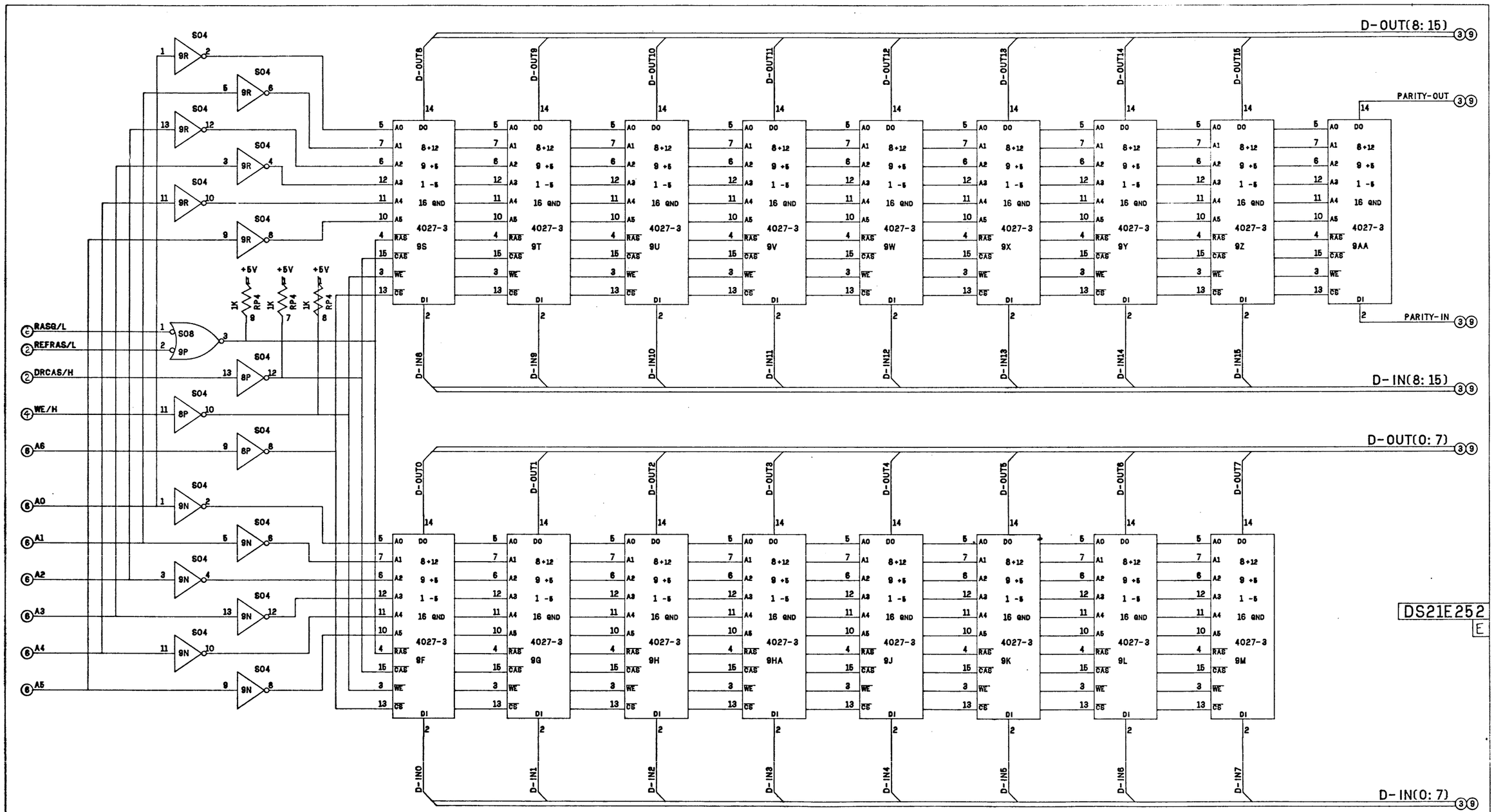
COMPUTERVISION CORP.
201 BURLINGTON RD. ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 13 OF 16 SHTS



MEMORY CHIPS 9S THRU 9AA
AND 9F THRU 9M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

DS21E252
E

MEMORY ROW G

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MATERIAL

FINISH

PART NUMBER DA21E250 1
NEXT ASSEMBLY QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
XX +-.01
XXX +-.005
XXXX +-.0010
FRACTIONAL +-1/64
ANGULAR +-.100

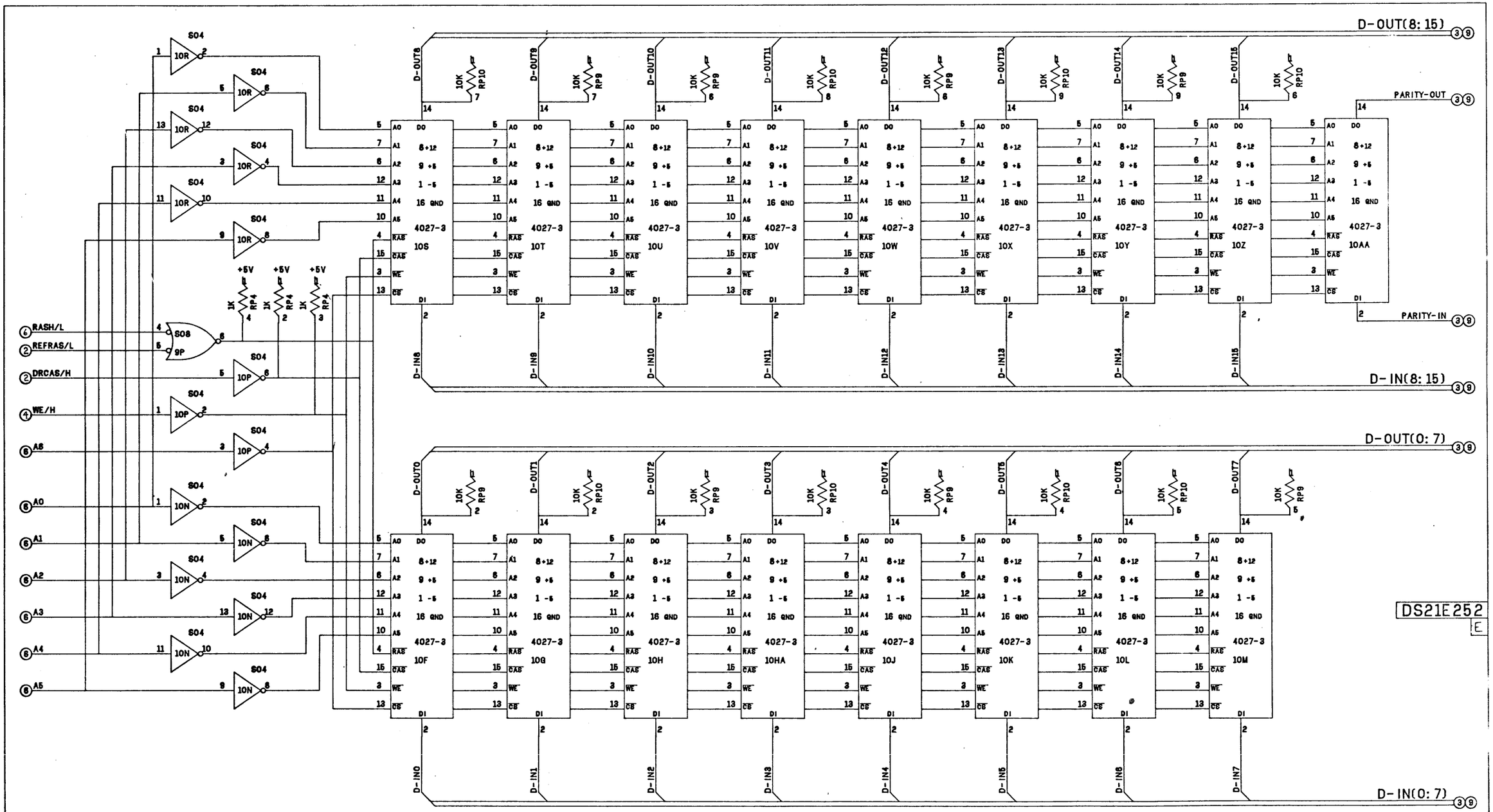
DRN S HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORTS SCHEDIA...

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 14 OF 16 SHTS



DS21E252
E

MEMORY CHIPS 10S THRU 10AA
AND 10F THRU 10M MAY BE
EITHER ALL 4027-3 OR
4116-3 PARTS

MEMORY ROW H

MATERIAL	
FINISH	
PART NUMBER	DA21E250
NEXT ASSEMBLY	
QTY	1

TOLERANCES UNLESS DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0050
FRACTIONAL ±1/64
ANGULAR ±1.00

DRN B HOBBS
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE

DWG NO. DS21E252

UNIT WT.

SHT 15 OF 16 SHTS

B PORT CONNECTORS

CONN C

1	$\overline{\text{BINTR}}$		2
3			4
5	$\overline{\text{BPORTACT}}$		6
7			8
9			10
11	BIORST		12
13	BCLR		14
15	BIOPLS		16
17			18
19	$\overline{\text{BDS 3}}$		20
21	$\overline{\text{BDS 2}}$		22
23	$\overline{\text{BDS 1}}$		24
25	$\overline{\text{BDS 0}}$		26
27			28
29			30
31	BRQENB		32
33			34
35	$\overline{\text{BDATA 10}}$		36
37	$\overline{\text{BDATA 1}}$		38
39	$\overline{\text{BDATA 4}}$		40
41	$\overline{\text{BDATA 5}}$		42
43	$\overline{\text{BDATA 6}}$		44
45	$\overline{\text{BDATA 7}}$		46
47	FREE		48
49		$\overline{\text{BINTPOUT}}$	50

CONN E

1		B MEM RD	2
3	$\overline{\text{B MEM RD}}$		4
5	B MEMWRT	$\overline{\text{BWEMWRT}}$	6
7		BLDMAR	8
9	BLDMAR		10
11	$\overline{\text{B MEM BUS 15}}$		12
13	$\overline{\text{B MEM BUS 14}}$		14
15	$\overline{\text{B MEM BUS 13}}$		16
17	$\overline{\text{B MEM BUS 12}}$		18
19	$\overline{\text{B MEM BUS 11}}$		20
21	$\overline{\text{B MEM BUS 10}}$		22
23	$\overline{\text{B MEM BUS 9}}$		24
25	$\overline{\text{B MEM BUS 8}}$		26
27	$\overline{\text{B MEM BUS 7}}$		28
29	$\overline{\text{B MEM BUS 6}}$		30
31	$\overline{\text{B MEM BUS 5}}$		32
33	$\overline{\text{B MEM BUS 4}}$		34
35	$\overline{\text{B MEM BUS 3}}$		36
37	$\overline{\text{B MEM BUS 2}}$	BWAD2	38
39	$\overline{\text{B MEM BUS 1}}$	$\overline{\text{BWAD1}}$	40
41	$\overline{\text{B MEM BUS 0}}$	$\overline{\text{RESET}}$	42
43	$\overline{\text{BMC 3}}$	$\overline{\text{BWADD}}$	44
45	$\overline{\text{BMC 2}}$	$\overline{\text{BWCO}}$	46
47	$\overline{\text{BMC 1}}$	$\overline{\text{BPARER}}$	48
49		$\overline{\text{B MEM BUSY}}$	50

ALL UNUSED PINS GROUNDED

VOLTAGE FEEDS FOR CONNECTORS PA,PB	
+12 VOLTS	B46,A7,A8
-5 VOLTS	B81
-12 VOLTS	B71,B72
+5 VOLTS	A/B3,A/B4,A/B97,A/B98
GND	A/B1,A/B2,A/B99,A/B100

DS21E252
E

MATERIAL

FINISH

PART NUMBER DA21E250 NEXT ASSEMBLY 1 QTY

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 3A
BEDFORD, MASS. 01730

TOLERANCES
DECIMAL
.XX ±.01
.XXX ±.005
.XXXX ±.0010
FRACTIONAL ±1/64
ANGULAR ±.100

DRN B MOSES
CHK
ENGR
PROJ
MFG
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT. 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

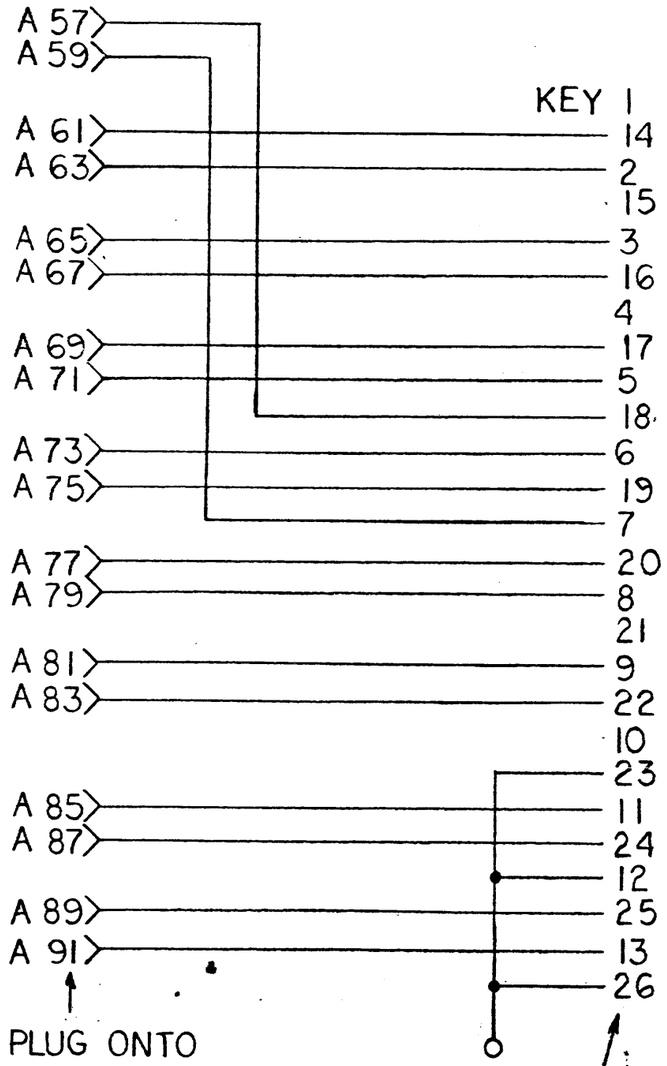
TITLE 128/32K MEMORY
A/B PORT SCH DIA

SCALE
DWG NO. DS21E252
UNIT WT.
SHT 16 OF 16 SHTS

VGU Adaptor Board

Schematic

BS23E027 A



NOTES:

THIS BOARD IS REQUIRED ON ALL CGP'S WITH BACKPLANE ARTWORK ET21E056 REV C OR EARLIER. IT MAY BE USED WITH MORE RECENT BACKPLANES IF DESIRED.

PART NUMBER	NEXT ASSEMBLY	QTY
	L23X004	1
	AA23E025	REF

MATERIAL :

FINISH :

COMPUTERVISION CORP.
201 Burlington Road
Bedford, Massachusetts 01730

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

	NAME	DATE
DRN	T. Rivera	4/17/
CHK		
ENGR		4/21/78
PROJ		
MFG		11/78
SIGNATURE		DATE

REMOVE ALL BURRS AND SHARP EDGES

UNIT WT. —

SYM	REVISION DESCRIPTION	APPD	DATE
A	REL ECO 2932		11/27/78

TITLE SCHEMATIC DIAGRAM, ADAPTOR BOARD

SCALE NONE

DWG NO. BS23E027

SHEET 1 OF 1 SHEETS

MAKEPEACE P-2059

REV A = REV 2

Please cut along this line

REMARKS FORM

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications. All comments and suggestions become the property of Computervision.

TITLE: _____

Order No.: _____

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