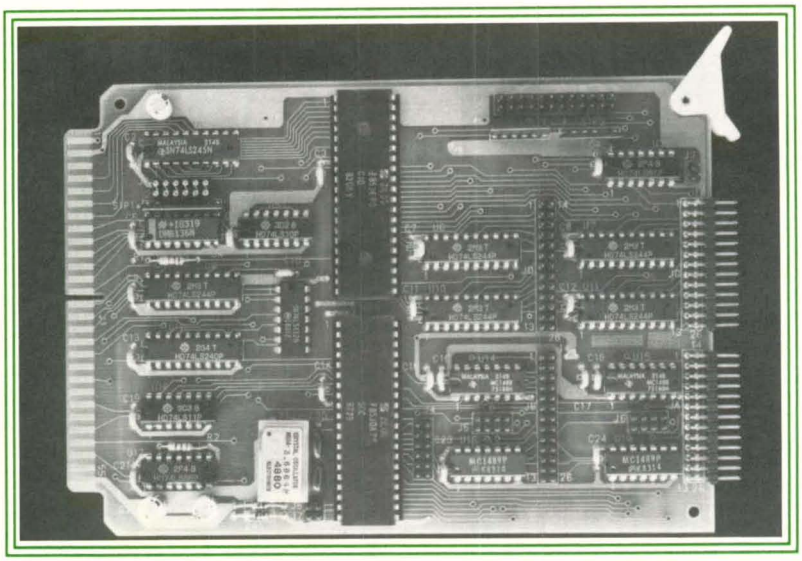
COLEX™

STD-PSIO

STD BUS



FEATURES

- STD Z80 Bus compatible
- Two 8-bit parallel I/O ports
- Two RS-232-C Full Duplex serial ports
- Parallel Channel:
  - — Two 8-bit input, output, or bi-directional I/O ports
  - — One 4-bit special purpose port
  - — Three 16-bit counter/timers
  - — Selectable I/O port polarity
  - — Ports linkable for 16-bit I/O
- Serial Channel:
  - — Multi-protocol — software selectable
  - — Synchronous, Asynchronous, HDLC, SDLC
  - — NRZ, NRZI, FM data encoding/ decoding
  - — Programmable baud rates for each port
  - — One data communication equipment (DCE) port
  - — One data terminal equipment (DTE) port
- 4 MHz operation
- 1 year warranty

DESCRIPTION

The STD-PSIO is a general purpose parallel and serial I/O board for the STD-Z80 Bus. The card contains a high performance ZILOG Z8536 CIO device in the parallel channel combining the features of both a PIO and a CTC. The card also contains a high performance Z8530 SCC device in the serial channel combining the features of a SIO device with on-chip capabilities for NRZ, NRZI, and FM encoding/decoding, as well as a digital phase locked loop for clock recovery and baud rate generator.

Both the parallel and the serial channel are fully featured and support most communications applications. The two 8-bit I/O ports in the parallel channel are fully buffered with handshake and can be individually configured for input, output, or bi-directional operation. One port supports a standard Centronics printer interface. One of the two RS-232-C ports of the serial channel is configured for Data Terminal Equipment (DTE), and the other is configured for Data Communication Equipment (DCE). The serial ports are capable of handling Asynchronous, synchronous, and synchronous-bit oriented protocols. They are also capable of local loop back and auto echo modes.

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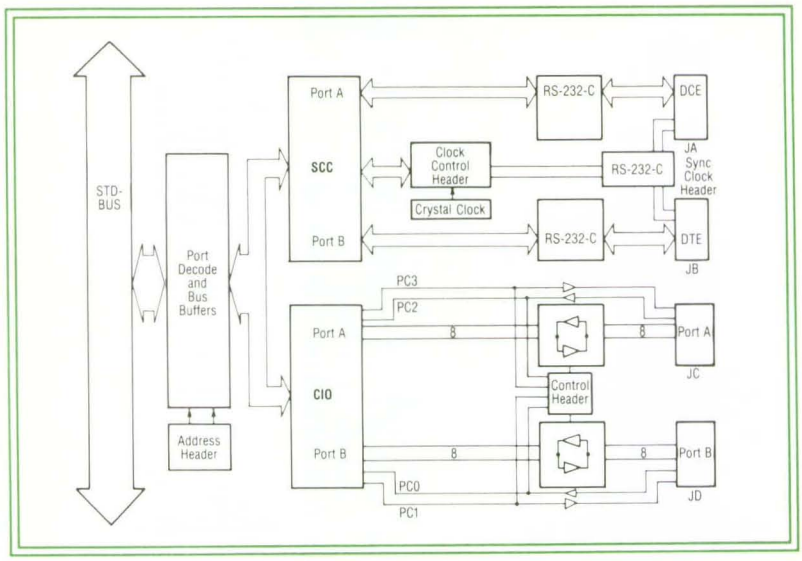
STD-PSIO BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL

- System Bus: STD-Z80
  Inputs: one 74LS load maximum
  Outputs: I_{OH} = −3mA min @ 2.4 volts
  I_{OL} = 24mA min @ 0.5 volts
- System Clock: 4 MHz
- Data Bus: 8-bit, bi-directional
- Address Bus: 16-bit
- I/O Address: Any 8 sequential ports
- I/O Capacity: 2 general purpose 8-bit parallel ports
  I_{OH} = −3 mA min @ 2.4 volts
  I_{OL} = 24 mA min @ 0.5 volts
  1 special purpose 4-bit port
  2 full duplex RS-232-C serial ports
- Interrupts: All three Z80 modes
- System Interrupt Units: 2 SIUs
- Operating Temperature: 0° to 60° C.
- Power Requirements: @ 25° C.

Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	—	4.75	5.00	5.25	volts
I_{CC}	5vdc	—	612	1043	mA
V_{CC}	—	11.4	12.0	12.6	volts
I_{CC}	12vdc	—	38	50	mA
V_{CC}	—	−11.4	−12.0	−12.6	volts
I_{CC}	−12vdc	—	36	46	mA

MECHANICAL

- Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- PC Board Thickness: 0.062 inch
- Connectors:
  STD-Z80 Bus: 56 pin, 0.125 inch centers
  Parallel: 26 pin, dual row, 0.100 inch grid
  Serial: 26 pin, dual row, 0.100 inch grid

ORDERING INFORMATION

Part Number	Description
STD-PSIO	4 MHz serial and parallel interface card with timers
STM-PSIO	STD-PSIO Technical Manual

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COLEX

PSIO

FEATURES

- ☐ STD-Z80 Bus Compatible
- ☐ Two 8-bit Parallel I/O Ports
- ☐ Two RS-232-C Full Duplex Serial Ports
- ☐ Parallel Channel:
  - Two 8-bit Input, Output or Bi-directional I/O Ports
  - One 4-bit Special Purpose Port
  - Three 16-bit Counter/Timers
  - Selectable I/O Port Polarity
  - Ports Linkable for 16-bit I/O
- ☐ Serial Channel:
  - Multi-protocol - Software Selectable Synchronous, Asynchronous, HDLC, SDLC
  - NRZ, NRZI, FM Data Encoding/Decoding.
  - Programmable Baud Rates for Each Port
  - One Data Communication Equipment (DCE) Port
  - One Data Terminal Equipment (DTE) Port
- ☐ 4 MHz Operation
- ☐ 1 Year Warranty

DESCRIPTION

The STD-PSIO is a general purpose parallel and serial I/O board for the STD-Z80 Bus. The card contains a high performance ZILOG Z8536 CIO device in the parallel channel combining the features of both a PIO and a CTC. The card also contains a high performance Z8530 SCC device in the serial channel combining the features of an SIO device with on-chip capabilities for NRZ, NRZI, and FM encoding/decoding, dual on-chip programmable baud rate generators, and a digital phase locked loop for clock recovery.

The two 8-bit I/O ports in the parallel channel are fully buffered and can be individually configured for input, output, or bi-directional operation, and one port supports a standard Centronics™ printer interface. One of the two RS-232-C ports of the serial channel is configured for Data Terminal Equipment (DTE), and the other is configured for Data Communication Equipment (DCE). Both the parallel and the serial channel are fully featured and support most communications applications. The two ZILOG devices on the STD-PSIO are extremely powerful and versatile, and the STD-PSIO allows their features to be fully exploited through software and jumper selected options.

PARALLEL CHANNEL

All Z-80 interrupt modes are supported by the STD-PSIO parallel channel. Each 8-bit port contains pattern recognition logic and special registers to facilitate its use for interrupt control and prioritization. The STD-PSIO is capable of interrupt arbitration among internal and on-board sources and signals are available for daisy-chained prioritizing of additional cards in the STD-Z80 Bus as well.

The three 16-bit counter/timers are all identical and independent. Three different output signal duty cycles are available from each counter/timer, and each is individually programmable for either retriggerable or

non-retriggerable operation. Port B of the CIO device can be software configured to provide access to two of the on-chip counter/timers and the third counter/timer is accessed through the 4-bit special purpose port.

The 8536 CIO device also contains a special 4-bit control port. This port provides handshaking control and signals for the two 8-bit ports. Four modes of handshaking are supported: interlocked, strobed, pulsed, and 3-wire (port A only). The lines are buffered through Exclusive OR gates allowing the user individual control of the polarity for each signal.

SERIAL CHANNEL

The basic role of the 8530 SCC device is parallel to serial conversion, serial to parallel conversion, and control of the process. Within this role, it is software configurable for a wide range of variations on the primary task of serial communication and can be optimized for specific serial communication applications.

The serial channel consists of port A and port B as well as clock, control, interrupt, and status lines. Port A of each channel is configured as a Data Terminal Equipment (DTE) port and port B of each channel is configured as a Data Communication Equipment (DCE) port. The SCC device contains an independently programmable baud rate generator for each port allowing both serial ports on the card to be run at different baud rates as well as other options such as different baud rates for receive and transmit through the same port as the user desires.

Each of the two serial ports are capable of operation under the following protocols: asynchronous, synchronous and synchronous bit or byte oriented protocols such as BISYNC, SDLC, HDLC, etc. NRZ, NRZI, and FM encoding/decoding are supported as well. Within each operating mode, there are provisions for protocol variations by checking odd/even parity, character insertion and deletion, CRC generation and checking, break and abort generation and detection, and many other protocol dependent features. In addition, each port has full modem control capability.

Each port is configured to EIA standard RS-232-C specification for DTE and DCE serial communications operation. All ports support a full complement of handshake signals for connection to a modem. Jumper selected options allow the configuration of each port for almost any synchronous clocking arrangement desired. In addition, jumpers are provided for bypassing the Data Carrier Detect (DCD) logic of each port if the external device does not support this signal.

Programmable configuration of the STD-PSIO by the system CPU is normally done at card initialization at which time all control and data registers are loaded. Control register contents may be examined and/or changed by the system CPU at any time, however.

Items to be loaded include baud rates, communication protocol, interrupt vectors, prioritization instructions, counter/timer parameters, and so on. Other options are selected by strapping pins on control headers. Care has been taken to ensure that jumper connections occur directly across the header where ever practicable allowing options to be selected by simple insertion of Berg™ type straps. In these and other cases, wire-wrapping is satisfactory as well.

For detailed operation and programming procedures, baud rate selection, and other detailed information on the 8530 or 8536, serial communications protocols, specific data on support devices, programming and operation of interrupt controllers, or detailed description or analysis beyond what is presented here, consult the various 7400 TTL data books, serial communications handbook, and Zilog Z80®, CPU, SCC, and CIO technical manual and product specification and data sheets.

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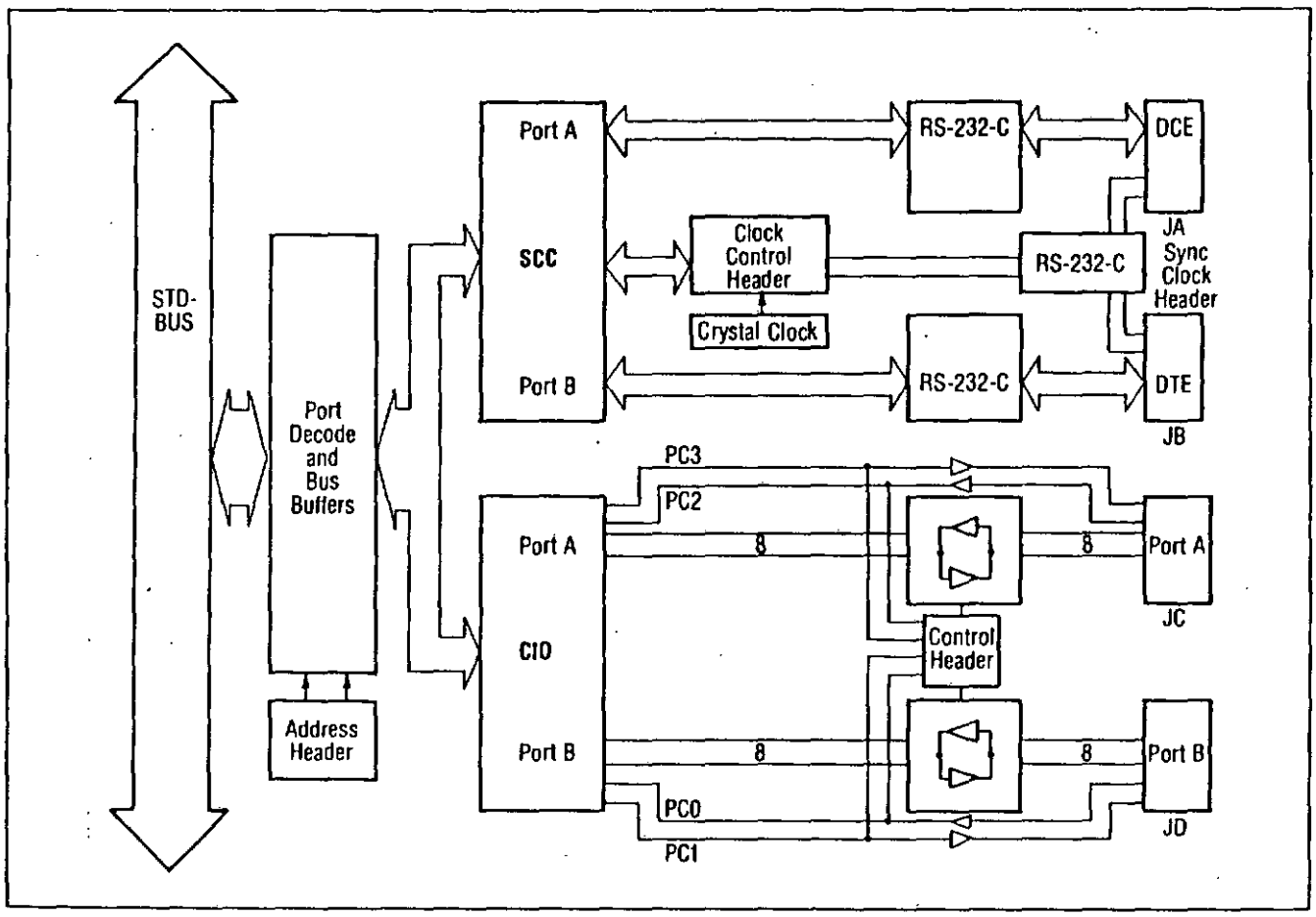


Figure 2. STD-PSIO Block Diagram

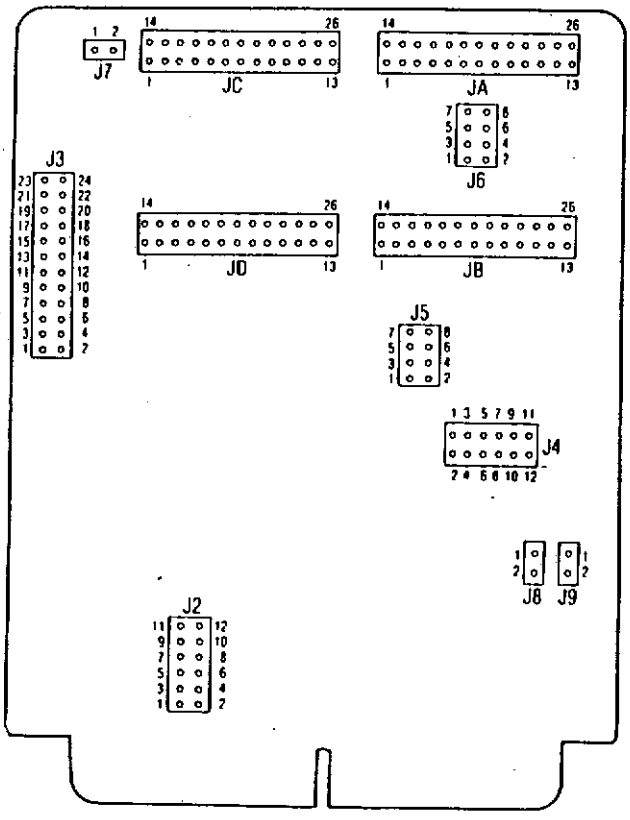


Figure 3. STD-PSIO Connector and Header Locations

Address Line	J-2 Pin Pair	Select 0	Select 1
A7	9-10	Jumpered	Open
A6	7-8	Jumpered	Open
A5	5-6	Jumpered	Open
A4	3-4	Jumpered	Open
A3	1-2	Jumpered	Open
IOEXP	11-12	Jumpered	Open

Figure 4. STD-PSIO Address Selection Header

Port Address				Device
A7-A3	A2	A1	A0	
X	0	0	0	SCC1 (Channel One) Port B Control/Status
X	0	0	1	SCC1 (Channel One) Port A Control/Status
X	0	1	0	SCC1 (Channel One) Port B Data Terminal
X	0	1	1	SCC1 (Channel One) Port A Data (Printer)
X	1	0	0	C101 (Channel One) Port C Read/Write
X	1	0	1	C101 (Channel One) Port B Read/Write
X	1	1	0	C101 (Channel One) Port A Read/Write
X	1	1	1	C101 (Channel One) Port Control

Figure 5. STD-PSIO Port Assignments

OPTION SELECTION

Jumper selectable options, port addresses, and so on are selected by inserting a shorting strap across a pair of control header pins. In most cases, the pins are situated directly across the header from each other allowing the option to be selected by inserting a Berg type strap. In these and other cases, wire-wrapping is satisfactory as well.

The STD-PSIO is addressed by any 8 sequential ports. The port address selection for the entire card is selected by jumpers installed on address header J-2. A jumper installed on the header represents a logic 0 as detailed in figure 4. Specific addresses decoded by the CIO and SCC devices for each port are shown in figure 5.

Beyond port addressing, each of the two channels is completely independent, is configured by separate control headers, and therefore must be configured through jumpers separately.

STD-PSIO SERIAL PORT CLOCK SELECTION

The Z8530 SCC device contains two internal baud rate generators. Only an external clock signal source is required. This source can have a wide variety of origins including a crystal, an oscillator module, System Bus Clock, synchronous communications devices, or some other external source. The baud rate generators divide this signal by a programmable time constant to arrive at the desired rate. The output of the baud rate generator can be used as either the receive clock, transmit clock, or both.

The STD-PSIO is supplied with a 3.6864 MHz crystal installed on the board allowing all popular baud rates to be generated most precisely. Jumpers allow an extremely wide variety of clock combinations to be selected for each port on the board. Figure 6 details logic and strapping locations for the serial channel clock options selections.

Two additional sync clock headers for the serial channel allow the widest flexibility for configuring the board for synchronous communications. These sync clock headers determine the source of both transmit and receive clocks for each of the two serial ports. Consult the Zilog data blocks and Colex application notes to identify jumpering for specific applications.

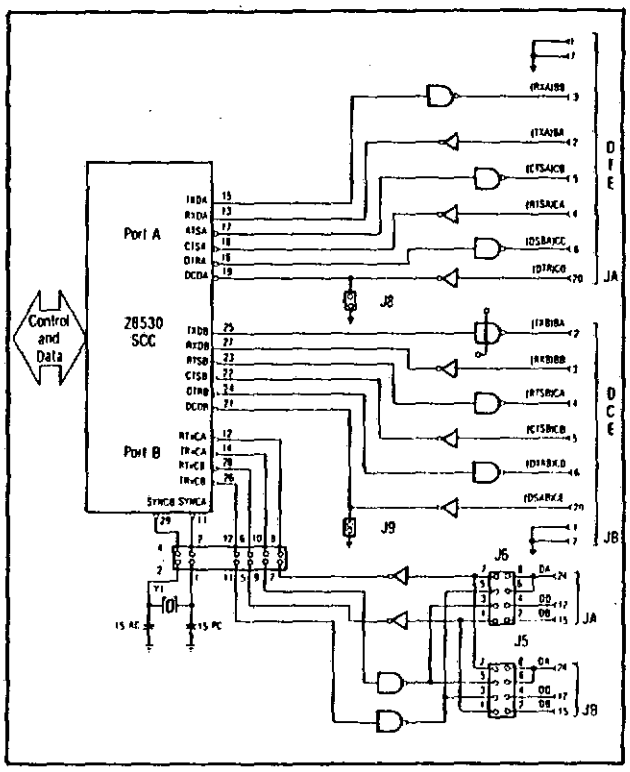


Figure 6: STD-PSIO Serial Channel Jumper Options

SIGNAL CONVENTION

The EIA RS-232-C standard defines machine interfaces as either DTE or DCE. Business machines are defined as Data Terminal Equipment (DTE), and communications equipment is defined as Data Communications Equipment (DCE). The STD-PSIO is designed to support DTE with PORT A and DCE with PORT B. Transmit data, receive data, and all appropriate control signals are provided by the board in accordance with the EIA specifications for signal direction and electrical levels.

The DCD headers permit a jumper to be installed to enable the Data Carrier Detect (DCD) logic in the SCC device. This jumper is required if the DTE does not supply a DTE input and if the DCE does not supply a DSR input. Figure 7 details the correspondence between the individual serial ports, their output connectors, DCD, and sync clock headers.

Serial Port	Output Connector	DCD Header	Sync Clock Header
Port A	J-A	J-8	J-6
Port B	J-B	J-9	J-5

Figure 7. Serial Port Connector and Header Table

PORT OUTPUT CONNECTORS

Both of the serial ports are configured to be RS-232-C type interfaces and each is brought out to a 26-pin, dual row, 0.100 inch grid connector. Figure 8 shows output connector pin out and signal names.

Signal Name	Pin #	Header	Pin #	Signal Name
GND	1	o o	14	-
RX (BA)	2	o o	15	TSE (DB)
TX (BB)	3	o o	16	-
RTS (CA)	4	o o	17	RSE (DD)
CTS (CB)	5	o o	18	-
DSR (CC)	6	o o	19	-
AUX GND	7	o o	20	DTR (CD)
RSLD (CF)	8	o o	21	-
-	9	o o	22	-
-	10	o o	23	-
-	11	o o	24	TSE (DA)
-	12	o o	25	-
-	13	o o	26	-
		o o		

Serial Communication Handshake Signals
TXD (BA) Transmit Data
RXD (BB) Receive Data
RTS (CA) Request to Send
CTS (CB) Clear to Send
DSR (CC) Data Set Ready
DTR (CD) Data Terminal Ready
TSE (DA) Transmit Signal Element Timing (DTE Source)
RSE (DD) Receiver Signal Element Timing (DCE source)
TSE (DB) Transmission Signal Element Timing (DCE source)

PARALLEL PORT CONTROL SELECTION

The control header (J-3) allows the user to control the direction of the channel's three ports. The general purpose 8-bit ports can be configured as bi-directional, input, or output through these headers, and the sense of each special purpose port line can be individually inverted as well. Header J-3 can be divided into two halves. The top half controls port A and two of port C's lines and the lower half controls port B and the other two of port C's lines.

Figure 9 shows selection options. NOTE that each of the general purpose ports (A and B) can be input or output or bidirectional and therefore must be jumpered accordingly. Figure 10 details the parallel port selection header and associated logic. Consult the schematic diagram, 7400 TTL data books, and the application notes for further selection information.

Pins Jumpered	Result
13-1 & 18-6	Port A is Bidirectional
14 & 2	Port A is Output
17 & 5	Port A is Input
15 & 3	Port C, line 2 is not Inv.
16 & 4	Port C, line 3 is not inv.
19-7 & 24-12	Port B is Bidirectional
23 & 11	Port B is Output
20 & 8	Port B is Input
21 & 9	Port C, line 1 is not inv.
22 & 10	Port C, line 0 is not inv.

Figure 9. STD-PSIO Control Header Selection

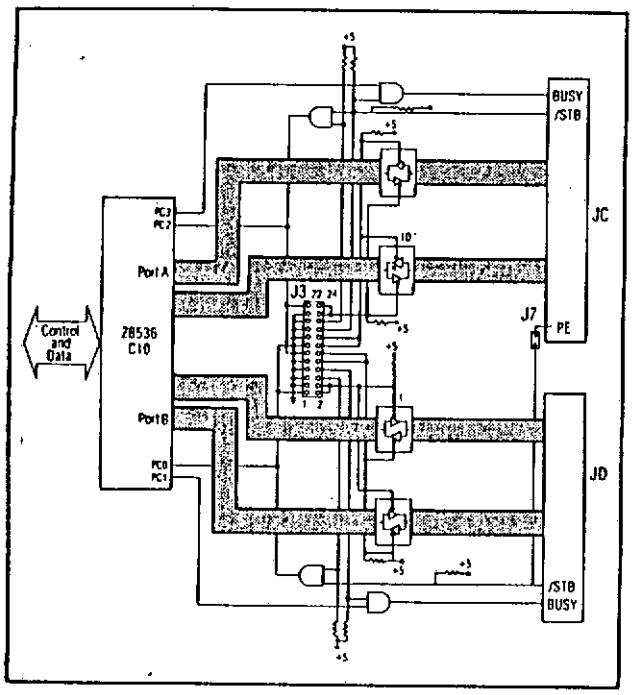


Figure 10. STD-PSIO Jumper Selection

Signal Name	Pin #	Header		Pin #	Signal Name
/STB	1	o	o	14	GND
D1	2	o	o	15	GND
D2	3	o	o	16	GND
D3	4	o	o	17	GND
D4	5	o	o	18	GND
D5	6	o	o	19	GND
D6	7	o	o	20	GND
D7	8	o	o	21	GND
D8	9	o	o	22	GND
N/C	10	o	o	23	N/C
BUSY	11	o	o	24	N/C
PE †	12	o	o	25	N/C
N/C	13	o	o	26	N/C

† Paper End signal available on PORT A only

Figure 11. STD-PSIO Parallel I/O Connector

PARALLEL PORT OUTPUT CONNECTORS

Each of the two general purpose 8-bit ports is brought out to a 26-pin, dual row, 0.100 inch grid connector. Signal names correspond to those used by a Centronics™ parallel printer port. The PE signal originates in the printer, and when activated, usually indicates that the paper has run out. An interrupt or some other action can be generated in response to this signal. If signal PE is to be available (PORT A) strap header J-7. The pin-out for each parallel I/O connector is identical and is shown in Figure 11.

STD-Z80 BUS CONNECTOR

Bus Connector: 56-pin dual edge connector, 0.125 inch centers.

Signal Name	Pin Numbers		Signal Name
+5 VDC	2	1	+5 VDC
GROUND	4	3	GROUND
N/C	6	5	N/C
D7	8	7	D3
D6	10	9	D2
D5	12	11	D1
D4	14	13	D0
N/C	16	15	A7
N/C	18	17	A6
N/C	20	19	A5
N/C	22	21	A4
N/C	24	23	A3
N/C	26	25	A2
N/C	28	27	A1
N/C	30	29	A0
RD*	32	31	WR*
MEMRQ*	34	33	IORQ*
N/C	36	35	IOEXP
N/C	38	37	N/C
N/C	40	39	STATUS1*
N/C	42	41	N/C
INTRQ*	44	43	INTAK*
N/C	46	45	N/C
N/C	48	47	SYSRESET*
N/C	50	49	CLOCK*
PCI	52	51	PCO
N/C	54	53	N/C
N/C	56	55	N/C

Figure 12. STD-Z80 Bus Connector

SPECIFICATIONS

ELECTRICAL

- ☐ System Bus: STD-Z80
- ☐ System Clock: 4 MHz
- ☐ Data Bus: 8-bit, bi-directional
- ☐ Address Bus: 16-bit
- ☐ Signal Loading: Inputs: One 74LS maximum
  Outputs: I_{OH}=3mA min @ 2.4 volts
  I_{OL}=24mA min @ 0.5 volts
- ☐ I/O Address: Any 8 sequential ports
- ☐ I/O Capacity: 2 general purpose 8-bit parallel ports
  Outputs: I_{OH}=-3mA min @ 2.4 volts
  I_{OL}= 24mA min @ 0.5 volts
  1 special purpose 4-bit port
  2 full duplex RS-232-C serial ports
- ☐ Interrupts: All three Z80 modes
- ☐ System Interrupt Units: 2 SIUs
- ☐ Operating Temperature: 0° to 60° C
- ☐ Power Requirement: @ 25° C

Parameter	Condition	Min.	Typ.	Max.	Units
V_{cc}	--	4.75	5.00	5.25	volts
I_{cc}	5vdc	--	612	1043	mA
V_{cc}	--	11.4	12.0	12.6	volts
I_{cc}	12vdc	--	38	50	mA
V_{cc}	--	-11.4	-12.0	-12.6	volts
I_{cc}	-12vdc	--	36	46	mA

MECHANICAL

- ☐ Card Dimensions:

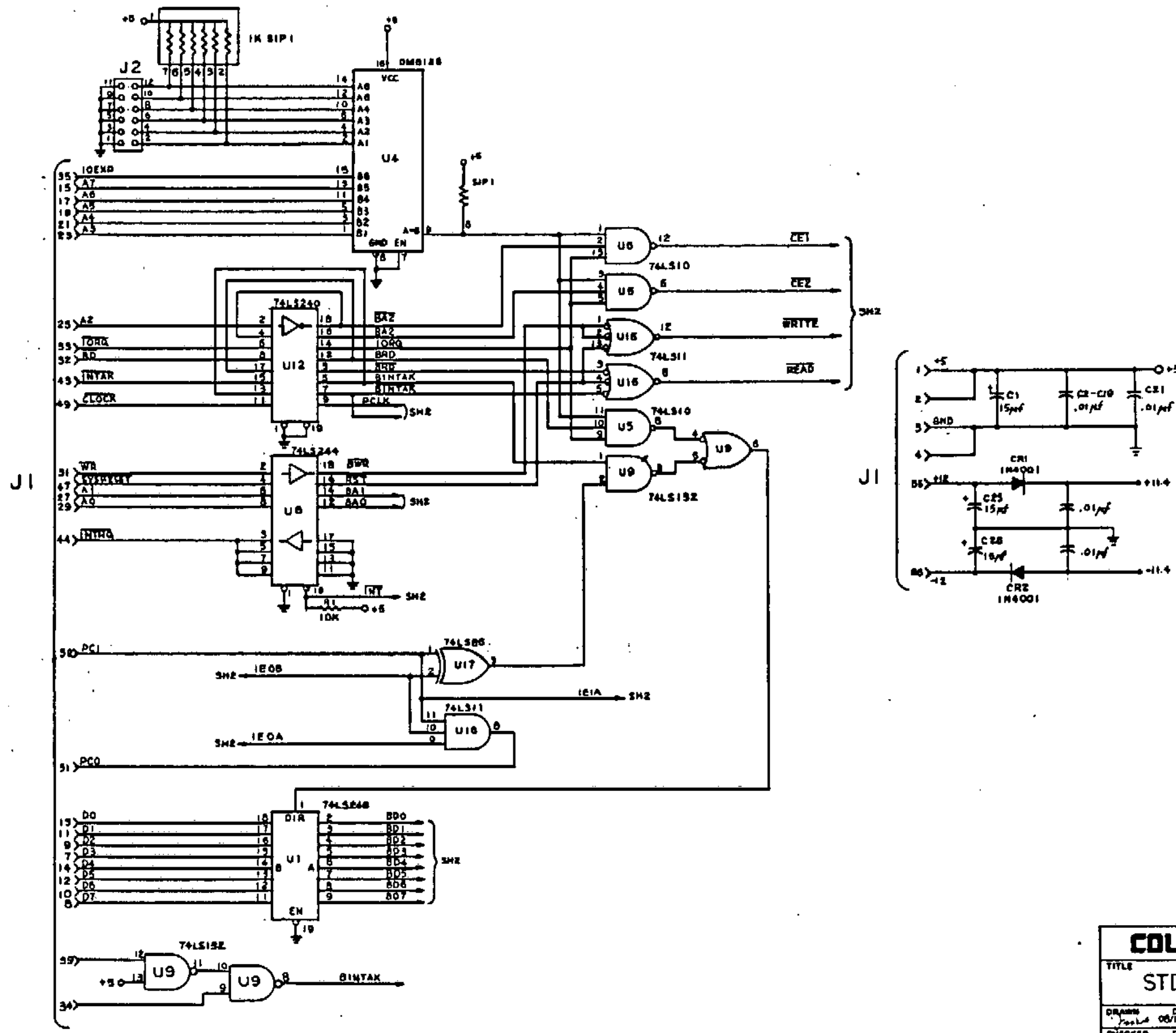
Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- ☐ PC Board Thickness: 0.062 inches
- ☐ Connectors: 56-pin, 0.125 inch centers

STD-Z80 Bus:

Parallel: 26-pin, dual row, 0.100 inch grid

Serial: 26-pin, dual row, 0.100 inch grid



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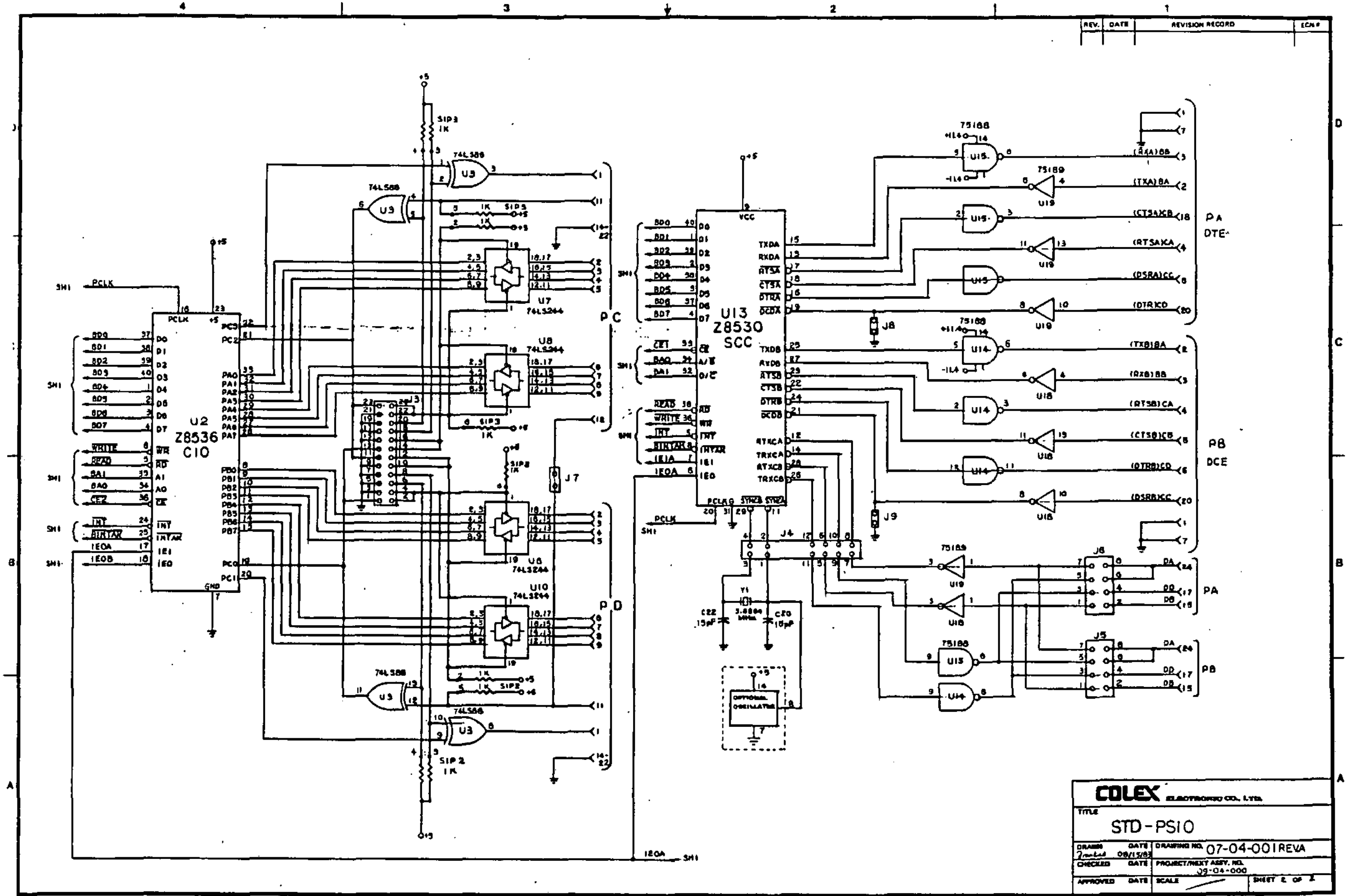
TITLE	STD-PS10		
DRAWN	DATE 08/13/83	DRAWING NO.	07-04-001 REV.A
CHECKED	DATE	PROJECT/NEXT ASSY. NO.	09-04-000
APPROVED	DATE	SCALE	SHEET 1 OF 2



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J9
J4
J5
J6
PC
PD
PA DTE
PB DCE
Y1 3.6864 MHz
C22 15pF
C20 15pF
OPTIONAL OSCILLATOR
COLEX ELECTRONICS CO., LTD.
TITLE
STD-PSIO
DRAWING NO. 07-04-001 REVA
DATE 08/15/83
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SHEET 2 OF 2