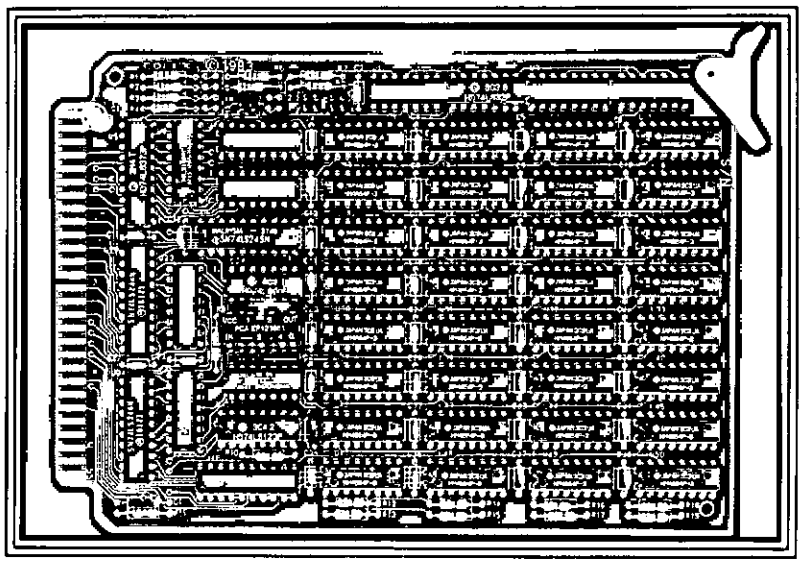
COLEX™ STD-64/128/256DRAM



FEATURES

- 64K, 128K or 256K bytes of dynamic RAM
- STD-Z80 and STD-68K compatible
  - — STD-Z80
    64K bytes direct addressing
    Supports bank select switching
  - — STD-68K
    Compatible with Colex STD-68000
    Direct addressing to 16 Mbytes
    SUPERVISOR protection mode
    USER mode memory disable
- Supports bi-directional DMA of 16- and 24-bit devices
- Supports STD-Z80 DMA cards
- 256K byte boundaries
- Single +5V operation
- 4 MHz operation with no wait states
- 1 year warranty

DESCRIPTION

The STD-256DRAM contains 262,144 (256K) 8-bit bytes of dynamic RAM on a STD-Z80/STD-68K compatible card. The STD-128DRAM contains 131,072 (128K) 8-bit bytes of dynamic RAM, while the STD-64DRAM contains 65,536 8-bit bytes. It provides mass storage of information for instantaneous access by the computer or peripherals via DMA control. The memory is logically oriented in four banks of 8x64K bit dynamic RAMs. Up to 16 Mbytes may be directly accessed and mapped on any 256K byte boundary using direct addressing or 64K byte boundaries using the bank select addressing method. A bank select addressing scheme provides an alternative method for Z80 based boards to address up to 16 Mbytes of RAM.

When used with the Colex STD-68000 card, direct addressing above 64K bytes is achieved by address multiplexing on board the processor card. The additional address lines (A16-A23) are driven on the data bus, latched on the STD-256K card and decoded in the memory map to address the RAMs. This operation is automatic and transparent to the user.

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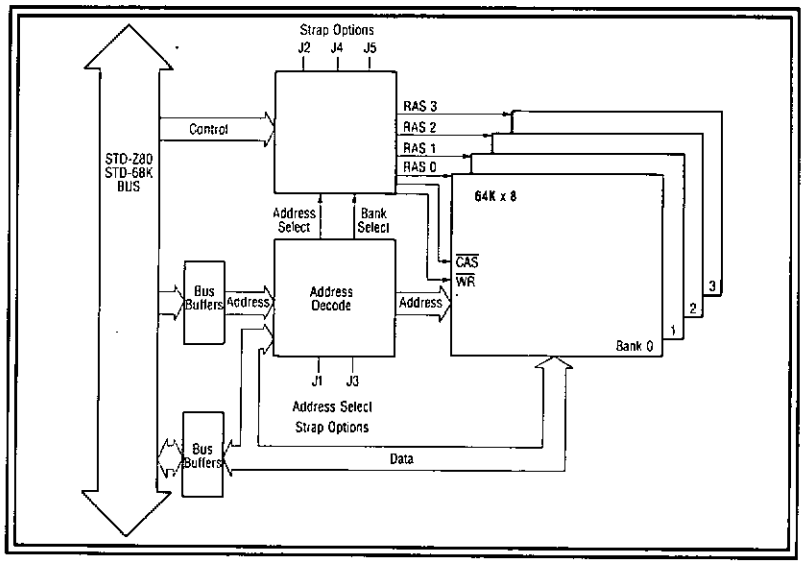
COLEX U.K. LTD. Index House, Ascot Berks, SL57EU, England, (0990)-23377
COLEX ASIA PACIFIC Luk Hop Industrial Bldg., 15th Floor, 8 Luk Hop St., San Po Kong, Kowloon, Hong Kong 3/7265651

STD-256DRAM BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL

- STD-Z80 and STD-68K Bus Compatible
- Data Bus: 8 bits bi-directional
- Address Bus: 16 bits standard with 8 bits extended
- System Clock: 4 MHz
- Access time: 200 ns
- Operating Temperature: 0°C to 60°C
- Signal Loading:
  Inputs: One 74LS maximum
  Outputs: −3mA min @ 2.4 volts
  24 mA min @ 0.5 volts
- System Interrupt Units: 0 SIU's
- Power Requirement @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	—	4.75	5.0	5.25	Volts
I_{CC}	5V	—	573	1985	mA

MECHANICAL

- Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- Printed Circuit Board: 0.062 inches thick
- Connectors:
  STD-Bus: 56 pin dual readout; 0.125 inch center

ORDERING INFORMATION

Part Number	Description
STD-256 DRAM	4 MHz 256K byte Dynamic RAM card
STD-128DRAM	4 MHz 128K byte Dynamic RAM card
STD-64DRAM	4 MHz 64K byte Dynamic RAM card
STM-256DRAM	STD-256DRAM, STD-128DRAM, STD-64 DRAM Technical Manual

COLEX

DRAM

FEATURES

- ☐ 256K, 128K or 64K Bytes of Dynamic RAM
- ☐ STD-Z80 and STD-68K Compatible
  - • STD-Z80
    - 64K Bytes Direct Addressing
    - Supports Bank Select Switching
  - • STD-68K
    - Compatible with Colex STD-68000
    - Direct Addressing to 16 Mbytes
    - SUPERVISOR Protection Mode
    - USER Mode Memory Disable
- ☐ Supports Bi-directional DMA of 16- and 24-bit Devices
- ☐ Supports STD-Z80 DMA Cards
- ☐ 256K Byte Boundaries
- ☐ 4 MHz Operation with No Wait States
- ☐ Single +5V Operation
- ☐ 1 Year Warranty

DESCRIPTION

STD-256DRAM

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When used with the Colex STD-68000 card, direct addressing above 64K bytes is achieved by address multiplexing on board the processor card. The additional address lines (A16-A23) are driven on the data bus, latched on the STD-256K card, and decoded in the memory map to address the RAMs. This operation is automatic and transparent to the user.

Bank select switching for COLEX Z80 CPU cards is also controlled by the MCSYNC* signal. If it is asserted by the processor, data on the data bus will select 1 of 256 possible banks of 64K bytes of memory. The MCSYNC* is asserted by writing to I/O port FF hexadecimal by the CPU board. The CPU then generates the MCSYNC* signal indicating a bank select request. The STD-256DRAM latches the address which is compared and decoded to the address space defined by the jumpers on connectors J1 and J3. The STD-256DRAM contains 4-64K byte banks of RAM on 256K boundaries. The jumpers in Figure 3 locate the banks within the memory map.

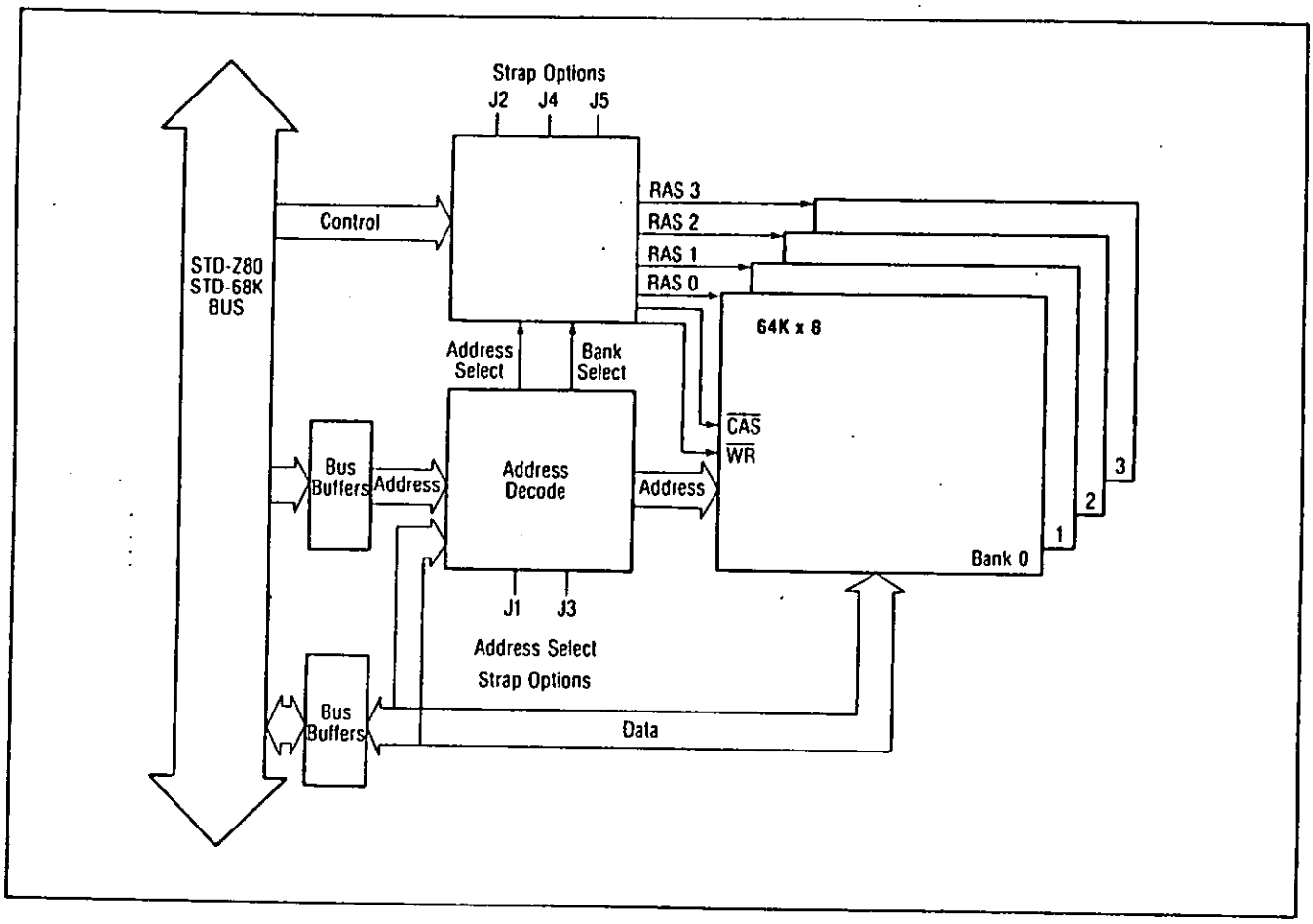


Figure 2. STD-256DRAM Block Diagram

ADDRESS MULTIPLEXER/DECODER

The address decoder decides whether the board is enabled during a memory cycle. The contents of the latched upper address lines (A18-A23) are compared to the board address specified in J1 and J3. The memory map decode is designated by the truth table below. It is a simple binary count sequence that selects 1 of 64 banks of a 256K byte address area in a total 16 Mbyte map.

Connector		J1	J1	J1	J1	J3	J3
Pin Pairs		7 8	5 6	3 4	1 2	3 4	1 2
Decimal Value	Starting Address (HEX)	A23	A22	A21	A20	A19	A18
0	000000	0	0	0	0	0	0
262,144	040000	0	0	0	0	0	1
524,288	080000	0	0	0	0	1	0
786,423	0C0000	0	0	0	0	1	1
1,048,576	100000	0	0	0	1	0	0
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
16,252,928	F80000	1	1	1	1	1	0
16,515,072	FC0000	1	1	1	1	1	1

Figure 3. Memory Address Jumpers

Strapping for address selection is accomplished by adding a jumper between pin pairs. A "0" indicates that a jumper should be inserted, a "1" indicates no jumper is necessary. For example, a system with a starting decimal address of 262,144 (256K) would have no jumper between pins 1 and 2 of J3. The other jumpers on J1 and J3 would be inserted. The STD-256K would then map and decode 256K bytes of memory in this space only.

SUPERVISOR/USER STATE

The STD-256DRAM has the capability of protecting an operating system from USER programs. This is specifically invoked in UNIX environments using a 68000 processor. The SUPERVISOR/USER mode bit is asserted by the processor card in the processor status word and signaled via the MEMEX pin on the STD-68K Bus. If MEMEX is enabled (active high), any memory on the card can be accessed. If MEMEX is not enabled, only the upper 128K bytes (bank 2 and 3) can be addressed. This provides a hardware lockout of memory access when the CPU is in the USER mode preventing unauthorized access to the lower 128K of RAM.

J5 pin pair 1 and 2 selects whether the SUPERVISOR/USER mode is enabled. Inserting a jumper between these pin pairs enables this function of memory lockout in the USER state.

NOTE: If MEMEX is grounded on the motherboard, the ground strap should be removed to enable this function.

DMA DEVICES

The STD-256DRAM supports DMA from STD-Z80 or STD-68K based devices. STD-Z80 compatible DMA's address 64K bytes of RAM on 16 address lines. STD-68K compatible DMA's address 16M bytes of RAM on 24 address lines. Since both types of devices are supported from this card, a jumper is provided to enable either a 16-bit or 24-bit address. Also, the STD-256DRAM will support 68000 systems using STD-Z80 peripheral boards. Each creates a special case and has a special jumper option.

DMA STRAPPING OPTIONS

The DMA and SUPERVISOR/USER options are enabled by strapping the desired pin pair identified in the chart below.

Connector	Pin Pairs	Description
J4	1-2	68000 using 16-bit DMA devices
J4	3-4	68000 using 24-bit DMA devices
J5	3-4	Z80 16-bit DMA
J5	1-2	SUPERVISOR/USER Mode

Figure 4. DMA Selection Jumpers

Note: Do not insert jumpers simultaneously on J4 pin pairs 1-2; J4 pin pairs 3-4 and J5 pin pairs 3-4. These straps are mutually exclusive.

Z80 16-BIT DMA

When using STD-Z80 DMA compatible peripherals with a STD-Z80 processor, pin pair 3-4 should be jumpered on J5. This allows a normal DMA transfer to occur into lower 64K RAM. The maximum memory addressing possible with this strap option is 64K bytes.

24-BIT DMA

When full 24-bit DMA devices are used with the 68000 processor on the STD-68K Bus, pin pair 3-4 should be jumpered on J4. Address decoding is enabled to allow selection of any byte within a 16 Mbyte memory space.

16-BIT DMA WITH STD-68000

The STD-256DRAM permits use of STD-Z80 Bus peripherals with 16-bit DMA's with the COLEX STD-68000 processor board. Peripheral cards such as the STD-FLP2 floppy disk controller require direct memory access. To enable this option, a jumper is inserted between pin pair 1-2 on J-4. This jumper configures the board to read/write data into Bank 0

only. This is done to prevent potential spurious addresses from being latched during DMA cycles from non-CPU bus masters. The STD-68000 CPU still has a full 16 Mbyte address capability.

When more than one STD-256DRAM memory card is running in a system using this DMA capability, a second configuration is required for the remaining memory cards. Pin 2 of J4 must be jumpered to Pin 1 of J5. This prevents dual addressing conflicts in these upper memory cards. No other jumpers should be inserted in pin pairs 1-2 and 3-4 of J4 and pin pairs 3-4 of J5.

J2

J2 is a jumper reserved by COLEX for future expansion. No jumper should be inserted between these pin pairs.

SYSTEM PRECAUTIONS

Data in the STD-256DRAM is not guaranteed to be valid after a PBRESET has been initiated.

The STD-256DRAM requires the dynamic RAM's to be refreshed by the processor every 2 milliseconds. The REFRESH* signal is provided by processor boards meeting the STD-Z80 and STD-68K Bus standards.

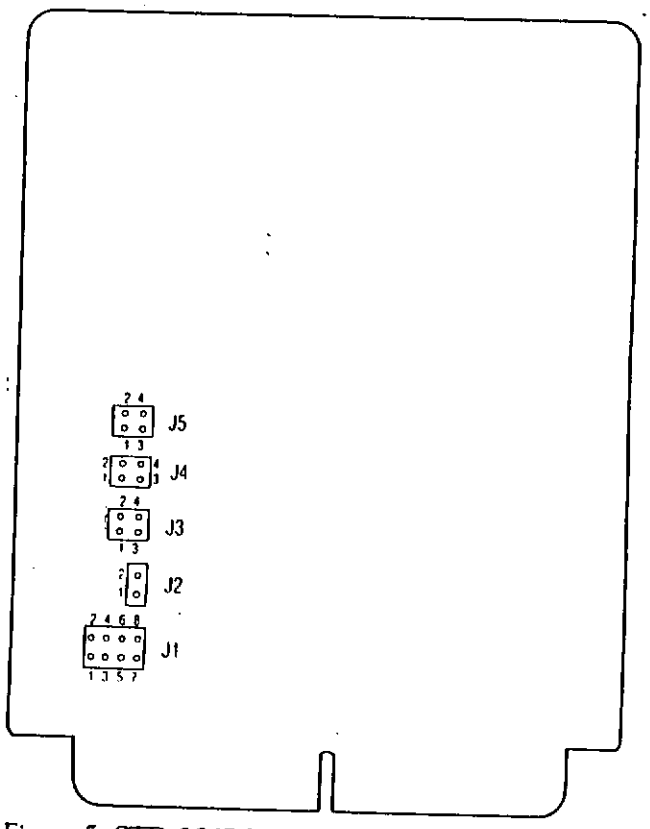


Figure 5. STD-256DRAM Header Locations

STD-128DRAM OPERATION

The STD-128DRAM is a depopulated STD-256DRAM card. The RAMs occupy the lower 128K bytes (bank 0 and 1) on the card. No special requirements or restrictions apply when using the board in this configuration. The board operation is similar except for the amount of addressable memory.

STD-64DRAM OPERATION

The STD-64DRAM is a depopulated STD-256DRAM card. The RAMs occupy Bank 0 on the card responding to the first 64K address space. The card responds to the 64K bytes of contiguous RAM addresses on any 256K boundary.

SPECIFICATIONS

ELECTRICAL

- ☐ STD-Z80 and STD-68K Bus Compatible
- ☐ System Clock: 4 MHz
- ☐ Access Time: 200ns
- ☐ Data Bus: 8 bits bi-directional
- ☐ Address Bus: 16 bits standard with 8 bits extended
- ☐ Signal Loading: Inputs: One 74LS maximum
  Outputs: I_{OH}=-3mA min @ 2.4 volts
  I_{OL}=24mA min @ 0.5 volts
- ☐ Operating Temperature: 0°C to 60°C
- ☐ System Interrupt Units: 0 SIU's
- ☐ Power Requirements: @ 25°C

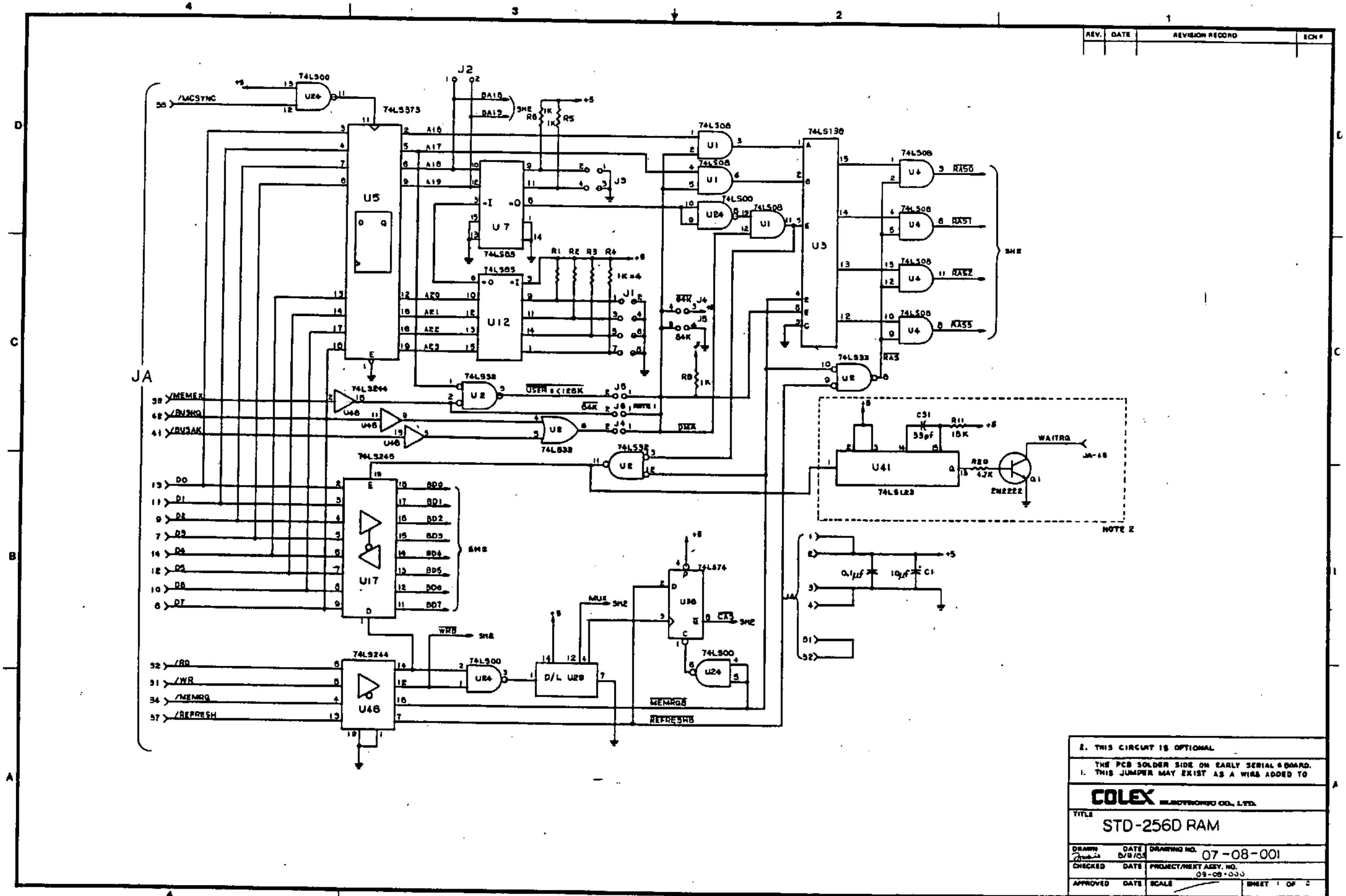
Parameter	Condition	Min.	Typ.	Max.	Units
V_{cc}	–	4.75	5.0	5.25	Volts
I_{cc}	5V	–	573	1985	mA

MECHANICAL

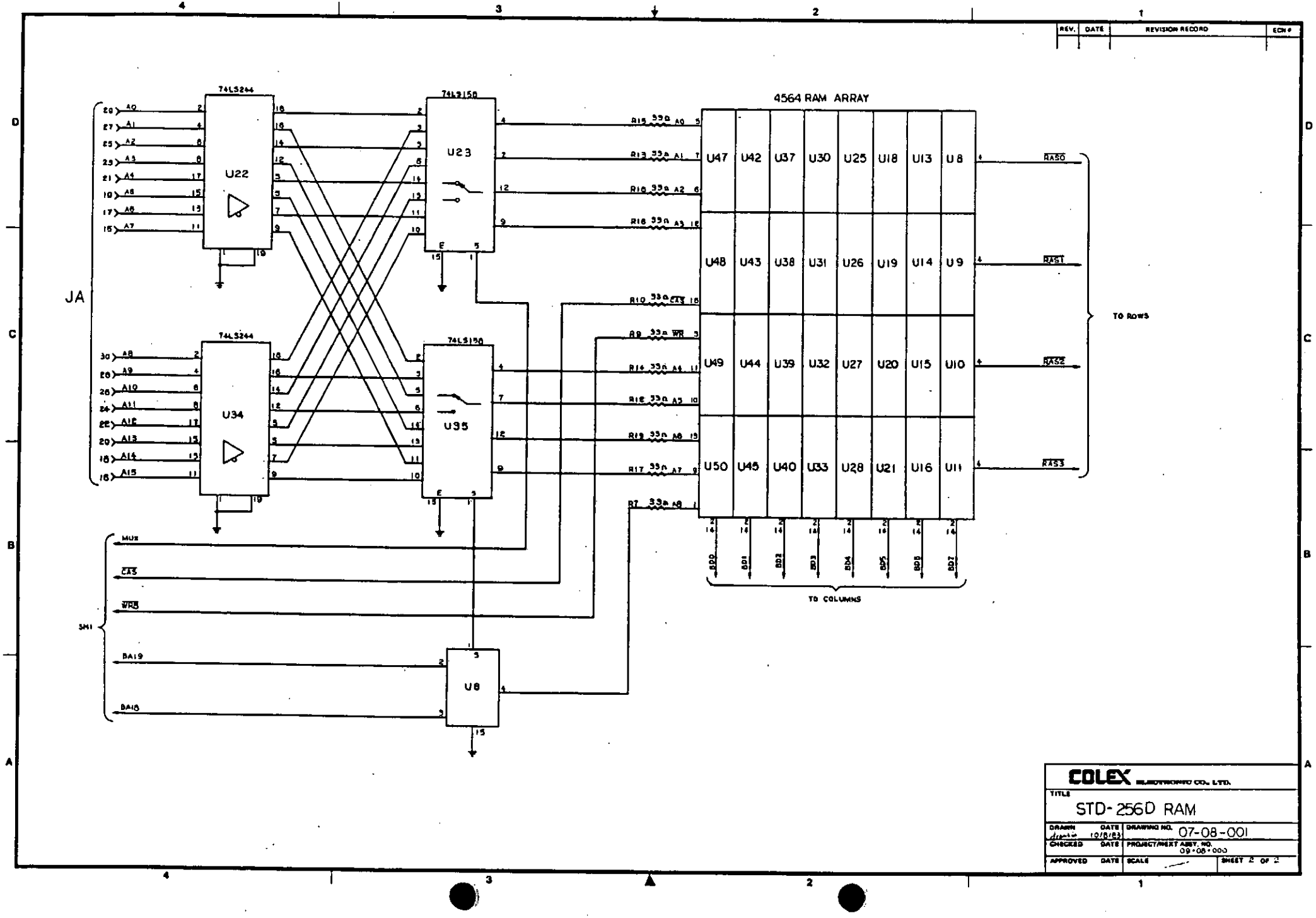
- ☐ Card Dimensions

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- ☐ Printed Circuit Board: 0.062 inches thick
- ☐ Connectors:
  STD-Bus: 56-pin dual readout; 0.125 inch centers



REV. DATE REVISION RECORD ECN #
2. THIS CIRCUIT IS OPTIONAL.
1. THE PCB SOLDER SIDE ON EARLY SERIAL # BOARD. THIS JUMPER MAY EXIST AS A WIRE ADDED TO
COLEX
TITLE STD-256D RAM
DRAWING NO. 07-08-001
SHEET 1 OF 2
JA
U5
U7
U12
U3
U17
U46
U41
74LS373
74LS138
74LS245
74LS244
NOTE 2


REV. | DATE | REVISION RECORD | ECN #
4564 RAM ARRAY
74LS244
74LS158
U22
U23
U34
U35
U8
JA
SMI
MUX
CAS
WRS
BA19
BA18
U47 U42 U37 U30 U25 U18 U13 U8
U48 U43 U38 U31 U26 U19 U14 U9
U49 U44 U39 U32 U27 U20 U15 U10
U50 U45 U40 U33 U28 U21 U16 U11
RAS0
RAS1
RAS2
RAS3
TO ROWS
TO COLUMNS
COLEX ELECTRONICS CO., LTD.
TITLE
STD-256D RAM
DRAWN DATE 10/8/82
DRAWING NO. 07-08-001
CHECKED DATE
PROJECT/NEXT ASSY. NO. 09-08-000
APPROVED DATE
SCALE
SHEET 2 OF 2