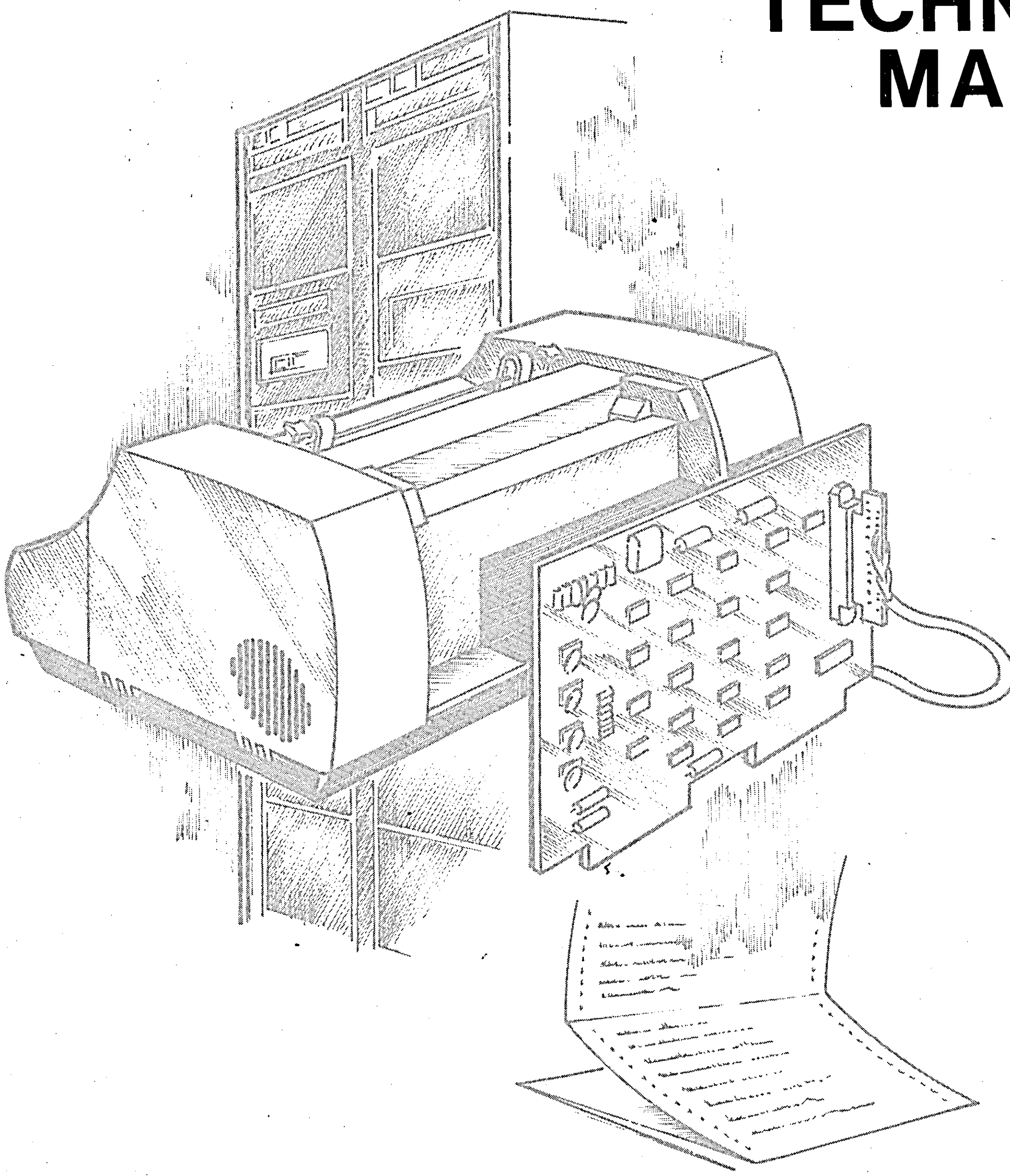
RS232 INTERFACE

TECHNICAL MANUAL



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1. GENERAL

The RS232 Interface is designed primarily to interface the 202C or 202D Dataphone directly (or indirectly via an optional Ring Buffer*) to the Centronics Models 101, 101A, 102A or 306 printers.

The interface accepts serial input data from the data set, assembles the received data into 8-bit characters (seven data bits and one parity bit), checks the parity of the received data and transfers the assembled character in parallel to the printer. Signal levels between the interface and the data set conform to RS232 standards. Signal levels between the interface and printer are TTL compatible.

A reverse channel indication to the data set, controlled by the received data (EOM code) and the status of the printer (or optional Ring Buffer), prohibits data transmission whenever the printer (or Ring Buffer) is not able to accept new data. The absence of a reverse channel response to a data transmission indicates that a parity error was detected in the received data.

A simplified block diagram of the major signal flow between the data set, RS232 Interface, and Printer (or Ring Buffer) is shown in Figure 1.

2. PHYSICAL DESCRIPTION

The RS232 Interface consists of a single printed circuit board and cable assembly all contained in the printer enclosure. The PC board plugs into the interface slot at the rear of the printer. The cable assembly consists of a 10-foot cable with a small etched card (fingerboard) connector at one end and a 25-pin cinch type DB-106040432 plug at the other end. The fingerboard plugs into a connector on the right side of the interface card, and the 25-pin connector plugs into the data set. A connector plate and strain relief bushing is also included which allows the cable to attach to the speaker bracket at the rear of the printer.

*The Centronics optional Ring Buffer is described in a separate manual

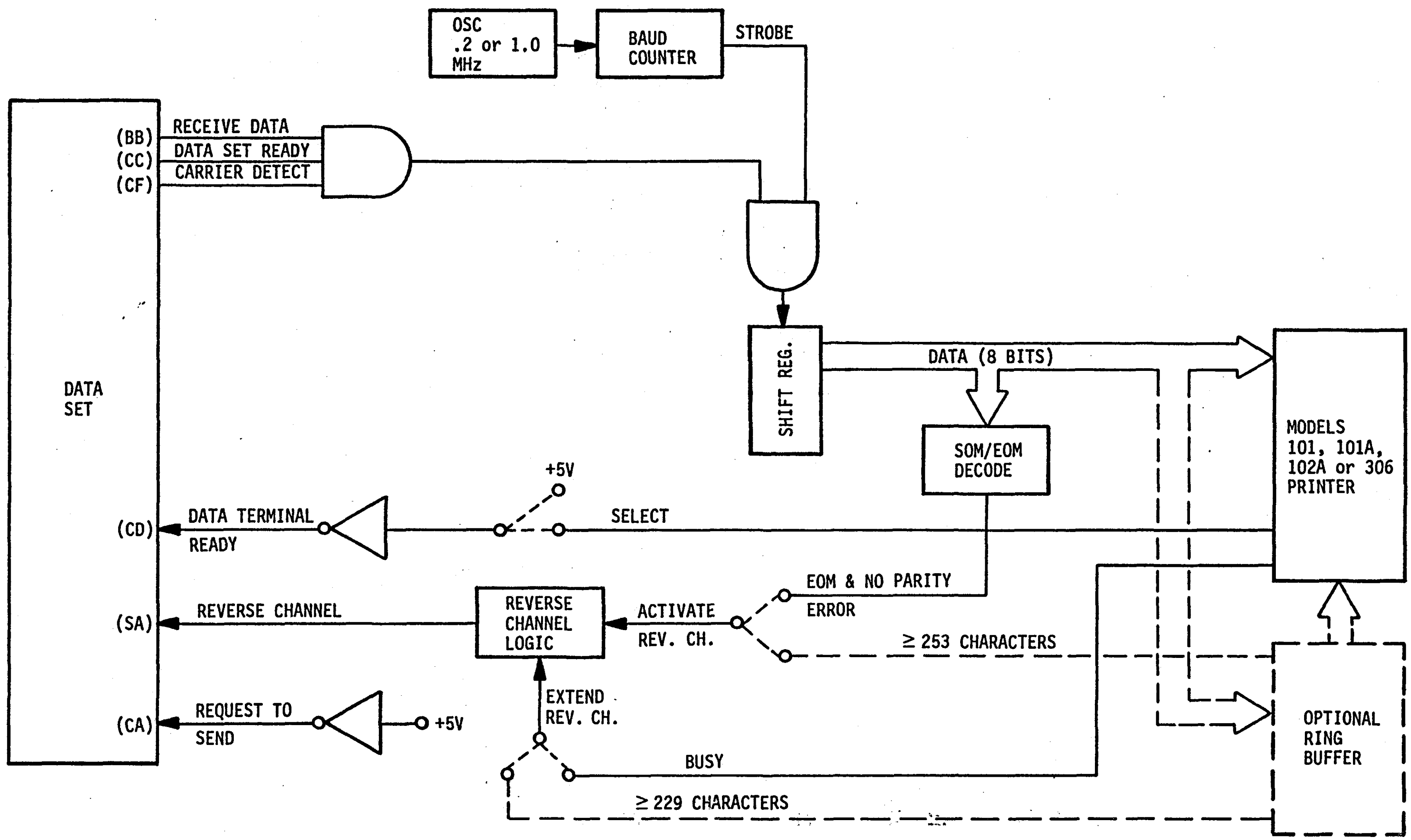


Figure 1. RS232 Interface Data Flow Diagram

3. PROGRAMMING NOTES

3.1 CONTROL CHARACTER FOLLOWED BY EOM

When the RS232 Interface is used, any transmitted control character which could cause a busy condition (e.g., LF, FF, CR, etc.) must be immediately followed by an EOM. The reason for this is a BUSY signal from the printer does not activate Reverse Channel, but only extends Reverse Channel, if it was previously activated.

Without a Reverse Channel response, the data set receives no indication that the printer has gone busy and further data transmissions could result in a loss of data.

An EOM (with no parity errors in the preceeding message) will activate Reverse Channel.

In the 102A, a busy condition can also be caused by an Elongated Character code (octal 016), because the carriage must return to the left margin before printing elongated characters. As a result, in a 102A an RS232 Interface, each octal 016 code must also be followed by an EOM.

3.2 TRANSMISSION DELAY

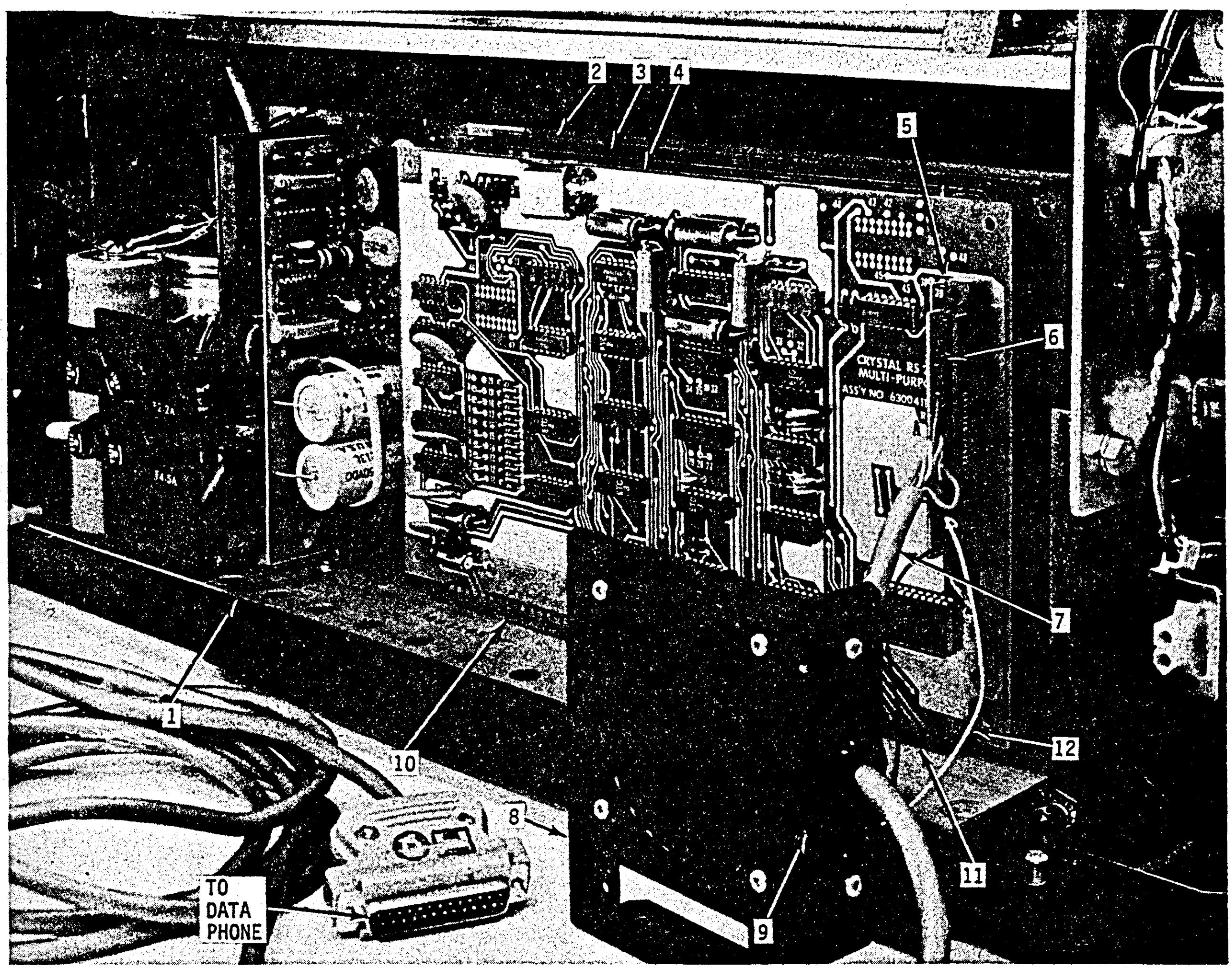
The Reverse Channel signal to the data set is at least 200 milliseconds long and remains active as long as the printer (or Ring Buffer) busy condition exists. After going inactive, Reverse Channel cannot be activated by a new EOM for another 200 milliseconds. This delay is generated on the interface board. As a result, new data should not be transmitted for at least 200 milliseconds after Reverse Channel goes inactive (-12V).

4. INSTALLATION

The RS232 interface is installed in the Model 101, 101A, or 102A printer, as follows: (Reference: Figure 2)

1. Remove the 36-pin Amphenol connector (57-40360) from the speaker bracket at the rear of the printer. Retain the hardware.
2. Unsolder and remove the two wires from the speaker.
3. Remove the ground connection near the speaker bracket and retain the hardware.
4. Unplug the fingerboard from connector J4 and remove the entire W2 cable, fingerboard and amphenol connector. Retain the hardware for possible future re-conversion to parallel interface.
5. Plug the RS232 interface board into connectors J3 and J4 at the rear of the printer.
6. Plug the fingerboard from the RS232 cable assembly into connector J15 on the interface card.
7. With the hardware retained from removing the Amphenol connector (Step 1), secure the adapter plate attached to the RS232 cable assembly, to the speaker bracket.
8. Solder the two loose wires located on the fingerboard to the speaker.
9. Plug the other end of the cable assembly to the data set.

To install the RS232 interface, a 306 printer, refer to Field Bulletin LP# 1018 dated 10/5/73, "Model 306 - Interface Conversion."



1. Electronics Cavity Model 101/101A Printer
2. Electronic Card No. 2
3. Electronic Card No. 1
4. RS232 Interface Card
5. Connector J15 (31230019)
6. Fingerboard Connector P15 (6300000-1)
7. Cable Assembly W4
8. Speaker bracket
9. Plate Adapter
10. Connector J3
11. Connector J4
12. Speaker Wires

Figure 2. RS232 Interface Installation Diagram

5. BOARD CONFIGURATIONS

5.1 GENERAL

Each board is stamped with its baud rate followed by a dash number and/or a special number.

For example,

1. 2400-2: The 2400 signifies that the board is configured for a 2400 baud data input, the -2 specifies the jumper connections on the board, as shown in Tables 1 and 2 in this section.

2. 1200-3-S7 signifies a special board configured for 1200 baud and the -3 jumper connections specified in Tables 1 and 2, but with special modifications such as a component change on the board or a cut in the etch. Each special is described in a separate documentation package.

5.2 BAUD RATE

Baud rates ranging from 110 to 9600 can be accomodated by the RS232 interface. For rates below 600 baud, the oscillator circuit contains a 0.2 MHz crystal and capacitors C3, C4 and C16. For rates of 600 to 9600 baud, a 1MHz crystal is used and capacitors C3, C4 and C16 are deleted.

The crystal and jumper configuration for each baud rate is specified in Tables A through E on drawing #63004114 (sheet 4).

As an example, the jumper connections for a 9000 baud rate are as follows:

1. Referring to Table A and Note 4, a 1MHz crystal is used, C3, C4 and C16 are not used, and Tables D and E specify the jumper connections.

E5-E15	(32 usec)	
E7-E17	(16 usec)	
E2-E12	(4 usec)	
E3-E13	(2 usec)	
	54 usec	(total)

5.3 JUMPER OPTIONS

There are presently five dash numbers specifying standard jumper options. These dash numbers and options are listed in Tables 1 and 2 in this section (and also Tables I and II on assembly drawing #63004113).

Table 1
Jumper Configuration

DASH NO.	JUMPER OPTIONS (see Table 2)	REMARKS
-1	A, F, I, J, L, N	Direct Input to Printer (Even Parity)
-2	B, F, I, J, L, N	Direct Input to Printer Input (Odd Parity)
-3	A, G, H, K, L, N	Ring Buffer Input (Even Parity)
-4	B, G, H, K, L, N	Ring Buffer Input (Odd Parity)
-5	D, F, I, L, N, P	Reference S3 Special

See also Tables A through E on Assembly and Schematic Drawings

Table 2
Jumper Options

JUMPER OPTION	JUMPER CONNECTION	DESCRIPTION
A	E22 to E21, E25 to E26	Even Parity (Normal)
B	E22 to E23, E25 to E26	Odd Parity (Normal)
C	E22 to E24, E25 to E24	Parity Disable (Disable Presetting of @ Sign).
D	E22 to E21, E25 to E24	Even Parity @ only (Disable Parity but Print @ Per Character).
E	E22 to E23, E25 to E24	Odd Parity @ only (Disable Parity but Print @ Per Character).
F	E28 to E27	Busy Enable (Normal)
G	E28 to E29	Busy Disable (Ring Buffer)
H	E32 to E31	HICNT Enable (Ring Buffer)
I	E32 to E30	HINCT Disable (Normal) Enables Reverse Channel when HICNT is not used.
J	E35 to E33	Select In (When selected, CD is held at +12V).
K	E35 to E34	Select Out (CD is always held at +12V) (Ring Buffer).
L	E36 to E37	Protective Ground In
M	- -	Protective Ground Floating
N	E39 to E38	Reverse Channel Normal Output
O	E40 to E35	CD (Controlled by Busy, Normally -12V, when active +12V).
P	E41 to E35	CD (Controlled by Busy Normally +12V, when active -12V).

6. DATA FLOW

6.1 DATA TRANSMISSION BY DATA SET

Once the call has been established, either manually or with the automatic calling unit, the transmitter starts data transmission with a Start of Message code (SOM, Octal 001). This must precede every transmitted line of data and every command code.

The data is transmitted serially and consists of one start bit, seven data bits, one parity bit, and one or more stop bits. In the 101, 101A or 306, if a short line is to be printed, the line is terminated with a Carriage Return code (Octal 015). After the carriage return or control function is transmitted, an End of Message (EOM, Octal 003) is transmitted.

The transmitter must then wait for the Reverse Channel to go active indicating an acknowledge from the interface. If the Reverse Channel level is not received by the transmitter within four seconds after EOM has been transmitted, a parity error may be assumed and the line or function may be retransmitted. If the Reverse Channel level is received, the transmitter waits until the Reverse Channel line goes inactive, waits at least 200 milliseconds, and then transmits the next line of data.

When all data has been transmitted, the call is terminated in accordance with the 202D Dataphone procedures.

6.2 DATA RECEPTION BY THE INTERFACE

Once the call has been properly established, the received SOM character clears the interface logic.

The leading edge of each Start bit starts a clock which clocks each subsequent bit from the data set into an 8-bit shift register. Once the shift register is loaded, parity is checked. If parity is correct, the character in the shift register is transferred in parallel to the printer (or Ring Buffer). If parity error is detected, an octal 100 (@ sign) is forced into the shift register, prior to transferring the data.

Data reception continues in this fashion until an EOM code is received, at which time the parity flip-flop is checked. If no parity error was detected, Reverse Channel is activated and remains active until the printer (or Ring Buffer) is ready to accept more data. If a parity error was detected in the received message, Reverse Channel remains unchanged, and the next SOM resets the error condition.

7. THEORY OF OPERATION

This Theory of Operation section describes the detailed operation of the RS232 Interface. Throughout this section, reference is made to the schematic diagrams in Section 8. The section is subdivided into the following major categories:

- 7.1 Power-Up Prime
- 7.2 Interface Levels
- 7.3 Serial Data Input
- 7.4 Parallel Data Output (to Printer)
- 7.5 Status Indication

7.1 POWER-UP PRIME

Resistor R28 and capacitor C17 from the power-up reset (prime) circuit. With C17 initially uncharged, 0V appears at $\overline{\text{PWPPRM}}$ when power is first turned on. This resets Character Clear flip-flop $\overline{\text{CHACLR}}$ (ME14(1))* which resets flip-flop ME8(2) and triggers one-shot ME19(2) generating a 200 millisecond pulse which resets latch flip-flop ME4(3) and (4). Signal $\overline{\text{PWRPRM}}$ also resets the $\overline{\text{ODDCNT}}$ flip-flop ME5(2), to initialize the STROBE logic.

7.2 INTERFACE LEVELS

7.2.1 Inputs

The signal levels from the data set to the RS232 interface board (+12V and -12V) are converted to TTL levels (0V and +5V respectively) by element ME22 (Type MC1489L). The 6.8K resistors (R21, R22 and R23) in conjunction with the 470 pf capacitors (C5, C6 and C7) establish proper hysteresis levels and frequency response for the circuits.

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*ME14(1) specifies gate 1 on element ME14.
ME14-5 specifies pin 5 on element ME14.

7.2.2 Outputs

The signal levels from the interface board (0V and +5V) to the data set are converted to +12V and -12V levels respectively by element ME26 (Type MC1488L).

When the printer is selected, pin ME18-4 is held low which holds the DATA TERMINAL READY signal (CD) high. The Request to Send signal (CA) is constantly held low by +5V at the ME26 (3) input.

7.3 SERIAL DATA INPUT

7.3.1 General

Data reception by the interface is initiated by detecting a space condition (Start bit) on the Receive Data line for at least a half-bit duration. Detection of this Start bit enables the timing logic to strobe the next eight bits from the Receive Data line into a shift register. The received character is then checked for parity and if no errors are detected, is transferred in parallel to the printer (or optional Ring Buffer).

Baud Rate = 100 - 9600
Start Pulse = One Bit Time
Stop Pulse = Min. of One Bit Time
Mark = Binary 1 (-3V to -27V)
Space = Binary 0 (+3V to +27V)

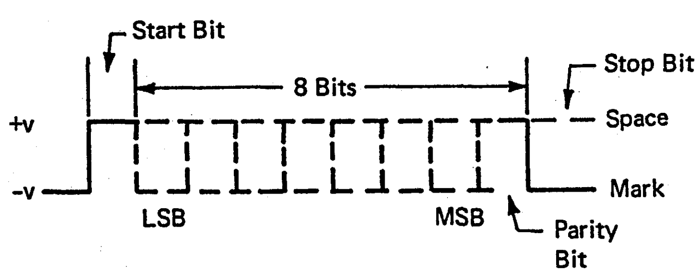

Figure 3. Serial Input Data

7.3.2 Shift Register

Serial data is assembled in an 8-bit shift register ME25. The data input to this register can be in either serial or parallel form depending on the status of the Shift/Load control input (pin 23). A high $\overline{\text{LOAD}}$ signal enables the serial input (pins 1 and 2) and a low $\overline{\text{LOAD}}$ enables the parallel inputs (A through H). Serial data is shifted synchronously on the positive-going clock input (pin 13). Data is shifted in the direction of A to H. Parallel input data is loaded into the associated flip-flop and appears at the outputs on the positive-going clock input.

7.3.3 Input Timing

The input timing logic for the RS232 interface is contained mainly on sheet 1 of the schematic diagrams. With no data being received, the Baud Counter (elements ME1, ME2 and ME3) is held reset by a high output from ME7-6.

As soon as the Receive Data line changes to a Space condition (+12V), RECDAT goes low. If at this time, the data set is ready (DSTRDY is low) and a data carrier is present ($\overline{\text{DACADE}}$ is low), the output of ME12-3 goes low. This causes a high out of ME7-12 and a low out of ME7-6, enabling the baud counter.

The crystal oscillator output OSCCLK (either .2MHz or 1MHz depending on selected baud rate) is counted down by the 10-stage Baud Counter. Each stage in the counter successively halves the output frequency of the preceeding stage. As a result, for a .2MHz clock frequency, the E1 output remains high for a 5 usec interval and the 10th stage output E10 remains high for a 2560 usec interval. For a 1MHz clock frequency, E1 is high for 1 usec and E10 is high for 512 usec.

When the desired count is reached,* decoder outputs ME7-8 and ME6-8 both go low causing ME4-4 and the J-input to ME5(1) to go high.

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*A description of how to configure the decoder for the desired count is contained in Section 5 on Board Configuration.

The next clock pulse sets flip-flop ME5(1). This causes a low input to ME7-4 and a high output at ME7-6, resetting and disabling the baud rate counter. In the interval between this clock pulse and the next (either 1 usec or 5 usec depending on the clock frequency), a STROBE pulse (at ME4-10) is generated. As shown in Figure 4, this STROBE Pulse occurs in the middle of the bit interval and is used to clock the received data into the shift register.

This STROBE pulse is also used in conjunction with a high DATA01 from the shift register to set flip-flop ME14(2). (Note: After each assembled character is transferred to the printer, the shift register is preset to all ONES causing a high DATA01). This causes a low signal at ME7-2, thereby preventing this gate from resetting the baud counter during the rest of the character input.

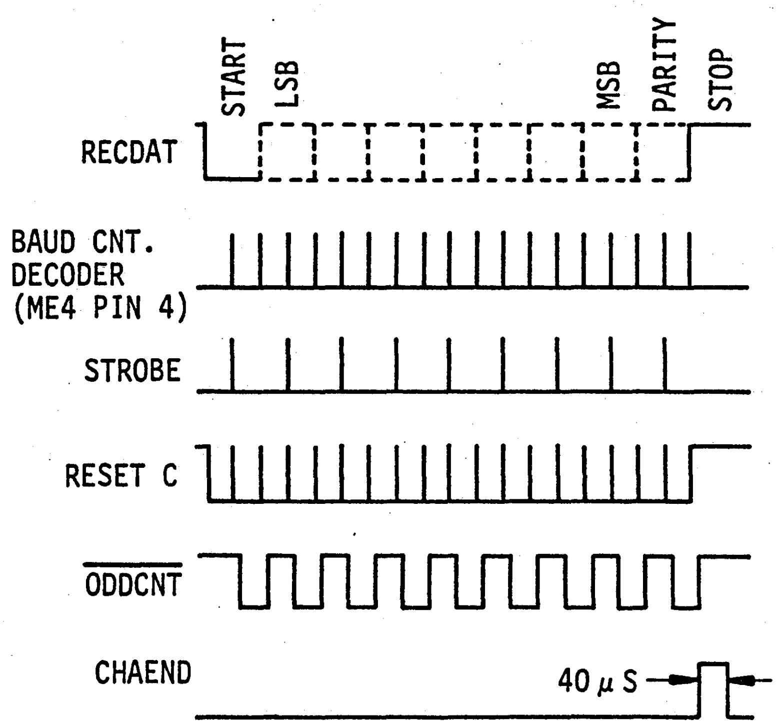


Figure 4. Serial Input Timing

With the counter reset, flip-flop ME5(1) is reset by the next low-going OSCCLK. The low going ME5-12 output then toggles the ODDCNT flip-flop set. This prevents the next decode output from generating a STROBE pulse, and allows only every other decode output to generate a STROBE. This is necessary since the counter is enabled on the leading edge of the Start bit and the decode pulse occurs at twice the baud rate. As a result, the first decode pulse develops a STROBE in the middle of the first bit interval. The second decode pulse which occurs at the end of the first bit interval, is blocked by flip-flop ME5(2) - ODDCNT. The third decode pulse is then enabled, the fourth blocked, etc., causing all STROBES to occur in the middle of the bit interval.

The first STROBE pulse loads the Start bit in the shift register. After the eighth STROBE pulse, this Start bit appears at the DATA01 output. The ninth STROBE pulse then shifts the parity bit into the register and resets flip-flop ME14(2) since DATA01 is now low.

With signal $\overline{\text{ODDCNT}}$ low, the baud counter counts through one more cycle before being reset by ME7(1). However, no more STROBE pulses are generated until the next Start bit is detected.

7.3.4 End of Character

The STROBE pulse that shifts the parity bit into the shift register also resets flip-flop ME14(2). This allows the next high-going $\overline{\text{ODDCNT}}$ output to set flip-flop ME8(2). To synchronize the received character with the internal timing in the printer, the next high-going oscillator output from the printer (OSCXT) sets the End of Character flip-flop (CHAEND). Signal CHAEND initiates the parallel transfer of the received character to the printer.

When the parallel transfer is accomplished, $\overline{\text{CHACLR}}$ goes low resetting flip-flop ME8(2) which allows the next OSCXT pulse to reset flip-flop ME8(1).

7.3.5 Parity Check

The parity circuit consists of flip-flops (ME9(1) and ME9(2). While data is being shifted into the shift register, the STROBE pulse toggles flip-flop ME9(1) whenever RECDAT is high (ONE). As a result, at the end of the character, if the character contains an odd number of ONES, ME9(1) will be in the set state. If the character contains an even number of ONES, ME9(1) will be in the reset state.

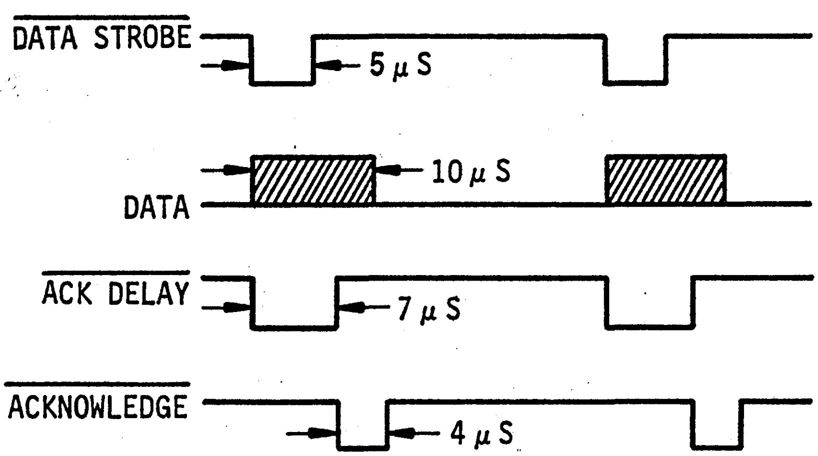
By jumper option, even or odd parity (CHAPAR) can be presented at the input to flip-flop ME9(2). The jumper connection is such that CHAPAR should be high if a parity error is present (see Section 5). If a parity error is present, flip-flop ME9(2) is set by signal PARCK and remains set until the next SOM character is received.

Also, if a parity error is detected, an octal 100 (@ sign) is preset into the shift register by gate ME11(3) before transferring data to the printer.

7.4 PARALLEL DATA OUTPUT (to PRINTER)

7.4.1 General

Once the serial character has been received and parity checked, that character (or an @ sign code if a parity error was detected) is transferred in parallel to the printer input data lines, a data strobe to the printer is generated, (see Figure 5) the RS232 interface logic is reset, and all ONES are preset into the shift register.



Binary 1 = Mark = +2.5V to +5.5V
Binary 0 = Space = 0.6V to 0.4V

Figure 5. Parallel Output Data

7.4.2 Control Character Decode

The shift register outputs are constantly monitored for an SOM (octal 001) or EOM (octal 003) code. Wired - OR gate ME15 and gate ME16 combine the SOM and EOM decodes with loading sequence signal CNT02 to generate $\overline{\text{SOMDEC}}$ and $\overline{\text{EOMDEC}}$.

7.4.3 Output Timing

Setting flip-flop CHAEND initiates the transfer of the received character from the shift register to the printer. As shown in Figure 6, a high CHAEND enables flip-flops ME10(1) and (2). Since CHAEND is synchronized with the system (printer) clock, $\overline{\text{SYSCLK}}$ goes low at the time that CHAEND goes high. When SYSCLK goes high, gate ME13(1) generates Parity Check)PARCK) which loads the Character Parity signal (CHAPAR) into the PARITY flip-flop ME9(2).

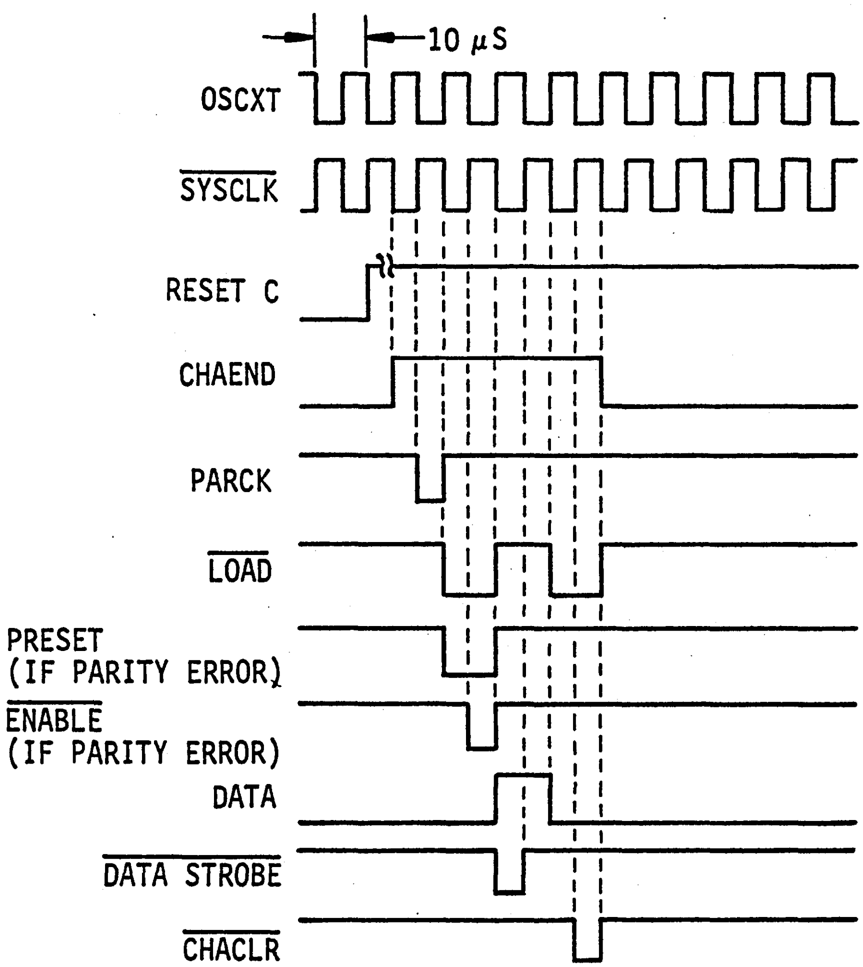


Figure 6. Parallel Output Timing

When $\overline{\text{SYSCLK}}$ goes low, flip-flop ME10(1) is toggled set causing LOAD to go low. This enables the parallel inputs to the shift register.

If CHAPAR is high at this time (indicating a parity error), the following action occurs:

1. Signal PRESET goes low placing an octal 100 code (@ sign at the parallel input to the shift register.);
2. PARITY flip-flop ME9(2) is set;
3. When $\overline{\text{SYSCLK}}$ goes high again, gate ME13(2) generates a low $\overline{\text{ENABLE}}$, which causes a high LOADIN signal out of gate ME12(4);
4. The high LOADIN transfers the @ sign (on the parallel input) into the shift register.

The next low-going $\overline{\text{SYSCLK}}$ toggles flip-flop ME10(1) reset and ME10(2) set causing LOAD and CNT02 to go high. A high $\overline{\text{LOAD}}$ and CHAEND gates the shift register outputs to the input data lines to the printer. A high CNT02 enables the EOM/SOM decoders - ME16(1) and (2). If the character in the shift register is an EOM and there is no parity error, then $\overline{\text{EOMDEC}}$ goes low. Similarly for an SOM character, signal $\overline{\text{SOMDEC}}$ goes low.

While $\overline{\text{SYSCLK}}$ is low, if the printer is not busy ($\overline{\text{BUSY}}$ is high and the Busy Enable jumper is used - E27 to E28), a low $\overline{\text{DATA STROBE}}$ is generated at ME11-8. If the printer becomes busy while DATA STROBE is low, the high output from gate ME15(6) holds ME17-1 low. This holds DATA OUT (ME17-13) high which allows the DATA STROBE pulse (5 usec) to remain high until the next low-going SYSCLK. However, all future DATA STROBE pulses are inhibited until the printer BUSY signal goes high. DATA STROBE is also inhibited if either an EOM or SOM is decoded (EOMDEC or SOMDEC disables gate ME11(1)).

When $\overline{\text{SYSCLK}}$ goes low again, flip-flops ME10(1) and (2) are both set enabling gate ME12(2). This causes the next high-going $\overline{\text{SYSCLK}}$ to reset Character Clear flip-flop ME14(1). The low $\overline{\text{CHACLR}}$ signal then: 1) clears flip-flop ME8(2), 2) clears the Character Parity flip-flop ME9(1), and 3) generates a high LOADIN signal which parallel-loads all ONES into the shift register.

7.5 STATUS INDICATION

7.5.1 General

When used as a direct input to the printer, the RS232 interface uses the Select (SLCT) and BUSY signals from the printer to indicate to the data set the status of the machine. When used as an input to the Centronics Ring Buffer (option), the RS232 interface used the ≥253 and ≥229 signals from the ring buffer for this status indication. In both cases, the reverse channel line is used to prevent transmission of data while the printer (and/or Ring Buffer) is incapable of receiving data. As a program function, reverse channel is also used to inform the transmitter of a parity error in the received data.

7.5.2 Reverse Channel

Two one-shots are associated with the reverse channel logic: 1) ME19(2), triggered when reverse channel goes active, holds RCHAN active for at least 200 milliseconds; 2) ME19(1) prevents an EOM from re-activating reverse channel for at least 200 milliseconds after RCHAN goes inactive.

When the RS232 interface is used as a direct input to the printer, reception of an EOM (low $\overline{\text{EOMDEC}}$) and no parity error detected in the received message (low PARITY) sets latch ME24(3) and (4). Providing that one-shot ME19(1) has timed out, this condition sets latch ME23(1) and (2) activating Reverse Channel (low RCHAN).

If the RS232 interface is used as the input to a Ring Buffer, the accumulation of 253 characters in that buffer (≥253), indicating that it is incapable of receiving more data, causes $\overline{\text{HICNT}}$ to go low. This condition also sets latch ME23(1) and (2) activating $\overline{\text{RCHAN}}$.

In either case, reverse channel going active triggers one-shot ME-19(2). The low $\overline{\text{Q}}$ output from ME19(2) holds pin ME24-2 low and ME24-3 high keeping RCHAN latch ME23(2) and (1) set for at least 200 msec. The one-shot output also resets latch ME24(3) and (4).

When one-shot ME19(2) times out, a Busy signal from the printer (or Ring Buffer) may still hold reverse channel active. If the interface is used as a direct input to the printer, when the EOM which initiated reverse channel is received, the printer will normally be busy operating on the data received in the preceeding message (signal $\overline{\text{BUSY}}$ will be low).

If the interface is used as input to a Ring Buffer, the BUSY signal is replaced with signal (≥229). A high ≥229 signal indicates that the Ring Buffer has accumulated more than 229 character.

When the printer is ready to accept new data (BUSY goes high), or the number of characters in the Ring Buffer drops below 229 (≥229 goes low), and one-shot ME19(2) has timed out, the output of gate ME23(3) goes low. This resets latch ME23(1) and (2) causing $\overline{\text{RCHAN}}$ to go high, deactivating the reverse channel.

The high-going output from ME23(1) fires one-shot ME19(1). The low output from this one-shot inhibits gate ME24(1) for approximately 200 milliseconds. This prevents activating reverse channel for at least 200 msec after reverse channel goes inactive.

7.5.3 Baud Limitation

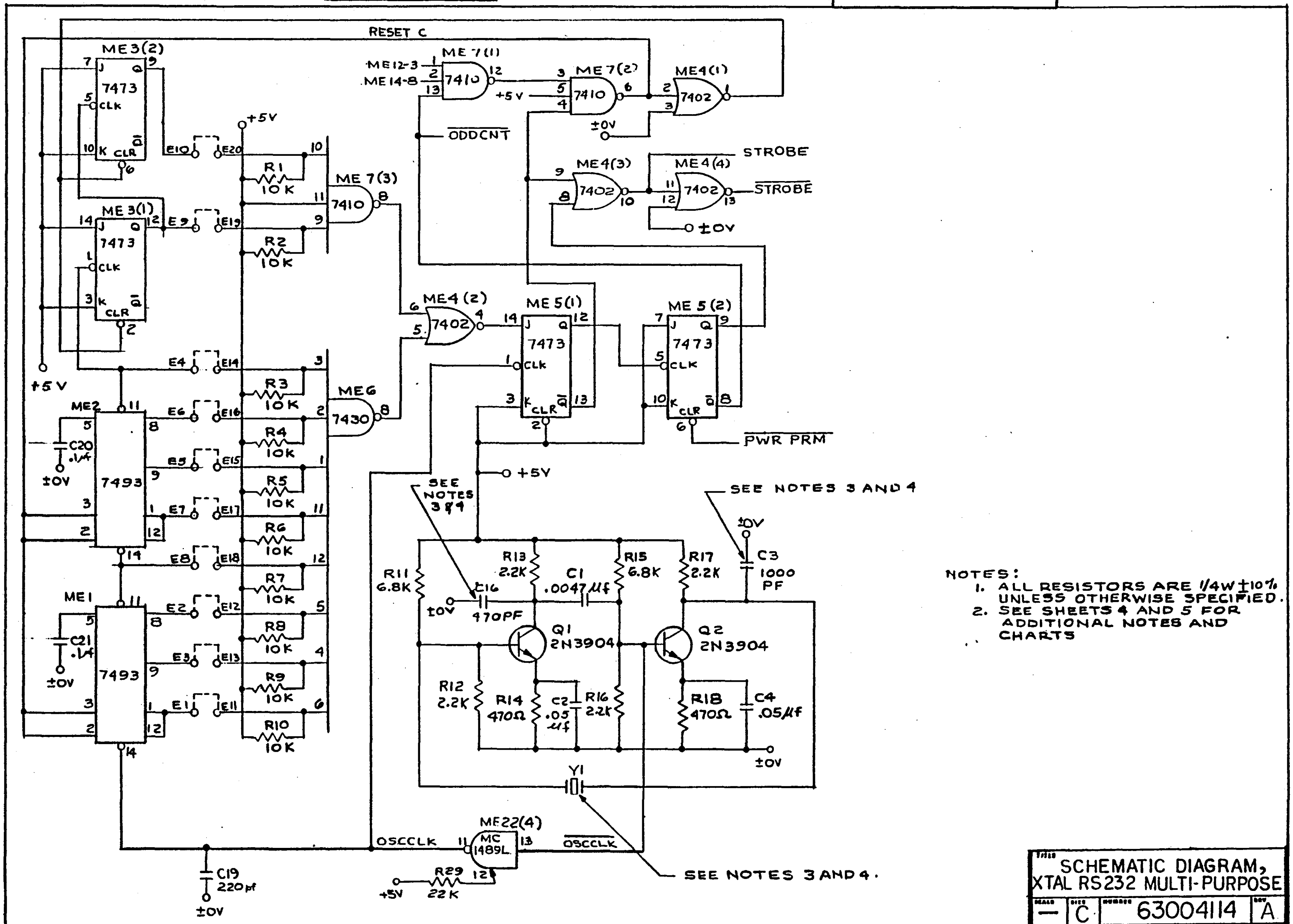
The 200 millisecond intervals developed by one-shots ME19(1) and ME19(2), ensure that a maximum reverse channel rate of 5 baud will not be exceeded.

8. SCHEMATICS AND ASSEMBLY DRAWING

This section contains the following drawings:

Figure	
7	Schematic Diagram (Sheet 1)
8	Schematic Diagram (Sheet 2)
9	Schematic Diagram (Sheet 3)
10	Schematic Diagram (Sheet 4)
11	Schematic Diagram (Sheet 5)
12	Electronics Cavity Assembly
13	Component Board Assembly (Sheet 1)
14	Component Board Assembly (Sheet 2)
15	Cable Assembly (W4)

Refer to the beginning of this section for possible changes not yet incorporated on this page.



SHEET 6 COVER SHEET

SHEET 1 OF6

Figure 7. Schematic Diagram (Sheet 1)

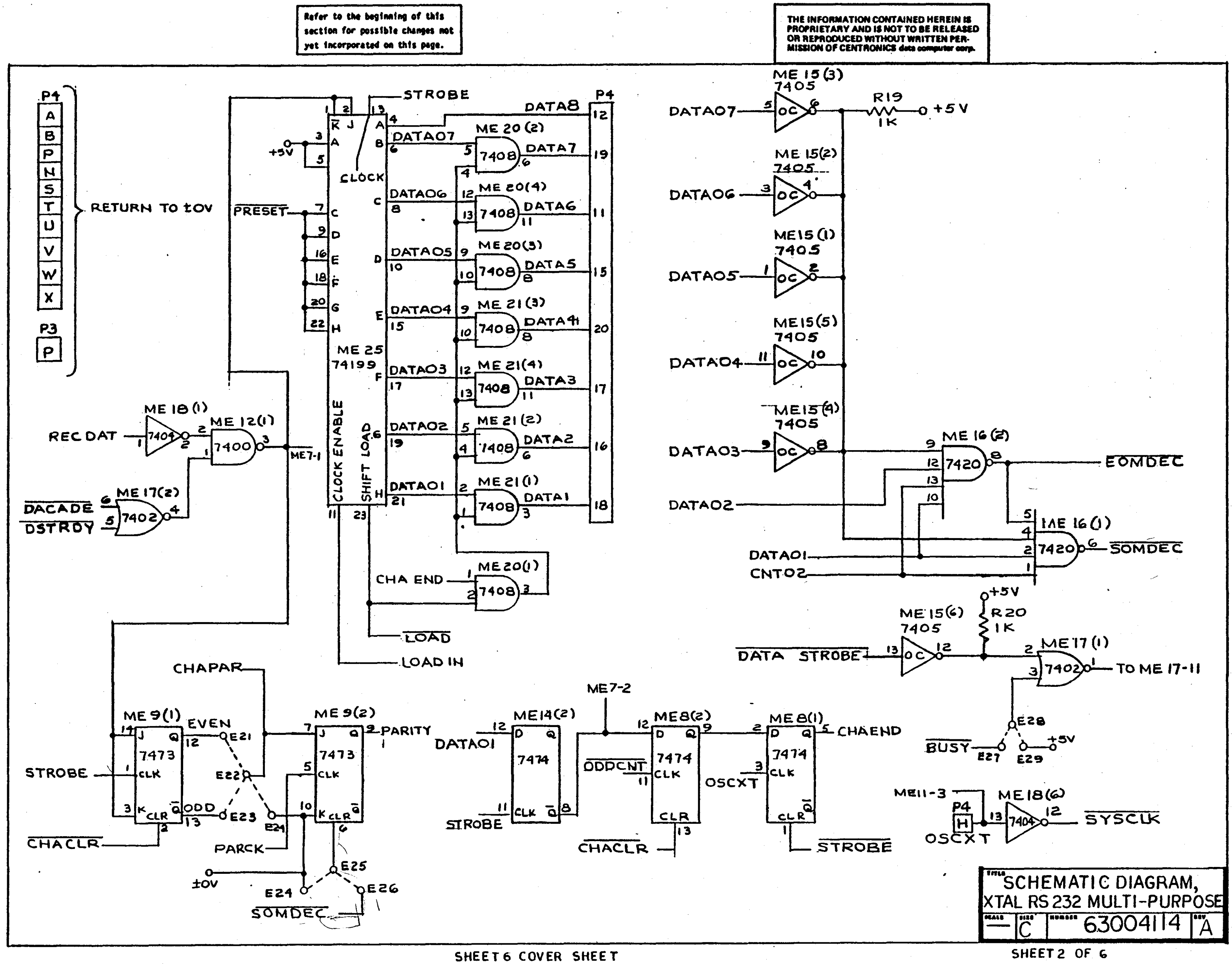
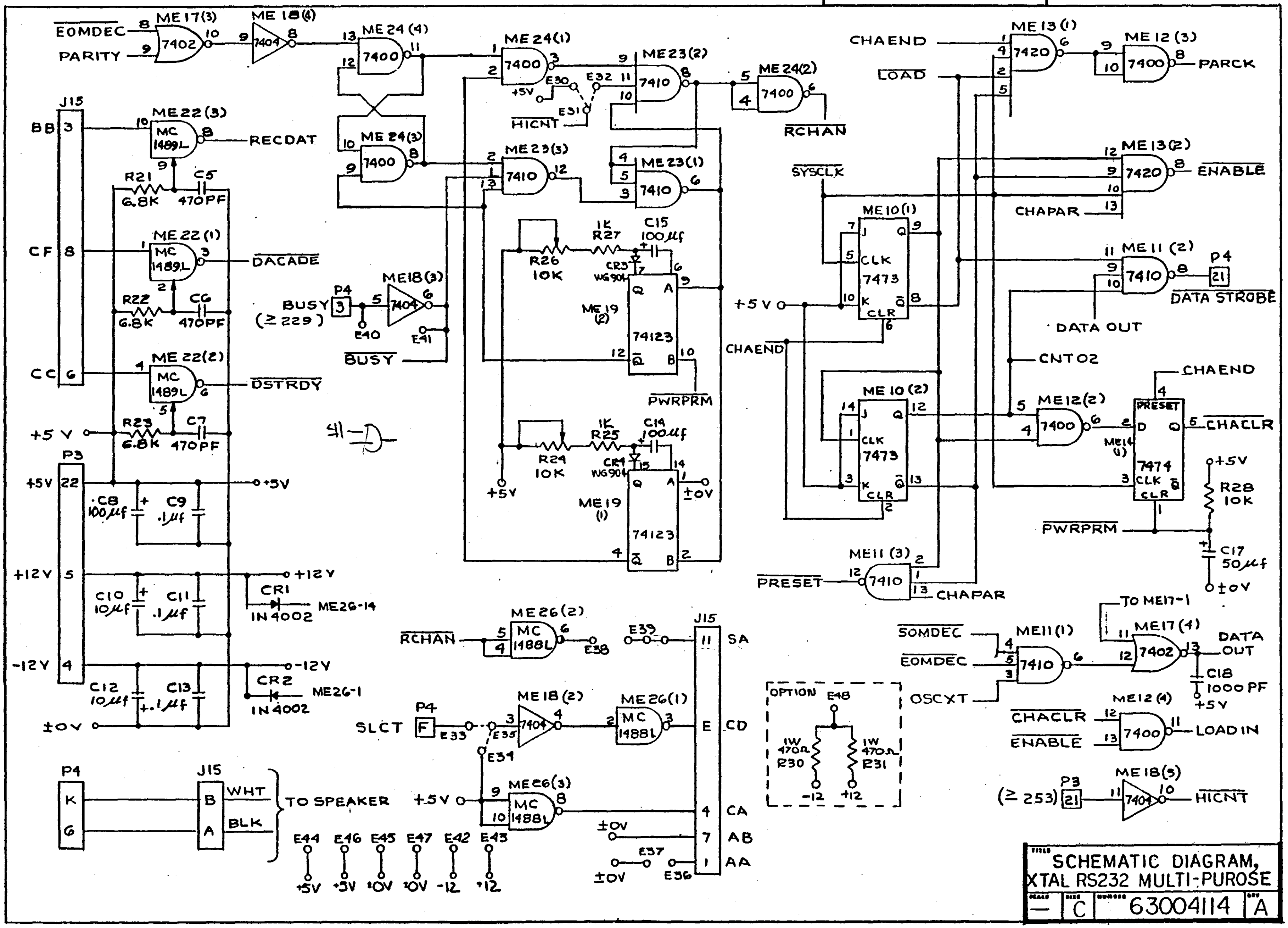


Figure 8. Schematic Diagram
(Sheet 2)

Rev. A

Refer to the beginning of this section for possible changes not yet incorporated on this page.



SHEET 6 COVER SHEET

SHEET 3 OF 6

Figure 9. Schematic Diagram (Sheet 3)

Rev. A

Refer to the beginning of this section for possible changes not yet incorporated on this page.

TABLE A

BAUD RATE	JUMPERS FROM	JUMPERS TO	XTAL	C3	C16	REMARKS
110	E1	E11	.2MHZ	.001µf	470PF	SEE NOTE 3
	E3	E13				
	E8	E18				
	E4	E14				
	E9	E19				
	E10	E20				
150	E1	E11	.2MHZ	.001µf	470PF	SEE NOTE 3
	E8	E18				
	E7	E17				
	E4	E14				
	E10	E20				
300	E1	E11	2MHZ	.001µf	470PF	SEE NOTE 3
	E3	E13				
	E8	E18				
	E6	E16				
	E9	E19				
600	E10	E20	1MHZ	N/A	N/A	SEE NOTE 4
	E9	E19				
	E5	E15				
	E7	E17				
	E8	E18				
	E2	E12				
	E3	E13				
	E1	E11				
1050	E9	E19	1MHZ	N/A	N/A	SEE NOTE 4
	E4	E14				
	E6	E16				
	E7	E17				
	E8	E18				
	E3	E13				
	E1	E11				
1200	E9	E19	1MHZ	N/A	N/A	SEE NOTE 4
	E4	E14				
	E7	E17				
	E8	E18				
	E2	E12				
	E3	E13				
	E1	E11				
1760	E9	E19	1MHZ	N/A	N/A	SEE NOTE 4
	E7	E17				
	E8	E18				
	E3	E13				
1800	E9	E19	1MHZ	N/A	N/A	SEE NOTE 4
	E7	E17				
	E2	E12				
2400	E4	E14	1MHZ	N/A	N/A	SEE NOTE 4
	E6	E16				
	E8	E18				
	E2	E12				
	E3	E13				
3600	E4	E14	1MHZ	N/A	N/A	SEE NOTE 4
	E8	E18				
	E1	E11				
4800	E6	E16	1MHZ	N/A	N/A	SEE NOTE 4
	E5	E15				
	E2	E12				
	E3	E13				
6800	E6	E16	1MHZ	N/A	N/A	SEE NOTE 4
	E8	E18				
7200	E6	E16	1MHZ	N/A	N/A	SEE NOTE 4
	E2	E12				
9000	E5	E15	1MHZ	N/A	N/A	SEE NOTE 4
	E7	E17				
	E2	E12				
	E3	E13				
9600	E5	E15	1MHZ	N/A	N/A	SEE NOTE 4
	E7	E17				
	E3	E13				

NOTES (CONT.)
SEE SHEET 1 FOR NOTES 1 AND 2.
3. TABLES B AND C WILL BE USED TO CONFIGURE BAUD RATES BELOW 600 BAUD. A .2 MHZ CRYSTAL WILL BE STANDARD WITH C3 AND C16 BEING USED.
4. TABLES D AND E WILL BE USED TO CONFIGURE BAUD RATES 600 BAUD TO 9600 BAUD. A 1MHZ CRYSTAL WILL BE STANDARD. C3 AND C16 WILL NOT BE USED.

TABLE B (SEE NOTE 3)

E1	5µs
E3	10µs
E2	20µs
E8	40µs
E7	80µs
E5	160µs
E6	320µs
E4	640µs
E9	1280µs
E10	2560µs

TABLE C (SEE NOTE 3)

TO CONFIGURE JUMPERS

$\frac{1}{\text{BAUD RATE}} \div 2 - 10\mu s = \text{DECODE}$

JUMPER TO GET APPROPRIATE SUM USING TABLE B

TABLE D (SEE NOTE 4)

E1	1µs
E3	2µs
E2	4µs
E8	8µs
E7	16µs
E5	32µs
E6	64µs
E4	128µs
E9	256µs
E10	512µs

TABLE E (SEE NOTE 4)

TO CONFIGURE JUMPERS

$\frac{1}{\text{BAUD RATE}} \div 2 - 2\mu s = \text{DECODE}$

JUMPER TO GET APPROPRIATE SUM USING TABLE D

TITLE SCHEMATIC DIAGRAM, XTAL RS 232 MULTI-PURPOSE
SCALE — SIZE C NUMBER 63004114 REV A

SHEET 6 COVER SHEET

SHEET 4 OF 6

Figure 10. Schematic Diagram (Sheet 4)

Refer to the beginning of this section for possible changes not yet incorporated on this page.

TABLE II

OPTION	JUMPER FROM	TO	FROM	TO	FROM	TO	FROM	TO	SPARE CHIPS NO.1 OR 2	SIGNAL IDENTIFICATION
A	E22	E21	E25	E26						EVEN PARITY (NORMAL)
B	E22	E23	E25	E26						ODD PARITY (NORMAL)
C	E22	E24	E25	E24						PARITY DISABLE (DISABLE PRESETTING OF @ SIGN)
D	E22	E21	E25	E24						EVEN PARITY @ ONLY (DISABLE PARITY BUT PRINT @ PER CHARACTER)
E	E22	E23	E25	E24						ODD PARITY @ ONLY (DISABLE PARITY BUT PRINT @ PER CHARACTER)
F	E28	E27								BUSY ENABLE (NORMAL)
G	E28	E29								BUSY DISABLE (RING BUFFER)
H	E32	E31								HICNT ENABLE (RING BUFFER)
I	E32	E30								HICNT DISABLE (NORMAL) ENABLES REV. CH. WHEN HICNT IS NOT USED
J	E35	E33								SELECT IN (WHEN SELECTED CD IS HELD AT +12V)
K	E35	E34								SELECT OUT (CD IS ALWAYS HELD AT +12V) (RING BUFFER)
L	E36	E37								PROTECTIVE GROUND IN
M	—	—								PROTECTIVE GROUND FLOATING
N	E39	E38								REVERSE CHANNEL NORMAL OUTPUT
O	E40	E35								CD (CONTROLLED BY BUSY NORMALLY -12V, WHEN ACTIVE +12V)
P	E41	E35								CD (CONTROLLED BY BUSY NORMALLY +12V, WHEN ACTIVE -12V)

SEE NOTE 5

NOTES (CONT.)
SEE SHEETS 1 AND 4 FOR NOTES 1-4
5. "CD" IS DATA TERMINAL READY.
6. "E" POINT USAGE NOT SPECIFIED INDICATES THEY ARE NOT USED.

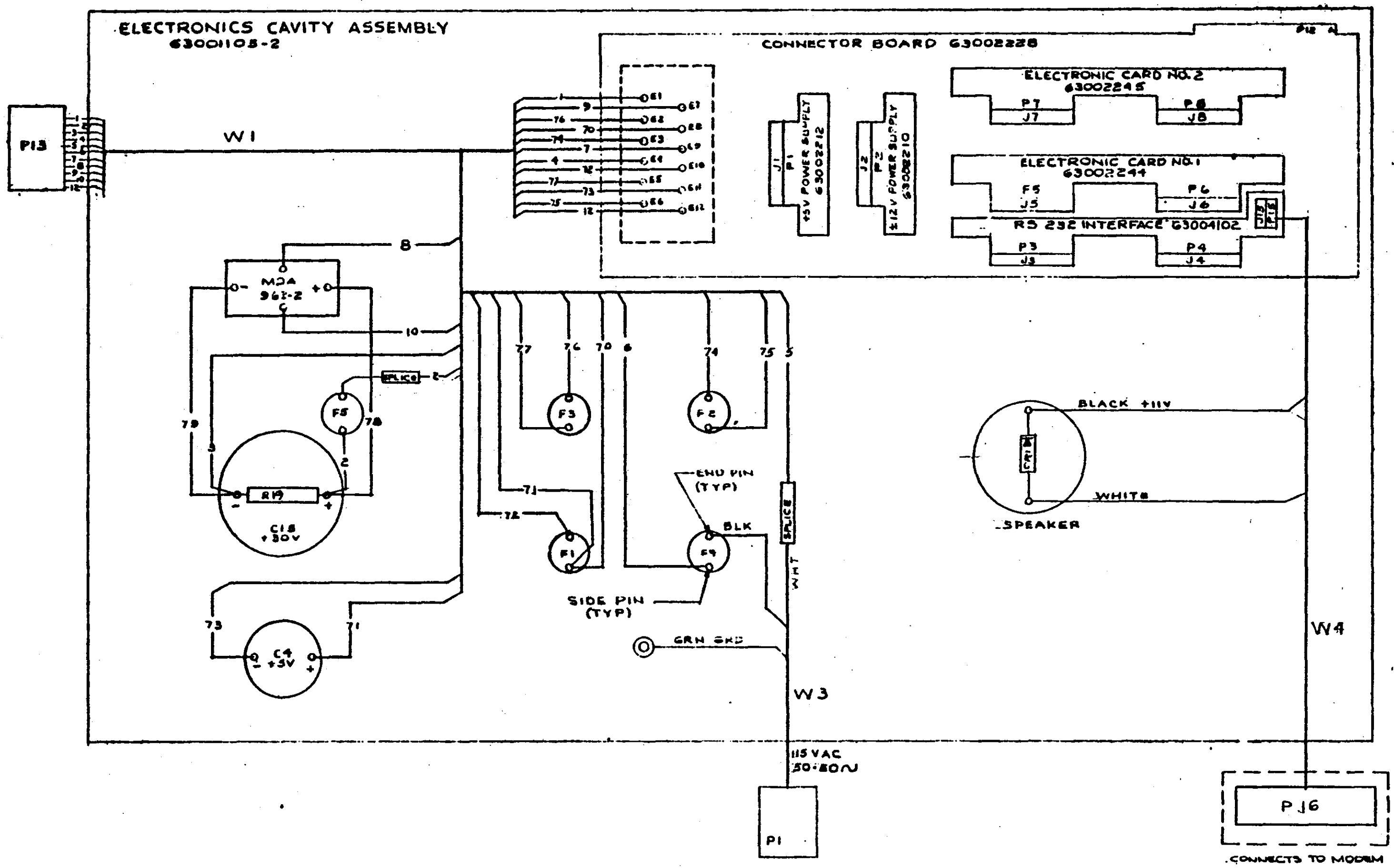
TITLE: SCHEMATIC DIAGRAM, XTAL RS232 MULTI-PURPOSE			
SCALE: —	SIZE: C	NUMBER: 63004114	REV: A

SHEET 6 COVER SHEET

SHEET 5 OF 6

Figure 11. Schematic Diagram (Sheet 5)

Refer to the beginning of this section for possible changes not yet incorporated on this page.

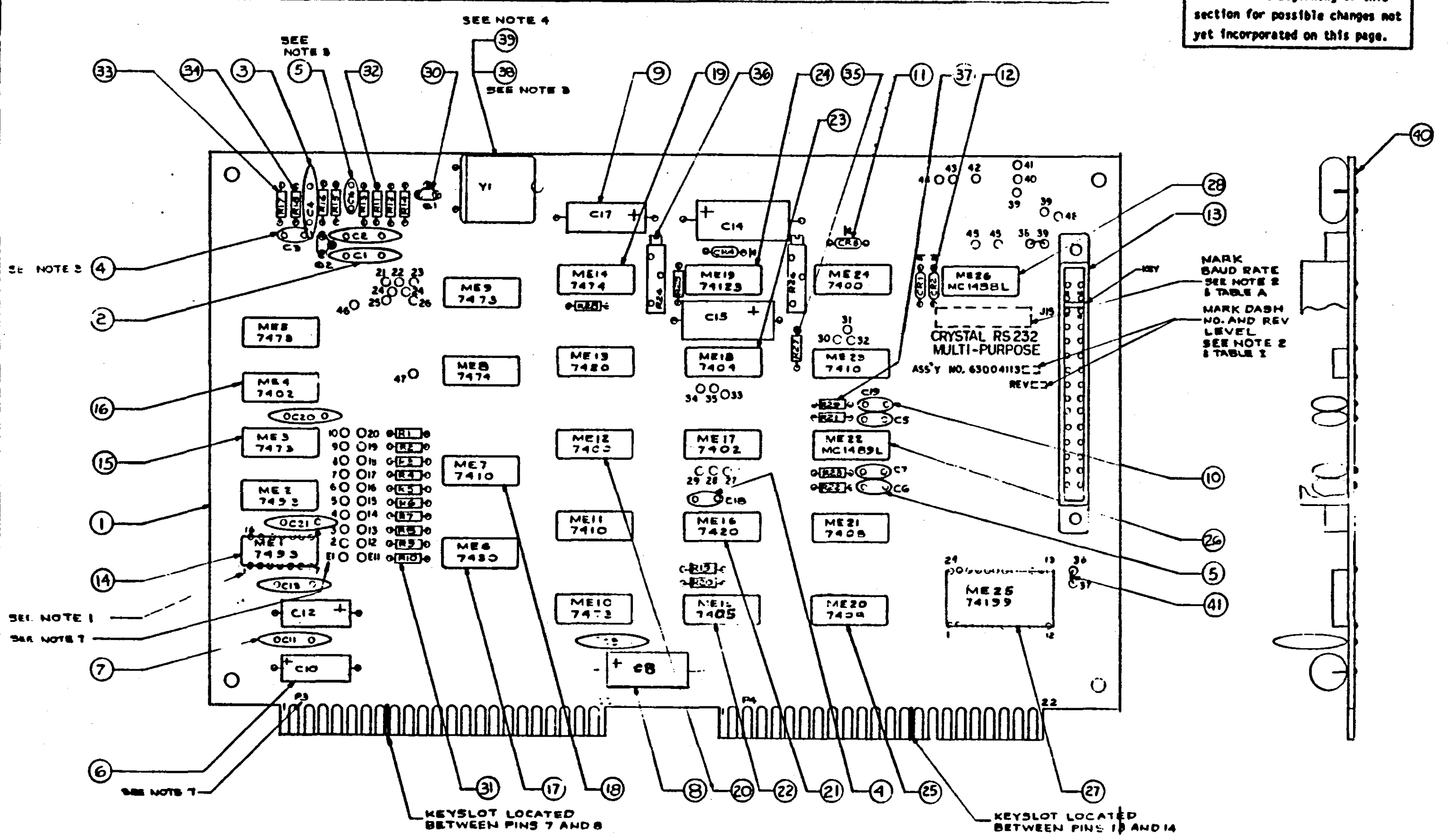


REFERENCE DRAWINGS:
SCHEMATIC DIAGRAM - C63002274
HARNESS ASSEMBLY (W1) D63002253-2
CABLE ASSEMBLY (W4) D63004103
POWER CABLE ASSEMBLY (W3) C63002258

Figure 12. Electronics Cavity Assembly (101/101A)

Refer to the beginning of this section for possible changes not yet incorporated on this page.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED TO PRODUCTION WITHOUT ECO		



NOTES:
1. ALL INTEGRATED CIRCUITS ARE TYPICALLY MOUNTED.
2. MARK 1/8 HIGH BLACK CHARACTERS AND LOCATE APPROX AS SHOWN.

SEE SHEET 2 FOR NOTES 3 THRU 6

7. THE LETTER "E" AHEAD OF 1 & 11 AND P3 & P4 ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON BOARD.

TABLE I

DASH NO.	JUMPERS FROM TABLE II	REMARKS
-1	A,F,I,J,L,N	STANDARD EVEN PARITY
-2	B,F,I,J,L,N	STANDARD ODD PARITY
-3	A,G,H,K,L,N	RING BUFFER EVEN
-4	B,G,H,K,L,N	RING BUFFER ODD
-5	D,F,I,L,N,P	REF 53

SEE ALSO TABLES A THRU E

REFERENCE DRAWINGS:
SCHEMATIC DIAG. 63004114
ARTWORK MASTER 63004012 REV-
LIST OF MATERIAL LM63004113

CENTRONICS

COMPONENT BOARD ASSEMBLY XTAL RS 232 MULTI-PURPOSE

E 63004113 A

Figure 13. Component Board Assembly (Sheet 1)

Refer to the beginning of this section for possible changes not yet incorporated on this page.

LIST OF MATERIAL FOR COMPONENT BOARD ASSEMBLY
(Reference: Figure 13)

Item	Symbol	Part Number	Nomenclature	Quantity
1		63004013-1	Component Board	1
2	C1	21472003	Capacitor, .0047 uf	1
3	C2, C4	21503003	Capacitor, .05 uf	2
4	C3, C18	21102000	Capacitor, 1000 PF	2
5	C5, C6	21471000	Capacitor, 470 PF	4
-	C7, C16	21471000	Capacitor, 470 PF	-
6	C10, C12	22106002	Capacitor, 10 uf	2
7	C9, C11	21104001	Capacitor, .1 uf	5
-	C13, C20	21104001	Capacitor, .1 uf	-
-	C21	21104001	Capacitor, .1 uf	-
8	C8, C14	22107002	Capacitor, 100 uf	3
-	C15	22107002	Capacitor, 100 uf	-
9	C17	22506002	Capacitor, 50 uf	1
10	C19	21221000	Capacitor, 220 PF	1
11	CR3, CR4	38100904	Diode, WG 904	2
12	CR1, CR2	38040020	Diode, IN 4002	2
13	J15	31230019	Connector, 225-21521-110	1
14	ME1, ME2	35474930	Integrated Circuit 7493	2
15	ME3, ME5	35474730	Integrated Circuit 7473	4
-	ME9, ME10	35474730	Integrated Circuit 7473	-
16	ME4, ME17	35474020	Integrated Circuit 7403	2
17	ME6	35474300	Integrated Circuit 7430	1
18	ME7, ME11	35474100	Integrated Circuit 7410	3
-	ME23	35474100	Integrated Circuit 7410	-
19	ME8, ME14	35474740	Integrated Circuit 7474	2
20	ME12, ME24	35474000	Integrated Circuit 7400	2
21	ME13, ME16	35474200	Integrated Circuit 7420	2
22	ME15	35474050	Integrated Circuit 7405	1
23	ME18	35474040	Integrated Circuit 7404	1
24	ME19	35474123	Integrated Circuit 74123	1
25	ME20, ME21	35474080	Integrated Circuit 7408	2
26	ME22	35214891	Integrated Circuit MC1489L	1
27	ME25	35474199	Integrated Circuit 74199	1
28	ME26	35214881	Integrated Circuit MCH88L	1
29				
30	Q1, Q2	38239040	Transistor, 2N3904	2
31	R1 thru R10	41103926	Resistor, 10K, ¼W, ±10%	11
-	R28	41103926	Resistor, 10K, ¼W, ±10%	-
32	R11, R15	41682926	Resistor, 6.8K, ¼W, ±10%	5
-	R21, R22	41682926	Resistor, 6.8K, ¼W, ±10%	-
-	R23,	41682926	Resistor, 6.8K, ¼W, ±10%	-
33	R12, R13	41222926	Resistor, 2.2K, ¼W, ±10%	3
-	R16, R17	41222926	Resistor, 2.2K, ¼W, ±10%	-
34	R14, R18	41471926	Resistor, 470Ω , ¼W, ±10%	2
35	R19, R20	41102926	Resistor, 1K, ¼W, ±10%	4
-	R25, R27	41102926	Resistor, 1K, ¼W, ±10%	-
36	R24, R26	46103910	Resistor, ±10% POT	2
37	R29	41223926	Resistor 22K, ¼W, ±10%	1
38	Y1	37816544-1	Crystal, .2MHz	1
39	Y1	37816544-2	Crystal, 1MHz	1
40		30070000	Solder, 60/40	AR
41		39610000-5	Wire, Bus No. 22AWG, Solid	AR
42	R12	41152926	Resistor, 1.5K, ¼W, ±10%	AR

Refer to the beginning of this section for possible changes not yet incorporated on this page.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED TO PRODUCTION WITHOUT ECO	8 NOV 78	

TABLE A

BAUD RATE	JUMPERS FROM	JUMPERS TO	XTAL	C3	C16	REMARKS
110	E1	E11	.2 MHZ	.001µf	470 PF	SEE NOTE 3
	E3	E13	ITEM 38	ITEM 4	ITEM 5	
	E8	E18				
	E4	E14				
	E9	E19				
	E10	E20				
150	E1	E11	.2 MHZ	.001µf	470PF	SEE NOTE 3
	E8	E18	ITEM 38	ITEM 4	ITEM 5	
	E7	E17				
	E4	E14				
	E10	E20				
200	E1	E11	.2 MHZ	.001µf	470 PF	SEE NOTE 3
	E3	E13	ITEM 38	ITEM 4	ITEM 5	
	E8	E18				
	E6	E16				
	E9	E19				
600	E10	E20	1 MHZ	N/A	N/A	SEE NOTE 4
	E9	E19	ITEM 39			
	E5	E15				
	E7	E17				
	E8	E18				
	E2	E12				
	E3	E13				
	E1	E11				
1050	E9	E19	1 MHZ	N/A	N/A	SEE NOTE 4
	E4	E14	ITEM 39			
	E6	E16				
	E7	E17				
	E8	E18				
	E3	E3				
	E1	E11				
1200	E9	E19	1 MHZ	N/A	N/A	SEE NOTE 4
	E4	E14	ITEM 39			
	E7	E17				
	E8	E18				
	E2	E12				
	E3	E13				
	E1	E11				
1760	E9	E19	1 MHZ	N/A	N/A	SEE NOTE 4
	E7	E17	ITEM 39			
	E8	E18				
	E3	E13				
1500	E9	E19	1 MHZ	N/A	N/A	SEE NOTE 4
	E7	E17	ITEM 39			
	E2	E12				
2400	E4	E14	1 MHZ	N/A	N/A	SEE NOTE 4
	E6	E16	ITEM 39			
	E8	E18				
	E2	E12				
	E3	E13				
3600	E4	E14	1 MHZ	N/A	N/A	SEE NOTE 4
	E8	E18	ITEM 39			
	E1	E11				
4800	E6	E16	1 MHZ	N/A	N/A	SEE NOTE 4
	E5	E15	ITEM 39			
	E2	E12				
	E3	E13				
6800	E6	E16	1 MHZ	N/A	N/A	SEE NOTE 4
	E8	E18	ITEM 39			
7200	E6	E16	1 MHZ	N/A	N/A	SEE NOTE 4
	E2	E12	ITEM 39			
9000	E5	E15	1 MHZ	N/A	N/A	SEE NOTE 4
	E7	E17	ITEM 39			
	E2	E12				
	E3	E13				
9600	E5	E15	1 MHZ	N/A	N/A	SEE NOTE 4
	E7	E17	ITEM 39			
	E3	E13				

TABLE B (SEE NOTE 3)
E1 — 5µs
E3 — 10µs
E2 — 20µs
E8 — 40µs
E7 — 80µs
E5 — 160µs
E6 — 320µs
E4 — 640µs
E9 — 1280µs
E10 — 2560µs

TABLE C (SEE NOTE 3)
TO CONFIGURE JUMPERS
$\frac{1}{\text{BAUD RATE}} \div 2 - 10\mu s = \text{DECODE}$
JUMPER TO GET APPROPRIATE SUM USING TABLE B

TABLE D (SEE NOTE 4)
E1 — 1µs
E3 — 2µs
E2 — 4µs
E8 — 8µs
E7 — 16µs
E5 — 32µs
E6 — 64µs
E4 — 128µs
E9 — 256µs
E10 — 512µs

TABLE E (SEE NOTE 4)
TO CONFIGURE JUMPERS
$\frac{1}{\text{BAUD RATE}} \div 2 - 2\mu s = \text{DECODE}$
JUMPER TO GET APPROPRIATE SUM USING TABLE D

TABLE II

OPTION	JUMPER (SEE NOTE 6) FROM	TO	FROM	TO	FROM	TO	FROM	TO	SPARE CHIP NO. 1 OR 2	SIGNAL IDENTIFICATION
A	E22	E21	E25	E26						EVEN PARITY (NORMAL)
B	E22	E23	E23	E26						ODD PARITY (NORMAL)
C	E22	E24	E25	E24						PARITY DISABLE (DISABLE PRESETTING OF @ SIGN)
D	E22	E21	E25	E24						EVEN PARITY @ ONLY (DISABLE PARITY BUT PRINT @ PER CHARACTER)
E	E22	E23	E25	E24						ODD PARITY @ ONLY (DISABLE PARITY BUT PRINT @ PER CHARACTER)
F	E28	E27								BUSY ENABLE (NORMAL)
G	E28	E29								BUSY DISABLE (RING BUFFER)
H	E32	E31								HICNT ENABLE (RING BUFFER)
I	E32	E30								HICNT DISABLE (NORMAL) ENABLES REV. CH. WHEN HICNT IS NOT USED
J	E35	E33								SELECT IN (WHEN SELECTED CD IS HELD AT +12V)
K	E35	E34								SELECT OUT (CD IS ALWAYS HELD AT +12V) (RING BUFFER)
L	E36	E37								PROTECTIVE GROUND IN
M	—	—								PROTECTIVE GROUND FLOATING
N	E39	E38								REVERSE CHANNEL NORMAL OUTPUT
O	E40	E33								CD (CONTROLLED BY BUSY NORMALLY −12V, WHEN ACTIVE +12V)
P	E41	E38								CD (CONTROLLED BY BUSY NORMALLY +12V, WHEN ACTIVE −12V)

SEE NOTE 5

NOTES (CONT.)

SEE SHEET 1 FOR NOTES 1, 2 & 7

3. TABLES B AND C WILL BE USED TO CONFIGURE BAUD RATE BELOW 600 BAUD. A .2MHZ. XTAL WILL BE STANDARD WITH C3 AND C16 BEING USED.
4. TABLES D AND E WILL BE USED TO CONFIGURE BAUD RATES 600 BAUD TO 9600 BAUD. A 1MHZ XTAL WILL BE STANDARD. C3 AND C16 WILL NOT BE USED.
5. "CD" IS DATA TERMINAL READY.
6. "E" POINT USAGE NOT SPECIFIED INDICATES THEY ARE NOT USED.

CENTRONICS data computer corp.

COMPONENT BOARD ASSEMBLY XTAL RS 232 MULTI-PURPOSE

E 63004113 A

3004

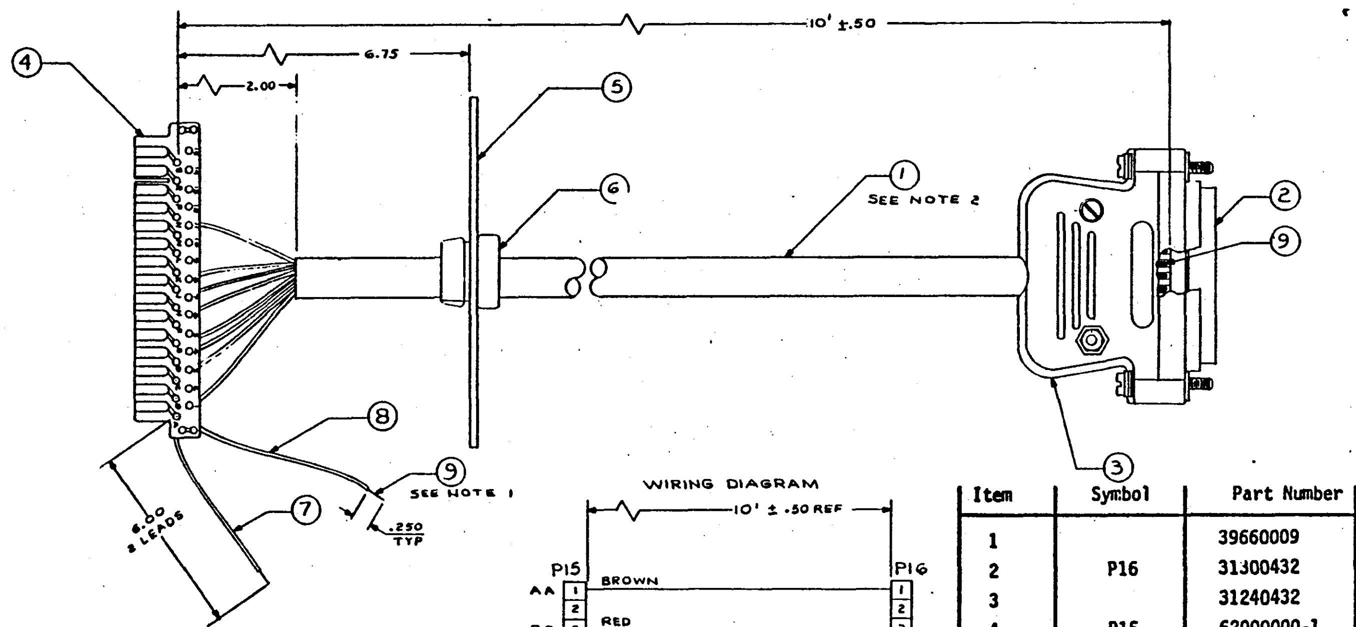
SHEET 2 OF 2

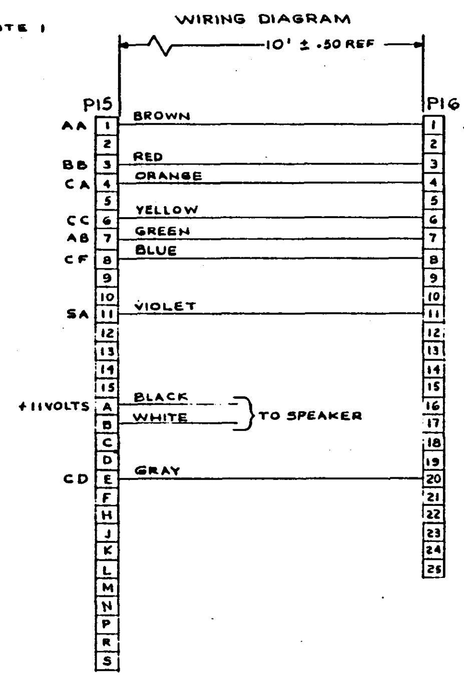
DO NOT SCALE PRINT

Figure 14. Component Board Assembly (Sheet 2)

Refer to the beginning of this section for possible changes not yet incorporated on this page.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	REDUC "A" SIZE LM AND RELEASED TO PRODUCTION WITHOUT ECO		





Item	Symbol	Part Number	Nomenclature	Quantity
1		39660009	Cable, I/O Conductor	10 ft.
2	P16	31300432	Connector, 25 Pin	1
3		31240432	Dataphone Hood	1
4	P15	62000000-1	Connector, Finger Board	1
5		63004100-1	Plate, Connector	1
6		36150000	Strain Relief Bushing	1
7		39640000-4	Wire, Hook-Up, 22 AWG, WHT	6 in.
8		39640000-4	Wire, Hook-Up, 22 AWG, BLK	6 in.
9		30700000	Solder	AR

NOTES:

1. STRIP ALL ENDS .250 AND TIN BEFORE ASSEMBLY.
2. CUT JACKET INSULATION BACK 1.500 INCHES BEFORE ASSEMBLING WITH CONNECTOR, ITEM 2.
3. CUT OFF BLACK AND WHITE WIRES TO JACKET INSULATION ON BOTH ENDS BEFORE ASSEMBLY.

(-1) FOR LIST OF MATERIAL SEE LM63004103-1

UNLESS OTHERWISE SPECIFIED...
1. CAPACITANCE IN μf
2. RESISTANCE IN Ω
3. DIMENSIONS IN INCHES.
4. TOLERANCES.
FRAC ± — .XX ± .25
.XXX ± .06 ANGLE ± —

63011128-2 3011
63001105-2 3000
NEXT ASSY / USED ON

DO NOT SCALE PRINT

centronics data computer corp.

CABLE ASSEMBLY RS 232 INTERFACE (W4)

D 63004103 A

Figure 15. Cable Assembly (W4)

9. INTERFACE CONNECTOR

Fingerboard Connector (P15)	Data Set Connector (P16)	Signal Name	Source	Signal Description
Pin 1	Pin 1	AA	Printer	Protective Ground
Pin 3	Pin 3	BB	Data Set	Received Data: A -V* is a Mark and a +V is a Space. When released, this line should be in the Mark condition.
Pin 4	Pin 4	CA	Printer	Request to Send: This line is held at -V.
Pin 6	Pin 6	CC	Data Set	Data Set Ready: A +V on this line allows the printer interface to accept data from the data set.
Pin 7	Pin 7	AB	Printer	Signal Ground
Pin 8	Pin 8	CF	Data Set	Data Carrier Detector: A +V on this line allows the printer interface to accept data from the data set.
Pin 11	Pin 11	SA	Printer	Reverse Channel: Used for transmitting printer status to the data set. It is normally in a Mark (-V) condition. After a line of data is received, this line goes to a Space condition (+V) until the printer is able to receive data again.
Pin A	-	-	Printer	To Speaker
Pin B	-	-	Printer	To Speaker
Pin E	Pin 20	CD	Printer	Data Terminal Ready: A +V on this line indicates that the printer is selected.
	All other connector pins are open.			

*+V indicates a voltage greater than +3 Volts,
-V indicates a voltage less than -3 Volts.

10. GLOSSARY

Mnemonic	Source*	Description
AA	J15-1	Protective ground
AB	J15-7	Signal ground
BB	J15-3	Received Data line from data set.
BUSY	P4-3	Status line from the printer indicating that the printer is busy performing an operation.
CA	ME26-8	Request to Send status line to the data set. Held low when printer is operational.
CC	J15-6	Data Set Ready status line from the data set. A high allows the interface to accept data.
CD	ME26(3)	Data Terminal Ready status line to the data set. A high indicates that the interface is prepared to accept data.
CF	J15-8	Data Carrier Detect from data set. A high allows the interface to receive data.
$\overline{\text{CHACLR}}$	ME14-5	Character Clear - Indicates the end of a parallel loading sequence to the printer.
CHAEND	ME8-5	Character - A 40 usec pulse indicating the end of a character.
CNT02	ME10-12	Timing signal used during the parallel loading operation and EOM or SOM decoding.
$\overline{\text{DACADE}}$	ME22-3	Data Carrier Detect - A DC level indicating the data carrier signal is present at the data set.
DATA01-08	ME25	Eight output data lines from the shift register.
DATA1-8	ME20, ME21	Eight gated data lines to the output connector.
DATA OUT	ME17-13	Signal used to inhibit or enable data strobe.
$\overline{\text{DATA STROBE}}$	ME11-8	Pulse used to clock data into the printer (5 us)
$\overline{\text{DSTRDY}}$	ME22-6	Data Set Ready - DC level indicating the data set is in a ready condition.
$\overline{\text{ENABLE}}$	ME13-8	Pulse used to generate a clock for the loading of an @ into the shift register in case of a character parity error.
$\overline{\text{EOMDEC}}$	ME16-8	EOM Decode - Decoded signal indicating the end of a transmitted message.
$\overline{\text{HICNT}}$	ME18-10	High Count - Buffered signal 253 from Ring Buffer.
$\overline{\text{LOAD}}$	ME10-8	Enables the parallel inputs to the shift register.
LOAD IN	ME12-11	Clocks parallel data into shift register.

*ME26-8 signifies element ME26 pin 8

10. GLOSSARY (Con't)

Mnemonic	Source	Description
ODDCNT	ME5-8	Odd Count - Used to block every other decoded pulse and to clock the End of Character flip-flop.
OSCCLK	ME22-11	A .2MHz or 1MHz crystal controlled clock used to generate to strobe; Clocks the serial data into the shift register.
OSCXT	P4-H	External Oscillator - 100 KHz oscillator output from printer.
PARCK	ME12-8	Parity Check - A pulse used to load character parity (CHAPAR) into the PARITY flip-flop.
PARITY	ME9-9	A DC level used to indicate a parity error during the received message.
$\overline{\text{PRESET}}$	ME11-12	A pulse used to force an octal 100 (@ sign) at the parallel inputs to the shift register, if a parity error was detected in the last character.
$\overline{\text{PWRPRM}}$	C17	Power Prime - Level used to prime the interface electronics when power is first applied.
$\overline{\text{RCHAN}}$	ME24-6	Reverse Channel - A 200 usec (minimum) pulse used to indicate to the transmitting device, the status of the interface and of the received data.
$\overline{\text{RECDAT}}$	ME22-8	Received Data line (buffered).
RESETC	ME7-6	Reset Counter - Used to reset the baud counter that generates the strobe.
SA	ME26-6	Reverse Channel line to data set.
SLCT	P4-F	Select status line from the printer.
SOMDEC	ME16-6	SOM Decode - A decoded signal indicating the beginning of a transmitted message.
STROBE	ME4-10	A $1\mu S$ or $5\mu S$ pulse used to load the incoming serial data into the shift register.
$\overline{\text{STROBE}}$	ME4-13	A $1\mu S$ or 5 usec pulse used to clear the CHAEND flip-flop.
$\overline{\text{SYSCLK}}$	ME18-12	System Clock - A 100 KHz clock derived from OSCXT, used to control the data loading sequence to the printer.
229	P4-3	≥ 229 Characters - Status line from the ring buffer indicating that the buffer is approaching maximum capacity.
253	P3-21	≥ 253 Characters - Status line from the ring buffer indicating that the buffer is incapable of storing any more data.