CONTROL DATA CORPORATION

SPEC 77653332
CD 5
REV C
DATE March 1982

PRODUCT SPECIFICATION

FOR

FINCH™ DISK DRIVE

MODEL 9410-3F

MAGNETIC PERIPHERALS INC.
a subsidiary of
CONTROL DATA CORPORATION

CONTROL DATA CORPORATION

SPEC	77653332
CD	5
REV	C
DATE	March 1982
PAGE	1 of 56

PRODUCT SPECIFICATION

FOR

FINCH™ DISK DRIVE

MODEL 9410-3F

MAGNETIC PERIPHERALS INC.

a subsidiary of CONTROL DATA CORPORATION

COPYRIGHT © 1982
by MAGNETIC PERIPHERALS INC.
ALL RIGHTS RESERVED
Printed in the United States of America

This publication may contain application, high technology, or product specification data, or any combination thereof, is considered advance technical information by the producer, and is subject to change without prior notice.

PRODUCT SPECIFICATION - MODEL 9410 FINCH DISK DRIVE

TABLE OF CONTENTS

PRODUCT SPECIFICATION - MODEL 9410 FINCH DISK DRIVE

TABLE OF CONTENTS (contd.)

TABLE OF CONTENTS (contd.)

1.0 SCOPE

This specification describes the Control Data Corporation Model 9410 FINCH™ Disk Drive. This 8-inch member of the rigid disk family utilizes a digital interface and is available in 8,24 and 32 megabyte unformatted capacities. The basic configurations are: 9410-8-3F, 9410-24-3F and 9410-32-3F.

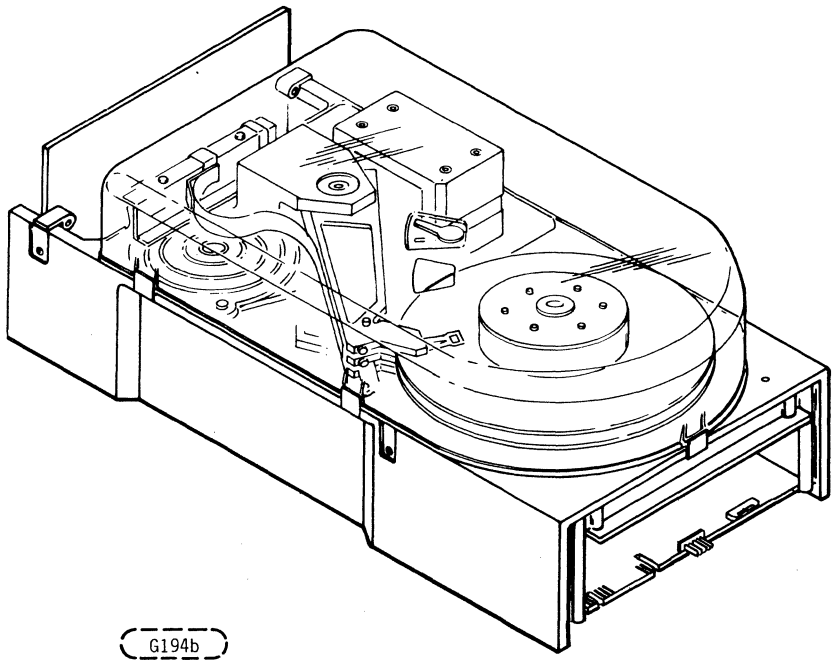


Figure 1. The 9410 (FINCH)

2.0 APPLICABLE DOCUMENTS

2.1 STANDARDS

The 9410 FINCH has been designed as a system peripheral to the highest standards of design and construction. The drive, however, must depend upon its host equipment to receive adequate power and environment in order to provide optimum performance and compliance with applicable industry and governmental regulations. Special attention must be given in the areas of safety, power distribution, shielding, audible noise control, and temperature regulation of the device to ensure specified performance and compliance with all applicable regulations.

The 9410 shall comply with CDC standards as noted in the appropriate sections of this specification.

In addition to the corporate standards, the 9410 shall comply with the requirements of UL 478 and CSA Standard C22.2 No. 154-1975.

The 9410 is a component and, as such, is not subject to standards imposed by FCC Docket 20780/FCC 80-148 Part 15 governing EMI of computing devices.

2.2 DOCUMENTATION

The following documentation is available for field support of the FINCH.

TBD	Hardware Maintenance Manual, Level 2
77653374	Application Note, Diagnostics for Model 9410 FINCH Disk Drive
77653472	Power Supply Product Specification
77653532	Hardware Maintenance Manual, Level 1
77653461	Application Note, Interfacing A 9406 Flexible Disk Drive with a 9410 FINCH Disk Drive

3.0 GENERAL DESCRIPTION

The 9410 FINCH is a member of a family of low-cost, high-performance, highly reliable, random access storage devices designed to meet the needs of the OEM marketplace.

The FINCH is designed to record and recover data on up to three eight-inch fixed disk media; it does not contain any removable media capability.

The FINCH digital interface is intended to utilize a single controller design capable of controlling both a 9410 and a Flexible Disk Drive (FDD).

The 9410 digital electrical interface consists of a 50-pin command interface and a 20-pin data interface. The 50-pin command interface is designed to allow daisy-chained or radial connections to 9410's and 9406-4 FDD;s. Thus, the 50-pin 9410 command interface contains functional and electrically compatible signals to a 9406-4; however, due to different step rates, access time, and data transfer rates, the timing relationships of the individual signals may vary. The 20-pin radial data interface is unique to the 9410 and is based on differential NRZ data plus clocks to meet electrical requirements for a 6.45 MHZ data rate.

The disk and actuator chamber is environmentally sealed. No outside air is drawn into the unit. Air is recirculated within the disk/actuator chamber and passes through the nonreplaceable absolute filter to ensure the maintenance of a contamination free disk/actuator environment.

Refer to Figure 2 for an exploded view of the FINCH. NEVER disassemble the FINCH. This exploded view is for information only. Servicing items in the upper sealed environmental enclosure (heads, media, actuator, etc.) requires special facilities. Only the printed circuit boards external to the sealted area can be replaced with no special facilities.

The FINCH utilizes a dedicated landing zone, thus eliminating the posibility of destorying data by not landing in the data zone area.

There is a rotory locking arm (Figure 2) that eliminates actuator movement during shipment or handling.

The FINCH will do an auto velocity adjust 12 sec after power up.

The FINCH applies a break to the shutter fan on power down. Disk rotation is stopped in <30 sec. Thus minimizing head to disk contact.

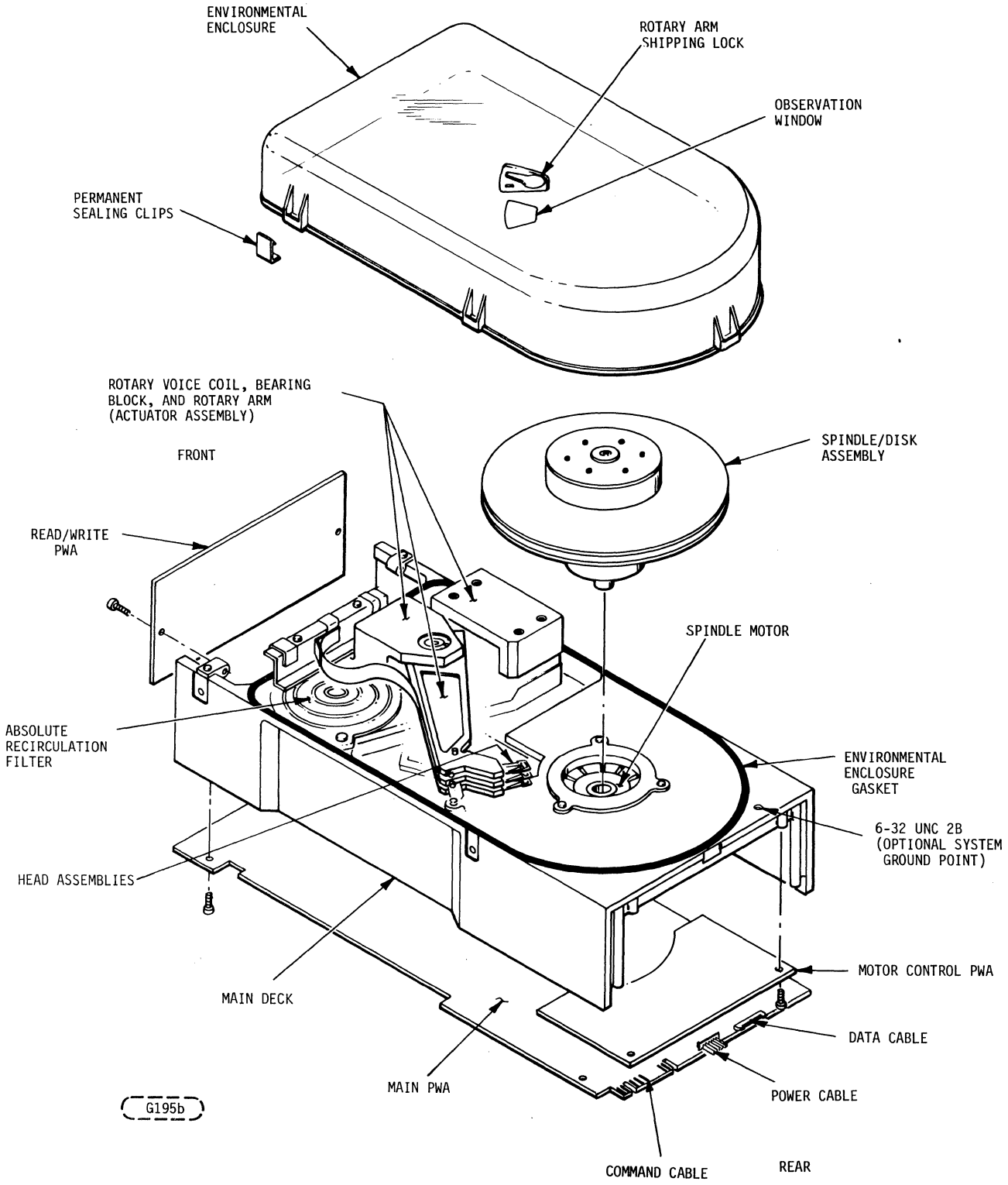


Figure 2. FINCH

4.0 FEATURES

4.1 STANDARD FEATURES

The FINCH has the following standard features:

- Full data recovery circuitry
- Sealed disk, head, and actuator chamber
- No preventive maintenance required
- LSI circuitry for high reliability
- Low audible noise for office environments
- Vertical (side) or horizontal (bottom) mounting
- Low power consumption
- Rotary voice coil actuator
- Operator and Installation Guide
- Terminators

4.2 OPTIONAL CONFIGURATION (FACTORY INSTALLED ONLY)

The following optional features are available for the FINCH:

- 8,24 or 32 megabyte capacity

5.0 ACCESSORIES

The following accessories are available for the FINCH and must be ordered separately:

- Shock mount kit
- Front panel kit
- Power supply - includes 5-foot DC power cable and a 10-foot AC power cable
- Operation installation and checkout manual Level-1
- Hardware maintenance manual Level-2
- Diagnostic Application Note
- MATE-N-Lok Power Adapter Kit

6.0 PERFORMANCE CHARACTERISTICS

Data Capacity (Unformatted)		
Bytes per Track	13,440 bytes	Note 1
Bytes per Surface	8,010,240 bytes	
Single Disk	8,010,240 bytes	
Double Disk	24,030,720 bytes	
Triple Disk	32,040,960 bytes	
Bits per inch	6,800	
Track Format		
Variable	User Defined	
Number of Byte Clocks Per Revolution	13,440	
Tracks per inch	554	
Recording Mode		
Interface	NRZ	
Disks	MFM	
Data Transfer Rate	6.45 Mb/s (806 kB/s)	
Data Interface	NRZ DATA + CLOCK	
Rotational Speed	3600 r/min ±1.5%	
Average Latency	8.33 ms	
Tracks Per Surface	605 (Note 2)	
Step Pulse Rate	50 kHz ±20% (20 µs between Step pulses)	
Single Track Seek Time	10 ms Max.	⚠1
Average Seek Time (Step Pulse Rate of 50 kHz ±20%)	50 ms	⚠1
Maximum Seek Time (605 Tracks) (Step Pulse Rate of 50 kHz ±20%)	100 ms	⚠1

Note 1: Based on 596 primary cylinders. Does not include spare tracks.

Note 2: See Media Characteristics, paragraph 9.0.

⚠1 Typ Single track seek time 8 ms

⚠1 Typ Average seek time 42 ms

⚠1 Typ Maximum seek time 84 ms

6.1 ACCESS TO DATA CHARACTERISTICS

6.1.1 Seek Time

Seek time is defined as the time required from the receipt of a seek or position command by the FINCH until the drive signals the controller that it is ready to perform another seek or read/write function on the new cylinder. Average seek time is determined by dividing the sum of the time for all possible movements by the total number of movements.

6.1.2 Spindle Speed and Latency

The spindle speed is 3600 ±1.5% r/min. The speed tolerance includes motor performance and motor control circuit tolerances, but does not include other variables which affect data transfer rates as seen at the interface.

The average latency time is 8.33 milliseconds, based on a nominal disk speed of 3600 r/min. The maximum latency time is 16.75 milliseconds based on a minimum disk speed of 3546 r/min.

6.1.3 Read to Write Recovery Time

Assuming a read operation is in progress, the required minimum time interval between the end of read gate and the initiation of write gate is 5 bit time periods.

6.2 DATA CAPACITY

The total unformatted data capacity of the 9410 is 8,010,240 bytes per data surface. This capacity does not include the spare data tracks.

6.3 READ DATA TRANSFER RATE

The nominal read serial data transfer rate is 6.45 Mbits per second. The range of transfer rate variations on a bit per second basis for read/write operations is 3% of the nominal. This range includes the effects of all factors including spindle speed variations and dynamic jitter on a byte to byte basis. Data on the interface is NRZ plus clock.

6.4 START/STOP TIME

The FINCH will become ready less than 60 seconds after application of DC power. Stop time will be less than 30 sec after removal of DC power.

There is no power control switch or indicator on the drive.

7.0 RELIABILITY SPECIFICATIONS

The following reliability specifications assume correct host/drive operational interface has been implemented, including all interface timings, power supply voltages, environmental conditions, and appropriate data-handling circuits in the host system.

Error Rates	
Soft Read Errors (Recoverable)	Less than 1 in 10^{10} bits transferred
Hard Read Errors (Unrecoverable)	Less than 1 in 10^{12} bits transferred
Seek Errors	Less than 1 in 10^{6} seeks
MTBF	First Year Production - 5000 hours minimum Second Year Production - 7500 hours minimum Third Year On - 10,000 hours minimum
Service Life	5 years or 30,000 hours
Preventive Maintenance	None required

7.1 ERROR RATES

The error rates stated in this specification assume the following:

a. That the 9410 is operated per this specification utilizing the CDC provided accessory power supply or its equivalent.

b. That a data format is employed fulfilling the requirements of the 9410 as outlined in Section 15.0.

c. That errors caused by media defects or host system failures are excluded from error rate computations. Refer to paragraph 9.0, Media Defect Recognition.

d. That power requirements as specified in paragraph 8.2 and system grounding requirements indicated in the installation instructions are met.

e. That all read/write operations are accomplished with the same physical orientation of the drive. (Refer to paragraph 8.5.1.)

7.1.1 Read Errors

Prior to the determination or measurement of read error rates:
a. The data which is to be used for a measurement of read error rates must be verified as being written correctly on the media.
b. All media defect induced errors must be excluded from error rate calculations.

A recoverable read error is one that can be reread correctly in 2 sets of 10 retries. After 10 retries, a recalibrate (RTZ) and seek to desired address must be accomplished. The soft read error rate for any read operation shall be less than one error in 10^{10} bits read.

An unrecoverable read error is one that cannot be read correctly after 2 sets of 10 retries. The hard read error rate for any read operation shall be less than one bit in 10^{12} bits read.

7.1.2 Environmental Interference

When operating at low effective data transfer rate, (that is, random access of sincle short records) the effective error rate may be expected to exceed the specified limits due to environmental interference. Excluding environmental interference, the recoverable read error rate shall be no more than one error in eight hours of operation.

When evaluating systems operation under conditions of EMI the performance of the 9410-3F FINCH within the system shall be considered acceptable if the device does not generate an unrecoverable error, or incur an unrecoverable condition.

An unrecoverable error, or condition, is defined as one which:
1. Is not detected and corrected by the device itself;
2. Or is not capable of being detected from the error or fault status provided through the device/system interface;
3. Or is not capable of being recovered by normal device or system recovery procedures without requiring operator intervention.

7.1.3 Write Errors

Write errors can occur as a result of the following: write data not being presented correctly, media defects, environmental interference, or equipment malfunction. As such, write errors are not predictable as a function of the number of bits passed.

If an unrecoverable write error occurs because of a FINCH equipment malfunction, the error is classified as a failure affecting MTBF. Unrecoverable write errors are those which cannot be corrected within four attempts at writing the record with a verify after each attempt, (excluding identified media defects).

7.1.4 Seek Errors

A seek error is defined as a condition where the drive fails to position the heads to the addressed track provided the correct stepping information has been presented to the FINCH. There shall be no more than one recoverable seek error in 10^6 physical seek operations. Unrecoverable seek errors are classified as failures for MTBF calculations.

7.2 RELIABILITY AND SERVICE

7.2.1 Mean Time Between Failure

Following an initial period of 200 hours, the Mean Time Between Failure shall exceed 5000 hours for units manufactured in the first year of production and 7500 hours for units manufactured in the second year. For units manufactured after the second year, the MTBF shall exceed 10,000 hours. The following equation defines MTBF:

$$\text{MTBF} = \frac{\text{Operating Hours}}{\text{No. of Equipment Failures}}$$

"Operating Hours" means total power on hours less any maintenance time. "Equipment Failure" means any stoppage or substandard performance of the equipment because of equipment malfunction, excluding stoppages or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, or other failure not caused by equipment. To establish a meaningful MTBF, operation hours must be greater than an average of 5200 hours per drive and shall include field performance data from all field sites.

The term equipment failure implies that emergency maintenance is required because of a hardware failure.

7.2.2 Preventive Maintenance

No routine scheduled preventive maintenance shall be required. Service will be performed only at an approved service depot (7.2.4).

7.2.3 Service Life

The FINCH shall have a useful service life of five years or 30,000 hours, whichever occurs first, before requiring factory overhaul. Depot repair or replacement of major parts will be permitted during the lifetime (7.2.4).

7.2.4 Service Philosophy

Due to the sophisticated design and special equipment required to repair the 9410, most repairs may only be effected at a properly equipped and staffed depot service and repair facility. These repair facilities will be capable of performing all warranty and routine repair activities in a timely manner.

Further details will be provided at a later date.

7.2.5 Installation

The FINCH is designed, manufactured, and tested with a "Plug-in and Play" installation philosophy. Basically, this philosophy minimizes the requirements for a highly trained personnel to integrate a FINCH into the OEM's system, whether in a factory or field environment. An Operator and Installation Guide is provided with each drive.

7.2.6 Service Tools

No special tools are required for site installation or site maintenance. Refer to paragraph 7.2.4.

8.0 PHYSICAL/ELECTRICAL SPECIFICATIONS

8.1 AC POWER REQUIREMENTS

None

8.2 DC POWER REQUIREMENTS

The voltage and current requirements for a single FINCH are shown in the following table. Values indicated apply at the drive power connector.

Table 1. DC Power Requirements

Voltage	+5 VDC	-5.2 VDC	+24 VDC
Regulation	±2%	±2%	±10%
Ripple	50 mV	50 mV	500 mV
Average Operating Current (Worst Case)	1.5 A	2.4 A	3.3 A
Operating Current (Typical)	1.1 A	2.0 A	2.8 A
Operating Current (Peak)	---	---	4.5 A
Absolute Maximum Voltage Without Physical Damage to Disk Drive	+6.8 VDC	-6.8 VDC	+30 VDC

NOTE 1: At power-up, the motor current regulator will limit the 24-volt current to an average of less than 4.2 amps for a maximum of 14 seconds with 8 amp peaks. (Worst case running and starting current waveforms, Figures 3a and 3b.)

NOTE 2: Minimum current loading for each supply voltage is not less than 30% of the worst case average shown in the table. The 24 volt supply can have instantaneous minimum current 0.3 amp.

NOTE 3: The +5 and -5.2 volt supplies may share a common DC return. The 24 volt supply shall have a separate return.

8.2 -contd.

NOTE 4: Where power is provided to multiple drives from a common supply, worst case average and peak current loading power-up must be considered. The average current noted must be available to each drive to ensure proper spindle acceleration.

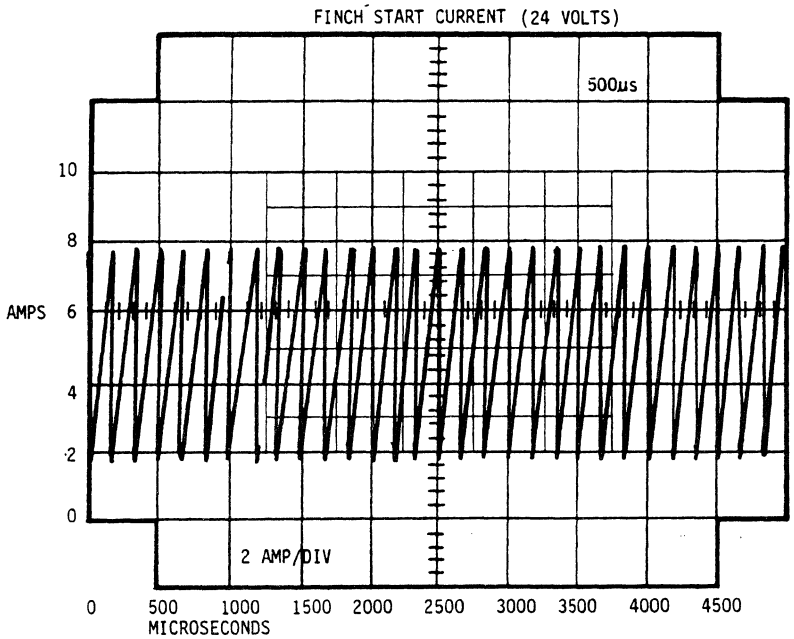
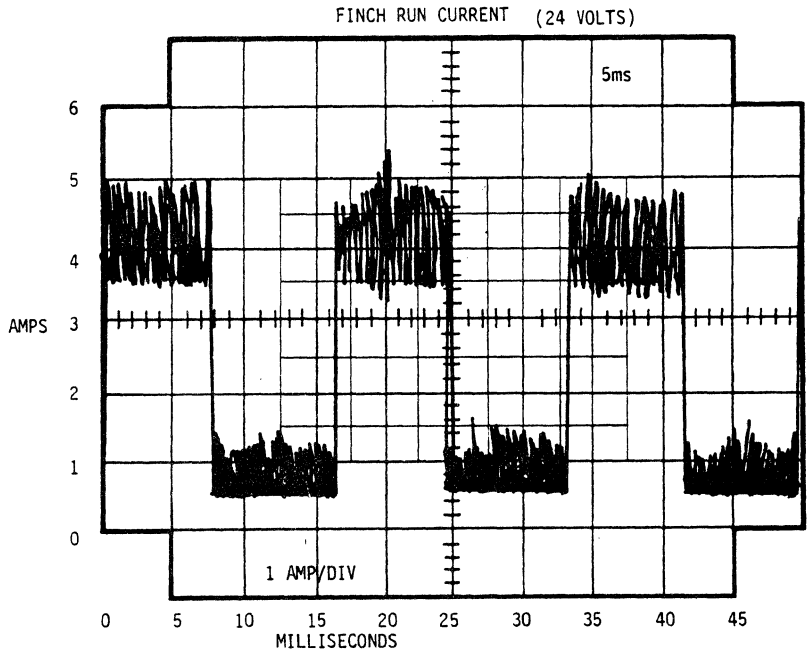


Figure 3a. Starting Current

G164a



G164b

Figure 3b. Running Current

8.2.1 Power Sequencing

There is no power sequencing required for the FINCH. The FINCH design protects against inadvertant writing during power up and down.

8.2.2 24 VDC Current Profile

Figure 4 identifies the 9410 FINCH 24 VDC current profile during the FINCH Operation. The graph times represent the following:

T1 When power is applied to drive
1. Spindle brake released
2. Servo Amp is disabled by Microprocessor
3. Spindle begins to turn, while motor control board is held Reset

T2 At about 10 sec after power to drive spindle reaches 3600 RPM, but Microprocessor still has motor control board Reset.

T3 The Microprocessor has checked the motor feedback signal and has determined that the spindle is turning, it now releases the Reset to the motor control board, the speed Regulator on the motor control board senses the over speed and turns off the drive current to the spindle. The spindle will begin to coast down to 3600 RPM.

T4 While the spindle has coasted down to 3600 RPM, the microprocessor begins the auto-velocity sequence.

T5 While the Velocity is being set to the proper value, the motor has coasted down to 3600 RPM and the motor control board Regulator begins to regulate the spindle at 3600 RPM.

T6 Velocity is set and drive is ready for reading and writing.

T7 Power is removed from drive.

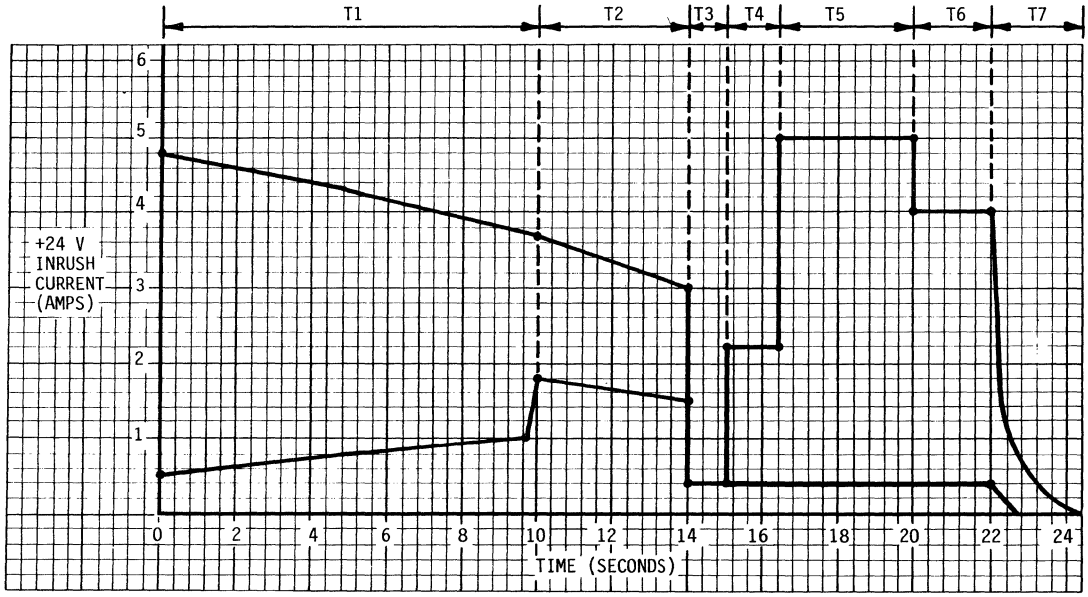


Figure 4. Typical +24VDC Current Profile

GG173a

8.3 HEAT/POWER DISSIPATION

Each FINCH will dissipate no more than 100 watts of dc power average or dissipate more than 350 BTU's per hour. Typical power dissipation under nominal conditions is 85 watts.

8.4 ENVIRONMENTAL LIMITS

Temperatures and humidity specifications preclude condensation on any drive part. Altitude and atmospheric pressure specifications are referenced to a standard day at 58.7°F (14.8°C).

8.4.1 Temperature

a. Operating

50° to 104°F (10° to 40°C) with a maximum gradient of 18°F (10°C) per hour. Above 983 feet (300 meters) altitude the maximum temperature is derated linearly to 95°F (35°C) at 6562 feet (2000 meters). Cabinet packaging designs should provide ample air circulation around the FINCH to ensure environmental limits are not exceeded as a result of heat transfer from other system components.

b. Transit

-40° to 158°F (-40° to 70°C) with a maximum gradient of 36°F (20°C) per hour. This specification assumes that the drive is packaged in the shipping container designed by CDC for use with the FINCH.

c. Storage

14° to 122°F (-10° to 50°C) with a maximum gradient of 27°F (15°C) per hour.

8.4.2 Relative Humidity

a. Operating

20% to 80% relative humidity with a maximum gradient of 10% per hour.

b. Transit

5% to 95% relative humidity.

c. Storage

10% to 90% relative humidity.

8.4.3 Effective Altitude (Sea Level Reference)

a. Operating

-983 to +6562 feet (-300 to +2000 meters)

b. Transit

-983 to +9830 feet (-300 to +3000 meters)

c. Storage

-983 to +8200 feet (-300 to +2500 meters)

8.4.4 Vibration and Shock

The FINCH is designed to withstand the vibration and shock conditions specified below without damage to its function, physical structure, or external appearance.

NOTE

Shock and vibration limits are measured directly on the drive casting. If the equipment is installed in an enclosure to which the stated shock/vibration criteria is applied, resonances may occur internally to the enclosure resulting in vibrations in excess of these limits. In this case, it may be necessary to add shock absorbers to the enclosure.

a. Operating

Equipment, as normally installed and positioned, shall meet the full specified performance while subject to the following conditions injected from the floor in a vertical direction.

1. Continuous vibration as indicated in Figure 5, Curve A (Operating).
2. Intermittent shocks of up to 2 g and not exceeding 10 milliseconds in duration. No shock is to be repeated more often than two per second.

b. Transit

Equipment in its normal upright position shall withstand the conditions of vibration and shock injected from the floor in the three major mutually perpendicular axes.

1. Vibration as shown in Figure 5, Curve C (Non-Operating Packaged).
2. Shocks of up to 5 g, not exceeding 10 milliseconds in duration. The time between consecutive shocks cannot be less than five seconds.

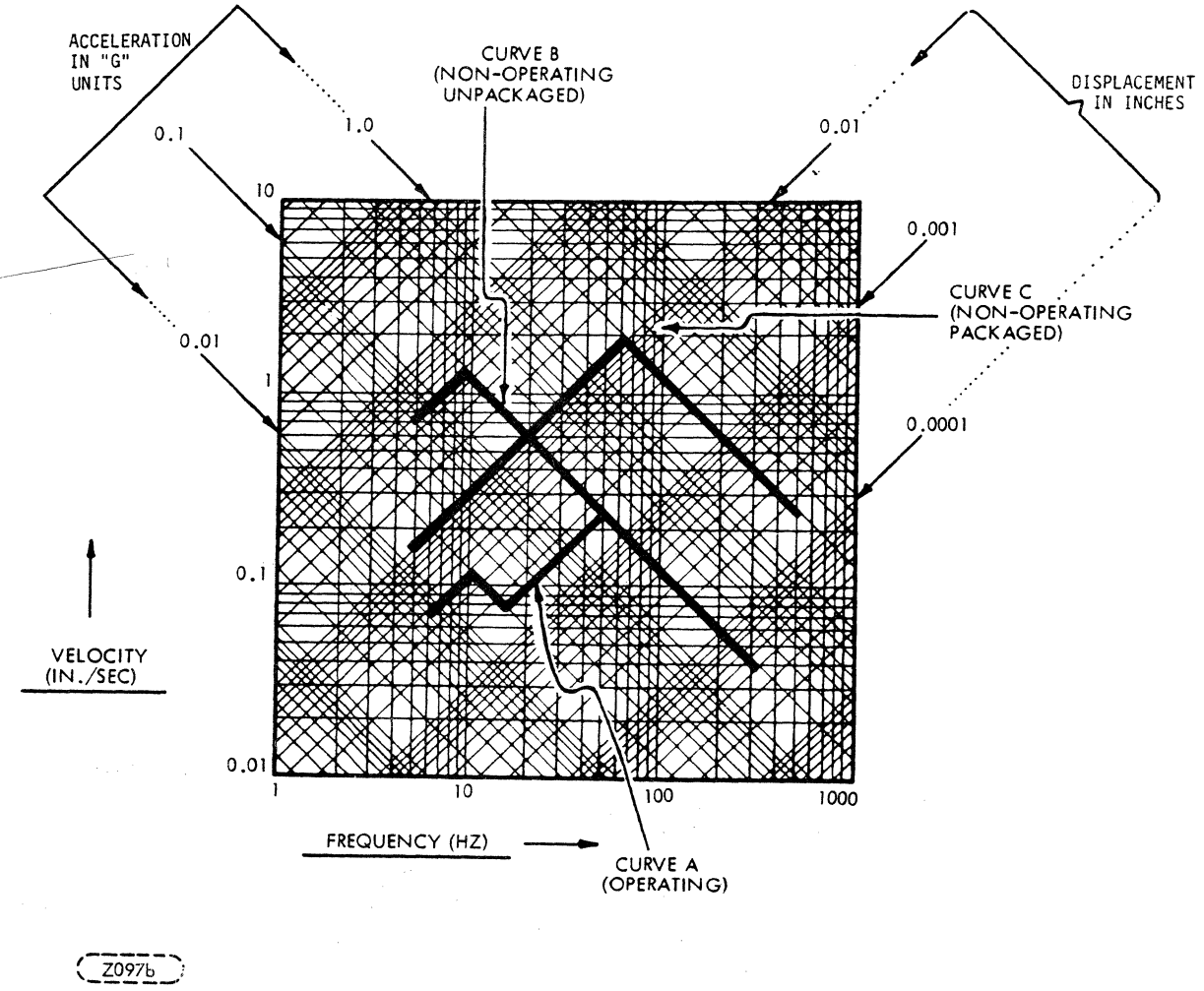


Figure 5. Vibration Levels

8.4.4 -contd

The FINCH is packaged by CDC for van or air freight shipment, shall withstand drop tests from 36 inches (914.4 mm) on all surfaces, three edges and one corner, against a concrete floor or equivalent. See Figure 6.

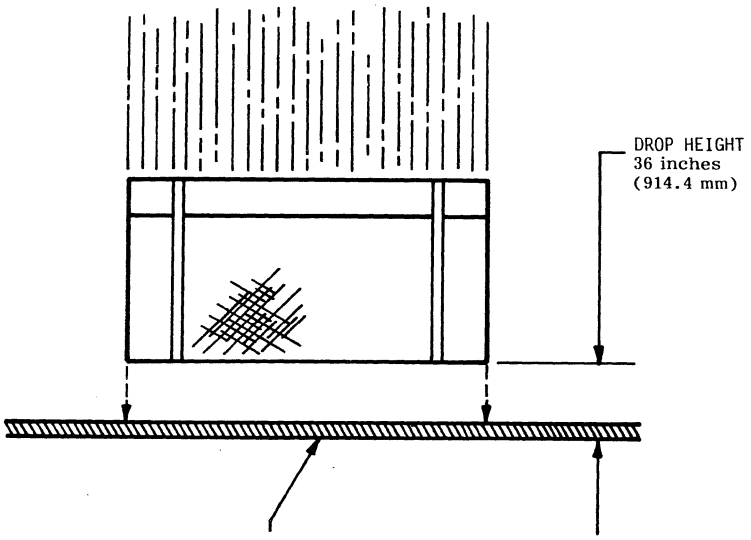


Figure 6. Flat Drop Test

8.4.5 Air Cleanliness

The FINCH is designed to operate in what CDC considers to be an office environment with minimum or no environmental control. Heating is provided, but artificial cooling may not exist for the equipment. Natural or forced air ventilation may be used to limit the maximum temperature. This range is considered the minimum acceptable environment for human comfort. In this environment, the FINCH will operate with the following levels of contamination:

a. Particle sizes greater than 1.0 micron-concentration of 4×10^7 particles per cubic meter.

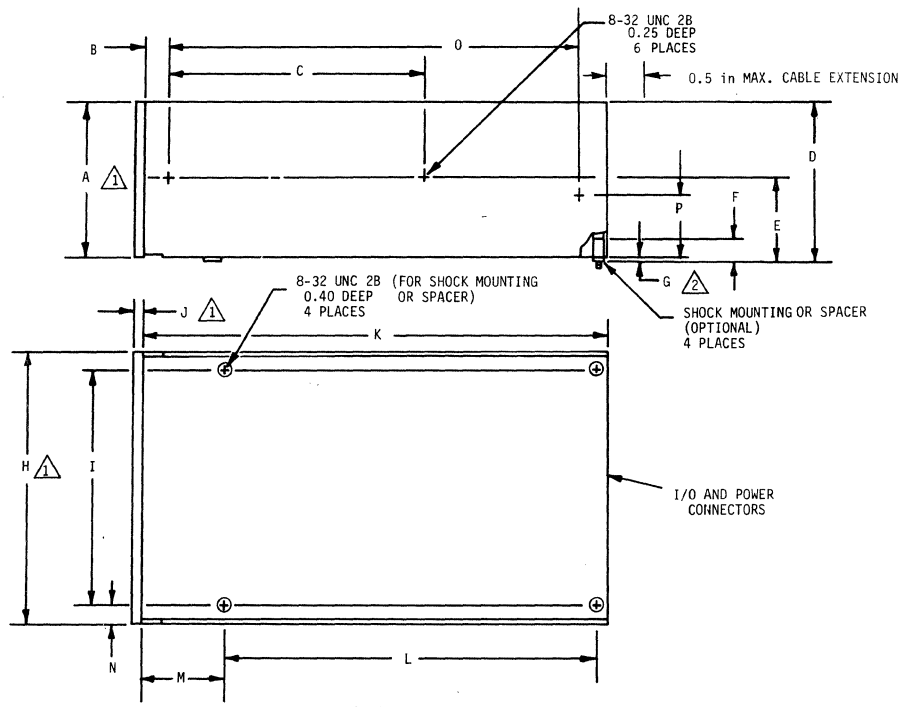
b. Particle sizes greater than 1.5 microns-concentration of 4×10^6 particles per cubic meter.

c. Particle sizes greater than 5.0 microns-concentration of 4×10^5 particles per cubic meter.

8.5 MECHANICAL SPECIFICATIONS

The following dimensions are exclusive of the decorative front panel accessory. Refer to Figure 7 for detailed mounting configuration dimensions. The illustration and dimensions are preliminary and subject to revision.

Height:	4.62 inches	117.4 millimeters
Width:	8.56 inches	217.42 millimeters
Depth:	14.00 inches	354.6 millimeters
Weight:	Approximately 20 pounds	Approximately 9.06 kilograms



DIMENSION	INCHES	MILLIMETERS
A	4.62 ±0.02	117.35 ±0.51
B	0.80 ±0.02	20.32 ±0.51
C	8.00 ±0.04	203.2 ±1.02
D	4.62 ±0.03	117.35 ±0.76
E	2.49 ±0.02	63.25 ±0.51
F	0.50 NOMINAL	12.70 NOMINAL
G	0.06 NOMINAL	1.52 NOMINAL
H	8.56 ±0.02	217.42 ±0.51
I	7.30 ±0.06	125.42 ±1.52
J	0.25 ±0.02	6.35 ±0.51
K	14.00 ±0.06	355.6 ±1.52
L	11.65 ±0.04	295.91 ±1.02
M	2.05 ±0.03	52.07 ±0.76
N	0.63 ±0.02	16.00 ±0.51
O	12.90 ±0.02	327.66 ±0.51
P	1.55 ±0.02	39.37 ±0.51

G287a

1 OPTIONAL FRONT PANEL
2 NOMINAL SHOCK OR SPACER PROTRUSION

Figure 7. Mounting Configuration Dimensions

8.5.1 Drive Orientation

The FINCH can be mounted in either of two positions:

1. When viewing from the rear (I/O connectors visible), with its right side facing down and its left side up. (The machine label is located on the left side.)
2. On its baseplate with the environmental enclosure facing up.

Further details on mounting will be included in the Operator and Installation Guide.

9.0 MEDIA CHARACTERISTICS

9.1 MEDIA DESCRIPTION

The media used on the FINCH has a diameter of approximately 8.0 inches. The aluminum substrate is coated with ferrous oxide with lubrication to permit the heads to contact the surface when starting and stopping.

Each data surface has total of 605 tracks and is capable of recording 8,010,240 bytes of unformatted data on 596 tracks. Two error-free spare tracks are provided for track reallocation in the event new media flaws should occur.

Media defects are characterized as being either correctable or uncorrectable as a function of the type and magnitude of the media flaw. Various error correction codes may be implemented to correct errors in the data read from the disk. However, the code chosen should be consistent with the media manufacturers media testing and certification methods. In the FINCH media certification is performed using the following standards:

1. an error burst of 11 bits or less is a correctable error
2. an uncorrectable error is one greater than 11 bits in length

Host systems utilizing the FINCH should have, as a minimum, resident capabilities to recognize and map defective tracks and perform track reallocation routines.

At the time of shipment from the point of manufacture, the FINCH recording surfaces will meet the following requirements.

1. 605 total tracks per data surface
2. 596 primary tracks plus two error-free spare tracks for future use
3. up to seven additional tracks may contain defects
4. tracks 0 and 604 to be error free
5. an area equal to 60 bytes in length immediately after Index to be defect free on each track

At the time of manufacture, media defect information is recorded in surface 0, track 604, and sector 0 (see Figure 8). This identifies flagged track data for those customers who wish to use it as part of a system initialization and track deallocation routine without recertification. If the customer wishes to use this data, it is imperative not to write on this area of the disk until the information has been recovered.

9.1 -contd.

Because the Finch is a soft sectored unit, the customer, after retrieving the ETF information, must calculate where the defective sector is located. Following is an example of how this should be done.

Using the formula of $L = \frac{N \cdot D}{210}$

where N = the number of sectors in the customer's format

where *D = the byte count divided by 64 (BCD64). The BCD64 number will be in the format log at Track 604 and also on the flag track label supplied with the unit

where L = the customer's defective sector

EXAMPLE: Sectors in customer's format = 32
Byte count in factory format log = 150

$L = \frac{32 \cdot 150}{210}$

L = 22 rounded down

Sector 22 will be the customer's defective sector.

---

*The format log has room for only one byte of the byte count information. Therefore, the 13440 bytes per track were divided by 210. This gave us a number that would fit into the one byte area.

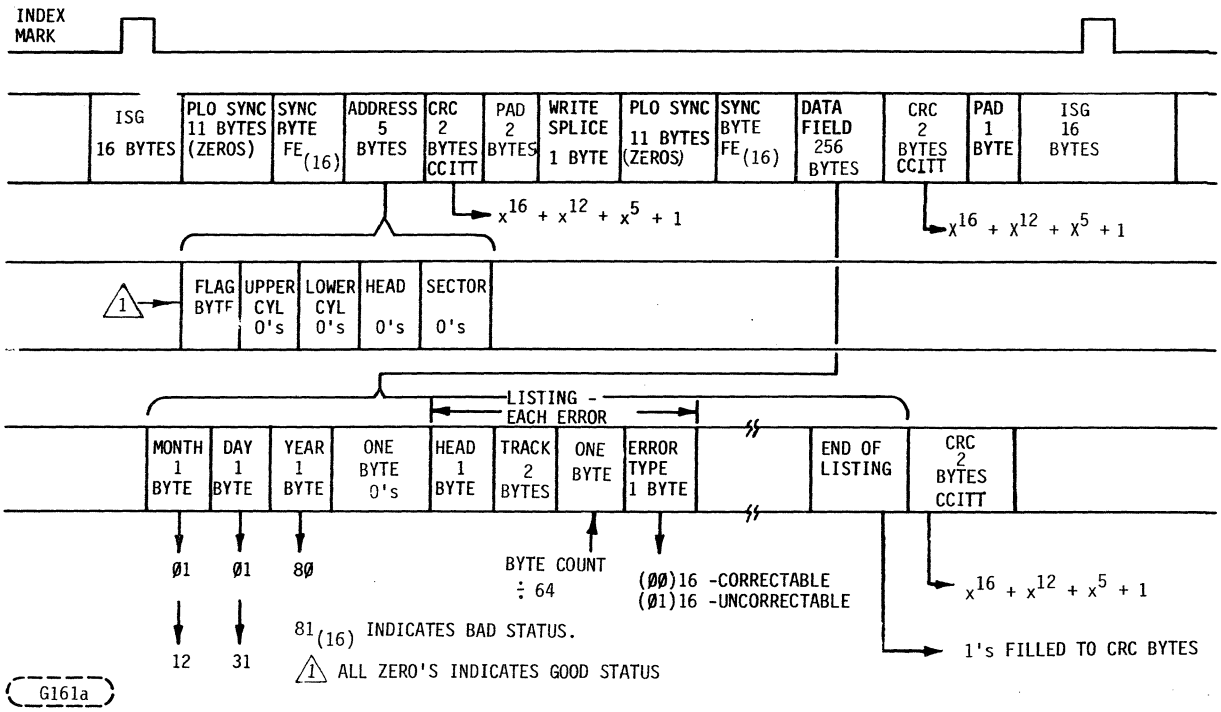


Figure 8. Format for Surface 0, Track 604, Sector 0-- Factory Flagged Track Data Track

10.0 EARLY/LATE STROBE

Error rate specifications will only be met with normal strobe timing. The use of early and late strobes is primarily for factory test; however, these signals could aid in attempts to recover marginal data.

10.1 EARLY DATA STROBE ENABLE

When this line is true, the device PLO data separator will strobe data at a time earlier than nominal. Normal strobe timing will be returned when both strobe enable lines are false.

10.2 LATE DATA STROBE ENABLE

When this line is true, the device PLO data separator will strobe data at a time later than nominal. Normal strobe timing will be returned when both strobe enable lines are false.

11.0 TRACK OR SECTOR REALLOCATION

The error rate and data capacity specifications of the FINCH do not require the utilization of sector reallocation or error correction codes (ECC). However, the FINCH design does not preclude the use of sector reallocation or ECC to aid in recovery of marginal data areas if desired by the user. The use of either method permits the continued use of the major portion, or perhaps all, of a track when a defect is found.

To maximize the available storage capacity, a bad track reallocation customer-designed program is required.

Under typical bad track reallocation, the defective track is reallocated to one of the spare tracks provided. Bad track (or sector) location information is normally recorded on track 604 and read into the customer's operating program during program initialization.

The size of the typical defect found on the disk is less than 11 bits. Obviously, this would affect at least one sector. Flagging and reallocating this one sector may allow the remainder of the track to be used for data storage.

In a sector skip program, one or two spare sectors are allocated at the end of each track. As an example, in a 30 plus 2 scheme, there are 30 data sectors plus 2 spare sectors per track. The defective sector is flagged, then shifted to the following sector when performing an actual operation. Or, a defective sector can be flagged and reallocated to a spare sector at the end of its track.

Defective byte location information will be provided on track 604, head 0 of the disk at the time of shipping from the point of manufacture.

11.1 ERROR DETECTION

Because no fault indication or operator/drive interaction is required, software must adequately inform the operator if any technical difficulties arise. In multi-unit installations, logical and physical identification are necessary for the operator to identify a defective unit. For further information refer to Application Note for Diagnostics, 77653374.

12.0 INTERFACE CABLING REQUIREMENTS/OPTIONS

Interface cabling options for the FINCH are shown in Figure 9. View A of Figure 9 shows each drive interfaced to its own command cable, which, in turn, allows interfacing of more than four drives and a variety of system operational techniques. Each drive has its data cable and command cable radially connected to the host controller. The length of each individual cable must not exceed 20 feet (6.1 meters). Terminator resistors must be installed in the host controller for each data cable and for each command cable. If instead of all FINCH's there are FDD's plus FINCH's in this radial configuration, then a terminator resistor pack also would be installed in each FDD for its data/command cable.

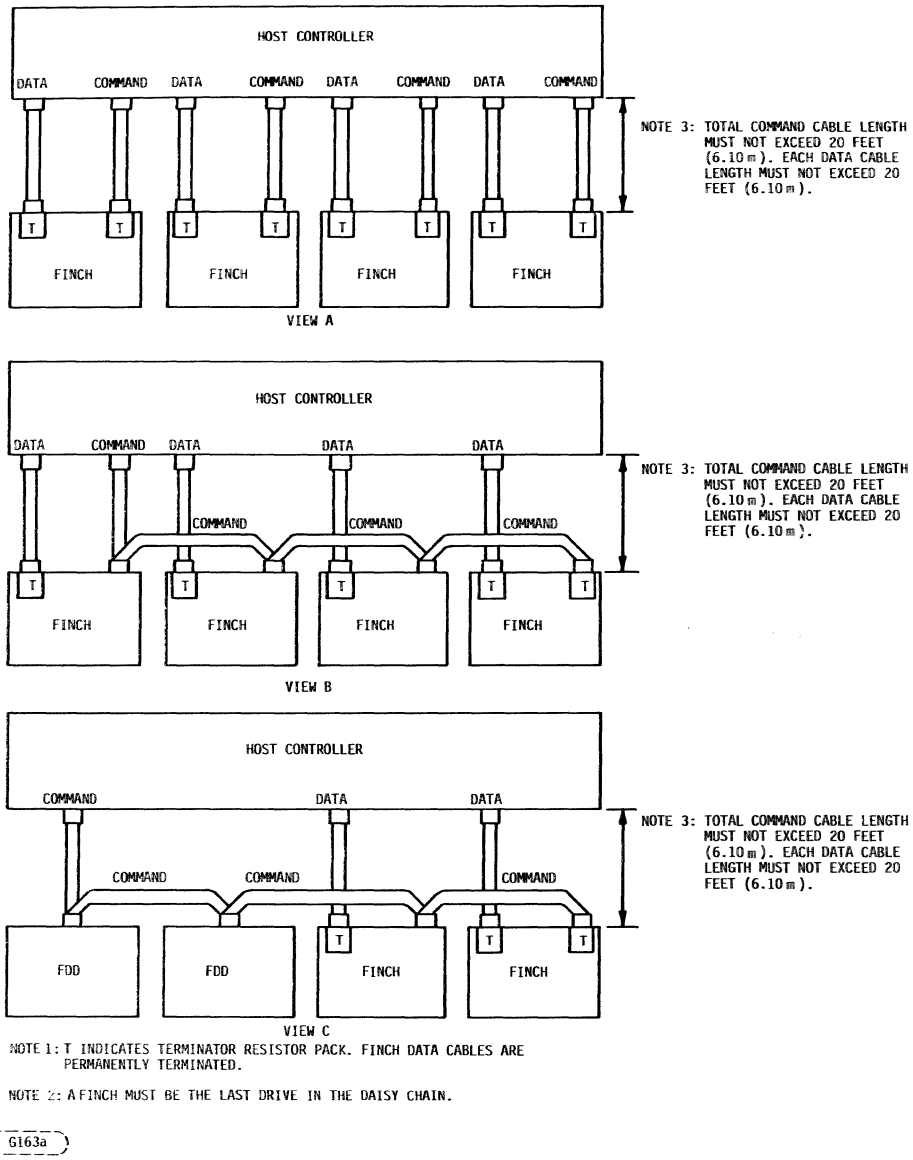
A daisy chain configuration incorporates parallel interfacing of the disk drives on a common command cable. A maximum of four drives may be daisy chained on the command cable. Only the drive which is selected by the host system has its control and data signals enabled through this common interface. View B of Figure 9 consists only of FINCH's. A terminator resistor is required in the host controller for each data cable. Only the last FINCH in the daisy chain requires a terminator resistor pack for the command cable. Terminator resistor packs for the command cable of other drives would be removed. The total combined command cable length (from the controller to the first drive, to the second and subsequent drives) must not be more than 20 feet (6.1 meters). A FINCH must be the last drive in the daisy chain; this is to ensure FINCH-unique lines are terminated.

View C of Figure 9 consists of a common controller for both FINCH's and FDD's. A maximum of four drives (any combination of FDD's plus FINCH's)) may be daisy chained on the command cable. Terminator resistors are required in the controller and in the last drive in the daisy chain for the command cable. Terminator resistor packs for the command cable of other drives would be removed. A terminator resistor is required in the controller for each data cable. The total combined command cable length (from the controller to the first drive, to the second and subsequent drives) must not be more than 20 feet (6.1 meters).

CAUTION

A FINCH must be the last drive in the daisy chain.

Refer to paragraph 14.1.1 for logical unit selection.



NOTE 1: T INDICATES TERMINATOR RESISTOR PACK. FINCH DATA CABLES ARE PERMANENTLY TERMINATED.

NOTE 2: A FINCH MUST BE THE LAST DRIVE IN THE DAISY CHAIN.

G163a

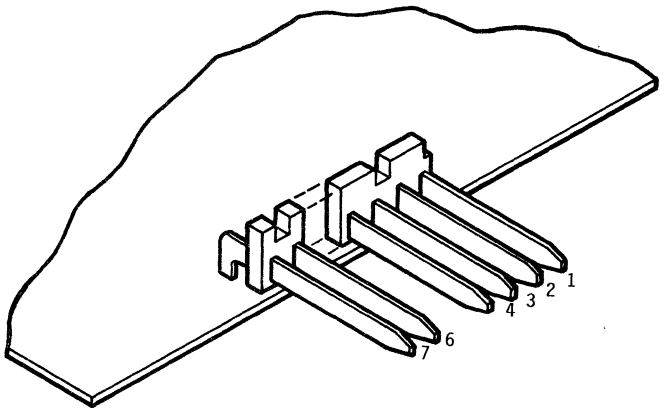
Figure 9. Interface Cabling Options

12.1 DC CABLE AND CONNECTOR

The FINCH receives DC power through a 7-position connector which plugs into either two right-angled headers or one 7-pin header mounted on the printed circuit board assembly. The 2-pin and 4-pin headers are mounted such that they form a composite 7-pin header with the fifth pin missing (see Figure 10). The plug-in connector consists of a locking clip housing with the fifth position molded shut for keying; this housing uses locking clip contacts. If locking clip contacts are not desired, a housing using high pressure contacts and a nylon keying post to be plugged into the fifth position can be used.

Recommended part numbers for the mating connector are included below, but equivalent parts may be used.

CONNECTOR	AMP PART NO.
7-Position Plug-in:	
With Locking Clip Housing	1-87270-1
Locking Clip Contacts	87278-2
Crimping Tool for Locking Clips	90308
Without Locking Clip Housing	3-87025-3
High Pressure Contacts	87024-3
Nylon Keying Post	87116-1
Mate-n-Lok Kit	77664325



G040b

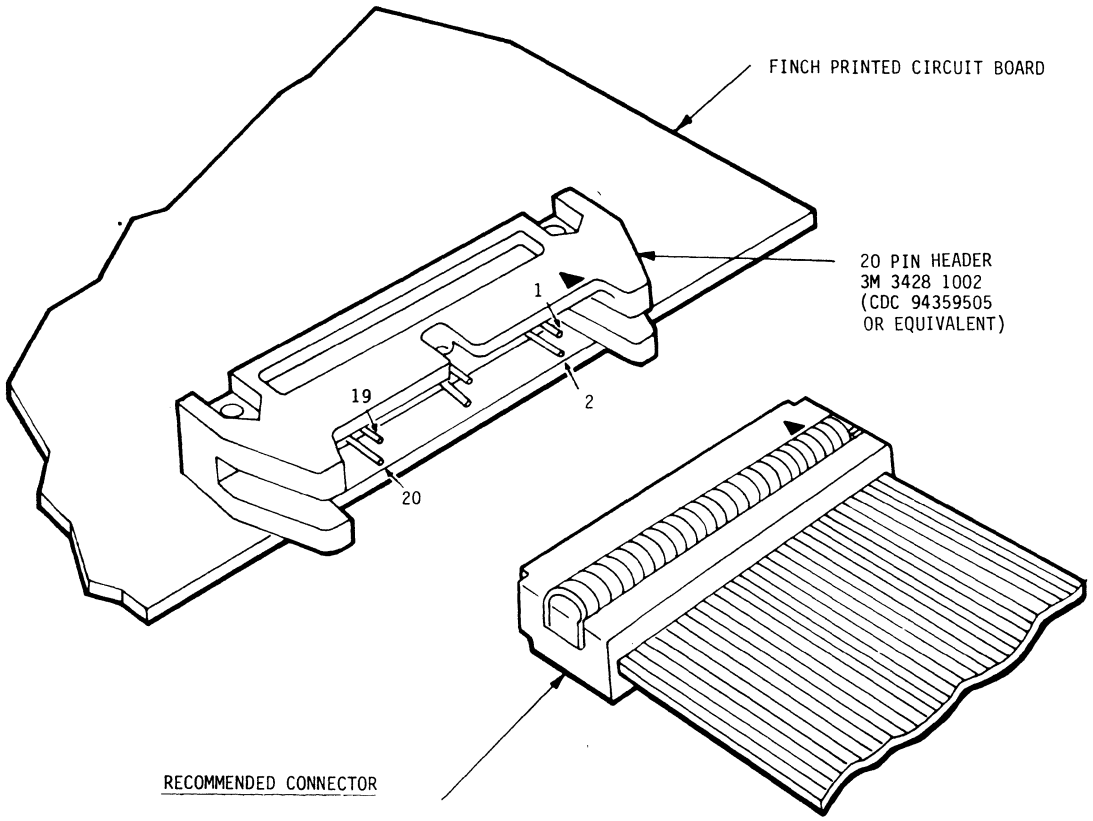
PIN	FUNCTION
1	-5.2 V
2	5.0 V
3	±5 V Common
4	+24 V
6	+24 V Common
7	±5 V Common

Figure 10. DC Cable Connector

12.2 DATA CABLE AND CONNECTOR

Refer to Figure 11 for a pictorial representation of the Data cable interface. Recommended part numbers for the mating connector are included below, but equivalent parts may be used.

CONNECTOR (20-Pin)	PART NO.	CABLE
With Strain Relief	3M-3421-3000 or AMP 86904-2	Flat Cable (Stranded AWG 28) 3M-3365-20
Without Strain Relief	3M-3421-0000	Flat Cable (Stranded AWG 28) 3M-3365-20
	3M-3421-0000	Flat Cable (Standed AWG 28) 3M-3476-20 (Shielded Cable)



G042b

Figure 11. Data Cable Interface

12.3 COMMAND CABLE AND CONNECTOR

The I/O connector for the command interface is a 50-pin board-edge connector (Figure 12). The odd pins are located on the non-component side of the printed circuit board and are connected to the ground plane. The even pins are on the component side of the printed circuit board.

Recommended part numbers for the mating connector are included below, but equivalent parts may be used.

CONNECTOR (50-Pin)	CONTACTS	CABLE
3M-3415-0001	---	Flat Cable (Stranded AWG 28) 3M-3365-50
AMP 1-583718-1	AMP 1-583616-1	Flat Cable (Stranded AWG 28) 3M-3365-50
AMP 1-583717-1	AMP 583616-5 (Crimp) AMP 583854-3 (Solder)	Twisted Pair AWG 26
Viking 3VH25/IJN-5	---	Twisted Pair AWG 26 (Solder Term)
3M-3415-0001	---	Flat Cable (Stranded AWG 28) 3M-3476-50 (Shielded Cable)

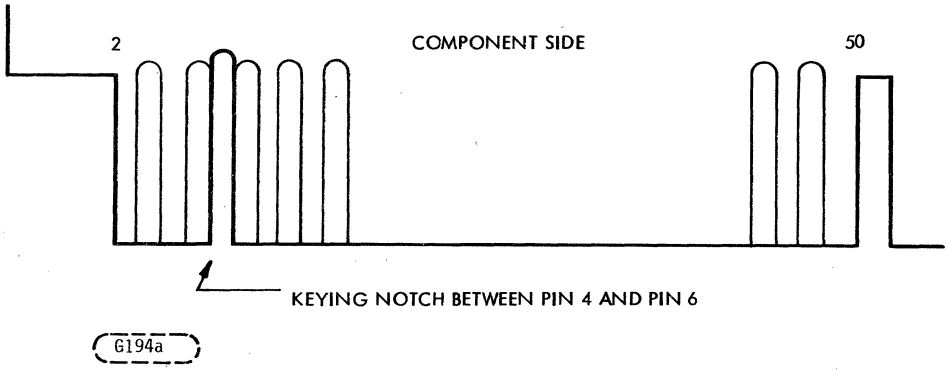


Figure 12. Command Cable Interface

12.4 INTERFACE DRIVERS/RECEIVERS

The FINCH utilizes two types of signals -- single-ended and balanced differential. The data and clock signals utilize balanced differential drivers and receivers. All other signals utilize single-ended drivers and receivers.

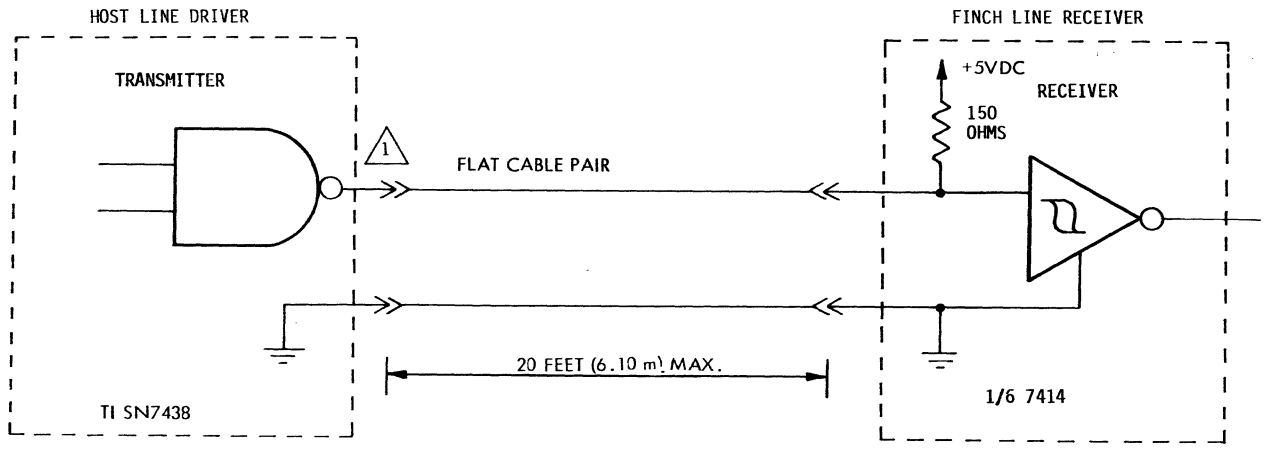
12.4.1 Single-Ended Drivers/Receivers

12.4.1.1 Transmitter Characteristics

The FINCH uses the 7438 open collector quad-2-input driver (or equivalent) to transmit status and data to the host. This driver is capable of sinking a current of 48 mA with a low-level output voltage of 0.4 volt (see Figure 13).

12.4.1.2 Receiver Characteristics

The FINCH uses the 7414 Hex Inverter with hysteresis gate (or equivalent) as a line receiver. The input of each receiver is terminated in 150 ohms as shown in Figure 13.



INTERFACE SIGNAL LEVELS AND LOGICAL SENSE AT THE FINCH I/O CONNECTOR ARE DEFINED AS FOLLOWS:

1 - DRIVER TERMINATION TBD

LOGIC LEVEL	FROM FINCH	TO FINCH
HIGH (FALSE OR DEACTIVATED) (0)	$\geq$ 2.4 V; $\leq$ 5.0 V	$\geq$ 2.0 V; $\leq$ 5.0 V
LOW (TRUE OR ACTIVATED) (1)	$\leq$ 0.4 V; $\geq$ 0.0 V	$\leq$ 0.8 V; $\geq$ 0.0 V

THE DIFFERENCE IN THE VOLTAGES BETWEEN INPUT AND OUTPUT SIGNALS IS DUE TO THE LOSSES IN THE CABLE.

ZZ192a

Figure 13. Single-Ended Transmitters and Receivers

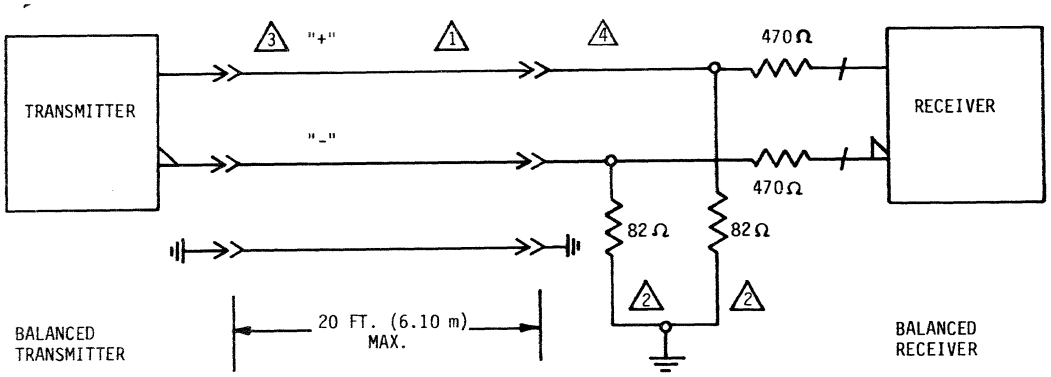
12.4.1.3 Terminator Characteristics

The terminators consist of a DIP resistor module which plugs into a DIP socket in the last unit in a daisy chain. Each drive is furnished with terminators. Terminators must be removed from all except the last drive on the cable prior to daisy-chain operation. An equivalent terminator must be provided in the controller on each input signal line from the FINCH to the controller. Refer to Figure 13. Only the Command cable DIP resistor module is removable.

12.4.2 Balanced Differential Drivers/Receivers

12.4.2.1 Transmitter Characteristics

The FINCH uses 75110A-type balanced differential drivers terminated per Figure 14. Logic 1 on the interface is defined when the "+" output is more positive than the "-" output.



1. CABLE SHALL BE FLAT CABLE 3M-3365-20 OR EQUIVALENT

2. TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER. THESE SIGNALS MUST BE RADIALLY-CABLED.

3. NOMINAL "-" LINE 0V
NOMINAL "+" LINE
LOGIC 0
LOGIC 1
1.21 V (MAX.)
0.623 V (MIN.)
-0.715 V
$10 \leq T_r \leq 35$ ns, 10% to 90% LEVEL

4. IF FINCH IS TO BE LOCATED EXTERNAL TO HOST CABINETRY, APPROPRIATE I/O CABLE SHIELDING AND SHIELD TERMINATION MAY BE REQUIRED TO MEET RADIATED EMISSIONS STANDARDS.

G048a

Figure 14. Balanced Differential Drivers/Receivers

12.4.2.2 Receiver Characteristics

The FINCH uses the 75107A-type balanced differential receiver terminated per Figure 14. Logic 1 on the interface is defined when the "+" input is more positive than the "-" input.

12.4.2.3 Terminator Requirements

Each differential receiver in the drive is terminated with 470-ohm and 82-ohm resistors per Figure 14. An equivalent terminator must be provided in the controller on each input signal line from the FINCH to the controller.

13.0 DIGITAL-INTERFACE SIGNAL DEFINITIONS

The FINCH utilizes two digital interface cables (Command and Data) for information transfer between it and the controller/host system. The connector pin assignment for the Command cable is shown in Figure 15. The connector pin assignment for the Data cable is shown in Figure 16. The signal direction, as well as type is also shown on these figures. (All single-ended signals are true when the interface voltage level is less than 0.4 volts.)

14.0 INTERFACE SIGNAL DEFINITIONS

This section lists and defines standard input and output signals. All non-reserved signal leads not used by the controller must be either terminated or set to a logic 0 state. Reserved interface leads are discussed in paragraph 14.3. All timing diagrams for single-ended signals are drawn with the true or logic 1 state signalled by the low voltage level.

All information in this section assumes valid drive operating conditions have been accommodated. Refer to Figures 15 and 16.

14.1 INPUT SIGNAL LINES

14.1.1 Drive Select (1-2-3-4)

These input lines are used to activate a device's drivers and receivers for up to four drives in a daisy-chained operation.

Drive select must remain active during any communication with the host controller.

All signals from the drive in the radial data cable are available to the controller regardless of the state of the Drive Select lines.

Logical unit designation is accomplished at the time of installation by setting the Unit Select plug located on the base board assembly.

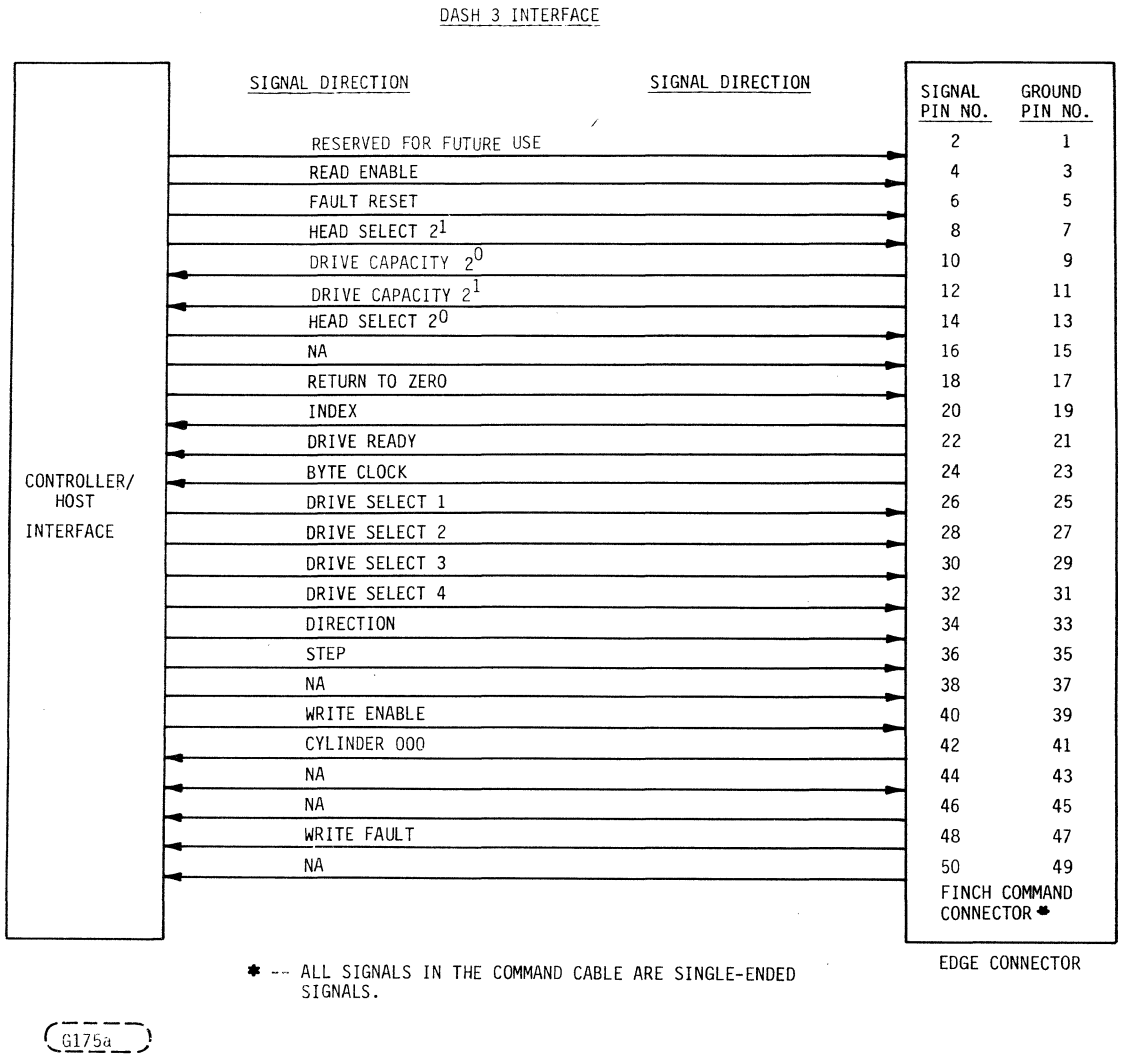


Figure 15. Command Cable Interface

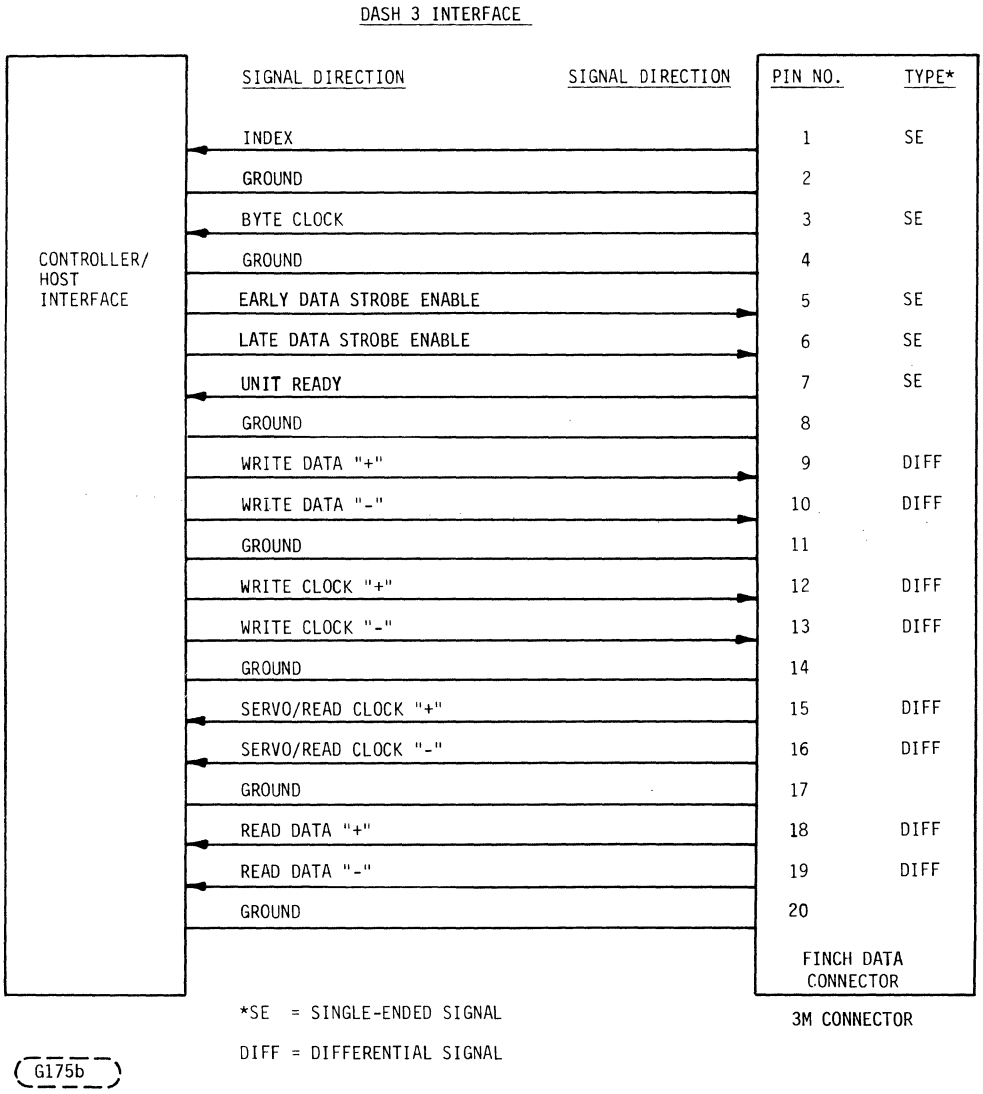


Figure 16. Data Cable Interface

14.1.1 -contd.

All command cable lines are gated with Drive Select. No data cable signal lines are gated with Drive Select.

The 9410 should not be selected until radial Unit Ready signal in the Data cable is received after DC power has been applied (Figure 17). The 9410 will be selected within 1 microsecond after the activation of Drive Select and deselected within 1 microsecond after the deactivation of Drive Select. Drive Select must be valid 1 microsecond before the first step pulse is received and 1 microsecond after the last step pulse is received.

At the completion of a write operation, Drive Select must remain active for 1 microsecond (Figure 19). When the Drive Select line is activated, a head change will occur, thus requiring a delay before a read or write operation can be initiated.

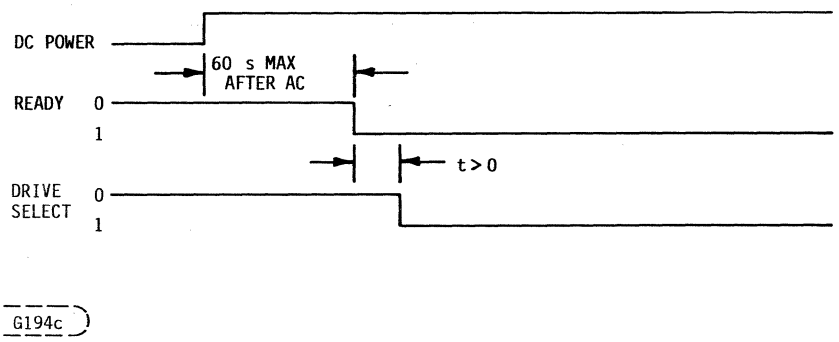
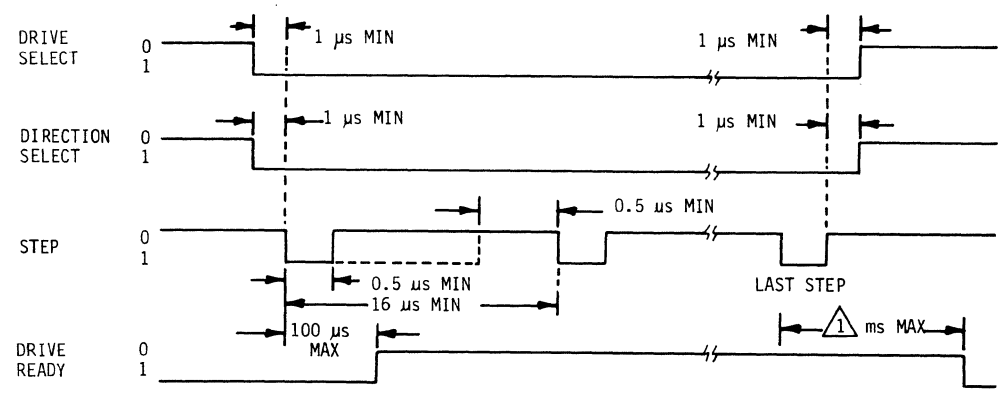


Figure 17. Power Turn On and Drive Selection

14.1.2 Direction

Direction determines the course of movement of the head carriage: a logic 1 on this line signifies head-carriage movement toward the higher-numbered cylinders; a logic 0 on this line signifies head-carriage movement toward the low-numbered cylinders.

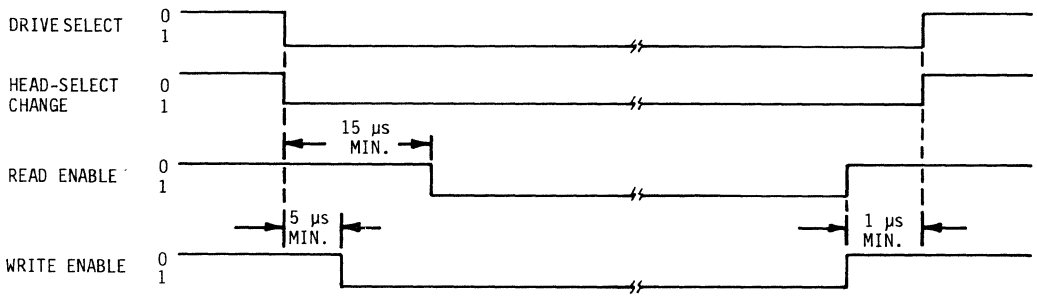
Direction must stabilize a minimum of 1 microsecond before each Step pulse and 1 microsecond after the last Step pulse (see Figure 18).



G194d

1 -- 10 ms FOR A SINGLE TRACK SEEK (I.E., 1 STEP PULSE).
-- DEPENDENT ON STEP RATE INPUT

Figure 18. Track-Access Timing



G195a

Figure 19. Head Select Timing

14.1.3 Step

Step is used with Direction to cause head-carriage movement. Each pulse on the Step line causes the head carriage to be moved one cylinder in the direction determined by the state of the Direction line.

Step pulses must be a minimum of 0.5 microsecond at the logic 1 or logic 0 level (See Figure 18). The minimum time between Step pulses is 16 microseconds. (To meet the 9410 seek performance characteristics, a maximum time between Step pulses is 25 microseconds.)

The 9410 operates in a semibuffered Step mode. The read/write heads will start to move when the first Step pulse is received. The rate of head movement is determined by the rate of the incoming Step pulses; however, the Step pulse rate may exceed the head movement rate. The Drive Ready line is used to indicate that a seek is in progress (see Figure 18). The Drive Ready line will be deactivated within 100 microseconds after the leading edge of the first Step pulse and will be activated when the seek function is successfully completed.

After the last Step pulse has been sent to the 9410, the Drive Select line may be deactivated and a different drive selected. The minimum time after the last Step pulse before the Drive Select or Direction line can be deactivated in 1 microsecond.

The first Step pulse to initiate a seek should not be sent to the 9410 unless the Drive Ready line is true.

The drive will always attempt to maintain the heads over the recording zone of the media (between tracks 0 and 604). Head positioning movement will normally terminate at the boundary (track 0 or 604) in the direction of movement; however, if a hardware fault existed within the drive such that the head was driven outside of the recording zone, the head will automatically be repositioned over track 0 if possible. If the head can be positioned within the recording zone successfully, no fault will be signified and the Drive Ready line will be activated after successfully positioning the head. It is the controller's responsibility to verify the correct head position after a seek function.

14.1.4 Head Select 2^0, 2^1

These lines are used to select the proper media nad head for data transfer as follows:

Head 2^1 J2-8	Selection 2^0 J2-14	Head	Media
0	0	0 - TOP	1st Disk Nearest Deck Casting
0	1	1 - BOTTOM	2nd
1	0	2 - TOP	2nd
1	1	3 - BOTTOM	3rd

Head Selection may be changed at any time following activation of Drive Select, but must occur a minimum of 15 microseconds prior to a read operation or 5 microseconds prior to a write operation. Read Enable or Write Enable must be deactivated a minimum of 1 microsecond prior to a head change (Figure 19).

The Drive Ready line will not change as a result of head change.

14.1.5 Fault Reset

Fault Reset is used to reset the Write Fault latch if the fault no longer exists. A minimum 1 microsecond pulse to the logic 1 level is required to reset the Write Fault latch.

14.1.6 Return to Zero

RTZ causes the actuator to return to track 0. This seek is significantly longer than a seek to track 0 and should only be used for recalibration and not data acquisition.

The RTZ function will be initiated by a logic 1 pulse (0.5 to 25 microseconds). The Ready signals will be deactivated within 100 microseconds after reception of an RTZ command. The successful completion of an RTZ will be signified by the activation of the Ready signals.

14.1.7 Read Enable

Activation (logic 1) of the Ready Enable signal enables digital read data on the Read Data lines and enables Read Clock on the Read/Servo clock lines. The leading edge of Read Enable triggers the read chain to synchronize the internal phase-locked oscillator to a media-recroded PLO synchronization field (refer to Section 15.0).

14.1.8 Write Enable

Activation (logic 1) of the Write Enable signal enables the write drive and initiates recording of the contents of the Write Data lines onto the media. (Refer to Section 15.0 for timing).

14.1.9 Write Data "+" and "-"

Data to be recorded on the media is supplied on these balanced differential lines. These lines carry NRZ data which is in phase sync with the Write Clock lines. (See Figure 20).

14.1.10 Write Clock "+" and "-"

These lines carry the balanced differential Write Clock signal which must be synchronized with the NRZ Write Data as illustrated in Figure 20. The Write Clock is the Servo Clock retransmitted to the drive during a Write operation. The Write Clock need not be transmitted continuously but must be transmitted at lease 2 1/2 servo clock periods prior to Write Enable.

14.1.11 Early Data Strobe Enable

When this line is true, the device PLO data separator will strobe data at a time earlier than nominal. Normal strobe timing will be returned when both strobe enable lines are false.

14.1.12 Late Data Strobe Enable

When this line is true, the device PLO data separator will strobe data at a time later than nominal. Normal strobe timing will be returned when both strobe enable lines are false.

14.2 OUTPUT SIGNAL LINES

14.2.1 Drive Ready

A logic 1 on this line indicates that the disk is up-to-speed and the drive is on cylinder and not executing a seek function. This line is gated with Drive Select. This signal is also available in the Data cable not gated with Drive Select and is referred to as Unit Ready. The Ready signals will be valid within 500 nanoseconds after the appropriate Drive Select is activated.

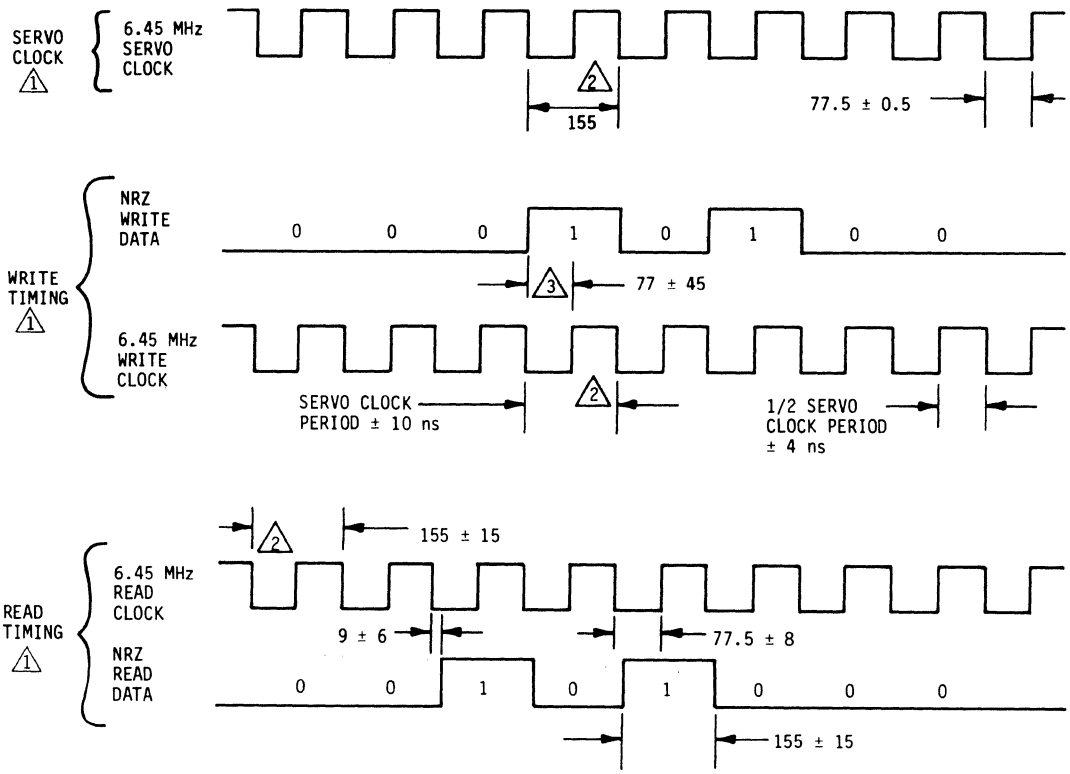
14.2.2 Cylinder 000

This line when true indicates the heads are positioned over cyl. 000.

First Quarter 82 Production Availability

14.2.3 Index

Index, which occurs once per revolution, indicates the physical beginning of the cylinders. Index is true for 1.24 microseconds nominal per revolution (see Figure 21). This signal is contained in the Command cable gated with Drive Select: it is also available in the Data Cable, not gated with Drive Select.



NOTES

1. ALL TIMES IN NANOSECONDS MEASURED AT DRIVE I/O CONNECTOR
2. SIMILAR PERIOD SYMMETRY SHALL BE ± 3 ns BETWEEN ANY TWO ADJACENT CYCLES DURING READING OR WRITING.
3. THIS TIME (77 ± 45 ns) IS MEASURED FROM THE ACTIVATION (OR DEACTIVATION) OF THE NRZ WRITE DATA LINE AND RISING EDGE OF THE WRITE CLOCK LINE.

ALL CLOCK TIMES ARE NOMINAL. A COMBINED SPINDLE SPEED AND CLOCK CIRCUIT TIMING TOLERANCE NOT EXCEEDING 1.5% MUST BE TAKEN INTO ACCOUNT.

SERVO CLOCKS ARE VALID WHEN NOT READING. OTHER TIMING IS APPLICABLE DURING READING OR WRITING.

G049a

Figure 20. NRZ Data and Clock Timing

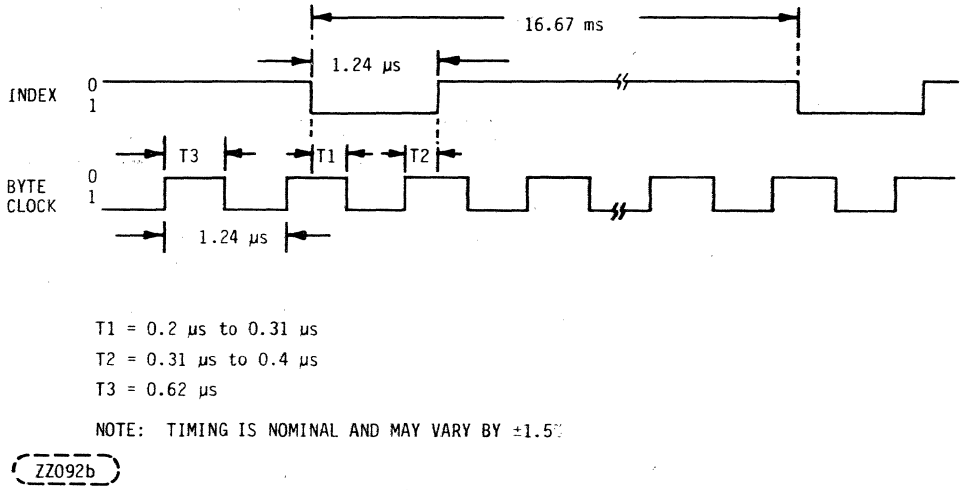


Figure 21. Index and Byte Clock Relationship

14.2.4 Byte Clock

Byte Clock occurs once per eight Servo Clock periods. There are 13,440 byte clocks per disk revolution at a nominal rate of 806 kHz. The controller is responsible for counting the byte clocks to determine the sector size and location. The interrelationship of Index and the Byte Clock is shown in Figure 21. This signal is continuously transmitted if the disk is up to speed and the heads are positioned over the recording zone of the disk.

This signal is contained in the Command cable gated with Drive Select: it is also available in the Data cable not gated with Drive Select.

14.2.5 Write Fault

Write Fault conditions detected by the FINCH will activate the Write Fault signal. The Write Fault signal will remain activated until it is deactivated by the Fault Reset lead or by power sequencing the FINCH. The Write Fault lead will be deactivated within 0.5 microsecond from the leading edge of the Fault Reset line. Writing of the disk will be inhibited if the Write Fault signal is activated.

A Write Fault condition will occur if Write Enable is true and either write current is absent, write data is absent, the FINCH is not ready, invalid head or internal multiple heads are selected, or Read Enable is true. Write Fault will also occur if Write Enable is false and write current is present.

14.2.6 Drive Capacity

(See Head Select Insert) These lines indicate drive capacity as follows:

Drive Capacity				
2^1	2^0			
J2-12	J2-10			
0	0	8 MB		
0	1	24 MB		
1	0	32 MB		

14.2.7 Unit Ready

A logic 1 on this line indicates that the disk is up-to-speed and the drive is on cylinder and not executing a seek function. This signal is not gated with Drive Select. The Ready signals will be valid within 500 nanoseconds after the appropriate Drive Select is activated.

14.2.8 Servo/Read Clock "+" and "-"

These balanced differential lines contain the drive-generated Read Clocks if the Read Enable signal is true or the drive-generated Servo Clocks if the Read Enable signal is false. This signal is located in the Date cable and is not gated with Drive Select.

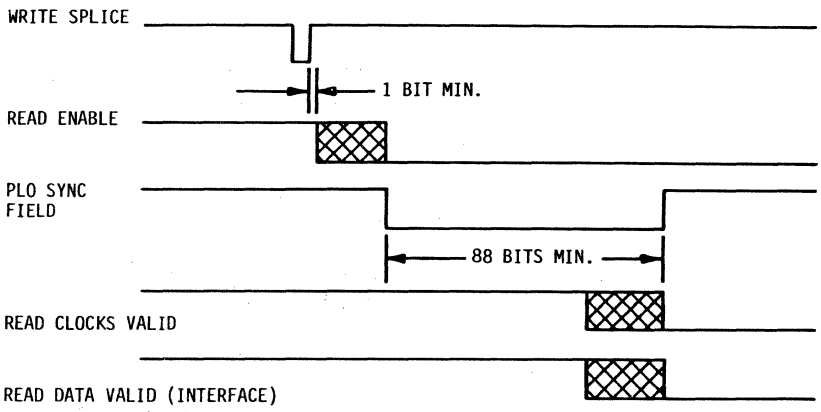
The Read Clock defines the beginning of a data cell and, when valid, is in phase and frequency synchronization with the Read Data as specified in Figure 20. The Read clocks will be valid within 88 Read Clock periods from the concurrence of Read Enable and a PLO synchronization field (refer to Section 15.0 for interface timing).

The Servo Clock is an internally generated phase-locked clock (6.45 MHz nominal) which should be used by the controller to generate Write Clocks (see Figure 20). This clock is phase and frequency locked to the disk rotational speed. Servo Clocks will be valid within two Servo Clock periods after the Read Enable signal is switched from the true to the false condition.

(Phase/Frequency discontinuities may exist, by no clock transistions, in the Servo/Read Clock signal when the Read Enable signal is being switched between the true and false conditions. Refer to Figure 25, Note 1.)

14.2.9 Read Data "+" and "-"

These balanced differential lines transmit the recovered media data in the NRZ form from the FINCH to the controller. This data is in frequency and phase synchronization with the Read Clocks as specified in Figure 20. The Read Data lines are valid within 88 Read Clock periods from the concurrence of Read Enable and PLO synchronization. Refer to Figure 22 for detailed timing and Section 15.0 for recommended format timings. The Read Data lines are located in the data cables and will be a logic 0 until PLO synchronization is established with a Read function.



READ ENABLE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. READ ENABLE MAY BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD.

G162b

Figure 22. Read Timing

14.3 RESERVED SIGNAL LINES

Reserved signal lines are provided for potential future enhancements or for test purposes within CDC. These leads should be left as an open circuit by the controller or supplied with a logic 0 input.

These reserved signal lines are as follows:

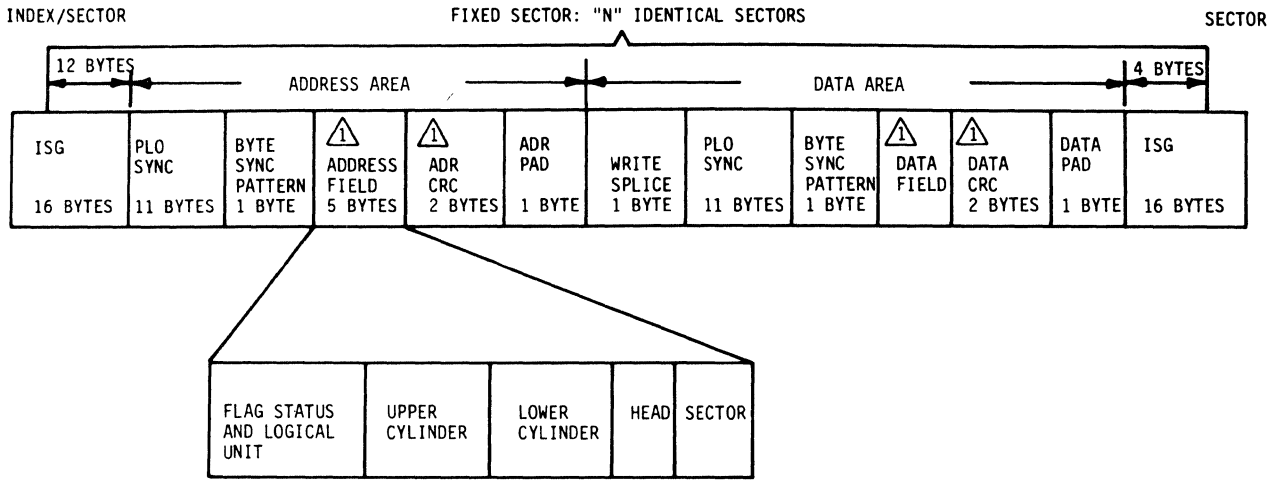
Command Connector, Pin 2 and Pin 12

15.0 DATA FORMAT AND DATA CONTROL TIMING

15.1 FORMAT DEFINITION (HARD SECTOR)

The record format on the disk is under control of the controller. The Index pulse and byte clocks are available for use by the controller to indicate the beginning of a track and allow the controller to define the beginning of a sector. A suggested format for fixed-length data records is shown in Figure 23.

The format presented in Figure 23 consists of three functional areas: Inter-sector Gap, Address, and Data. The Data area is used to record the system's data files. The Address area is used to locate and verify the track and sector location on the disk where the Data areas are to be recorded. This section refers to a Sector pulse which is generated internal to the controller from the Byte clock to ease the format description.



1 THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

G042a

Figure 23. Sector Format

15.1.1 Intersector Gap (Figure 22)

The Intersector Gap (ISG) is 16 bytes long and is oriented to begin four bytes before a Sector (Index) pulse and 12 bytes after a Sector (Index) pulse. This gap size was chosen for the following reasons:

1. It satisfies the drive-required write-to-read recovery time (that is, minimum time between the deactivation of Write Enable to the activation of Read Enable).

2. It allows the heads to be switched during an ISG and the header of the sector following this ISG to be read without incurring a rotational latency.

3. It allows for controller decision making time between sectors.

15.1.2 Address Area (Figure 23)

The address area is used to provide a positive indication of the track and sector locations. The address area is normally read by the controller and the address bytes verified prior to a data area read or write. The address area is normally only written by the controller during a format function (Section 15.2) and thereafter only read to provide a positive indication of the sector location and establish the boundaries of the data area. The address area consists of the following bytes.

1. PLO Sync (11 bytes minimum). These 11 bytes of zeroes are required by the drive to allow the drive's read-data phase-locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

2. Byte Sync Pattern (one byte). This byte is user-defined; it indicates to the controller the beginning of the address field information, and it establishes byte synchronization (ability to partition serial bit stream into meaningful information groupings, such as bytes.) It is recommended that the Byte Sync Pattern contain more than a single one bit for a greater confidence level of detection.

3. Address Field. These bytes are user-defined and interpreted by the controller. A suggested format consists of five bytes, which allows one byte to define flag status bits or logical unit number, two bytes to define the cylinder address, one byte to define the head address, and one byte to define the sector address.

4. ADR CRC (two bytes recommended) - (Address Field Check Codes). Selection of an appropriate error-detection mechanism, such as a cyclic redundancy check (CRC) code, is made by the user and applied to the address for file-integrity purposes. These codes are generated by the controller and written on the media when the address is written. Data integrity is maintained by the controller recalculating and verifying the address-field check codes when the address field is read.

15.1.2 -contd.

5. ADR Pad (one byte) - (Address Field Pad). The Address Field Pad byte must be written by the controller and is required by the drive to ensure proper recording and recovery of the last bits of the address-field check codes.

15.1.3 Data Area (Figure 23)

The data area is used to record the user's data fields. The contents of the data fields within the data area are specified by the host computer system. The remaining parts of the data area are specified and interpreted by the controller to recover the data fields and ensure their integrity. The data area consists of the following:

1. Write Splice (one byte). This byte area is required by the drive to allow time for the write drivers to turn on and reach a recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format and is described in greater detail in Section 15.3.

2. PLO Sync (11 bytes). These 11 bytes of zeroes are required when reading to allow the drive's phase-locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

3. Byte Sync Pattern (one byte). This byte is user defined and indicates to the controller the beginning of the data field bytes and establishes byte synchronization for the data field. It is recommended that this byte contain more than a single one bit.

4. Data Field. The data field contains the host system's data files.

5. Data CRC (two bytes) - (Data-Field Check Codes). These codes are generated by the controller and written on the media with the data field. The controller maintains data integrity by recalculating and verifying the data field check codes when the data field is read.

6. Data Pad (one byte) - (Data Field Pad). The Data Field Pad byte must be written by the controller and is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes.

15.2 WRITE-FORMAT PROCEDURE

Provisions must be made within the controller to format the disk. The following procedure is recommended for fixed-length sector formats with separate address and data fields. This procedure is based on formatting from "Index to Index."

1. Select the desired unit, cylinder, and head. The controller must wait for Ready to begin a search for the leading edge of Index. If a head change was affected, the controller must provide a 5 microsecond minimum delay before Write Enable may be activated.

2. Search for and detect the leading edge of Index and activate Write Enable.

3. Write 12 bytes of zeroes for the ISG following the Index/Sector pulse.

4. Write 11 bytes of zeroes for the address field PLO sync area.

5. Write a byte sync pattern, the address field, the address field check bytes (2).

6. Write all zeroes for the address pad byte, the write splice byte and 11 bytes of the data area PLO sync.

7. Write the data area byte sync byte, the data field, two data field check bytes and the data pad byte.

8. Write four bytes of zeroes for the ISG preceeding the sector pulse.

9. If the next sector of the same track is to be formatted and the head is not deselected, Write Enable should remain true and the format procedure followed starting at Step 3. If the last sector of the track was just formatted, zeroes should be written until the Index pulse is again detected, then Write Enable should be deactivated; then proceed to Step 1.

   Write Enable must be deactivated 1 microsecond before a head change can be initiated; however, Write Enable may not be activated until 5 microseconds after a head change. Thus, it may be desired to affect the head change prior to the Index pulse according to the format chosen.

15.3 READ/WRITE CONTROL TIMING (See Figures 24 and 25)

This section specifies the interrelationship of the drive interface control leads necessary to recover or record data fields on a formatted disk media. The format of Section 15.1 will be assumed; however, critical drive-dependent parameters are summarized in Figures 24 and 25.

To perform a data field read function, the address field is read and verified, then its data field is read. To perform a data field write function, the address field is read and verified, then the data area is written. The following sections will expand on these concepts.

15.3.1 Read Function

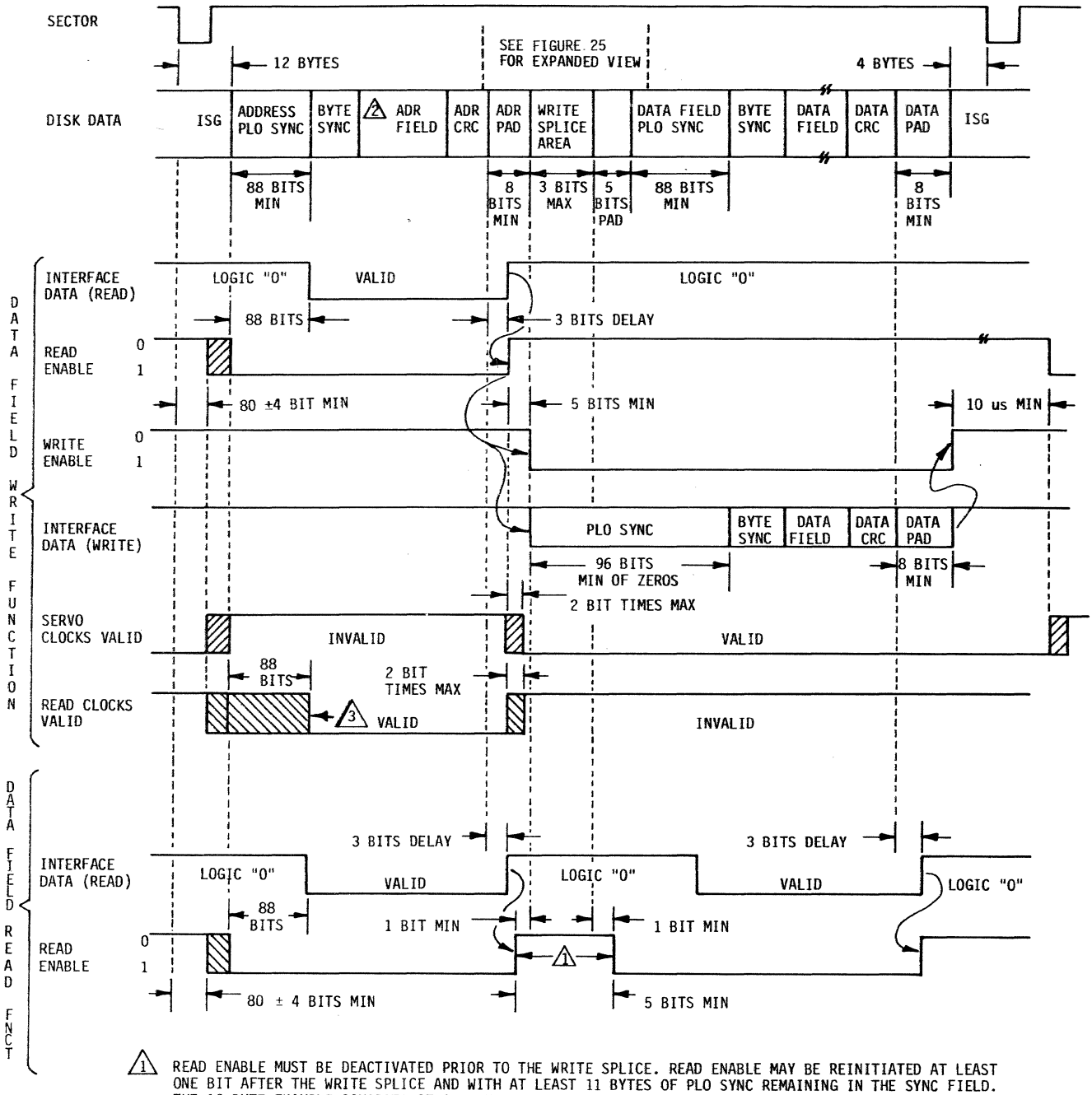
The read function consists of reading the address fields and then the data fields. The critical interface lines associated with a read function are the Sector (Index) pulses, Read Enable, Read Data, and Read Clock lines.

Address-Field Read (See Figures 24 and 25)

The location of the address field is defined relative to the sector (index) pulse. To recover the address field, the controller waits for the leading edge of a sector pulse. 80 ±4 servo clock periods after the leading edge of a sector pulse, Read Enable may be activated. The leading edge of Read Enable forces the phase-locked oscillator to synchronize on the PLO sync field. Read Enable also enables the read output of the data separator after frequency and phase synchronization is established.

Read Clocks will be in phase and frequency synchronization with the Read Data within 88 Servo Clock periods after the concurrence of Read Enable and the PLO Sync field. The Read Data lines will be a logic 0 until the first one bit of the byte sync pattern is detected. It is then the controller's responsibility to establish byte synchronization, perform the address field verification and interpret the address field check codes (CRC). Read Enable may be deactivated after the last bit of the address field check code is received by the controller and must be deactivated at least one bit prior to a Write Splice area.

For example, consider the data field read function shown in Figure 23. This example has a Write Splice area located on the disk one byte after the address field check codes (the creation of this Write Splice area will be explained in Section 15.3.2). An examination of the interface Data (Read) timing signal of Figures 24 and 25 reveals that the Interface Read Data is delayed by three bit times from data recorded on the media. Thus, to meet the requirement that Read Enable must be deactivated at least one bit prior to a Write Splice area requires that, for the format of Figure 24, Read Enable must be deactivated within four bit times after the reception of the last bit of the address-field check code by the controller.



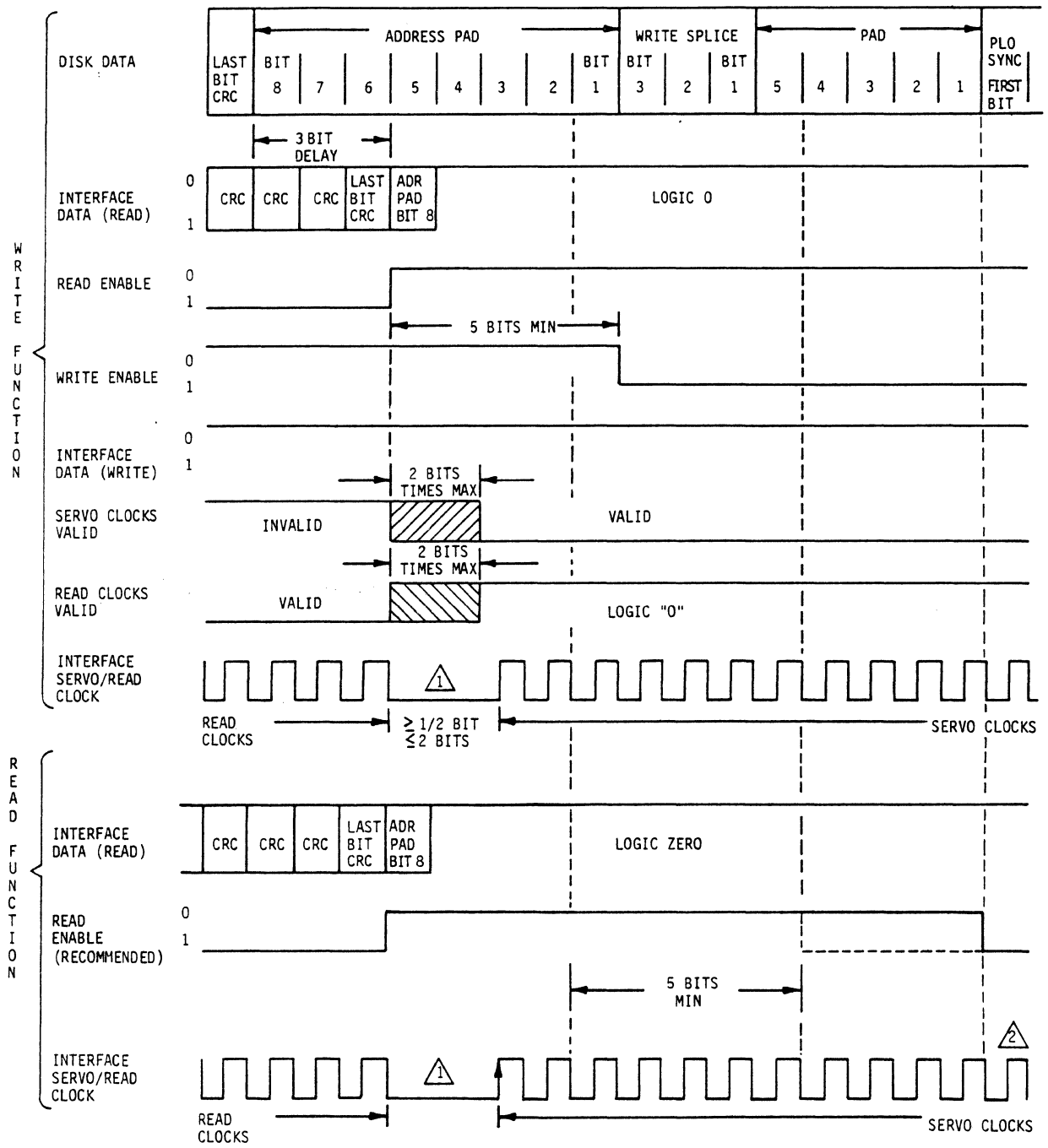
1 READ ENABLE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. READ ENABLE MAY BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD. THE 12 BYTE EXAMPLE CONSISTS OF ONE BYTE OF WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

2 THE ADDRESS FIELD INCLUDES THE TRACK, HEAD, AND SECTOR LOCATION.

G044a

3 READ CLOCKS ARE AVAILABLE BUT NOT PHASE AND FREQUENCY SYNCHRONIZED FOR 88 BITS.

Figure 24. Typical Read/Write Timing



1 WHEN READ ENABLE IS DEACTIVATED, THE INTERFACE SERVO/READ CLOCK LINE WILL CONTAIN VALID SERVO CLOCKS WITHIN ONE HALF OF A SERVO CLOCK PERIOD MINIMUM TO 2 SERVO CLOCK PERIODS MAXIMUM. THIS TRANSITION AREA WILL NOT CONTAIN ANY SHORTENED PULSE WIDTHS, BUT IT MAY CONTAIN NO TRANSITIONS FOR UP TO TWO CLOCK PERIODS MAXIMUM.

2 WHEN READ ENABLE IS ACTIVATED, THE INTERFACE SERVO/READ CLOCK LINE WILL CONTAIN SERVO CLOCKS UNTIL PLO SYNCHRONIZATION IS ESTABLISHED. THE TRANSITION FROM SERVO CLOCKS TO READ CLOCKS WILL BE ACCOMPLISHED IN THE SAME MANNER DESCRIBED IN NOTE 1 , i.e., NO TRANSITIONS FOR UP TO TWO CLOCK PERIODS MAXIMUM, ETC.

ZZ075a

Figure 25. Typical Read/Write Data - Expanded Write Splice Area

15.3.1 -contd.

The controller may compare the contents of the disk media recorded address field to the desired sector location as they are received from the drive. However, a valid comparison should not be assumed until the disk media recorded CRC check code verifies its correctness. If the recorded and desired address fields compare and no check-code error is detected, then the desired data area for either a data-field update or data-field read function has been found.

Data-Field Read (See Figures 24 and 25)

After the desired sector location has been found, the data field may be read. When a data field is updated, a three-bit-wide Write Splice area is created on the media. Read Enable must be deactivated a minimum of one bit time preceding a Write Splice area and may be activated a minimum of one bit after a Write Splice area.

For example, consider the format of Figure 24. To satisfy the Read Enable/ Write Splice timing requirements, Read Enable could be deactivated as soon as the last bit of the Address Field check code was received by the controller and activated 11 Servo/Read Clock periods later. The example chose to deactivate Read Enable as soon as the last bit of the address field check code was received (versus deactivating Read Enable four bit times after the last bit of the address-field check code) for timing compatibility with the data field update function which assumed this timing relationship to enable Write Gate and create the Write Splice area. The example also chose to activate Read Enable by counting 11 Servo/Read Clock periods. The 11 Servo/Read Clocks guarantee that 11 PLO sync bytes will be seen for read PLO synchronization and that the read Enable signal will be enabled at least one bit past the write splice. This counting of 11 Servo/Read Clocks to reactivate Read Enable also allows the Write Splice to be shifted two bit positions to the right of Bit 1 of the Address Pad and still guarantees that in the worst case, Read Enable was not activated until one bit time after a shifted write splice. This shifted write splice could occur if the controller counted five Interface Servo/ Read Clocks between the deactivation of Read Enable and the activation of Write Enable due to the one-half bit to two bits of no Interface Servo/Read Clocks when Read Enable is deactivated.

Refer to Figure 24. If Read Enable is activated after the Write Splice and at the beginning of the Data Field PLO Sync area, the interface Read Data lines will be valid within 88 servo clock periods. When Read Enable is activated, the Interface Servo/Read Clock line will contain Servo Clocks until Read PLO synchronization is established. After PLO synchronization is established the interface Servo/Read Clock line will switch from servo clocks to read clocks within two bit times. This transition area will contain no shortened pulse widths but may contain no transitions for up to two clock periods.

15.3.1 -contd.

Thus, within 88 servo clock periods from the start of a PLO sync field the controller may search for the Data field byte sync pattern, establish byte synchronization, and read the Data field and read and interpret the Data field check codes. Read Enable may be deactivated after the last bit of the Data field check code (Data CRC) is received.

Summary of Critical Read-Function Timing Parameters

Controller variations of the read timing are allowed if the following drive-dependent parameters are met:

1. Read Initialization Time

   A read operation may not be initiated until 15 microseconds following a head change.

2. Read-Enable Timing

   Requesting the drive to establish bit synchronization (that is, enabling Read Enable) for the address area should be done no earlier than 80 ±4 bits from the leading edge of a Sector (Index) pulse and at least 11 bytes prior to the address field byte sync pattern.

   Read Gate may not be enabled or true during a Write Splice area. (Read Gate must be deactivated one bit time minimum before a Write Splice area and may be enabled one bit time minimum after a Write Splice area.)

   NOTE

   Data (Read) at the interface is delayed by three bit times from the data recorded on the disk media.

3. Read Clock Timing

   Read Clocks and Read Data are valid within 11 bytes after Read Enable and a PLO sync field.

4. The Interface Servo/Read Clock line may contain no transitions for up to two Servo Clock periods for transitions between servo and read clocks. The transition period will also be one-half of a Servo Clock period minimum with no shortened pulse widths.

15.3.2 Write Function (Figures 24 and 25)

The Write function consists of reading the address field to verify the sector location, and then writing the Data Area PLO Sync characters, the Byte Sync pattern, the Data Field, the Data Field Check Codes (CRC) and a Data Field Pad byte. The critical interface lines associated with the write function are the Write Enable, Write Data, Write Clock, and Servo/Read Clock lines.

Read-Address Field Prior to Write

The address field and address field check codes could be read and verified prior to writing the data area, except while formatting.

Write-Splice Creation

A write-splice area is created on the disk media when the Write Enable signal is either activated or deactivated. A write splice area three Servo Clock periods wide is created due to write-drive turn-on time plus data-encoder turn-on delays. Figure 24 shows a write-splice area located between the address field and the data field. The creation of this write-splice area is as follows.

The write-splice area shown in Figures 24 and 25 was created at a location relative to the address field. Its location is defined by the following drive parameters:

1. Interface Data (Read) is delayed by three bit times from data recorded on the media.

2. Write Clocks must precede Write Enable by a minimum of two and one-half servo clock periods.

3. Servo clocks (used by the controller to create Write Clocks) may not be valid on the Servo/Read Clock lines until two servo clock periods after Read Enable is deactivated.

4. Read Enable and Write Enable may not occur simultaneously.

Thus, from Figures 24 and 25, if Read Enable were deactivated when the last interface data bit of the address field check code was received by the controller and Write Enable was activated five Servo Clock periods after Read Enable was deactivated, a Write Splice area on the media would be eight bit times from the last bit of the recorded address field check code. In addition, if Write Clocks were enabled, two Servo clock periods after Read Enable was deactivated, the drive requirement for Write Clocks to precede Write Gate by two and one-half Servo Clock periods would also be met.

15.3.2 -contd.

If the clocks available on the Interface Servo/Read Clock lines are used to count five servo clock periods from the deactivation of Read Enable to the activation of Write Enable, the Write Splice may be shifted two bit positions to the right of the first bit of the address pad. This is possible because the Interface Servo/Read Clock line may contain no clock transitions for up to two servo clock periods after Read Enable is deactivated.

Since the write-driver turn-on and data-encoder turn-on delay is three Servo Clock periods from the leading edge of Write Enable, the width of the Write Splice area recorded on the disk media will be three Servo Clock periods.

PLO Sync-Field Write

The PLO Sync Field must consist of 11 valid and recoverable bytes of interface data zeroes. From Figure 24, a five-bit pad area is shown between the three-bit splice area and the start of the Data Field PLO sync. This five-bit pad area allows Read Enable to be activated one bit after a Write Splice and be valid at the Drive Interface prior to the Data Field PLO sync bytes. Thus, to guarantee writing 11 valid bytes of PLO sync characters, allow for the Write Splice area, and allow Read Enable to be activated one bit time after a Write Splice but prior to an 11-byte PLO Sync Field, it is recommended that the controller transmit 12 bytes of zeroes after Write Enable is activated.

Byte-Sync, Data-Field, Data-CRC and Data-Pad Write

After the Data Field PLO sync field is written, a Byte Sync character should be written to enable the controller to establish byte synchronization for the data field.

After the Data Field is written, the Data Field check codes should be written followed by one Data Pad byte at the end of the check field to ensure proper recording and recovery of the check field codes.

After the Data Pad byte is written, the Write Enable should be deactivated and Read Enable should not be activated to read the address area of the next sector until 80 ±4 Servo clock periods after the next sector pulse is detected. This will allow ample time for the write-to-read recovery time (that is, the 10 microseconds minimum between the trailing edge of Write Enable and the leading edge of Read Enable).

With the four bytes of ISG preceding the Index pulse, a head change can be made after a sector update and read the next sequential header of the new track.

15.3.2 -contd.

Summary of Critical Write-Function Parameters

Controller timing variations in the record-update function are allowed if the following drive-dependent write (and interrelated read) timing parameters are met:

1. Read-to-Write Recovery Time. Assuming head selection is stabilized, the time lapse from deactivating Read Enable to activating Write Enable shall be five Servo clock periods minimum.

2. Write Clock-to-Write Enable Timing. Write Clocks must precede Write Enable by a minimum of two and one-half clock periods.

3. Write-Driver and Data-Encoder Turn-On From Write Enable. The write driver plus data-encoder turn-on time (write splice width) is three servo periods maximum.

4. Write-Driver Turn-Off From Write Enable. To account for data-encoding delays, Write Enable must be held on for at least one byte time after the last bit of the information to be recorded. (Refer to "Data Pad" in Figure 23.)

5. Write-to-Read Recovery Time. The time lapse before Read Enable can be activated after deactivating the Write Enable is 10 microseconds.

6. Head Switching Time. Write Enable must be deactivated at least 1 microsecond before a head change. Write Enable may not be activated until 5 microseconds after a head change command is received by the Drive.

7. Servo Clocks Valid Time. The Servo/Read Clock lines will contain valid Servo clocks within two Servo clock periods after the deactivation of Read Enable. Pulse widths will not be shortened during this transition time but clock transitions may not occur for up to two servo clock periods.

8. Write Encoder Delay. Interface data will be delayed a maximum of 4 bit times to the actual transitions recorded on the media.

TECHNICAL INQUIRY

FROM: NAME _____

_____

ADDRESS _____

CITY _____

STATE _____ ZIP _____

For additional information contact:

Control Data Corporation
10321 West Reno Avenue
Oklahoma City, OK 73130

ATTN: APPLICATIONS ENGINEERING OKM 154

DOCUMENT: TITLE/NUMBER/REVISION _____

_____

COMMENTS: _____

NO POSTAGE REQUIRED IF MAILED IN USA

FOLD, STAPLE & MAIL

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
Permit Number 1332
OKLAHOMA CITY,
OKLAHOMA

BUSINESS REPLY MAIL
No Postage Stamp Necessary If Mailed in the United States

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION

10321 West Reno Avenue

Oklahoma City, Oklahoma 73130

ATTN: APPLICATIONS ENGINEERING OKM154

FOLD

FOLD

CUT ALONG LINE