CONTROL DATA
CORPORATION

CONTROL DATA®
CYBER 70 MODELS 72/73/74
6000 COMPUTER SYSTEMS

INPUT/OUTPUT SPECIFICATIONS

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INTRODUCTION 1

This specification gives detailed operation and timing information for the data channels used on the CONTROL DATA® CYBER 70 Series (model 72, 73, and 74) and 6000 Series computers. Five distinctive types of data channels are used on the CDC CYBER 70 Series (model 72, 73, and 74) and 6000 Series computers: 6000/CDC CYBER internal, single rank 6000 external, double rank 6000 external, single rank CDC CYBER external, and double rank CDC CYBER external. The similarities and differences between these channels are discussed in this specification.

CHANNEL CHARACTERISTICS 2

Computer systems may include up to 20 separate peripheral processors, any one of which can exchange data with external equipment connected to the data channels. Each external equipment communicates with a data channel via a controller. Two types of cable signal transfers may be used, one-shot pulse transmission and static direct current level transmission. The one-shot pulse is used for all signal transfers between a data channel and a controller. A controller changes the one-shot pulse signals used by the data channel into signals required by the particular external equipment, and vice versa.

Each data channel has a 12-bit bidirectional register plus several bidirectional control designators that define the status of the register and the channel. Each data channel transfers 12-bit words at rates up to a maximum of one word every microsecond (a 1-megacycle transfer rate). All channels may be in operation at the same time. Pulse communication is used on all the data and control lines of a channel, and all lines are synchronized to the peripheral processor clock system.

A channel active designator is set from an internal source to reserve a channel for communication between a processor and controller. A channel inactive signal from an internal or external source clears the channel active flag to terminate communication.

A channel full designator is set from an internal or external source to indicate that a 12-bit data word has entered the channel register. An internal or external channel empty signal clears the full flag, which in turn statically clears the channel register.

The pulses on the data and control lines are one-shot, nonrepeated type transmissions, and all controllers must provide for storing the information. Other control includes two clock signals and one master clock signal for external devices. Clock signals are 10 megacycles (100-nanosecond period) and 1 megacycle (1-microsecond period).

Channel data and control lines are grouped into two cables, input and output. Refer to Figure 2-1 for 10 PPUs and Figure 2-2 for 20 PPUs. The output cable carries processor signals to the controller; the input cable carries controller signals to the processor and also carries the two processor clock signals to the controllers. Most devices on a channel connect to the data and control lines in a series-parallel scheme. Each controller samples the lines and may unconditionally relay all signals to the next in-line controller.† Each controller times the signal relay on the 10-megacycle clock signal from the processor so all controllers and the processors are synchronous and time-displaced from each other one or more clock periods.

DATA CHANNEL SIGNAL SPECIFICATIONS

The data channel cable signals are listed in Table 2-1. Separate output and input cables are used for each data channel. Each cable line originates and terminates at taper pins plugged into printed circuit module connectors. The cable lines have a maximum length of 75 feet.

A binary 1 voltage measured at the circuit terminals of the sending device is illustrated in Figure 2-3 and described in Table 2-2. No voltage is impressed on the line for a binary 0.

Input circuits in the external equipment must terminate the line in its characteristic impedance to minimize standing waves.

SIGNAL TIMING

All lines connecting the processor and external equipment controllers are synchronized to the data channel clock signals. Signal delay on the lines and through the controller hardware must be taken into account to keep the data exchange synchronous. Coaxial cable delay is calculated at 1.5 nanoseconds per foot. Refer to Figure 2-4.

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† This is not true in all controllers. For example, in the 6684 and 6681, function codes are not relayed when the converter is selected.

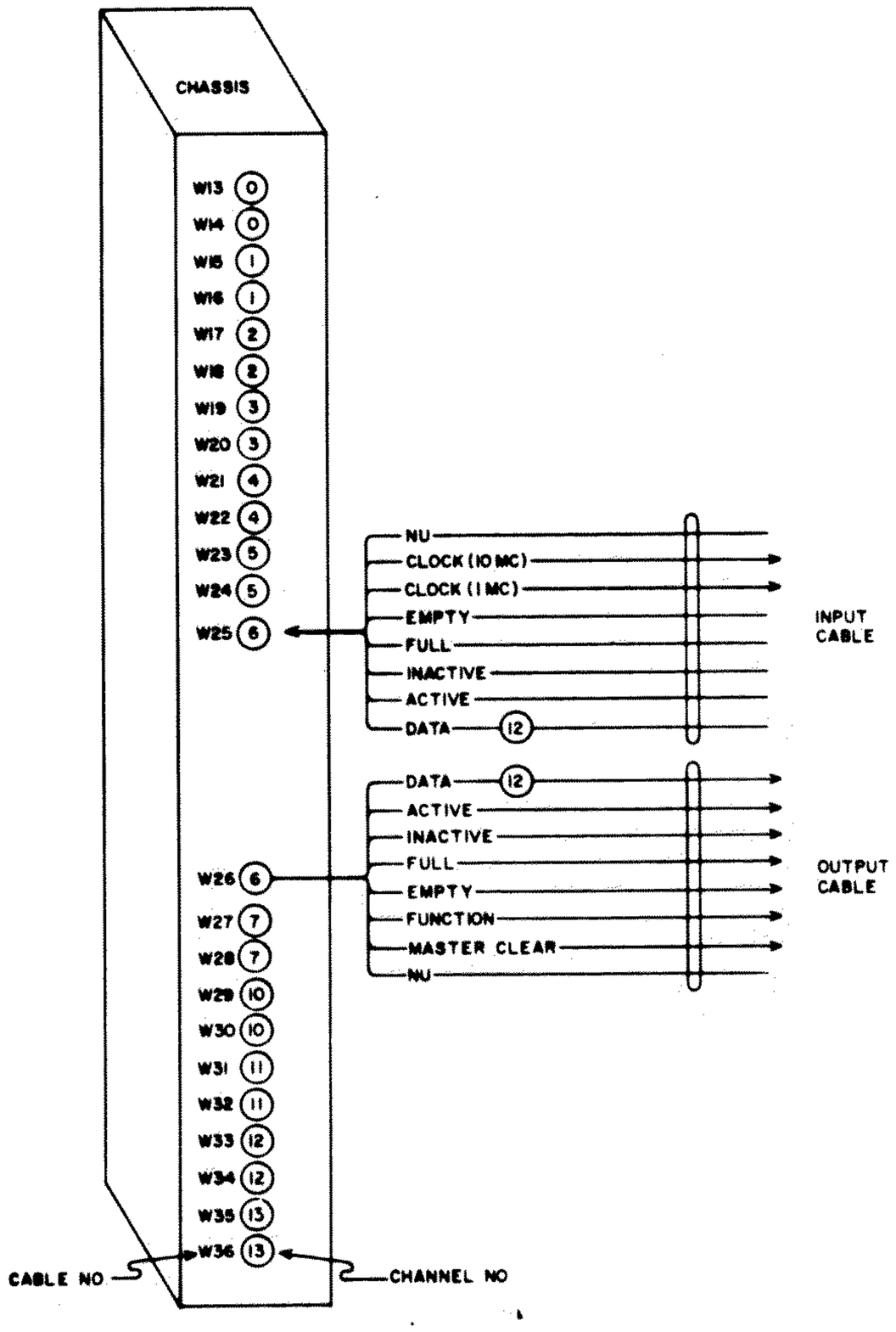


Figure 2-1. Internal Data Channels, Chassis 1

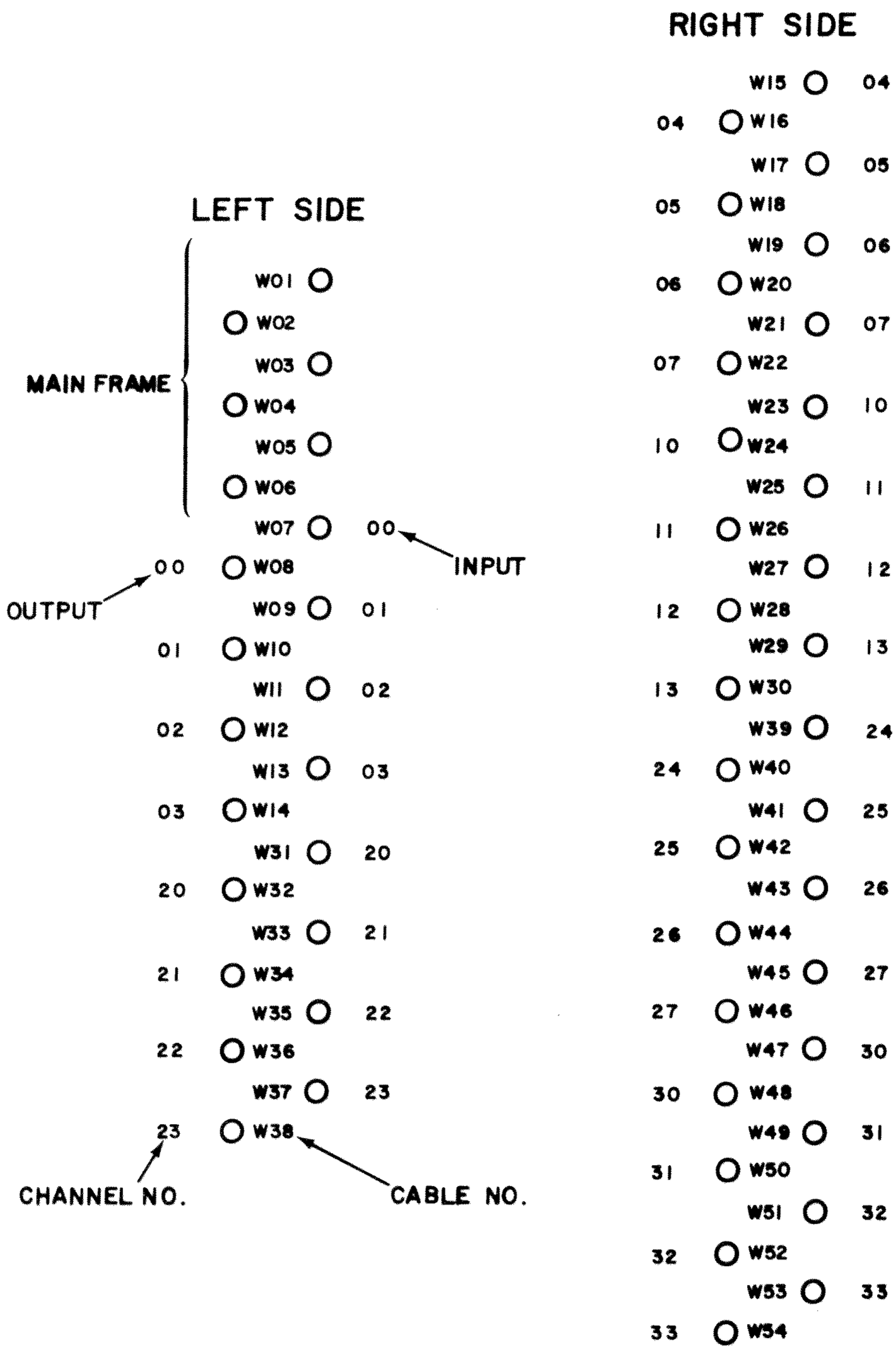


Figure 2-2. External Data Channels

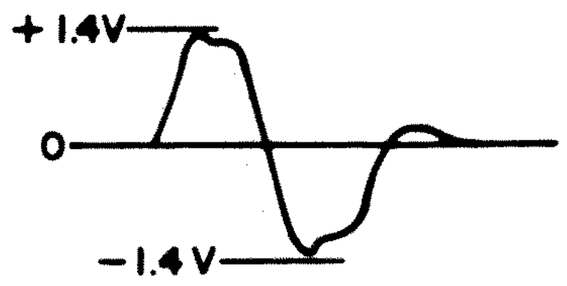


Figure 2-3. Line Voltage Waveform

TABLE 2-1. DATA CHANNEL COAXIAL CABLE LINES

Input Cable	Color Code	Output Cable
Data 2^0	90	Data 2^0
Data 2^1	91	Data 2^1
Data 2^2	92	Data 2^2
Data 2^3	93	Data 2^3
Data 2^4	94	Data 2^4
Data 2^5	95	Data 2^5
Data 2^6	96	Data 2^6
Data 2^7	97	Data 2^7
Data 2^8	98	Data 2^8
Data 2^9	99	Data 2^9
Data 2^{10}	900	Data 2^{10}
Data 2^{11}	901	Data 2^{11}
Active	902	Active
Inactive	903	Inactive
Full	904	Full
Empty	905	Empty
Clock (10 mc)	906	Function
Clock (1 mc)	907	Master clear
Not used	908	Not used

TABLE 2-2. LINE CHARACTERISTICS

Parameter	Description
Line maximum length	75 feet (typical CDC cable)
Pulse amplitude	1.8-volt peak at 19 milliamperes into 70 to 73 ohms coaxial cable at a signal rate of 1 megaHertz. The cable is terminated in its approximate characteristic impedance (Figure 2-3).
Rise time	5 nanoseconds
Fall time	5 nanoseconds
Line capacitance	21.5 picofarad/foot maximum (typical CDC cable)
Line attenuation	0.16 decibel/foot maximum
Voltage rating	30 volts maximum

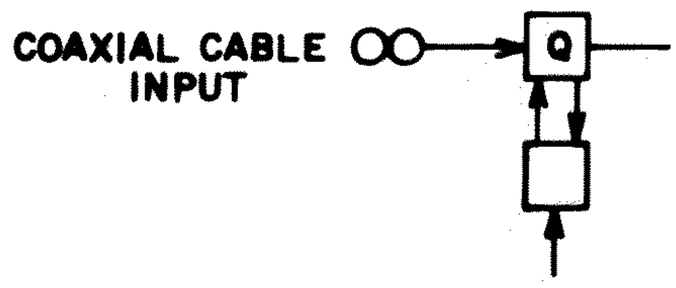
Synchronize the controller by adjusting the length of time that function signal is set in the controller input register. Use the relationship specified in Table 2-3 to determine how much the 10 MHz clock must lead the function signal. Adjust the time the input register is set to align the clocks between the controller and the processor as specified in Table 2-3.

Signal timing for all output signals and the requirements for the input signals are specified for the different types of data channels in Table 2-3.

Depending on external requirements, the 10-megacycle clock pulses can be used to generate a multiple phase clock for incremental gating signals. The 1-megacycle clock pulses are synchronous with the 10-megacycle clock and are an alternate clocking signal for gating or other purposes.

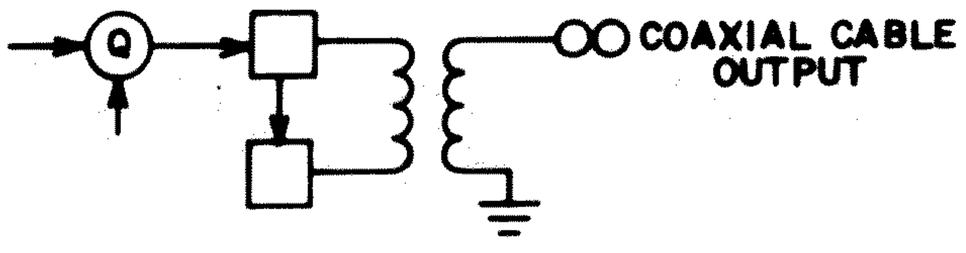
The master clear line is pulsed at 4096-microsecond periods as long as the DEADSTART switch on the computer deadstart panel is in the ON position or the DEADSTART button on the DD60 display console is pressed.

Typical Output Circuit



The output signals used in the data channel are: data (12 lines), function, full, empty, active, inactive, master clear, 10 MHz clock, and 1 MHz clock. The times in Table 2-3 are specified for the collector of transistor Q.

Typical Input Circuit



The input signals used in the data channel are: data (12 lines), full, empty, active, and inactive. The times in Table 2-3 are specified for the collector of transistor Q.

Figure 2-4. Measurement of Signal Timing

TABLE 2-3. SIGNAL TIMING SPECIFICATIONS

NOTE

All times specified in the table reference the computer mainframe clock. Refer to Figure 2-4 for places of measurement.

Parameter Description / Type of Channel	Distance 10-megacycle clock leads function (nanoseconds)	10-megacycle clock and 1-megacycle clock transmit time (pulse width of 25 nanoseconds)	Master clear transmit time (pulse width of 25 nanoseconds)	Output Control (full, active function, empty, inactive)		Output data		Distance full leads data on input (nanoseconds)	Input control signal leading edge (full, empty, inactive)	Minimum input signal pulse width (nanoseconds)
				Leading edge ±5 ns	Width	Leading edge ±5 ns	Width			
6000 internal	25	40	65	65	45	65	45	10 to 15	60 to 70	25
6000 external single rank (AT177-A)	15	45	65	60	25	45	45			
6000 external double rank (AT177-A)	15	45	65	60	25	75	25			
CDC CYBER 72/73/74 internal	25	40	65	65	45	65	45			
CDC CYBER 72/73/74 external signal rank	25	45	65	70	25	75	25			
CYBER 72/73/74 external double rank	25	45	65	70	25	75	25			

MAXIMUM RATE DATA TRANSFERS

The maximum data rate transfer is one 12-bit word every microsecond (a 1-megacycle transfer rate) in either direction.

The controller response time is specified by the following equation.

$$T - 2 [1.5X + 87 N] = Y$$

T	Maximum time for the controller response measured at the data channel
X	Total one-way coaxial cable length on data channel in feet
N	Number of controllers between the data channel and the controller concerned
Y	Maximum internal turnaround time necessary to respond to a full or empty signal during block data transfers

On outputs:

T equals 900 nanoseconds on the 6000/CDC CYBER 72/73/74 internal channels.

T equals 500 nanoseconds on the 6000/CDC CYBER 72/73/74 single rank external channels.

T equals 1000 nanoseconds on the 6000/CDC CYBER 72/73/74 double rank external channels.

On inputs:

T equals 900 nanoseconds for all channel configurations.

When the device is operating at the maximum internal turnaround time (Y), the timing considerations listed in Table 2-3 become extremely important. Incorrect signal timing retards the data channel transfer rate to one word every 2 microseconds. A recommended practive is to design at least 100 nanoseconds less than the maximum specified limit for Y.

SIGNAL RELAY

Signal relay is necessary in all controllers on a channel except in the one at the end of the line. Signal timing through the relay is at a 10-megacycle rate. Each controller appears as the processor to the next in-line controller except for a time lag. This time lag depends on the cable length and the internal circuitry for each synchronizer between it and the data channel. Each controller samples and stores all output signal lines in addition to sending them on to the next in-line controller.

Each controller also transfers all input signal lines on to the next in-line controller. In addition, the device must provide for entering its signals on the same lines. The network feeding the processor (or next in-line controller) is thus an OR combination of a controller and the one feeding it.

Computation of cable time and signal delay time through internal hardware allows a controller to place the signals on the lines for the relay to the next in-line controller at the same time relative to the processor, but later by an integral multiple of clock (10 megacycles) periods. Thus, each controller appears as the processor to the one next in line.

DATA INPUT SEQUENCE

An external device sends data to the processor by way of the controller in the following manner (refer to Figure 2-5).

1. The processor places a function word in the channel register and sets the full flag and the channel active flag. Coincidently, it sends the word and a function signal to all controllers. The function signal tells all controllers to sample the word and identifies the word as a function code rather than a data word. The code selects a controller and a mode of operation. Nonselected controllers clear; only the selected one is turned on.
2. The controller sends an inactive signal to the processor indicating acceptance of the function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.

3. The processor sets the channel active flag and sends an active signal to the controller which signals the device to start sending data.

4. The device reads a word and then sends the word to the channel register with a full signal which sets the channel full flag (10 to 15 nanoseconds before the data arrives).

5. The processor stores the word, drops the full flag, and returns an empty signal indicating acceptance of the word. The device clears its data register and prepares to send the next word.

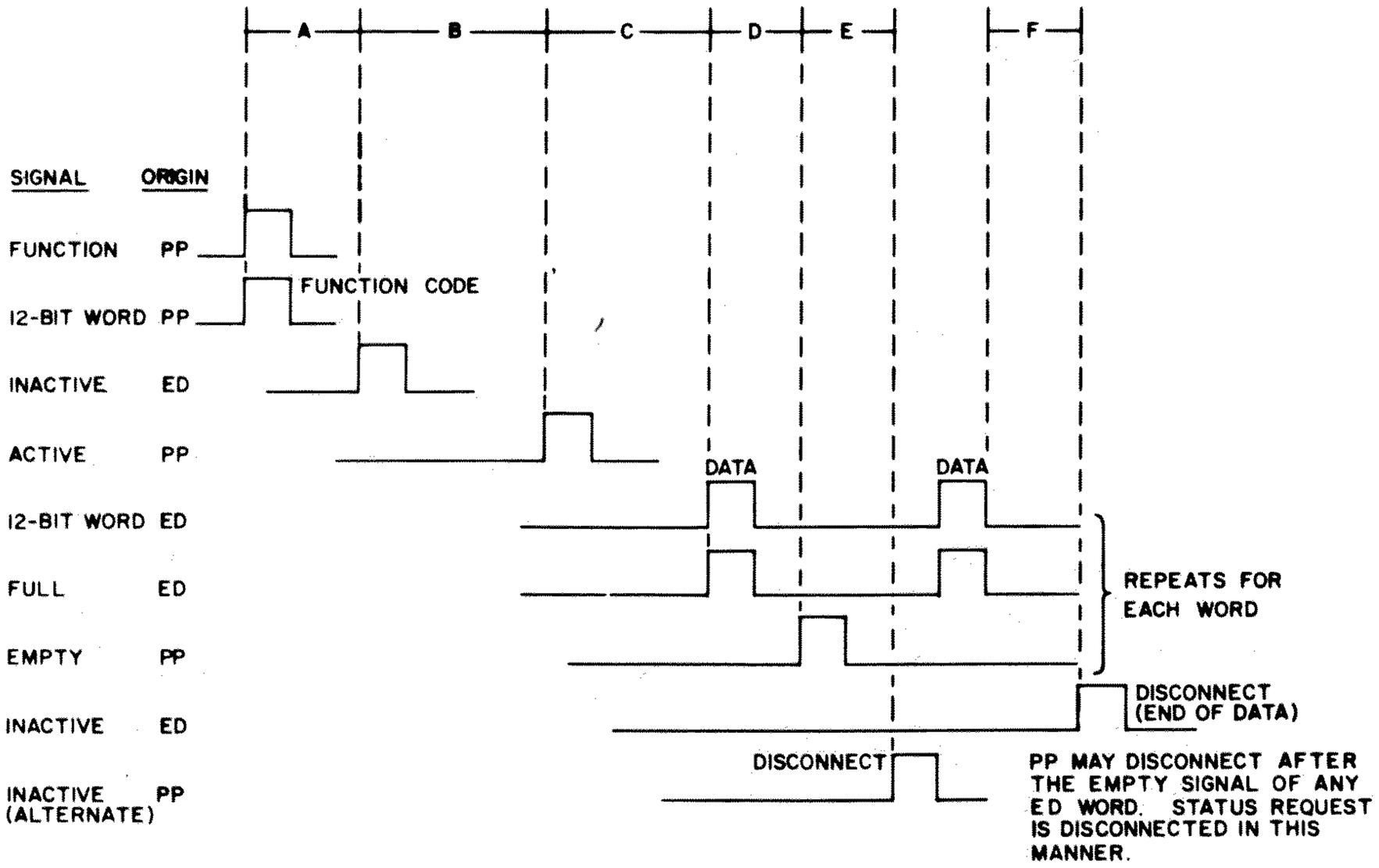
6. Repeat steps 4 and 5 for each word transferred.

7. At the end of the transfer, the controller clears its active condition and sends an inactive signal to the processor to indicate end-of-data. The signal clears the channel active flag to disconnect the controller and the processor from the channel.

8. As an alternative, the processor may choose to disconnect from the channel before the device has sent all of its data. The processor does this by dropping the active flag and sending an inactive signal to the controller which immediately clears its active condition and sends no more data, although the device may continue to the end of its record or cycle (for example, a magnetic tape unit continues to end-of-record and stop in the record gap).

STATUS REQUEST

A status request is a special one-word data input transfer in which an external device indicates a ready or error condition to a processor (refer to Figure 2-5).



PP = peripheral and control processor; ED = external device

A.	Time is a function of ED	PP recognizes inactive 1 microsecond after function or at an integral multiple thereafter.
B.	Time is a function of PP	Minimum time is 100 nanoseconds, actual time is a function of the PP program.
C.	Time is a function of ED	
D.	Time is a function of PP	Minimum time is 100 nanoseconds, maximum time is an integral multiple of 100-nanosecond intervals thereafter.
E.	Time is a function of PP	Minimum time is 3 microseconds, maximum time is an integral multiple of 1-microsecond intervals thereafter.
F.	Time is a function of ED	10 to 15 nanoseconds to allow the full signal to remove the clear on data input receivers.

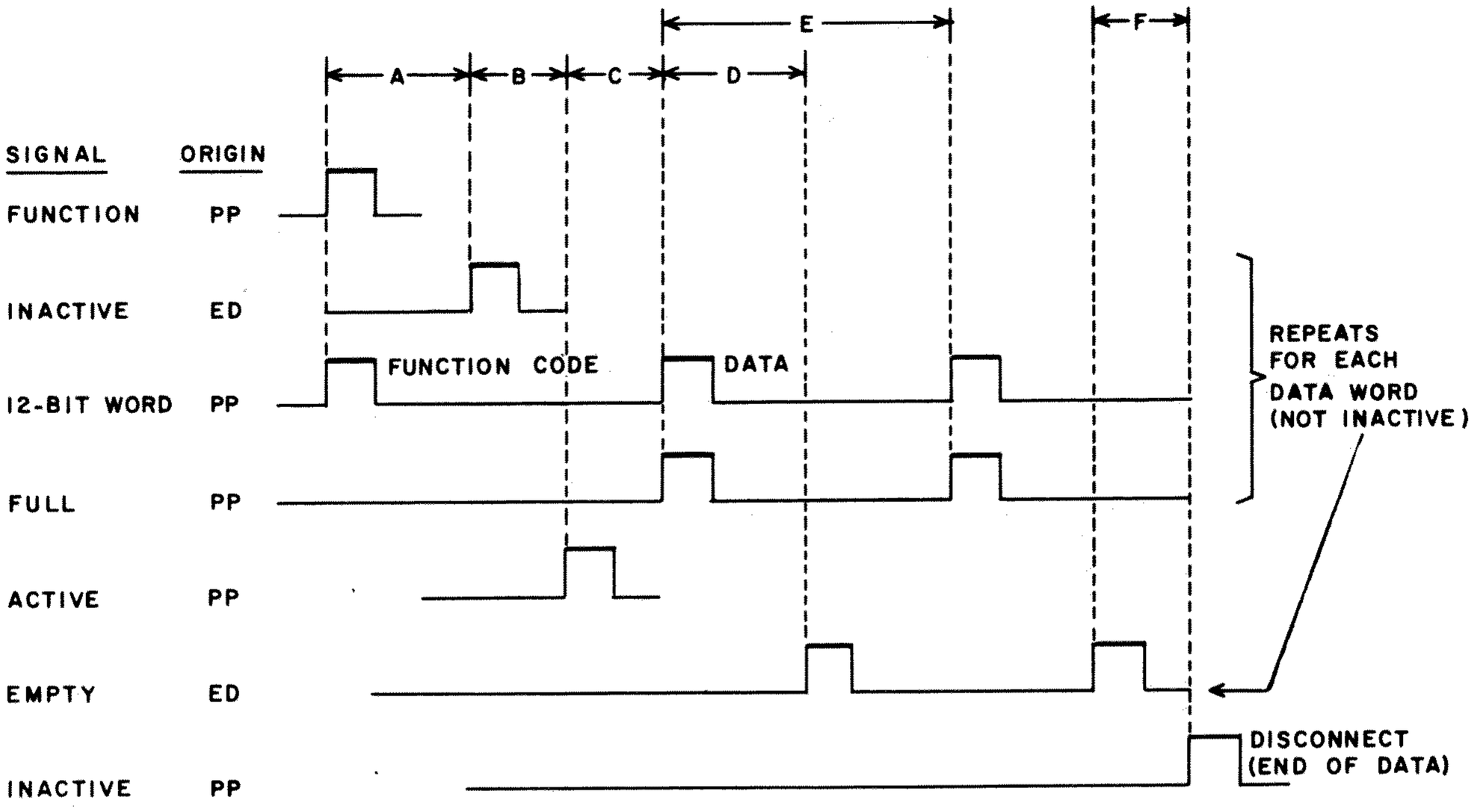
Figure 2-5. Data Input Sequence, Data Channel

1. The processor places a function word in the channel register and sets the full flag and the channel active flag. At the same time, it sends the word and a function signal to all controllers. The function signal tells all controllers to sample the word and defines the word as a function code rather than a data word. The code selects a controller and places it in status mode. Nonselected controllers clear; only the selected one is turned on.
2. The controller sends an inactive signal to the processor indicating acceptance of the status function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.
3. The processor sets the channel active flag and sends an active signal to the controller which signals the device to send the status word.
4. The controller sends the status word to the channel register with a full signal which sets the channel full flag (10 to 15 nanoseconds before the data arrives).
5. The processor stores the word, drops the full flag, and returns an empty signal indicating acceptance of the word.
6. The processor drops the channel active flag to disconnect the channel and sends an inactive signal to the controller to disconnect it.

DATA OUTPUT SEQUENCE

The processor sends data to an external device in the following manner (refer to Figure 2-6).

1. Perform step 1 under Data Input Sequence in this section.
2. The controller sends an inactive signal to the processor, indicating acceptance of the function code. The signal drops the channel active flag which in turn drops the full flag and clears the channel register.
3. The processor sets the channel active flag and sends an active signal to the controller which signals the device that data flow is starting.
4. The processor places a data word in the channel register and sets the full flag. Coincidently, it sends the word and a full signal to the controller.



PP = peripheral and control processor; ED = external device

A. Time is a function of ED	PP recognizes inactive 1 microsecond after function or at an integral multiple thereafter.
B. Time is a function of PP	Minimum time is 100 nanoseconds, actual time is a function of the PP program.
C. Time is a function of PP	Minimum time is 2 microseconds or 4 microseconds depending on instruction, actual time is a function of the PP program.
D. Time is a function of ED	
E. Time is a function of ED	Minimum PP time is 1 microsecond.
F. Time is a function of PP	Minimum time is 2 microseconds after empty from ED

Figure 2-6. Data Output Sequence, Data Channel

5. The controller accepts the word and sends an empty signal to the processor where it clears the channel register and drops the full flag.

6. Repeat steps 4 and 5 for each processor word.

7. After the last word is transferred and acknowledged by the controller empty signal, the processor drops the channel active flag and sends an inactive signal to the controller to turn it off.

CONTROLLER/EQUIPMENT CONNECTIONS 3

TYPICAL CONNECTIONS

Controllers are connected to an associated data channel as shown in the typical configuration in Figure 3-1.

Several controllers may be connected to a common data channel provided none have identical select function codes.

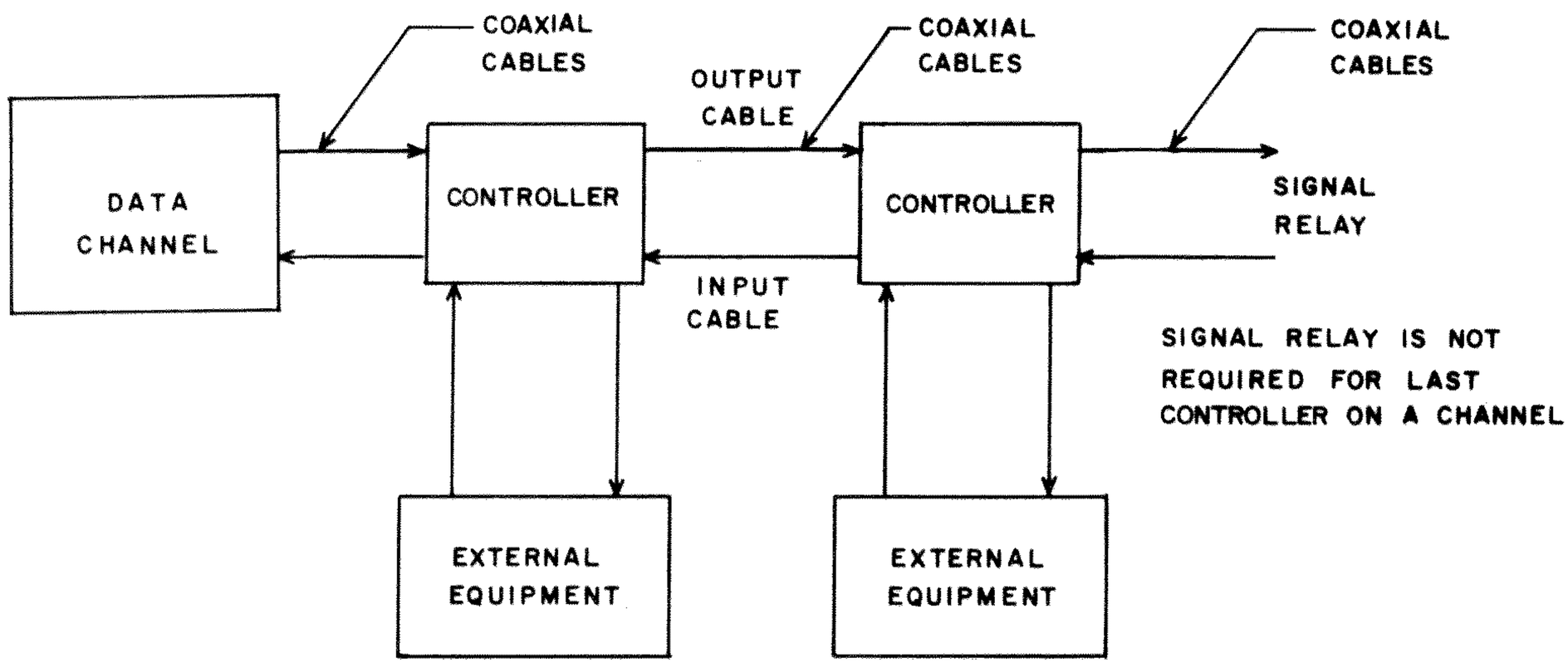


Figure 3-1. Typical Controller/Equipment Connections

SPECIAL CONNECTIONS

Two special equipment have a modified configuration. These are the 6681 data channel converter and the 6682/83 satellite coupler (refer to Figures 3-2 and 3-3).

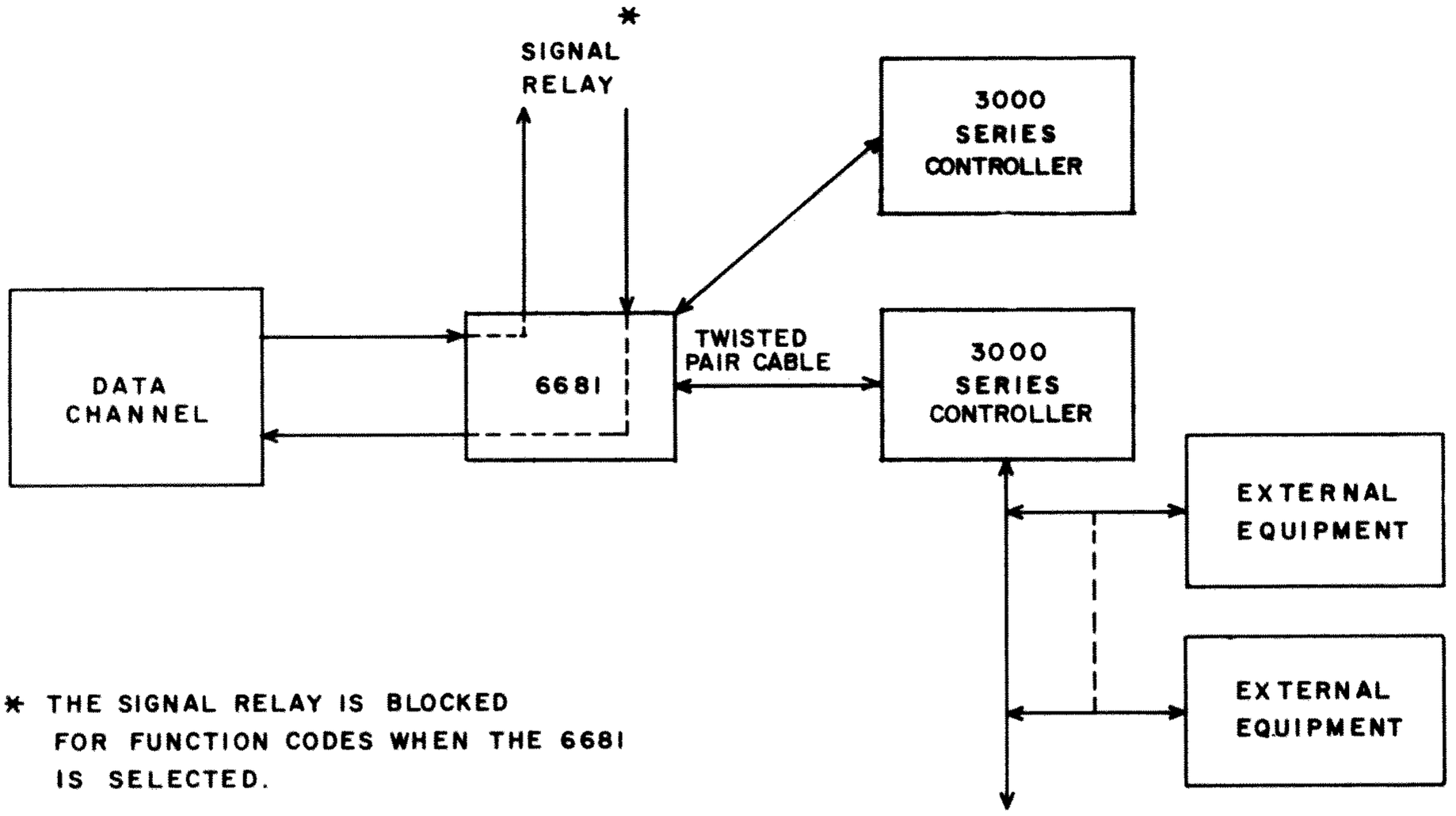


Figure 3-2. Typical 6681 Configuration

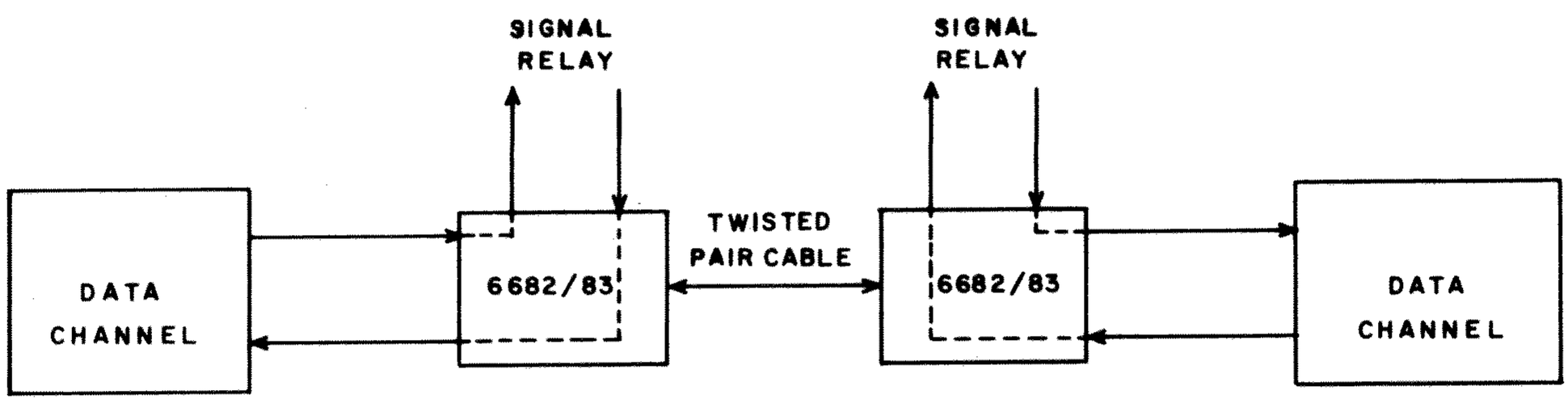


Figure 3-3. Typical 6682/83 Configuration

The 6681 may be selected by a select function code or by performing a master clear. The 6682/6683 and all other controllers may be selected by a select function code only.

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