74700900

CONTROL DATA CORPORATION

CDC® ASYNCHRONOUS COMMUNICATIONS LINE ADAPTER

DU 137-A

DU 189-A/B

DU 190-A/B

DU 191-A/B

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

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E 10/79	Revised to incorporate electromagnetic interference cable changes, and Engineering Change Orders 8246 and 8648, and Technical Action Request, 045640. Added configurations DY189-A/B, DY190-A/B, and DY191-A/B.

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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
DU137-A	01		
DU189-A	01		
DU189-B	01		
DU190-A	01		
DU190-B	01		
DU191-A	01		
DU191-B	01		

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PREFACE

This manual contains information on operation, maintenance, installation and checkout as well as relevant programming considerations for the CDC Asynchronous Communications Line Adapter DU137-A. The communications line adapter and associated cables are used within the 255X Network Processor Unit.

The DU137-A Communications Line Adapter (CLA) interfaces with different modems, according to the cable set to be selected. The DU189-A/B, DU190-A/B, and DU191-A/B CLAs each consist of a DU137-A circuit card and includes a preselected interface cable set.

The A version and B version 255X cabinets referred to in this manual are described in the system cabinets manual listed below.

The B version cabinets contain electromagnetic interference (EMI) protection.

The manual is intended for use by Customer Service engineers and presumes minimal knowledge of the 255X Network Processor Unit (formerly called host communications processor).

Preventive maintenance and fault isolation procedures to the circuit card level are given and card repair on-site should be limited to emergency conditions only.

The related publications listed below are available through the CDC Literature and Distribution Services, 308 North Dale Street, St. Paul, Minnesota 55103.

Publication Title	Publication Number
255X Network Processor Unit, Hardware Maintenance Manual	60472000
255X Network Processor Unit, Hardware Reference Manual	60472800
255X Host Communications Processor Site Preparation Manual	74641200
Loop Multiplexer and Card Cage DY200-A, DY197-A, Hardware Maintenance Manual	74873938
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INTRODUCTION

This section describes the physical and functional characteristics of the asynchronous communications line adapter (ACLA).

The ACLA is an asynchronous data conversion and control device which provides for the connection of asynchronous communications facilities to a communications processor.

PHYSICAL DESCRIPTION

An ACLA consists of integrated circuits and components mounted on an 11- by 14-inch (279.4 by 355.6 mm) circuit card as shown in figure 1-1. Two complete, identical ACLAs are contained on one card. The rear edge of the card contains two 102-contact tab connectors, extending the full length of the card. When the card is inserted in its card cage, these tab connectors engage the cage backpanel to provide signal paths between the ACLAs and their interfacing element in the multiplexing subsystem, the loop multiplexer.

The card is reinforced and protected with a metal frame which is riveted to the ACLA card. The front surface (card handle) provides an accessible mounting surface for the switches, indicators, cable connectors, and identification labels. The card handle when installed forms a cover to assure that cooling air is contained within the card cage. Two plastic ejectors on the handle facilitate removal of the card from the card slot.

Two pair of hexadecimal switches permit address selection of each ACLA and four signal indicators show when signals are passing through the ACLA. Two 25-pin connectors on the card handle provide the connection for ACLA-to-terminal/modem signal cables. Two toggle switches permit enabling or disabling of the input-available signal from the ACLA to the loop multiplexer.

All ACLA circuit cards are installed in a CLA and loop multiplexer card cage assembly, which also contains one or two loop multiplexer circuit cards, as shown in figure 1-2. The cage assembly provides 16 positions (card slots) for communications line adapters; an ACLA may reside in any position. Figure 1-3 shows the placement of ACLAs in a 2550 Series Network Processor Unit (NPU).

Figure 1-4 illustrates the use of a communications line expansion (CLE) unit. When more than 16 CLA cards are required or the number of communications lines exceeds 32, a CLE unit may be used. The first CLE is used for expansion beyond 16 cards or 32 lines. A second CLE allows expansion beyond 32 cards or 64 lines with a third CLE permitting expansion to 64 cards or 128 lines. Each CLE consists of one or two loop multiplexers and required power and cooling assemblies.

ACLA CHARACTERISTICS

A summary of the physical specifications for the ACLA are given in table 1-1. Nonoperating environmental requirements for the ACLA are given in table 1-2, and operating environmental requirements are listed in table 1-3.

SYSTEM APPLICATION

The loop multiplexer, multiplex loop, multiplex loop interface adapter, and all of the CLAs make up the multiplexing subsystem. The multiplexing subsystem hardware elements function as follows:

- Communications line adapters (CLAs) provide data conversion and control between the loop multiplexer and communications lines that are connected to the customer-supplied terminals or modems.
- The loop multiplexer provides a multiplexed path between a group of CLAs and the multiplex loop.
- The multiplex loop interconnects several loop multiplexers and the MLIA, residing in the communications processor.
- The multiplex loop interface adapter (MLIA) provides the hardware interface between the multiplex loop and the processor.

A sample system application is shown in figure 1-4, which is for illustrative purposes only; it does not necessarily represent a typical nor practical configuration.

FEATURES

HALF- AND FULL-DUPLEX OPERATION

The ACLA can be operated in either the half- or full-duplex mode. The request-to-send function is under program control. For half-duplex operation, it can be turned on

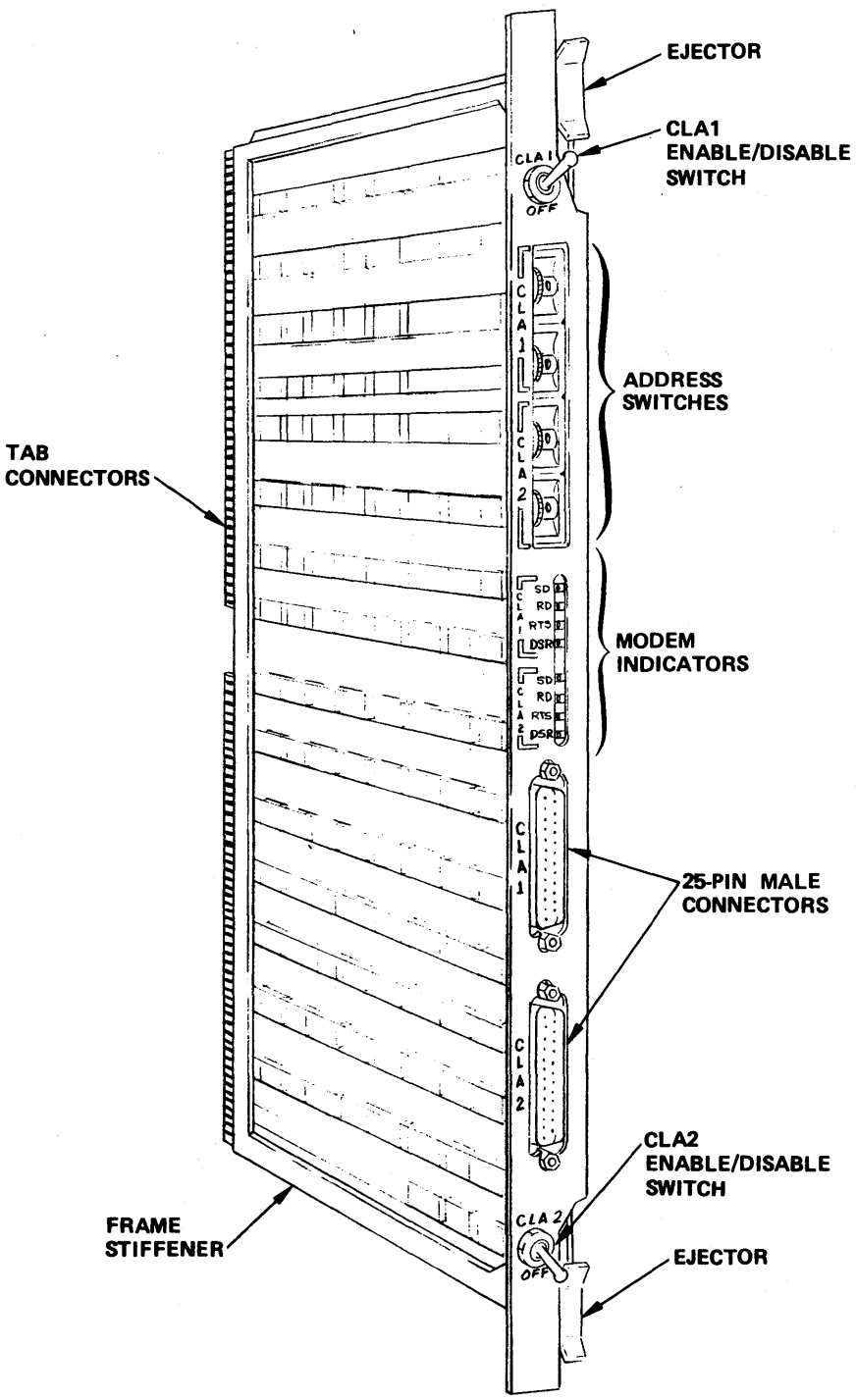


Figure 1-1. ACLA Circuit Card

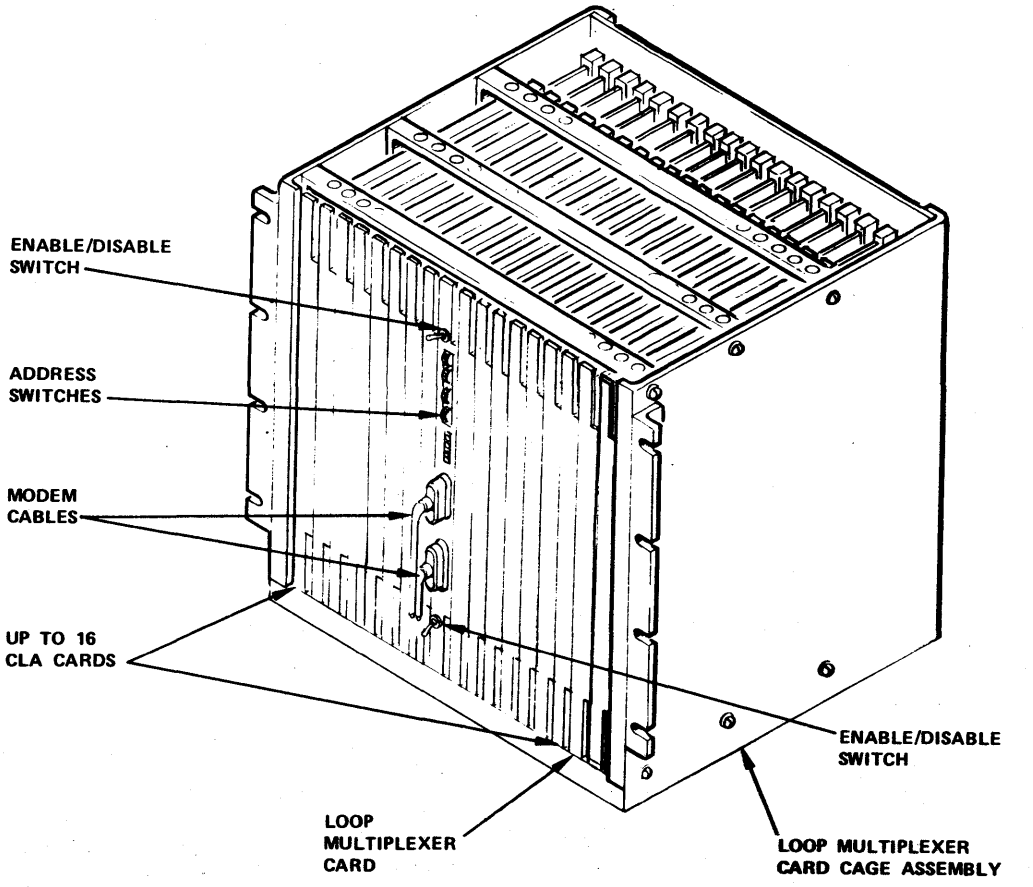


Figure 1-2. ACLA Card Placement

or off independent of other ACLA commands to switch the modem between transmit and receive modes. Also, the input section can be disabled while in transmit mode to avoid receiving back what is being sent. For full-duplex operation, a request-to-send signal is generally left on by program control and the input section continuously enabled.

CODE LENGTHS

The ACLA can receive or transmit 5-, 6-, 7-, or 8-bit characters. A parity bit may also be added. Stop bit duration can be 1, 1.5, or 2 units in length. Character length, parity bit, and stop bit duration are all selected by program commands.

CHARACTER PARITY GENERATION/DETECTION

As a software option, the ACLA can be commanded to check input for and generate output with odd, even, or without character parity. When a character is received with incorrect parity, parity-error-status is sent to the processor coincident with the character.

AUTOMATIC ANSWERING

The ACLA may be used with modems capable of automatic answering. Upon receipt of a call, the local modem sends a ring-indicator signal to the ACLA, which in turn reports ring-indicator status to the processor. If the software had previously activated data-terminal-ready (DTR), the modem answers the call after one ring. If DTR is not on, the modem does not answer the call until the software issues a command to turn on DTR. Thus, the software may precondition DTR on and calls are answered when received, or DTR can be left off and the software decides, upon receipt of ring-indicator status, whether to answer the call or not.

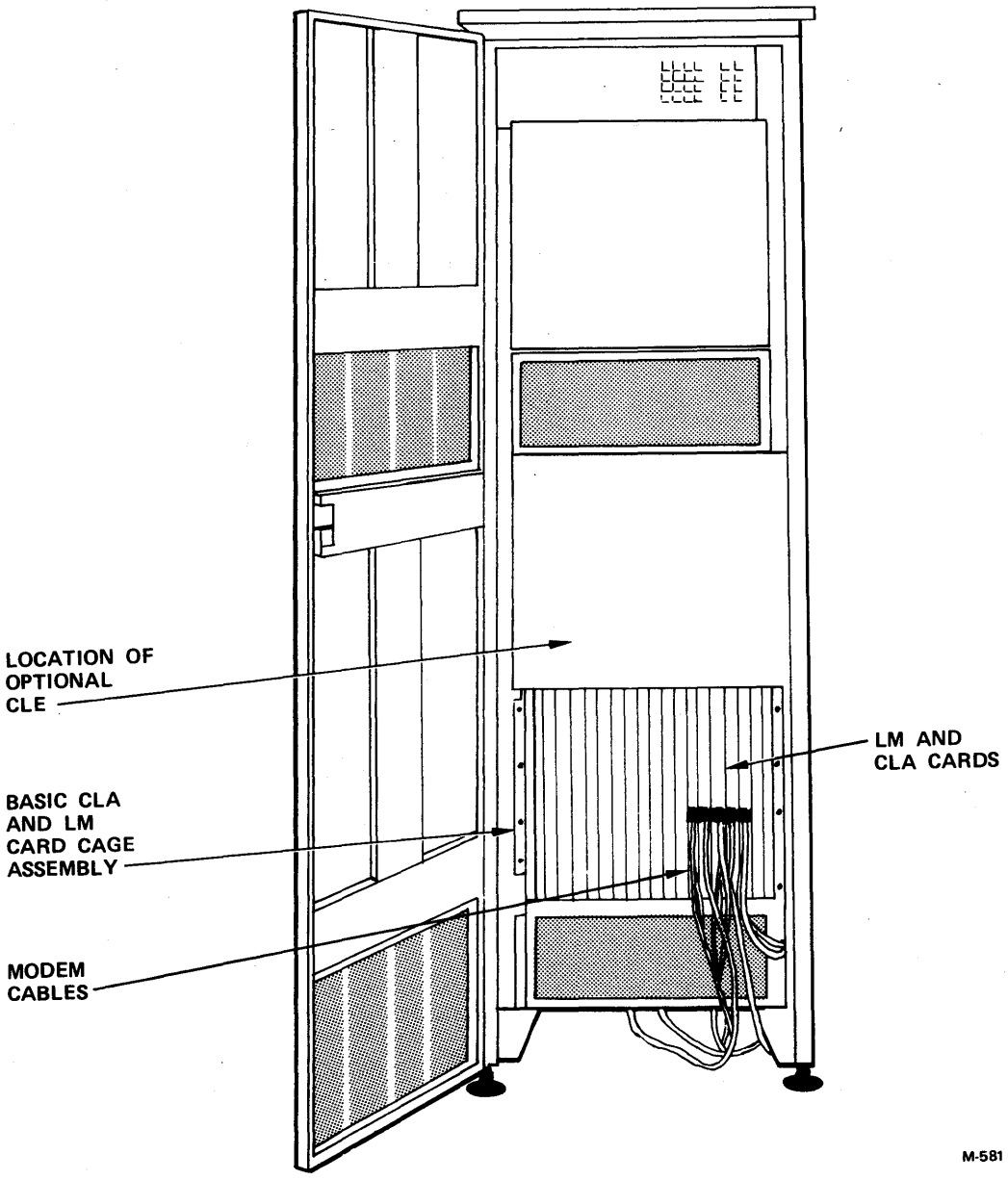
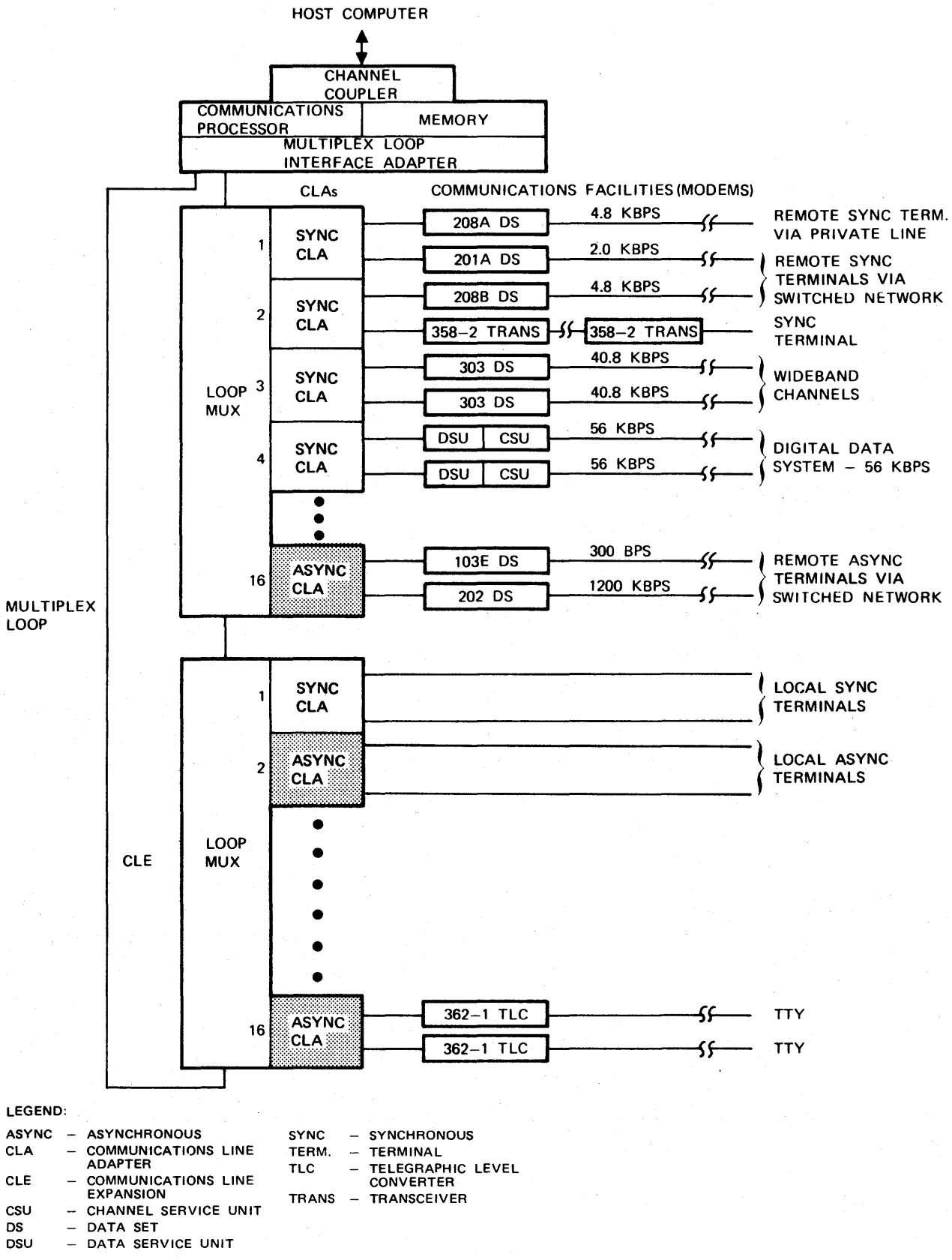


Figure 1-3. Location of CLA and LM Card Cage in NPU Cabinet



LEGEND:

ASYNC	– ASYNCHRONOUS	SYNC	– SYNCHRONOUS
CLA	– COMMUNICATIONS LINE ADAPTER	TERM.	– TERMINAL
CLE	– COMMUNICATIONS LINE EXPANSION	TLC	– TELEGRAPHIC LEVEL CONVERTER
CSU	– CHANNEL SERVICE UNIT	TRANS	– TRANSCEIVER
DS	– DATA SET		
DSU	– DATA SERVICE UNIT		

Figure 1-4. NPU System Application

TABLE 1-1. PHYSICAL CHARACTERISTICS

Characteristics	Value
Dimensions	
Length	14 in. (356 mm)
Width	11 in. (279 mm)
Thickness	
with card handle	0.9 in. (23 mm)
card only	0.063 in. (1.6 mm)
Weight	1.6 lb (0.73 kg)
Power Requirement	
Consumption	13.6 watts
Logic voltages	+5.0 ±0.25 V 2.00 amp; +12.0 ±0.50 V 0.15 amp; -12.0 ±0.50 V 0.15 amp

TABLE 1-2. NONOPERATING ENVIRONMENTAL REQUIREMENTS

Parameter	Requirement
Altitude	1000 ft (305 m) below sea level to 15,000 ft (4575 m) above sea level
Temperature	-30°F to +150°F (-35°C to +66°C)
Thermal Shock	+80°F to -30°F (+27°C to -35°C) or +80°F to +150°F (+27°C to +66°C) (rate of change not to exceed 20°F (11.1°C) per hour)
Humidity	5% to 95% (no condensation)
Shock	18 impacts of 5g ±10% for a duration of 11 ±1 msec, with a maximum g occuring at 5.5 msec.
	3 impacts in each direction along 3 major axes
Vibration	Peak displacement ±0.005 in. at 5 to 60 Hz, and acceleration of 2g at 60 to 500 Hz as packed for shipment

TABLE 1-3. OPERATING ENVIRONMENTAL REQUIREMENTS

Parameter	Requirement
Altitude	1000 ft (305 m) below sea level to 6000 ft (1830 m) above sea level
Temperature	Recommended: +72°F (+22°C) (ambient temperature for 255X Series system)
Humidity	Continuous operation at 90% relative humidity and 104°F(40°C). No operational condensation requirements. Excursion rate: not to exceed 10% per hour
Particulate Contamination	Range 3
Caustic Chemical Environment	Not allowed

SIGNALING RATE SELECTION

The ACLA can operate at any of the standard signaling rates: 75, 110, 134.5, 150, 300, 600, 1200, 2400, 4800, and 9600 baud. Other rates are also available. The signaling rate is selected by program command and can be different for transmit and receive.

RESTRAINT SIGNAL DETECTION

The ACLA provides the necessary interface for operating with an AT&T 811B Auxiliary Data Set used for TWX network connections. When the 811B detects a restraint condition from the TWX central office equipment, it activates a restraint-detection signal to the ACLA, causing the ACLA to suspend data transmission.

DATA TRANSFER OVERRUN

The ACLA generates data-transfer-overrun status bit if it assembles a new character before a previously assembled character has been transferred to the processor.

LOOPBACK TEST

On-line maintenance and checkout of the ACLA can be performed by use of the loopback test feature. When the ACLA receives a loop-internal-test (LIT) command from the processor, data from the output section is routed directly to the input section. Also, modem control signal lines (e.g., request-to-send) are routed back to appropriate modem status lines (e.g., clear-to-send). The loopback test mode allows testing of all ACLA sections except the modem interface (level conversion) circuits.

MODEM INTERFACE

The ACLA provides full interface with EIA RS-232-C and CCITT Recommendation V.24 standard signal levels at variable speeds. In addition to the normal data signals, the following control signals are accommodated:

- Request to send
- Clear to send
- Data set ready
- Data terminal ready
- Data carrier detector (Received line signal detector)
- Ring indicator
- Restraint detector
- Originate mode
- Local mode
- Secondary request to send
- Secondary data carrier detector
- Terminal busy

FUNCTIONAL DESCRIPTION

OPERATIONAL CONCEPT

The ACLA is a functional element of a demand-driven loop multiplexing subsystem. Figure 1-4 shows the interrelationship of the other functional elements of the subsystem.

The multiplex loop gathers input data and status from, and distributes output data and control to, many communications line adapters (CLAs). CLAs gain access to the multiplex loop through a loop multiplexer. The loop multiplexer allows a group of CLAs to access the multiplex loop through a single attachment point. It is essentially a passive device.

Both ends of the multiplex loop terminate at the multiplex loop interface adapter (MLIA), a control unit attached to the processor's input/output and direct memory access channels. The MLIA controls the operation of the multiplex loop, and transfers data and supervision between the loop and the processor. For more detailed information on the operation of the multiplexing subsystem, refer to the 255X Series HCP/NPU Hardware Reference Manual.

The ACLA assembles data character in its input section and disassembles them in its output section. On input, it converts serial data to parallel data, assembling the serial data at the signaling rate of the communications facility and transferring the data to the loop multiplexer. On output the ACLA functions as a parallel-to-serial converter, receiving the data characters from the loop multiplexer and outputting them serially at the signaling rate of the communications facility. The data paths of the ACLA are shown in figure 1-5.

FUNCTIONAL SECTIONS

The ACLA consists of four functional sections: input, output, speed generators, and modem interface.

The input section receives serial data from the communications line and converts it to parallel format for input to the processor. The input section also monitors the data transfer process and communications facility (via the modem interface section) and reports status to the processor.

The output section converts parallel data from the processor to serial form for transmission to the communications line. The output section also accepts commands from the processor, which are used to control the data transfer process and communications facility.

The transmit and receive speed generators supply separate clock sources to the ACLA to operate at various baud rates. Each generator, under program control, can select one of four reference frequencies (provided by the loop multiplexer or special option) and divides it to produce the clock signals needed by the ACLA. All commonly used baud rates can be accommodated.

The modem interface section contains circuits that convert the electrical interface signals required by the communications facility (e.g., modem) to levels compatible with the internal ACLA logic. The ACLA interfaces with communications facilities that conform to EIA Standard RS-232-C or CCITT Recommendation V.24 interface standards and operates with modems compatible with AT&T 103, 113, and 202 Data Sets and CDC 358-1 transceiver. It operates at variable input and output speeds up to a maximum of 9600 bps.

Input Section

DATA INPUT

The input section of the ACLA may be set, via a command through the loop multiplexer, so that it ignores all inputs on the data line. Data assembly occurs only if the ACLA has received a command instructing it to monitor the input data line.

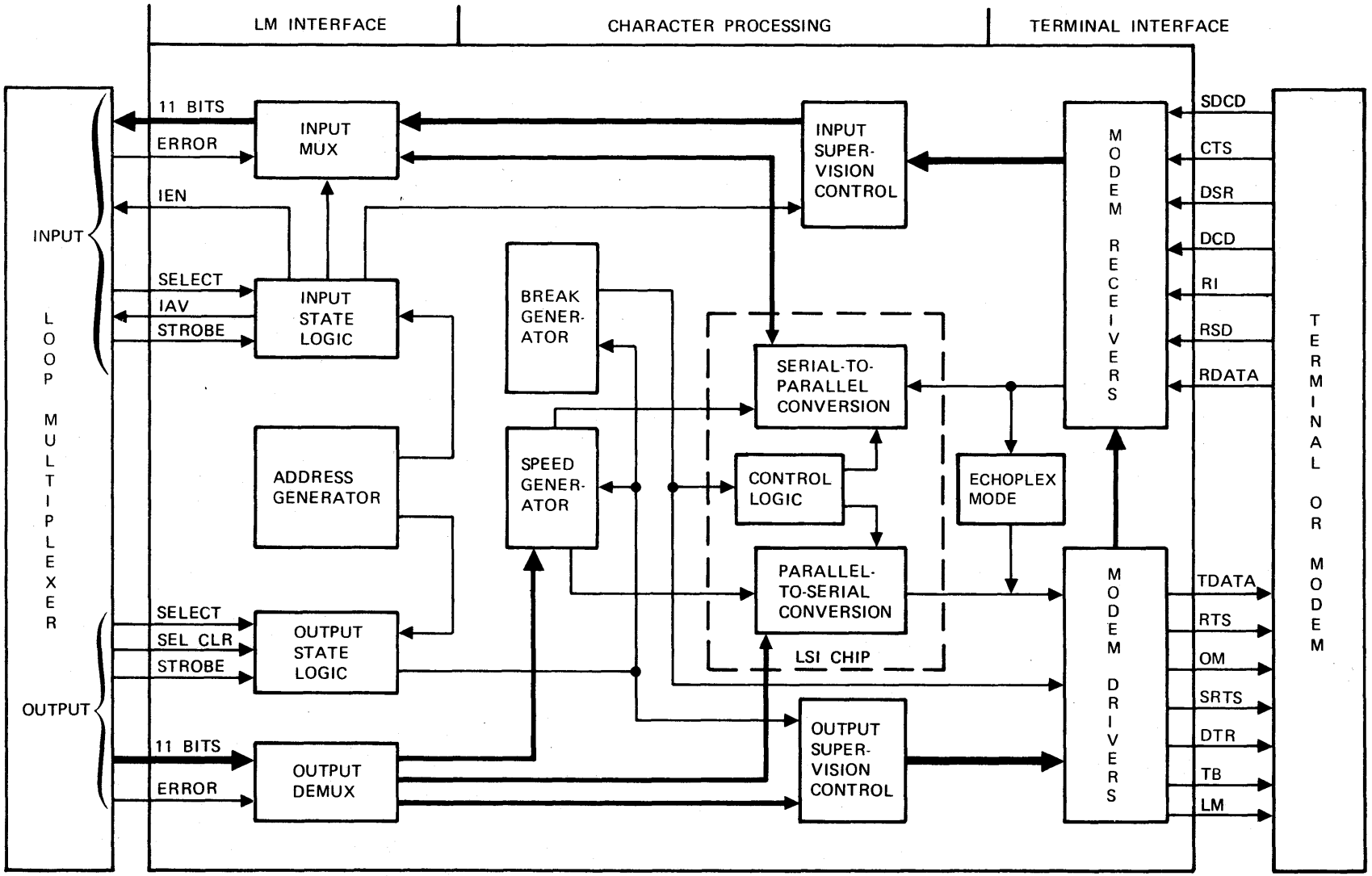


Figure 1-5. ACLA Block Diagram

Following initialization by the processor, the ACLA monitors the input data line for a mark (negative voltage) to space (positive voltage) transition. Upon detection of the mark-to-space transition, the ACLA initiates input character timing and ensures that a valid character start bit is present. If the input data line is found to be of a marking condition at one-half bit time after the beginning of the start bit, the ACLA resets its character timing and halts character assembly. If the data line is still at a spacing condition, the timing continues running until the incoming data character is assembled and transferred to the storage buffer in preparation for transfer to the loop multiplexer. At this time, the ACLA sets input available (IAV) which notifies the loop multiplexer that data is ready to be accessed. The ACLA does not transfer the received parity bit to the loop multiplexer when checking parity, but does transfer all bits received when not checking parity.

INPUT ERROR CONDITIONS

The ACLA uses three methods of error checking to ensure the integrity of the incoming data. This is to insure that no data is lost or transferred in error without a report being made to the software. Via command from the processor, the ACLA can be instructed to check for either even or odd character parity or to ignore character parity. Upon detection of a character parity error, input-available signal to the loop multiplexer is set and the parity-error-status (PES) bit is set to a 1 in the status buffer.

The second method of error checking is the framing error which is also used to detect a break condition. To assure that the incoming character is valid, the ACLA checks to see if a valid stop bit is present. If the data line is at spacing condition in the middle of the first stop bit, input-available to the loop multiplexer sets and the framing-error-status (FES) bit is set to a one in the status buffer. Following detection of a framing error, the ACLA ceases to record the information on the data line until it sees a mark-to-space transition on the data line. The data-line-monitor command from the processor can be used to force this condition. The break condition (one or more character-times of spacing) is detected by the reporting of a null character and framing error by the ACLA for each character time of break. To determine the length of the break condition, the program issues the data-line-monitor command to cause the ACLA to monitor the data line for one more character time. When a break condition has been determined to exist, the program may periodically interrogate the ACLA to determine the condition of the data line with the use of data-line-monitor. FES is monitored and reported regardless of the state of input-on signal as long as input-status-on is logic 1.

When assembling characters, a previously assembled data character is held in the transfer buffer until the next data character is assembled. If the character in the transfer buffer has not been accessed by the loop multiplexer by the time the new character is assembled, the previous character is erased and the new character set into the buffer; input-available is set and the data-transfer-overrun (DTO) bit is set to 1 in the status buffer. The input section does not store more than one data character.

Output Section

DATA OUTPUT

The ACLA output section receives commands and parallel data from the processor via the LM and transfers the data in serial form to the modem at a signaling rate determined by an internal timing source.

The output section of the ACLA is presented with an address and a select signal. If the address corresponds to the settings of the address switches, the ACLA recognizes commands and/or data received at the output bus.

Any combination of commands and data can be received by the ACLA; however, the ACLA can receive no more than one character at a time and process no more than two characters at a time. These commands must be contiguous.

Commands consist of the appropriate format bits and 8 bits of information. When a command is received, the 8 information bits are loaded into the command 1 register. In the same manner, the second, third, and fourth commands are stored in their appropriate registers. These commands are used to determine word length, parity, mode, and the state of the modem control lines.

Before the initiation of transmitting data, the ACLA must be programmed to include: 5, 6, 7, or 8 bits of data; even, odd, or inhibited parity; and 1 or 2 stop bits. Asynchronous transmission requires that the ACLA add a start bit to the beginning of each character and parity and stop bits to the end.

When the processor is ready to output data, it sends the output-on (OON) command to the ACLA. Upon receipt of the OON command and if CTS is active from the modem, the ACLA generates output-data-demand (ODD), which in turn causes input-available (IAV) to be set. The LM responding to the IAV, selects the input side of the ACLA, picking up the ACLA address with the ODD bit set, and forwards it to the processor. The processor reacts to this ODD by sending

the first data character to the ACLA. The ACLA is inhibited from generating ODDs if any one of the following conditions are met: clear-to-send (CTS) signal from the modem is inactive; restraint detector from the modem is active; or OON is inactive.

Data received by the ACLA is loaded into the transmitter holding register by the output strobe signal and then into the transmitter shift register in preparation for a serial transmission on the transmit data line. This transference of data from the holding register to the shift register causes an ODD to be generated, which is forwarded to the processor, informing the processor that the ACLA can accept another character. If another data character is not received by the ACLA before completion of the serial transmission of the character in process, the transmit data line remains in the marking condition.

ECHOPLEX MODE

Upon receipt of a command, the ACLA can route the data received from the modem back to the modem while accomplishing normal processing of the incoming data.

BREAK GENERATION

Following the receipt of a break command, the ACLA places the transmit-data line at a constant spacing condition. This condition continues until a command is received to turn break command to off.

LOOP ERROR DETECTION

The ACLA monitors two error lines from the loop multiplexer for the reporting of errors on the loop. One line indicates errors on the input loop while the other indicates errors on the output loop. The ACLA reports input error status if the input line toggles true during an input select or output error status if the output line toggles true during the output select.

CLA ADDRESSING

Each CLA may be one of 32 CLAs attached to the loop multiplexer backplane. In order to increase efficiency, many of the signals coming to the ACLA are bus organized. Because of this, each ACLA must be capable of generating an 8-bit address on input frames and recognizing the same 8-bit address on output frames. Figure 1-5 shows the data interchange between the ACLA and the loop multiplexer.

MASTER CLEAR

When the master-clear (MCL) signal originating at the LM attains a logic 1 condition, the ACLA is set to an idle state; all bits of command word 1, break and ISON bits of command word 2, and ECHO and LIT bits of command word 3 are set to a logic 0; in addition, the transmit and receive shift register, receive storage buffer, framing-error status, parity-error status, and data-transfer-overrun status are reset. The transmit-data line sets to a marking condition. Input-loop-error, output-loop-error status, and ODD are not reset. MCL must be active a minimum of 30 microseconds before the ACLA is guaranteed to be in the idle condition.

Modem Interface Section

The modem interface section of the ACLA provides the level conversion logic to make the ACLA compatible with the signal levels of the modem. This section of the ACLA also monitors the modem status lines for a change of condition: either a logic 1-to-0, or 0-to-1 transition. When a change occurs, status is reported to the processor. An exception of this procedure is that the ring-indicator signal only triggers a status report on a logic 1-to-0 transition.

Via command from the processor, the ACLA can route the transmit data back to the input data assembly logic to test the data handling logic. The ACLA also returns the modem control signals to the modem monitor lines to verify operation of the modem interface circuits. The ACLA displays the condition of four RS-232-C interface lines via lights located on the card handle.

Speed Generators

The receive and transmit sections of the ACLA require clock sources that have a frequency 16 times the desired baud rate. The ACLA provides a receive or a transmit speed generator that selects one of four clock frequencies, divides it by a predetermined number between 1 and 16, and applies the quotient to the respective receive or transmit section of the ACLA. The speed generators function identically but are controlled by the processor independently through use of command words 2 and 4.

This section provides information on control, setup, and operation of the ACLAs as well as program control. The format of address, data, status and command (supervision) information flowing through or used by the ACLA is treated and descriptions of the various status and command bits are included.

CONTROLS AND INDICATORS

The controls and indicators consist of four modem light-emitting diode (LED) indicators, two thumbwheel address switches and an enable/disable toggle switch for each ACLA. Each address switch has a total of 16 different positions (hexadecimal); thus each pair of switches can be set to a total of 256 (16 times 16) different settings. The numerals 0 thru 9 and the letters A thru F are used to display the 16 possible settings for each switch. The upper thumbwheel switch in each pair represents the most significant digit.

Functionally, the address switch settings are encoded as an 8-bit binary address. Each ACLA in the user's system must be set to a unique address by means of the address switches. The communications processor receives data from or transmits to an ACLA based on the setting of its address switches; this routing of data is independent of the location of an ACLA card in its card cage.

The CLA1 and CLA2 enable/disable switches, when in the OFF position, disable the associated ACLA. This effectively cuts off all input from the ACLA to the processor. The switches should be at OFF while address switches are changed if the card is plugged in and the system is operating. The switches are set to the on position only after the card has been inserted and the proper address selected. The names and functions of all ACLA switches and indicators are listed in table 2-1. The switches and indicators are shown in figure 2-1.

OPERATING PROCEDURES

Operation of the ACLA is automatic, and no operator action is required.

PROGRAMMING CONSIDERATIONS

The following programming reference information for the ACLA does not contain specific procedures for constructing an actual program. To prepare a program to control the ACLA requires detailed knowledge of the operation of the multiplexing subsystem elements, the multiplex loop interface adapter, multiplex loop, and loop multiplexer. The information required may be found in the network processor unit hardware reference manual.

TABLE 2-1. SWITCHES AND INDICATORS

Name	Display/Status	Function
Address switches	Two hexadecimal digits	Designation of ACLA at setting displayed in hexadecimal code (00 to FF). The top switch is most significant digit; bottom switch is least significant digit.
CLA(1 or 2)/OFF switches	OFF/on	Logical disconnection of the input-available signal to the LM from each ACLA
Modem indicator SD	Blinking/off	Blinking, indicates ACLA sending data to modem
Modem indicator RD	Blinking/off	Blinking, indicates ACLA receiving data from modem
Modem indicator RTS	Lighted/off	Lighted, indicates request-to-send from ACLA is active
Modem indicator DSR	Lighted/off	Lighted, indicates data-set-ready from modem is active

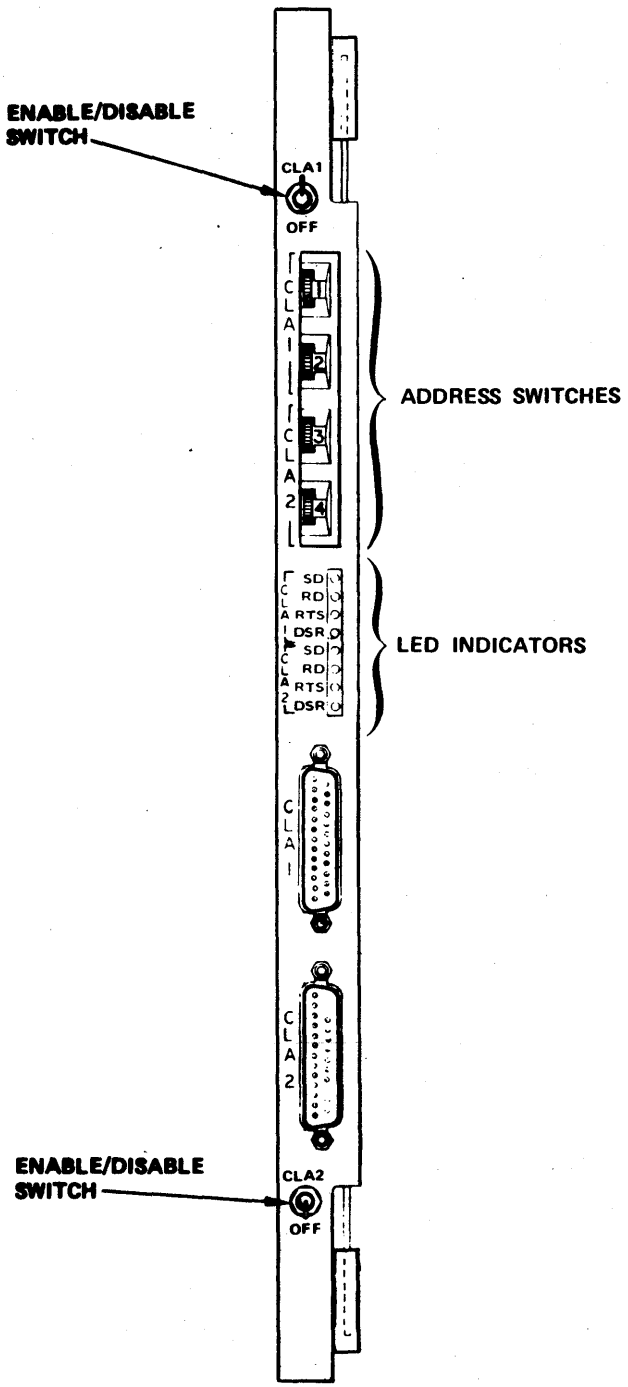


Figure 2-1. Controls and Indicators, ACLA Card Handle

MULTIPLEXING SUBSYSTEM OVERVIEW

The processor communicates with a CLA via the multiplex loop. The multiplex loop consists of two independent loops, the input loop and the output loop. The input loop carries output data demands, input data, and supervision (status) from the ACLA to the processor. The output loop carries output data and supervision (commands) from the processor to the ACLA.

Information is transferred serially bit by bit on the loops. Loop cell structure is shown in figure 2-2. Every twelfth bit is a cell frame marker that defines a 12-bit loop cell. The cell frame marker is followed by a cell identification field (three bits), which defines the contents of the remaining field (8 bits) of the cell. The loop multiplexer receives information from the output loop and presents the cells in parallel form to the CLA (an 11-bit interface is used; the cell frame marker bit is deleted). Similarly, the ACLA transfers cells (11 bits) to the loop multiplexer, which presents them serially (and adds the cell frame marker bit) to the input loop.

A line frame is a group of contiguous loop cells related to a particular ACLA. The first cell of a line frame contains the address of the CLA and the last cell contains a cyclic redundancy check (CRC) character. Other cells within the frame may contain data and/or supervision (status or commands). All cells are passed unmodified between the multiplex loop and the CLA, except the check character which is removed from the output loop and added to the input loop by the loop multiplexer.

LINE FRAME FORMATS

The ACLA uses the following general line frame format on the input loop:

ACLA Address	Input Data	Status Word 1	Status Word 2	CRC Character

The ACLA address cell is always present and may contain an active output data demand bit. The data cell may appear next and contains input data. Two supervision cells may also follow and contain status word 1 and status word 2. If any status is to be reported, both status words always appear. The CRC (cyclic redundancy check) character is added by the loop multiplexer and does not concern the ACLA.

The following general line frame format is required by the ACLA on the output loop:

ACLA Address	Output Data	Command Word 1	Command Word 2	CRC Character

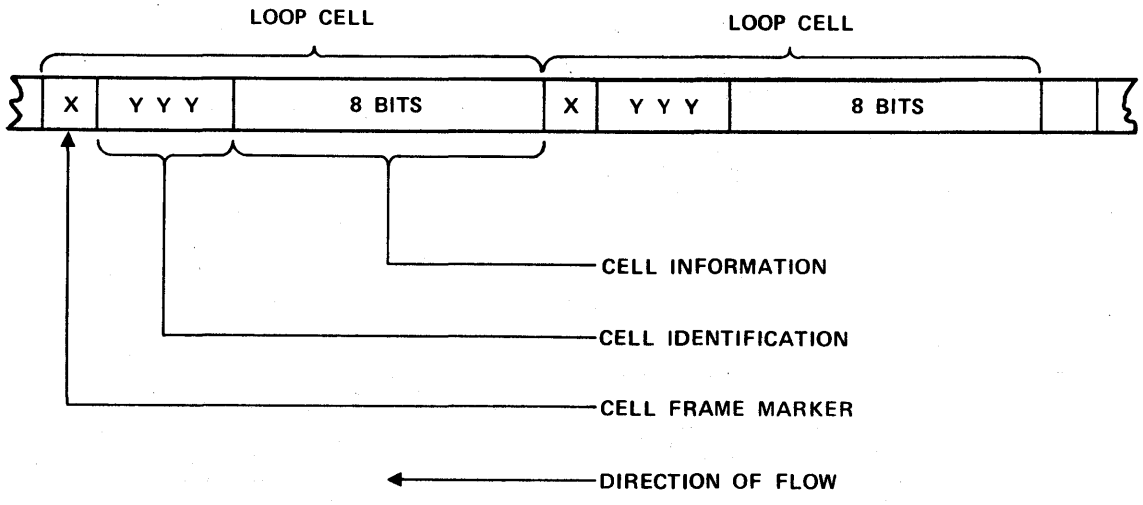


Figure 2-2. Loop Cell Structure

The ACLA address cell is always present. Either the data cell or command words may appear next. The data cell contains output data. From one to four supervision cells may appear and contain command words 1, 2, 3, and 4. Allowable combinations of command words are: none; 1; 1 and 2; 1, 2 and 3; or 1, 2, 3, and 4. The CRC character is removed by the loop multiplexer before being transferred to the ACLA.

CELL AND WORD FORMATS

The formats of the various word types used within the ACLA are presented in table 2-2. Processor word and loop multiplexer cell bit position identifications are shown in the table. These are for reference only and are of no real concern to the ACLA. Within the loop multiplexer and processor, each word consists of 12 bits. As noted earlier, however, bit position 0 of the LM is a cell frame marker used for loop timing. This bit is not employed within the ACLA as noted by each X in the table.

The rightmost 8 bits (I1 thru I8) of the LM cell contain information while the leftmost 3 bits (F1 thru F3) contain a code defining the type of information included in I1 thru I8. These codes, which are shown in the table, designate the information as the ACLA address, data, an ACLA status report to the processor, or a command from the processor.

Addressing Cell

Each ACLA is designated by a different 8-bit binary address, as set by the hexadecimal address switches on the ACLA card handle. Thus, when data, input-supervision, or output-data-demand signals are presented to the loop multiplexer from the ACLA, the first operation of the ACLA is to present its particular address.

Data or output supervision presented to the ACLA from the LM is preceded by an address. The ACLA compares this address with the internally preset address. If the two agree, the ACLA accepts the data or supervision. The addressing code format is shown in table 2-3. The mnemonics OF, IO, IF and II represent output format, information output, information format and information input, respectively.

In table 2-3 bit position IF3 is the output-data-demand bit in the address code. When the address is presented to the LM from the ACLA, the bit is a logic 1 if an ODD is present, and is a logic 0 if no ODD is present. This bit must be a logic 1 in an output loop address cell (OF3).

Address position A1 is the most significant bit and A8 is the least significant bit in the binary coded address.

Data Cell

The data cell transfers information into or out of the ACLA via the loop multiplexer. The data cell format is presented in table 2-4. Bit D1 is always the first bit received from or transmitted to the modem by the ACLA.

Supervision Cell

The supervision cell on output gives information to the ACLA in the form of commands. On input this cell gives information to the processor in the form of status words from the ACLA.

TABLE 2-2. CELL FRAME FORMATS

Word/Field Type	Bit Position												Flow
Processor Word	11	10	9	8	7	6	5	4	3	2	1	0	
LM Cell	0	1	2	3	4	5	6	7	8	9	10	11	
Information Field	X				I1	I2	I3	I4	I5	I6	I7	I8	
Identification Field	X	F1	F2	F3									
Address ID Field	X	1	1	†	← Address →								LM ↔ ACLA
Data ID Field	X	1	0	0	← Data →								LM ↔ ACLA
Status ID Field	X	1	0	1	← Status →								ACLA → LM
Command ID Field	X	1	0	1	← Command →								LM → ACLA

†This bit is the output data demand (ODD) during an address transfer to the LM.

TABLE 2-3. ADDRESSING CODE FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
ACLA to LM Interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
Bit Content		1	1	0/1	A1	A2	A3	A4	A5	A6	A7	A8

TABLE 2-4. DATA CELL FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
ACLA to LM Interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
8- or 9-bit† character		1	0	0	D8	D7	D6	D5	D4	D3	D2	D1
7-bit character		1	0	0	0	D7	D6	D5	D4	D3	D2	D1
6-bit character		1	0	0	0	0	D6	D5	D4	D3	D2	D1
5-bit character		1	0	0	0	0	0	D5	D4	D3	D2	D1

†For a 9-bit character the additional bit is a parity check bit. This is handled internally and does not appear at the ACLA/LM interface; consequently, only 8 bits are shown in this table.

STATUS WORDS

Most status changes, error conditions, or a status request command cause status to be reported, and two characters are sent to the processor. The status word 1 and status word 2 formats are shown in tables 2-5 and 2-6, respectively. In both tables a logic 1 indicates that the associated modem signal or status condition is active (on), and a logic 0 indicates that the condition is not active (off).

COMMAND WORDS

The command words are instructions from the processor in the form of command words 1, 2, 3 and 4, which must be received in sequence. For example, words 1 and 2 must be received before word 3, and word 2 must always be preceded by command word 1. However, command word 1 can be received as a single word command. Formats for command word 1 and command word 2 are shown in tables 2-7 and 2-8. A logic 1, in the position indicated, activates the associated signal, while a logic 0 deactivates the signal. The commands operate independently of each other.

TABLE 2-5. STATUS WORD 1 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
ACLA to LM Interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
Bit Content		1	0	1	CTS	DSR	DCD	RI	SDCD		ILE	OLE

CTS - Clear-to-send. This status bit indicates the state of the clear-to-send modem signal. When active, it indicates the modem is ready to accept data from the ACLA. It must be active to enable data output from the CLA. If this signal changes from a logic 1 to a logic 0 during character output, the current character is completed and the transmit-data line is set to marking condition. A change of state of this signal does not cause status to be reported.

DSR - Data-set-ready. This status bit indicates the state of the data-set-ready modem signal. When active, it indicates that power is applied to the modem and that it is connected to the communications line. Any change of state of this signal causes status to be reported.

DCD - Data-carrier-detect. This status bit indicates the state of the receive-line-signal-detect modem signal. When active, it indicates that a carrier signal is being received by the modem. Any change of state of this signal causes status to be reported.

RI - Ring-indicator. This status bit is set and status reported each time the modem ring-indicator signal goes from an on state to an off state. This indicates that the modem is receiving an incoming call from a remote station. The status bit is reset when the status words are sent to the processor.

SDCD - Secondary-data-carrier-detector or secondary-received-line-signal detector. This status bit indicates the state of the secondary data-carrier-detector signal from the modem. This signal is used to indicate circuit assurance status or to signal an interrupt. Any change of state of this signal causes status to be reported.

ILE - Input-loop-error. When set to a 1, the bit indicates that the LM has detected a loop error while the ACLA was using the input loop. This status is reset when the status words are sent to the processor.

OLE - Output-loop-error. When set to a 1, this bit indicates that the LM has detected a loop error while the ACLA was using the output loop. This status is reset when the status words are sent to the processor.

TABLE 2-6. STATUS WORD 2 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
ACLA to LM Interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
Bit Content		1	0	1	PES	DTO	FES					

PES - Parity-error-status. This status is generated when the ACLA has been instructed to check for even or odd character parity and a character is received with incorrect character parity. The status always appears in the same line frame as the character. This status is reset when the status words are sent to the processor.

DTO - Data-transfer-overrun. This status is generated by the ACLA when it has a data character that is ready for transfer to the LM before the LM has accepted the previously assembled character. The previously assembled character is lost. This status is reset when the status words are sent to the processor.

FES - Framing-error-status. This status is posted by the ACLA when a character is received from the modem without the presence of a stop bit. The status always appears in the same line frame as the character. This status is not reset until another character with proper stop bit is received.

NOTE

FES can be set independently of the state of the ION (input-on) command. The character received that caused FES is always transferred. See Programming Notes for use of FES in break detection.

TABLE 2-7. COMMAND WORD 1 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit Content		1	0	1	RTS	SRTS	OM	LMA	DTR	TB	ION	OON

RTS - Request-to-send. A logic 1 here activates the request-to-send line to the modem while a logic 0 deactivates RTS.

SRTS - Secondary request-to-send. A logic 1 activates the secondary request-to-send line to the modem (referred to as secondary send-data on some modems). On modems equipped with a reverse channel transmitter, supervisory information can be sent to a remote station while the ACLA is receiving data from the station over a half-duplex, 2-wire circuit. Typical uses include circuit assurance, error control, and interrupt (break). A logic 0 deactivates SRTS.

OM - Originate mode/auxiliary. A logic 1 in this position causes the ACLA to notify the modem equipment that it is in the originate mode. A logic 0 indicates answer mode. This line is an auxiliary signal line and may be used for other functions as designated by system design.

LMA - Local mode/auxiliary. A logic 1 in this position causes the ACLA to notify the modem (when equipped) to loop back the analog signal on the modem. A logic 0 disables the loopback. This line is an auxiliary signal line and may be used for other functions as designated by system design.

DTR - Data-terminal-ready. A logic 1 in this location causes the ACLA to notify the modem that the system is ready to communicate with the modem. A logic 0 causes a not-ready signal to be reported.

TB - Terminal-busy. A logic 1 causes the ACLA to notify the modem to busy-out-the-line. A logic 0 disables this function.

ION - Input-on. When this bit is a logic 0, the input section of the ACLA cannot receive data characters nor transfer data to the LM. A logic 1 causes normal input operation.

OON - Output-on. A logic 1 causes the output section of the ACLA to report output-data-demand initially when command is received if clear-to-send is active, and enables the output to report output-data-demand whenever the output buffer is empty. A logic 0 inhibits reporting of output-data-demand.

TABLE 2-8. COMMAND WORD 2 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit Content		1	0	1	BREAK	ISR	ISON	DLM	RSR1	RSR2	TSR1	TSR2

BREAK - Break-mode. A logic 1 here causes the ACLA to place the transmit-data line in a spacing condition (0 state). A logic 0 inhibits the break operation and returns the line to marking condition (1 state).

ISR - Input-status-report. A logic 1 in this position causes the ACLA to report the status of the RS-232 interface lines and any other ACLA status that may be active once each time the command is received. The ISR command is honored only when the ACLA has previously received a logic 1 in the ISON position. This is a momentary nonstored command. (If ISR is a 1 and ISON is a 1 in the same line frame, status is reported.)

ISON - Input-status-on. When a logic 1 is in this bit position, the ACLA monitors the modem interface and reports input supervision. A logic 0 inhibits monitoring and reporting. Status is not reported automatically when this command bit is first received by the ACLA. The ACLA must receive either an ISR command or status change to report input supervision.

DLM - Data-line-monitor. A logic 1 here causes the ACLA to monitor the receive-data line that is in a break condition for one character time after reception of the command. This command is used to allow the processor to determine the length of a break condition on data input. This is a momentary, nonstored command.

RSR1, RSR2 - Receive-speed-range 1 and 2. This code causes the ACLA to select a reference frequency from the LM to provide a range of baud rates selectable by bits IO1 thru IO4 in command word 4. See table 2-9.

TSR1, TSR2 - Transmit-speed-range 1 and 2. This code causes the ACLA to select a frequency from the LM to provide a range of transmit baud rates selectable by bits IO5 thru IO8 in command word 4. Table 2-9 shows the code and related reference frequencies.

TABLE 2-9. CODE BITS AND REFERENCE FREQUENCIES

Freq Desig	Code IO5	IO6	IO7	IO8	Reference Frequency	Baud Rate
A	0	0	0	0	9.6 kHz	45 to 100
B	1	0	1	0	19.2 kHz	100 to 600
C	0	1	0	1	153.6 kHz	600 to 9600
D	1	1	1	1	Special†	Special†

†Provided by an optional 115.2 kHz oscillator attached to the LM backplane. This special frequency can be used to accommodate a baud rate not available from the range of transmit baud rates shown in table 2-10.

Each time a command is given to the ACLA, each bit (IO1 thru IO8) must be set to the condition desired on the associated function. Failure to do this will result in the condition being cleared or set to a different condition. Each time a command is given, the ACLA monitors each bit and takes the action dictated.

NOTE

When IO1 thru IO8 in command words 1 and 2 are all set to logic 0, the ACLA is cleared to a known state which disables any input (output data demand, status or data) from the ACLA to the processor.

In command word 3, four bit positions (B4 thru B7) specify: 1) character length to be employed in interfacing with the external communications facilities, 2) whether parity bits are included in the data, and 3) whether the parity bit, if included, is odd or even. Parity bit management applies only to the serially transferred data on the communications line. There is no parity bit exchange between the ACLA and the LM.

Command word 3 format is depicted in table 2-11. Bit position 7, PSET, selects odd or even parity as indicated by the presence of a logic 0 or 1, respectively. Bit position 6, denoted PI for parity inhibit, commands the ACLA to check for parity upon input and to add a parity bit to the transmitted serial data stream upon output. A PI bit of logic 0 initiates these functions whereas a bit content of logic 1 commands the ACLA to dispense with parity generation and checking. This is indicated in table 2-12, which also presents the CO1 and CO2 bit code determining the character length employed during data transfers with the modems.

The character length, in terms of information content may be either 5, 6, 7, or 8 bits in length. However, if the PI bit is a logic 0, a parity bit is coupled with the information. In this case, the character length may be as long as 9 bits. Bit positions 10 and 11 specify the character length without parity and are coded as shown in table 2-12.

Command word 4, shown in table 2-13, is used in conjunction with bits IO5, IO6, IO7 and IO8 of command word 2 to set the baud rate for the input and output sections. The input and output baud rates may differ. To determine the proper code for the baud rate, select the range from command word 2 in which the desired rate is contained and the desired baud rate from command word 4.

The baud rate can be determined using an algorithm with the appropriate bits (4 bits on input or 4 bits on output) from command word 4 in conjunction with the range selected from command word 2. Proceed as follows to find the baud rate:

1. Complement each bit of the two 4-bit fields of command word 4. Convert each result to a base ten number using IO4 as the most significant bit for the input field and IO8 as the most significant bit for the output field. Add one to each result.
2. Multiply the above result by 16_{10}.
3. Divide this product into the reference frequency selected from table 2-10.

The following example illustrates this algorithm for baud rate determination:

Given:

from command word 4 - IO4 IO3 IO2 IO1
0 1 0 1

from command word 2 - IO5 IO6
1 0 (19.2 kHz)

Complement $0101_2 = 1010_2 = 10_{10}$

Add one to the result = $1011_2 = 11_{10}$

Then, the baud rate = $\frac{19.2 \times 10^3}{111 \times 16}$ =

109.1 baud

NOTE

The ACLA must be able to receive data that might have up to 40 percent distortion, that is, 40 percent of a bit per character. The result found above is valid for a 110 baud communications line, having .82 percent tolerance of the nominal value of 110 baud.

TABLE 2-10. COMMON BAUD RATES AND COMMAND CODES

Baud Rate	Speed - Command Word 4								Range - Command Word 2				
	Input				Output				Freq Desig	Input		Output	
	I1	I2	I3	I4	I5	I6	I7	I8		I5	I6	I7	I8
9600	1	1	1	1	1	1	1	1	C	0	1	0	1
7200 (Special)	1	1	1	1	1	1	1	1	D	1	1	1	1
4800	0	1	1	1	0	1	1	1	C	0	1	0	1
3600 (Special)	0	1	1	1	0	1	1	1	D	1	1	1	1
2400	0	0	1	1	0	0	1	1	C	0	1	0	1
1800 (Special)	0	0	1	1	0	0	1	1	D	1	1	1	1
1600	0	1	0	1	0	1	0	1	C	0	1	0	1
1200	0	0	0	1	0	0	0	1	C	0	1	0	1
1050	1	1	1	0	1	1	1	0	C	0	1	0	1
800	0	0	1	0	0	0	1	0	C	0	1	0	1
600	0	1	1	1	0	1	1	1	B	1	0	1	0
300	0	0	1	1	0	0	1	1	B	1	0	1	0
150	0	0	0	1	0	0	0	1	B	1	0	1	0
133.3	1	1	1	0	1	1	1	0	B	1	0	1	0
120	0	1	1	0	0	1	1	0	B	1	0	1	0
110	1	0	1	0	1	0	1	0	B	1	0	1	0
100	0	0	1	0	0	0	1	0	B	1	0	1	0
75	0	0	0	0	0	0	0	0	B	1	0	1	0
66.67	1	1	1	0	1	1	1	0	A	0	0	0	0
50.0	0	0	1	0	0	0	1	0	A	0	0	0	0

TABLE 2-11. COMMAND WORD 3 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit Content		1	0	1	PSET	PI	CO1	CO2	SB		ECHO	LIT

PSET - Parity-set. When B4 is a logic 1, concurrent with PI set to a logic 0, the ACLA generates and checks for even parity. A logic 0 concurrent with PI set to a logic 0 causes the ACLA to generate and check for odd character parity.

PI - Parity-inhibit. When B5 is a logic 0, the ACLA checks character parity on input and generates character parity on output. A logic 1 causes the ACLA to ignore parity.

CO1, CO2 - Code 1 and Code 2 bits form a code so that each combination corresponds to a character length of either 5, 6, 7 or 8 bits. The checking and generation of character parity adds one information bit to the character and therefore must be considered when selecting the unit code. Table 2-12 shows these code bits in relation to parity-inhibit bit.

SB - Stop-bit. A logic 1 in B8 position causes the output logic to generate two stop bits (For 5 data bits, the stop bit is 1.5 units in length.) on output and a logic 0 generates one stop bit.

ECHO - Echoplex mode. A logic 1 in this position causes the ACLA to return all data received from the modem on the receive-data line back to the modem on the send-data line while maintaining normal data processing in the input logic. A logic 0 inhibits echoplex operation.

LIT - Loop-internal-test. A logic 1 in this position causes the ACLA to go into an echoplex mode. Data and modem control signals from the output section are routed (looped back) to the input section. Refer to Programming Notes for additional information on this mode of operation. A logic 0 disables the echoplex mode.

TABLE 2-12. CHARACTER LENGTH AND PARITY STATUS CODE

Parity	Code (B9-B11)			Character Length (incl. parity)
	PI	CO1	CO2	
Yes	0	0	0	6
	0	1	0	7
	0	0	1	8
	0	1	1	9
No	1	0	0	5
	1	1	0	6
	1	0	1	7
	1	1	1	8

PROGRAMMING NOTES

The following notes provide additional information on the operation of the ACLA and are intended to assist the programmer. Typical input and output operations are presented.

ACLA INITIALIZATION

Before the ACLA is used following a power-up situation (either power up of a system in which the ACLA is already installed, or installation of the ACLA in an operating system or enablement of the ACLA by setting one of the enable/disable switches from the OFF to ON position), it should be cleared. Clearing the ACLA in this situation requires that the program perform the following:

1. Send output supervision with command words 1, 2 and 3 set to logic 0.
2. Momentarily activate the input-supervision-on (ISON) command with the appropriate output supervision. This causes any erroneous status set during the power-up sequence to be reported and cleared.

Any input line frames received from the ACLA prior to completion of the clear process should be ignored.

Once the ACLA is known to be in a cleared state, it can be initialized. Initialization generally consists of sending output supervision to activate ISON, selecting parity option and character length, and setting baud rate.

COMMUNICATIONS LINE CONNECTION

For switched (dial up) network connections, ring-indicator (RI) status indicates that the local modem is receiving an incoming call from a remote station. To cause the modem to answer the call, the program must send a command to turn data-terminal-ready (DTR) on. When the call has been answered, data-set-ready (DSR) is turned on and status reported.

For dedicated (private line) network connections, RI and DTR generally are not used. The program can determine the state of DSR by sending an input-supervision-report (ISR) command and observing the state of DSR status in the supervision returned.

In either type of network connection, DSR on indicates that the modem is connected to the communications line and data transmission can take place. DSR off at any time indicates that the modem is not connected to the communications line and data transmission cannot take place. Loss of DSR can occur because of any one of the following conditions:

1. Local modem is in a power-off condition.
2. Local modem is in a nondata mode of operation, such as alternate voice or test modes.
3. ACLA to modem cable is disconnected.
4. Local modem has gone to an "on hook" state and logically disconnected itself from the communications line.

INPUT OPERATION

When the remote station begins transmission, a carrier signal is applied to the communications line. The local modem detects this carrier, and DCD status is reported.

NOTE

In some situations, carrier is present continuously and is not turned on and off with each transmission.

To receive data (i.e., message from remote station), ION must be activated.

On two-wire, half-duplex communications facilities, ION should be deactivated before

TABLE 2-13. COMMAND WORD 4 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit Content		1	0	1	F1	F2	F4	F8	F1	F2	F4	F8
Field Definition		Format			Receive				Transmit			

output to avoid receiving back the message transmitted.

OUTPUT OPERATION

To transmit data, output-on (OON) command must be activated. Also, request-to-send (RTS) must be turned on if not so conditioned previously. When the modem is ready to transmit data, it returns clear-to-send (CTS) signal, which causes the ACLA to generate the first output-data-demand (ODD) and to report CTS status.

When the program receives an ODD, it should return a character to the ACLA. Each time that the ACLA transfers a character from its buffer register to the shift (disassembly) register, it generates an ODD. This sequence is repeated until the last character of the message is transmitted. RTS can be deactivated one character time (or more, depending on the modem type) after the generation of the last ODD.

LOOPBACK TEST OPERATION

To operate in loopback test mode, the loop internal test (LIT) command must be sent to the ACLA. Data and modem control signals from the output section are routed (looped back) to the input section as follows:

1. Transmit-data (TD) is connected to receive-data (RD).
2. Request-to-send is connected to clear-to-send.
3. Data-terminal-ready is connected to data-set-ready.
4. Local-mode is connected to data-carrier-detector (receive-line-signal-detector).
5. Secondary request-to-send is connected to secondary-data-carrier detector (secondary-receive-line-signal-detector).
6. Terminal-busy connects to ring-indicator.

While in this mode, all signals received from the modem are blocked and ignored by the ACLA. However, on the output side, signals to the modem are not blocked and caution must be used while in loopback test mode to avoid undesirable operation of the modem. For instance, while testing the operation of data-terminal-ready, an on condition is being received by the modem as well as being looped back as in item 3 above. If an incoming call was received in this situation, the modem would answer; this may confuse the calling station since no data transfer would occur. Therefore, DTR should only be turned on momentarily to test its operation and left off during other ACLA tests.

BREAK/OPEN-LINE DETECTION

Break (one or more character times of a spacing) or open-line (continuous spacing) conditions on the receive-data line can be detected by use of framing-error-status (FES) and the data-line-monitor (DLM) command. When a character is received without a stop bit (spacing or logic 0 condition detected when receive-data line is sampled for first stop bit), FES is reported in conjunction with the character. Following detection of a framing error, the ACLA locks up and is not in a condition to assemble additional characters until it sees a space-to-mark transition on the receive-data line or a data-line-monitor command. The program must issue a DLM command each time it receives FES to cause the ACLA to monitor the receive-data line for another character time. The program detects a break condition by the receipt of one or more (the exact number is established by software) consecutive null (all zero) characters accompanied by FES. Once a break or open-line condition has been determined to exist, the program may periodically interrogate the state of the line by issuing a DLM command. If the line remains in a spacing condition, the DLM command causes a null character to be assembled and FES reported. If the line has returned to a marking condition, the DLM command has no effect.

The ACLA monitors for framing errors at all times. It transfers the character received and reports FES whenever the ISON command is active, independent of the state of the ION command. Thus, break detection is possible while the ACLA is transmitting to a remote station even though the input section may be disabled (ION off).

RESTRAINT DETECTOR

For operation on the TWX network, the local modem may occasionally signal the ACLA to suspend data transmission. This condition may occur when the ACLA can transmit data to the TWX central office faster than the central office can convert the data and transmit it on to the appropriate station. The ACLA simply inhibits generation of ODDs while the restraint-detection signal is active, the net effect on software being a momentary delay in receipt of ODDs.

INSTALLATION AND CHECKOUT

UNCRATING

CAUTION

Although the integrated circuits and discrete components mounted on the individual printed circuit card can withstand considerable shock, the units must be handled with care. In no case should units be stacked directly upon one another because the printed circuit foil, components, or integrated circuits may be loosened or broken by such action.

The ACLA may be shipped already installed in a card cage assembly, or independently in a specially padded cardboard shipping container. Regardless of the method used for shipment, carefully unpack the units and check for damage. If a unit has been damaged in shipping, refer to section 8:503:00 of the Field Procedures Guide for Customer Engineers for instructions on disposition of damaged equipment.

INSTALLATION

CIRCUIT CARD TYPES

The DU137-A ACLA, PN74447001, is directly interchangeable with the DU189-A, DU189-B, DU190-A, DU190-B, DU191-A, or DU191-B ACLA, PN74877129, tables 3-1 and 3-2.

CABLE TYPES

Two cables are required for each ACLA card. The DU137-A ACLA is used with any of the cable sets listed in table 3-1. The DU189, DU190, and DU191 ACLAs, listed in table 3-2, contains the card and cables selected for specific applications.

Three types of cable assemblies are available for ACLA cards, each type used for a different application. The cable type is identified by its assembly part number on a band around the cable at one end. A typical cable and its connectors are illustrated in figure 3-1. Tables 3-3, 3-4, and 3-5 provide pin connection data for each type of cable.

ACLA cables with exposed shields are used with B version NPU cabinets containing electromagnetic interference shielding. On each cable, 3 feet (0.9 metre) of cable shielding adjacent to the CLA connector is exposed to enable grounding to the cabinet frame.

CIRCUIT CARD LOCATIONS

ALCA circuit cards are installed in a CLA and loop multiplexer card cage. See figure 1-2. There may be from one to four card cages used in the multiplexing subsystem, all identical. If only one card cage is used, it is located in the lower section of the bay. See figure 3-2. Of the 18 slots available in a card cage, the two rightmost are reserved for loop multiplexer cards. ACLA cards can be inserted into any or all of the remaining 16 slots.

COMMUNICATIONS LINE EXPANSION UNITS

Optional CLA and LM card cages have the same capacity as the basic card cage and are known as communications line expansion (CLE) units.

The first optional communications line expansion provides the second card cage assembly, which is mounted in the center of the cabinet above the first cage.

The second optional CLE unit provides the third card cage assembly, which is mounted in the lower section of the stand-alone cabinet. See figure 3-3. This option also includes a blower assembly and a power supply.

NOTE

The 2550-2 Host Communications Processor and the 2552-2 NPU each contain a second bay which houses the second and third CLEs.

The final CLE option provides a fourth card cage assembly, which is mounted in the center of the stand-alone cabinet. This unit uses power and cooling from the second CLE unit.

CARD LOCATION PRIORITIES

Because each CLE card cage assembly is identical in configuration and each CLA is the same as another in size, a CLA card can be physically installed in any card slot of any CLA and LM card cage.

Although random insertion of CLA cards into any of the available slots is permissible, best system performance is obtained when the cards having the highest character rates are inserted into the highest priority slots.

TABLE 3-1. CABLES USED WITH DU137-A ACLA

Equipment Number	Part Number	Application	Connector to Modem/Terminal	Connector to ACLA
XA133-A YA228-A	74657700 74875756†	Compatible with AT&T 103/113 Data Sets	25-contact plug	25-contact receptacle
XA135-A YA230-A	74657900 74875846†	Connects directly to terminal without a modem. Compatible with any terminal with RS-232-C interface capable of operating AT&T 103/113 or 202 Data Sets.	25-contact receptacle with threaded retaining spacers	25-contact receptacle
XA134-A YA229-A	74658300 74875760†	Compatible with AT&T 103F, 202R Data Sets or CDC telegraphic level converter	25-contact plug	25-contact receptacle
XA229-A†† YA234-A††	74874002 74876194†	Compatible with AT&T 202 Data Sets with reverse channel option	25-contact plug	25-contact receptacle

†Used with B version cabinets
††Special application

TABLE 3-2. DU189-A/B, DU190-A/B, and DU191-A/B Cable Sets

Equipment Number	Part Number		
	ACLA Card†	Cable	
DU189-A	74872129	74657700	Compatible with AT&T 103/113 Data Sets
DU189-B ††	74872129	74875756	
DU190-A	74872129	74657900	Compatible with any RS-232-C interface capable of operating AT&T 103/113/203 Data Sets. Connects directly to a terminal without a modem.
DU190-B ††	74872129	74875846	
DU191-A	74872129	74658300	Compatible with AT&T 103F/202R Data Sets or CDC telegraphic level converter.
DU191-B ††	74872129	74875760	

†ACLA card, PN 74872129, is interchangeable with DU137-A ACLA, PN 74447001.
††Used with B version cabinet.

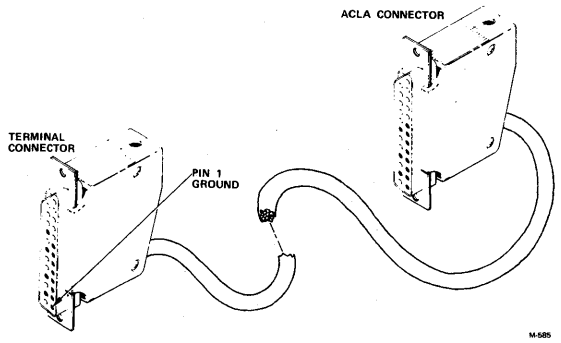


Figure 3-1. Typical ACLA Cable Connectors

TABLE 3-3. CABLE 10400-1
SIGNALS AND PIN CONNECTIONS

CLA Connector		Signal Flow	Modem Pin No.
Description	Pin No.		
Protective Ground (AA)	1†	←→	1
Transmitted Data (BA)	2	→	2
Received Data (BB)	3	←	3
Request to Send (CA)	4	→	4
Clear to Send (CB)	5	←	5
Data Set Ready (CC)	6	←	6
Signal Ground (AB)	7	←→	7
Rcvd Line Sig Det (CF)	8	←	8
Data Term. Ready (CD)	20	→	20
Ring Indicator (CE)	22	←	22
Terminal Busy (-)	25	→	25

†Cable shield terminated to connector shell and pin 1 at each end.

TABLE 3-4. CABLE 10400-2
SIGNALS AND PIN CONNECTIONS

CLA Connector		Signal Flow	Term. Pin No.
Description	Pin No.		
Protective Ground (AA)	1†	←→	1
Transmitted Data (BA)	2	↘	2
Received Data (BB)	3	↙	3
Request to Send (CA)	4	→	8
Clear to Send (CB)	5	←	
Data Set Ready (CC)	6	←	20
Signal Ground (AB)	7	←→	7
Rcvd Line Sig Det (CF)	8	←	4
		→	5
Data Term. Ready (CD)	20	→	6

†Cable shield terminated to connector shell and pin 1 at each end.

TABLE 3-5. CABLE 10400-3
SIGNALS AND PIN CONNECTIONS

CLA Connector		Signal Flow	Modem Pin No.
Description	Pin No.		
Protective Ground (AA)	1†	←→	1
Transmitted Data (BA)	2	→	2
Received Data (BB)	3	←	3
Request to Send (CA)	4	→	4
Clear to Send (CB)	5	←	5
Data Set Ready (CC)	6	←	6
Signal Ground (AB)	7	←→	7
Rcvd Line Sig Det (CF)	8	←	8
Originate Mode	11	→	11
Data Term. Ready (CD)	20	→	20

†Cable shield terminated to connector shell and pin 1 at each end.

Character rate is the bit per second (bps) rate divided by the unit code. Thus:

$$\text{character rate} = \frac{\text{bps}}{\text{unit code}}$$

where the unit code equals the number of bits per character, including any start, stop, or parity bits.

Each card cage is organized so that the leftmost card slot has the highest priority and each succeeding slot to the right has a lower operating priority than its neighbor on the left. Moreover, CLA1, as labeled on a card, has a higher priority than CLA2 on the same card.

If the system has more than one CLA card cage, the LM with the highest priority has its upper cable connected to the MLIA. The LMs are connected serially so that the LM with top priority has its lower cable joined to the upper connector of the LM next in operating priority. These priorities of interconnection are illustrated in figure 3-4.

CARD INSTALLATION

ACLA cards are installed in the selected CLA and LM card cage assembly as follows:

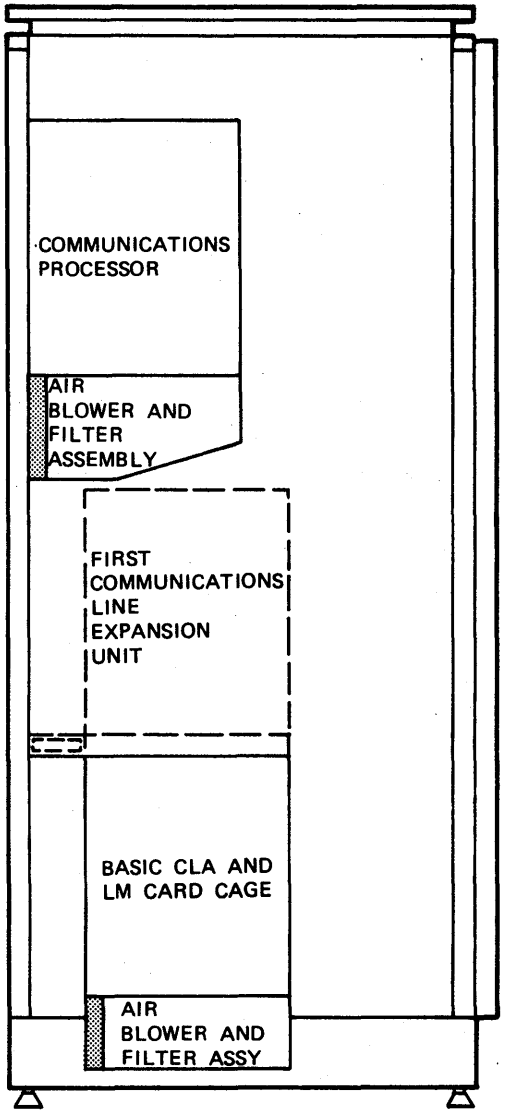


Figure 3-2. Component Location, Basic NPU Cabinet, Side View

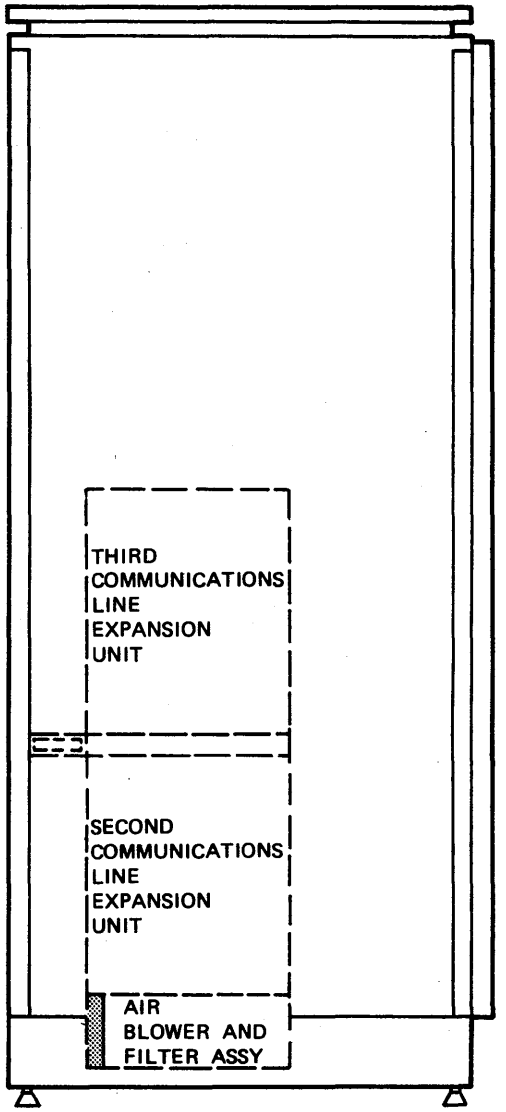
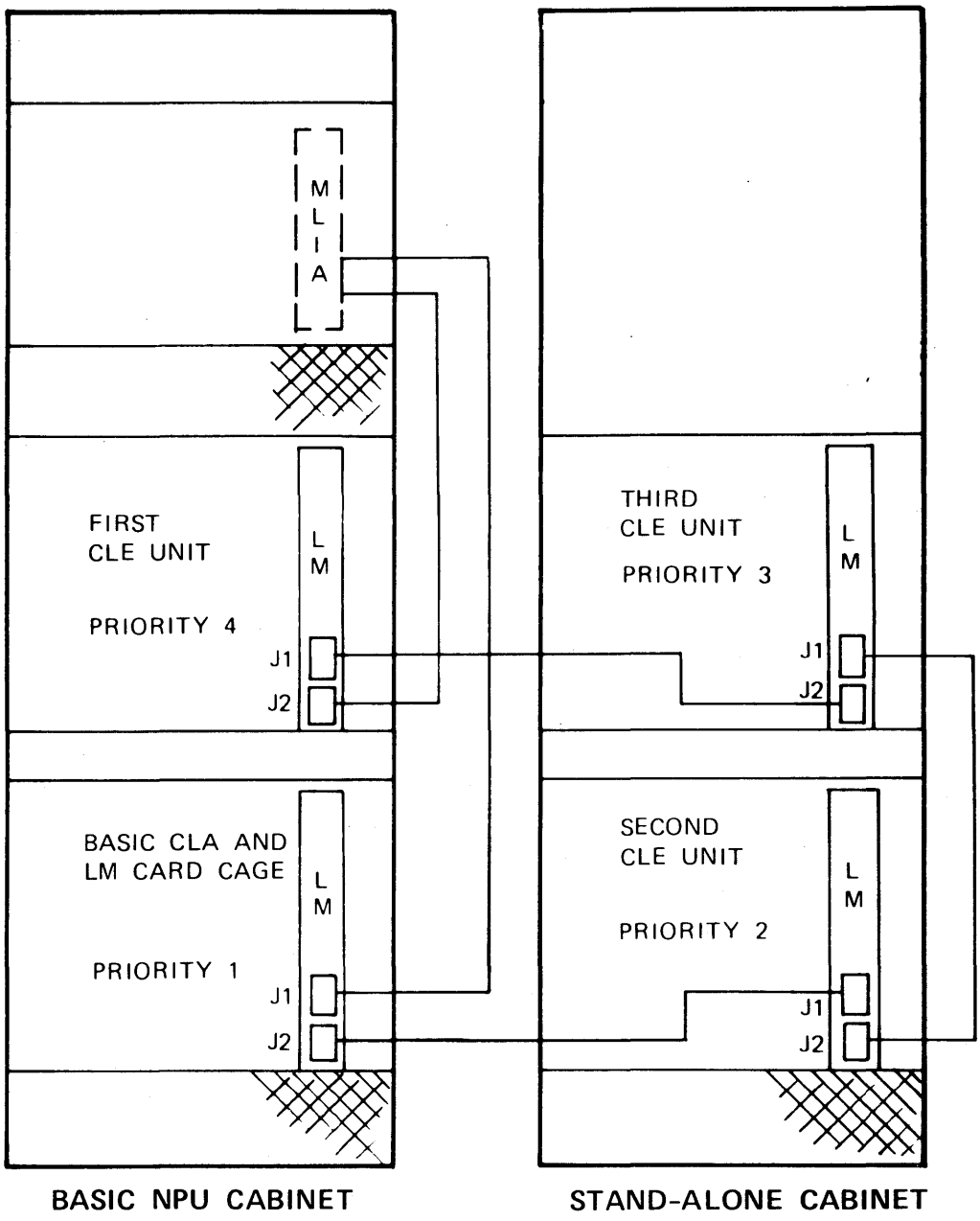


Figure 3-3. Component Location, Stand-Alone Cabinet, Side View



LEGEND:

CLA – COMMUNICATIONS LINE ADAPTER
CLE – COMMUNICATIONS LINE EXPANSION
LM – LOOP MULTIPLEXER

Figure 3-4. Priorities of Loop Multiplexer Interconnection

CAUTION

Do not attempt to install an ACLA card in the communications processor card cage, located at the top of the basic cabinet. If attempted, the communications processor backplane will be damaged.

1. Set CLA1 and CLA2 enable/disable switches to OFF.

2. Position card vertically so that connector on card handle is on lower part and thumbwheel switches are on upper part.

3. If system is operating, set thumbwheel address switches on card handle to the proper hexadecimal address before installing ACLA card. Refer to Controls and Indicators, section 2, for method of setting an address.

CAUTION

Ensure that 51-pin tab connectors on rear edge of card are properly aligned with their mating connectors on card cage backplane. Cross-slotting will destroy the backplane.

4. Insert rear edge of card into slotted guides, making certain that card is perfectly vertical and not cross-slotted.

5. Slide card into card cage, applying firm pressure on card handle to engage connectors on card with backplane connectors. All card handles will be flush with one another when cards are correctly installed.

6. Position blank slot covers in all card slots that are not used to assure that blower air flow is contained in card cage.

7. Set thumbwheel address switches on card handle. Refer to Controls and Indicators, section 2, for the method of setting an address.

8. Set enable switches to CLA1 and CLA2 (enable) positions.

CABLE INSTALLATION

ACLA cables are installed as follows:

1. Select a cable that is compatible with terminal or modem to be connected to ACLA. Refer to the cable indentification.

2. Attach cable to terminal or modem, then attach the other end of cables to the ACLA card handle. All cables exit through bottom of cabinet. In the B version cabinets, cables are routed through cable grounding assembly located at bottom of cabinet. See figure 3-5. For ACLAs installed in upper expansion position of cabinets, route cables through cable tray provided on either side and then down along the side to bottom of cabinet.

3. Tighten down retaining screws on all cable connectors. Apply pressure to grounding clamp (B version) and tighten screws.

4. Lay out surplus length of cable in a long, flat loop under the raised floor or in enclosures; this manner of storage minimizes kinking of cables.

5. Place protection padding, if available, over stored loops of cable before installing flooring.

INITIAL CHECKOUT

After all ACLA cards are installed and connected, diagnostic or system programs can be used to determine overall ACLA function.

If a fault is isolated to the ACLA, the following mechanical checks may be made:

1. Check that enable switch of ACLA in question is in the on (up) position.

2. Check that ACLA cable connectors are firmly attached.

3. Ensure card is firmly placed in card slot.

4. Monitor LED indicators under ACLA card handle to ensure electrical power is on ACLA card.

5. If LED indicators are not lit on the ACLA card, check LED indicators on LM card handle to ensure power is available to card cage.

CRATING AND SHIPPING

If ACLAs are to be shipped installed in a card cage assembly, the packaging must be designed to hold the ACLA cards securely in place during shipment, as well as to provide protection for the exterior of the card cage.

If the ACLAs are to be shipped independently, they must be packaged in well-padded cardboard containers to protect the integrated circuits, discrete components, switches and printed circuit foil from damage during shipment.

Packaging should conform to the requirements of CDC Procedure 13-002, Packaging and Material Handling Documentation.

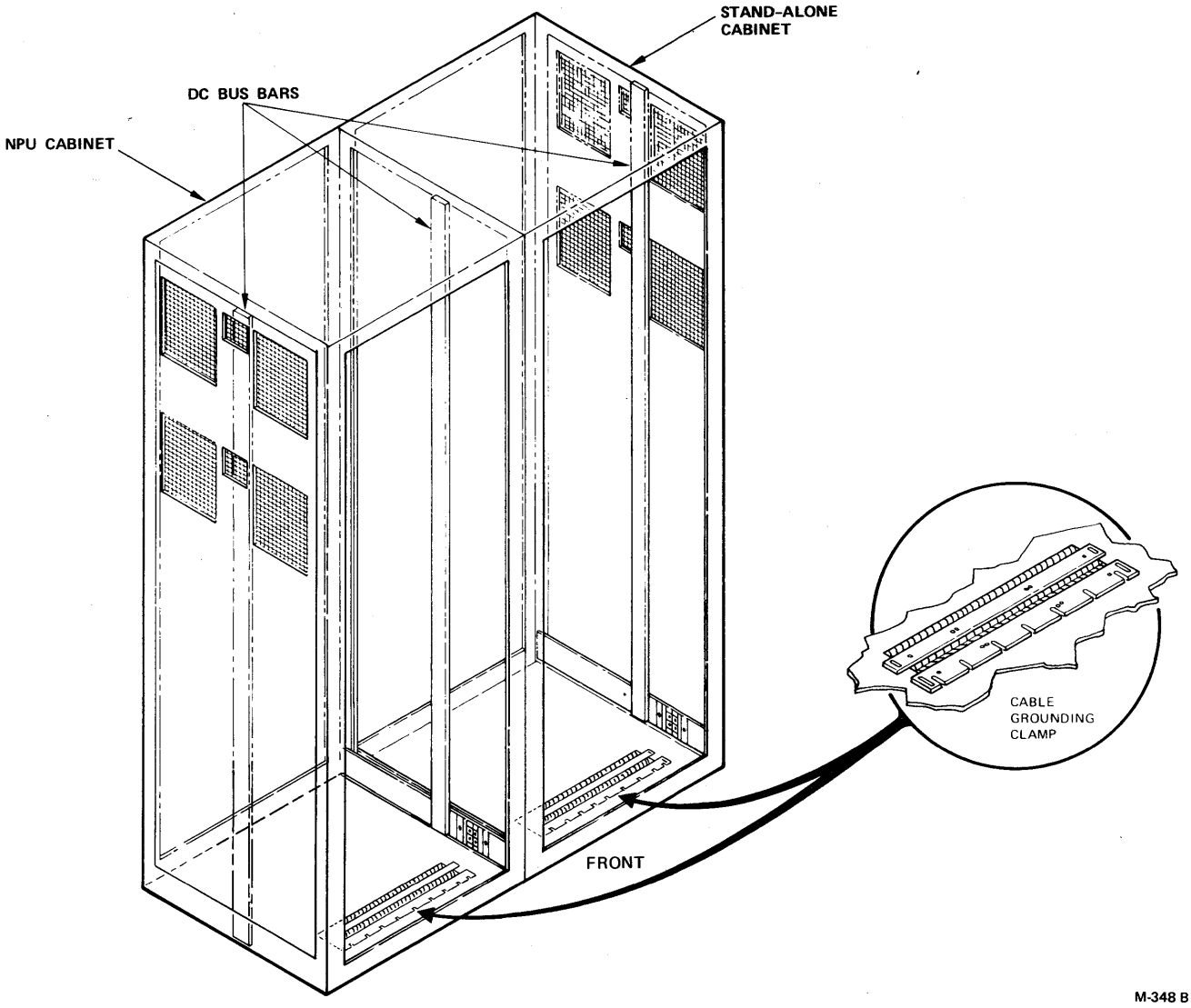


Figure 3-5. Typical Grounding Arrangement for B Version NPU Cabinets

INTRODUCTION

The ACLA logic circuit card is functionally divided into two ACLAs. Certain parts of the logic are used by both ACLAs. For the purpose of this discussion, the logic of only one ACLA (ACLA1) is detailed; the other ACLA (ACLA2) is mentioned only in discussing certain circuits shared by both ACLAs. ACLA1 is subdivided into four major sections: output, input, speed generator, and modem interface. Refer to the logic diagrams in section 5 to aid in understanding the following discussion.

OUTPUT SECTION

The output section of the ACLA receives commands and data from the processor via the loop multiplexer (LM) output bus. The information in the commands controls both the output and input sections. Data received by the ACLA in parallel is shifted out serially onto the communications line.

BUS BUFFERS

All signals originating at the LM are buffered by the ACLA so that no more than one transistor-transistor-logic (TTL) load is created by the ACLA. Inverting and non-inverting elements are used to perform this function. For the most part, these buffered signals are used by both ACLAs (primarily the bus signals). A timing diagram for the LM to ACLA interface is shown in figure 4-1.

SELECT OUTPUT

Commands and/or data must always be preceded by an address. Each ACLA has a unique 8-bit address which is selectable by means of two hexadecimal thumbwheel switches located on the card handle. On the 2-digit switch, the upper digit is the most significant digit (refer to section 2). The LM places the address, the output-select (OSL) signal, and the output-strobe (OST) signal on the bus when it has information for the ACLA. This address is compared with the preset address by two 4-bit comparators. The comparators are cascaded with OSL and applied to the J input of the select-output (SELO) flip-flop.

NOTE

In the descriptions and diagrams in this section, all mnemonics for signals that are active in the low condition are followed by an asterisk. Those shown without an asterisk are active in the high condition.

On the rising edge of OSTA*, the SELO flip-flop is clocked to a set condition. The ACLA output is thus selected and is prepared to accept commands or data until it is deselected. When the LM has provided all information in a particular line frame to the ACLA, it sets output-select-clear* (OSC*) to a logic 1. This signal is applied to the $\overline{K}$ input of the SELO flip-flop. On the rising edge of output-strobe OSTA*, the SELO flip-flop is clocked to a reset condition, deselecting the ACLA output section.

FORMAT DECODE

Output format bits 2 and 3 (OF2, OF3) are monitored by a 2-to-4 decoder. Only two decoded formats are used by the ACLA, namely, output-data cell (ODATA) and output-supervision (OSUP) cell. If bits OF2 and OF3 are both logic 0, ODATA is decoded, thereby enabling the acceptance by the ACLA of the data character which is present on the output bus (IO1 thru IO8). OSUP is decoded when there is a supervision format present (OF2 is logic 0 and OF3 is logic 1). OSUP enables the command counter. The format decoder is used by both ACLA1 and ACLA2 and is enabled only if either SELO1 or SELO2 is active.

COMMAND COUNTER

Since all commands sent to the ACLA have the same format code, the ACLA must keep track of the sequence of commands so that it can route them to the proper section of the logic. The command counter is responsible for this task. It is implemented by using a 4-bit register as a shift register with a single true bit which is shifted on each output strobe (OST).

The command counter is enabled only when OSUP is decoded by the format decoder. This signal is applied to the reset of the command counter so that for any format code other than supervision the command counter is disabled.

When the first command is sent by the processor, OSUP is decoded, enabling the command counter. The $\overline{Q}_3$ from the first stage of the counter is high and is gated with OSUP to produce the signal COM1, which is used to enable the storage of the first command word. On the rising edge of OST*, the counter is advanced to COM2, and to COM3 and COM4 on subsequent edges. The clock to the counter is produced by the ORing of OST1 and OST2. COM2, 3, and 4 enable the storage of command words 2, 3, and 4, respectively. The command counter is used by both ACLAs.

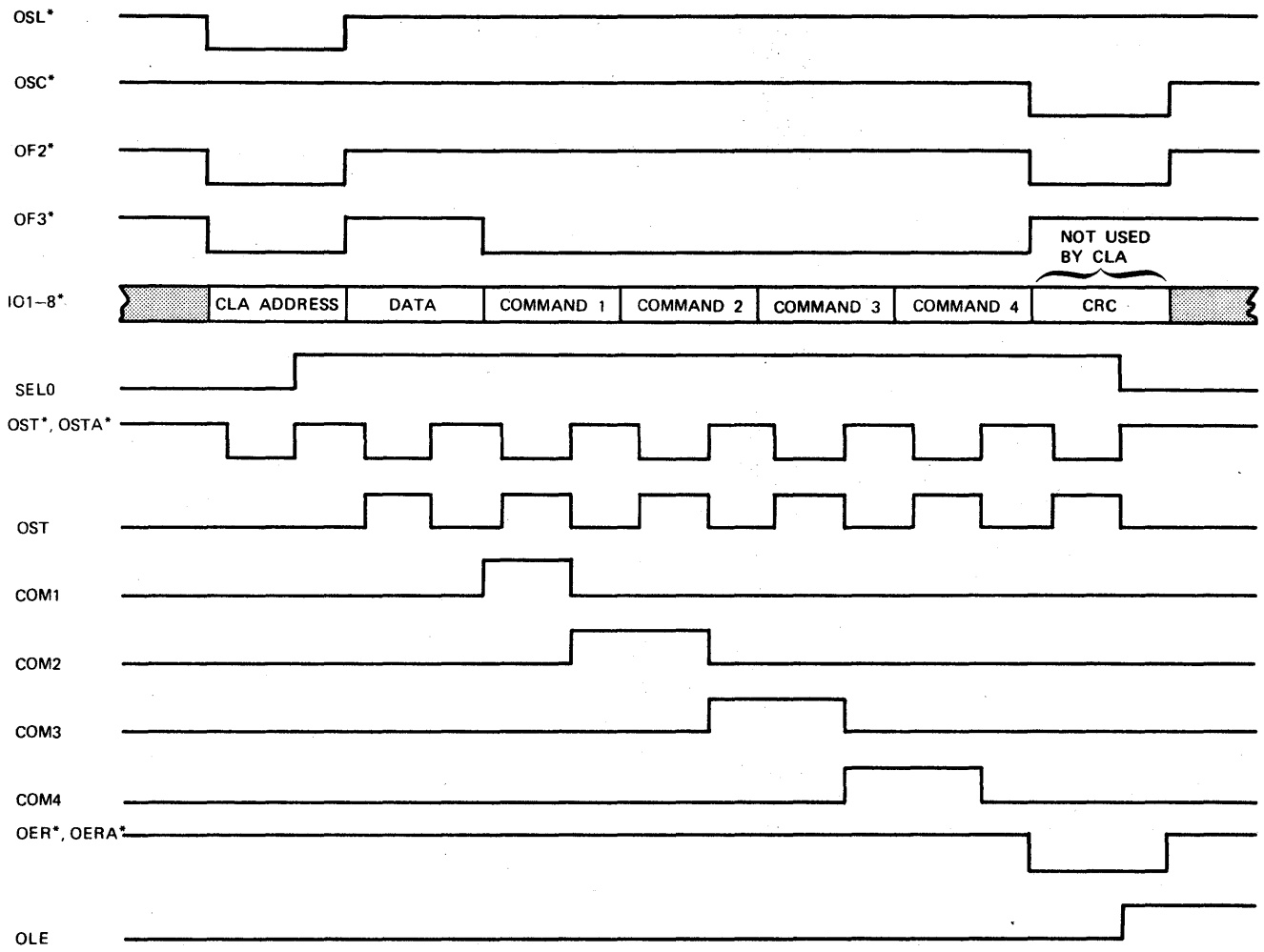


Figure 4-1. Loop Multiplexer-to-ACLA Interface and Command Timing Diagram

COMMAND REGISTERS

All commands are strobed into their associated registers with either COM1, COM2, COM3, or COM4, and OST. The command 1 register stores all of the modem control signals plus output-on (OON) and input-on (ION). It is implemented with two 4-bit parallel-load shift registers. COM1 enables parallel-entry, and on the falling edge of OST the registers are loaded with the information output IO1 thru IO8 bits present at their inputs. Break, input-status-on (ISON), receiver shift register, and transmitter shift register (RSR1, RSR2, TSR1, and TSR2) of the second command are stored in the same type of register in a like manner with COM2 and on the falling edge of OST. Also, the echo and loop-internal-test (LIT) commands of command 3 and all the speed generator divider bits of command 4 are stored in the same manner on the falling edge of OST and COM3 and COM4, respectively. The PSET, PI, CO1, CO2 and SB (stop bit) commands of command 3 are strobed into the control register of the UART with the rising edge of OST if COM3 is active. The data-line-monitor (DLM) and input-status-report (ISR) commands of command 2 are non-stored commands having an active duration equal to the pulse width of OST (300 nanoseconds with a 20-mHz loop).

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

The universal asynchronous receiver/transmitter (UART), a large-scale integration (LSI) package, is the main functional element in the ACLA. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, parity, and stop bits into parallel data and verifies proper code transmission by checking the receipt of a valid stop bit and proper parity if selected for parity.

The UART is programmable as to word length (5, 6, 7 or 8 bits), parity (even, odd, or parity inhibited) and the number of stop bits (normally 1 or 2 bits, but 1-1/2 bits with a 5-unit code). The transmitter and receiver share the control register and thus are configured in the same manner.

The control register is loaded during command word 2 with IO1 thru IO8 bits present on its inputs. These bits are strobed in with the control register load.

Transmitter

Figure 4-2 is a block diagram of the transmitter portion of the UART, and figure 4-3 is a timing diagram. Data can be loaded into the transmitter holding register (THR) whenever the transmitter holding register empty (THRE) is at a logic 1, indicating that the THR is empty. The data is loaded in by strobing the transmitter holding register load (THRL) line to 'low'. Data is transferred automatically to the transmitter shift register (TSR) as soon as the register becomes empty. The desired start, stop and parity bits are then added to this data, and serial transmission is initiated and is seen at transmit-data lines. This process is then repeated for each subsequent character as it becomes available. The transmitter requires a clock (TCK) that is a frequency 16 times the desired baud rate. The master clear clears the transmitter to an idle state whenever this line is strobed to a logic 1. It resets the TSR and the TD and THRE lines to a high level.

Receiver

Figures 4-4 and 4-5 show receiver block and timing diagrams, respectively. Serial asynchronous data is provided to the receive data (RD) input. The control logic searches for a logic 1-to-0 transition while in the idle state. If the input is still a logic 0 at the bit center, the signal is assumed to be a valid start bit, and the control logic is bit-synchronized so as to find the center of all subsequent data and stop bits. The receiver is then under the control of the control register.

The serial character present on the receive-data line is shifted into the receiver shift register. When the timing logic determines that the last stop bit is present, the character is transferred to the receiver holding register (RHR), and the input-buffer-full (IBF) line is set to a logic 1, thus indicating that a character is present on bits DAT1 thru DAT8. When this character is picked up, the reset-input-buffer-full (RIBF) line is pulsed low by external logic to reset the IBF line. If the IBF line is not reset before another character is assembled and transferred to the RHR, the data-transfer-overrun status (DTOS) line is set to a logic 1. This line remains logic 1 until the next character is loaded into the receiver holding register.

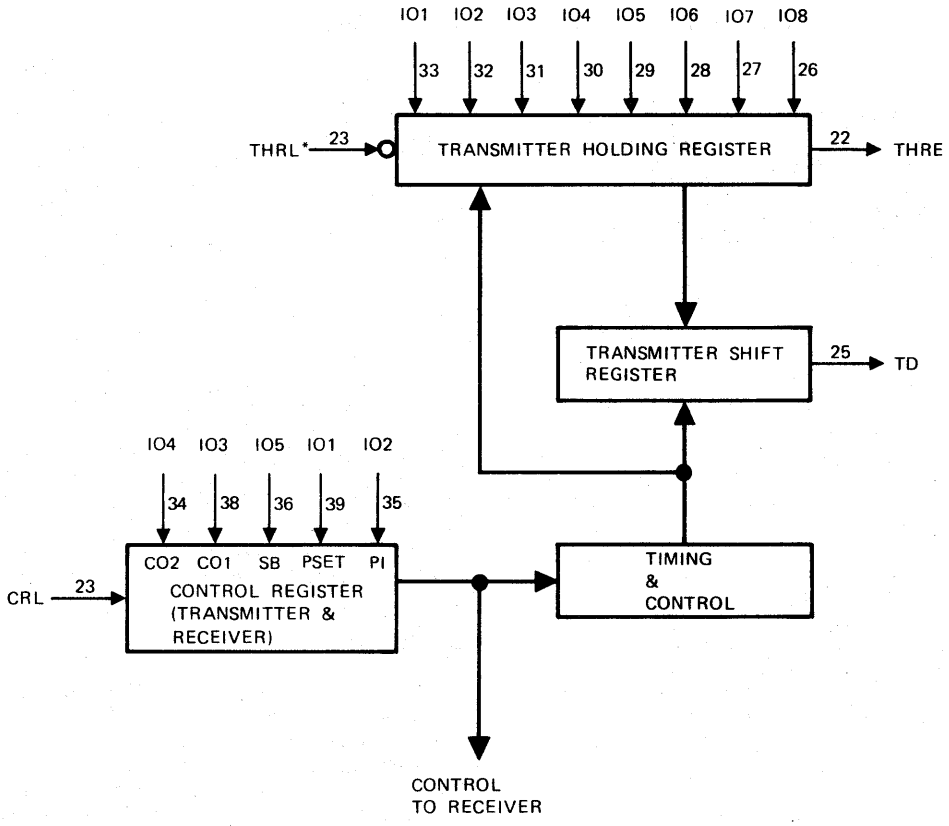


Figure 4-2. UART Transmitter Block Diagram

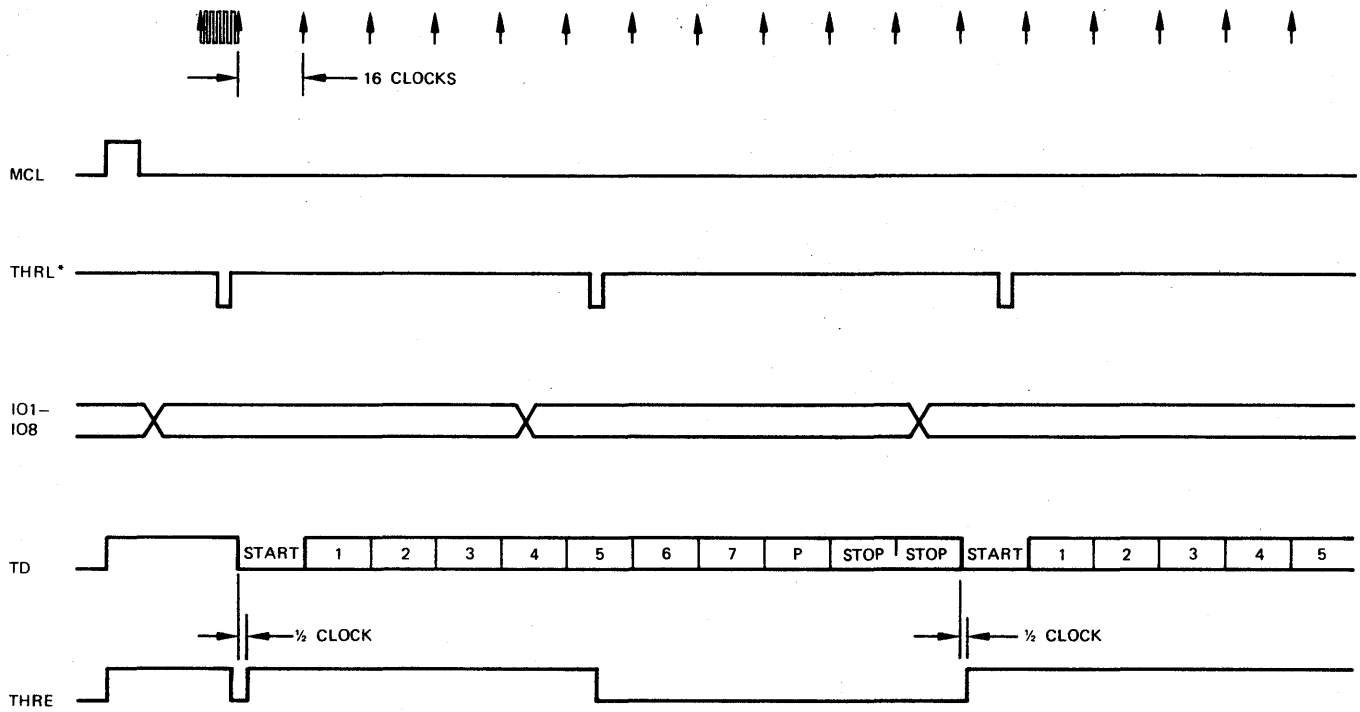


Figure 4-3. UART Transmitter Timing Diagram

If the UART is programmed to detect parity errors (even or odd) and a character is received with a parity error, the parity-error-status line is set to a logic 1 at the nominal center of the last stop bit. This signal is held until the next character is transferred to the RHR.

If the first stop bit is not a marking condition, the framing-error-status line (FES) is set to a logic 1 and held until the next character is transferred to the RHR. If the cause of FES is the receipt of a break character (null character without stop bits), the receiver is in a locked-up state so that the IBF does not set to a logic 1 until at least one character time has elapsed after a valid stop bit has been detected.

The timing for all receiver functions is obtained from the external receive clock (RCK) whose frequency is 16 times the desired baud rate. When the master clear line is strobed to a logic 1, the UART is set to an idle state. This resets TSR, RSR, RHR, FES, DTOS, PES and IBF, and sets TD and THRE.

OUTPUT DATA DEMAND

When the ACLA is able to accept a character from the LM, it sets the output-data-demand (ODD) flip-flop, which in turn causes IAV to activate. The ACLA address with the ODD flag bit set is picked up by the LM when the ACLA's input section is selected. The ODD flip-flop is reset during this selection. The processor, responding to the ODD, provides a data character to the output section of the ACLA via the LM.

The setting of the ODD flip-flop is controlled by four signals: ODD, THRE, restraint-detector* (RSD*), and clear-to-send status (CTSS). These signals are ANDed together to produce the clock for the ODD flip-flop. Since the D input is pulled up, the ODD flip-flop is set whenever three of the signals are logic 1 and the fourth makes a logic 0-to-1 transition. The resetting of the ODD flip-flop is discussed in the input section. Normally THRE triggers the ODD flip-flop.

OUTPUT DATA

After receipt of an ODD from the ACLA, the processor sends a character via the LM to the output section of the ACLA. SELO sets to 1 when the ACLA's address is detected by the ACLA. After the address is presented, the next word may be a data character, in which case the data format code is detected by the format decoder, making ODATA a logic 1. The data character present on bits IO1 thru IO8 is loaded into the transmitter holding register of the UART with

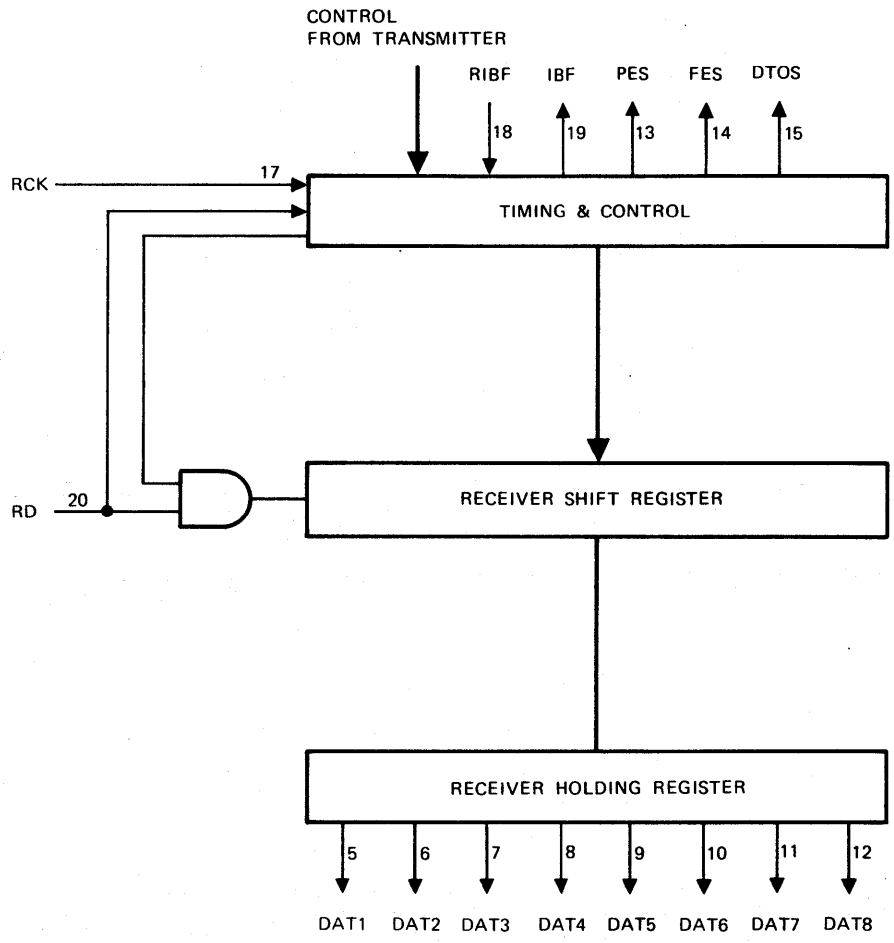


Figure 4-4. UART Receiver Block Diagram

the THRL* pulse that is produced by the NANDing of OST and ODATA.

The loading of the character into the transmitter holding register forces the THRE signal of the UART to logic 0, indicating that the transmitter holding register is no longer empty. When the character is transferred to the transmitter register, the THRE signal again goes to logic 1, which in turn sets the ODD flip-flop.

If the transmitter holding register is not loaded with a character before the center of the last bit of the character being transmitted from the transmitter shift register, the transmit-data line continues marking.

Transmit data, which is the output from the transmitter shift register of the UART, is fed to the modem interface for level conversion and transmission to the modem or terminal.

When the processor wishes to output a break on the send-data line, it must set the break bit in command word 2 to a logic 1. This causes the SD line to be clamped to a spacing condition.

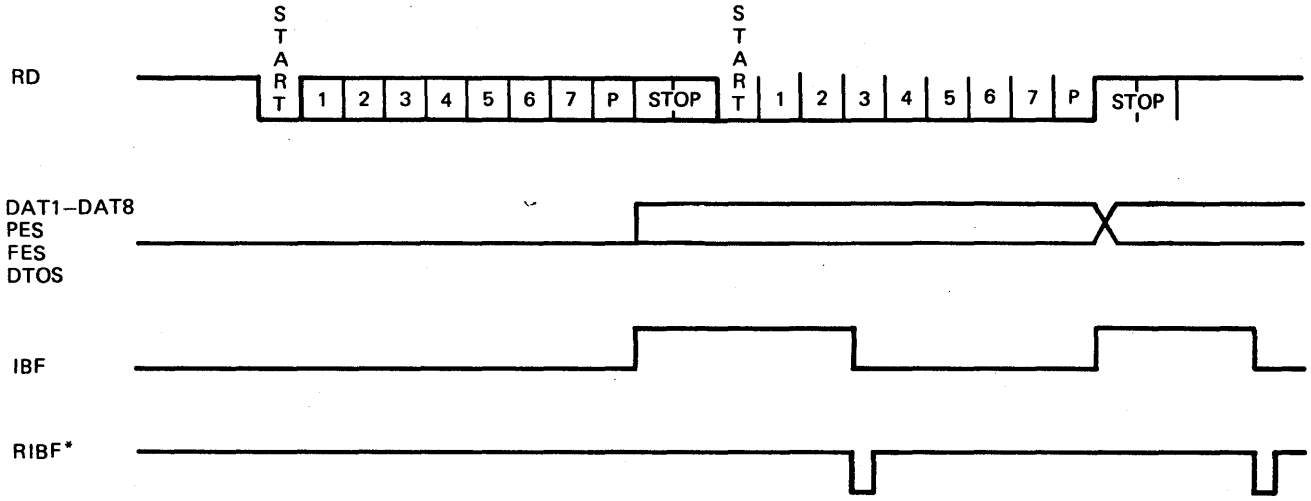
When an echo command is received from the processor, the receive-data signal is routed back to the send-data signal through the use of an AND-OR-Invert gate.

OUTPUT LOOP ERROR

Whenever the LM detects an error on the output loop while presenting information to the ACLA, it informs the ACLA of this condition via the output error line (a bussed signal). The output error signal is coincidental with IO1 thru IO8.

INPUT SECTION

The input section of the ACLA is responsible for the transference of data and the various statuses to the processor via the LM. Information is transferred in 11-bit parallel bytes (3 format bits and 8 input information bits). It performs the serial-to-parallel conversion of data incoming from



DETAIL:

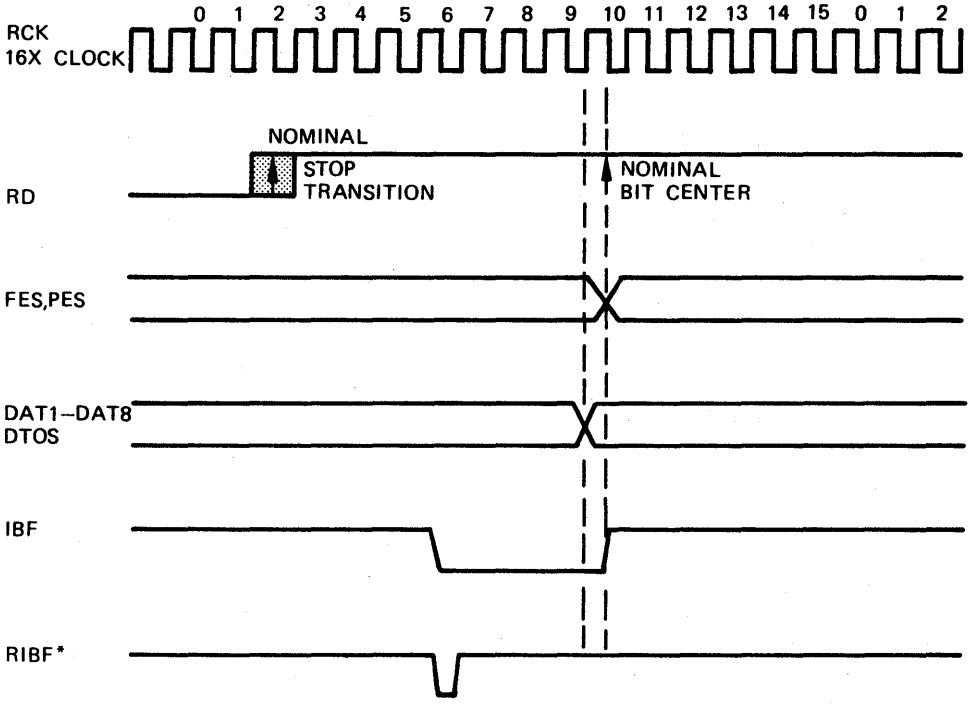


Figure 4-5. UART Receiver Timing Diagram

a modem or terminal device. The input section receives commands from the output section to program its characteristics.

INPUT AVAILABLE

The IA signal is activated by the ACLA whenever it has either output-data-demand, data, or status to report to the processor. The LM acts on this signal so that it selects the input section of the ACLA when it sees the next available input loop train.

The IA signal is derived by ORing status-available*, output-data-demand*, and data-available, then NANDing this result with the enable switch so that IA can be active only if the enable switch is in the on position. In the off position, the input to the NAND gate is at a low level, thus inhibiting the IA signal.

This enable switch should be in the off position when the ACLA card is inserted in an operating system and only turned on after the selection of the proper address. It should also be off when changing the address.

INPUT CONTROL LOGIC

The input control logic produces all signals which control the ACLA-to-LM interface. This logic is used by both ACLA1 and ACLA2 on a shared basis and is active only when the input section of either ACLA is selected by the loop multiplexer. It consists of a 2-bit input control states register, a states decoder, a holding register, a multiplexer and associated control logic. A diagram of the input control states is shown in figure 4-6. Timing diagrams of the input control (IC) and related signals are shown in figures 4-7 thru 4-10.

The LM selects the input section of ACLA by dropping input select (IS) to a logic 1 and providing input strobes (IST*). On each falling transition of IST*, the ACLA places information cells (address, data, or supervision) on the LM input bus. The transference continues until the input control logic activates the input-end (IEN) signal on the bus, indicating the last cell. The LM discontinues ISTs and raises IS* after detecting the IEN* signal. At that time the input control logic is again in an idle state.

Assume for the following discussion that ODD1*, DAV1 (data available), and SAV1* (status available) are logic 1. When input select (IS1*) goes to a logic 1, select input (SELI1*) is activated if IER is logic 0. SELI1* is ORed with SELI2* to produce SELI, which in turn releases the set of the input control register. In the idle state, SELI is logic 0, holding input control (IC1 and IC2) in a set condition. ODD1*, ODD2*, DAV1 (data available), DAV2, SAV1* (status available) and SAV2* are applied to the input of a D-type holding register that is loaded on the leading edge of SELI. The outputs of this register are connected with a two-to-one multiplexer which is controlled by SELI2*. In this case, SELI2* is high since SELI1* is active (SELI1* and SELI2* are mutually exclusive). ODD1*, DAV1 and SAV1* are transformed on the outputs of the two-to-one multiplexer to ODD*, DAV, and SAV*, respectively. These signals are used to determine the state changes as shown in the states diagram. See figure 4-6.

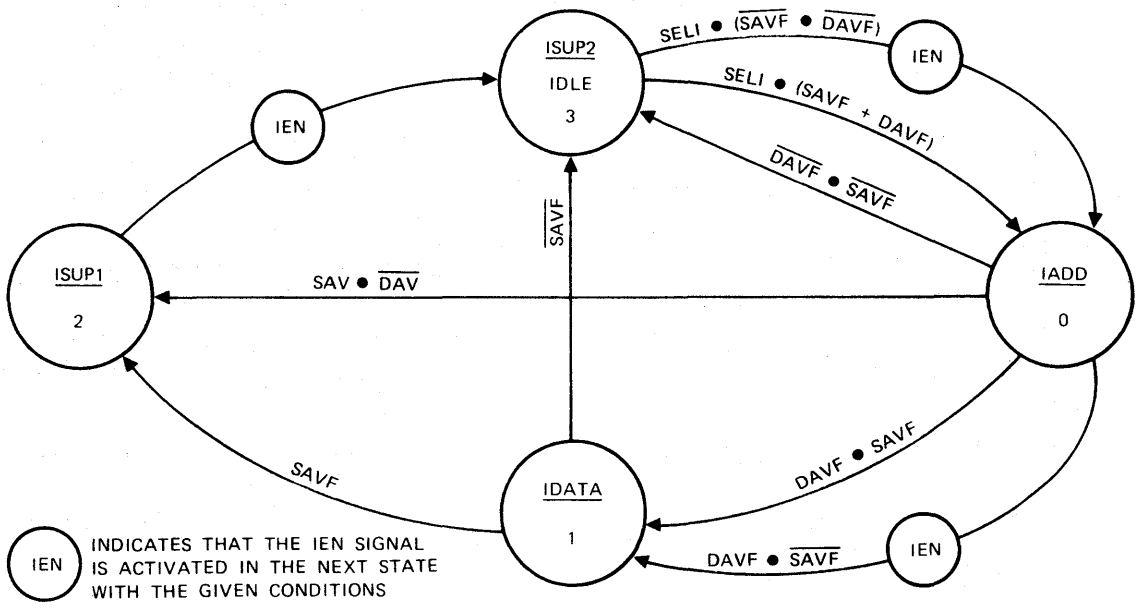


Figure 4-6. Input Control (IC2-IC1) States Diagram

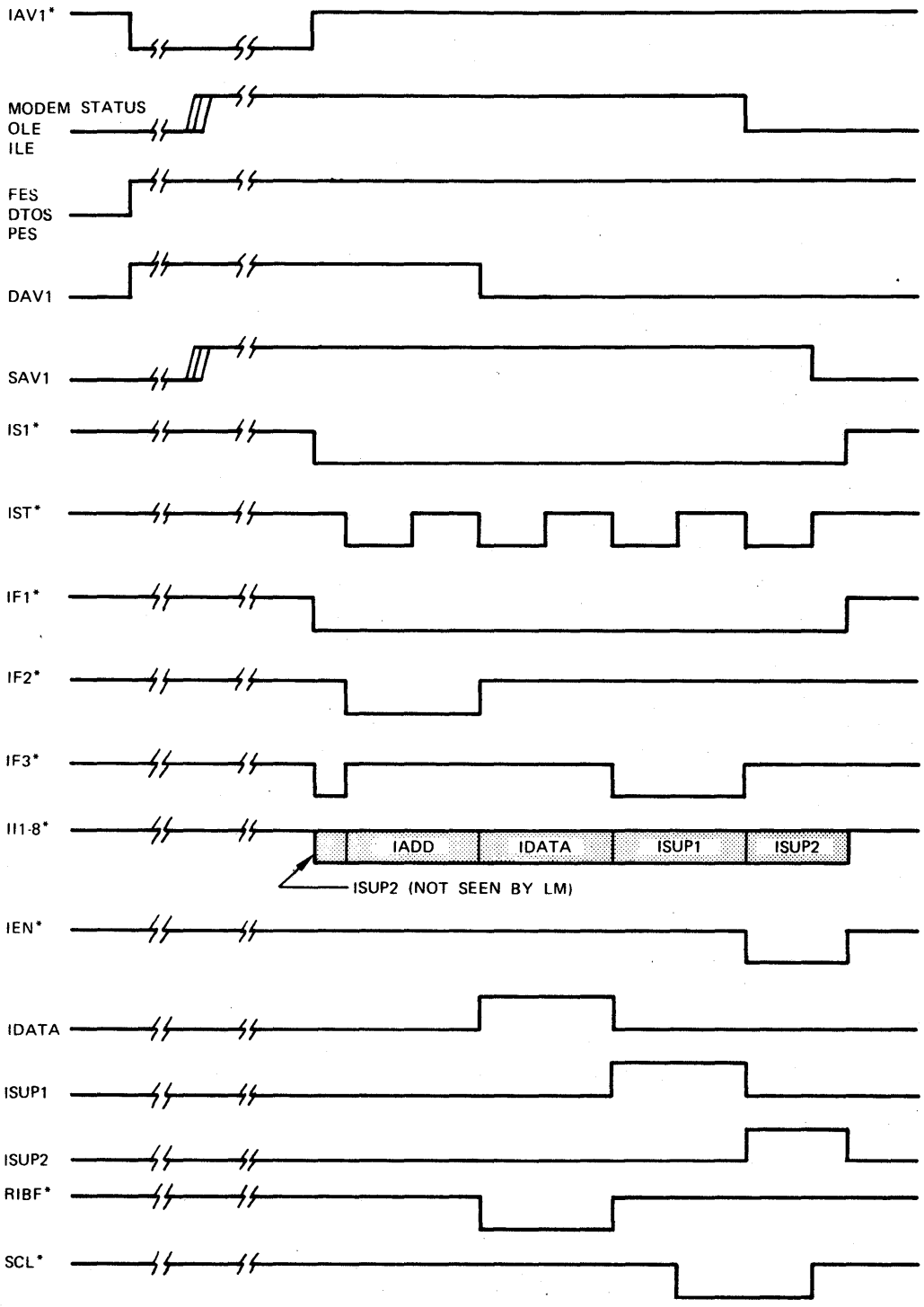


Figure 4-7. Input Control (ODD, DATA, SUPV) Timing Diagram

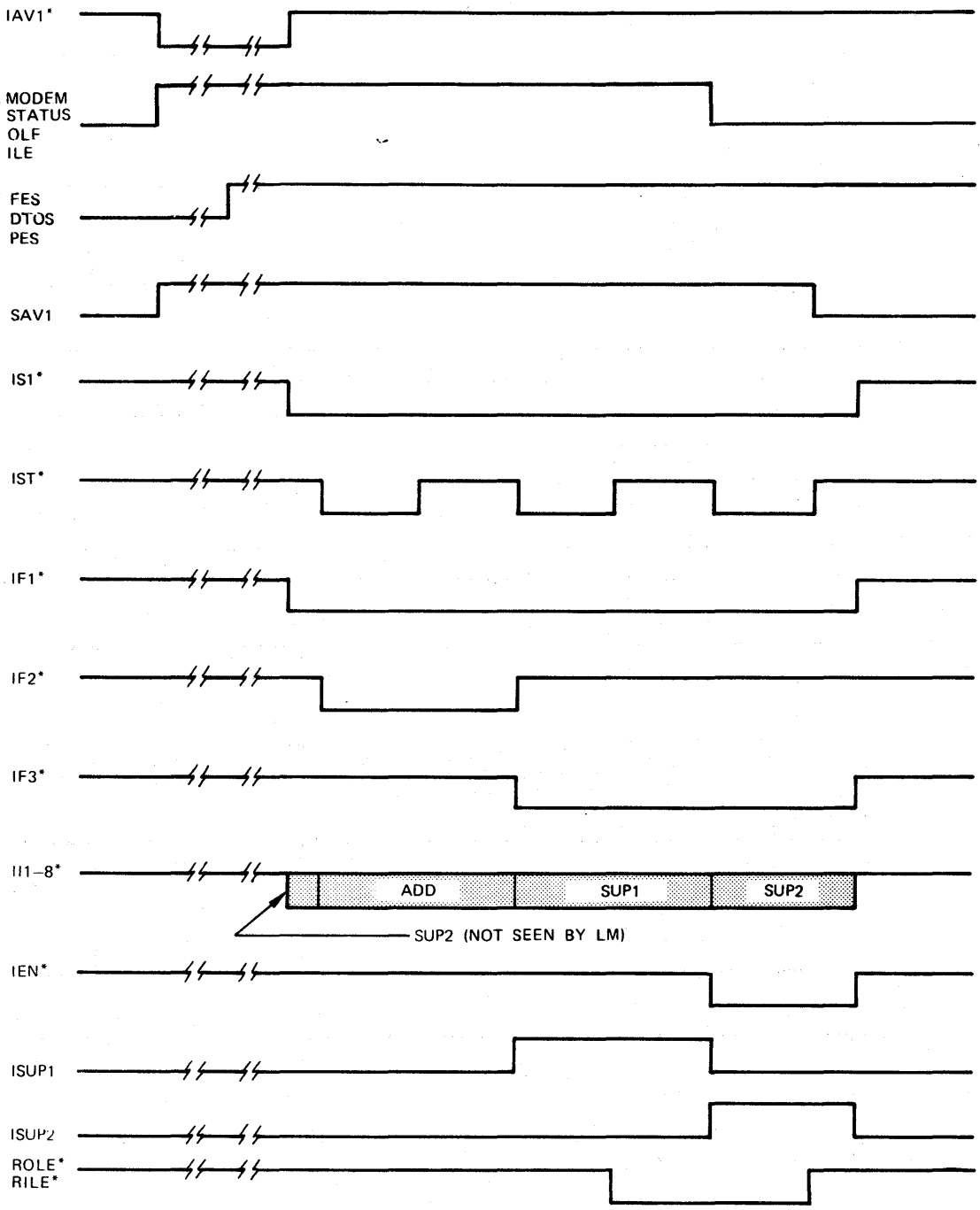


Figure 4-8. Input Control (SUPV only) Timing Diagram

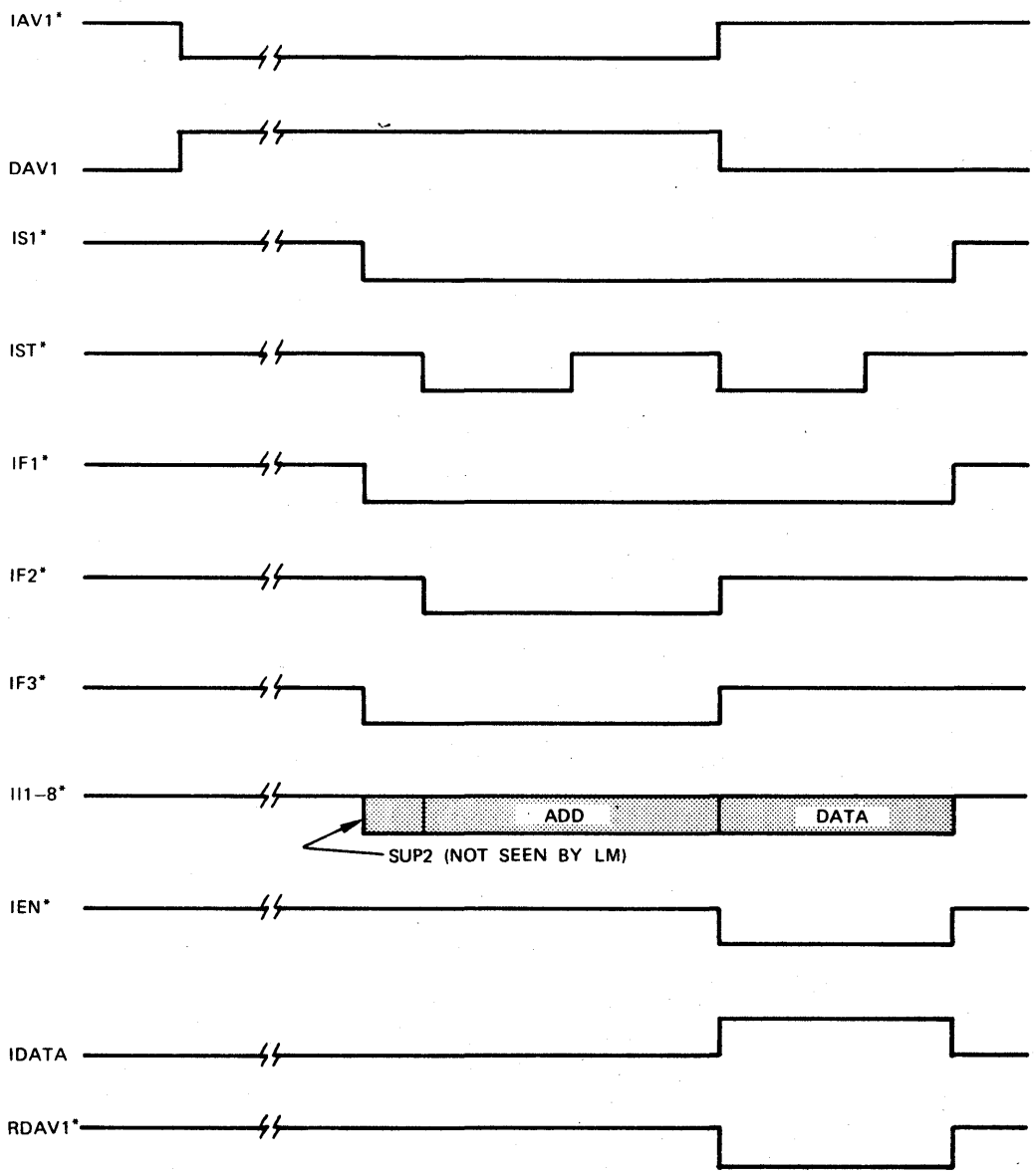


Figure 4-9. Input Control (DATA only) Timing Diagram

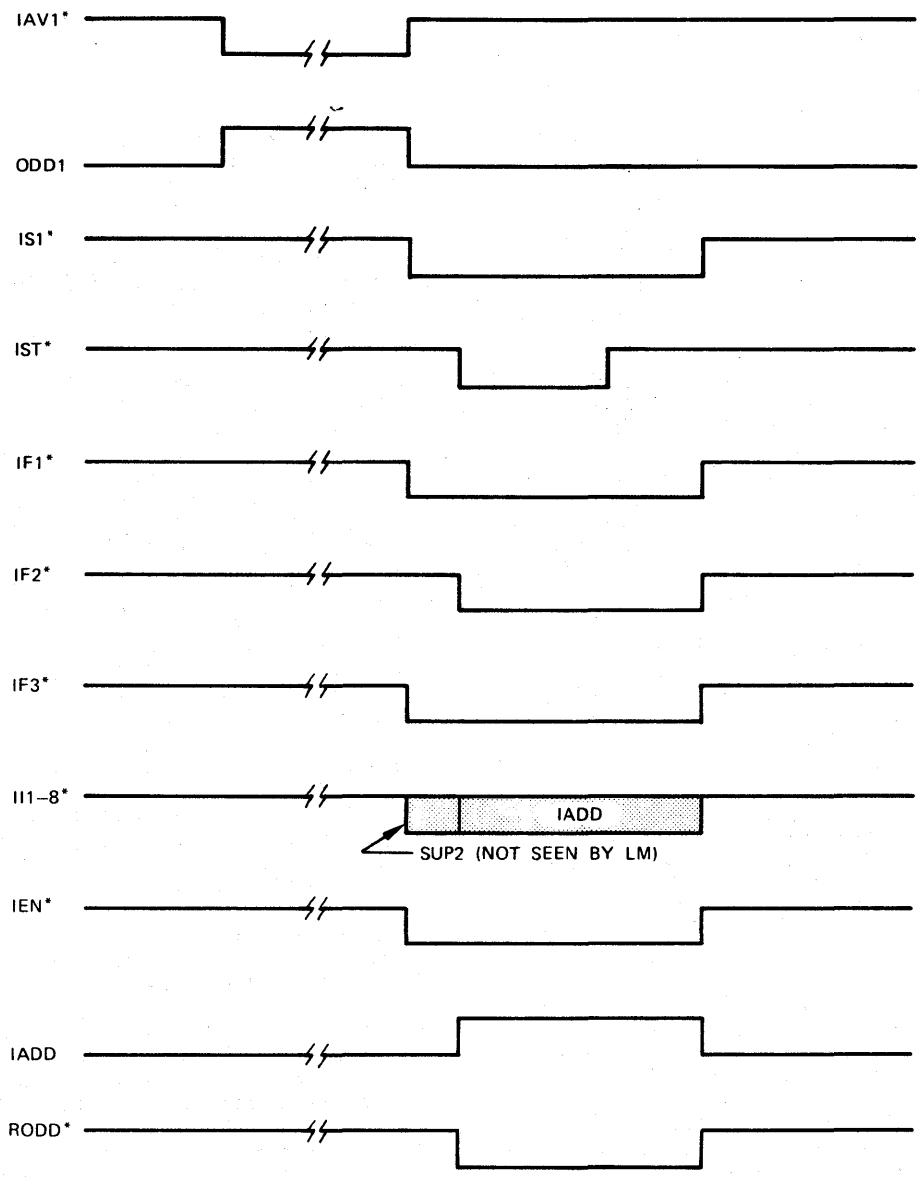


Figure 4-10. Input Control (ODD only) Timing Diagram

INPUT CONTROL STATES

The input control states are defined as follows:

State 0 is IADD, i.e., ACLA address with or without ODD bit is placed on the input bus;

state 1 is IDATA, i.e., data serially received from the communications line is placed in parallel on the input bus;

state 2 is ISUP1, i.e., the first status word is placed on the input bus;

and state 3 is ISUP2, i.e., the second status word is placed on the input bus.

INPUT MULTIPLEXER

The input multiplexer is used by both ACLA1 and ACLA2. It provides a 3-state interface with the LM input bus for the signals of IF2*, IF3* (input format) and II1* thru II8*. IF1* is activated by an open collector gate whenever SELI is a logic 1.

The input multiplexer is controlled by the signals SELI2*, SELI*, IC1 and IC2 of the input control logic. Eight 8-to-1 multiplexer integrated circuits make up the input multiplexer, the outputs of which are connected to the LM input bus lines of II1 thru II8. Address, data, and supervision bits from ACLA1 and ACLA2 are applied to the respective inputs of each multiplexer in such a way that the proper word is selected for transfer to the LM.

The signals SELI2*, IC1, and IC2 dictate which of the possible words are selected. SELI* enables the 3-state outputs of the multiplexers, i.e., if IC1 is logic 1, IC2 is logic 0 and SELI2 is logic 0, then receive data bits DAT1 thru DAT8 of ACLA1 appear at II1 thru II8, respectively.

Input format bits 2 and 3 (IF2, IF3) are produced by the outputs of two 4-to-1, 3-state multiplexers. These multiplexers are controlled by the signals of SELI*, IC1 and IC2. SELI* enables the 3-state outputs, while IC1 and IC2 place the proper format code on the bus. All of the multiplexed inputs are "hard-wired" except the ODD flag bit which is connected to ODD*.

INPUT LOOP ERROR

Whenever the multiplex loop interface adapter detects an input loop error during a loop batch, it notifies the LM via a restart loop end. If the ACLA used the last input loop batch, the LM activates the IER line and the IS line and provides one IST. When both IER and IS are logic 1, a low level is applied to the D input of the input loop error status (ILES) flip-flop. On the trailing edge of IST, the ILES flip-flop is clocked, thus storing the error condition. The ILES* signal sets the status R/W (if input-status-on is logic 1), which in turn activates the input available. ILES is picked up by the LM in ISUP1. The ILES flip-flop is reset when the status clear signal makes a logic 0-to-1 transition. The SCL signal is produced by a flip-flop which is set by the trailing edge of IST while in the input control state of ISUP1 and reset on the next trailing edge of IST.

CHARACTER ASSEMBLY

Before the ACLA can receive data from the communications line and transfer it to the LM, it must be programmed via the ACLA output section. It must be programmed to the proper character length and even or odd parity and programmed to enable the input section (ION is a logic 1).

After level conversion by the modem interface section, the receive-data signal is fed to the receive section of the UART. The UART monitors this signal for a start bit which begins the processing of the character as shown in the discussion of the UART. In the center of the first stop bit, the UART transfers the character to its receive holding register so that the character is present on DAT1 thru DAT8 and raises its input-buffer-full flag (IBF). ION is NANDed with IBF to activate input available. IBF is reset with reset-input-buffer-full (RIBF*), which is produced by the NANDing of IBF, SELI, IC1, and IC2.

The resetting occurs during the time that the LM picks up the data word. The preceding is the normal resetting procedure for IBF, but it is also reset when ION goes from the 0-to-1 condition by the NANDing of ION*, IO7, COM1, and OST.

When assembling characters, if IBF is not reset by the time that another character is transferred to the receive holding register, the data-transfer-overrun status (DTOS) flag sets to a logic 1. This signal is applied to the input multiplexer and accessed by the LM in the first status word. DTOS is reset on the first end of the next received character after the resetting of IBF. End of character is in the center of the first stop bit of the received character.

If the received data is in a spacing condition during the first stop bit of a received character, the framing error status (FES) flag of the UART sets to a logic 1 at the bit center of that stop bit. FES and IBF applied to an A-O-I gate set the status R/W, if ISON is logic 1. ISON also allows DAV to activate, which in turn allows data and status to be reported to the LM. This occurs regardless of the state of ION. This function facilitates the detection of a breaking condition: FES, reported to the LM in the same line frame as a data character of spacing, is interpreted by the

software as a character time of break (constant spacing).

Following the detection of FES, the UART loses character timing and cannot set IBF until it sees a space-to-mark transition on the RD line (the beginning of a stop bit).

If the RD line is in a break condition, the processor can determine the length of the break by issuing a data-line-monitor (DLM) command to the ACLA. DLM* is produced by the NANDing of IO4, COM2 and OST, and then ORed with the RD line to cause a short marking pulse on the RD line, and forces the receive clock to a high state. This results in the monitoring of the RD line by the UART for one more character time. If a break condition still exists, the ACLA reports a data character of all spacing and FES. In this manner, the processor may periodically interrogate the ACLA to determine the condition of the RD line.

MODEM INTERFACE SECTION

The modem interface provides the level converting receivers and drivers to interface the RS-232-C signals (±25V max) of the modem to the logic used in the ACLA. This section also provides the logic necessary to monitor the state of certain signals received from the modem.

The RS-232-C signals are considered in the marking, off, or logic 1 condition when the voltage level is more negative than minus 3 volts with respect to signal ground. The signals are considered in the spacing, on, or logic 0 condition when the voltage is more positive than plus 3 volts with respect to signal ground. The RS-232-C drivers of the ACLA provide, for the marking condition, a level more negative than minus 8 volts and, for the spacing condition, a level more positive than 8 volts.

MODEM STRAPPING

To insure compatibility of the ACLA with various types of modems, strapping options are provided on the ACLA logic card. The proper strapping must be verified for each modem type. This involves which modem signals are connected to certain pins on the 25-pin modem connector. The signals affected and their strapping points are shown in table 4-1.

MONITORING

The modem signals of clear-to-send (CTS), data-carrier-detector (DCD), secondary data-carrier-detector (SDCD) and data-set-ready are monitored by the ACLA for a level change (either an on-to-off transition or an off-to-on transition). Ring-indicator (RI) is monitored for an on-to-off transition. The modem interface section also contains the logic for operating in the loopback test mode, so that the following modem control and monitor signals are connected: SD to RD, RTS to CTS, LM to DCD, DTR to DSR (data-terminal-ready to data-set-ready), TB (terminal busy) to RI, and SRTS to SDCD.

TABLE 4-1. STRAPPING POINTS

Option	Signal	Strapping Points			
		ACLA1		ACLA2	
		From	To	From	To
1.	SRTS (Pin 19)	I	A	F	G
2.	SRTS (Pin 11)	J	D	N	E
3.	OM (Pin 11)	L	D	M	E
4.	LM (Pin 12)	K	C	P	H
5.	SDCD (Pin 12)	B	C	O	H

1. Standard production cards are set up with options 1, 3, and 5 as shown.
2. Options 2 and 3 cannot be chosen for the same ACLA.
3. Options 4 and 5 cannot be chosen for the same ACLA.

MONITOR SIGNALS

All modem monitor signals are inverted by the RS-232-C receivers. The resulting signals are supplied to a 2-to-1 multiplexer which is used for the self-test mode. The outputs of the multiplexer (CTS*, DCD*, SDCD*, and DSR*) are presented to change detecting circuits. If there is a level change in any one of these four signals, the status R/W is set, providing ISON is a logic 1. The setting of the status R/W causes the most recent condition of the four modem signals to be stored in a register. The outputs of this register are CTSS, DCDS, secondary data-carrier-detector status (SDCDS), and data-set-ready status (DSRS). These outputs are presented to the input multiplexer for transference to the LM when the ACLA's input section is selected.

Each change detection circuit consists of one section of the register and an exclusive OR gate. For example, if both DSR* and DSRS are logic 1, the status R/W does not set, since the output of the exclusive OR gate to which DSR* and DSRS are applied is a high level. Assume that now the state of DSR* is changed so that it makes a logic 1-to-0 transition. The output of the exclusive OR gate goes low, setting the status R/W which strobes the register storing the present condition of DSR*. Now DSR* and DSRS are both a logic 0, and the exclusive OR gate output is high. The DSR change detector is primed to respond in the same manner when DSR* makes a logic 0-to-1 transition. Note that the register is updated every time the status R/W is set. A timing diagram of the modem interface signals is presented in figure 4-11.

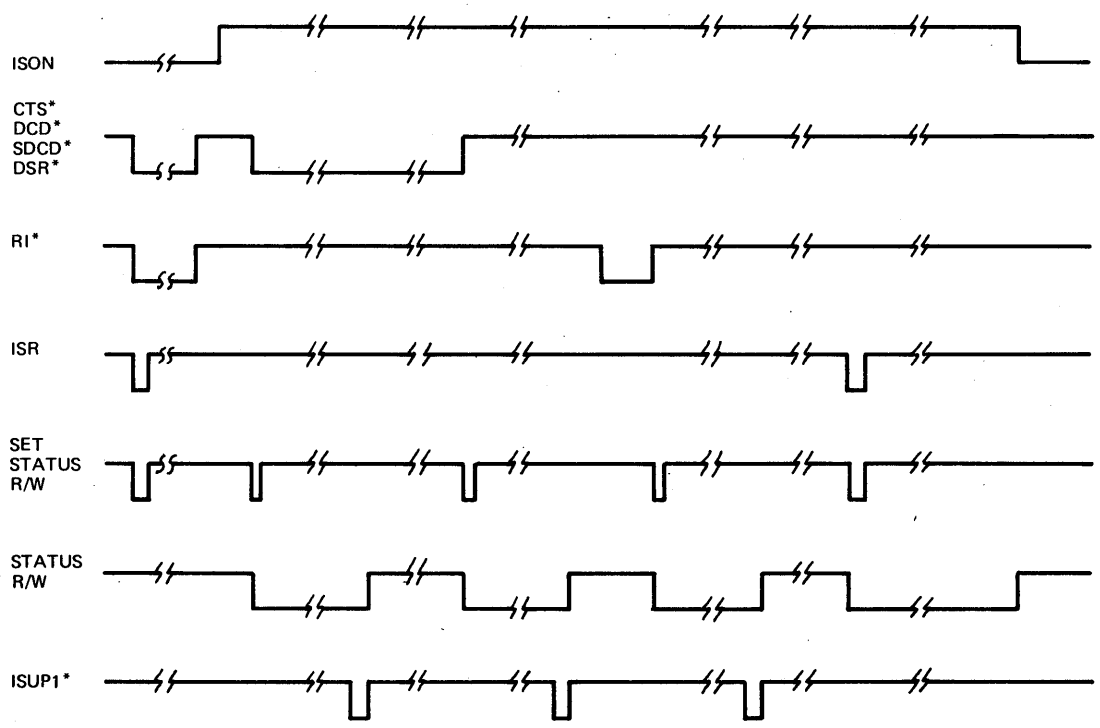


Figure 4-11. Modem Interface Timing Diagram

RING INDICATOR STATUS

Ring indicator status (RIS) is stored in a flip-flop. A logic 1-to-0 transition of ring indicator causes the status R/W to set. The setting of the status R/W causes the RIS flip-flop to be clocked to a logic 1. The next time the status R/W is set, if not caused by the toggling of the ring indicator (RI), the RIS flip-flop is clocked to a logic 0. The RI detection logic consists of an exclusive OR gate, a NAND gate, an inverter, the RIS flip-flop and a delay network. When the RI line goes to a logic 1, a low level is applied to the resistor-capacitor network, causing the capacitor to discharge through the resistor until the level across the capacitor reaches ground potential. The inputs to the RIS flip-flop are armed with a high level. When RI makes a logic 1-to-0 transition, the output of the NAND gate goes low, thereby setting the status R/W. The high level on the inputs to the RIS flip-flop is clocked into the RIS flip-flop by the setting of the status R/W. This level goes low 200 to 400 nanoseconds afterwards, then the capacitor charges to the turn-on voltage of the exclusive OR gate.

STATUS READ/WRITE

The status R/W is reset when the ACLA puts the second status word on the LM input bus. Since ISON is applied to the direct reset of the status R/W, this status is inhibited from setting when ISON is logic 0.

The status R/W can be set with any of the following eight signals: data-associated-status, input-loop-error, output-loop-error, or one of the five ouputs of the change detection circuit.

DATA ASSOCIATED STATUS

Data-associated-status* (DAST*) is produced by an A-O-I gate and may be activated by an input-data-error (parity or framing error or data-transfer-overrun) signal. FES, PES, and DTOS are applied to the A-O-I gate. If any one is logic 1, and IBF is logic 1, data-associated-status also goes to a logic 1. The remaining element of the A-O-I gate decodes the input-supervision-report command which causes data-associated-status to go to logic 1 if OST1, COM2 and IO2 are logic 1. The input-supervision-report command is a single-pulse signal.

INDICATORS

Light-emitting diodes are used to monitor the modem interface for the activity of the send-data, receive-data, request-to-send and data-set-ready. The indicators are activated with a logic 0, on, or spacing condition on their associated signals.

SPEED GENERATORS

The receive and transmit sections of the UART require separate clock sources that are each 16 times the desired baud rate of their associated section. These clock sources are supplied by the receive and transmit speed generators. Each speed generator, under program command, can select one of four reference frequencies supplied to the CLA (by the LM or special option) and can divide it by a predetermined integer to produce the 16 times clock required by the UART. All commonly used reference frequencies are necessary to the normal functioning of an ACLA. More than one reference frequency is available between a multiplexer and the communications line adapters it is servicing. The three reference frequencies supplied by the LM to the ACLA are: RF1 (9.6 kHz), RF2 (19.2 kHz), and RF3 (153.6 kHz). The ACLA can accommodate RF4, which is a special frequency supplied by an optional oscillator. These reference frequencies are applied to a 4-to-1 multiplexer which is controlled by receive speed ranges 1 and 2 of command word 2. The desired speed range is applied to a synchronously loaded binary counter. The counter is loaded with the levels present on RF1, RF2, RF4, and RF8. See figure 4-12. The loading is enabled by its own carry-out when the count reaches the F_{16}, which happens on the low-to-high transition of the selected reference frequency. The carry-out pulse is NANDed with the inversion of the reference frequency to produce the 16 times clock for the receive section of the UART. The speed generator for the transmit section of the UART operates in an identical manner to the receive sections speed generator described above.

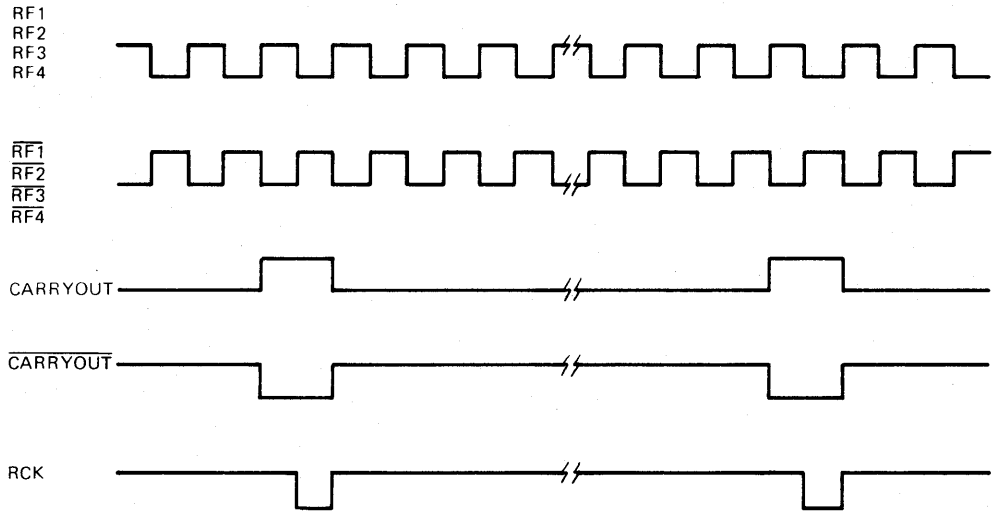
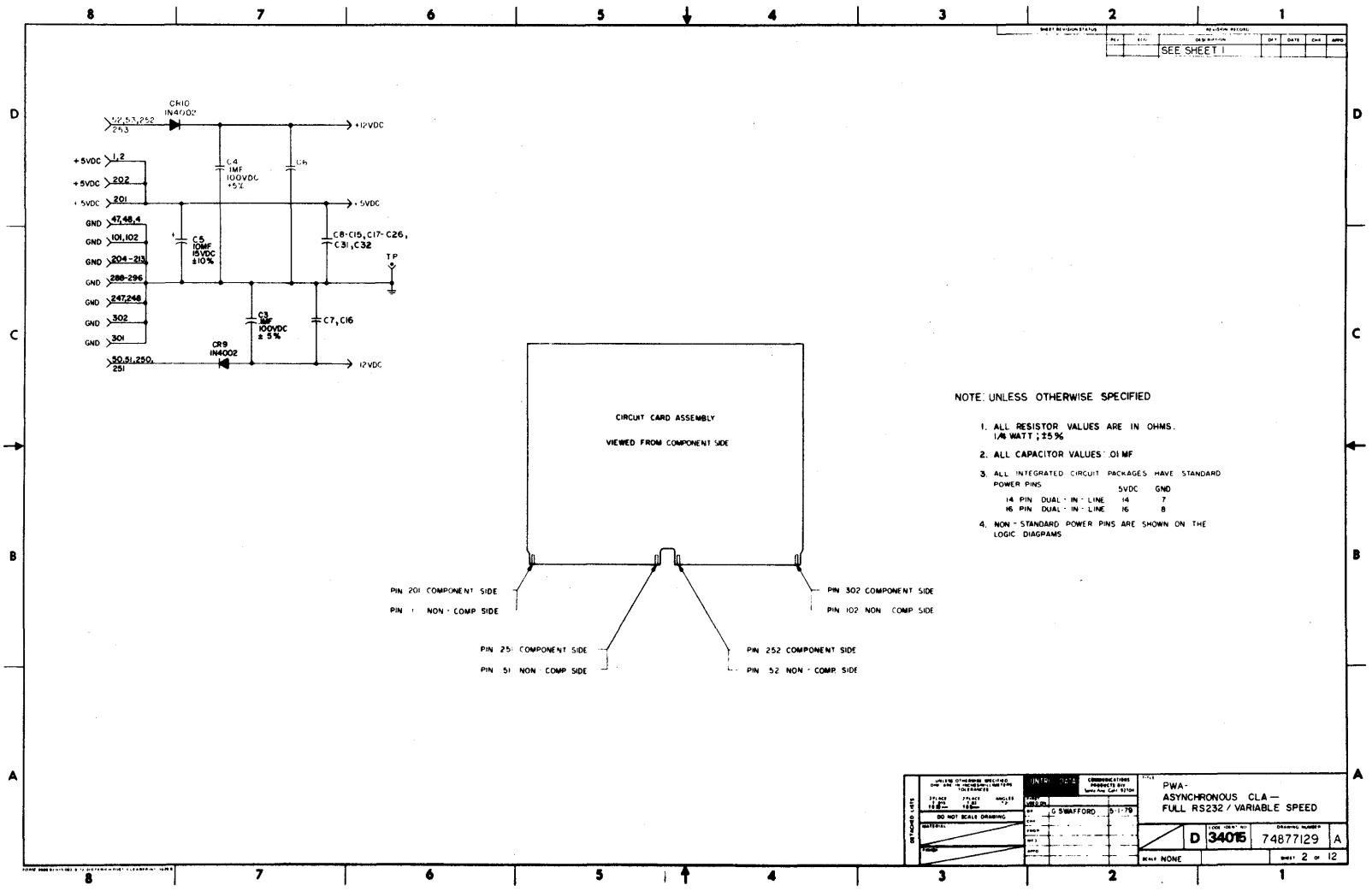
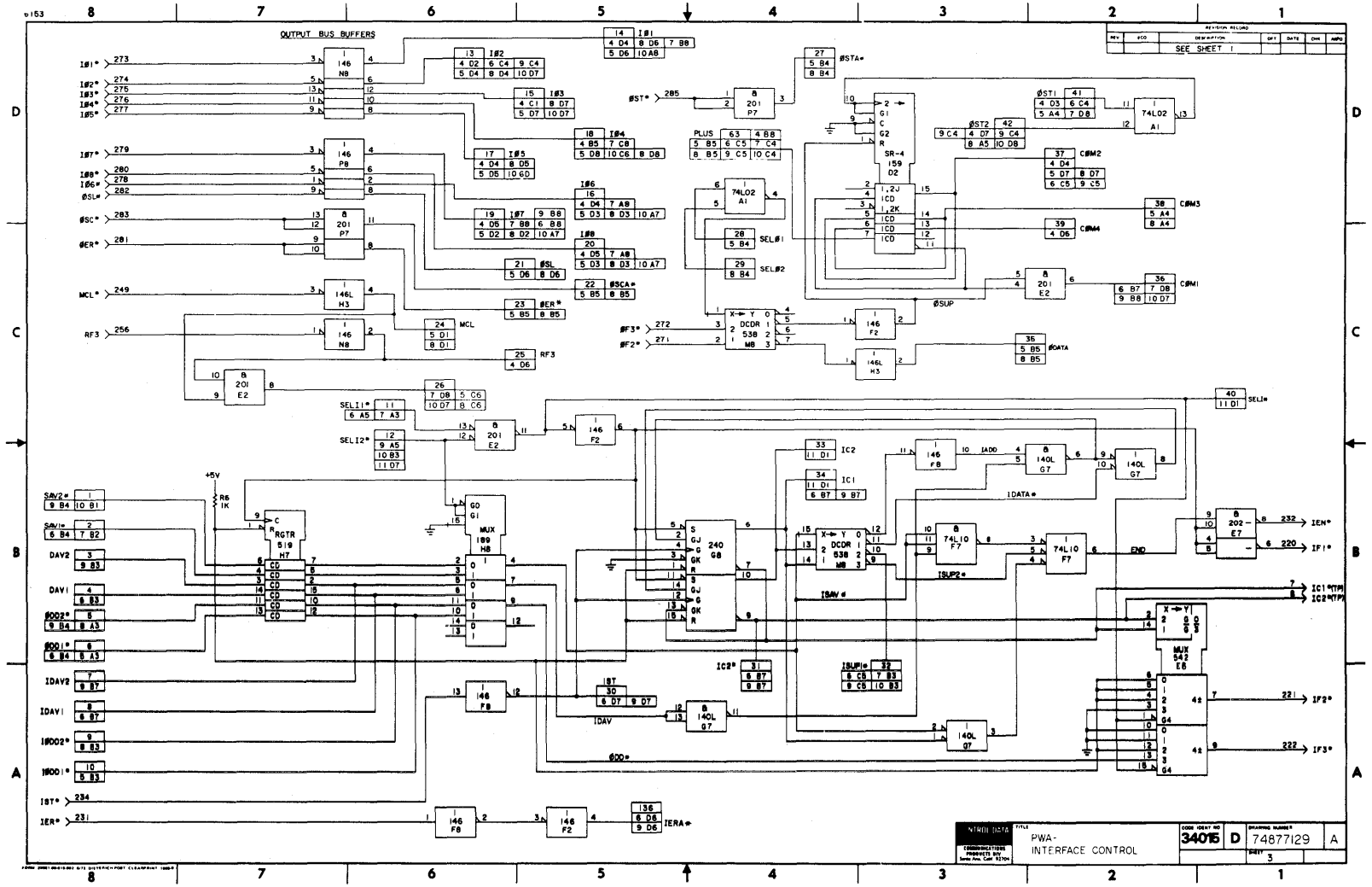
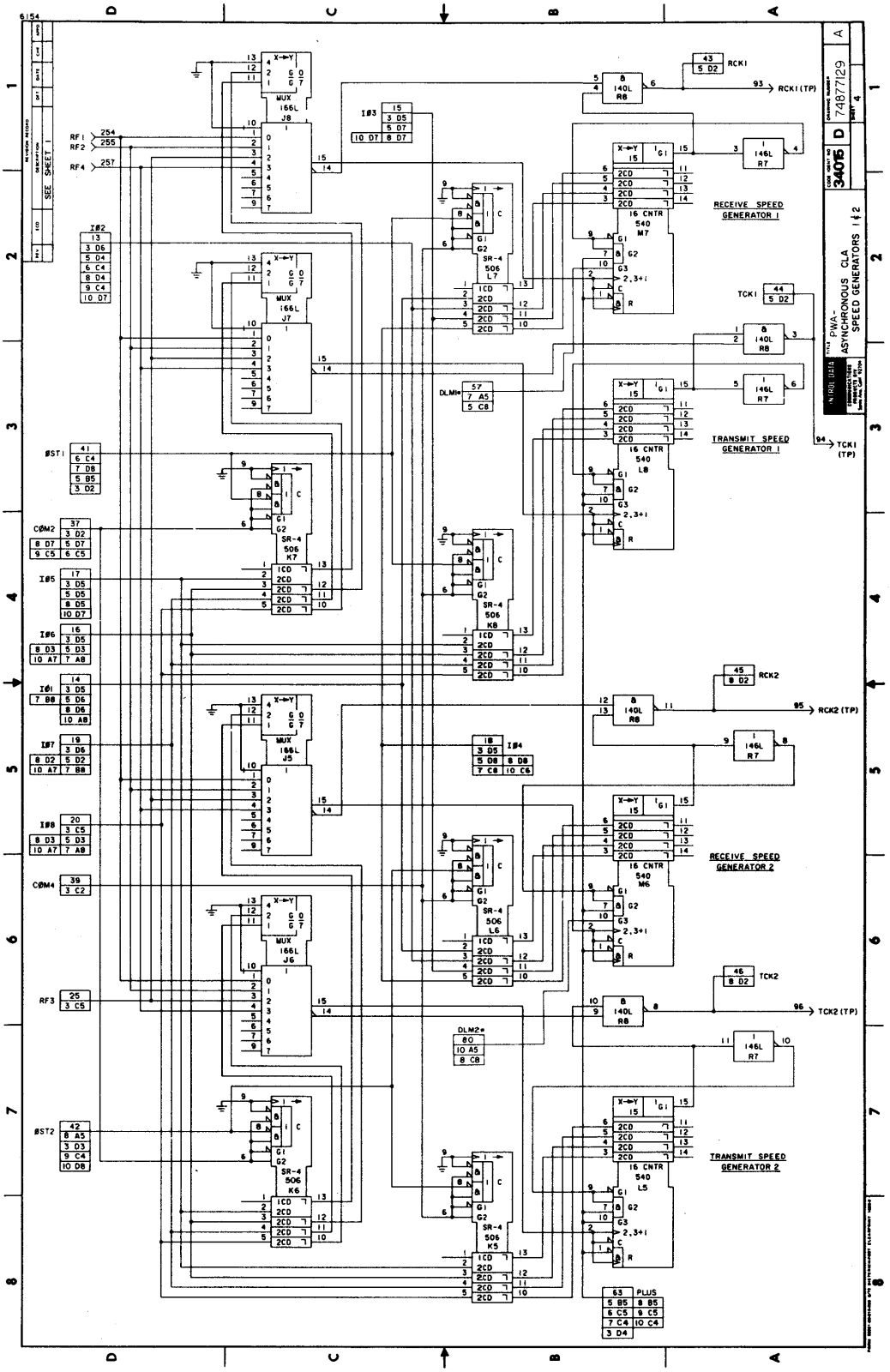


Figure 4-12. Speed Generator Timing Diagram

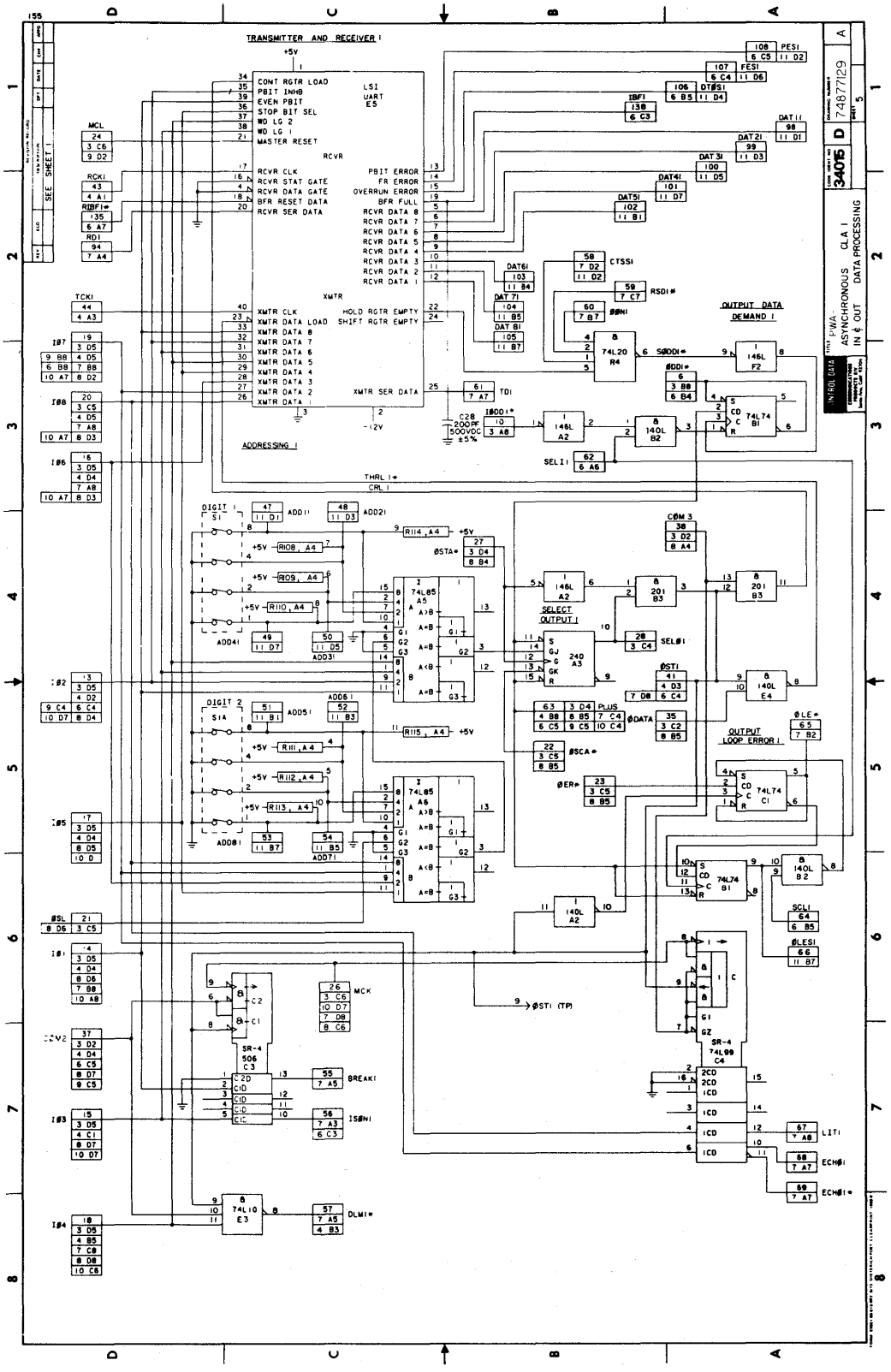
This section contains the logic diagram for the ACLA.

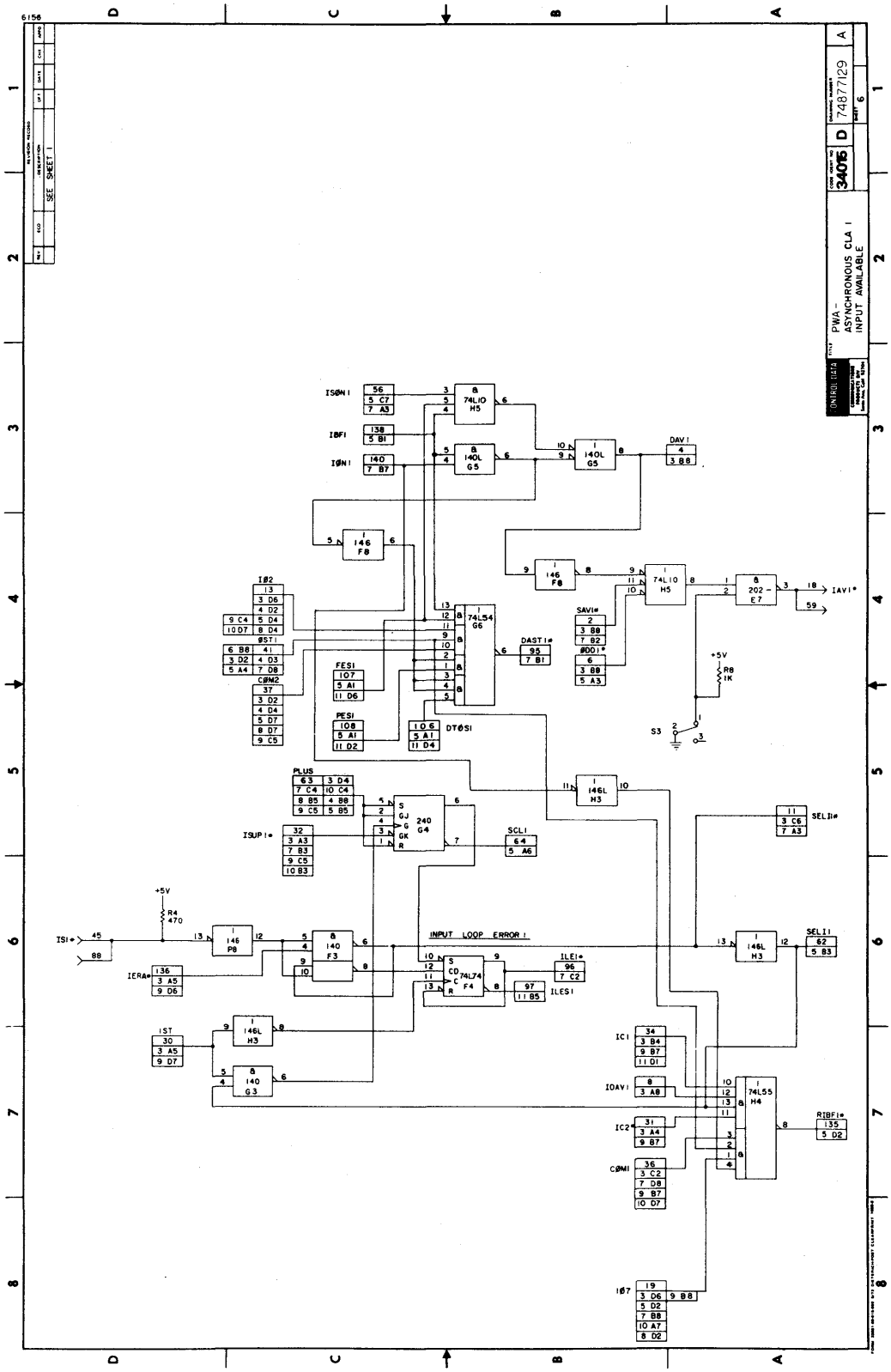

SEE SHEET 1
CR10 IN4002
+12VDC
+5VDC
GND
C4 1MF 100VDC +5%
C5 10MF 15VDC ±10%
C8-C15, C17-C26, C31, C32
TP
C3 1MF 100VDC ± 5%
C7, C16
CR9 IN4002
CIRCUIT CARD ASSEMBLY
VIEWED FROM COMPONENT SIDE
PIN 201 COMPONENT SIDE
PIN 1 NON - COMP SIDE
PIN 302 COMPONENT SIDE
PIN 102 NON - COMP SIDE
PIN 251 COMPONENT SIDE
PIN 51 NON - COMP SIDE
PIN 252 COMPONENT SIDE
PIN 52 NON - COMP SIDE
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS. 1/4 WATT ; ±5%
2. ALL CAPACITOR VALUES .01 MF
3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS
5VDC GND
14 PIN DUAL - IN - LINE 14 7
16 PIN DUAL - IN - LINE 16 8
4. NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS
DO NOT SCALE DRAWING
G SWAFFORD 5-1-79
PWA- ASYNCHRONOUS CLA — FULL RS232 / VARIABLE SPEED
D 34015
74877129 A
SCALE NONE
SHEET 2 OF 12

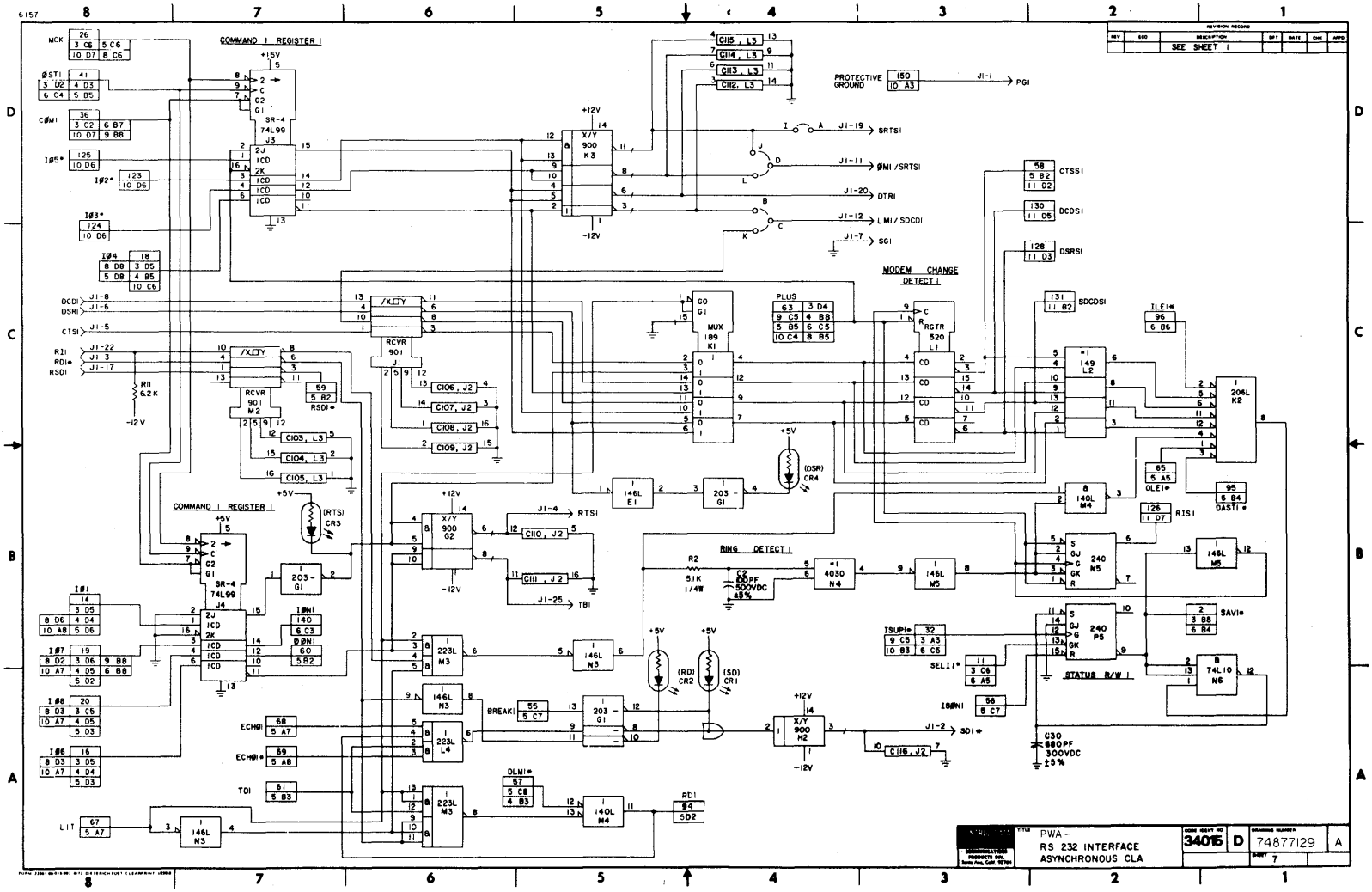

OUTPUT BUS BUFFERS
REVISION RECORD
SEE SHEET 1
PWA-
INTERFACE CONTROL
CODE IDENT NO 34015
D
74877129
A
SHEET 3

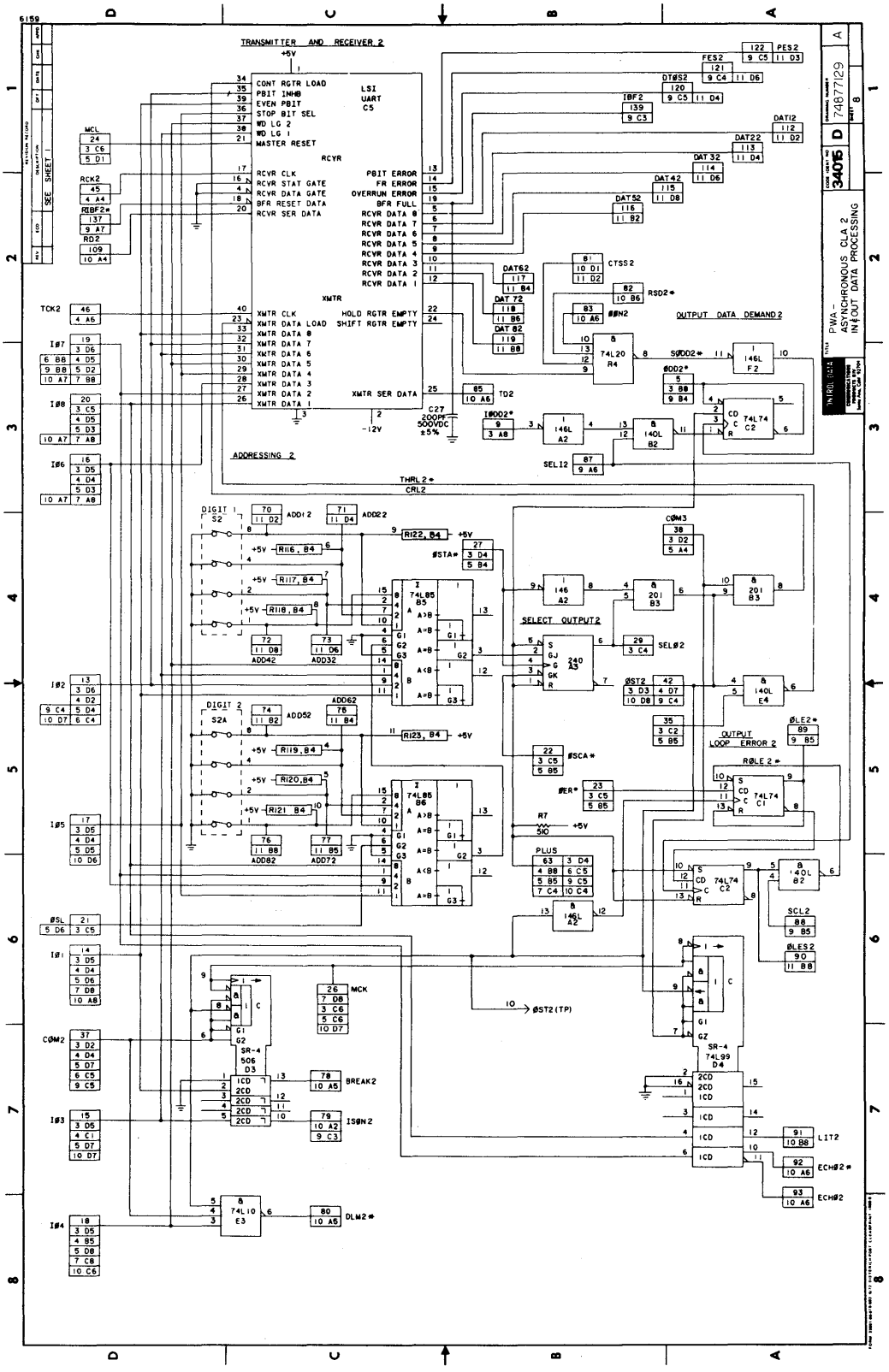


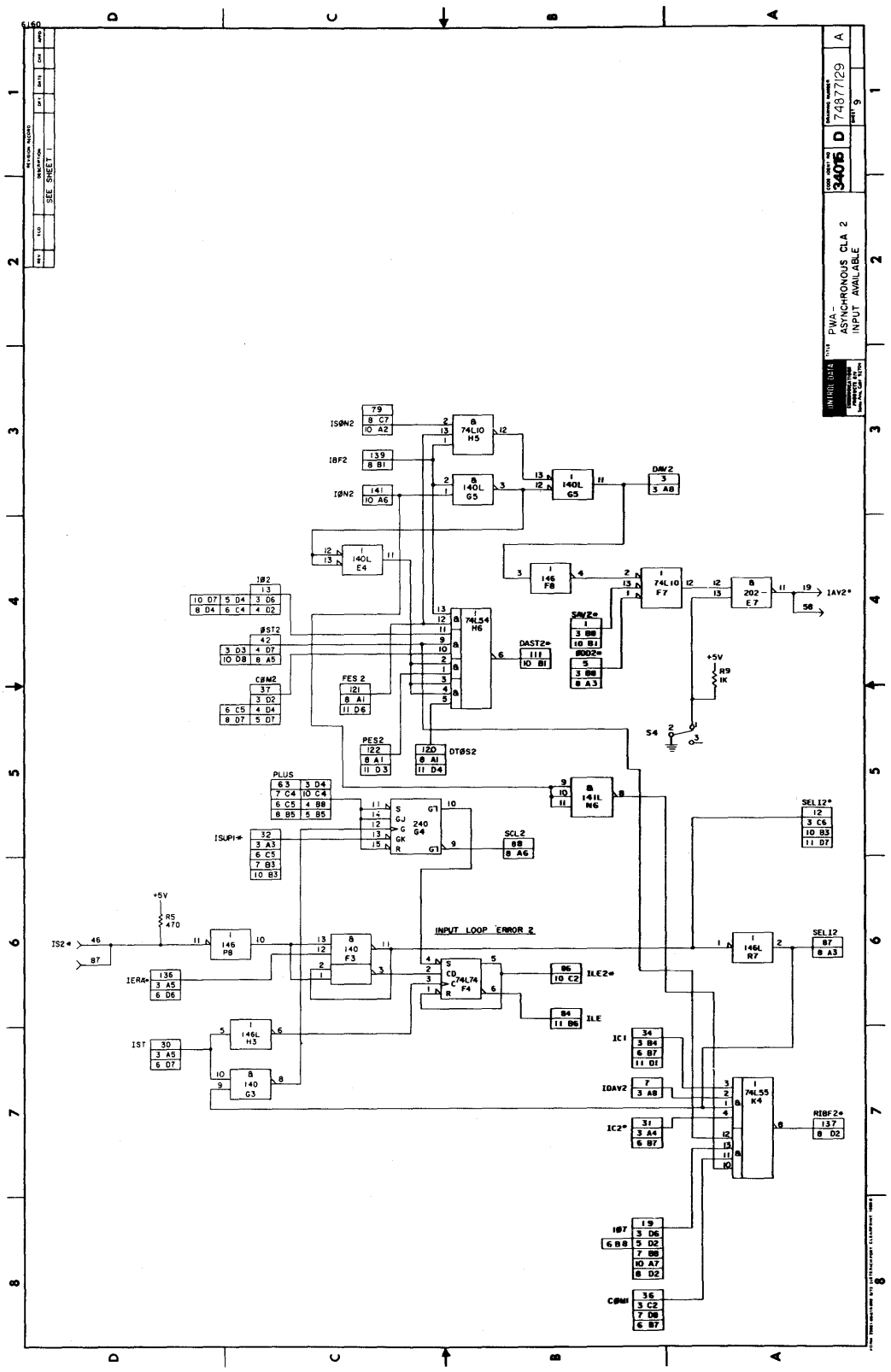
PWA-
ASYNCHRONOUS CLA
SPEED GENERATORS 1 & 2
INTROL DATA
34015
D
74877129
A
RECEIVE SPEED GENERATOR 1
TRANSMIT SPEED GENERATOR 1
RECEIVE SPEED GENERATOR 2
TRANSMIT SPEED GENERATOR 2
MUX 166L J8
MUX 166L J7
MUX 166L J5
MUX 166L J6
SR-4 506 L7
SR-4 506 K7
SR-4 506 K8
SR-4 506 L6
SR-4 506 K6
SR-4 506 K5
16 CNTR 540 M7
16 CNTR 540 L8
16 CNTR 540 M6
16 CNTR 540 L5
RCK1
RCK1 (TP)
TCK1
TCK1 (TP)
RCK2
RCK2 (TP)
TCK2
TCK2 (TP)
DLM1*
DLM2*
PLUS
RF1
RF2
RF4
RF3
ØST1
ØST2
CØM2
CØM4
I Ø1
I Ø2
I Ø3
I Ø4
I Ø5
I Ø6
I Ø7
I Ø8
SEE SHEET 1

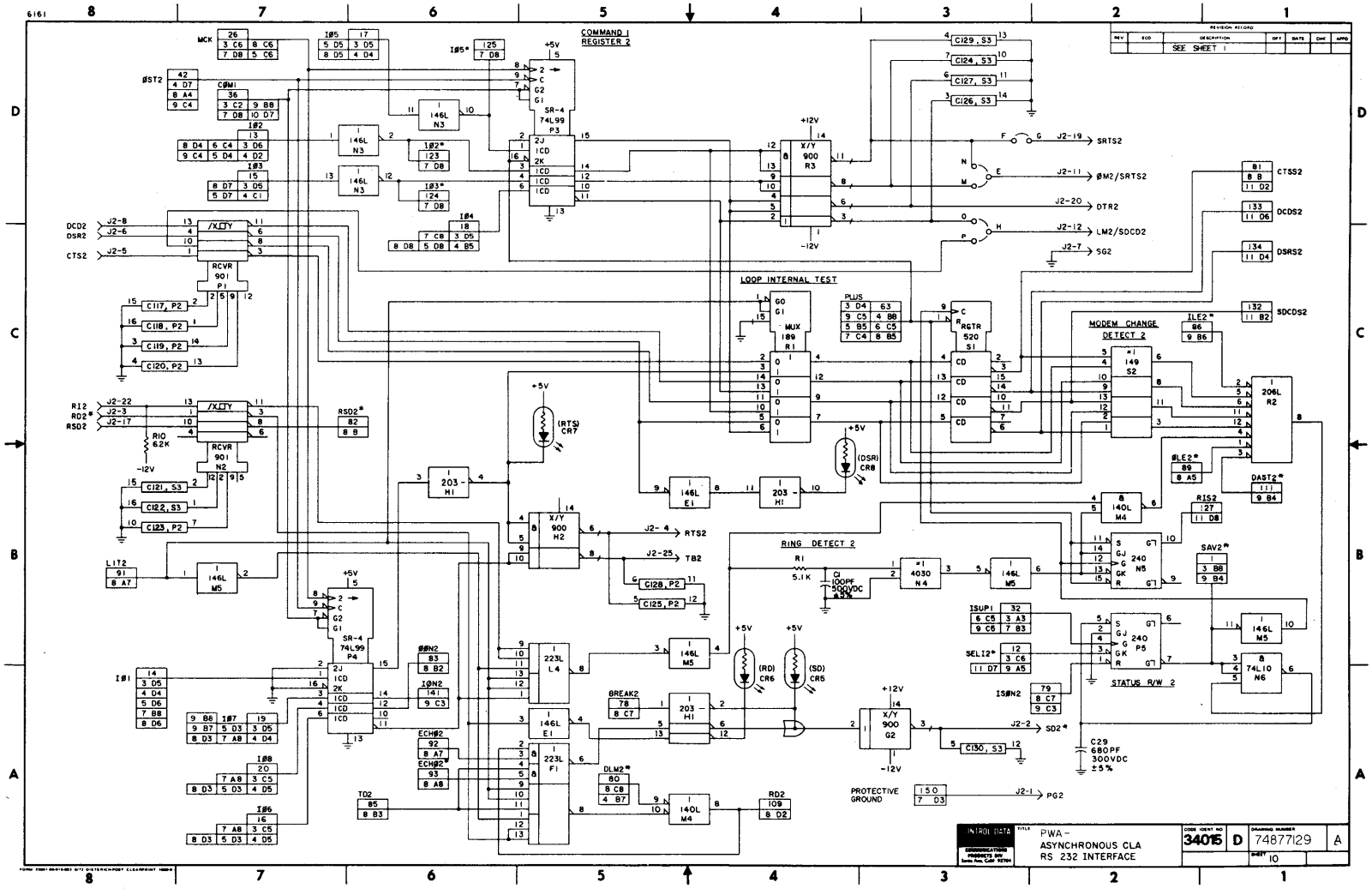

TRANSMITTER AND RECEIVER I
ASYNCHRONOUS GLA I
IN & OUT DATA PROCESSING
CONT RGTR LOAD
PBIT INHB
EVEN PBIT
STOP BIT SEL
WD LG 2
WD LG 1
MASTER RESET
RCVR
RCVR CLK
RCVR STAT GATE
RCVR DATA GATE
BFR RESET DATA
RCVR SER DATA
PBIT ERROR
FR ERROR
OVERRUN ERROR
BFR FULL
RCVR DATA 8
RCVR DATA 7
RCVR DATA 6
RCVR DATA 5
RCVR DATA 4
RCVR DATA 3
RCVR DATA 2
RCVR DATA 1
XMTR
XMTR CLK
XMTR DATA LOAD
XMTR DATA 8
XMTR DATA 7
XMTR DATA 6
XMTR DATA 5
XMTR DATA 4
XMTR DATA 3
XMTR DATA 2
XMTR DATA 1
HOLD RGTR EMPTY
SHIFT RGTR EMPTY
XMTR SER DATA
LSI UART E5
ADDRESSING I
OUTPUT DATA DEMAND I
SELECT OUTPUT I
OUTPUT LOOP ERROR I
SEE SHEET 1
74700900 E
5-5

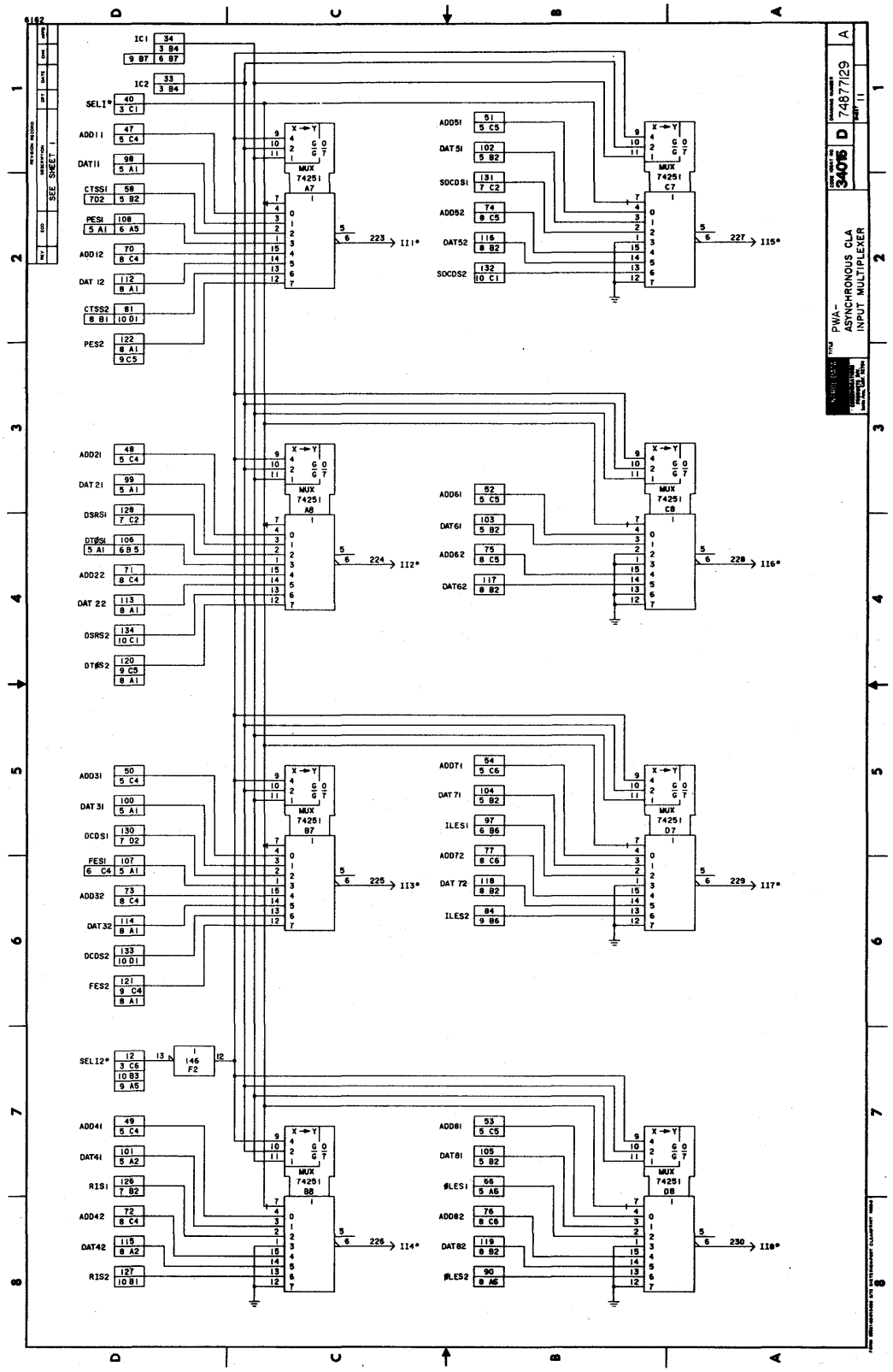

PWA - ASYNCHRONOUS CLA 1 INPUT AVAILABLE
ONTROL DATA
34015
D
74877129
A
SHEET 6
SEE SHEET 1
INPUT LOOP ERROR 1
74L10 H5
140L G5
146 F8
74L54 G6
202 - E7
146L H3
240 G4
146 P8
140 F3
74L74 F4
140 G3
74L55 H4
DAV1
IAV1*
SAV1*
ØDD1*
DAST1*
FES1
PES1
DTØS1
PLUS
ISUP1*
SCL1
SEL1*
SEL1
ILE1*
ILES1
IERA*
IST
IC1
IDAV1
IC2
CØM1
RIBF1*
IØ7
ISØN1
IBF1
IØN1
IØ2
ØST1
CØM2
+5V
R8 1K
S3
R4 470
IS1*


COMMAND I REGISTER I
MODEM CHANGE DETECT I
RING DETECT I
COMMAND I REGISTER I
STATUS R/W I
PROTECTIVE GROUND
SEE SHEET 1
PWA -
RS 232 INTERFACE
ASYNCHRONOUS CLA
34015
D
74877129
A
SHEET 7


TRANSMITTER AND RECEIVER 2
LSI UART C5
RCYR
XMTR
ADDRESSING 2
OUTPUT DATA DEMAND 2
SELECT OUTPUT2
OUTPUT LOOP ERROR 2
PLUS
SR-4 506 D3
SR-4 74L99 D4
PWA - ASYNCHRONOUS CLA 2 IN&OUT DATA PROCESSING
74877129
3401S


PWA-
ASYNCHRONOUS CLA 2
INPUT AVAILABLE
74877129
SEE SHEET 1
INPUT LOOP ERROR 2


COMMAND 1 REGISTER 2
LOOP INTERNAL TEST
MODEM CHANGE DETECT 2
RING DETECT 2
STATUS R/W 2
SEE SHEET 1
J2-19 SRTS2
J2-11 ØM2/SRTS2
J2-20 DTR2
J2-12 LM2/SDCD2
J2-7 SG2
J2- 4 RTS2
J2-25 TB2
J2-2 SD2*
J2-1 PG2
CTSS2
DCDS2
DSRS2
SDCDS2
PROTECTIVE GROUND
DRAWING NUMBER 74877129 A
SHEET 10

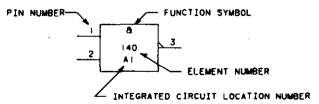

PWA-
ASYNCHRONOUS CLA
INPUT MULTIPLEXER
34016
D
74877129
A
11
SEE SHEET 1
IC1
IC2
SELI*
ADD11
DAT11
CTSS1
PES1
ADD12
DAT 12
CTSS2
PES2
ADD21
DAT21
DSRS1
DTØS1
ADD22
DAT 22
DSRS2
DTØS2
ADD31
DAT31
DCDS1
FES1
ADD32
DAT32
DCDS2
FES2
SELI2*
ADD41
DAT41
RIS1
ADD42
DAT42
RIS2
ADD51
DAT51
SDCDS1
ADD52
DAT52
SDCDS2
ADD61
DAT61
ADD62
DAT62
ADD71
DAT71
ILES1
ADD72
DAT 72
ILES2
ADD81
DAT81
ØLES1
ADD82
DAT82
ØLES2
MUX
74251
A7
A8
B7
B8
C7
C8
D7
D8
II1*
II2*
II3*
II4*
II5*
II6*
II7*
II8*
146
F2

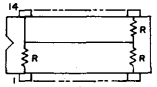
6650

REVISION RECORD

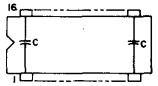
REV	ECO	DESCRIPTION	DRFT	DATE	CHK	APPD
		SEE SHEET 1				

CIRCUIT ELEMENT SYMBOLOGY



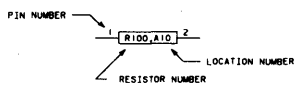


I.C. RESISTOR PACK
LOCATION U47,U48
10K

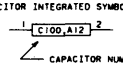


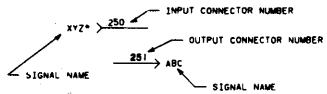
I.C. CAPACITOR PACK
LOCATION U25,U28,U41,U46
220PF

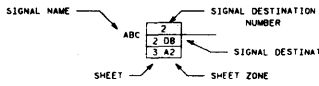
RESISTOR INTEGRATED SYMBOLOGY



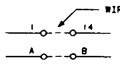
CAPACITOR INTEGRATED SYMBOLOGY







COMMON CONTROL BLOCK.
SIGNALS ENTERING THIS BLOCK
ARE COMMON TO MORE THAN ONE
SECTION OF THE CIRCUIT



IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
140	7400	TTL QUAD 2-INPUT NAND GATE
140L	74L00	TTL QUAD 2-INPUT NAND GATE
203	7405	TTL HEX INVERTER (OPEN COLLETOR)
141L	74L10	TTL TRIPLE 3-INPUT NAND GATE
146	7404	TTL HEX INVERTER
146L	74L04	TTL HEX INVERTER
—	74L54	TTL 4-WIDE 2 INPUT AND-OR-INVERTER
148L	74L02	TTL QUAD 2-INPUT NOR GATE
175	7474	TTL DUAL D-TYPE F/F
175L	74L74	TTL DUAL D-TYPE F/F
189	74187	MULTIPLEXER,TTL QUAD 2-INPUT GATE
201	7408	TTL QUAD 2-INPUT AND GATE
202	7403	TTL QUAD 2-INPUT NAND GATE
206L	74L30	TTL 8-INPUT NAND GATE
—	7486	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
208L	74L20	TTL DUAL 4-INPUT NAND GATE
223L	74L51	TTL DUAL 2-WIDE 2-3 IN AND-OR-INVERTER
240	9024	TTL DUAL J-K F/F
166L	93LI2	MULTIPLEXER,TTL 8-INPUT GATE
519	74174	LATCH,TTL 6-BIT D-TYPE
520	74175	LATCH,TTL 4-BIT D-TYPE
524L	74L85	COMPARATOR, TTL 4-BIT MAGNITUDE
538	9321	DECODER, TTL DUAL (1 OF 4)
542	8214	MULTIPLEXER TTL DUAL 4-BIT TRISTATE
540	74163	COUNTER,TTL 4-BIT BINARY
900	MC1488	DRIVER,DTL TO RS-232C QUAD LINE
901	MC1489A	RECEIVER, RS-232C TO DTL QUAD LINE
506	7495A	REGISTER, TTL 4-BIT RIGHT/LEFT SHIFT
—	7425I	MULTIPLEXER, TTL 8-INPUT TRISTATE
—	74L99	REGISTER,TTL 4-BIT RIGHT/LEFT SHIFT
—	9L24	TTL DUAL J-K F/F
—	9300	REGISTER,TTL 4-BIT UNIVERSAL
—	4030	QUAD 2-INPUT EXCLUSIVE-OR GATE
—	74L55	TTL 2-WIDE 4-INPUT AND-OR-INVERTER

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
⊓	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH IN=1BIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH IN=1BIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⊓	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

◇& OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
◺	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
—/—	NON-STANDARD LOGIC LEVEL
—⌇—	ANALOG OR NON-LOGIC LEVEL
—↗—	VARIABLE PARAMETER CONTROL
—○	IN=1BIT DESIGNATOR WITH POLARITY INDICATOR
—○	IN=1BIT DESIGNATOR

FUNCTION ABBREVIATIONS

ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER W IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

CONTROL DATA CORPORATION COMMUNICATIONS PRODUCTS DIV Santa Ana, Calif. 92705	PWA - ASYNCHRONOUS CLA - FULL RS232/VARIABLE	CODE IDENT NO 34015	D	74877129 A
			SHEET 12	

This section covers troubleshooting, card replacement, card repair, maintenance checks, and preventive maintenance. In order for the ACLA to operate, the system must be operating.

TROUBLESHOOTING

SPECIAL TOOLS

Troubleshooting is facilitated by the use of an Extender Board, CDC Part No. 74555600. The extender board is oriented so that its female connector is on the left when viewed from the front of the card cage assembly. The extender board is inserted into the card cage assembly in place of the suspected faulty ACLA card. The ACLA card is then inserted into the guide rails of the extender board. All points on the ACLA card are thus made readily accessible for troubleshooting.

A Loop External Test Connector, CDC Part No. 74715600, may be used for off-line diagnostics.

TEST EQUIPMENT

The following items of test equipment are recommended for troubleshooting the ACLA circuit cards:

1. Oscilloscope, Tektronix Model 475, or equivalent
2. Volt-Ohm-Milliammeter, Simpson Model 261, or equivalent.

ON-LINE DIAGNOSTICS

On-line diagnostics incorporated into the communications control program are used to isolate trouble to the module level. This method is enhanced by the operator, or repair personnel, periodically checking the error counters built into the on-line diagnostic system. This method is preferred since it usually provides successful trouble isolation without creating system downtime.

OFF-LINE DIAGNOSTICS

Off-line diagnostics (MST 041) are also used to isolate trouble to the module level. Solid or intermittent errors are found by using this method. In most cases, the solid error is located without difficulty, but the intermittent error may prove more difficult to detect, and more exhaustive checks are required to isolate the error.

A loop external test connector may be used to diagnose problems in the modem receivers and drivers. This connector tests only send data/receive data, request-to-send/clear-to-send, data-terminal-ready/data-set-ready, secondary request-to-send/secondary data carrier-detector, terminal busy/ring indicator signals. System downtime is a serious problem when off-line diagnostic methods are used, and should be avoided if possible.

PIN CONNECTIONS AND SIGNALS

The following tables serve as troubleshooting aids to facilitate the monitoring of ACLA interface signals. The LM-to-ACLA interface signals with associated pin connections are listed in table 6-1. The RS-232-C modem-to-ACLA interface signals and pin assignments for the 25-pin connections are listed in table 6-2.

CARD REPLACEMENT

To remove and reinstall ACLA cards in the card cage assembly, proceed as follows:

NOTE

ACLA cards can be removed from and reinstalled in the card slots while the system is operating.

1. Set CLA1 and CLA2 toggle switches to OFF.
2. Remove ACLA modem cables.
3. Trip two plastic ejectors, located at top and bottom of ACLA card handle, until tab connectors on rear edge of card are forced out of connectors on the LM backplane.
4. Grasp card by handle and pull card from card cage.
5. Inspect pins on cage backplane for bent, missing, or damaged pins.

CAUTION

Ensure that the 51-pin tab connectors on the rear edge of the card are properly aligned with their mating connectors on the card cage backpanel. Cross-slotting will destroy the backpanel.

TABLE 6-1. LOOP MULTIPLEXER-TO-ACLA INTERFACE SIGNALS

ACLA Pin No.	Signal Name	Mnemonic	Function	Signal To:
18/59†	Input Available ACLA1	IAV1	Notifies LM that ACLA1 has input	LM
19/58†	Input Available ACLA2	IAV2	Notifies LM that ACLA2 has input	LM
231	Input Error	IER	Notifies ACLA of error on last input frame	ACLA
232	Input End	IEN	Notifies LM that present information is last	LM
220 thru 222	Input Format Bits 1 thru 3	IF1 thru IF3	Informs LM of address, data, or supervision on information input bus	LM
45/88†	Input Select ACLA1	IS1	LM selects ACLA1 input	ACLA
46/87†	Input Select ACLA2	IS2	LM selects ACLA2 input	ACLA
234	Input Strobe	IST	LM notifies ACLA of access	ACLA
223 thru 230	Information Input Bits 1 thru 8	II1 thru II8	Information to LM (data, address, supervision)	LM
283	Output Select Clear	OSC	LM deselects ACLA output	ACLA
282	Output Select	OSL	LM presents ACLA address	ACLA
271 and 272	Output Format Cell Bits 2 and 3	OF2 and OF3	Informs ACLA of address, data, or supervision on information bus	ACLA
285	Output Strobe	OST	LM notifies ACLA of information present	ACLA
273 thru 280	Information Output Bits 1 thru 8	IO1 thru IO8	Information to ACLA (data, supervision, address)	ACLA
281	Output Error	OER	Notifies ACLA of errors in last frame	ACLA
249	Master Clear	MCL	Clears ACLA	ACLA
254	Ref Frequency 1	RF1	9.6 kHz Clock	ACLA
255	Ref Frequency 2	RF2	19.2 kHz Clock	ACLA
256	Ref Frequency 3	RF3	153.6 kHz Clock	ACLA
257	Ref Frequency 4	RF4	Special	ACLA

†Signals are available at two different pins depending on location of card in card cage.

TABLE 6-2. MODEM-TO-ACLA INTERFACE SIGNALS AND PIN CONNECTIONS

ACLA Pin No.	Description	Circuit Designation		Signal To:
		EIA RS-232C	CCITT V.24	
1	Protective Ground (PG)	AA	101	NA
2	Transmitted Data (SD)	BA	103	Modem
3	Received Data (RD)	BB	104	ACLA
4	Request to Send (RTS)	CA	105	Modem
5	Clear to Send (CTS)	CB	106	ACLA
6	Data Set Ready (DSR)	CC	107	ACLA
7	Signal Ground (SG)	AB	102	NA
8	Data Carrier Detector (DCD)	CF	109	ACLA
9	Not Used			
10	Not Used			
11	Originate Mode (OM)†	(non-EIA)	(non-CCITT)	Modem
11	Secondary Request to Send (SRTS)†	SCA	120	Modem
12	Secondary Data Carrier Detector (SDCD)†	SCF	122	ACLA
12	Local Mode (LM)†	(non-EIA)	(non-CCITT)	Modem
13	Not Used			
14	Not Used			
15	Not Used			
16	Not Used			
17	Restraint Detector (RSD)	(non-EIA)	(non-CCITT)	ACLA
18	Not Used			
19	Secondary Request to Send†	SCA	120	Modem
20	Data Terminal Ready (DTR)	CD	106.2	Modem
21	Not Used			
22	Ring Indicator (RI)	CE	125	ACLA
23	Not Used			
24	Not Used			
25	Terminal Busy	(non-EIA)	(non-CCITT)	Modem

†Selection of these signals is determined by strapping options. See table 4-1.

6. Insert proven card into cage slot and firmly engage card into connector on cage backplane.

7. Connect ACLA modem cables to connectors on card handle.

8. Set each address switch to proper setting.

9. Set CLA1 and CLA2 toggle switches to enabled (on) position.

LED INDICATORS

The LED indicators on the ACLA card handle are lighted when the LM is inputting from and outputting to the ACLA. Observing these LEDs can readily indicate modem or system errors to the operator. A blinking RD indicator indicates that the ACLA is receiving data from the modem; when the SD indicator is blinking, it indicates that the ACLA is sending data to the modem; a lighted RTS indicator shows that request-to-send is active from the ACLA; and a lighted DSR indicator shows that data-set-ready from the modem is active.

Suspected power failure to the card may be monitored for +5 vdc at the card.

PREVENTIVE MAINTENANCE

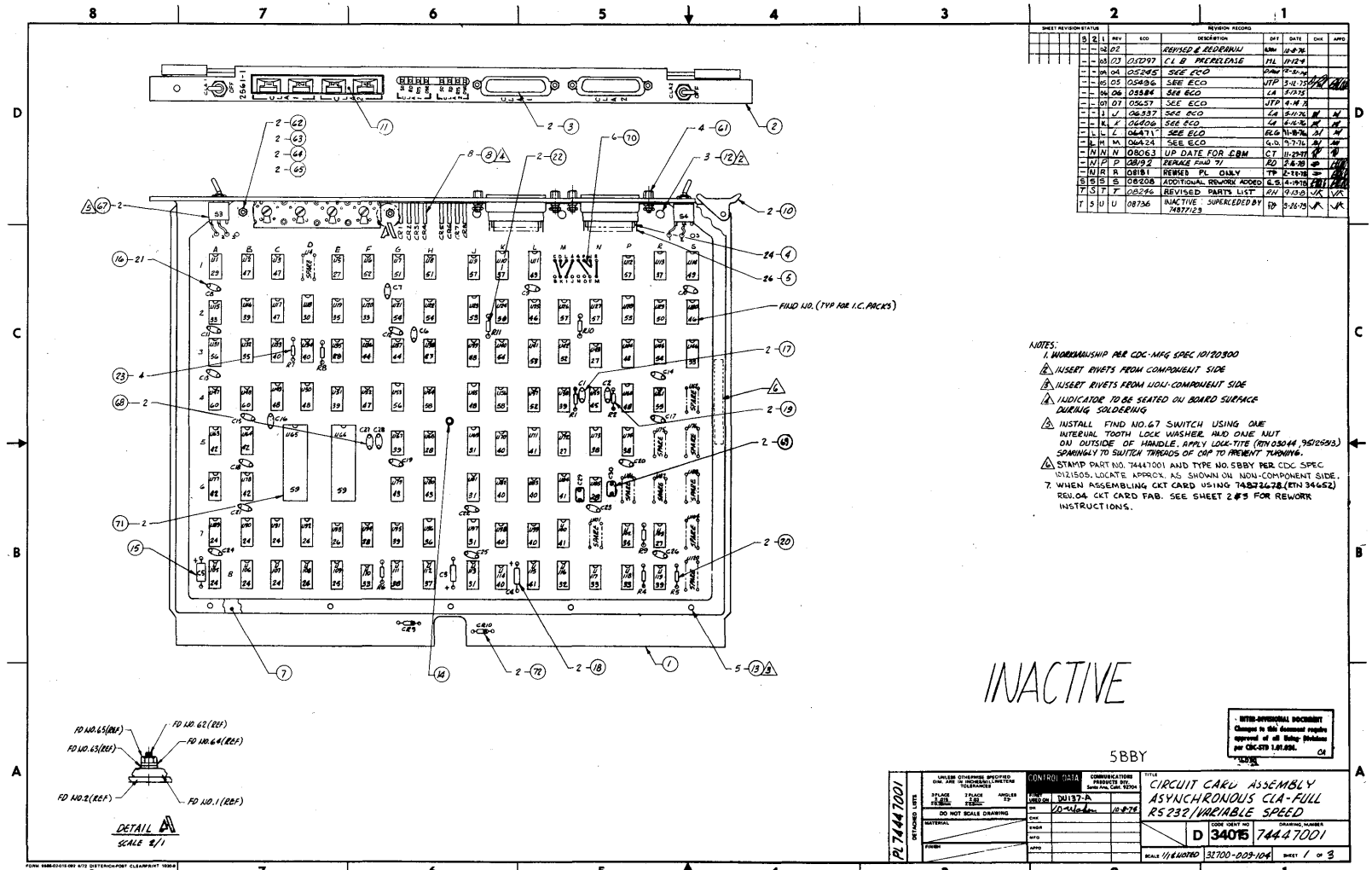
Preventive maintenance of the ACLAs is minimal. Excessive handling of cards may induce faults and is thus discouraged. However, the following should be performed at regular intervals:

1. Use spare cards periodically to ensure integrity of the spares.

2. Inspect connectors and cables for fraying or other damage.

3. When a card is removed, inspect connectors at card cage backplane for bent, damaged, or burned pins.

This section contains parts lists for the asynchronous communications line adapter and associated cable assemblies. The lists are provided primarily for reference purposes. Field repair of ACLA cards by parts replacement is neither authorized by any maintenance contract nor is such on-site repair recommended. System repair is to be accomplished via card replacement with the spares provided. However, in the event of multiple card failures, exhausting spares, the parts information is furnished.



NOTES:

1. WORKMANSHIP PER CDC-MFG SPEC 10120300
2. INSERT RIVETS FROM COMPONENT SIDE
3. INSERT RIVETS FROM NON-COMPONENT SIDE
4. INDICATOR TO BE SEATED ON BOARD SURFACE DURING SOLDERING
5. INSTALL FIND NO.67 SWITCH USING ONE INTERNAL TOOTH LOCK WASHER AND ONE NUT ON OUTSIDE OF HANDLE. APPLY LOCK-TITE (RTN 03044, 95125513) SPARINGLY TO SWITCH THREADS OF CAP TO PREVENT TURNING.
6. STAMP PART NO. 74447001 AND TYPE NO. 5BBY PER CDC SPEC 10121505. LOCATE APPROX. AS SHOWN ON NON-COMPONENT SIDE.
7. WHEN ASSEMBLING CKT CARD USING 74872678 (RTN 34652) REV.04 CKT CARD FAB. SEE SHEET 2 & 3 FOR REWORK INSTRUCTIONS.

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
02		REVISED & REDRAWN	[illegible]	10-8-76		
03	05097	CL B PRERELEASE	ML	11-12-4		
04	05245	SEE ECO	[illegible]	12-31-74		
05	05436	SEE ECO	JTP	3-12-75	[illegible]	[illegible]
06	05584	SEE ECO	LA	3-17-75		
07	05657	SEE ECO	JTP	4-14-75		
J	06337	SEE ECO	LA	5-11-76	[illegible]	[illegible]
K	06406	SEE ECO	LA	6-16-76	[illegible]	[illegible]
L	06471	SEE ECO	ELG	11-18-76	[illegible]	[illegible]
M	06424	SEE ECO	G.D.	9-7-76	[illegible]	[illegible]
N	08063	UP DATE FOR CBM	CT	11-29-77	[illegible]	[illegible]
P	08192	REPLACE FIND 71	RD	2-16-78	[illegible]	[illegible]
R	08181	REVISED PL ONLY	TP	2-22-78	[illegible]	[illegible]
S	08208	ADDITIONAL REWORK ADDED	G.S.	4-19-78	[illegible]	[illegible]
T	08246	REVISED PARTS LIST	RH	9-13-8	[illegible]	[illegible]
U	08736	INACTIVE: SUPERCEDED BY 74877123	[illegible]	3-26-79	[illegible]	[illegible]

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.034.

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

DO NOT SCALE DRAWING

CIRCUIT CARD ASSEMBLY
ASYNCHRONOUS CLA-FULL
RS232/VARIABLE SPEED

D 34015 74447001

SCALE 1/1 & NOTED — 32700-009-104 — SHEET 1 OF 3

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
744-7001	U	INA	D	ASYNCH CLA FULL RS232 VARIABLE	DM	2951	11/30/77	09/26/79	2/ 2

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN RC	S OR N
57	A	3611A6501	400	PC	IC CHIP TYPE 1489	IN	J08246	091878	PPP4		N
14	A	38807901	100	PC	TERMINAL HOLLOW SINGLE END.103	IN			PPP3		N
17	A	38836926	200	PC	CAPACITOR,SILVERED MICA 100 PF	IN			PPP4		N
66	A	38836933	200	PC	CAP SILVERED MICA 200PF 500V	IN			PPP4		N
69	A	38836951	200	PC	CAP, SILVERED MICA 680PF	IN			PPP4		N
33	B	39436700	500	PC	INT CKT 7404	IN	J08181	022278	PPP4		N
71	A	51858100	200	PC	SOCKET,IC,PC TYPE 40 PIN	IN	J08192	021778	PPP4		N
40	A	52335500	800	PC	ACCEPT.TEST SHIFT REG.4031T7495	IN			PPP4		N
70	C	52629925	500	IN	WIRE 26AWG KYNAR GREEN	IN			PPP3		N
3	C	53397814	200	PC	CONN-RECTANGULAR,MALE PLUG	IN			PPP4		N
44	A	66249099	200	PC	MICROCIRCUIT TYPE 7400 (SPEC)	IN	J08181	022278	PPP4		N
15	A	72006016	100	PC	CAPACITOR 10 UF 15V TANT	IN			PPP4		N
66	D	74513501	REF	PC	ASYNCH CLA FULL RS232 VARIABLE	IN					N
2	C	74618702	100	PC	HANDLE SERSORNG ASYNCH CLA	IN			ATV4		N
7	C	74632700	100	PC	INSULTR CKD STIFFENER	IN			PPP4		N
53	A	74870525	400	PC	CAP ARRAY 220 PF	IN			PPP4		N
8	A	74870586	800	PC	INDICATOR LED	IN			PPP4		N
16	A	74870616	2100	PC	CAPACITOR CER DISC .01UF 25VDC	IN			PPP4		N
4	A	74870625	2400	PC	PIN RT ANGLE CONTACT 2ND ROW	IN			PPP4		N
5	A	74870626	2000	PC	PIN RT ANGLE CONTACT 3RD ROW	IN			PPP4		N
10		74870632	200	PC	EJECTOR CKT CARD WHT NYLON	IN			PPP4		N
11	A	74870636	100	PC	SWITCH THUMBWHEEL 4 STATION	IN			PPP4		N
67	A	74872299	200	PC	SWTCH LOCKNG TOGGLE 1 THRU 4 P	IN			PPP4		N
1	D	74872076	100	PC	ASYNC CLA RS232 VARIABLE FAB.	IN			PPP4		N
60	A	75009943	200	PC	RES PKG 10 OK OHMS	IN			PPP4		N
25	A	88881700	100	PC	IC 8214 TTL DUAL 4/1 MUX	IN	J08181	022278	PPP4		N
36	A	88882600	100	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN	J08181	022278	PPP4		N
49	A	88882900	200	PC	IC 74175 TTL QUAD D F/F W/CLR	IN	J08181	022278	PPP4		N
38	A	88889400	300	PC	IC 9024 TTL DUAL FLIP/FLOP	IN	J08181	022278	PPP4		N
46	A	88895700	200	PC	IC 7486 TTL QUAD 2-IN EXCL OR	IN	J08181	022278	PPP4		N
37	A	88896400	300	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN	J08181	022278	PPP4		N
35	A	88897100	300	PC	IC 7408 TTL QUAD 2-INPUT AND	IN	J08181	022278	PPP4		N
61	C	94288124	400	PC	CONNECTOR LOCKING DEVICE	IN			PPP4		N
26	A	9E744154	100	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN	J08181	022278	PPP4		N
					NUMBER OF LINE ITEMS = 73						
					HIGHEST FIND NUMBER = 72						

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74447001	U	INA	D	ASYNCH CLA FULL RS232 VARIABLE	DM	2951	11/30/77	09/26/79	1/ 2

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN RC	S OR N
62	A	99006005	200	PC	SCR MACH FLAT FHL H NO. 2	IN			PPP4		N
12	C	99J3J409	300	PC	RIVET TUBULAR	IN			PPP3		N
13	C	99J3J419	500	PC	RIVET TUBULAR	IN			PPP3		N
65	A	9J1251J2	200	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP3		N
63	A	9J1256J2	200	PC	PLAIN WASHERS	IN			PPP3		N
64	A	9J1258J2	200	PC	SPRING LOCK WASHERS (MED.)	IN			PPP3		N
52	A	15111400	500	PC	INTEGRATED CIRCUIT 74L51	IN			PPP4		N
39	A	15112300	600	PC	INT CKT 74L00	IN			PPP4		N
27	B	15112700	500	PC	INT CKT 74L04	IN			PPP4		N
29	A	15116000	100	PC	INTEGRATED CIRCUIT 74L02	IN			PPP4		N
41	A	15117000	400	PC	IC-SYNC 4 BIT COUNTER 74163	IN			PPP4		N
59	A	15125700	200	PC	I.C. TR1602A UNIV. ASYNCHRON	IN			PPP4		N
45	A	15134200	100	PC	IC QUAD EXCL ORNOR 4030	IN			PPP4		N
24	A	15142800	800	PC	IC 74251	IN			PPP4		N
28	A	15142900	400	PC	MICROCIRCUIT TYPE 74L10 TTL 3	IN			PPP4		N
55	A	15143000	100	PC	MICROCIRCUIT TYPE 74L20 TTL DU	IN			PPP4		N
50	A	15143100	200	PC	MICROCIRCUIT TYPE 74L30 TTL 8	IN			PPP4		N
43	A	15143200	200	PC	IC 74L54 TTL 4-WD AND/OR INVRT	IN			PPP4		N
31	A	15143600	400	PC	MICROCIRCUIT TYPE 93L12	IN			PPP4		N
56	A	15143700	200	PC	MICROCIRCUIT TYPE 9L24 DL JK F	IN			PPP4		N
48	A	15144000	600	PC	MICROCIRCUIT TYPE 74L99 4 BIT	IN			PPP4		N
58		15156000	200	PC	IC 74L55 J	IN			PPP4		N
47		15156100	400	PC	IC 74L74 J	IN			PPP4		N
30	A	15158200	100	PC	I C 9300 74195	IN	J08181	022278	PPP4		N
51	A	15161300	200	PC	I.C. TYPE 7405 TTL-HEX INVERT.	IN	J08181	022278	PPP4		N
57	C	15163326	400	PC	IC 1489A RECEIVER RS232C DTL	IN	J08246	100978	PPP4		N
57	C	15163326	400	PC	IC 1489A RECEIVER RS232C DTL	OUT	J08246	041379	PPP4		N
32	C	15163327	100	PC	IC 9321 TTL DUAL DECODER	IN	J08181	022278	PPP4		N
42	A	17184000	400	PC	IC 74L85 4BIT MAGNITUDE COMPRTR	IN			PPP4		N
20	C	245JJ055	200	PC	RES FXD .25W 47J OHMS	IN			PPP4		N
23	C	24500063	400	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
19	C	24500080	200	PC	RES FXD .25W 5100 OHMS	IN			PPP4		N
22	C	24500082	200	PC	RES FXD .25W 6200 OHMS	IN			PPP4		N
72	C	24519100	200	PC	RECTIFIER SILICON 750 MA	IN			PPP4		N
18	C	24521125	200	PC	NOT FOR NEW DESIGN (CAPACITOR)	IN			PPP4		N
54	A	38166400	400	PC	IC CHIP,TYPE 1488	IN			PPP4		N

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

DWN	LEVENTHAL	7/14	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY ASYNCHRONOUS RS232 TO 103A/118		74657700/03	D
ENG		7-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON		SHEET 1 OF 6	
APPR			CODE IDENT 34015	31770-009-070			

SHEET REVISION STATUS

6	5	4	3	2	1	REV	ECO	DESCRIPTION	DRFT	DATE	APP
–	–	–	00	00	00	00	–	PRELIM RELEASE	ML	10/31/74	
–	–	–	00	01	01	01	–	REV QTY FD NO. 415	LA	1-3-75	
–	–	–	00	01	02	02	05360	CL "B" PREPELEASED	DMM	4-10-75	
–	–	–	00	03	03	03	06707	CL II CONN. CONTACT CHG	DMM	1-11-77	
–	–	04	00	04	04	04	08139	FIND NO. 5 WAS 6203601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
–	–	A	A	A	A	A	08063	CLASS A RELEASE	TP	1-27-78	
–	–	A	B	B	B	B	08290	ADDED TABS TO DWG	AV	5-10-78	
–	–	A	B	C	C	C	D8744	CORRECT P2 PIN1 LOCATION, CORRECT HOOD ORIENTATION	VD	7-12-79	
D	D	D	D	D	D	D	08622	CORRECTED DRAWING ADDED : WIRE LIST	TP	8-22-79	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

NOTES:

PL 74657700/03
DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

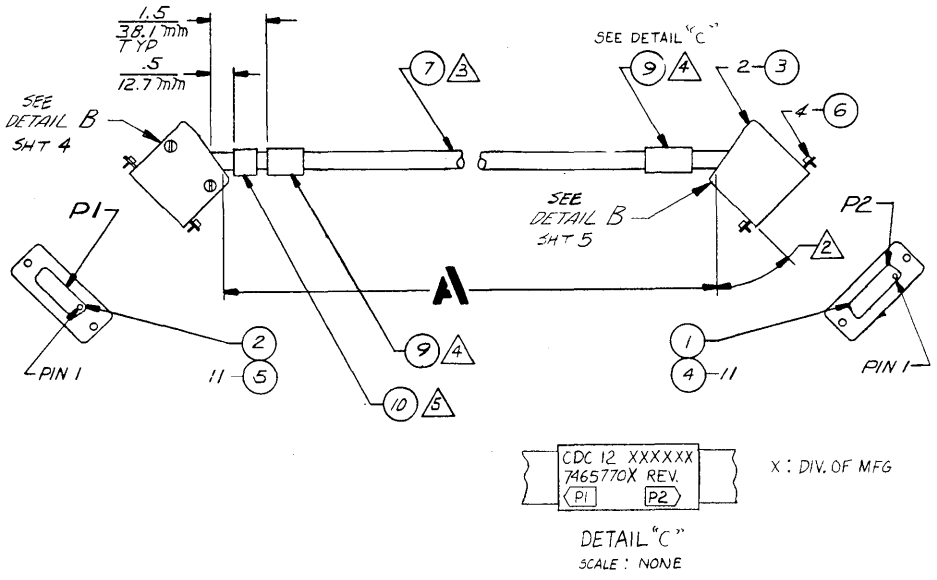
COMMUNICATIONS SYSTEMS DIV. Anaheim, Calif. 92803	CODE IDENT 34015	SHEET 2 OF 6	A	DOCUMENT NO. 74657700/03	REV. D

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300.
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR SHELL & PIN 1.
4. FIND NUMBER 9 TO BE MARKED WITH P/N 74657700/03, CDC 12, DIV OF MFG, REV, CONNECTOR NUMBER P1 AND P2, DATE CODE (E.G. 12/78) PER CDC STD 1.30.008.
5. P1 END TO BE COLOR IDENTIFIED BLUE WITH FIND NUMBER 10.
6. STRIP BACK INSULATION AT BOTH ENDS OF WIRE .25 (6.4mm).
7. SLEEVE ALL BARE WIRE USING FIND NO. 13.

FORM 19245 02 015 092 10/78 DIETERICH POST CLEARPRINT 1020 PRINTED IN U.S.A.

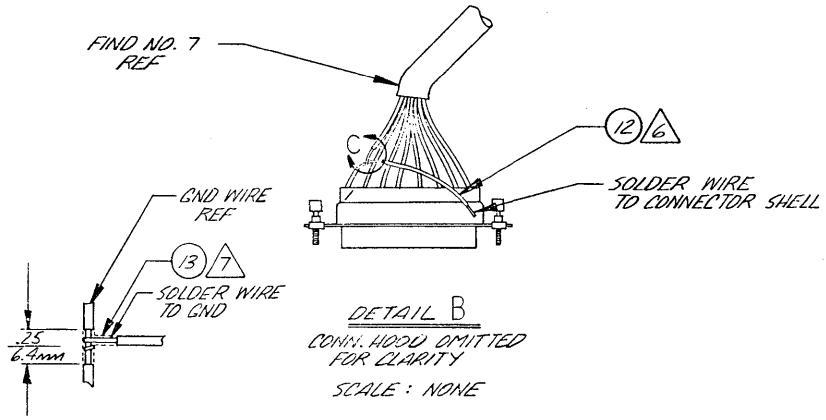
CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 6	DOCUMENT NO. 74657700/03	REV. D



CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 6	DOCUMENT NO. 74657700/03	REV. D

CDC NO.	LENGTH		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74657700	50.0	15.24	31770
74657701	100.0	30.48	38097
74657702	150.0	45.72	38098
74657703	200.0	60.96	38099

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 5 OF 6		DOCUMENT NO. 74657700/03	REV. D



DETAIL B
CONN. HOOD OMITTED FOR CLARITY
SCALE : NONE

DETAIL C
SCALE : NONE

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 6 OF 6	WL	DOCUMENT NO. 74657700/03	REV. D

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	7	22	SHIELD WIRE	SEE TABLE (SHEET 4)	CONN P1	1	5	CONN P2	1	4	PROTECTIVE GND (AA)
2			BLK			2			2		TRANSMITTED DATA (BA)
3			BRN			3			3		RECEIVED DATA (BB)
4			RED			4			4		REQUEST TO SEND (CA)
5			ORN			5			5		CLEAR TO SEND (CB)
6			YEL			6			6		DATA SET READY (CC)
7			GRN			7			7		SIGNAL GND (AB)
8			BLU			8			8		RCVD LINE SIG DET (CF)
9			VIO			20			20		DATA TERM READY (CD)
10			GRY			22			22		RING INDICATOR (CE)
11			WHT			25	5		25	4	TERM BUSY (-)
12			WHT/BLK								NOT USED
13	7	22	WHT/BLK		CONN P1			CONN P2			NOT USED

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
7465773J	C	CLA	A	CBL AY ASYNCH RS232 TO 103A 11	DM	2551	01/29/78	09/11/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP3		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP3		N
9	B	39296400	200	PC	LABEL, CABLE MARKING	IN	JJ8622	J82279	PPP4		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN			PPP4		N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
5	A	62013606	1100	PC	SOCKET	IN			PPP3		N
1	A	62J137J2	100	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN			PPP3		N
7	A	74871633	6JJJJ	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	J08500		PPP4		N
10	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	J08500		PPP4		N
6	A	74873611	200	PC	RETAINER MALE SCREW	IN	JJ8622	J82279	PPP4		N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74657731	J	CLA	A	CBL AY ASYNC CLA TO 103A 100FT	DM	2551	07/23/78	09/11/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008290	J72678	PPP3		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN	008290	J72678	PPP3		N
9	B	39296400	200	PC	LABEL, CABLE MARKING	IN	008622	082279	PPP4		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN	008290	072678	PPP4		N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN	008290	072678	PPP4		N
5	A	62013606	1100	PC	SOCKET	IN	008290	072678	PPP3		N
1	A	62J137J2	100	PC	CONN PIN HOUSING 25 PIN	IN	008290	072678	PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN	008290	072678	PPP3		N
7	A	74871633	12JJJJ	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008290	072678	PPP4		N
10	A	74871674	140J	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	JJ8290	J72678	PPP4		N
6	A	74873611	200	PC	RETAINER MALE SCREW	IN	JJ8622	J82279	PPP4		N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
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ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74657702	D	CLA	A	CBL AY ASYNC CLA TO 103A 15JFT	DM	2551	07/23/76	09/11/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S ON N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008290	072678	PPP3		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN	008290	072678	PPP3		N
9	B	39296400	200	PC	LABEL, CABLE MARKING	IN	006622	082279	PPP4		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN	008290	072678	PPP4		N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN	008290	072678	PPP4		N
5	A	62013606	1100	PC	SOCKET	IN	008290	072678	PPP3		N
1	A	62013702	100	PC	CONN PIN HOUSING 25 PIN	IN	008290	072678	PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN	008290	072678	PPP3		N
7	A	74871633	100000	IN	CABLE 13 CONDUCTOR W GA SHIEL	IN	008290	072678	PPP4		N
10	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	008290	072678	PPP4		N
6	A	74873611	200	PC	RETAINER MALE SCREW	IN	006622	082279	PPP4		N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74657703	D	CLA	A	CBL AY ASYNC CLA TO 103A 200FT	DM	2551	07/23/76	09/11/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S ON N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008290	072678	PPP3		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN	008290	072678	PPP3		N
9	B	39296400	200	PC	LABEL, CABLE MARKING	IN	006622	082279	PPP4		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN	008290	072678	PPP4		N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN	008290	072678	PPP4		N
5	A	62013606	1100	PC	SOCKET	IN	008290	072678	PPP3		N
1	A	62013702	100	PC	CONN PIN HOUSING 25 PIN	IN	008290	072678	PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN	008290	072678	PPP3		N
7	A	74871633	24000	IN	CABLE 13 CONDUCTOR W GA SHIEL	IN	008290	072678	PPP4		N
10	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	008290	072678	PPP4		N
6	A	74873611	200	PC	RETAINER MALE SCREW	IN	006622	082279	PPP4		N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

DWN	LEVENTHAL	1/24/75	CONTROL DATA	TITLE CABLE ASSY ASYNCHRONOUS RS232 TO TERMINAL	PREFIX	DOCUMENT NO. 74657900	REV G
CHKD							
ENG		1-25-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG							
APPR			CODE IDENT 34015	FIRST USED ON XA135-A	31771-009-070	SHEET 1 OF 4	

SHEET REVISION STATUS

4	3	2	1
-	00	00	00
-	00	01	01
-	00	01	02
-	0	0	0
-	D	E	E
F	D	F	F
F	D	F	G

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	PRELIM RELEASE	ML	10-31-74	
01	-	REV ALL FIND NO.S	LA	1-2-75	
02	05360	CL "B" PRERELEASED	DPM	1-10-75	
D	06248	SEE ECO	LA	3-5-76	
E	06707	CL B CONN. CONTACT CHG	DPM	1-11-77	
F	08139	FIND NO. 3 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
G	08063	CLASS "A" RELEASE CBM	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

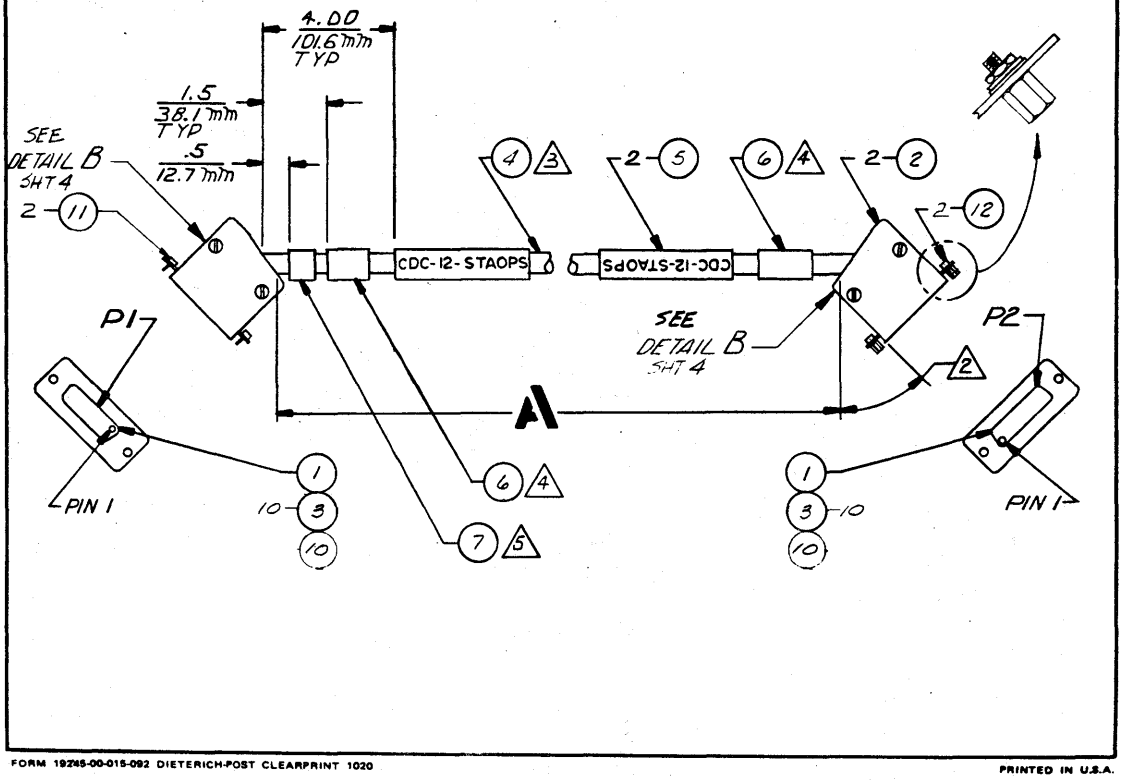
NOTES:

	DN 74657900
WL 74658000	PL 74657900
ASSOC. LISTS	DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

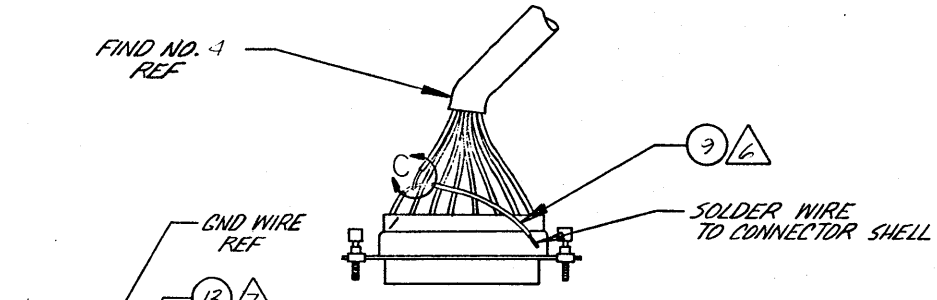
31771-009-070

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	DOCUMENT NO. 74657900	REV. F



FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CDC NO.	LENGTH A		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74657900	50.0	15.24	31771



DETAIL B
CONN. HOOD OMITTED FOR CLARITY
SCALE : NONE

DETAIL C
SCALE: NONE

DWN	LEVENTHAL	10/31/79	CONTROL DATA	TITLE CABLE ASSY ASYNCHRONOUS RS232 TO TERMINAL	PREFIX DN	DOCUMENT NO. 74657900	REV F
CHKD							
ENG	D Dal	1-15-79	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON XA135-A	31771-009-070		SHEET 1 OF 2
APPR			CODE IDENT 34015				

SHEET REVISION STATUS

2	1
00	00
01	01
01	02
D	D
D	E
F	F

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	—	PRELIM RELEASE	ML	10-31-79	
01	-	REV NOTES 3, 4 & 5	LA	1-2-79	
02	05360	CL 8" ARERELEASED	DPM	1-10-79	
D	06248	SEE ECO	LA	3-9-76	
E	06707	CLI CONN. CONTACT CHG.	DPM	1-11-77	
F	08139	FIND NO. 3 WAS 62013601 ADDED: BLK WIRE (GND)	FLG	1-19-78	

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31771-009-070

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO. 74657900	REV. F

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300.
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR SHELL AND PIN 1
4. FIND NUMBER (6) TO BE MARKED PER 10121508 WITH PART NUMBER 74657700, CONNECTOR NUMBER P1 OR P2, AND SERIAL NUMBER.
5. P1 END TO BE COLOR IDENTIFIED BLUE WITH FIND NUMBER (7).
6. STRIP BACK INSULATION AT BOTH ENDS OF WIRE .25(6.4mm).
7. SLEEVE ALL BARE WIRE USING FIND NO. 13.

FORM 19246-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74657900	G	CLA	A	CBL AY ASYNC RS232 TO TERMINAL	DM	2551	01/29/78	01/29/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN HC	S OR N
10	A	15003409	2.00	IN	WIRE ELECT,20 GA,PVC UL 1061	IN			PPP2		N
13	C	24534706	.100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
9	C	24548301	.100	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP5		N
2	A	51892202	1.00	PC	HOOD CONNECTOR	IN					N
5		51904701	1.00	PC	CABLE LABLE	IN					N
1	C	62013502	1.00	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
3	A	62013606	1.00	PC	SOCKET	IN					N
6	B	73995400	1.00	PC	NMPLT KIT BLNK SMALL CABLES	IN			PPP4		N
8	A	74658000	REF	PC	WIRE LIST ASYNC RS232 TO TERM	IN			RFE4		N
4	A	74871632	40.00	IN	CABLE 9 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
7	A	74871674	2.00	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	008500		PPP4		N
11	A	74873611	1.00	PC	RETAINER MALE SCREW	IN			PPP4		N
12	C	94288024	1.00	PC	CONNECTOR LOCKING DEVICE	IN			PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER ARDEN MILLS

AA 2708 REV. 7-75

DWN	LEVENTHAL		CONTROL DATA	TITLE CABLE ASSY ASYNCHRONOUS RS232 TO 103F MODEM	PREFIX	DOCUMENT NO. 74658300	REV A
CHKD							
ENG	D. Post	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON 31773-009-070		SHEET 1 OF 4	
APPR			CODE IDENT 34015				

SHEET REVISION STATUS

4	3	2	1
–	00	00	00
–	00	00	01
–	00	02	02
–	00	03	03
–	00	04	04
05	00	05	05
A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	–	PRELIM RELEASE	ML	10-30-74	
01	–	REV. REVISION STATUS	DAM	12-17-74	
02	–	REV QTY FD NO. 4 & 5	LA	1-8-75	
03	05360	CL B PRERELEASED	DAM	1-10-75	
04	06707	CL II COMM. CONTACT CAGE	DAM	1-11-77	
05	08139	FIND NO. 5 WAS 620136001 ADDED: BLK WIRE (GND)	ELG	1-19-78	
A	08063	CLASS "A" RELEASE CBM	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA
AA6030

NOTES:

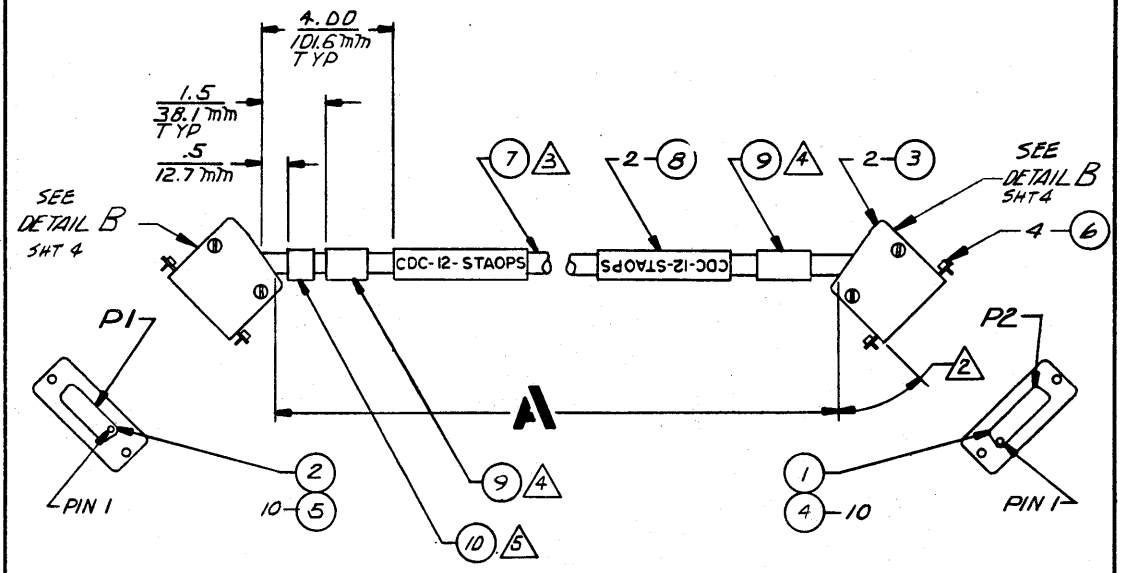
DN 74658300
PL 74658300
DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

31773-009-070

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	DOCUMENT NO. 74658300	REV. A



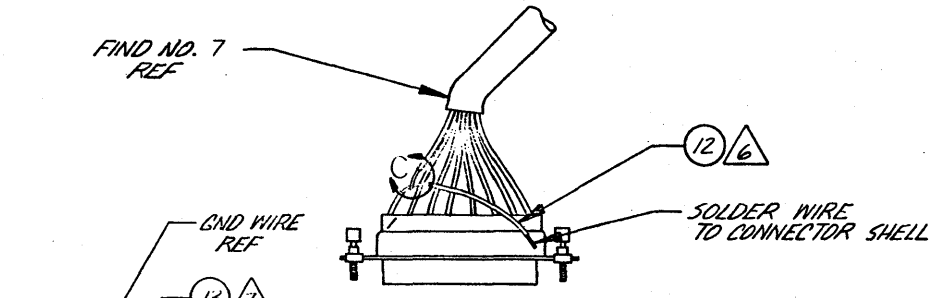
FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

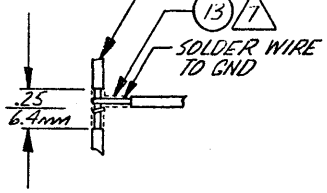
MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	DOCUMENT NO. 74658300	REV. A

CDC NO.	LENGTH A		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74658300	50.0	15.24	31773

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	DOCUMENT NO. 74658300	REV. A



DETAIL B
CONN. HOOD OMITTED FOR CLARITY
SCALE : NONE



DETAIL C
SCALE: NONE

DWN	LEVENTHAL	10/30/74	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY ASYNCHRONOUS RS232 TO 103F MODEM	DN	74658300	A
ENG	[signature]	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG			CODE IDENT 34015	FIRST USED ON 31773-009-070		SHEET 1 OF 2	
APPR							

SHEET REVISION STATUS

2	1
00	00
00	01
02	02
02	03
02	04
05	05
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	—	PRELIM RELEASE	ML	10-30-74	
01	—	REV. REVISION STATUS	DPM	12-17-74	
02	-	REV NOTE 3	LA	1-8-75	
03	05360	CL B AREARELEASE	DPM	1-10-75	
04	06707	CL II CONN. CONTACT CHAG	DPM	1-11-77	[illegible]
05	08139	FIND NO. 3 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	[illegible]
A	08063	CLASS "A" RELEASE CBM	TP	1-27-78	[illegible]

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31773-009-070

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO. 74658300	REV. A

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300.
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR SHELL & PIN 1.
4. FIND NUMBER (9) TO BE MARKED PER 10121508 WITH PART NUMBER 74658300, CONNECTOR NUMBER P1 OR P2, AND SERIAL NUMBER.
5. P1 END TO BE COLOR IDENTIFIED BLUE WITH FIND NUMBER (10).
6. STRIP BACK INSULATION AT BOTH ENDS OF WIRE .25 (6.4mm).
7. SLEEVE ALL BARE WIRE USING FIND NO. 13.

FORM 19246-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74658300	A	CLA	A	CBL AY ASYNCH RS232 TO 103F MO	DM	2551	01/29/78	01/29/78	1/ 1

MF

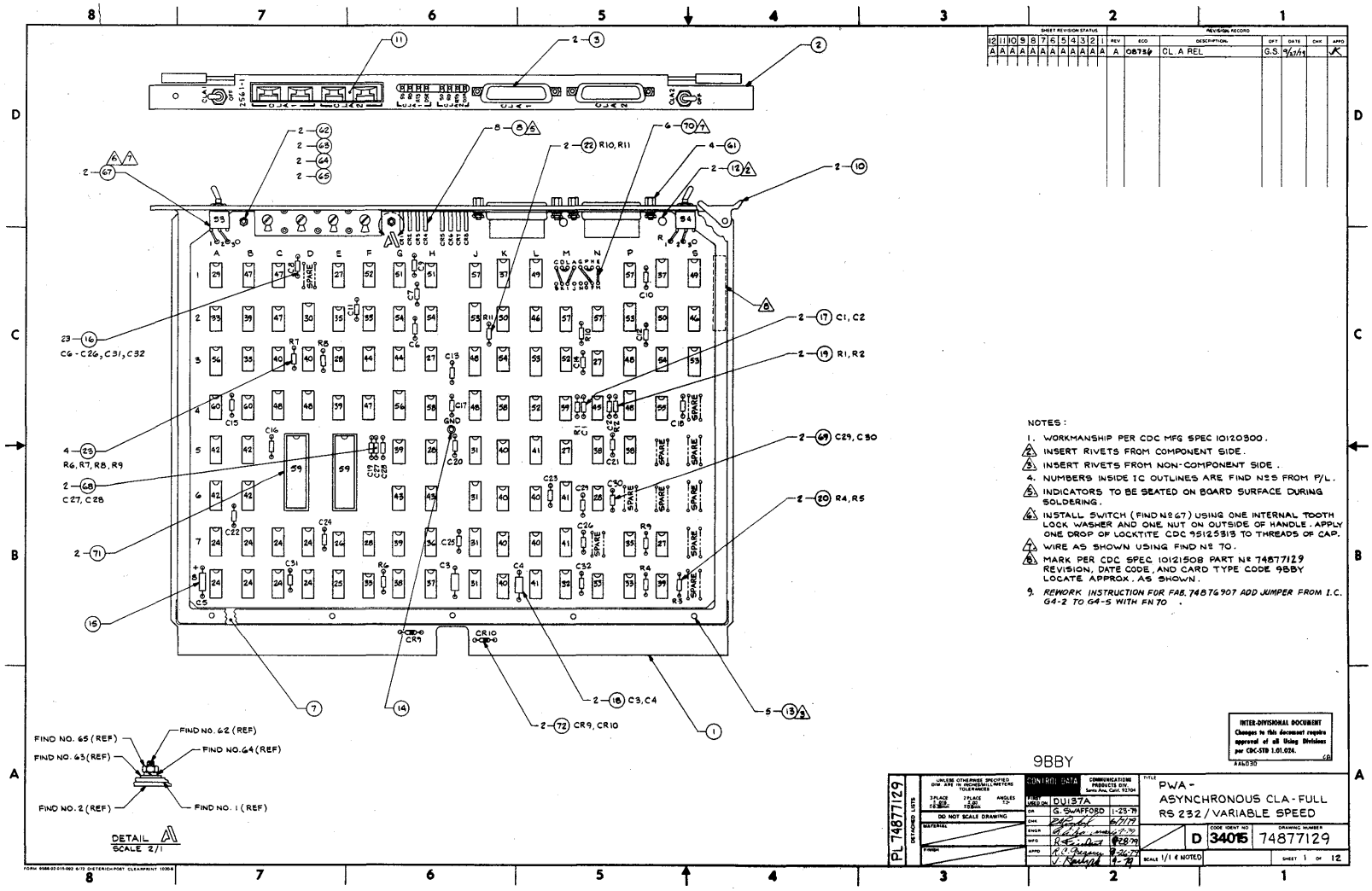
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP5		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN					N
8		51904701	200	PC	CABLE LABLE	IN					N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
5	A	62013606	1000	PC	SOCKET	IN					N
1	A	62013702	100	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
4	A	62013801	1000	PC	CONTACT PIN	IN			PPP4		N
9	B	73995500	200	PC	NMPLT KIT BLNK LARGE CABLES	IN			PPP4		N
11	A	74658400	REF	PC	WIRE LIST ASYNC RS232 TO 103F	IN					N
7	A	74871633	6000	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
10	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	008500		PPP4		N
6	A	74873611	400	PC	RETAINER MALE SCREW	IN			PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75



NOTES:
1. WORKMANSHIP PER CDC MFG SPEC 10120300.
2. INSERT RIVETS FROM COMPONENT SIDE.
3. INSERT RIVETS FROM NON-COMPONENT SIDE.
4. NUMBERS INSIDE IC OUTLINES ARE FIND NºS FROM P/L.
5. INDICATORS TO BE SEATED ON BOARD SURFACE DURING SOLDERING.
6. INSTALL SWITCH (FIND Nº 67) USING ONE INTERNAL TOOTH LOCK WASHER AND ONE NUT ON OUTSIDE OF HANDLE. APPLY ONE DROP OF LOCKTITE CDC 95125313 TO THREADS OF CAP.
7. WIRE AS SHOWN USING FIND Nº 70.
8. MARK PER CDC SPEC 10121508 PART Nº 74877129 REVISION, DATE CODE, AND CARD TYPE CODE 9BBY LOCATE APPROX. AS SHOWN.
9. REWORK INSTRUCTION FOR FAB. 74876907 ADD JUMPER FROM I.C. G4-2 TO G4-5 WITH FN 70.
INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
9BBY
PWA - ASYNCHRONOUS CLA-FULL RS 232/VARIABLE SPEED
D 34015 74877129
SCALE 1/1 & NOTED
SHEET 1 OF 12
PL 74877129
DETAIL A
SCALE 2/1
FIND NO. 65 (REF)
FIND NO. 63 (REF)
FIND NO. 2 (REF)
FIND NO. 62 (REF)
FIND NO. 64 (REF)
FIND NO. 1 (REF)
C6-C26, C31, C32
R6, R7, R8, R9
C27, C28
C1, C2
R1, R2
C29, C30
R4, R5
C3, C4
CR9, CR10
R10, R11

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74877129	A	CLA	D	PWA-ASYNC CLK RS232 VAR	DM	2551-2	09/26/79	09/26/79	1/ 2

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN RC	S OR N
62	A	3903003J5	200	PC	SCR MACH FLAT FIL H NO. 2	IN			PPP4		N
65	A	1J1251J2	200	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP3		N
63	A	1J1256J2	200	PC	PLAIN WASHERS	IN			PPP3		N
64	A	1J1258JJ	200	PC	SPRING LOCK WASHERS (MED.)	IN			PPP3		N
52	A	15111400	300	PC	INTEGRATED CIRCUIT 74L51	IN			PPP4		N
39	A	15112300	600	PC	INT CKT 74L32	IN			PPP4		N
27	E	15112700	500	PC	INT CKT 74L04	IN			PPP4		N
29	A	15116000	100	PC	INTEGRATED CIRCUIT 74L02	IN			PPP4		N
41	A	15117000	400	PC	IC-SYNC 4 BIT COUNTER 74163	IN			PPP4		N
59	A	15125700	200	PC	I.C. TR1602A UNIV. ASYNCHRON	IN			PPP4		N
45	A	15134200	100	PC	IC QUAD EXCL OR NOR 4030	IN			PPP4		N
24	A	15142800	800	PC	IC 74251	IN			PPP4		N
28	A	151429JJ	400	PC	MICROCIRCUIT TYPE 74L10 TTL 3	IN			PPP4		N
55	A	151430JJ	100	PC	MICROCIRCUIT TYPE 74L20 TTL DU	IN			PPP4		N
53	A	151431JJ	200	PC	MICROCIRCUIT TYPE 74L30 TTL 8	IN			PPP4		N
43	A	151432JJ	200	PC	IC 74L54 TTL 4-WD AND/OR INVRT	IN			PPP4		N
31	A	151436JJ	400	PC	MICROCIRCUIT TYPE 93L12	IN			PPP4		N
56	A	151437JJ	200	PC	MICROCIRCUIT TYPE 9L24 DL JK F	IN			PPP4		N
48	A	151440CC	600	PC	MICROCIRCUIT TYPE 74L99 4 BIT	IN			PPP4		N
58		151560CC	200	PC	IC 74L55 J	IN			PPP4		N
47		151561CC	400	PC	IC 74L74 J	IN			PPP4		N
30	A	15158200	100	PC	I C 9300 74195	IN			PPP4		N
51	A	151613JC	200	PC	I.C. TYPE 7405 TTL-HEX INVERT.	IN			PPP4		N
32	C	15163327	100	PC	IC 9321 TTL DUAL DECODER	IN			PPP4		N
42	A	17184000	400	PC	IC 74L05 4BIT MAGNITDE COMPRTR	IN			PPP4		N
16	C	19115400	2300	PC	CAPACITOR,FIXED,CERAMIC,50 VDC	IN			PPP4		N
18	C	19115431	200	PC	CAP. FIXED CERAMIC 50VDC .1MFD	IN			PPP4		N
20	C	245JJJ55	200	PC	RES FXD .25W 470 OHMS	IN			PPP4		N
23	C	245JJJ63	400	PC	RES FXD .25W 1KJJ OHMS	IN			PPP4		N
19	C	245JJJ8J	200	PC	RES FXD .25W 91JJ OHMS	IN			PPP4		N
22	C	245JJJ82	200	PC	RES FXD .25W 82JJ OHMS	IN			PPP4		N
72	C	24519100	200	PC	RECTIFIER SILICON 75J MA	IN			PPP4		N
54	A	36186400	400	PC	IC CHIP,TYPE 1488	IN			PPP4		N
57	A	36186501	400	PC	IC CHIP TYPE 1489	IN			PPP4		N
14	A	38807901	100	PC	TERMINAL HOLLOW SINGLE END.185	IN			PPP3		N
33	B	39369700	300	PC	INT CKT 7404	IN			PPP4		N

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74877129	A	CLA	D	PWA-ASYNC CLK RS232 VAR	DM	2551-2	09/26/79	09/26/79	2/ 2

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN RC	S OR N
71	A	5165B103	200	PC	SOCKET,EC,PC TYPE 40 PIN	IN			PPP4		N
3	A	51873411	200	PC	CONN,PC RIGHT ANGLE 25 PIN	IN			PPP4		N
40	A	52335500	800	PC	ACCEPT.TEST SHIFT REG.4BIT7495	IN			PPP4		N
70	C	52629925	500	IN	WIRE 26AWG KYNAR GREEN	IN			PPP3		N
44	A	65299J99	200	PC	MICROCIRCUIT TYPE 7400 (SPEC)	IN			PPP4		N
15	A	72JJ3616	100	PC	CAPACITOR 10 VF 15V TANT	IN			PPP4		N
2	C	74618702	100	PC	HANDLE SEKSCRND ASYNCH CLK	IN			ATV4		N
7	C	74632700	100	PC	INSULTR CRD STIFFENER	IN			PPP4		N
53	A	74870525	400	PC	CAP ARRAY 220 PF	IN			PPP4		N
8	A	74870560	800	PC	INDICATOR LED	IN			PPP4		N
10		74870632	200	PC	EJECTOR CKT CARD WHT NYLON	IN			PPP4		N
67	A	74872299	200	PC	SWTCH LOCKNG TOGGLE 1 THRU 4 P	IN			PPP4		N
1	D	74876907	100	PC	PWB ASYNC CLK RS232 VARIABLE	IN			PPP4		N
11	A	74878101	100	PC	SWITCH THUMBWHEEL HEX COMPLI	IN			PPP4		N
60	A	75009943	200	PC	RES PKG 10 OK OHMS	IN			PPP4		N
17	A	77612383	200	PC	CAPACITOR 100PF 50V 5PCT	IN					N
68	A	77612387	200	PC	CAPACITOR CERAMIC AXIAL	IN			PPP4		N
69	A	77612393	200	PC	CAPACITOR 68PF 50V 5PCT	IN					N
25	A	88817JJ	100	PC	IC 8214 TTL DUAL 4/1 MUX	IN			PPP4		N
36	A	88828JJ	100	PC	IC 74174 TTL HEX D F/F M/CLEAR	IN			PPP4		N
49	A	88829JJ	200	PC	IC 74175 TTL QUAD D F/F M/CLR	IN			PPP4		N
38	A	88854JJ	300	PC	IC 9324 TTL DUAL FLIP/FLOP	IN			PPP4		N
46	A	88857JJ	200	PC	IC 7486 TTL QUAD 2-IN EXCL OR	IN			PPP4		N
37	A	88886CC	300	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN			PPP4		N
35	A	88897CC	300	PC	IC 7408 TTL QUAD 2-INPUT AND	IN			PPP4		N
12	A	92030017	200	PC	EYELET	IN					N
13	A	92030019	300	PC	EYELET	IN					N
61	C	94288024	400	PC	CONNECTOR LOCKING DEVICE	IN			PPP4		N
26	A	96744154	100	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN			PPP4		N

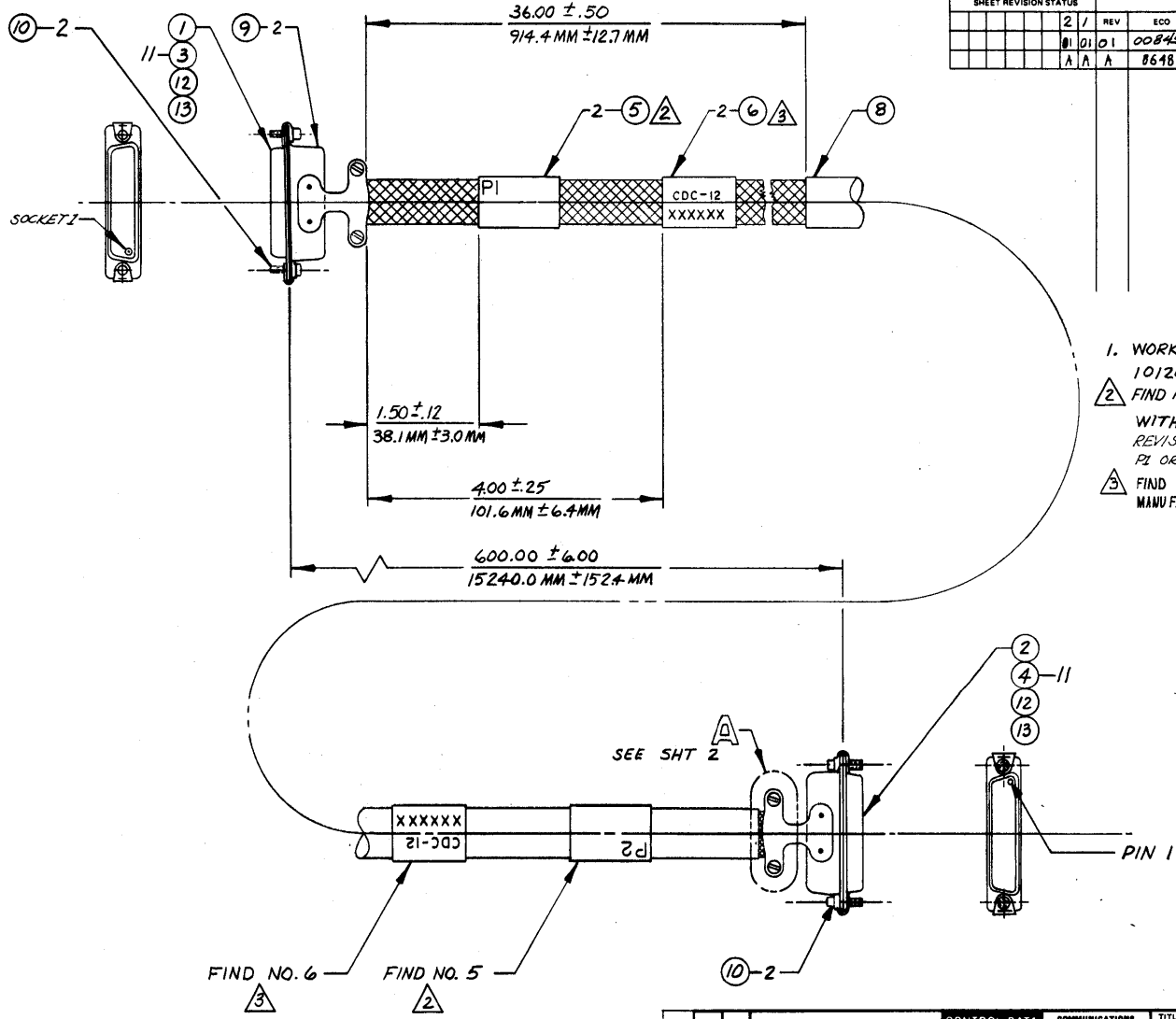
NUMBER OF LINE ITEMS = 65
HIGHEST FIND NUMBER = 72

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.



SHEET REVISION STATUS		REVISION RECORD						
2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01	01	01	008457	CLASS B RELEASE	AV	6-78	VK	VK
A	A	A	8648	REMOVED CL"C" PARTS	TD	5 APR 79	VK	VK

1. WORKMANSHIP PER CDC MFG. SPEC. 10120300.
2. FIND NO. 5 TO BE MARKED PER CDC-SPEC 10121508 WITH PART NO. 74875756 REVISION. DATE CODE (E.G. 12/78) AND P1 OR P2 AS APPLICABLE.
3. FIND NO. 6 TAB NUMBERS INDICATE RESPONSIBLE MANUFACTURING DIVISION (REF. CDC SPEC 10123800)

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
AA6030

WL 74875756 | PL 74875756 | DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES
3 PLACE ±.015 ±0.38mm | 2 PLACE ±.03 ±0.8mm | ANGLES ±2°
DO NOT SCALE DRAWING
MATERIAL
FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

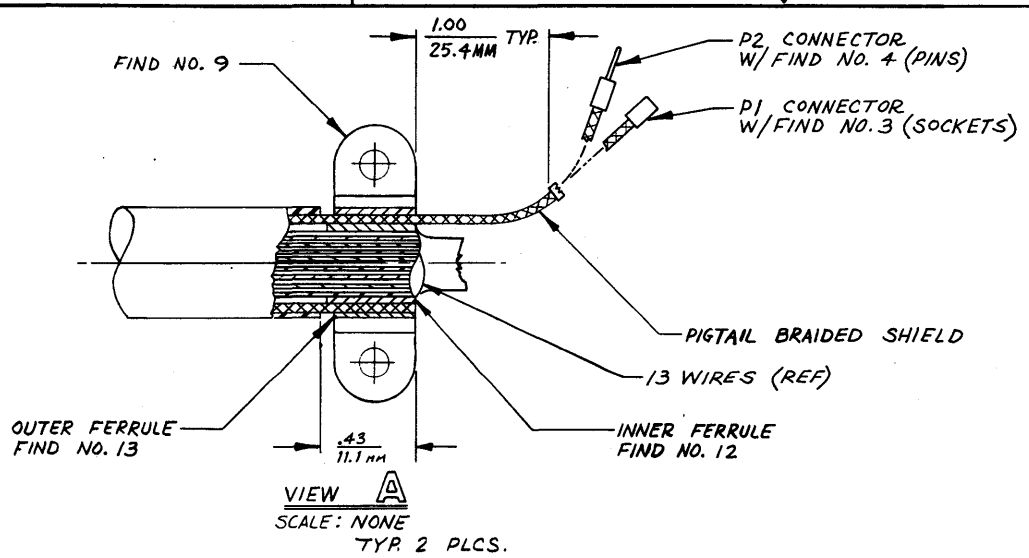
FIRST USED ON	YA 228-A	
DR	ECKHOLDT	3/16/78
CHK	[illegible]	3/16/78
ENGR	[illegible]	[illegible]
MFG	R. Fradrich	10-4-78
APPD	J. Kanyon	10-78

TITLE: CABLE ASSY - ASYNCHRONOUS RS-232 TO 103A/113

C | CODE IDENT NO. 34015 | DRAWING NUMBER 74875756

SCALE FULL & NOTED | 36947-009-070 | SHEET 1 OF 2

FORM 9587-02-015-092 6/72 DIETERICH-POST CLEARPRINT 1020-8



VIEW A
SCALE: NONE
TYP. 2 PLCS.

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	——	SEE SHEET 1	——	——		

CONTROL DATA
COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

TITLE: CABLE ASSY- ASYNCHRONOUS RS 232 TO 103A/113

CODE IDENT NO. 34015 | C | DRAWING NUMBER 74875756 | A

36947-009-070 | SHEET 2 OF 2

FORM 23580-00-015-092 6/72 DIETERICH-POST CLEARPRINT 1020-8

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74A75756	A	CLA	A	CABLE ASSY ASYNC RS232-103A	DM	2551	08/30/78	04/10/79	1/ 1

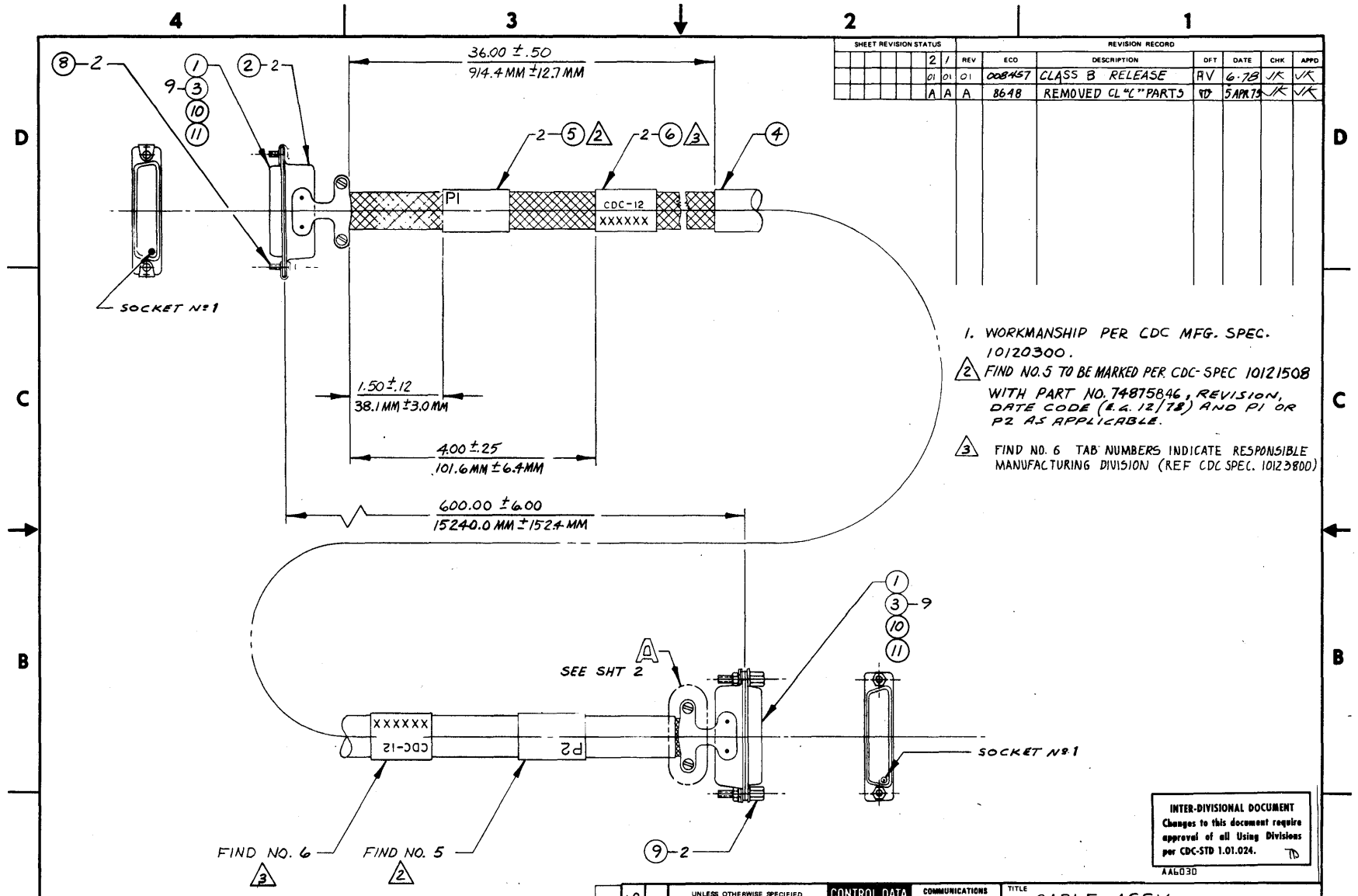
FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
6	A	10123801	200	PC	LABEL, CABLE MARKING	IN	008648	040979			N
6	A	10123835	200	PC	LABEL CABLE MAR CDC 12 STAMPS	IN	008648	040979			N
8	A	15165361	60000	IN	CABLE SHIELDED 13COND 24AWG	IN	008648	040979			N
9	C	36183207	200	PC	CLAMP CABLE 2.109 GOLD IRIDITE	IN			PPP4		N
5		51904701	200	PC	CABLE LABLE	IN			PPP4		N
1	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
3	A	62013606	1100	PC	SOCKET	IN			PPP4		N
2	A	62013702	100	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN			PPP4		N
10	A	74A73611	400	PC	RETAINER MALE SCREW	IN			PPP4		N
12	A	74A74794	200	PC	FERRULE INNER	IN			PPP4		N
13	A	74A74795	200	PC	FERRULE OUTER	IN			PPP4		N

NUMBER OF LINE ITEMS = 12
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER
SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.



SHEET REVISION STATUS			REVISION RECORD						
2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01	01	01	008457	CLASS B RELEASE	RV	6·78	VK	VK
A	A	A	8648	REMOVED CL "C" PARTS	RD	5APR79	VK	VK

1. WORKMANSHIP PER CDC MFG. SPEC. 10120300.
2. FIND NO. 5 TO BE MARKED PER CDC-SPEC 10121508 WITH PART NO. 74875846, REVISION, DATE CODE (E.G. 12/78) AND P1 OR P2 AS APPLICABLE.
3. FIND NO. 6 TAB NUMBERS INDICATE RESPONSIBLE MANUFACTURING DIVISION (REF CDC SPEC. 10123800)

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

PL 74875846 DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS
TOLERANCES
3 PLACE ±.015 ±0.38mm | 2 PLACE ±.03 ±0.8mm | ANGLES ±2°
DO NOT SCALE DRAWING
MATERIAL
FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

FIRST USED ON	YA 230-A	
DR	ECKHOLDT	3/16/78
CHK	[illegible]	3/16/78
ENGR	[illegible]	[illegible]
MFG	R. Friedrich	10/4/78
APPD	[illegible]	10·78

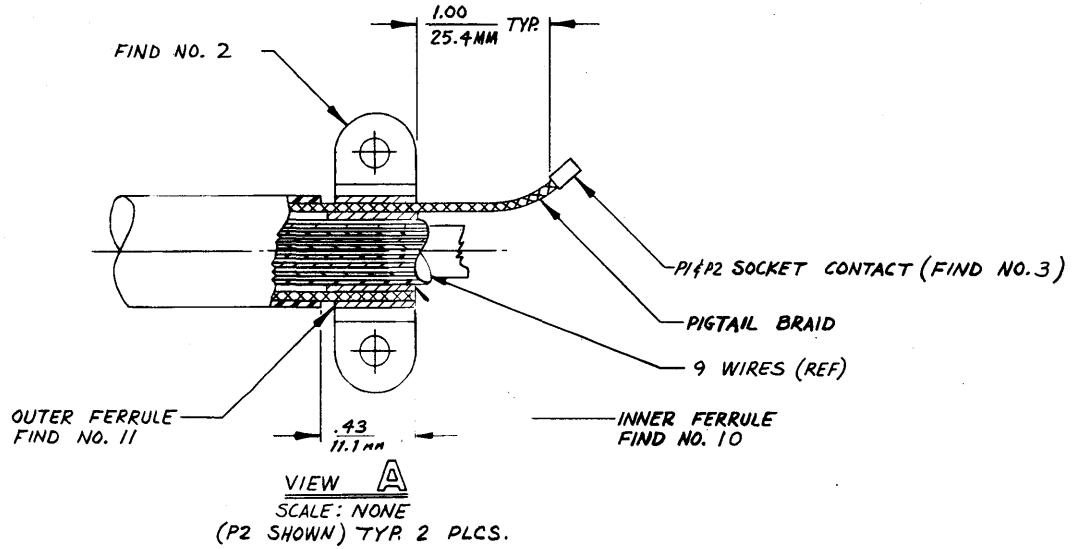
TITLE: CABLE ASSY - ASYNCHRONOUS RS-232 TO TERMINAL

CODE IDENT NO. C 34015 | DRAWING NUMBER 74875846

SCALE FULL & NOTED | 36949-009-070 | SHEET 1 OF 2

FORM 9587-02-015-092 6/77 DIETERICH-POST CLEARPRINT 1020-8

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	———	SEE SHEET 1	—	———		



VIEW A
SCALE: NONE
(P2 SHOWN) TYP. 2 PLCS.

CONTROL DATA	TITLE	CODE IDENT NO.		DRAWING NUMBER	
COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CABLE ASSY- ASYNCHRONOUS RS 232 TO TERMINAL	34015	C	74875846	A
		36949-009-070		SHEET 2 OF 2	

FORM 23080-00-015-002 6/72 DIETERICH-POST CLEARPRINT 1000-6

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74875846	A	CLA	A	CABLE ASSY ASYNC RS232 TO TERM	DM	2551	08/30/78	04/10/79	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
6	A	10123801	200	PC	LABEL, CABLE MARKING	IN	008648	040979			N
6	A	10123835	200	PC	LABEL CABLE MAR CDC 12 STAMPS	IN	008648	040979			N
4	A	15165360	60000	IN	CABLE SHIELDED 9 COND 24AWG	IN	008648	040979			N
13	C	24548310	200	IN	WIRE ELEC STRD INS. UL APPD	IN			PPP4		N
2	C	36183207	200	PC	CLAMP CABLE 2.109 GOLD IRIDITE	IN			PPP4		N
5		51904701	200	PC	CABLE LABLE	IN			PPP4		N
1	C	62013502	200	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
3	A	62013606	1800	PC	SOCKET	IN			PPP4		N
8	A	74873611	200	PC	RETAINER MALE SCREW	IN			PPP4		N
10	A	74874794	200	PC	FERRULE INNER	IN			PPP4		N
11	A	74874795	200	PC	FERRULE OUTER	IN			PPP4		N
9	C	94288024	200	PC	CONNECTOR LOCKING DEVICE	IN	008648	040979	PPP4		N

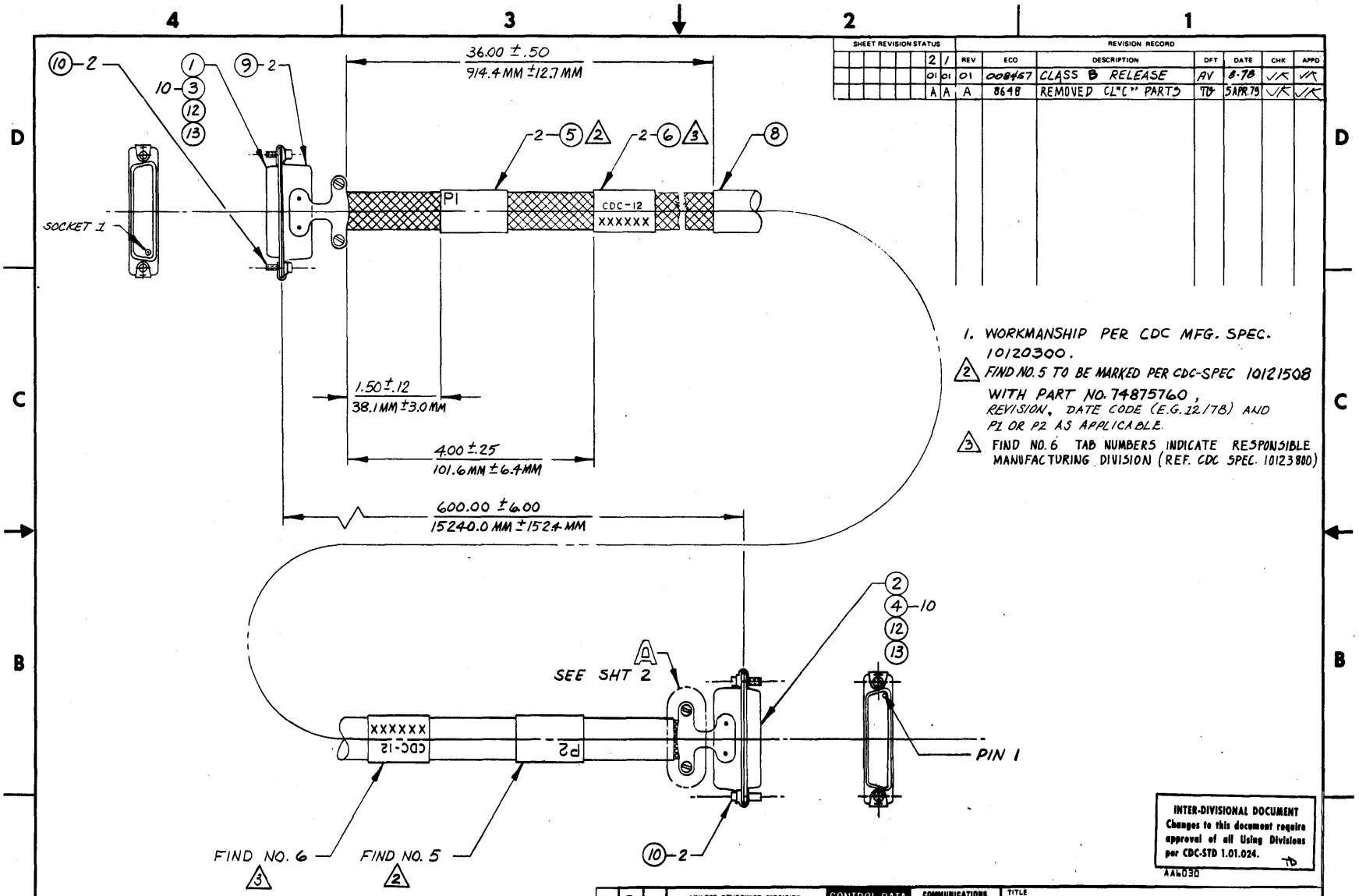
NUMBER OF LINE ITEMS = 12
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.



SHEET REVISION STATUS								REVISION RECORD							
						2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
						01	01	01	008457	CLASS B RELEASE	AV	8-78	VK	VK
						A	A	A	8648	REMOVED CL"C" PARTS	TD	5APR.79	VK	VK

1. WORKMANSHIP PER CDC MFG. SPEC. 10120300.
2. FIND NO. 5 TO BE MARKED PER CDC-SPEC 10121508 WITH PART NO. 74875760, REVISION, DATE CODE (E.G. 12/78) AND P1 OR P2 AS APPLICABLE.
3. FIND NO. 6 TAB NUMBERS INDICATE RESPONSIBLE MANUFACTURING DIVISION (REF. CDC SPEC. 10123800)

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

PL 74875760

PL 74875760 DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS
TOLERANCES: 3 PLACE ±.015 ±0.38mm; 2 PLACE ±.03 ±0.8mm; ANGLES ±2°

DO NOT SCALE DRAWING

MATERIAL

FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

FIRST USED ON	YA 229-A	
DR	ECKHOLDT	3/15/78
CHK	[illegible]	5/15/78
ENGR	[illegible]	
MFG	R. Faulkner	10-4-78
APPD	[illegible]	10-7-78

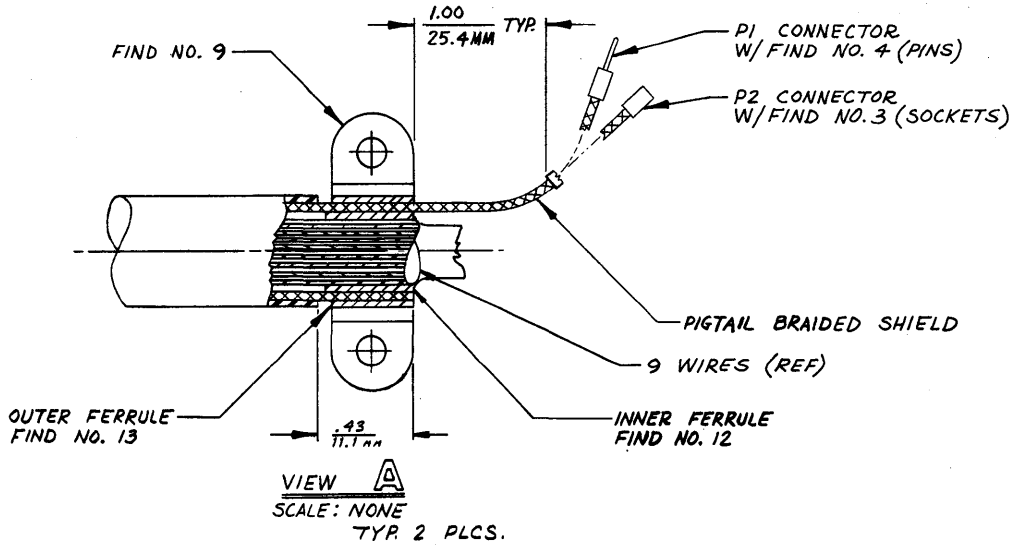
TITLE: CABLE ASSY - ASYNCHRONOUS RS-232 TO 103F MODEM

CODE IDENT NO. C 34015 — DRAWING NUMBER 74875760

SCALE FULL & NOTED — 38007-009-070 — SHEET 1 OF 2

FORM 9587-02-015-092 6/77 DIETERICH-POST CLEARPRINT 1020-8

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	—	SEE SHEET 1	—	—		



VIEW A
SCALE: NONE
TYP. 2 PLCS.

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE: CABLE ASSY- ASYNCHRONOUS RS 232 TO 103F MODEM	CODE IDENT NO. 34015	C	DRAWING NUMBER 74875760 A
		38007-009-070		SHEET 2 OF 2

FORM 23860-00-019-092 8/72 DIETERICH-POST CLEARPRINT 1020-B

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74A75760	A	CLA	A	CABLE ASSY ASYNC RS232-103F	DM	2551	08/30/78	04/10/79	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
6	A	10123801	2.00	PC	LABEL, CABLE MARKING	IN	008648	040979			N
6	A	10123835	2.00	PC	LABEL CABLE MAR CDC 12 STAMPS	IN	008648	040979			N
8	A	15165360	60.00	IN	CABLE SHIELDED 9 COND 24AWG	IN	008648	040979			N
9	C	36183207	2.00	PC	CLAMP CABLE 2.109 GOLD IRIDITE	IN			PPP4		N
5		51904701	2.00	PC	CABLE LABLE	IN			PPP4		N
1	C	62013502	1.00	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
3	A	62013606	10.00	PC	SOCKET	IN	008457	091878	PPP4		N
2	A	62013702	1.00	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
4	A	62013801	10.00	PC	CONTACT PIN	IN	008457	091878	PPP4		N
10	A	74A73611	4.00	PC	RETAINER MALE SCREW	IN			PPP4		N
12	A	74A74794	2.00	PC	FERRULE INNER	IN			PPP4		N
13	A	74A74795	2.00	PC	FERRULE OUTER	IN			PPP4		N

NUMBER OF LINE ITEMS = 12
HIGHEST FIND NUMBER = 13

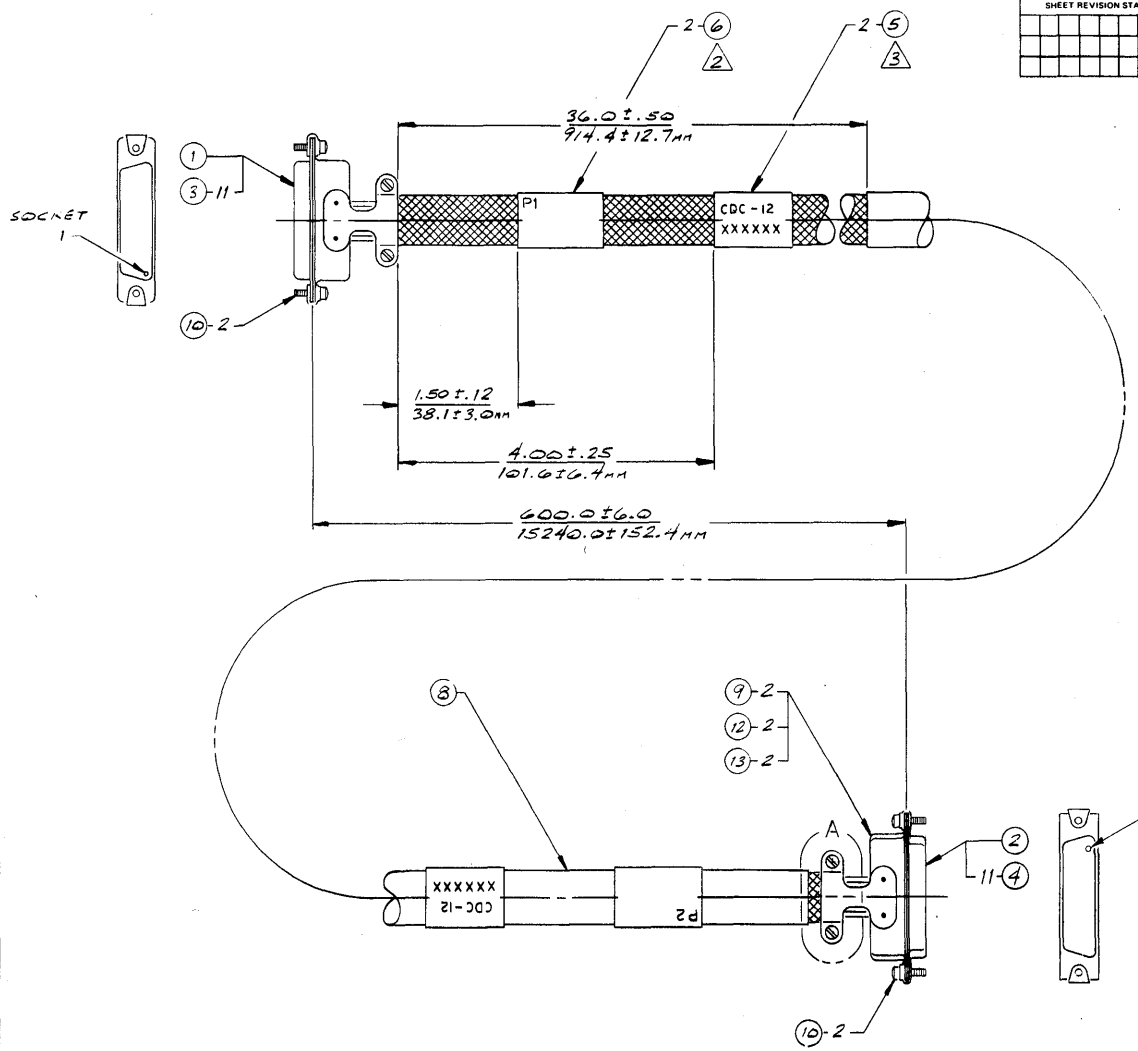
PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

SHEET REVISION STATUS									REVISION RECORD							
							2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
							01	01	01	08507	CLB RELEASE	AV	8-78	JK	JK
							A	A	A	8648	CHANGED PIN 1 REF.	TD	4-79	JK	JK



NOTES:

1. WORKMANSHIP PER CDC SPEC 10120300

2. FIND Nº 6 TO BE MARKED PER CDC SPEC 10121508 WITH PART Nº (74876194), REVISION, DATE CODE (E.G. 12/78) AND P1 OR P2 AS APPLICABLE

3. FIND Nº 5 TAB NUMBERS INDICATE RESPONSIBLE MANUFACTURING DIVISION (REF. CDC SPEC 10123800)

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. TD

AA6030

WL 74876194
PL 74876194

DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES
3 PLACE ±.015 ±0.38mm | 2 PLACE ±.03 ±0.8mm | ANGLES ±2°

DO NOT SCALE DRAWING

MATERIAL

FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

FIRST USED ON	XA229-B	
DR	A. VOLPE	8-7-78
CHK	RA CRAWFORD	10/78
ENGR	RA Crawford	10/78
MFG	R. FRIEDRICH	10-78
APPD	J. Fan-[illegible]	11-78

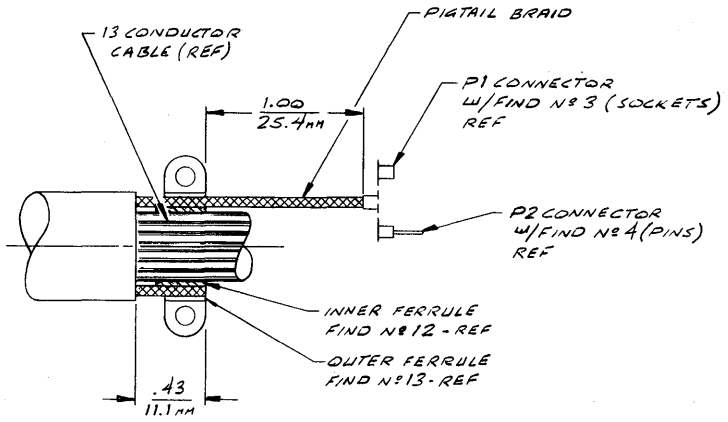
TITLE: CABLE ASSEMBLY ASYNCHRONOUS CLA TO 202 S MODEM (REV CHAN)

C | CODE IDENT NO. 34015 | DRAWING NUMBER 74876194

SCALE FULL | SHEET 1 OF 2

FORM 9587 02 015 092 6/72 DIETERICH-POST CLEARPRINT 1020-B

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	———	SEE SHEET 1	AV	8.78		



DETAIL A
TWICE SIZE

CONTROL DATA COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE: CABLE ASSEMBLY ASYNCHRONOUS CLA TO 202S MODEM	CODE IDENT NO. 34015	C	DRAWING NUMBER 74876194	A
				SHEET 2 of 2	

FORM 73560 00 015 092 6/72 DIETERICH POST CLEARPRINT 1020 B

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74876194	A	CLA	C	CBL ASSY ASYNC CLA-202S MOD MC	DM	2551	10/30/78	04/11/79	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PRI MC	S ON B
5	A	10123800	200	PC	LABEL, CABLE MARKING	IN			PPP4		N
8	A	15165361	60000	IN	CABLE SHIELDED 13COND 24A#G	IN	008648	041079			N
9	C	36183207	200	PC	CLAMP CABLE 2.109 GOLD IRIDITE	IN			PPP4		N
6		51904701	200	PC	CABLE LABLE	IN			PPP4		N
1	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
3	A	62013606	1100	PC	SOCKET	IN			PPP4		N
2	A	62013702	100	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN			PPP4		N
10	A	74873611	400	PC	RETAINER MALE SCREW	IN			PPP4		N
12	A	74874794	200	PC	FERRULE INNER	IN			PPP4		N
13	A	74874795	200	PC	FERRULE OUTER	IN			PPP4		N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

DWN	L. ANDERSON	4/27/77	CONTROL DATA	TITLE CABLE ASSY, ASYNC CLA TO 202S MODEM	PREFIX SE	DOCUMENT NO. 74874002	REV B
CHKD	[signature]	4-27-77	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
ENG	[signature]	4-77					
MFG			CODE IDENT 34015	FIRST USED ON QSE 19990-A	35689-009-070		SHEET 1 OF 4
APPR							

SHEET REVISION STATUS

4	3	2	1
A	A	A	A
A	A	A	B

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	6838	INITIAL RELEASE	LA	4-27-77	[illegible]
B	08063	CLASS A RELEASE	TP	1-20-78	[illegible]

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA

AA6030

NOTES:

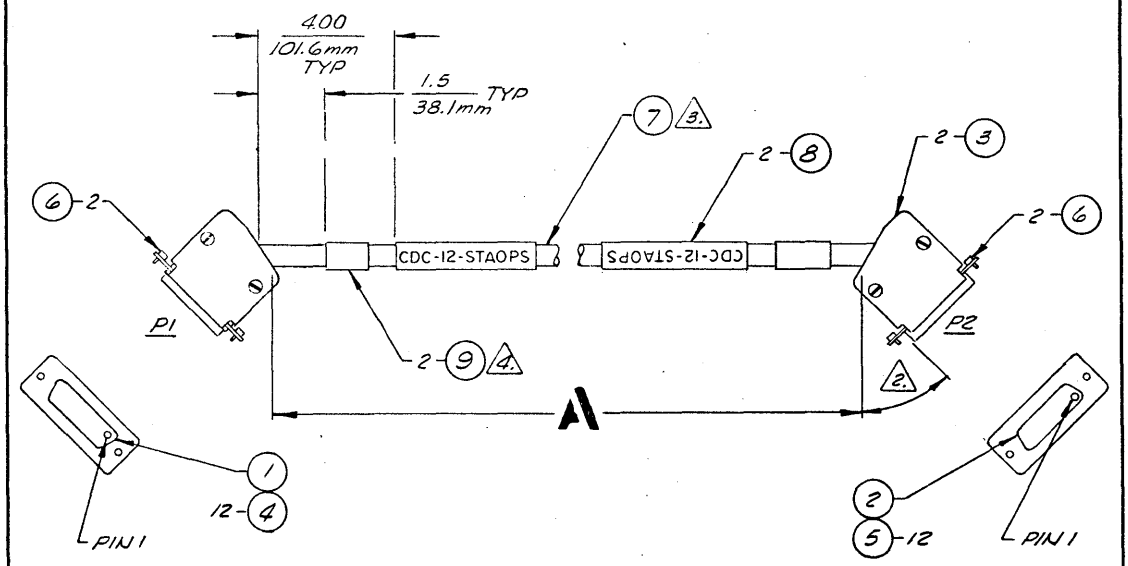
PL 74874002

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

35689-009-070

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	SE	DOCUMENT NO. 74874002	REV. A



FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

35689-009-070

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	SE	DOCUMENT NO. 74874002	REV. A

CDC Nº.	A LENGTH		RTN Nº.
	FEET ±0.5 FT	METERS ±.15 METERS	
74874002	50.0	15.24	35689

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COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	SE	DOCUMENT NO. 74874002	REV. A

NOTES:

1. WORKMANSHIP PER CDC SPEC 10120300
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR PIN 1.
4. MARK FIND NO. 9 PER CDC SPEC 10121508 WITH PART NO. 74874002, CONNECTOR NO. P1 OR P2, AND SERIAL NUMBER.

FORM 19245-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74874002	B	CLA	A	ASYNC CLA TO 2025 MODEM	DM	2551	01/29/78	01/29/78	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
3	A	51892202	2.00	PC	HOOD CONNECTOR	IN					N
8		51904701	2.00	PC	CABLE LABLE	IN					N
1	C	62013502	1.00	PC	CONN*SOCKET*HOUSING 25 PIN	IN			PPP4		N
4	A	62013601	12.00	PC	CONTACT SOCKET	IN			PPP4		N
2	A	62013702	1.00	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
5	A	62013801	12.00	PC	CONTACT PIN	IN			PPP4		N
9	B	73995500	2.00	PC	NMPLT KIT BLNK LARGE CABLES	IN			PPP4		N
7	A	74871633	60.00	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
6	A	74873611	4.00	PC	RETAINER MALE SCREW	IN			PPP4		N
20	A	74874003	REF	PC	WIRE LIST ASYNC TO 2025 MODEM	IN					N

NUMBER OF LINE ITEMS = 10
HIGHEST FIND NUMBER = 20

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

DWN	CRAWFORD	2-21-75	CONTROL DATA	TITLE CONNECTOR ASSY – ASYNC CLA LOOP EXTERNAL TEST CONNECTOR	PREFIX /	DOCUMENT NO. 74715600	REV 00
CHKD							
ENG	RAE	2-21-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG							
APPR			CODE IDENT 34015	FIRST USED ON 32161-009-122	/	SHEET 1 OF 2	

SHEET REVISION STATUS

2	1
00	00

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05515	CL B RELEASE		2-24-75	JJR

NOTES: 1. WORKMANSHIP PER CDC-SPEC 10120300.

1 LABEL, FIND NO. 5, IS LOCATED ON BACKSIDE OF FIND NO. 3
LABEL SHOULD HAVE THE FOLLOWING TYPEWRITTEN:
ACLA 2561-1, External, Test Conn.

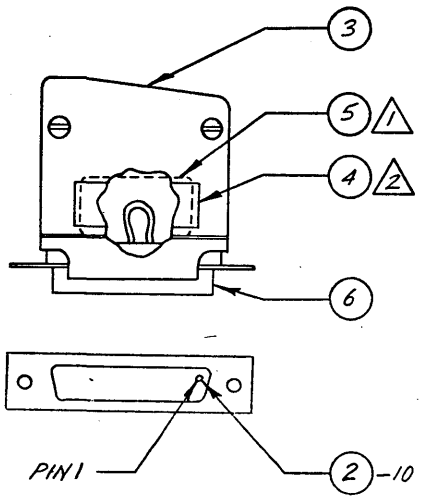
2 FIND NO. 4 TO BE MARKED PER 10121508.

WL 74715700	PL 74715600
ASSOCIATED LIST	DETACHED LISTS

FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

32161-009-122

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DOCUMENT NO. 74715600	REV. 00



FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	CRAWFORD	2-21-75	CONTROL DATA	TITLE CONNECTOR ASSY— ASYNC CLA LOOP EXTERNAL TEST CONNECTOR	PREFIX	DOCUMENT NO.	REV
CHKD					PL	74715600	00
ENG	LHC	2-21-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	FIRST USED ON			
MFG				32161-009-122		SHEET 1 OF 2	
APPR			CODE IDENT 34015				

SHEET REVISION STATUS

2	1
00	00

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05515	CL B RELEASE		2-24-75	LHC

NOTES:

DETACHED LISTS

FORM 19246 01-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

32161-009-122

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	PL	DOCUMENT NO 74715600	REV. 00

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1		1	FT		WIRE, 22GA	01435-002
2	7397700	1	PC		CONTACT, SOCKET	14198-002
3	73919803	1	EC		HOOD, CONNECTOR	26046-002
4	73954300	1	PC		LABEL	15486-002
5		1	PC		LABEL, SELF-ADHESIVE	01223-002
6	74394500	1	PC		CONNECTOR BLOCK-SOCKET	14196-002

FORM 19247-01-015-092 DIETERICH-POST CLEARPRINT 1020

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Wire lists for the cable assemblies used with the asynchronous communications line adapter are provided in this section.

Actual pin connections from ACLA to modem or terminal are listed in section 3 and connections to the loop multiplexer are listed in section 6.

DWN	LEVENTHAL	10/31/74	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY - ASYNCHRONOUS RS232 TO 103A/113	WL	74657800	A
ENG	[signature]	11-5-74	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON		SHEET 1 OF 2	
APPR			CODE IDENT 34015	31770-028-070			

SHEET REVISION STATUS

2	1
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01	01
01	02
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	PRELIM RELEASE	ML	10-31-74	
01	-	DELETED COND 9 & 10; RENUMBERED COND.; REV CABLE FO NOS	LA	1-3-75	
02	05360	CL B PRERELEASED	DDM	1-10-75	
A	08063	CLASS "A" RELEASE	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA
AAL030

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31770-028-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74657800	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	7	22	SHIELD WIRE		CONN P1	1	5	CONN P2	1	4	PROTECTIVE GND (AA)
2	↑	↑	BLK		↑	2	↑	↑	2	↑	TRANSMITTED DATA (BA)
3			BRN			3			3		RECEIVED DATA (BB)
4			RED			4			4		REQUEST TO SEND (CA)
5			ORN			5			5		CLEAR TO SEND (CB)
6			YEL			6			6		DATA SET READY (CC)
7			GRN			7			7		SIGNAL GND (AB)
8			BLU			8			8		RCVD LINE SIG DET (CF)
9			VIO			20			20		DATA TERM READY (CD)
10	↓	↓	GRY		↓	22	↓	↓	22	↓	RING INDICATOR (CE)
11	7	22	WHT		CONN P1	25	5	CONN P2	25	4	TERM BUSY (-)

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	LEVENTHAL	10/31/74	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY ASYNCHRONOUS RS232 TO TERMINAL	WL	74658000	F
ENG	D. K. M.	11-5-74	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG			CODE IDENT 34015	FIRST USED ON XA135-A	31771-028-070	SHEET 1 OF 2	
APPR							

SHEET REVISION STATUS

2	1
00	00
01	01
01	02
0	0
E	E
E	F

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	—	PRELIM RELEASE	ML	10-31-74	
01	-	DELETE COND 10,11,12&13; COND 10 WAS 14. REV CABLE & CONTACT PD NOS. REV COLORS	LA	1-2-75	
02	05360	CL "B" PRERELEASED	PPM	4-10-75	
0	06248	SEE ECO	LA	3-5-76	
E	06707	CL II CONN. CONTACT CHG	PPM	1-11-77	
F	08063	CLASS A RELEASE CBM	TP	1-20-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

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NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31771-028-070

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74658000	REV E

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	4	22	SHIELD WIRE		CONN P1	1	3	CONN P2	1	3	PROTECTIVE GND (AA)
2	4		BLK			2	3	P2	3	3	TRANS/RCVD DATA
3	4		BRN			3	3	P2	2	3	RCVD/TRANS DATA
4	10		WHT			4	3	P1	5	3	REQ/CLEAR TO SEND
5	4		RED			5	-	P2	8	3	RCVD LINE SIG DET
6	4		ORN			6	3		20	3	DATA SET/TERM READY
7	4		YEL			7	3		7	3	SIGNAL GND (AB)
8	4		GRN		P1	8	3		4	3	RCVD LINE SIG DET
9	10		WHT		P2	4	-		5	3	REQ/CLEAR TO SEND
10	4	22	BLU		CONN P1	20	3	CONN P2	6	3	DATA TERM/SET READY

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	LEVENTHAL		CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY ASYNCHRONOUS RS232 TO 103F MODEM	WL	74658400	A
ENG	[illegible]	1-5-78	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG			CODE IDENT 34015	FIRST USED ON 31773-028-070		SHEET 1 OF 2	
APPR							

SHEET REVISION STATUS

2	1
00	00
01	01
02	02
02	03
D	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	PRELIM RELEASE	ML		
01	-	REV. IDENT NO. 9 & 10 REMARK	DPM	12-12-74	
02	-	REV COLORS & CABLE PD NO; DELETE COND 10 & 12	LA	1-8-75	
03	05360	CL B PRERELEASE	DPM	1-10-75	
A	08063	CLASS A RELEASE LBM	TP	1-20-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
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NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31773-028-070

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74658400	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	7	22	SHIELD W/WIRE		CONN P1	1	5	CONN P2	1	4	PROTECTIVE GND (AA)
2	"	"	BLK		"	2	"	"	2	"	TRANSMITTED DATA (BA)
3			BRN			3			3		RCVD DATA (BB)
4			RED			4			4		REQUEST TO SEND (CA)
5			ORN			5			5		CLEAR TO SEND (CB)
6			YEL			6			6		DATA SET READY (CC)
7			GRN			7			7		SIGNAL GND (AB)
8			BLU			8			8		RCVD LINE SIGNAL DET (CF)
9	"	"	VIO		"	11	"	"	11	"	ORIGINATE MODE
10	7	22	GRY		CONN P1	20	5	CONN P2	20	4	DATA TERM. READY (CD)

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	CRAWFORD	2-24-75	CONTROL DATA	TITLE CONNECTOR ASSY - MSYNC CLH LOOP EXTERNAL TEST CONNECTOR	PREFIX NL	DOCUMENT NO. 74715700	REV 00
CHKD			COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
ENG	KJK		CODE IDENT 34015	FIRST USED ON	32161-028-122		SHEET 1 OF 2
MFG							
APPR							

SHEET REVISION STATUS

2	1
00	00

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05515	CLR RELEASE		2-24-75	KJK

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

32161-028-122

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74715700	REV. 00

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	1	22	WHT		P1	2	2	P1	3	2	SD/RD
2	↑	↑	↑		P1	4	↑	P1	5	↑	RTS/CTS
3	↕	↕	↕		P1	6	↕	P1	20	↕	DSR/DTR
4	↓	↓	↓		P1	12	↓	P1	19	↓	SDCD/SRTS
5	1	22	WHT		P1	22	2	P1	25	2	RI/TB

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DWN	ECKHOLDT	3/16/78	CONTROL DATA	TITLE CABLE ASSY – ASYNCHRONOUS RS 232 TO 103A/113	PREFIX WL	DOCUMENT NO. 74875756	REV A
CHKD	ECH	3/16/78	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
ENG	ECH	3/16/78					
MFG	R. Fredrick	10-4-78	CODE IDENT 34015	FIRST USED ON YA228-A		SHEET 1 OF 2	
APPR	J. Ramos	10-78					

SHEET REVISION STATUS

2	1
01	01
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	008457	CLASS B RELEASE	AV	6-78	VK
A	8648	REMOVED CL "C" PARTS	TD	4-79	VK

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
TD
AA6030

NOTES:
1. CUT OFF REMAINING WIRES FROM CABLE (FIND NO. 8) THAT ARE NOT USED.

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704 — CODE IDENT 34015 — SHEET 2 OF 2 — WL — DOCUMENT NO. 74875756 — REV A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	8	24	SHIELD WIRE		CONN P1	1	3	CONN P2	1	4	PROTECTIVE GND (AA)
2	↑	↑	BLK		↑	2	↑	↑	2	↑	TRANSMITTED DATA (BA)
3	↑	↑	BRN		↑	3	↑	↑	3	↑	RECEIVED DATA (BB)
4	↑	↑	RED		↑	4	↑	↑	4	↑	REQUEST TO SEND (CA)
5	↑	↑	ORN		↑	5	↑	↑	5	↑	CLEAR TO SEND (CB)
6	↑	↑	YEL		↑	6	↑	↑	6	↑	DATA SET READY (CC)
7	↑	↑	GRN		↑	7	↑	↑	7	↑	SIGNAL GND (AB)
8	↑	↑	BLU		↑	8	↑	↑	8	↑	RCVD LINE SIG DET (CF)
9	↑	↑	VIO		↑	20	↑	↑	20	↑	DATA TERM READY (CD)
10	↑	↑	GRY		↑	22	↑	↑	22	↑	RING INDICATOR (CE)
11	8	24	WHT		CONN P1	25	3	CONN P2	25	4	TERM BUSY (-)
12	8	24	W/BLK		—	—	—	—	—	—	⚠1
13	8	24	W/BRN		—	—	—	—	—	—	⚠1
14	8	24	W/RED		—	—	—	—	—	—	⚠1

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DWN	ECKHOLDT	3/16/78	CONTROL DATA	TITLE CABLE ASSY- ASYNCHRONOUS RS-232 TO TERMINAL	PREFIX WL	DOCUMENT NO. 74875846	REV A
CHKD	[illegible]	3/16/78					
ENG	[illegible]	3/16/78	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG	R. [illegible]	10/4/78		FIRST USED ON YA 230-A		SHEET 1 OF 2	
APPR	J. [illegible]	10-7-78	CODE IDENT 34015				

SHEET REVISION STATUS

2	1
01	01
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	008457	CLASS B RELEASE	AV	8-78	[illegible]
A	8648	REMOVE CL "C" PARTS	[illegible]	4-79	[illegible]

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74875846	REV A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	4	24	SHIELD WIRE		CONN P1	1	3	CONN P2	1	3	PROTECTIVE GND (AA)
2	4		BLK			2	3	P2	3		TRANS/RCVD DATA
3	4		BRN			3	3	P2	2		RCVD/TRANS DATA
4	13		WHT	1.0 25.4MM		4	3	P1	5		REQ/CLEAR TO SEND
5	4		RED			5	-	P2	8		RCVD LINE SIG DET
6	4		ORN			6	3		20		DATA SET/TERM READY
7	4		YEL			7	3		7		SIGNAL GND (AB)
8	4		GRN		P1	8	3		4		RCVD LINE SIG DET
9	13		WHT	1.0 25.4MM	P2	4	-		5		REQ/CLEAR TO SEND
10	4	24	BLU		CONN P1	20	3	CONN P2	6	3	DATA TERM/SET READY

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	ECKHOLDT	3/15/78	CONTROL DATA	TITLE CABLE ASSY- ASYNCHRONOUS RS-232 TO 103F MODEM	PREFIX WL	DOCUMENT NO. 74875760	REV A
CHKD	[illegible]	3/15/78					
ENG	[illegible]	4/78	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG	[illegible]	10-4-78		FIRST USED ON YA 229-A		SHEET 1 OF 2	
APPR	[illegible]	10-78	CODE IDENT 34015				

SHEET REVISION STATUS

2	1
01	01
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	008457	CLASS B RELEASE	AV	8-78	[illegible]
A	8648	REMOVED CL "C" PARTS	TD	9 APR 79	[illegible]

NOTES:

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74875760	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	8	24	SHIELD WIRE		CONN P1	1	3	CONN P2	1	4	PROTECTIVE GND (AA)
2	↑	↑	BLK		↑	2	↑	↑	2	↑	TRANSMITTED DATA (BA)
3	↑	↑	BRN		↑	3	↑	↑	3	↑	RECEIVED DATA (BB)
4	↑	↑	RED		↑	4	↑	↑	4	↑	REQUEST TO SEND (CA)
5	↑	↑	ORN		↑	5	↑	↑	5	↑	CLEAR TO SEND (CB)
6	↑	↑	YEL		↑	6	↑	↑	6	↑	DATA SET READY (CC)
7	↑	↑	GRN		↑	7	↑	↑	7	↑	SIGNAL GND (AB)
8	↑	↑	BLU		↑	8	↑	↑	8	↑	RCVD LINE SIGNAL DET (CF)
9	↓	↓	VIO		↓	11	↓	↓	11	↓	ORIGINATE MODE
10	8	24	GRY		CONN P1	20	3	CONN P2	20	4	DATA TERM. READY (CD)

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	A. VOLPE	8-7-78	CDC COMMUNICATIONS SYSTEMS DIV. Santa Ana, Ca. 92704	TITLE CABLE ASSEMBLY ASSYNCHRONOUS CLA TO 202S MODEM (REV CHAN)	PREFIX WL	DOCUMENT NO. 74876194	REV A
CHKD	R.A. CRAWFORD	10/78					
ENG	R.A. CRAWFORD	10/78					
MFG	R. FRIEDRICH	10-6-78					
APPR	JK	11-78	CODE IDENT 34015	FIRST USED ON YA234-A		SHEET 1 OF 2	

SHEET REVISION STATUS

2	1
01	01
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	08507	CL B RELEASE	AV	8-78	JK
A	8648	CHANGED PIN1 REF.	TP	4-79	JK

AA6030

NOTES:

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

DETACHED LISTS

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CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74876194	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX) FT	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	8	22	SHIELD WIRE	50.0	P1	1	3	P2	1	4	GND (FRAME)
2	↑	↑	BLK	↑	↑	2	↑	↑	2	↑	SEND DATA
3			BRN			3			3		REC DATA
4			RED			4			4		RTS
5			ORN			5			5		CTS
6			YEL			6			6		DSR
7			GRN			7			7		GND (FRAME)
8			BLU			8			8		DCD
9			VIO			19			19		SRTS
10			GRY			12			12		SDCD
11	↓	↓	WHT	↓	↓	20	↓	↓	20	↓	DTR
12	8	22	WHT/BLK	50.0	P1	22	3	P2	22	4	RI

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GLOSSARY

This appendix consists of an alphabetical listing of all terms and abbreviations, including acronyms and mnemonics, used in this manual. In the text many signal names listed herein only exist in their false ($\overline{xx}$) or reverse level ($\overline{xx}$*) state but are presented here only in their true or conventional state.

ACLA	Asynchronous communications line adapter
ADD	Address
A-O-I	AND-OR-Invert (circuit or function)
CLA	Communications line adapter
CLE	Communications line expansion
CO	Code bit
COM	Command word
CRC	Cyclic redundancy check
CTS	Clear to send
CTSS	Clear to send status
DAST	Data associated status
DAT	Data receive register
DAV	Data available
DCD	Data carrier detect
DCDS	Data carrier detect status
DLM	Data line monitor
DSR	Data set ready
DSRS	Data set ready status
DTO	Data transfer overrun
DTOS	Data transfer overrun status
DTR	Data terminal ready
ECHO	Echoplex mode
END	End of input frame
FDX	Full duplex
FES	Framing error status
HDX	Half duplex
IADD	Input address
IAV	Input available
IBF	Input buffer full
IC	Input control
IEN	Input end
IER	Input error
IF	Information format
II	Information input
ILE	Input loop error
ILES	Input loop error status
IO	Information output
IODD	Output data demand
ION	Input on
IS	Input select
ISON	Input status on
ISR	Input status request
IST	Input strobe
ISUP	Input supervision
LED	Light-emitting diode
LIT	Loop internal test
LM	Loop multiplexer
LSI	Large-scale integration
MCL	Master clear
MLIA	Multiplex loop interface adapter
Modem	Modulator-demodulator
NAND	Not and (circuit or function)
NOR	Not or (circuit or function)
NPU	Network processor unit
ODATA	Output data
ODD	Output data demand
OER	Output error
OF	Output format
OLE	Output loop error
OM	Originate mode

OON	Output on
OSC	Output select clear
OSL	Output select
OST	Output strobe
OSUP	Output supervision
PES	Parity error status
PI	Parity inhibit
PSET	Parity set
RCK	Receive clock
RD	Receive data
RF	Reference frequency
RHR	Receive holding register
RI	Ring indicator
RIBF	Reset input buffer full
RIS	Ring indicator status
RLSD	Receive line signal detector
RODD	Reset output data demand
RSD	Restraint detector
RSR	Receive shift register
RTS	Request to send
R/W	Read/write
SAV	Status available
SB	Stop bit
SCL	Status clear
SCLA	Synchronous communications line adapter
SD	Send data
SDCD	Secondary data carrier detector
SDCDS	Secondary data carrier detector status
SELI	Select input
SELO	Select output
SODD	Set output data demand
SRLSD	Secondary receive line signal detector
SRTS	Secondary request to send
TB	Terminal busy
TCK	Transmit clock
TD	Transmit data
THR	Transmitter holding register
THRE	Transmitter holding register empty
THRL	Transmitter holding register load
TSR	Transmitter shift register
TTL	Transistor-transistor logic
UART	Universal asynchronous receiver-transmitter

TO CONVERT DECIMAL TO HEXADECIMAL

1. Find decimal number in body of table (Example: 157).
2. Scan horizontally to the left to find the first hexadecimal digit (in this case, 9).
3. Scan vertically up (from 157 in table) to find second hexadecimal digit (in this case, D).
4. Thus decimal number 157 = hexadecimal number 9D.

TO CONVERT HEXADECIMAL TO DECIMAL

1. Find first hexadecimal digit in left-hand column (Example: D).
2. Find second hexadecimal digit in top row (Example: 9).
3. Simultaneously scan horizontally to right (from D) and scan vertically downward (from 9) to find point of intersection in body of table (in this case, 217).
4. Thus hexadecimal number D9 = decimal number 217.

TABLE B-1. HEXADECIMAL/DECIMAL CONVERSION

First Hexadecimal Digit	Second Hexadecimal Digit															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
A	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
B	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
C	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
E	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
F	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

COMMENT SHEET

MANUAL TITLE: Asynchronous Communications Line Adapter DU137-A, DU189-A/B, DU190-A/B, and DU191-A/B, Hardware Maintenance Manual

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