89673100

CONTROL DATA CORPORATION

CONTROL DATA®
SYSTEM 17
1784 COMPUTER

INPUT/OUTPUT SPECIFICATIONS

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Address comments concerning this manual to:
Control Data Corporation
Publications and Graphics Division
4455 Eastgate Mall
La Jolla, California 92037
or use Comment Sheet in the back of this manual.

PREFACE

This specification manual provides the channel operating characteristics for the engineer concerned with the peripheral interface on the CONTROL DATA® 1784 Computer.

The following publications may be found useful:

Control Data Publication	Pub. No.
1784 Computer System Reference Manual	89633400
1784 Computer, Customer Engineering Manual	89633300
TTL A/Q DSA Bus Expander, Hardware Reference Manual	89758600

In addition, the 1784 Computer System Peripheral Equipment Customer Engineering and Reference Manuals should be consulted.

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SECTION 1

INTRODUCTION

INTRODUCTION

SCOPE AND PURPOSE

This specification manual applies to all external equipment used with the CONTROL DATA® 1784 Computer. The purpose of the manual is to describe the common operating characteristics which apply to all peripherals connected on the computer A/Q Data Channel or on the Direct Storage Acess (DSA) Channel.

The manual is written for the engineer concerned with the peripheral interface. The general discussion of the computer input/output access is followed by the mechanical and electrical specifications for all interface assemblies. Descriptions and specifications for the two access channels as well as for the interrupt system are given. More detailed discussion of the logic design of the computer system are found in the applicable manuals written for customer engineers (for a partial list refer to the Preface for this manual). Use the 1784 Reference Manual, publication number 89633400 and the software documentation for applications and programming. Refer to the TTL A/Q DSA Bus Expander Hardware Reference Manual, publication number 89758600 for a description of the interface required between the TTL components of the 1784 and the input/output equipment of the CONTROL DATA® 1700 system peripherals (3000 series current logic).

GENERAL DISCUSSION

The Two Access Channels

Communication between the 1784 computer and its external peripherals takes place through two data channels:

1. Direct Storage Access (DSA) Channel:
   provides fast buffered bi-directional data transfer with direct access to the memory.

2. A/Q Channel:
   provides non-buffered bi-directional data transfer, utilizing the A and Q registers of the Computer. The A register holds the data and the function codes, it also accepts the status replies from peripheral equipment; the Q register holds the address of the peripheral equipment.

The A and Q registers are also used to initiate and monitor data transfer through the DSA Channel.

Rate of data transfer depend on the computer mode of operation. Exact timing specifications are given in later sections; the following table summarizes approximate rates in terms of 16-bit words-per-second. Note that the two versions of the computer differ in their memory cycle times as follows:

1784-1 : memory cycle time 900 nsec
1784-2 : memory cycle time 600 nsec

APPROXIMATE DATA TRANSFER RATES

Channel	RATE (16-bit words/second) for equipment		Notes
	1784-1	1784-2	
DSA	1.1×10^6	1.6×10^6	with priority
	$>0.7 \times 10^6$	$>0.5 \times 10^6$	no priority
A/Q	110×10^3	160×10^3	-

Channel Access

Peripheral equipments communicate with the appropriate channel through peripheral controllers and adaptors. A data bus provides the connection between the peripheral controllers and each input/output channel (A/Q, DSA). The peripherals connected to a bus, time-share the access to the corresponding channel.

The access priority is controlled by the computer interrupt system (refer to Section 6). Access connections to each channel bus are available on identical pins of preassigned slots in the computer enclosure. Each slot can accommodate a peripheral controller. Connections to each channel may be made on a random basis provided bus loading conditions are observed (refer to Sections 4,5). The logic signal levels are those of TTL integrated circuits. A typical configuration of the 1784 Computer with peripheral devices is shown in Figure 1-1.

The slot assignment for peripheral controller and adaptor assembly placements in the computer enclosures is shown in Figure 1-2 (DSA Bus, A/Q Bus). Preassigned slots provide access to both the A/Q and the DSA channel for the following equipments, through their respective controllers:

Peripheral Equipment		Controller
856-2, 856-4	Cartridge Disk Drive (CDD)	1733-2
615-73 or 615-93	Magnetic Tape Transport (MTT)	1732-2
616-72, 616-92 or 616-95	Magnetic Tape Transport (MTT)	1732-3
	Phase-Encoding Formatter (PE) option	10300-1 or 10300-2

Note that the 1784 computer equipment includes the TTY Controller to communicate with a Teletypewriter (TTY) or a Conversational Display Terminal (CDT) through the A/Q channel; refer to the 1784 CE manual, publication number 89633300 and 1784 Reference manual, publication number 89633400.

The mechanical and electrical specifications of the printed wiring assemblies which can be accommodated in the enclosure slots are given in Sections 2 and 3, and the signal and timing specifications on the two channels in Sections 4 and 5.

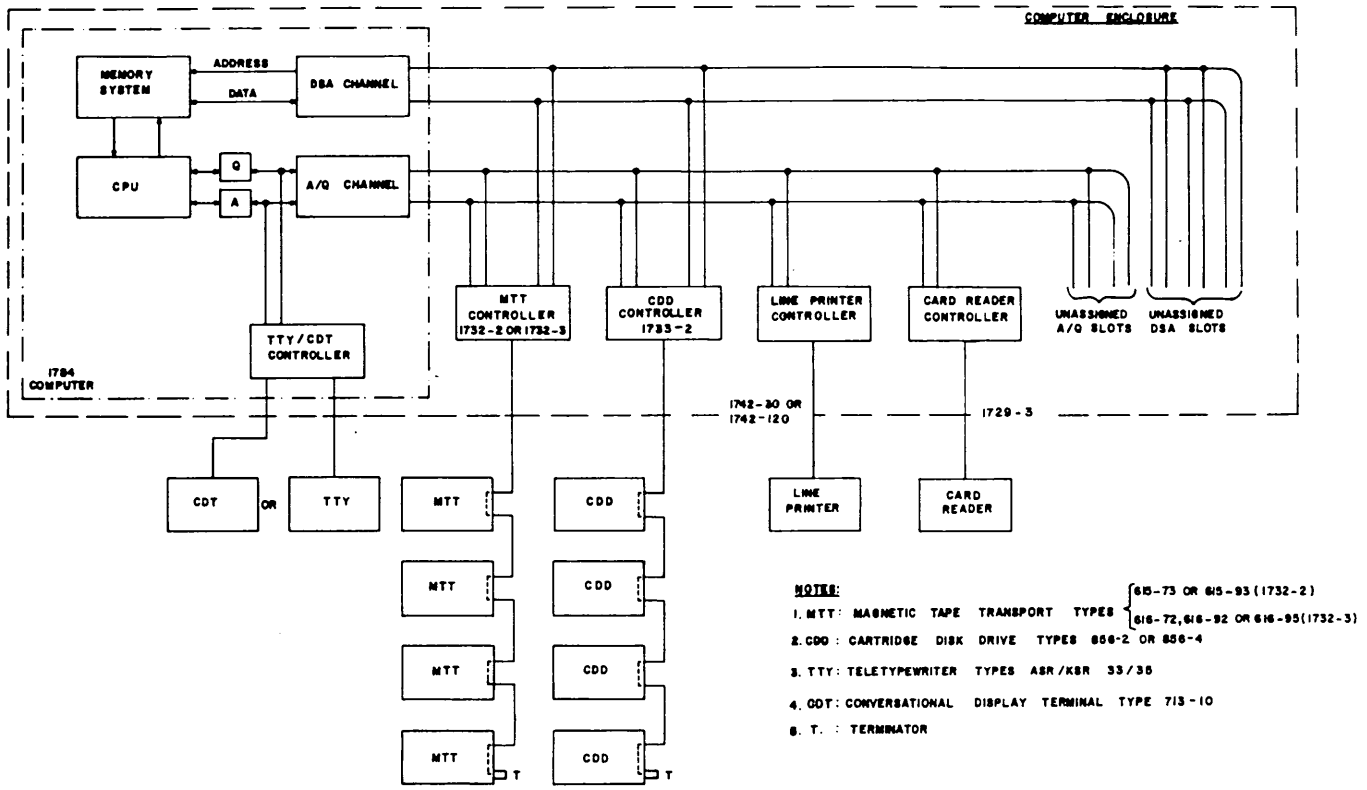
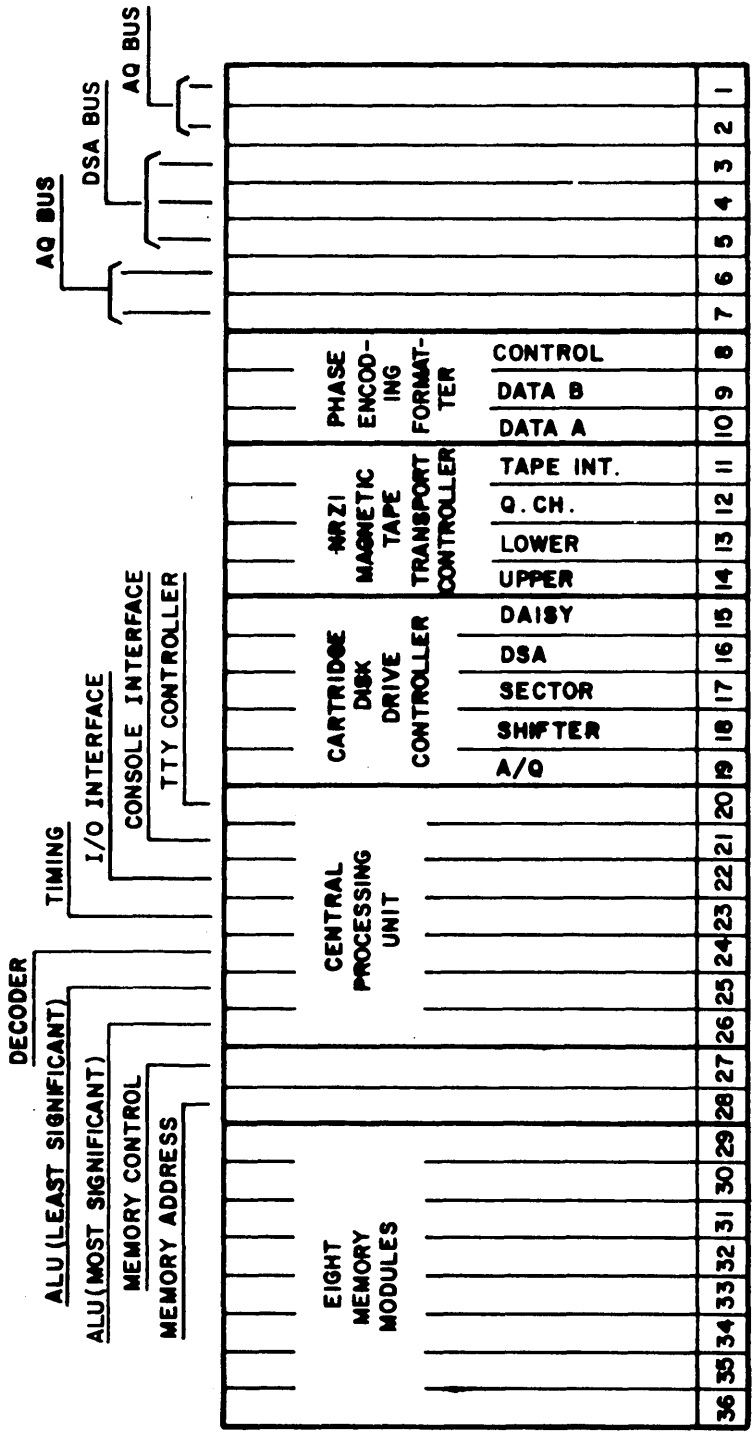
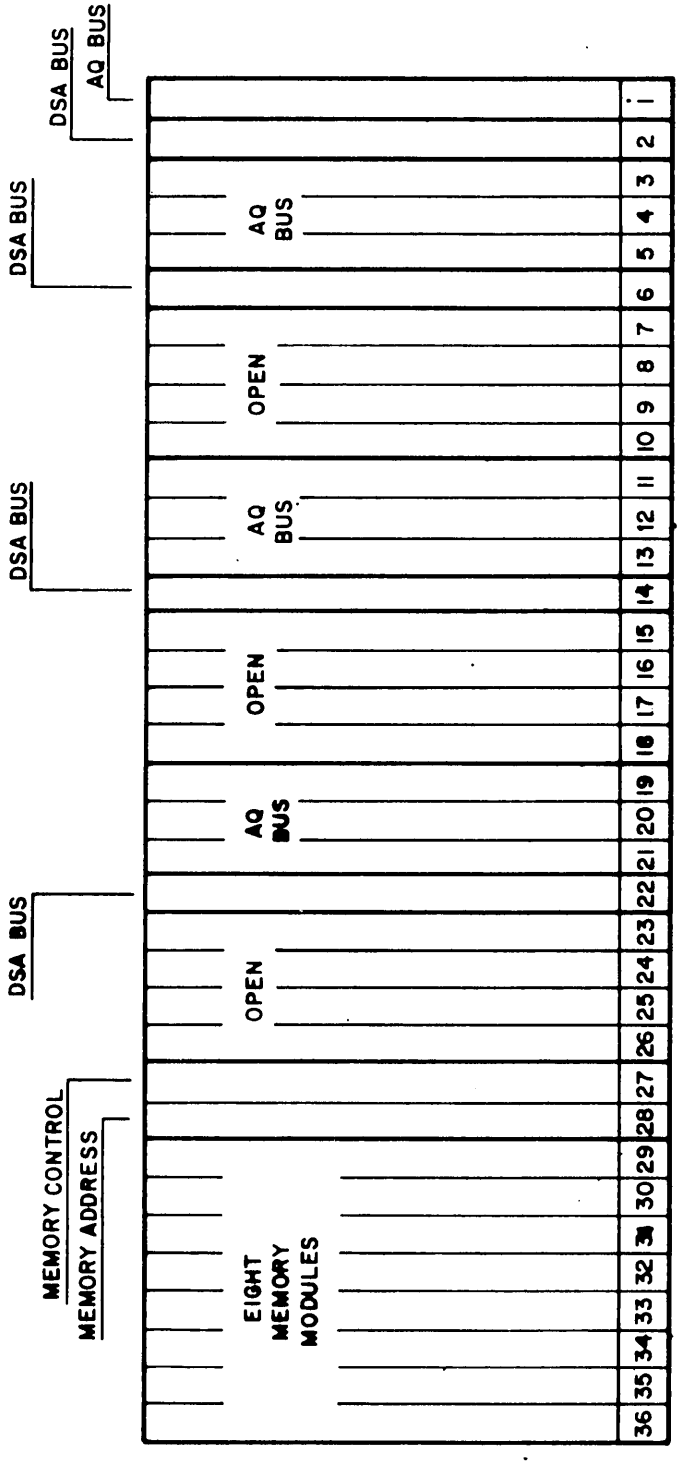


Figure 1-1. Typical Configuration of 1784 Computer System



a. Main Computer Enclosure

Figure 1-2. Card Placement Slot Assignment



b. Expansion Enclosure

Figure 1-2. Card Placement Slot Assignment

SECTION 2

MECHANICAL SPECIFICATIONS

MECHANICAL SPECIFICATIONS

INTRODUCTION

All peripheral controllers and adaptors accommodated within the computer enclosures must conform to the mechanical constraints imposed by these enclosures. Thus the circuitry has to be accommodated on one or more printed wiring assemblies. These must conform to CDC 50-PAK specifications as well as other dimensional and heat-dissipation constraints.

This section gives the applicable specifications. Guide lines to aid in the mechanical design and layout of the printed wiring assembly are given in Appendix B.

SPECIFICATIONS FOR PRINTED WIRING ASSEMBLY

This specification gives the mechanical requirements for Printed Wiring Assemblies (PWA) designed to be accommodated in the 1784 Computer enclosures. The PWA is built on a double sided Printed Wiring Board (PWB).

Dimensions and Standard Hole Locations

For dimensions of the CDC 50-PAK Printed Wiring Board (PWB) and hole locations for the connector and test points refer to Figure 2-1.

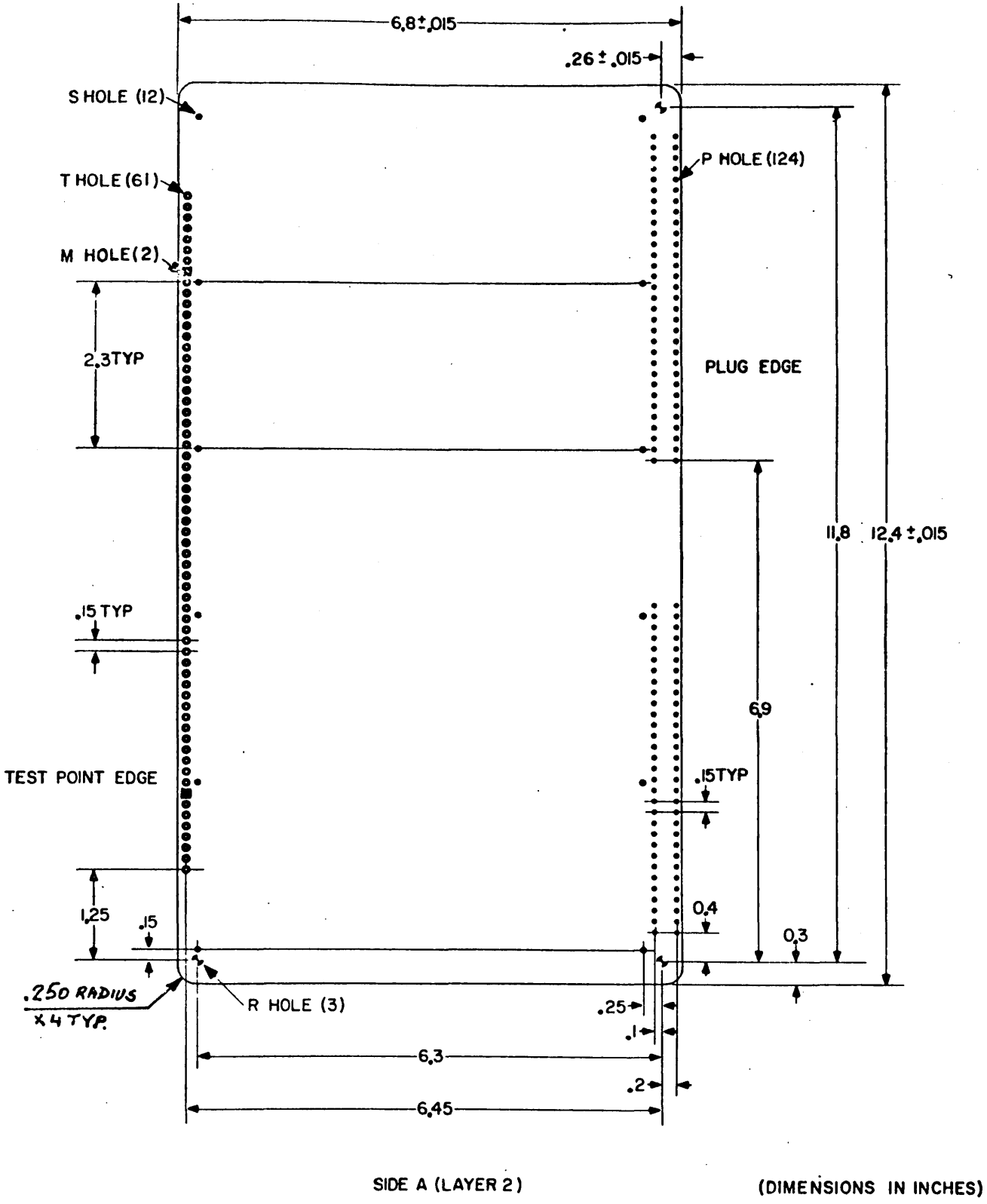


Figure 2-1. 50-PAK Printed Wiring Board Dimensions and Standard Hole Locations

Notes for Figure 2-1

1. All dimensions are in inches.

2. Unless otherwise specified, all hole centers must be located within 0.004 of the intersections of a 0.05 square grid. (All holes must be located ⌖0.008 diameter to a 0.025 BSC grid at maximum material condition).

3. Any unmarked hole electrically isolated from all other copper on the board is Class B.

4. Hole legend:

SYMBOL	DIAMETER	TOLERANCE	CLASS
T	.073	±.005	A
P	.039	±.003	A
S	.090	±.005	B
R	.125	±.005	B
M	.090	±.005	B
Unmarked	.031	+.003 / -.000	A

5. Clearances of components and foil from board edges:

	TEST POINT EDGE	PLUG EDGE	SHORT EDGES
Components	0.4	0.65	0.15
Foil	0.1	0.1	0.15

Material

The base material for the PWB is 0.062 fiber glass according to CDC specification 52338700.

Card Stiffener

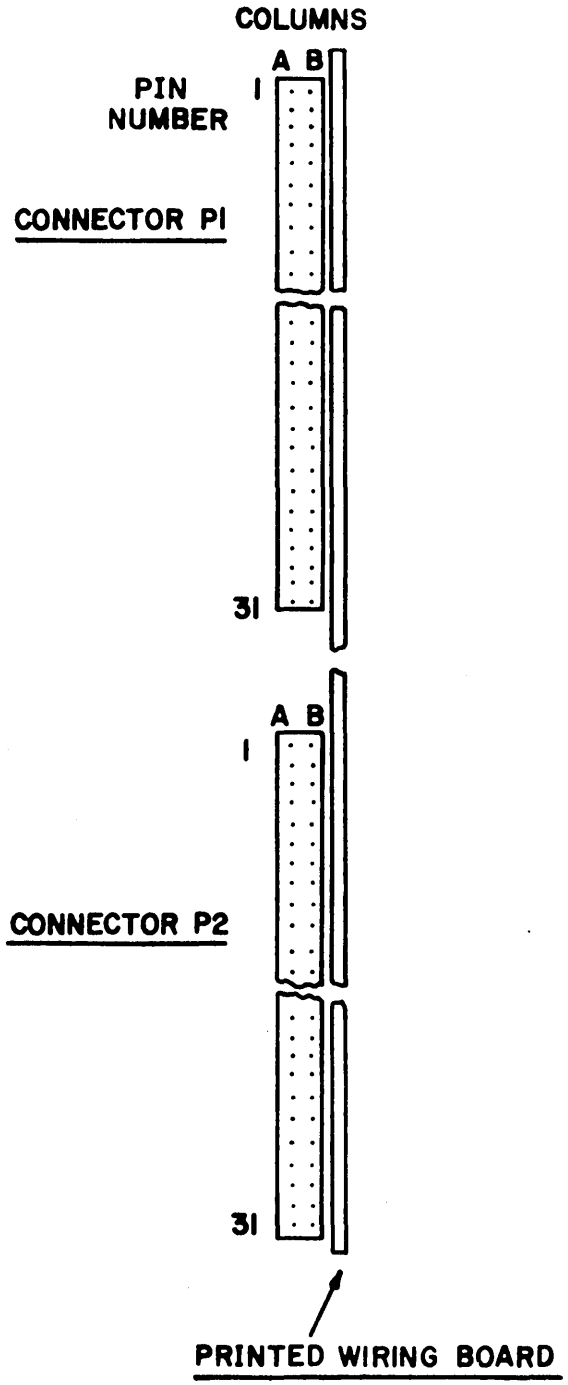
A card stiffener must be used along both long edges of the PWB (plug edge and test point edge, refer to Figure 2-1). The recommended card stiffener is shown in Figure 2-3.

Component Protrusion from Board

Component side (side A)	0.27" max
Soldering side (side B)	0.09" max

Connector

Each PWA plugs into two female connectors on the back-plane of the computer enclosure. Two matching male connectors (CDC P/N 94243400) are mounted on the PWB in the standard holes (refer to Figure 2-1), on the left hand side of the PWB when viewed from the connector end (refer to Figure 2-2).



Notes:

1. View from connector end of printed wiring board.
2. Connector pin designation is illustrated in the following example:
   P1B03 is pin number 3 in column B of connector P1.

Figure 2-2. 50-PAK Connector Pin Configuration

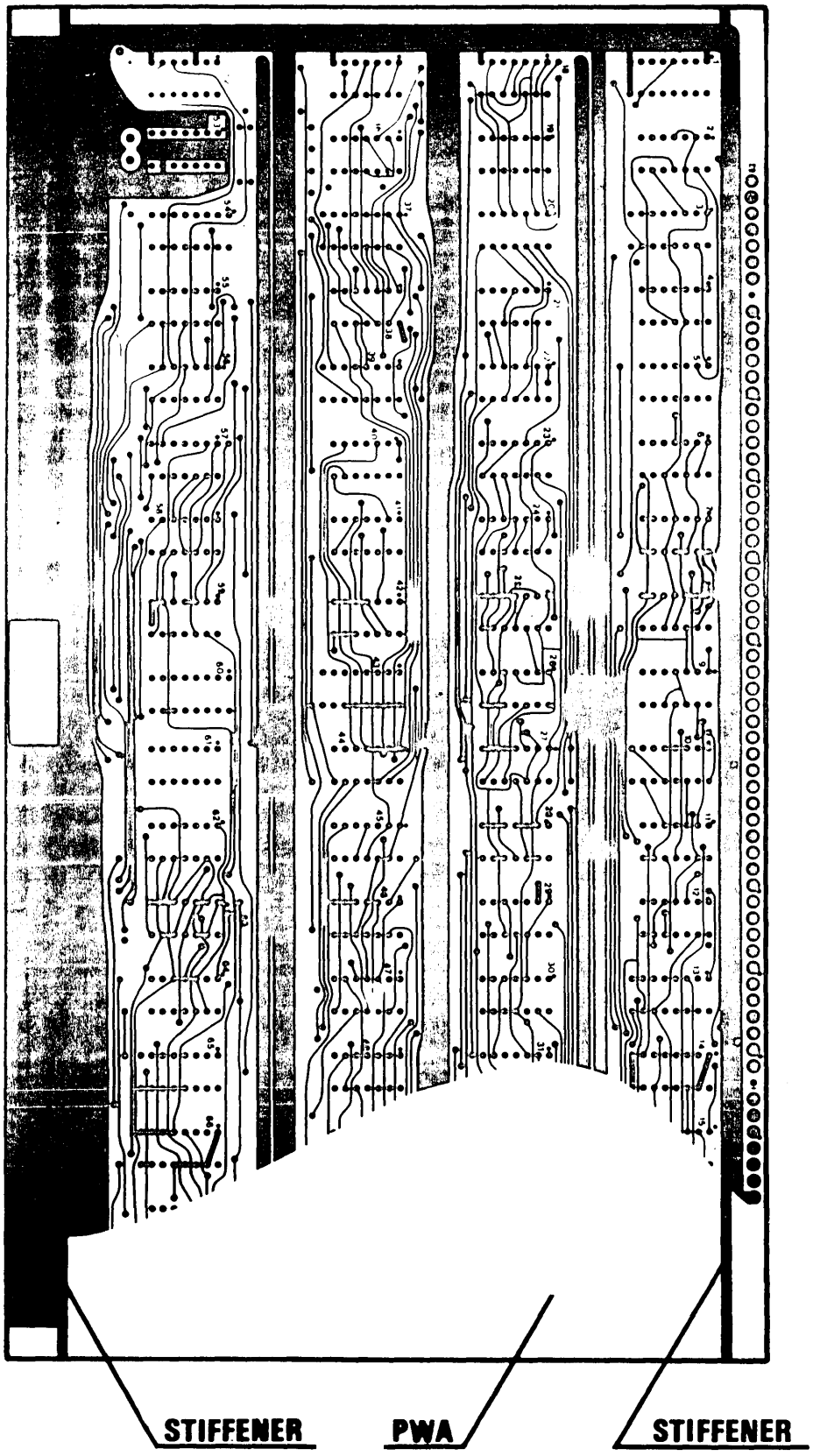


Figure 2-3. Card Stiffener on the 50-PAK PWB

Connector Nomenclature

When the PWA is viewed from the connector end (refer to Figure 2-2) the following designations apply:

- Connector P1 and connector P2 are in top-to-bottom order
- Column A and column B of connector pins are in left-right order
- Pins 1 to 31 are numbered from top-to-bottom.

Pin Assignments

The following connector pins are assigned permanently:

Connector Pin	Assigned to	Remarks
P2A31	V_{CC} (+5V)	Main logic voltage
P1A01	V_{EE} (-5V)	
P1B11 P1A29 P2A03 P2A21	Logic ground	At best four pins are assigned for logic ground
P2B31 P1B01	Logic ground (optional	If there are free pins available, these two should be grounded (order of preference as given)

Test Points

The column of holes on the left hand side of the PWB are designated test points (PWB viewed from component side, connectors to the fight, - refer to Figure 2-1). The Test Points (TP) are numbered consecutively from top to bottom. Test point 1 is reserved for logic ground, 63 for V_{cc}.

Back-Plane Interconnections

The layout of interconnected Printed Wiring Assemblies (PWA's) must be coordinated so that back-plane wiring is as short and direct as possible. To implement this, the designer must specify approximately the plug and pin number for each signal.

SECTION 3

ELECTRICAL SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

INTRODUCTION

This section gives the electrical constraints applicable to the peripheral controllers and adaptors accommodated on Printed Wiring Assemblies (PWA's) within the 1784 Computer enclosures.

SPECIFICATIONS

Supply Voltages

The power supply voltage normally available at the peripheral controller slots is the enclosure main logic voltage (V_{CC} = +5V) and logic ground.

Other supplies are available within the enclosures, refer to Table 4-6 of the 1784 Computer CE Manual, publication number 89633300.

Supply Drain

The PWA may draw current from the enclosure power supply subject to the following limitations:

- the overall current drain allowed is 30A for all controllers in each enclosure (refer to 1784 Computer CE Manual, publication number 89633300).

- current allowed per connector contact is 3A maximum.

- power dissipation (see below).

Power Dissipation

Power dissipation from PWA's accommodated within the computer enclosure is restricted as follows:

Maximum from any one PWA:	15 watts
Average from three or more adjacent PWA's:	10 watts each PWA

Power concentrations substantially higher than average may need special provisions.

Voltage Brought into Back-Plane

If a voltage other than that available in the enclosure, is supplied through the back-plane, it shall be 0 to +7V max if unprotected, or ±30V max if isolated to prevent unintentional shorts to adjacent back-plane pins.

Pin Assignment

Refer to Section 2 of this manual.

Channel Loading

Each signal (data or control) transmitted from a peripheral controller to the CPU in the A/Q channel must be driven by an open-collector NAND buffer (IC Type 7438, CDC P/N 62031200 or equivalent). Each input line is terminated at the input to the CPU by a 180 ohm pull-up resistor (to V_{cc}). The input loads the line with 20 TTL loading units.

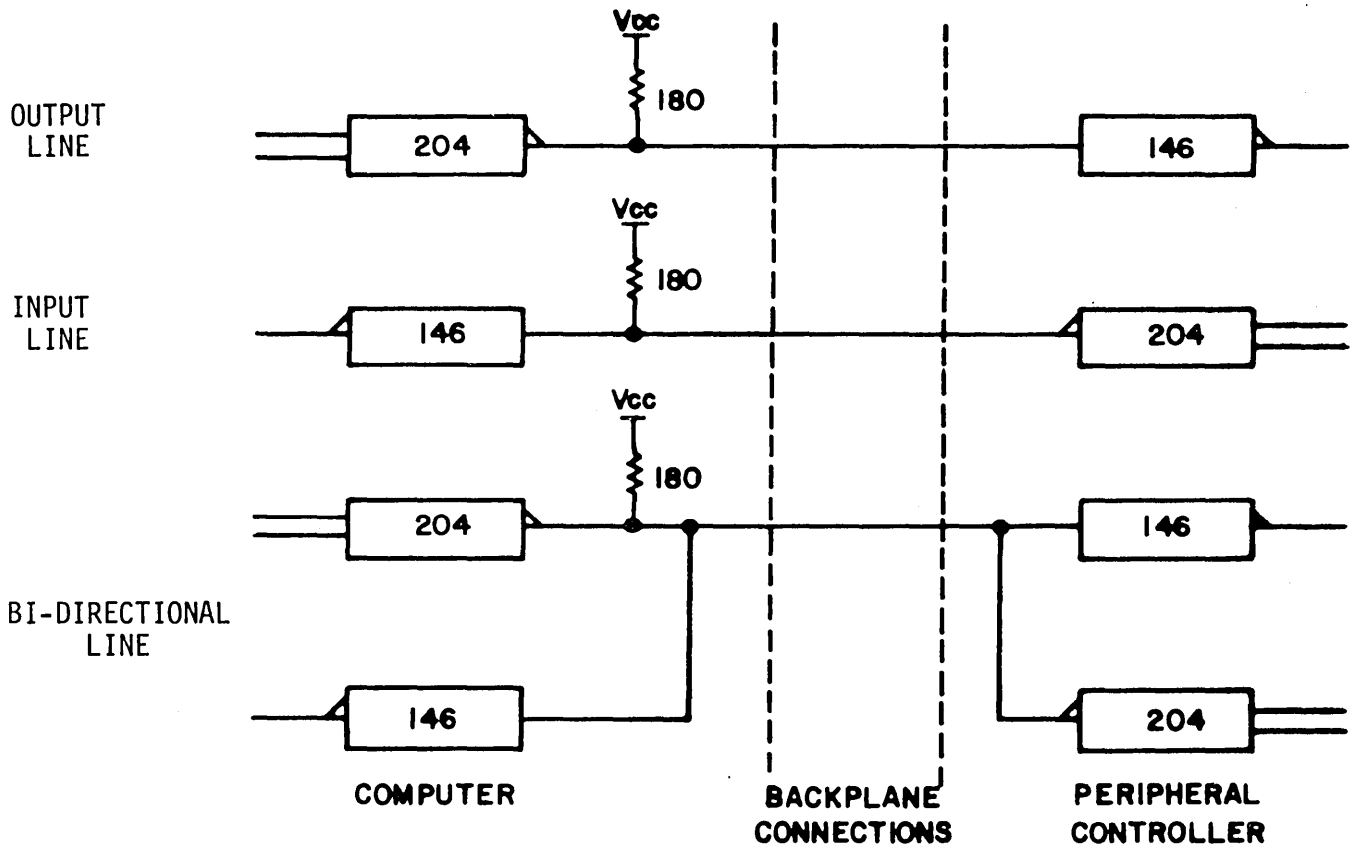
Each device on the A/Q channel is allowed to load any line from the CPU by one TTL load unit. The data bus (A register) is bi-directional. Figure 3-1 gives examples of typical input, output and bi-directional lines.

Peripheral Equipment Connections

For connections between a peripheral equipment and its controller consult the relevant customer engineering manual.

Connection to Expansion Enclosure

For installation of connections between the main enclosure and the expansion enclosure, refer to Section 3 (and in particular Figure 3-4) of the 1784 Computer Engineering Manual, publication number 89633300.



NOTE: 146 can be replaced by any TTL logic circuit gate providing that the line is loaded by only one load unit.

Figure 3-1. A/Q Channel Input/Output Lines

SECTION 4

THE A/Q CHANNEL

THE A/Q CHANNEL

The A/Q channel provides non-buffered bi-directional access to the computer memory and controls the program interrupt system. It transfers data, a word at a time, through the A register using the Q register to hold the address of the peripheral system. The A and Q registers also initiate and monitor the DSA Channel operation. They perform a number of other internal, computer functions as well.

INPUT, OUTPUT ON A/Q CHANNEL

A single 16-bit word is input to or output from the A register when an input or output command is executed by the computer. The data transfer is performed on an asynchronous bidirectional (hand-shaking) basis.

The computer initiates the instruction by generating a command signal as follows:

Operation	Signal
Input to computer	READ
Output from computer	WRITE

The address of the peripheral system selected for the current operation is always available in the equipment (E) field of the Q register. The peripheral controller whose equipment number corresponds to this address responds with a Reply or Reject signal to the command, provided the whole of the Q register content has the correct format (see Address Format below).

Data is transferred on the 16 line bi-directional A register bus when the peripheral controller responds with a Reply signal. The Reply is generated, provided -

- the peripheral system has been addressed correctly
- the peripheral system is in a state to accept the data on the A-register bus (output operation) or it has made the data available on the A-register bus (input operation).

If the peripheral system addressed cannot accept data in input operation or has not made data available in output operation, it normally responds with a Reject signal within 4.0 microseconds of the command (Read or Write).

If the computer does not receive any response within 4.0 microseconds (AB107) it generates an Internal Reject signal which resets the correct instruction. The computer proceeds to the next command after execution of the current command. The address location of the next command, relative to the current command address (P) is given in the following table:

Response	Location of Next Command
Reply	P + 1
Reject	P + 1 + Δ
No response (Internal Reject)	P + Δ

Here Δ is the field consisting of the lowest 8 bits of the input command, the highest bit of Δ being a sign bit.
P is the contents of the P (Program) register.

CONTROL SIGNALS

The operation of the computer and its peripherals is coordinated by a number of control signals.

READ

Input command signal

The Read signal of the computer indicates a request for an input operation from the peripheral equipment addressed. If data is available at the peripheral, its controller returns a Reply within 4.0 microseconds in response to the Read signal. If no data is available, or the peripheral is otherwise not ready, a Reject signal should be returned from the peripheral controller within 4.0 microseconds.

WRITE

Output command signal

The Write signal of the computer indicates the request for an output operation from the computer to the peripheral equipment addressed. If the peripheral can use the data, its controller responds to the Write signal with a Reply within 4.0 microseconds. If the peripheral cannot use the data, its controller responds with a Reject signal within 4.0 microseconds.

Note that in some cases the peripheral addressed does not respond to a Read or Write signal within the specified microseconds. In this case an Internal Reject signal is generated within the computer to terminate the operation.

REPLY

Positive response from controller

In response to the computer Read or Write signal going active the peripheral controller addressed checks conditions within its own system. If it has data available for transmission on the A-register bus (input operation) or it can accept data from the A-bus (output operation), the controller stores the data in its own register and sends

a Reply signal to the computer. This resets the Write signal to inactive which in turn resets the controller Reply and the A-register data lines. Figure 4-1 is the timing diagram of this sequence.

REJECT

Negative response from controller
If the peripheral system addressed cannot perform the computer command, it responds to the Read or Write signal with a Reject within 4.0 microseconds (see Figure 4-1).

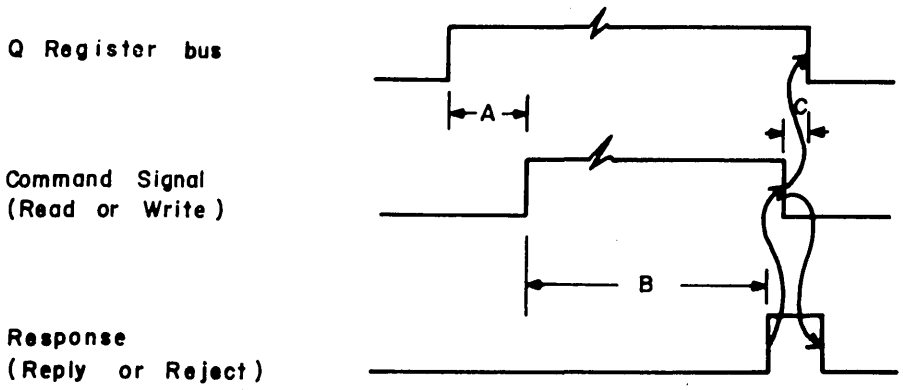
PROGRAM PROTECT

The Program Protect signal is present if the I/O instruction requires access to a protected equipment. If this signal is not present and the equipment addressed is protected, it returns a Reject signal for all access attempts excluding status requests. Conversely, an unprotected equipment will accept both protected and unprotected commands.

The protected status of an equipment is normally determined by the setting of a switch or jumper plug on its controller.

CHARACTER INPUT

This signal is generated by the peripheral equipment if the data transfer is an 8-bit character or less in the low-order bit positions. Equipments which never exceed an 8-bit transfer may have this line active continuously during data transfer.



Notes:

A: 100 nsec maximum
B: 4 μsec maximum
C: 100 nsec maximum

Figure 4-1. Input-Output Timing Diagram

CONTINUE BIT

Bit 15 of the Q register is the Continue bit and can be used to speed up the operation of peripheral systems which require continuous random addressing. This mode operates as follows:

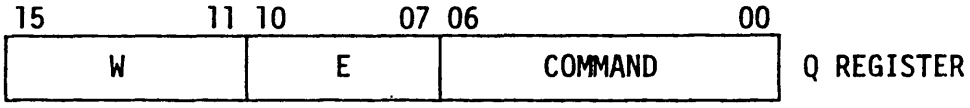
1) The peripheral device is addressed with Q15 = 1 and the remainder of Q set to the desired address. This connects the peripheral.

2) All succeeding addresses with Q15 = 1 will be recognized by this device. Thus 15 bits of address are available to the selected peripheral for internal use.

3) The next address with Q15 = 0 will disconnect the peripheral unless the address of the peripheral is zero (field E all zeros).

ADDRESSING

The Q register of the 1784 computer is used to hold the address codes of the peripheral equipments being accessed. The format of the Q register content is shown below.



CONVERTER

The W field (Q11 ÷ Q15) must be zero for all standard peripheral controllers.

WEZ

Only the zero state of the W field is of interest for the operation of peripheral equipments. The signal WEZ (W equals Zero) indicates this state on a single line allowing the lines Q11 ÷ Q15 not to be connected.

EQUIPMENT

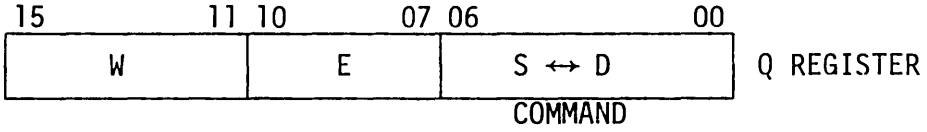
Address bits Q07 ÷ Q10 (field E) contain the equipment number of the peripheral system connected to the channel (0 through F_{16}). The controller of the peripheral system responds when the setting of the Equipment Number and the code in field E match. The Equipment Number is normally set on the controller PWA by means of switches or jumper plugs.

COMMAND CODE

Bits Q00 ÷ Q07 are not preassigned and are therefore available to meet specific requirements of the station and unit. These bits control and direct information on the A/Q channel in the following ways:

- Specify the data transfer
- Direct the control functions and function level
- Direct the status and status level
- Address the line to specific stations under one equipment having multiplexing capabilities.

The Command code is divided into two sections: "S" contains the Station code and "D" contains the Director. The Station code is located in bit 06 and adjacent lower order bits as required. The Director is located in bit 00 and adjacent higher order bits as required. They cannot overlap; all bits in the Command code are not necessarily used.



UNIT (CHANNEL)

Units (or channels) within a peripheral system are controlled by a higher-level controller in that system and respond only to that controller. A function code directs the controller to recognize the information on the A-register bus as the address of the desired unit.

I/O OPERATIONS

DIRECTOR

All input/output operations in the 1784 Computer System are initiated by the Read (Input to A) and Write (Output from A) commands. The 16 bits of register A and the associated bus contain the information of the channel. The meaning of this information during input and output operations is determined by the Director (bits 00 and upward of the Q register). Bit 00 of the Director determines whether the contents of A is data, a function code, or status. The use of the remainder of the Director bits (if any) is detailed in the reference information for each equipment.

TABLE 4-1. USE OF DIRECTOR

DIRECTOR BIT 00	1784 INSTRUCTION	PERIPHERAL OPERATION
clear	Output from A	Write Data
clear	Input to A	Read Data
set	Output from A	Director Function code sent to peripheral
set	Input to A	Director Status of peripheral sent to the computer

DATA TRANSFER

To transfer data, all bits of the Director must be low. A Read or a Write command specifies the direction of the data flow. If the peripheral system can receive data from or send data to the channel, it will respond with a Reply. If the peripheral system is unable to receive or send data, it will normally respond with a Reject. A read or Write signal will always be rejected during data transfers if the device is not Ready.

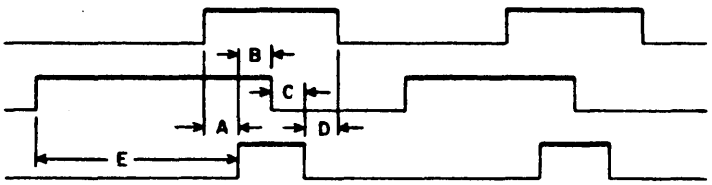
FUNCTIONS — Refer to Section 5 of 1784 Reference Manual, publication number 89633400.

STATUS — Refer to Section 5 of 1784 Reference Manual, publication number 89633400.

A/Q CHANNEL TIMING

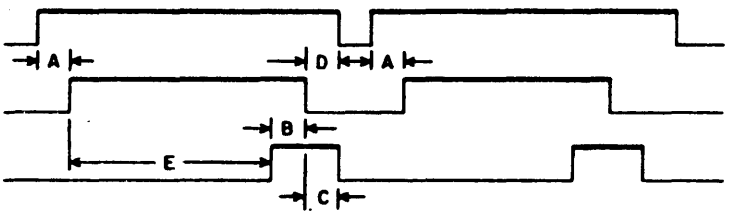
Input and output signal timing restrictions are shown in Figure 4-2. In addition to the signals shown, a timing pulse is generated 135 μsec (±40 μsec) before a Read or Write signal can appear on the A/Q channel. This timing pulse is active for 75 μsec (±20 μsec).

INPUT OPERATION



A = 0 μSEC MIN @ PERIPHERAL DEVICE
B = 0.0 μSEC MIN @ COMPUTER
C = 0.0 μSEC MIN @ PERIPHERAL DEVICE
D = 0 μSEC MIN @ PERIPHERAL DEVICE
E = 4.0 μSEC MAX @ PERIPHERAL DEVICE
0.2 μSEC MIN @ PERIPHERAL DEVICE

OUTPUT OPERATION



A = 0.1 μSEC MIN @ COMPUTER
B = 0.0 μSEC MIN @ COMPUTER
C = 0.0 μSEC MIN @ PERIPERAL DEVICE
D = 0.1 μSEC MIN @ COMPUTER
E = 4.0 μSEC MAX @ PERIPHERAL DEVICE
0.2 μSEC MIN @ PERIPHERAL DEVICE

NOTE:
THE ADDRESS BITS WILL BE ON THE CHANNEL A MINIMUM OF 0.1 μSEC BEFORE AND AFTER THE READ OR WRITE SIGNAL.

Figure 4-2. A/Q Input/Output Timing

A/Q CHANNEL ACCESS

Access to the A/Q channel is available on identical pin locations on the enclosure back plane. The pin locations correspond to prewired slots allocated for the A/Q channel (refer to Figure 1-2). Each slot accommodates the two 62-pin connectors of the 50-PAK printed wiring assembly. Table 4-2 lists pin assignments for the various signals.

TABLE 4-2. A/Q CHANNEL PIN ASSIGNMENTS

P_1			P_2		
A		B	A		B
$\overline{A05}$	1	$\overline{A01}$		1	
$\overline{A06}$	2	$\overline{A02}$		2	
$\overline{A00}$	3	$\overline{A07}$	GND	3	
$\overline{A12}$	4	$\overline{A08}$		4	
$\overline{A11}$	5	$\overline{A09}$		5	
$\overline{A03}$	6	$\overline{A10}$		6	
$\overline{A04}$	7	$\overline{CMI}$		7	
	8			8	
TP	9	$\overline{A13}$		9	
	10	$\overline{A14}$		10	
$\overline{A15}$	11	GND		11	
Q00	12	Q01		12	
Q02	13	Q03		13	
Q04	14	Q05		14	
Q06	15	Q07		15	
Q08	16	Q09		16	
Q10	17	Q11		17	
Q12	18	Q13		18	
Q14	19	Q15		19	
$\overline{WEZ}$	20			20	
$\overline{READ}$	21	$\overline{WRITE}$		21	GND
$\overline{REPLY}$	22	$\overline{REJECT}$		22	
$\overline{PRTM}$	23	$\overline{MC}$		23	
	24			24	
	25			25	
	26			26	
	27			27	
	28			28	
GND	29			29	
	30			30	
	31		V_{CC}	31	

Notes: 1) Q00 ÷ Q15 active high; all other signals active low.

2) V_{CC} = +5V. Total usage of all A/Q and DSA controllers should not exceed 30 amps.

3) GND = logic ground.

SIGNAL DEFINITIONS

TABLE 4-3. SIGNAL DEFINITIONS FOR A/Q CHANNEL

SIGNAL/LINE	DEFINITION
$\overline{A00}$ ÷ $\overline{A15}$	A 16-line bi-directional bus carrying data or status information between register A of the computer and all associated input/output (I/O) system controllers. It is termed the A-bus and is part of the A/Q channel of the computer. Each of the 16 lines of each I/O system is wire-ORed to the A-bus. The direction of flow of the information (to/from the computer) is determined by the input/output commands (READ, WRITE). The signals transmitted from the computer are active low on lines held normally by pull-up resistors within the computer. The line drivers for signals transmitted to the computer on the peripheral controllers are open collector output gates. For typical connection refer to Figure 3-1.
Q00 ÷ Q15	16 lines from the computer which specify the address of the peripheral equipment for data transfer. The 9 highest order bits uniquely specify the device. The lower 7 bits can specify functions of lower level devices.
Converter ($\overline{WEZ}$)	WEZ is active when the W field of the Q register (bits Q11 ÷ Q15) is zero. The W field is always zero during input/output operations.
$\overline{READ}$	Control signal from the computer to the peripheral equipment, initiates one input transfer operation.
$\overline{WRITE}$	Control signal from the computer to the peripheral equipment, initiates one output transfer operation.

Continued on next page

SIGNAL DEFINITIONS (Cont'd.)

TABLE 4-3. SIGNAL DEFINITIONS FOR A/Q CHANNEL (Cont'd.)

SIGNAL/LINE	DEFINITION
$\overline{\text{REPLY}}$	Positive response originating in the peripheral equipment or its controller in response to a signal on the Read or Write line. The Reply is reset when the Read or Write signal goes inactive.
$\overline{\text{REJECT}}$	Negative response originating in the peripheral equipment in response to Read or Write signal indicating that the operation cannot be performed. The Reject is reset when the Read or Write signal goes inactive.
Master Clear ($\overline{\text{MC}}$)	General reset signal sent by the computer. It clears the I/O channels and the peripheral system.
Program Protect ($\overline{\text{PRTM}}$)	Signal transmitted by the computer. It indicates that the operation was initiated by an I/O instruction whose program protect bit is set. It permits buffered I/O devices to write via direct access to protected computer storage locations. When Programmer's Console Protect switch is not set, the Program Protect bit is active.
Character Input ($\overline{\text{CHI}}$)	Signal transmitted to the computer during input operations. When this signal is present during an input to register A, the lower 8-bits of the word are loaded into the lower 8 bits of A without disturbing the upper 8 bits of A.
Timing Pulse (TP)	The Timing Pulse is a 75 nsec (±20 nsec) pulse. It occurs once during each storage cycle. It begins 135 nsec (±40 nsec) before a Read or Write signal can appear on the A/Q channel. This timing applies to the A/Q channel only.

INTERRUPT SIGNALS Refer to Section 6.

SECTION 5

DIRECT STORAGE ACCESS CHANNEL

DIRECT STORAGE ACCESS CHANNEL

The Direct Storage Access (DSA) Channel provides fast external access to the 1784 Computer memory. It transfers data direct between the memory and buffered controllers of bulk storage or other peripherals. The transfer takes place independently of the internal operations of the computer, though it is initiated and monitored by the A and Q registers. Peripherals working through the DSA channel may have priority over others by means of the interrupt system. This allows continuous, fast bulk data transfer.

INPUT, OUTPUT ON DSA CHANNEL

During a DSA input or output command a single 16-bit word is transferred between a buffered peripheral controller and the computer memory.

A peripheral controller on the DSA channel initiates the transfer cycle by means of the Request ($\overline{SRQ}$) signal after obtaining use of the channel through the Scanner.

The direction of data transfer is determined by the Write Enable signal: in its presence (the signal active) data is transferred from the peripheral controller to the memory; in its absence data transfer is in the opposite direction.

The Scanner gives each peripheral controller connected to the DSA channel access to the channel on a first-come-first-served basis, and allows a number of peripherals to time-share the channel. The principles of the scanner operation are described later in this section.

INPUT, OUTPUT ON DSA CHANNEL (Cont'd.)

Priority access for the fast transfer of bulk data can be obtained by each peripheral controller on the DSA channel by means of the DSA PRIORITY interrupt signal. This signal, when active, ensures that the CPU does not access the memory and therefore gives the peripheral on the DSA channel uninterrupted access. In this case the data flow to or from the memory is interrupted only by the memory refresh cycles (refer to Memory System, 1784 Computer CE Manual, publication number 89633300).

The address of the memory location for data transfer must be available at the peripheral controller immediately after the access Request signal (refer to Figure 5-1, DSA Timing Diagram).

Data is transferred when the memory responds to the access Request (refer to Figure 5-1, DSA Timing Diagram).

Error signals (Parity Error, Protect Fault) available from the memory have to be checked in the peripheral controller and appropriate action taken.

CONTROL SIGNALS

The operation of the computer memory and the peripheral controller on the DSA channel accessing it is coordinated by a number of control signals. These are described below. Note that a peripheral controller on the DSA channel obtains access to the channel through the scanner which is described later in this section. The timing diagram of the control signals is given in Figure 5-1.

REQUEST ($\overline{SRQ}$)

The memory access Request signal is generated immediately after the peripheral controller obtained access to the DSA channel through the scanner. It indicates a request to transfer data to/from the memory location specified by the 16 address bits of the peripheral controller (AD00 ÷ AD15).

Write Enable (SWRITE)

The Write Enable signal of the peripheral controller specifies the direction of data transfer as shown in the following table:

Write Enable	Operation	Data Transfer
Active	Write	Memory to Peripheral
Inactive	Read	Peripheral to Memory

Resume ($\overline{\text{SRSM}}$)

The computer response to access request by the peripheral controller is the Resume signal. This signal resets the Request signal and the address bits of the peripheral controller and initiates data transfer. When the Resume signal becomes inactive, the memory parity error and protect fault lines should be checked and appropriate action taken in the peripheral controller.

Program Protect Protect Fault

The Program Protect signal corresponds to the memory word protect bit (bit 17: SD17). If an attempt is made to write into a protected memory location when an unprotected instruction was the ultimate source of this attempt, a protect violation occurs and the Protect Fault line ($\overline{\text{SVFO}}$) is activated; it is available to the peripheral controller to stop data transfer or to take other appropriate action.

Storage Parity
Parity Fault

A storage parity bit is entered as bit 16 (SD16) with every word written into memory. It is generated in the memory system. Storage parity is checked (and consequently a Parity fault may occur) in two cases:

1. when a word is read from memory;

2. when a word is written into a memory location, and the word already in that location is read and its parity checked.

The Parity Fault line ($\overline{\text{PEL}}$) is available to the peripheral controller to stop data transfer or to take other appropriate action.

ADDRESSING

The address of the memory location to be accessed (16 address bits SA00÷SA15) must be available at the address bus terminals immediately after the access request signal becomes active. Note that the 16 bits can address any location within the full 64 kiloword memory.

I/O OPERATIONS

DATA TRANSFER

Data is transferred a word at a time during each memory access cycle. For data transfer from the memory to the peripheral the Write Enable ($\overline{\text{SWRITE}}$) must be active high; the data (Data Out: SD00÷SD15), is active high. Data transfer from a peripheral to the memory takes place with the Write Enable signal inactive (low); the data (Data In: $\overline{\text{SD00}}$÷$\overline{\text{SD15}}$) is active low. Refer to Figure 5-1. If a DSA cycle is followed by another one within the maximum delay specified after the start of Resume ($\overline{\text{SRSM}}$) (see Figure 5-1), and the CPU is waiting to reference the

DATA TRANSFER (Cont'd.)

memory, then the second DSA request will be taken and the CPU forced to wait. This is because the memory system gives the DSA priority over the CPU. Thus the DSA can obtain continuous memory cycles and block CPU memory accesses by sending memory requests at a high enough rate. This does not apply in two bank operation because the CPU can access the upper bank while the DSA sends a request to the lower bank. If the DSA then tries to access the upper bank it has to wait until the CPU access ends.

Note that once a DSA memory cycle has been initiated, the CPU is free to continue the main program while the input/output operation is handled by the appropriate peripheral controller.

DSA PRIORITY ($\overline{SS}$)

Peripherals that require particularly fast access to computer memory may generate a Priority signal to block access from the CPU. Peripherals that require continuous memory access may halt the scanner for the duration of the access.

A peripheral controller on the DSA channel can thus unconditionally block all CPU memory accesses with this signal. This allows it to access both banks at maximum speed, although it has to wait for refresh cycles.

WARNING

Care should be taken in halting the scanner for more than one storage cycle as this may interfere with the operation of other non-buffered devices concurrently operating or the DSA channel.

DSA CHANNEL TIMING

The timing of data and control signals is shown in Figure 5-1. Note that the timing is different for computers with different memory cycle times. The relationship between cycle times and equipments is given here:

Computer	Memory Cycle Time (nanoseconds)
1784-1	900
1784-2	600

Note also that the transfer timing depends on DSA priority assignments and the need to interpose memory refresh cycles.

Refer to the notes to Figure 5-1 and to the explanation on operation with two memory banks at the end of this section.

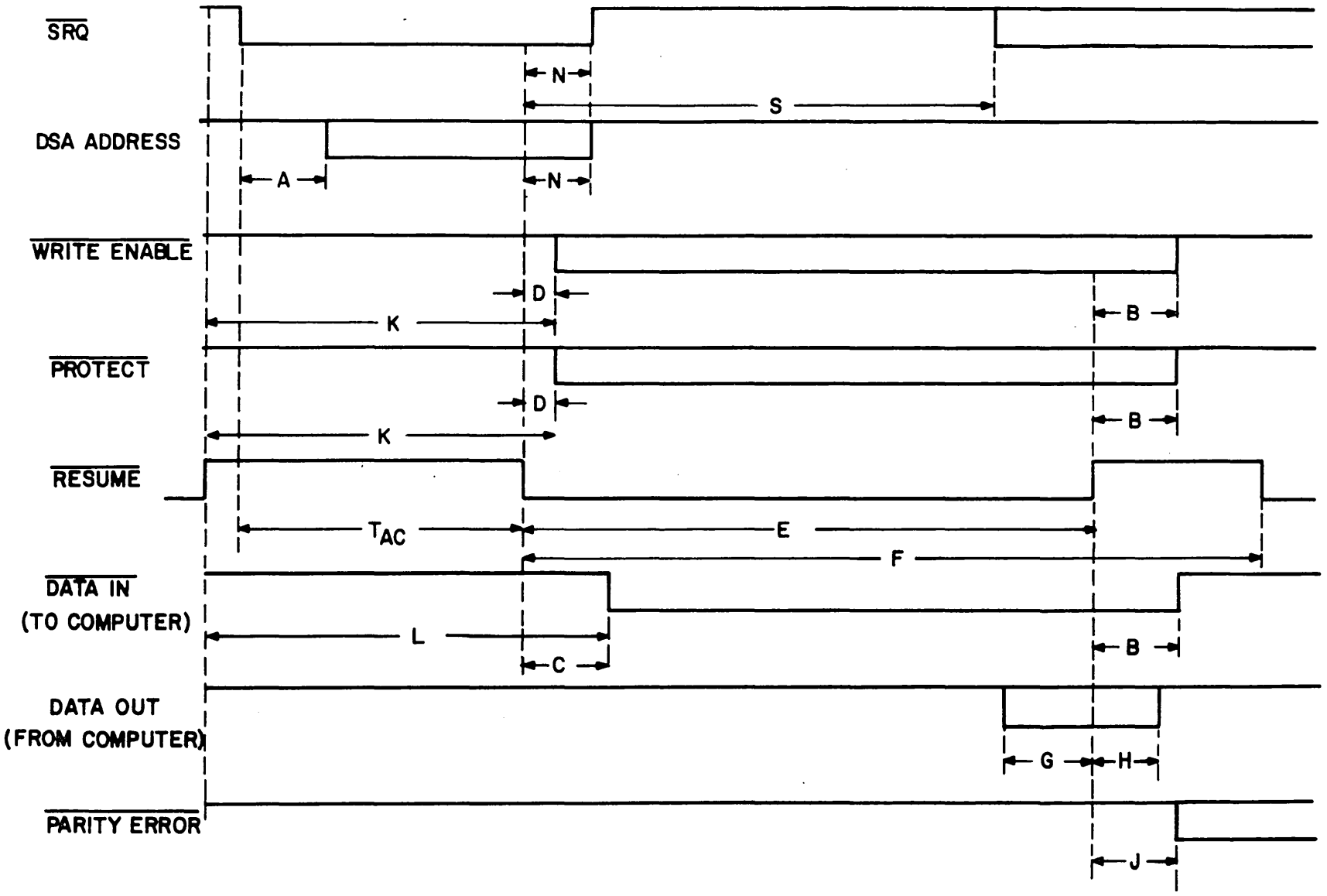


Figure 5-1. DSA Channel Timing

NOTES (to Figure 5-1):

1. Nomenclature:

T_{AC}	: DSA Access Time	$\overline{PEL}$	: Parity Error
$\overline{SRQ}$	: Memory Access Request from DSA channel	DSA Address	: SA00÷SA15
		Data In	: $\overline{SD00}$÷$\overline{SD15}$
$\overline{SWRITE}$	: Write enable	Data Out	: SD00÷SD15
$\overline{SPI}$	: Protect		

2. Timing

	1784-1			1784-2			Remarks
	minimum (nsec)	typical (nsec)	maximum (nsec)	minimum (nsec)	typical (nsec)	maximum (nsec)	
A.	-	-	70	-	-	110	
B.	50	-	175	50	-	200	
C.	-	-	120	-	-	245	
D.	-	-	60	-	-	60	
E.	390	440	490	605	655	705	
F.	-	600	-	-	900	-	
G.	110	-	-	190	-	-	
H.	70	-	-	120	-	-	
J.	-	-	10	-	-	10	
K.	0	-	-	0	-	-	
L.	150	-	-	210	-	-	
N.	0	-	215	0	-	320	
S.	-	-	285	-	-	470	at maximum DSA access rate
T_{AC}	220	-	855	330	-	1240	with DSA Priority
			1455			2140	without DSA Priority

NOTES (to Figure 5-1) (Cont'd.):

3. Refresh cycle time:

   490 nsec once every 32 microseconds (600 nsec Memory)
   735 nsec once every 48 microseconds (900 nsec Memory)

4. Modes of Operation

   Worst Case

   The maximum DSA access time (T_{AC}) occurs when the memory system performs CPU access cycles and successive Refresh cycles.

   DSA Priority signal active

   The memory system cannot perform CPU cycles. The DSA access time (T_{AC}) is minimum; it is increased by the regular occurrence of Refresh cycles.

   Successive DSA requests

   The memory system cannot perform CPU cycles on the memory bank addressed by the equipment on the DSA channel. The DSA cycle time is equal to the memory cycle time (600 nsec or 900 nsec). The DSA cycle time will be increased by the Refresh cycles. Note that on single-bank operation (32KW active) no CPU access can occur if the DSA requests are generated fast enough.

TIMING CONSIDERATIONS FOR TWO BANK OPERATION

The computer can have one or two memory banks (refer to 1784 Computer CE Manual, publication number 89633300), each with a maximum of 32 kilowords. The two banks work independently. Any memory request using an address of $7FFF_{16}$ or less will access the lower bank. Any memory request using an address 8000_{16} or above will access the upper bank.

If the CPU accesses one bank, the DSA can simultaneously access the other bank. In this case, the CPU and DSA can work at maximum speed subject to refresh cycle requirements.

If the CPU and DSA access the same bank, then memory cycles are shared between them. If the CPU requests a memory access while a DSA cycle is in progress, it must wait until the DSA cycle is finished. If a refresh cycle is pending when the DSA cycle ends, the CPU must also wait for that refresh cycle to be completed.

Similarly, if the DSA requests access while a CPU cycle is in progress, it must wait until the CPU cycle is finished. If a refresh cycle is pending when the CPU cycle ends, the DSA must also wait for that refresh cycle to be completed.

DSA CHANNEL ACCESS

Access to the DSA channel is available on identical pin locations on the back plane of the main computer enclosure. The pin locations correspond to prewired slots allocated for the DSA channel (refer to Figure 1-2). Each slot accommodates a standard 50-PAK PWB - refer to Section 2.

Table 5-1 lists pin assignments for the various signals.

TABLE 5-1. DSA CHANNEL PIN ASSIGNMENTS

P_1			P_2		
A		B	A		B
SD05	1	SD01		1	
SD06	2	SD02		2	
SD00	3	SD07	GND	3	
SD12	4	SD08		4	
SD11	5	SD09		5	
SD03	6	SD10		6	
SD04	7			7	
	8			8	
$\overline{MC}$	9	SD13		9	
	10	SD14		10	
SD15	11	GND		11	
	12	$\overline{SS}$		12	
$\overline{SRSM}$	13			13	
	14	$\overline{SPI}$		14	
$\overline{SRQ}$	15	$\overline{SRI}$		15	
	16	$\overline{SCRØM}$ ($\overline{SRØ}$)		16	
$\overline{PEL}$	17	$\overline{SVIO}$		17	
SD16	18	AUTOLOAD		18	
$\overline{SFI}$	19	$\overline{SCFØM}$ ($\overline{SFØ}$)		19	
SD17	20			20	
32KW	21	$\overline{SWRITE}$		21	GND
	22			22	
SA08	23	SA00		23	
SA09	24	SA01		24	
SA10	25	SA02		25	
SA11	26	SA03		26	
SA12	27	SA04		27	
SA13	28	SA05		28	
GND	29			29	
SA14	30	SA06		30	
SA15	31	SA07	V_{CC}	31	

NOTES:

1. Signal polarity
   Address bits (SA00÷SA15) are active high.
   Data bits (SD00÷SD15) are active high for DSA transfers from the computer (Write)
   Data bits (SD00÷SD15) are active low for DSA transfers to the computer (Read).
   All other signals on the DSA bus are as indicated (overlined: active low).
2. Power Supply
   V_{CC} = +5V.
   Total usage of all controllers on A/Q and DSA buses should not exceed 30 amperes.
3. GND = logic ground.

SIGNAL DEFINITIONS

TABLE 5-2. SIGNAL DEFINITIONS FOR DIRECT STORAGE ACCESS (DSA) CHANNEL

SIGNAL/LINE	D E F I N I T I O N
Data (SD00÷SD15)	A 16 line bidirectional bus which carries data as follows: 1. In a DSA Read operation, a 16-bit data word is written directly into the memory locations defined by the address bits of the peripheral controller (active high data). 2. In a DSA Write operation, a 16-bit data word is transferred from a memory location to the appropriate register and then to the peripheral controller on the DSA channel (active low data).
Protect Bit (SD17)	Signal line showing the state of the Program protect bit of the storage location currently being addressed. It is active low when the storage location is protected.
Parity Bit (SD16)	Signal line for the parity signal of the 18-bit memory word. It is active low when the total number of high signals on the 18 lines (16 data lines, protect bit and parity bit lines) is odd (odd parity).
Parity Error ($\overline{\text{PEL}}$)	Signal transmitted from the computer. It is active low when the storage parity error flip-flop is set.
Protect Fault (SVIO)	Signal transmitted from the computer. It is active low when an unprotected peripheral equipment tries to write into a protected memory location via the DSA channel while the front panel Program Protect switch is set.

TABLE 5-2. SIGNAL DEFINITIONS FOR DIRECT STORAGE ACCESS (DSA) CHANNEL (cont'd)

SIGNAL/LINE	D E F I N I T I O N
Address (SA00:SA15)	A 16 line bus which transmits the address of the storage location to be accessed from the peripheral controller. When the storage cycle starts, the address is placed in the appropriate computer register.
Request ($\overline{SRQ}$)	Signal transmitted to the computer requesting access to storage. The signal becomes inactive after the computer responds by the Resume signal.
Resume ($\overline{SRSM}$)	Computer response to Request. Starts DSA data transfer, resets Request signal and address bits, indicates timing for checking Parity Error and Protect Fault lines.
Write Enable ($\overline{SWRITE}$)	Control signal in peripheral controller for directing data transfer. When the signal is active, data is transferred from the computer memory location addressed to the peripheral controller (Write operation). When the signal is inactive, data is transferred from the peripheral controller to the memory location (Read operation).
Protect ($\overline{SPI}$)	Signal transmitted to the computer. When active low it allows data from a peripheral system to be written into a protected storage location.
Master Clear ($\overline{MC}$)	General reset signal transmitted from the computer. When active low it clears the peripheral system.

SIGNAL DEFINITIONS (Cont'd.)

TABLE 5-2. SIGNAL DEFINITIONS FOR DIRECT STORAGE ACCESS (DSA) CHANNEL (cont'd).

SIGNAL/LINE	D E F I N I T I O N
Priority ($\overline{SS}$)	DSA priority signal transmitted to the computer. When active low, it prevents the CPU from accessing the memory. This increases the DSA data transfer rate because data transfer from a peripheral equipment on the DSA channel will not be interrupted by the CPU. Note that the data flow is interrupted by refresh cycles even if the DSA priority is set.
$\overline{AUTOLOAD}$	Active low signal transmitted from the computer when the AUTOLOAD pushbutton on the Programmer's Console is pressed.
Scan Forward In (SFI) Scan Reverse In (SRI) Scan Forward Out (SFØ) Scan Reverse Out (SRØ)	Four lines connecting the peripheral controller with the distributed scanner (see Scanner Connections).
32KW	Signal transmitted from the computer. It is inactive when the computer is set to operate with two memory banks (65 Kilowords) by the 32K/65K mode switch on the Programmer's Console. It is active for one memory bank operation (mode switch at 32K).

DISTRIBUTED SCANNER

Access to the DSA channel is controlled through the distributed scanner. This is formed of flip-flops, one on each peripheral controller, connected as a ring-counter-oscillator.

This scans the indicating lines from the controllers requesting channel access (NEED); a controller requests access to the channel by halting the scanner. The various scanner stages (one in each device) are connected through the enclosure back plane wiring. This connection has to be done at the time of system installation. The following paragraphs will aid in understanding the setting up of the distributed scanner.

SCANNER OPERATION

When a peripheral equipment controller connected to the DSA requires access to computer storage, it generates the Need signal. This causes the scanner to halt at the stage in this controller; at the same time the Request ($\overline{SRQ}$) signal is activated to obtain memory access for the controller. Typical timing is shown in Figure 5-3

SCANNER CONNECTIONS

Any scanner stage flip-flop transmits an active high signal when set and a low signal when cleared. A stage receiving an active high signal will set, while a stage receiving an active low will attempt to reset. The stages must be connected to form an oscillating ring by appropriate signal reversals in the chain and by connecting the output of the last stage to the input of the first one.

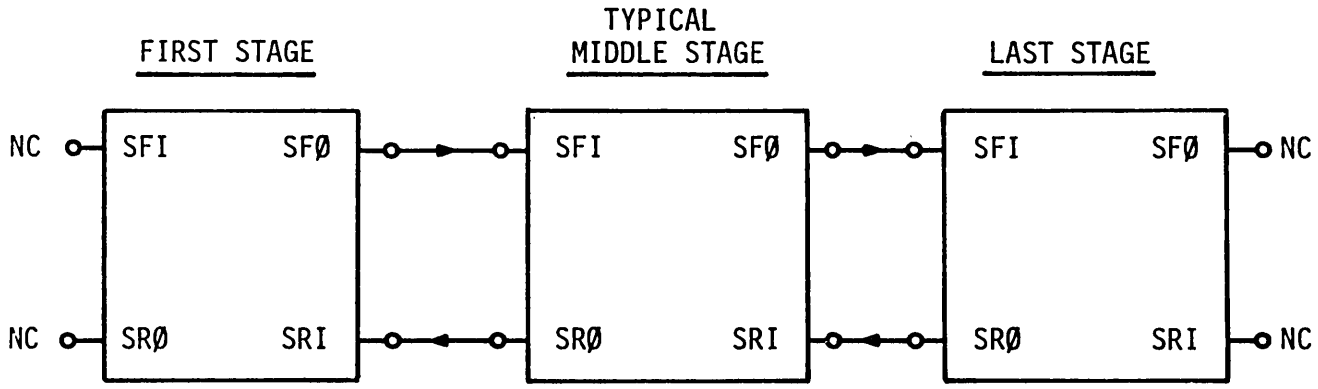
The position of the controller in the scanner chain depends on the particular system. Three positions can be distinguished, each having a specific polarity, as follows:

CONTROLLER POSITION	SIGNAL POLARITY	
	RECEIVED	TRANSMITTED
First	High	Low
	Low	High
Middle	High	High
	Low	Low
Last	High	High
	Low	Low

To aid in the connection, inputs and outputs for forward and reverse scan are distinguished on each scanner stage, as follows:

	Input	Output
Forward scan	Scan Forward In (SFI)	Scan Forward Out (SFØ)
Reverse scan	Scan Reverse In (SRI)	Scan Reverse Out (SRØ)

Figure 5-2 illustrates the connection of three stages in an oscillating ring. Note that there may be several middle stages.



Notes:

1. NC: Terminal not connected

2. All connections are on the enclosure backplane. In interconnection diagrams the following changes in nomenclature may occur:

   SCFØM for SFØ, SCRØM for SRØ.

Figure 5-2. Scanner Wiring Connections

SPECIAL CONNECTIONS

1. When only two peripheral controllers are connected to the DSA channel, the first and last stages will be connected directly as follows:

First Stage		Last Stage
SFØ	⟶	SFI
SRI	⟵	SRØ

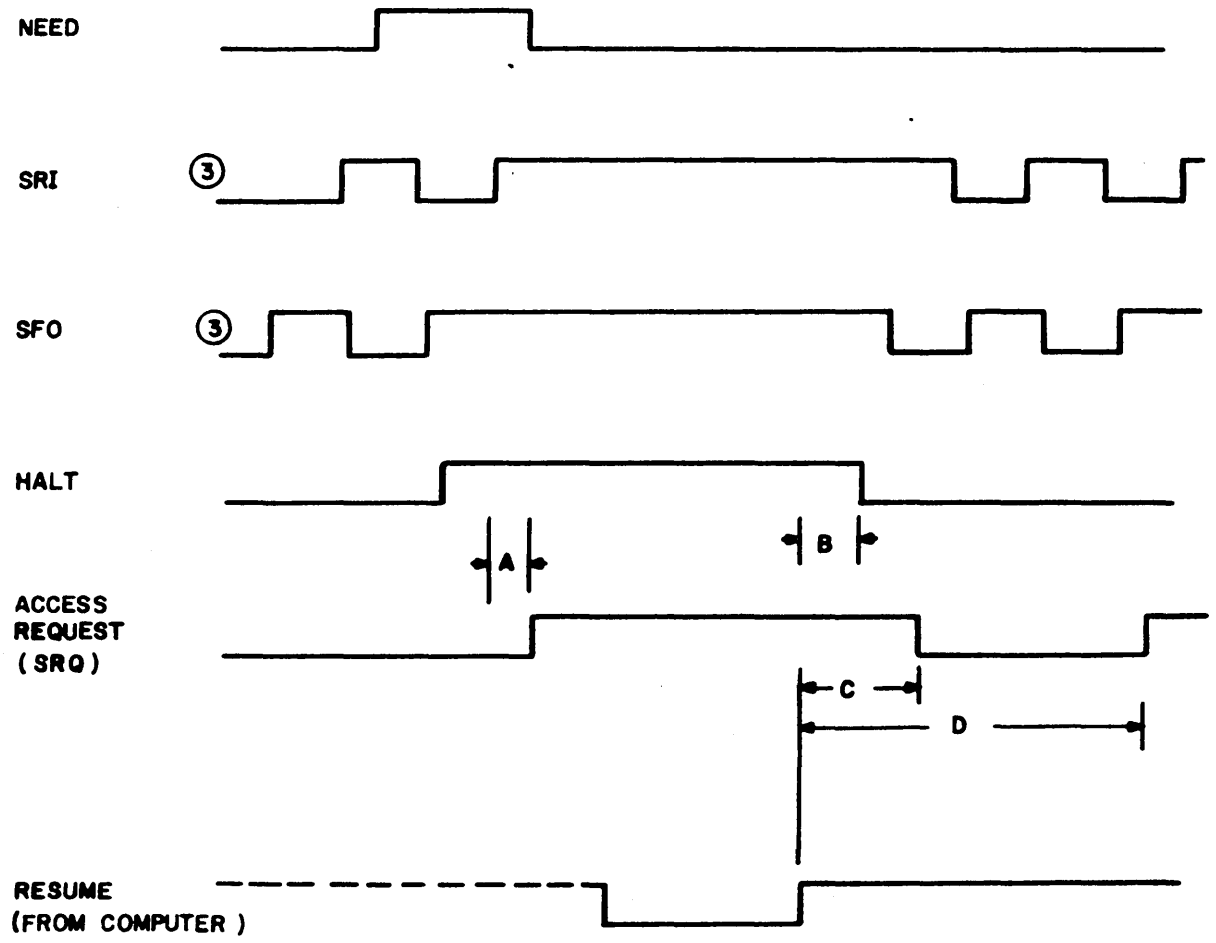
2. When only one peripheral controller is connected to the DSA channel, it will be connected to be self-oscillating as follows:

Single Stage

3. If a controller is removed from a middle position in the scanner, jumpers must be connected in its place as shown:

Previous Stage	Removed Middle Stage	Next Stage
SFØ	—o—o—	SFI
SRI	—o—o—	SRØ

4. If a controller is removed from the first or last position of the scanner, the one next to it is set in its position.



NOTES:

1. A: min. 0
   B: min. 0
   C: ≤ 100 nsec
   D: ≤ 275 nsec
2. All signals shown valid high, irrespective of actual polarity.
3. SRI, SFØ shown assuming scanner stage to be first in the chain. (SFØ is sometimes shown as SCFØM)

Figure 5-3. Typical Scanner Timing

SECTION 6

INTERRUPTS

INTERRUPTS

Peripheral systems have the ability to send an interrupt signal, via the interrupt hardware, to the computer CPU. There is an internal interrupt and 15 external interrupt positions, each brought out on an individual computer back plane pin. These are used to interrupt the computer program on specific conditions arising in the peripherals. The computer program assigns priority for the interrupt positions, higher priority ones always taking precedence. The hardware priority arrangement is a first-come-first-served scheme to prevent the overlap of interrupts.

INTERNAL INTERRUPT

Internal interrupt is generated within the computer on occurrence of the following fault conditions:

- storage parity error
- program protect fault
- power failure

Internal interrupts are assigned positions 00 in the mask register (M) and normally have the highest priority.

INTERRUPT SIGNALS

The following peripheral interrupt requests are set and cleared by director function codes of the computer.

Interrupt on Data

On a Read operation, the interrupt occurs when data has been loaded into the data hold register of the peripheral system and is ready for transfer to the computer. The interrupt response is cleared by the reply to data transfer. On a Write operation, the interrupt occurs when data can be loaded into the data hold register of the peripheral system. The interrupt response is cleared by the reply to data transfer. A status bit indicates the condition of the interrupt.

Interrupt on End-of-Operation

The operation may or may not be in progress at the time of the interrupt selection, but the interrupt cannot occur as a result of an operation which has ended before the selection was made. An operation and an End-of-Operation must be defined for each peripheral device. A status bit indicates the condition of the interrupt.

Interrupt on Alarm

An alarm condition that exists at the time of the interrupt request immediately provides a response. The alarm conditions must be defined for each peripheral device. A status bit indicates the state of each alarm condition.

Other interrupts may be defined by further status bits of the computer. For a description of the director system refer to the Reference Manual for the 1784 Computer System, publication number 89633400.

INTERRUPT HARDWARE

The peripheral system interrupt lines are connected through the 15 external interrupt positions on back plane pins of the main enclosure. A single wire (CDC part number 89724700) is required to connect an interrupt source to the appropriate interrupt level. Table 6-1 lists the pin assignments for the interrupt levels. Interrupt signals are active low.

INTERRUPT PRIORITIES

The computer program determines the interrupt priorities, that is, the order in which the peripheral interrupt requests are dealt with by the computer. The program acts through the computer mask (M) register. Should two interrupts occur simultaneously, the hard-wired order of interrupts will determine priorities (refer to Table 6-1).

TABLE 6-1. INTERRUPT ACCESS PIN ASSIGNMENT ON A/Q SLOTS

Interrupt Line	Computer	
	Card Slot	Pin
00	--	--
01	25	P1B10
02	25	P1A07
03	25	P1B07
04	25	P1A05
05	25	P1A06
06	25	P1B06
07	25	P1B05
08	26	P1A10
09	26	P1B10
10	26	P1A07
11	26	P1B07
12	26	P1A05
13	26	P1A06
14	26	P1B06
15	26	P1B05

Notes:

1. Interrupt line 00 is internal.

2. Interrupt hardware priority levels are in reverse order of interrupt line numbers (highest hardware priority assigned to line 00).

PROTECTED PROGRAM

Each peripheral equipment controller working with a protected program has a protect switch (or jumper plug). When this switch (or plug) is set to its "protect" position, the peripheral system accepts only protected instructions and status requests, it responds with a Reject to all unprotected instructions except status requests.

A protected instruction is defined by an active project line. When the peripheral program protect switch (or plug) is in the unprotected position the protect line is not monitored and the peripheral system responds to both protected and unprotected instructions.

If the peripheral system uses the direct storage access (DSA) channel, it must store the state of the program protect line at the time a computer I/O instruction causes it to access storage. The Stored Program Protect state is then presented to storage with each storage request. Thus, a protected I/O instruction allows the peripheral system to transfer data into any storage location. An unprotected I/O instruction allows the peripheral to transfer data into unprotected storage locations only.

APPENDIX A

PERIPHERAL CABLES

PERIPHERAL CABLES

All signals from the computer to a peripheral equipment are processed by the appropriate peripheral controller in an A/Q or DSA channel slot in the enclosure. The signals from the controller to the peripheral equipment are taken through

a. an internal cable from the enclosure back plane connector to the equipment connector on the enclosure rear cover;

b. an external cable from the equipment connector to the peripheral equipment.

Figure A-1 shows a typical schematic arrangement.

Cable and wire lists are given in the appropriate CE Manual.

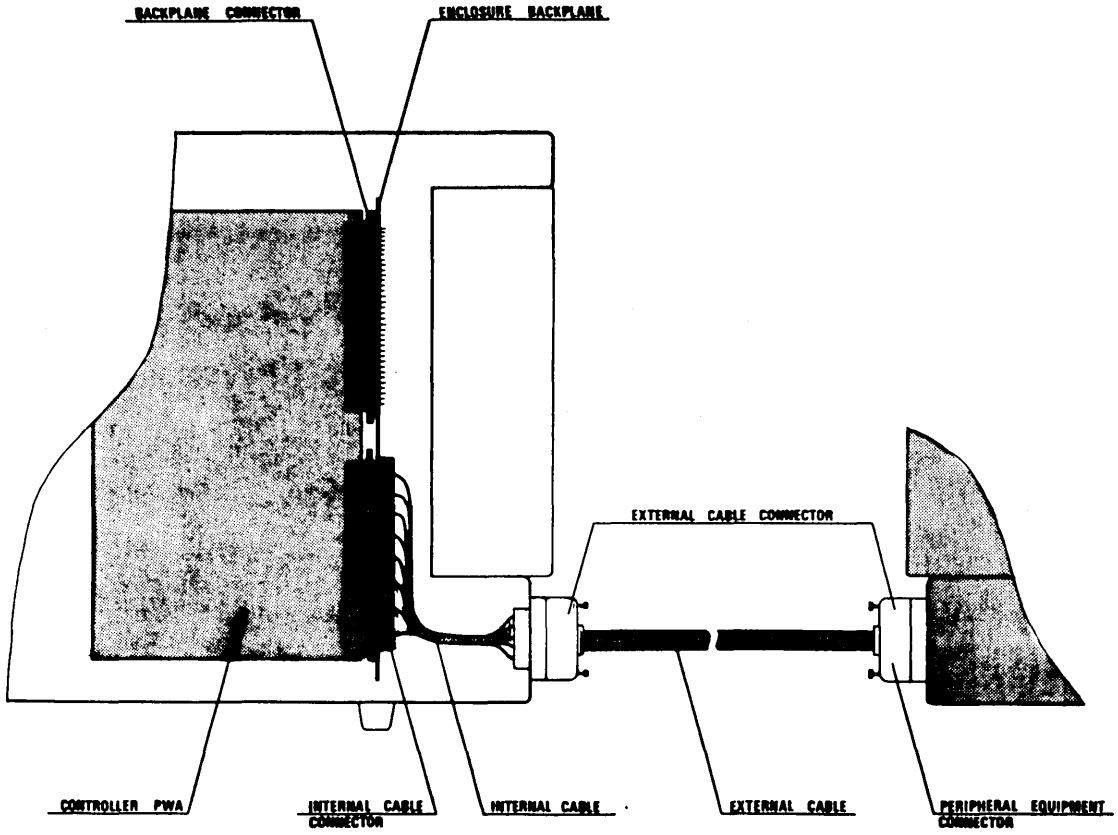


Figure A-1. Arrangement of Internal and External Cables

DESIGN AIDS

INTRODUCTION

This appendix is included in the 1784 Computer I/O Specification Manual to aid the engineer concerned with the design of peripheral controllers. The information supplied gives current practice in relation to the preparation and design of printed wiring assemblies for equipment relating to the 1784 computer. It is not to be regarded as a specification.

ARTWORK FOR THE PRINTED WIRING

Note: Dimensions are given in inches, after photo reduction.

Layout Grid and References

The artwork is done on a standard 0.05 inch grid. An X axis and a Y-axis are defined by three reference points located on the board (refer to Figure B-1, B-2). Holes through the reference points are used to position the board for automated production operations. Any holes or other board features which are not located on the grid must be fully dimensioned, using the reference axes, on the printed wiring board detail specification.

Reference Side

The reference side for all dimensioning and for all manufacturing operations is side A also referred to as layer 2 (Figure B-1). The other side of the board is side B.

Holes

Holes are shown on the artwork by tape pads with a 1/64 inch diameter aperture centered within 0.005 inch of the true grid position.

Board Edges

The board edges are shown on the artwork by straight lines, drawn in ink, 0.020 inches wide. The inside edge of the inked line shows the board edge. At outside corners the lines extend 0.5 inch past the actual board outline.

Dimensioning and alignment

The artwork includes three targets outside the limits of the board, for dimensioning and photographic reduction (refer to Figure B-2). The targets are referenced to the on-board axes and the origin formed at the point of intersection of these axes. A single dimension for photo reduction is given on the artwork, from the origin to the target on the long axis (DIM).

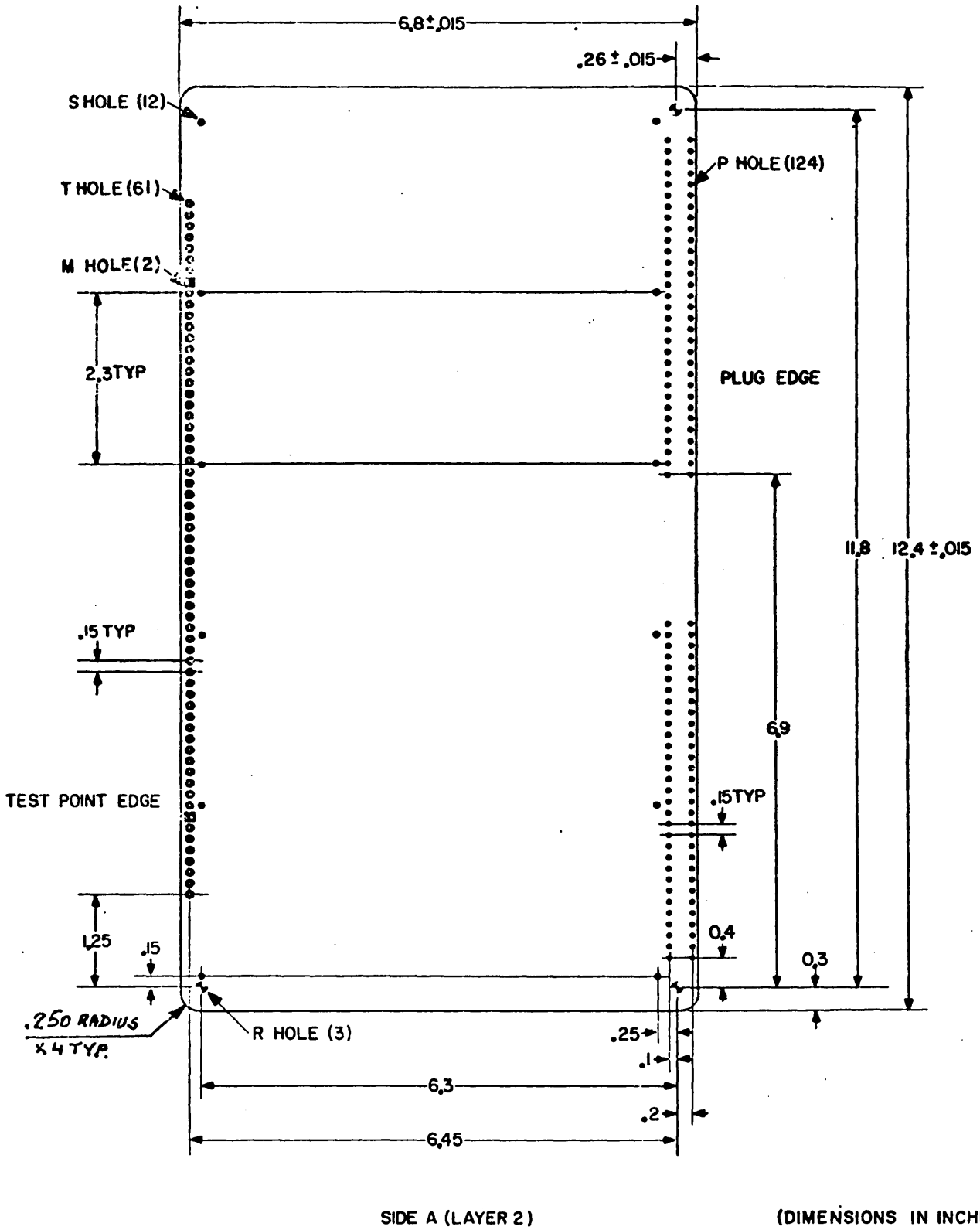
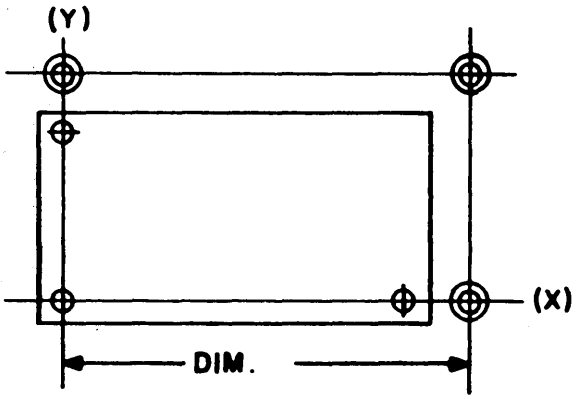


Figure B-1. Printed Wiring Board Dimensions and Standard Hole Locations



Notes: ⊕ on-board reference points

◉ off-board reference points

The reference axes (x, y) are the straight lines drawn through the three on-board reference points.

Figure B-2. Dimensioning and Alignment

Artwork for Printed Conductors

Note: all dimensions are given in inches, after photo reduction

Dimensions:

	Dimension			Remarks
	Min	Typ	Max	
Line Width	0.0115	0.0125	0.014	Conductor for Logic Line
Component pad	0.059			Diameter
Non-Common Conductor Clearance	0.010	0.015		pad-to-pad
	0.011			line-to-line
	0.012			line-to-pad

Feed-thru Holes

If avoidable, feed-thru holes should not be located under packages or other components.

Component Mounting Holes

Hole pattern:
For components designed for mounting on PWB, use the pattern specified by the manufacturers. For axial lead components, hole spacing is the specified maximum body length plus 0.25 inch, rounded off to the nearest 0.05 inch.

Component spacing:
The clearance between mounting holes of adjacent packages is 0.15 inch minimum.

The clearance between mounting holes of axial lead components mounted end to end is 0.2 inch minimum.

High Speed Signal Lines

To avoid reflections on signal lines, special treatment is needed for any line whose total on-board and wired length exceed the total shown below. Any line exceeding this length must be designed so that:

- no branch exceeds the tabulated stub length;
- the impedance of the line is controlled;
- the line is terminated - refer to Terminations below.

Driver Type	Total Line Length	Stub Length
54/74	20 inch	4 inch
54H/74H	15 inch	3 inch
54S/74S	12 inch	2.4 inch

Parallel Signal Lines

Parallel runs of signal lines close together should be avoided.

If such runs are unavoidable, the surface of the PWB (side B) opposite the parallel run must be a continuous copper area to provide shielding and ground current return.

The table lists examples of maximum allowable parallel device input signal (or flip-flop output) lines with a continuous copper area backing. All signal lines are assumed parallel to an adjacent line propagating its signal in the opposite direction.

Signal Line	Spacing (center-to-center) inch	Allowable Parallel Run (maximum) inch
74 series	0.050	8
	0.025	7
74H series	0.050	5
74S series	0.050	2.0
	0.025	2.5

Note that an input is sensitive if it is one stub-length or less from a parallel run. Stub lengths are listed in the table for maximum line lengths above.

Processing for Printed Conductors

Note: all dimensions are given in inches

Dimensions:

	Dimensions			Remarks
	Min	Typ	Max	
Line Width	0.008		0.016	Conductor for Logic Line
Non-Common	0.008			pad-to-pad
Conductor Clearance	0.004			all other conductors

Thickness of finished copper plating is 0.0028 ±0.0007 inch on each side of the PWB.

LAYOUT RULES FOR TTL PWA DESIGN

The following are some recommended practices in the design of PWA's using TTL components.

Supplies and Filtering

Ground is distributed by a conductor at least 1/2" wide forming a loop around the board connected to the backplane ground through pins P1B11, P1A29, P2A3 and P1B21.

The main logic voltage (V_{CC}) and ground at points inside this loop is distributed by conductors at least 0.125" wide, running as parallel pairs with 1/64" separation. The area covered by all the V_{CC} and ground conductors shall be at least 50% of the total board area.

A rectangular grid is formed by fully interconnected vertical and horizontal conductors at least 1/16" wide. These make maximum use of the dc distribution conductors and of the space available for ground plane fill-in. The filled-in copper areas must always be connected to the ground grid. The conductors forming the ground grid should be no more than 4" apart for the 74 series, 3" for the 74H series and 2.4" for the 74S series, if at least one element of the corresponding series is inside the rectangle defined by the conductors.

In every group of 10 packages or fewer, space shall be provided for a ceramic disc bypass capacitor 0.5" in diameter, 0.16" thick, and with 0.1" lead spacing. CDC part number 89636200 is recommended.

The dc supply current loop from each package to its nearest bypass capacitor shall use conductors at least 1/16" wide, and be of minimum area. This shall be accomplished as follows:

- As much of the loop as possible, but no more than 2", shall be formed by the 1/8" dc distribution pair, as measured from the capacitor to the point where V_{CC} or Gnd (whichever is closer to the capacitor) takes off for the device lead.

- The sum of the length of conductors in the remainder of the loop shall be no more than 2". Any longer conductors shall be routed under the device if possible.

A solid tantalum bypass capacitor shall be located as close as possible to the point where V_{CC} enters the card. If V_{CC} or other voltages enter in more than one place, each entry shall be bypassed.

The space provided on the board shall accept a capacitor 0.21" in diameter and 0.51" in length. CDC part number 89636318 is recommended.

Unused Elements

No input of any TTL element must be left floating, if the element is used. No element must be left floating, if not used.

Inputs which are permanently grounded must be so indicated on the circuit diagram by a ground symbol.

Inputs which are permanently connected to high logic voltage must be so indicated on the circuit diagram. These inputs are connected in one of the following ways (the choice may be left to the layout technician):

- up to 25 input loads may be connected to V_{CC} through one 1K resistor.
- up to 10 input loads may be connected to a nearby unused gate of similar fan-in, biased for high output.

Inputs to be connected directly to V_{cc} must be so indicated on the circuit diagram by the symbol "V_{cc}"

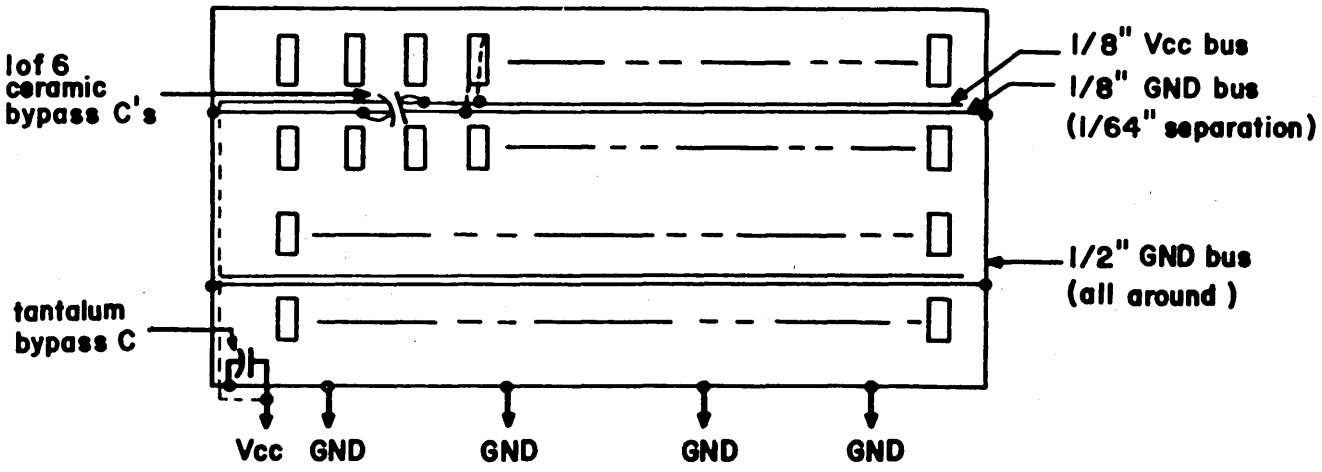
WARNING

Inputs to a multiple emitter element must not be connected directly to V_{cc}.

Layout Procedure

The following procedure is recommended for laying out cards.

Place the packages in an array as shown:



Each package connects directly to the V_{cc} and ground bus at the nearest point, with short conductors 1/16" wide.

Arrange the packages to minimize the conductors required on the component side.

Ground System

After laying out all conductors, cover all unoccupied areas on the component side with conductors connected to the dc ground supply bus. This serves as a skeletal groundplane.

Verify that each ground area is connected to the ground bus by at least one path and as many additional paths as possible. Add ground conductors on the copper side, at least every three inches, to complete the ground grid.

Printed Wiring Patterns

Fibure B-3 illustrates good (and poor) practice in patterning printed wiring pads for solder areas.

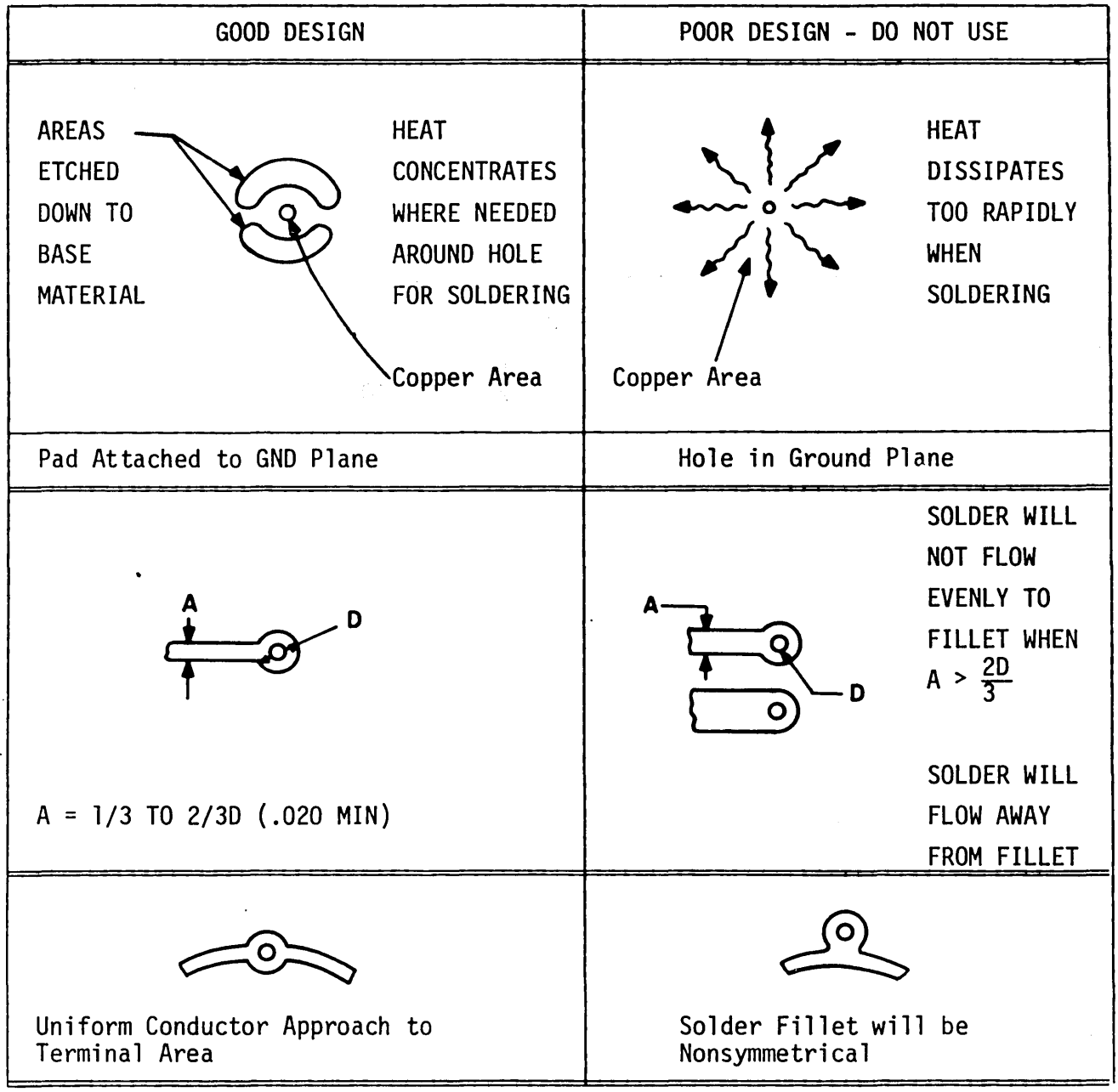


Figure B-3. Etched Circuit Patterns for Solder Areas

When using 1.5 mm circle and 1/16" conductor for connections, the configuration of Figure B-4 is recommended.

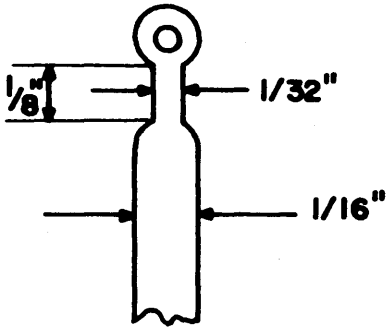


Figure B-4. Recommended Ground and Logic Voltage Connection

ELECTRICAL

Terminations

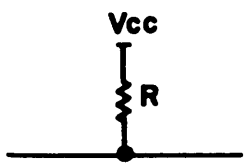
High speed signal lines may be terminated in either of the two ways shown in Figure B-5. The terminating impedance (R) is determined as follows (quantities referenced are defined in the tables below):

- the value of the terminating resistance should exceed Z_L by 20% to 50% ($1.2\ Z_L < R < 1.5\ Z_L$)
- the total load (added low state load plus load already present) must not exceed the low state drive factor

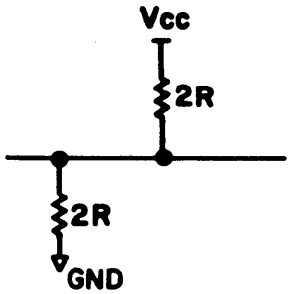
Example: a 74H00 gate drives a line with two 3" brances and 15" end-to-end length, all on the PWB. This adds up to 21" total, which exceeds the 15" limit. Two terminating resistors 390 ohm, one to V_{cc} and one to ground, provide a termination of R = 195 ohm. This is suitable for 50% ground place coverage. Added low state loading is

$$\frac{1.3}{0.195} = 6.7$$

When subtracted from the drive factor for the 74H series gates (12-5) this gives 5.8, which permits four 74H gate loads to be driven by the line.



a. Single resistor



b. Two resistors

Figure B-5. Signal Line Terminations

LOW STATE LOAD

Termination	Low State Load (Kilohm)
Single resistor	2.9 R
Two resistors	1.3 R

NOMINAL IMPEDANCE

% Groundplane	Nominal Z_L
0	280
25	190
50	160
75	130
100	110

DRIVE FACTOR (LOW STATE)

Driving Gate	Drive Factor
74XX	10.0
7440	30.0
74HXX	12.5
74H40	37.5
74SXX	10.0

COMMENT SHEET

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