B 9489
FLEXIBLE DISK DRIVE

TECHNICAL MANUAL

Burroughs

FIELD ENGINEERING

F.E. Dist. Code BD

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December 1979

For Library Binder 424

Form 2102141–001

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This Publication Change Notice provides additional information regarding the Preventive Maintenance Guide.

Remove the following pages :	Add the following pages :
iii & iv	iii & iv
5–1 & 5–2	5–1 & 5 –2

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Remove the following:	Insert the following:
Title	Title
A Page	ii
v thru vi	iii thru viii
4–1 thru 4–2	4–1 thru 4–10

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LIST OF EFFECTIVE PAGES

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3–1 thru 3–9	Original
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SECTION 1

INTRODUCTION AND OPERATION

GENERAL DESCRIPTION

The A/B 9489 Flexible Disk Drive provides a storage capacity of 1 megabyte per disk. The disks are removable, allowing unlimited off-line storage and easy transportation of data between sites.

The disks are made from flexible mylar and are coated with iron oxide on both sides. A protective envelope shields the disk from contamination. Data is recorded on both sides of the disk by two heads, one for each side. The heads are mounted on a carriage that is movable, so that the heads are positioned to one of the 88 concentric tracks on the disk. Movement of the carriage is controlled by a stepper motor connected to a lead screw.

Writing or reading is accomplished with the head that is in contact with the disk. To ensure contact, a pressure pad presses the disk against the head from the opposite side of the disk. In order to reduce wear, the pressure pads are retracted if the unit is not in use. Only one pressure pad can be active at any time.

Each disk has 2 recording sides with 88 tracks on each side. Each track contains 32 sectors with 180 bytes of information in each sector.

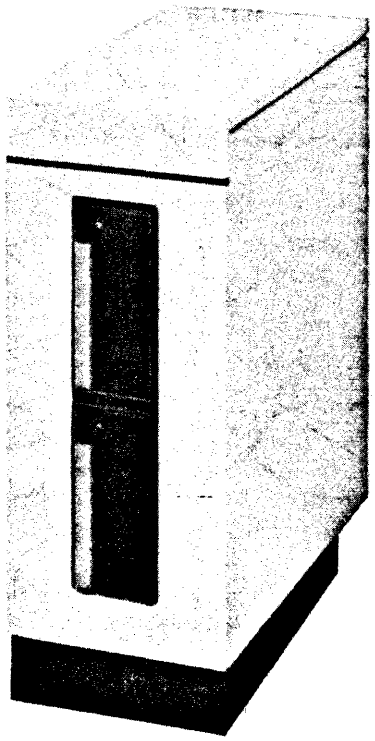


Figure 1–1. Complete unit

CONFIGURATIONS

Two units of the Flexible Disk Drive are available:

Master Unit (A/B 9489–1)
Slave Unit (A/B 9489–2)

The master unit is connected to the system controller (IO Control, Device Dependent Port) and contains additional electronics common to both units. The slave unit, if required, cannot function alone and connects to the master unit. The slave unit obtains DC power from the master unit.

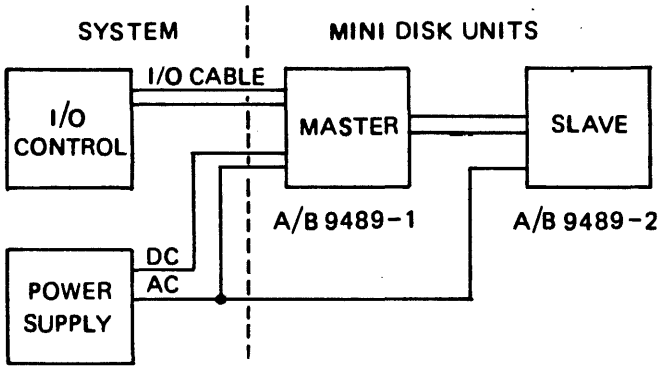


Figure 1–2. Master/Slave Configuration

APPLICATIONS

Each sector of the disk (180 bytes) has a unique address consisting of a side track and sector number. Any sector can be accessed by moving the head to the correct track and then waiting until the correct sector arrives under the head. This enables any sector to be accessed independently and is known as RANDOM ACCESS. Random access permits selective reading or writing of records within a file without having to read or write the entire file (as is the case with magnetic tape).

Random access makes the unit ideal for memory expansion of small computer systems where programs and software need to be read into memory at frequent intervals. In such a system the master disk would be used to contain system software and program and the slave would be used to record users files such as inventory, payroll, and accounting information.

In this application, the systems disk is a semi-permanent fixture while the user selects the second disk according to the programs required to run. Other uses are as follows:

Software/program transportation.
Collection of diagnostic information.
Data collection.

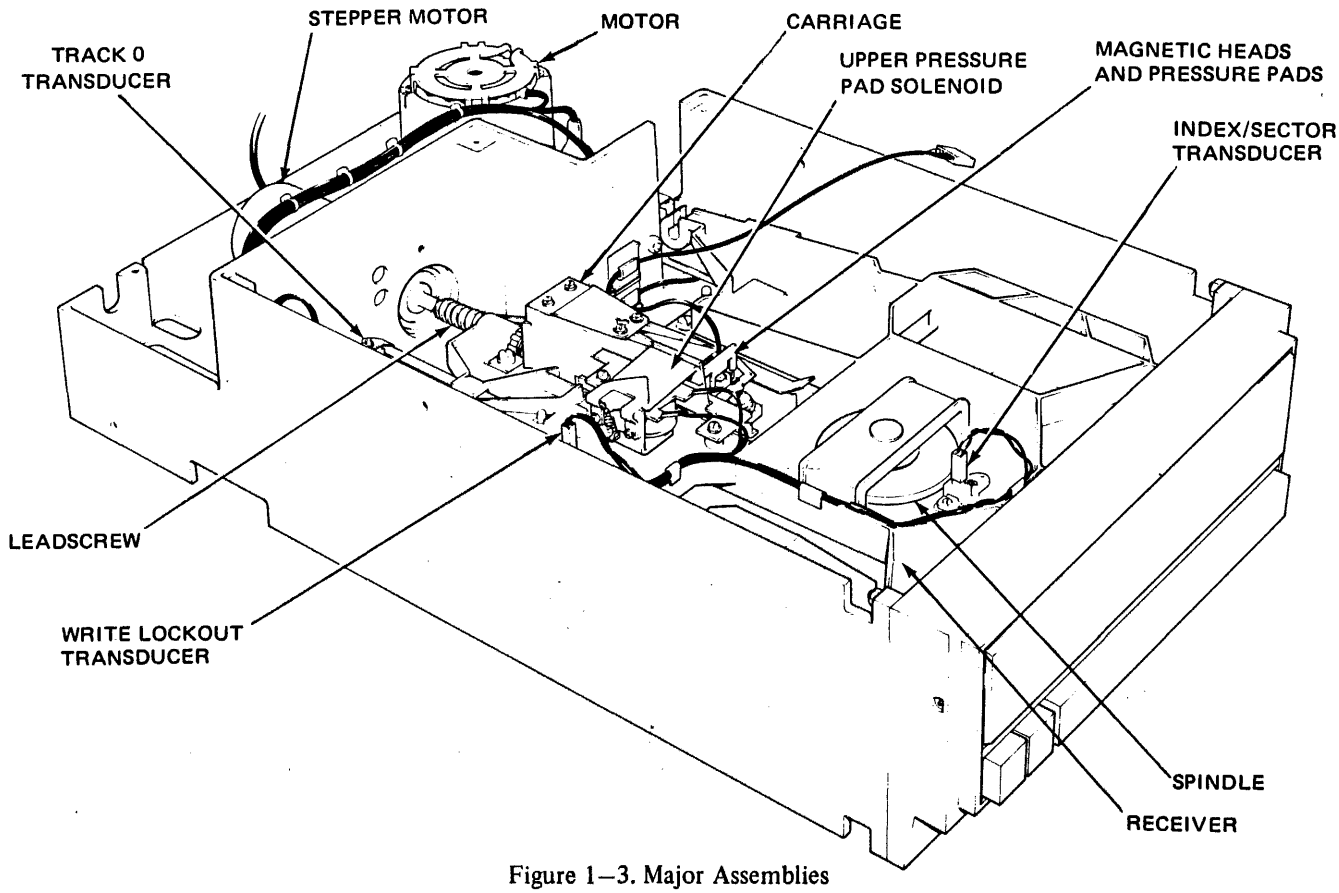


Figure 1–3. Major Assemblies

MAJOR ASSEMBLIES (Refer to figure 1–3).

MOTOR AND SPINDLE

The ac motor (115Vac) drives the spindle at 370 rpm via a pulley and self tensioning belt. The purpose of the spindle is to rotate the disk and it is cone shaped to center the disk as the disk is engaged with the spindle. Conversion from 50Hz to 60Hz is achieved by reversing the pulley on the motor shaft.

RECEIVER

The receiver accepts and holds the disk in the unit. It has two positions, up when the door is open, and down when the door is closed. When the door is open and the receiver is up, disks may be inserted or extracted. When the door is closed and the receiver down, the disk is not accessable to the operator and is in use by the unit.

The receiver operates as follows:

1. Accepts the disk when it is inserted.
2. Lowers the disk when the door is closed.
3. Engages the disk with the spindle by means of the annulus.
4. The index/sector transducer provides timing pulses for use of the controller.
5. The write inhibit transducer detects disks which are write protected.
6. Provides a mounting for the upper pressure pad solenoid.
7. Switches the motor ON when the receiver lowers and OFF when the receiver lifts.
8. Lifts the upper head clear of the disk when in the up position to enable easy insertion and extraction of the disk.

STEPPER MOTOR AND LEADSCREW

The purpose of the stepper motor and lead screw is to move the carriage to the required track. The stepper motor is three phase (3 windings) with 15 degrees per step. If the windings are energised in the correct sequence the motor will step in one direction and if the sequence is reversed, the motor will step in the other direction. The lead screw is an integral part of the motor and is a "Three Start Leadscrew". Each step of the motor corresponds to a 1/64 inch movement of the carriage.

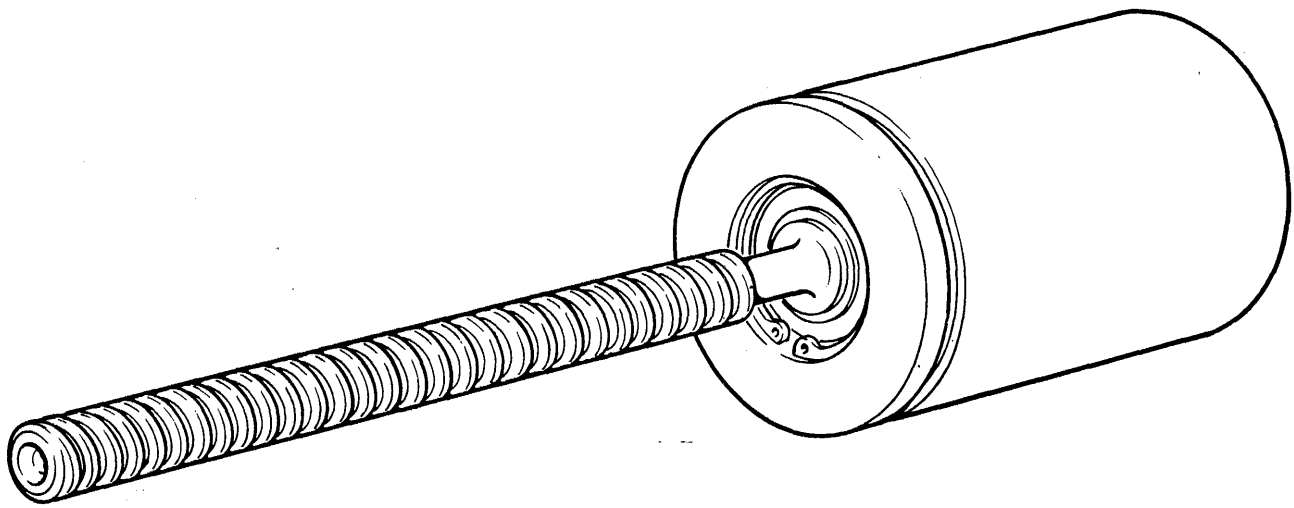


Figure 1–4. Stepper Motor and Leadscrew

CARRIAGE

The purpose of the carriage is to hold the heads in the correct position. The carriage is threaded on the lead screw so that as the lead screw rotates, the carriage moves towards, or away from, the spindle. An alignment rod prevents rotation of the carriage with the lead screw.

The backlash nut ensures that all play between the leadscrew and carriage is taken up in the direction of the spindle.

The vane interrupts the track 00 transducer when the carriage is situated at track 00. This is used to calibrate the electronics when a disk is first inserted and each time track 00 is accessed.

The lower magnetic head is bonded to the body of the carriage. The upper magnetic head is bonded to an arm which can move vertically. This arm is lifted when the receiver is raised to allow the disk to pass between the heads. When the receiver is lowered, the arm is returned to its position by spring tension.

PRESSURE PADS

The magnetic head pressure pads are mounted on the carriage and press the disk against the head to ensure good contact. A force of 11 grams is provided by the torsion springs. The pressure pads are only active when their respective solenoids are selected. Only one solenoid can be picked at any time. (A function of the electronics). When a head is selected, the pressure pad solenoid on the opposite side of the disk is energised, allowing the pressure pad to push the disk against the selected head. 5 revolutions after the read or write operation the pressure pad is disengaged if no further commands are received. This reduces disk and head wear.

MAGNETIC HEADS

The magnetic heads contain 2 windings, one for writing and reading and one for erase. Writing is achieved by passing current through the write/read winding. When current passes through the winding, a magnetic flux flows in the core. In the area of the gap the region of least reluctance to the magnetic flux is through the disk. Flux passing through the disk magnetises it permanently, completely saturating it. (refer to figure 1–6). By reversing the current in the winding, the direction of magnetisation is reversed. A change in direction of magnetisation is known as a "flux reversal."

By writing flux reversals in a specific pattern, data can be recorded.

RECORDING MODE (Refer to the paragraph)

During read, the flux reversals passing under the head flow through the core and induce a current in the winding. The induced current is amplified and decoded into the original data. Read is non-destructive and the data can be read repeatedly.

The purpose of the erase winding is to magnetise a band on each side of the data. This erases any flux left from previous writing operations and provides a "guard band". If old data was allowed in this position a slight misposition of the head would pick up both sets of data and result in errors.

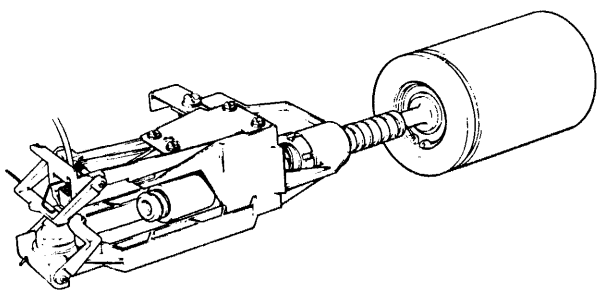


Figure 1–5. Carriage Assembly

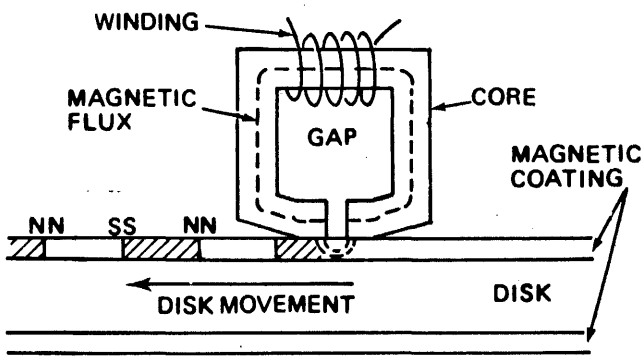


Figure 1–6. Diagrammatic Recording Head

Refer to figure 1–7 The recorded data is approximately 0.0104 inch wide with a guard band of 0.0052 inch on each side. This type of head is known as a single gap, tunnel erase head.

The cores are mounted in a ceramic shoe for long life. Figure 1–8 is an electrical schematic of the magnetic head.

PRINTED CIRCUIT BOARD

The master printed circuit board contains the following:

1. Interface electronics
2. Positioner electronics
3. Index/Sector pulses
4. Write encoding
5. Write amplifier
6. Read amplifier
7. Read decoding
8. Write lockout

The slave printed circuit board contains the following:

1. Positioner electronics
2. Write amplifier
3. Write lockout
4. Read amplifier
5. Index/Sector pulses

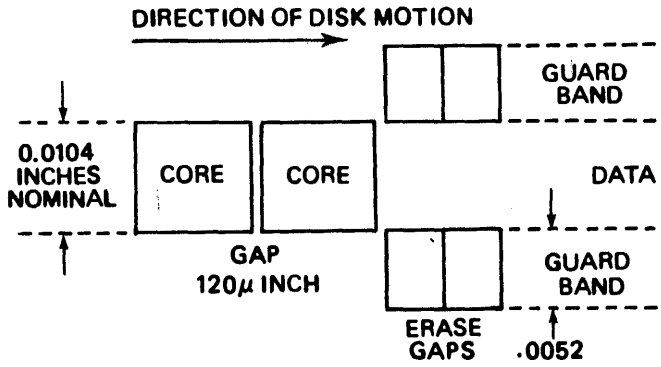


Figure 1–7. Magnetic Head Layout

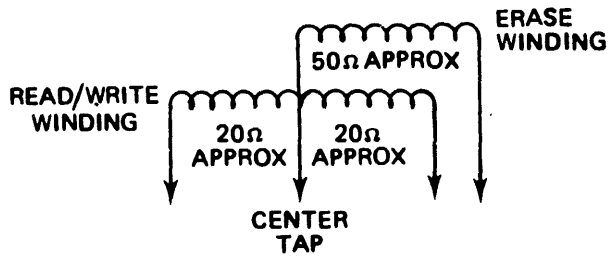


Figure 1–8. Head Schematic

OPERATION

FLEXIBLE DISK (MINI-DISK)

Data is recorded on the flexible disk on 88 concentric tracks. The lower magnetic head is offset relative to the upper magnetic head in order to make space for the pressure pads and the distance of the tracks from the center of the disk is different on the upper and lower surface. (refer to figures 1–9 and 1–10).

The two tracks in line with the heads at any one time (one on the upper surface and one on the lower) is known as a CYLINDER.

Sector Configuration

Each track contains 32 sectors with 180 bytes of data per sector. The sectors are marked by holes on the disk (refer to figure 1–9).. A transducer detects these holes as the disk rotates and applies pulses to the controller. The sectors are numbered 0 to 31 and sector 0 is marked by an index hole immediately preceding the sector mark. The index hole is located midway between the sector 31 and sector 0 holes.

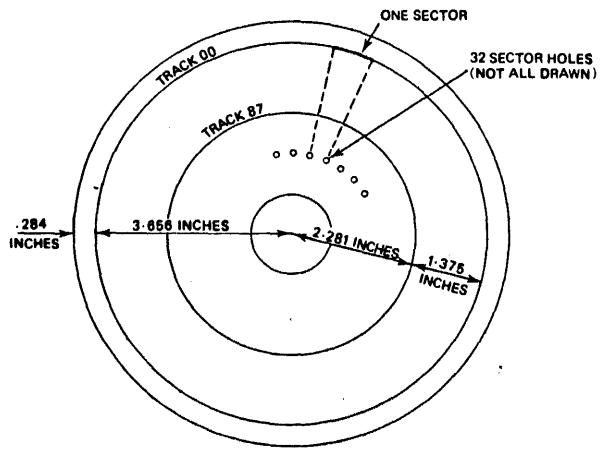


Figure 1–9. Track Format (Upper Side)

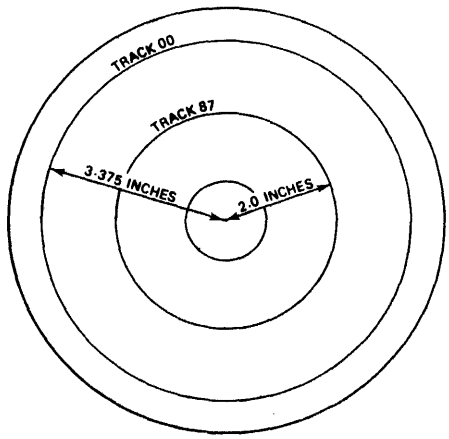


Figure 1–10. Track Format (Lower Side)

Data configuration

The data within one sector consists of the following: (refer to figure 1–11).

1. Preamble (32 bytes of zeros)
2. Sync byte (2 bytes)
3. Address (2 bytes)
4. Data (180 bytes)
5. Parity byte (1 byte)
6. Postamble (remainder of sector, bytes of zeros)

Recording Mode

The recording mode used is Miller Frequency Mode (M.F.M.) A comparison of the various recording modes is illustrated in figure 1–12. M.F.M. is a self clocking mode (that is, it does not require a separate clock track) and it enables approximately twice as much data to be stored for the same flux-change density.

M.F.M. consists of a flux-change at the edge of a data cell for a zero and a flux change in the centre of a cell for a one. If a zero follows a one, a fluxchange is not recorded. This is recognised and corrected during read and the fluxchange density is minimised.

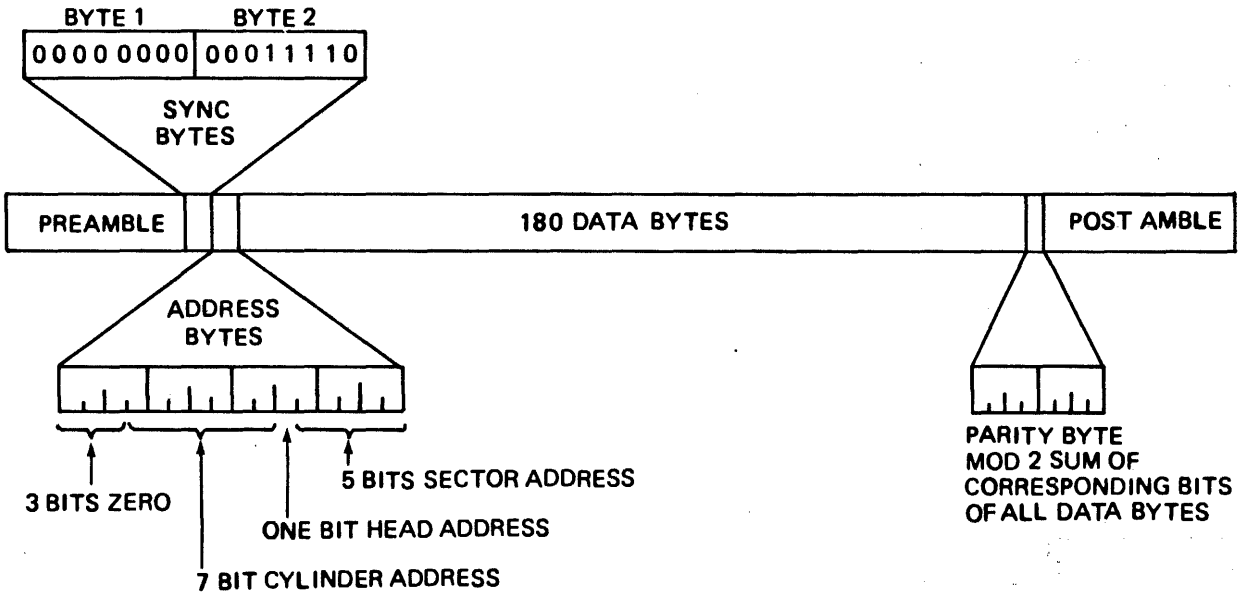


Figure 1–11. Sector Configuration

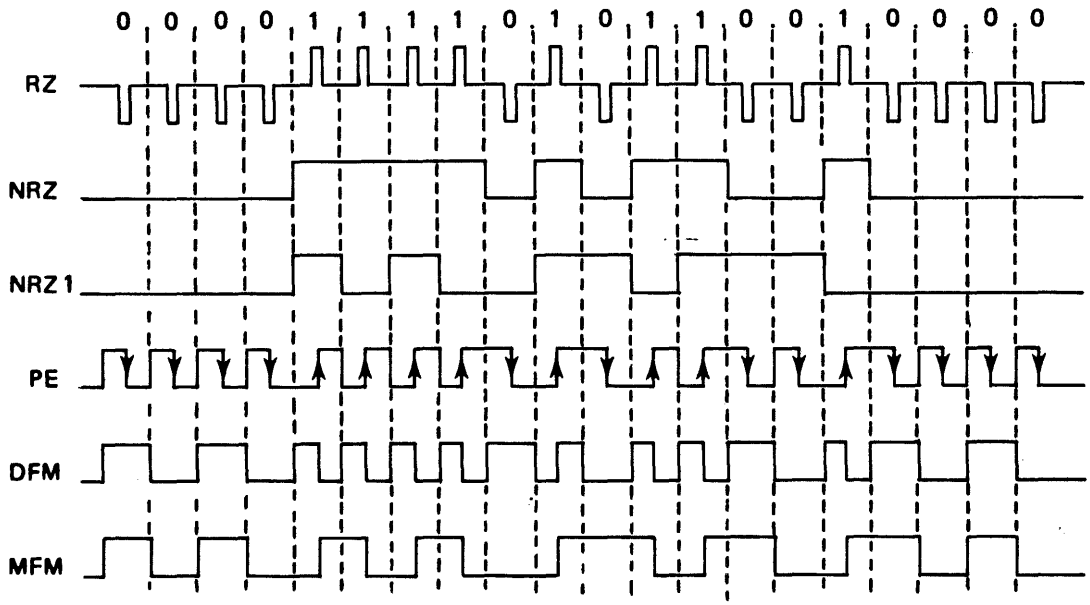


Figure 1–12. Encoding Comparison

FUNCTIONS

Seek

The Seek function is the command from the controller to the unit to move the heads to a new track. The seek function sequence is as follows:

1. A new track address is applied to units.
2. A seek pulse is applied from the controller to the master or slave.
3. The carriage moves to a new track and settles.
4. The POSITION SETTLE signal is applied to the controller.

POSITION SETTLE is the signal that a write or read operation may begin. Overlapping seek is permitted and consists of performing a seek on one unit while a seek is in progress on the other unit.

Write

A write is initiated from the controller by making WRITE ENABLE true. If the Write lockout hole on the disk jacket is covered, the WRITE ENABLE signal enables the write and erase drivers on the selected drive.

NRZ data (WRITE DATA) is supplied to the drive in synchronisation with the DATA CLOCK which is generated in the disk drive.

The NRZ data is converted to M.F.M. in the common electronics (see figure 1–16).

The MFM data is then transferred to the selected unit where it controls the direction of current flowing through the head.

The erase coils are also energised to provide a "guard band" of erased disk on either side of the data written.

The formatting of the data into preamble, address data, parity bits etc. is a function of the controller.

Read

As the disk passes over the selected head, the flux reversals induce an alternating current into the coil of the head. This is amplified, filtered for noise and digitised.

The digitised read information from the selected unit is applied to the common electronics portion of the PCB. On receiving READ ENABLE from the controller an oscillator locks onto the data providing a data sampling window and a READ CLOCK. The purpose of this oscillator (phase locked loop) is to enable translation from MFM to NRZ.

The READ DATA is then applied to the host, synchronised with READ CLOCK.

The read operation ends when READ ENABLE from the controller goes false. READ ENABLE is made true shortly after a sector pulse so that the Phase Locked Loop can lock in on the preamble prior to the address and data. READ ENABLE is made false at the end of the sector.

PHYSICAL AND ELECTRICAL CHARACTERISTICS

Physical

Length	17.25 inch	(43.8 cm)
Width	10 inch	(25.4 cm)
Height	5.62 inch	(14.3 cm)
Weight	20 lbs.	(9.07 kg)
Shipping weight	23 lbs.	(10.43 kg)

Electrical

AC Power	120V $^{+\ 6\%}_{-\ 10\%}$	
	50–60Hz	0.3 A per unit
DC Power	+ 5V ± 10%	2.0 A per master unit
		1.8 A per slave unit
	+ 12V ± 10%	0.3 A per unit
	− 12V ± 10%	0.3 A per unit
	+ 24V ± 10%	2.25A per unit
Heat dissipation	75W	

RECORDING CHARACTERISTICS

Format

Number of cylinders per disk.	88
Number of sides per disk	2
Number of tracks per disk	176
Sectors per track	32
Sectors per cylinder	64
Sectors per disk	5,632
Data bytes per Sector	180
Data bytes per Surface	506,880
Data bytes per disk.	1,013,760
Tracks per inch	64
Bit density (Bits per inch)	4,774 max.
Recording mode	M.F.M.

Data access

Disk rotation speed	370 rpm
Average latency	80 ms
Track to track	47 ms
Maximum access time	516 ms
Data transfer rate	375 K bits/second

FLEXIBLE DISK

The flexible disks are made from Mylar, or a similar material, 0.003 inch thick. The disk is coated with a 110 microinch thick layer of iron oxide/polymer. Figure 1–13 illustrates the dimensions of the disk.

Jacket

Figure 1–14 illustrates the dimensions of the disk jacket. The inside of the jacket is covered with cleaning tissue to keep the disk clean.

Disk Handling

The disk should be used under the following environmental conditions:

Temperature: 50°F to 125°F (10°C to 51.6°C)

Humidity: 8% to 80%

The disk should be stored under the following conditions:

Temperature: 30°F to 125°F (−1°C to 51.6°C)

Humidity: 5% to 90% No moisture to be present on the disk.

The following procedures and precautions should always be observed in order to avoid damaging the disk.

1. Always put the disk back in the envelope when out of the drive.
2. Always keep the disk in the envelope in the ten pack box.
3. Always return the empty envelope to the ten pack box.
4. Treat the disk as fragile and easily damaged.
5. Use a felt tip pen to write on the disk label (a pencil or ball point pen will damage the disk).
6. DO NOT touch the magnetically coated (brown) surfaces.
7. DO NOT leave the disk lying around on work surfaces.
8. DO NOT put objects, including papers, on top of the disk.
9. DO NOT expose the disk to temperatures above 125°F (51.6°C).
10. DO NOT allow the disk to become contaminated by tea, coffee, cigarette ash or similar contamination.
11. DO NOT put a contaminated disk into a drive.
12. DO NOT attempt to load a disk into a drive that is switched off. Damage to the center hole may result.
13. DO NOT expose a disk to magnetic fields in excess of 50 oersteds. Always remember that tools can become magnetised.
14. DO NOT fit labels other than those supplied in the ten pack box.
15. DO NOT handle the center hole of the disk.

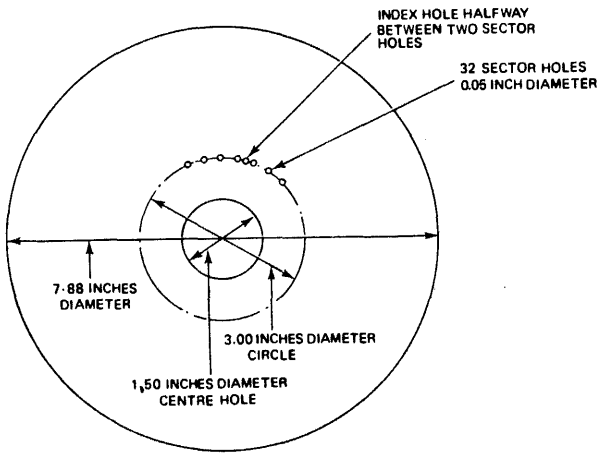


Figure 1–13. Disk

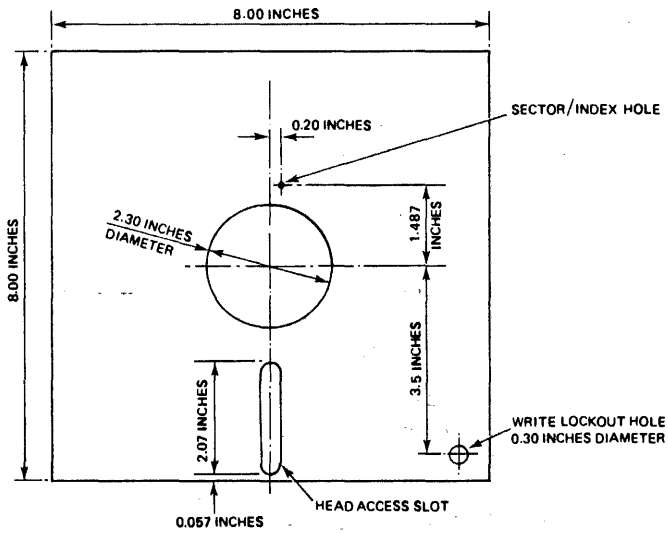


Figure 1–14. Jacket

OPERATING PROCEDURES

Indicators and Control (refer to figure 1–15)

Door Release Bar

Depressing the release bar unlatches the door and receiver for disk insertion. Closing the door securely automatically latches it shut.

Write Enable Indicator

When the Write Enable (red) indicator is illuminated it indicates that the disk in the unit can be written on and that old data will be destroyed. When the red indicator is out it indicates that the disk cannot be written on and data is protected.

File Operational Indicator (File Op.)

When the File Op (blue) indicator is illuminated it indicates that a disk is inserted, up to speed and is in an operational state.

Disk Insertion

1. Ensure that the power is ON.
2. Press blue Door Release Bar to open the door.
3. Remove disk from envelope.
4. Insert the disk into the drive, head access slot first, with the label away from the release bar (see figure 1–14 and 1–15).
5. When the disk is correctly inserted close the door. When the blue File Op indicator is illuminated the unit is ready.

NOTE:
If the disk is inserted the wrong way, the File Op. indicator will not illuminate.

Disk Extraction

1. Wait until the system has completed processing with the disk.
2. Press Door Release Bar on the unit.
3. Extract the disk.
4. Immediately return the disk to its envelope.
5. Close the door of unit.

ELECTRICAL INTERCONNECTIONS

HOST TO MASTER INTERFACE

Table 1–1 contains the logic interface signals between the host system and the master drive. Each signal line is formed into a twisted pair with its ground return.

CABINET SELECT/ – is used to select one of the two drive cabinets. When CABINET SELECT/ is set to logic 1 cabinet 0 is selected. When CABINET SELECT/ is set to logic 0 cabinet 1 is selected.

Table 1–1. Logic Interface Between Host System And Master Drive

SIGNAL PIN	GROUND PIN		
42	32	Cabinet Select/	From Host System
47	30	Unit Select/	
11	12	Head Select/	
15	31	Address–1/	
17	16	Address–2/	
50	33	Address–4/	
49	48	Address–8/	
13	14	Address–16/	
6	25	Address–32/	
7	8	Address–64/	
43	26	Seek/	
46	29	Write Enable/	
44	27	Write Data/	
45	28	Read Enable/	From Disk Drive
4	5	Read Data/	
40	23	File Operational/	
39	22	Positioner Settled/	
34	18	Write Inhibit/	
36	20	Index/	
35	19	Sector/	
37	21	Illegal Address/	
41	24	Seek Incomplete/	
2	3	Data Clock/	

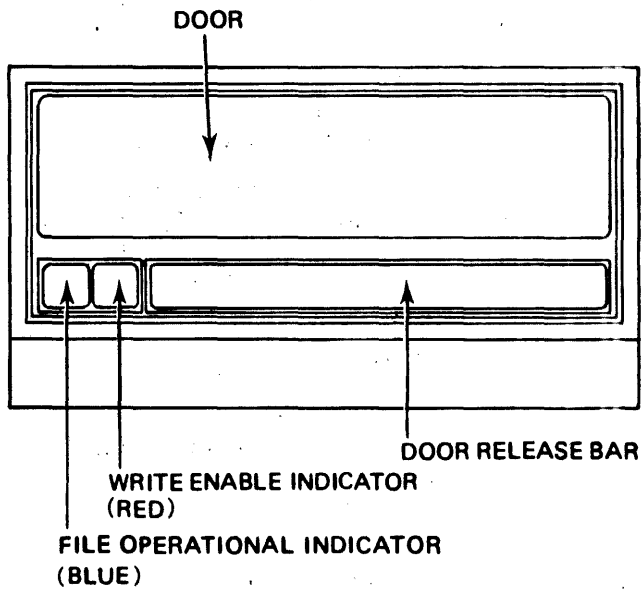


Figure 1–15. Operator Controls

UNIT SELECT/ – is used to select either the master drive or the slave drive. When UNIT SELECT/ is set to logic 1 the master drive is selected. When UNIT SELECT/ is set to logic 0 the slave drive is selected.

HEAD SELECT/ – is used to select one of the two heads. When HEAD SELECT/ is set to logic 1 side 0 of the disk is selected. When HEAD SELECT/ is set to logic 0 side 1 of the disk is selected.

ADDRESS–1/ through ADDRESS–64/ – select the cylinder address. The cylinder address is coded in binary. When ADDRESS–1/ is set to logic 0 and all the other ADDRESS signals are set to logic 1 cylinder 01 is addressed.

SEEK/ – is used to start a positioner movement to the address selected by ADDRESS–1/ through ADDRESS–64/. This signal also causes selection and mechanical loading of the head selected by HEAD SELECT/. The positioner movement and head selection are started by SEEK/ changing from logic 0 to logic 1.

WRITE ENABLE/ – is used to enable writing data onto the disk. When WRITE ENABLE/ is set to logic 0 data is written onto the disk.

WRITE DATA/ – is the data to be written onto the disk. When WRITE DATA/ is set to logic 1 a data 0 is written onto the disk. When WRITE DATA/ is set to logic 0 a data 1 is written onto the disk.

READ ENABLE/ – is used to enable reading data from the disk. When READ ENABLE/ is set to logic 0 data is read from the disk.

READ DATA/ – is the data being read from the disk. A data 0 bit from the disk will set READ DATA/ to logic 1. A data 1 bit from the disk will set READ DATA/ to logic 0.

FILE OPERATIONAL/ – is set to logic 0 if a disk is in the drive, the disk is rotating within 10% of full speed and the positioner has recalibrated to track 00. If FILE OPERATIONAL/ is set to logic 1 all signals from the drive are invalid.

POSITIONER SETTLED/ – is set to logic 1 when:

1. FILE OPERATIONAL/ is set to logic 1,
2. The positioner is in motion after a SEEK/ signal, or,
3. A head solenoid is in motion after a SEEK/ signal.

WRITE INHIBIT/ – is set to Logic 0 if the disk in the unit selected is write protected.

INDEX/ – signal pulses to logic 0 when the index hole on the disk is detected.

SECTOR/ – signal pulses to logic 0 when a sector hole on the disk is detected.

ILLEGAL ADDRESS/ – is set to logic 0 if the ADDRESS/ lines exceed decimal 87 when SEEK/ changes from logic 0 to logic 1.

SEEK INCOMPLETE/ – is not used and is always set to logic 1.

DATA CLOCK/ – is used to strobe the data on the WRITE DATA/ and READ DATA/ signal lines.

MASTER DC SUPPLIES

Table 1–2 contains the DC supplies to the master drive. Each supply line is formed into a twisted pair with its return. All DC returns are connected together on the master drive.

Table 1–2. DC Supplies To The Master Drive

PIN	LINE
1	+24V
2	+24V Return
3	±12V Return
4	–12V
5	+12V
6	+24V
7	+ 5V Return
8	+5V
9	–12V

MASTER DRIVE TO SLAVE DRIVE INTERFACE

All DC, ground and logic signals are transferred from master drive to slave drive on one 40-way cable.

Figure 1–16 shows the master drive to slave drive interface. READ DATA and WRITE DATA are both encoded in M.F.M.

LINE POWER AND GROUNDING

The host system must provide line power to both the master drive and the slave drive.

Pin

1. Not Connected
2. Not Connected
3. Line
4. Neutral

A ground stud is provided adjacent to the line connector.

CAUTION

ON EACH DRIVE THIS GROUND STUD MUST BE CONNECTED TO THE HOST SYSTEM.

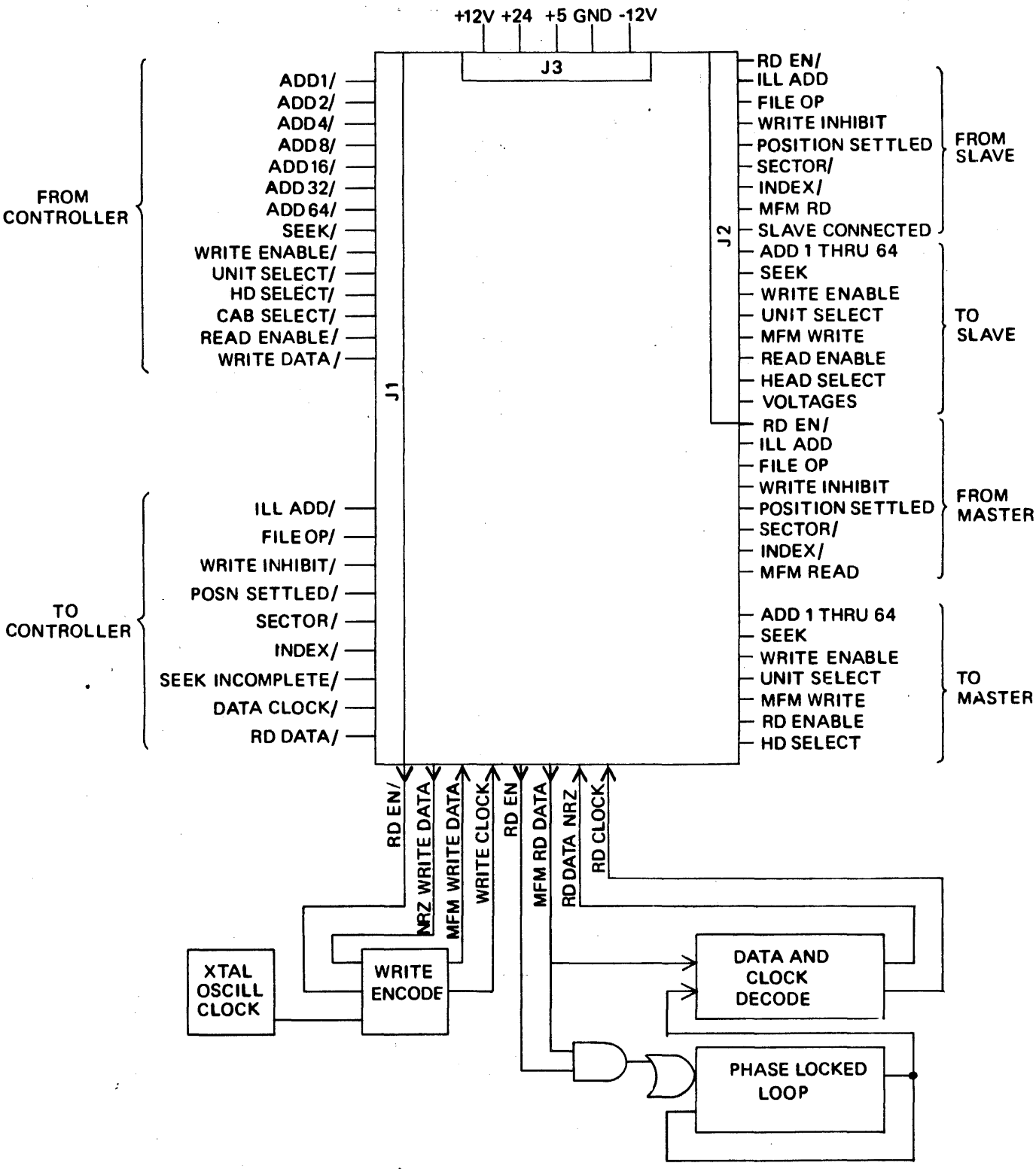


Figure 1–16. Common Electronics

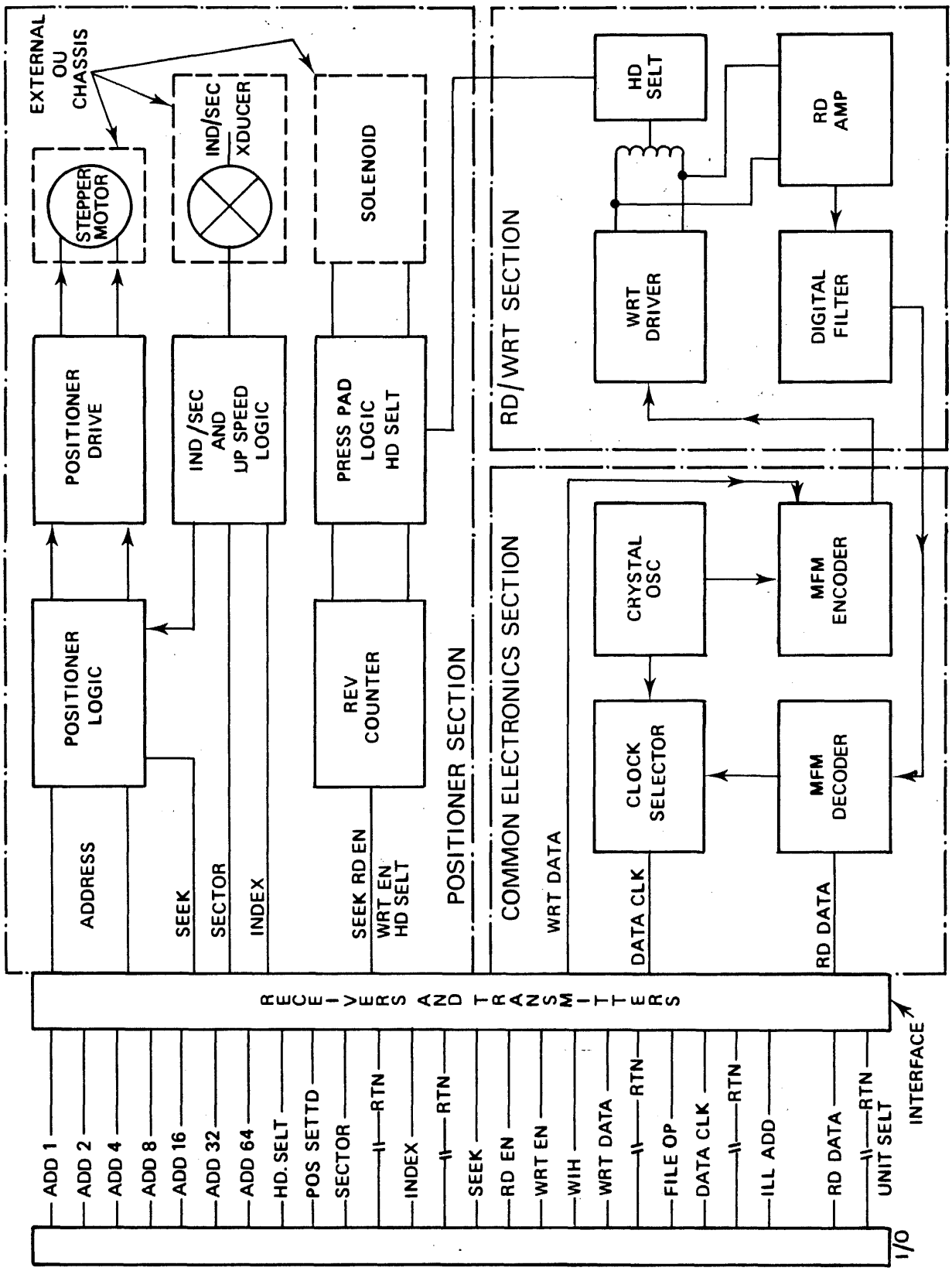


Figure 1 – 17. Block Diagram

SECTION 2
FUNCTIONAL DETAIL

POSITIONER

GENERAL DESCRIPTION

Positioning the leads to any of the 88 cylinders is achieved by a carriage mounted on a lead screw/stepper motor assembly. Rotation of the stepper motor one step moves the heads 1/64 inch along the radius of the disk onto the next track. Normally, a SEEK involves a number of steps in either direction.

There is no "Home Position" similar to other Disk Cartridge drives. The carriage is always at one of the 88 cylinder positions whether a disk is in the drive or not.

When a disk is inserted and up to speed, the carriage moves to track 00 and the electronics is calibrated with the positioner. This is achieved by use of the track 00 transducer and the vane attached to the carriage (see figure 2-1).

Whenever a new track is needed, the new address and a SEEK pulse is sent to the unit from the controller. The new address is compared with the present address and the stepper motor is driven forwards if the new address is higher and backwards if the address is lower. When the track requirement has been reached a delay is started which permits the carriage to settle. At the end of this delay, POSITION SETTLED is sent to the controller informing it that read/write operations can start.

MECHANICS

The carriage is threaded onto the lead screw and is entirely supported by the lead screw (see figure 2-1). The carriage is prevented from rotating with the lead screw by the alignment rod and the yoke in the lateral arm of the carriage. Play between the lead screw and the carriage is taken up towards the spindle by the backlash nut. The stepper motor/lead screw is mounted on an accurately machined surface of the base casting to make sure that the heads will always travel on a true radius.

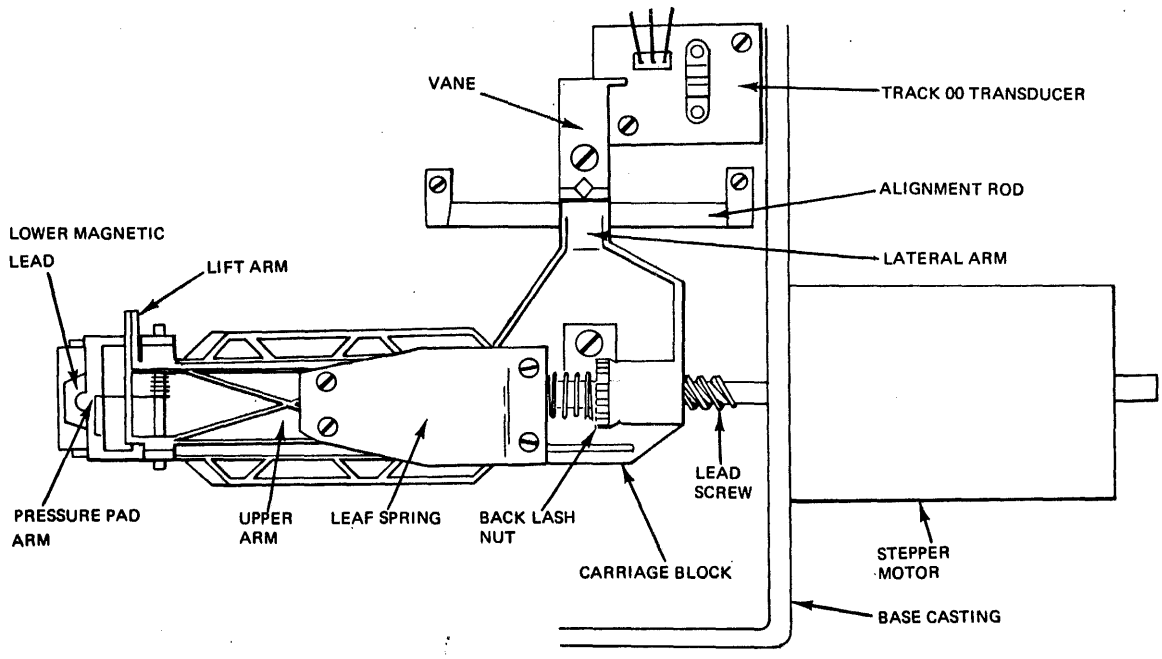


Figure 2-1. Positioner Mechanics. (top view)

Functional Detail

CARRIAGE

The carriage block contains the lower head which is fixed in position with adhesive. This is factory set in order to make sure that cores are parallel with the tangent of the track at the point of contact. The upper head is similarly set in the upper arm, but, for easy insertion of the disk the arm is mounted on a leaf spring. This permits the upper arm to be lifted by the receiver to give clearance for the disk to pass between the heads. The upper arm is held in position by a key on the under surface engaging a slot in the upper extension of the carriage block. The upper head can be adjusted in relation to the lower head along the disk radius. Both heads can be adjusted by turning the stepper motor on its mounting.

A vane fitted to the lateral arm is aligned with the track 00 transducer when the carriage is at track 00.

MAGNETIC HEADS

The magnetic heads are offset in relation to each other, with the lower head nearer the spindle than the upper head, to give the space needed for the pressure pads (see figure 2–2.) The pressure pads are on opposite sides of the disk from the heads and press the disk on to the heads.

ELECTRONICS

Refer to the block diagram figure 2-3.

The positioner electronics contains the sections which follow:

1. File Operational (File Op) – Gives an indication to the controller when the unit is ready for use.
2. Address Latches – Contains the new track address from the controller, gated in with SEEK.

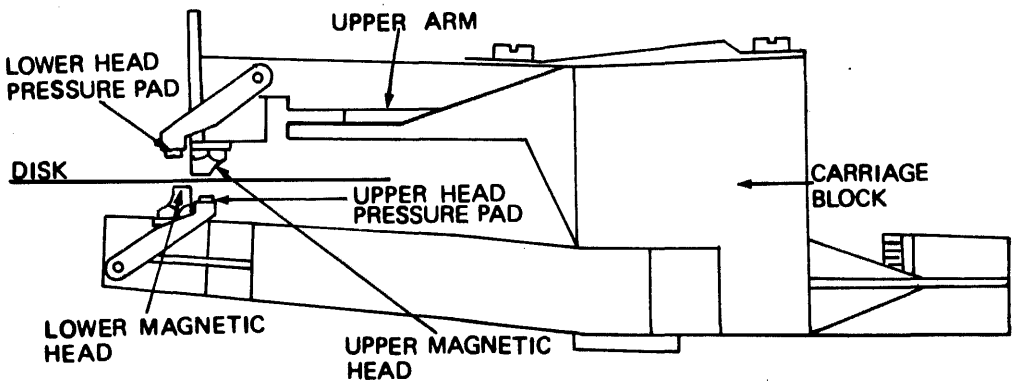


Figure 2-2. Carriage (side view)

3. Illegal Address – Gives an indication if the address latches contain an address greater than 87.
4. Current Address Counter – An 8-bit up/down counter that always contains the present track address of the carriage/heads.
5. Comparator – Compares new address with present address.
6. Stepper motor driver – Self explanatory.
7. Stepper motor register – Energizes the coils of the stepper motor, in sequence, via the stepper motor drivers.
8. Positioner Clock – Controls the step rate of the stepper motor.
9. Clock Control – Causes stepping to start and stop.
10. Direction Control – Determines whether the carriage will step forward or backward.
11. Position settle circuitry – Gives an indication to the controller when the heads have settled on the new track at the end of a SEEK.

FILE OP

The purpose of the File Op circuit, is to give information to the controller and the operator that the unit is ready for operation (refer to figure 2-4).

Initial conditions are:

1. There is no disk in the unit.
2. The carriage is away from track 00.

The track 00 transducer signal is low giving a high on IC25, pin 5. The up-to-speed (UTSF) signal is low providing a low on IC25, pin 1. This causes pin 3 to be high and pin 6 to be low holding the File Op latch reset. IC13 pin 6 is low giving a low File Op signal to the common electronics. The File Op indicator is not illuminated.

When the disk is inserted and the receiver is lowered, the disk turns and index/sector pulses are generated. When the correct disk speed is detected (see up-to-speed) UTSF goes high placing a high on IC25 pin 10. Pin 9 is high from ILL ADD/. The high on pin 9 causes IC24 pin 6 to go high to enable the positioner clock. Count Down is also enabled so that the carriage will step backwards. When track 00 is reached, IC25 pin 5 goes low setting the File Op flip-flop, to stop any further clock pulses and therefore carriage movement. The File Op lamp illuminates, the heads are on track 00 and, if the unit is selected, the FILE OP signal is applied to the controller via the multiplexor chip IC67 (figure 2–4).

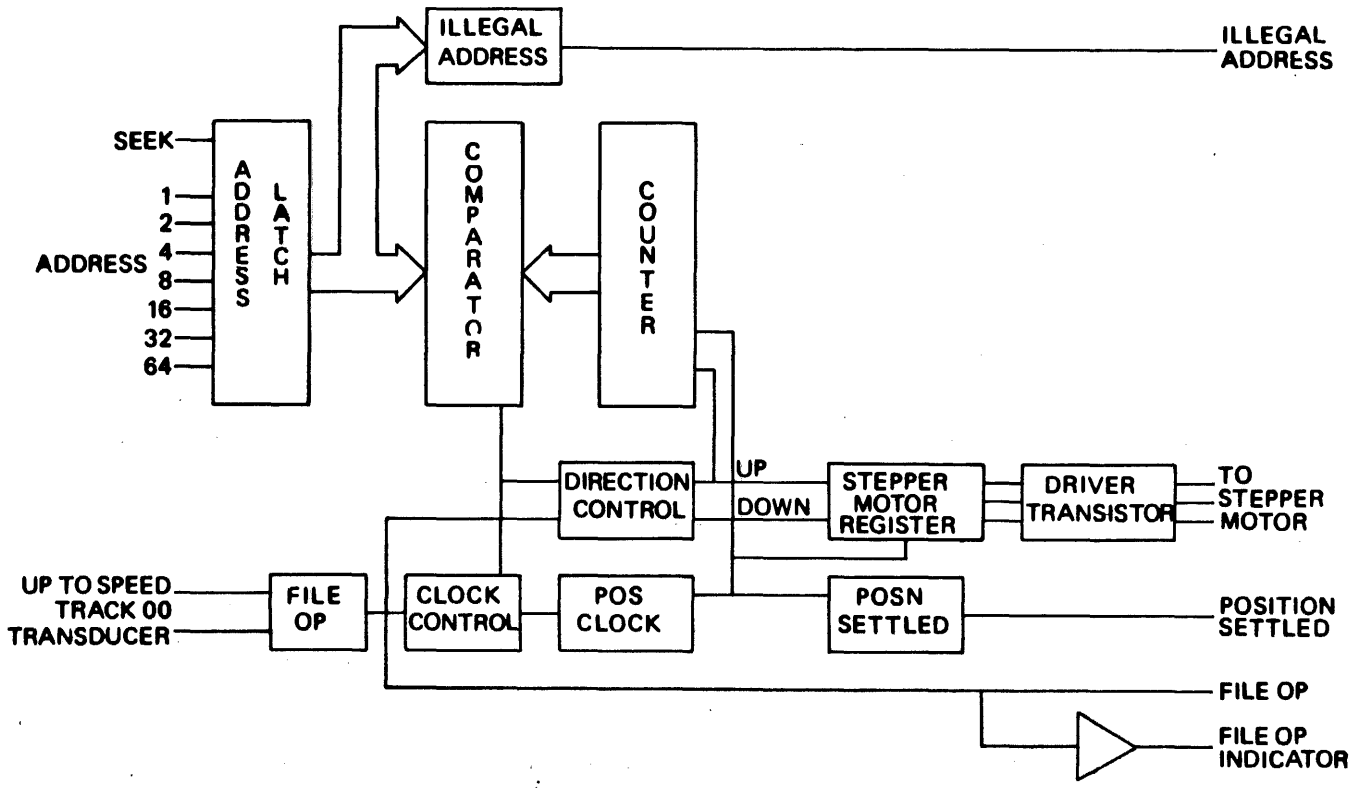


Figure 2–3. Positioner Electronics Block Diagram

Functional Detail

ADDRESS LATCHES

An overlapping seek is a seek initiated on a master or slave while a seek is in progress on the other. Each drive has an address latch to enable overlapping seeks to be performed. This consists of a dual 4 bit latch integrated circuit. The address lines are sent to both master and slave, but, the seek pulse is gated only to the unit selected. (Refer to figure 2-4).

The seek pulse is gated with WRT EN/and Unit Select to become a negative pulse on TP 8/2. The leading (negative) edge of the pulse gates the new address at the input of the address latches onto the output of the address latches.

When the disk is removed, UTSF goes low and causes a low on pins 1 and 13 of IC46 to reset the address latches.

ADDRESS 00 DETECTOR

When the address latches contain 00 (all outputs are low) IC36,41 and 26 decode a high at IC36 pin 4 and low at IC26 pin 3. This signal is used to force a recalibration of the carriage onto track 00.

ILLEGAL ADDRESS

The mini disk has 88 tracks, numbered 00 to 87. Any address received that is higher than 87 is "Illegal". If this occurs, the signal "ILLEGAL ADD" is returned to the controller and carriage movement is inhibited. IC28 pin 6 goes low for addresses between 88 and 95, and IC18 pin 11 goes low for addresses of 96 or higher. (Refer to figure 2-4).

The leading edge of the seek pulse clocks the new address into the address latch. If the address is illegal, IC16 pin 2 goes high and the trailing edge (positive) of the seek pulse clocks flip-flop IC16 to set illegal address flip-flop. This signal goes to the common electronics of the master unit where it is gated to the controller by UNIT SELECT through multiplexor IC16.

Carriage movement is inhibited by a low on IC26 pin 8, a high on IC25 pin 8 and a low on IC12 pin 13 which stops clock pulses from reaching the stepper motor register.

CURRENT ADDRESS COUNTER AND COMPARATOR

The purpose of the Current Address Counter is to give information to the address comparator of the cylinder that the heads are currently situated on. The counter steps up and down as the carriage steps towards or away from the spindle.

Calibration of the counter and carriage occurs when a disk is first inserted and subsequently whenever track 00 is seeked. This permits software recovery if the counter and carriage become mis-calibrated.

The counter consists of two hexadecimal up/down counters connected in series. When the Carry In (pin 2), Set (pin 12), Reset (pin 13) and Count Enable (pin 1) are high, the counter will count whenever the clock pulse goes low. The direction of count is controlled by the Up/Down signal. A high will cause the counter to count up and a low will cause it to count down. The Carry Out (pin 3) goes high at count 15 when counting up and count 0 when counting down. Since the carry out from the Least Significant Bits (LSB) counter is connected to the carry in of the MSB counter, IC29 counts 1 for every 16 clock pulses to continue the count.

The counter is reset (whenever the carriage vane cuts the track 00 transducer) by the following path: IC45 pin 12 high, pin 11 low, IC13 pin 4 high, IC11 pin 8 low, IC29 pin 13 and IC30 pin 13 low. Counting is enabled when File Op goes high.

The purpose of the address comparator is to compare the contents of the address latch with the current address counter. The comparator has three output signals:

1. A > B. This signal occurs when the new address is higher than the current address and the carriage movement must be toward the spindle.

2. A < B. This signal occurs when the new address is lower than the current address and the carriage movement must be away from the spindle.

3. A=B. This signal occurs at the end of a seek when the carriage has moved to the new track position and the current address counter has counted up or down with each step until it is equal to the address latches.

The comparator consists of two 5-bit comparators connected in series. Comparison is enabled when the File Op flip-flop sets and pins 1 of IC37 and 38 go low. Before comparison is enabled. A > B, A < B and A = B are all low.

Functional Detail

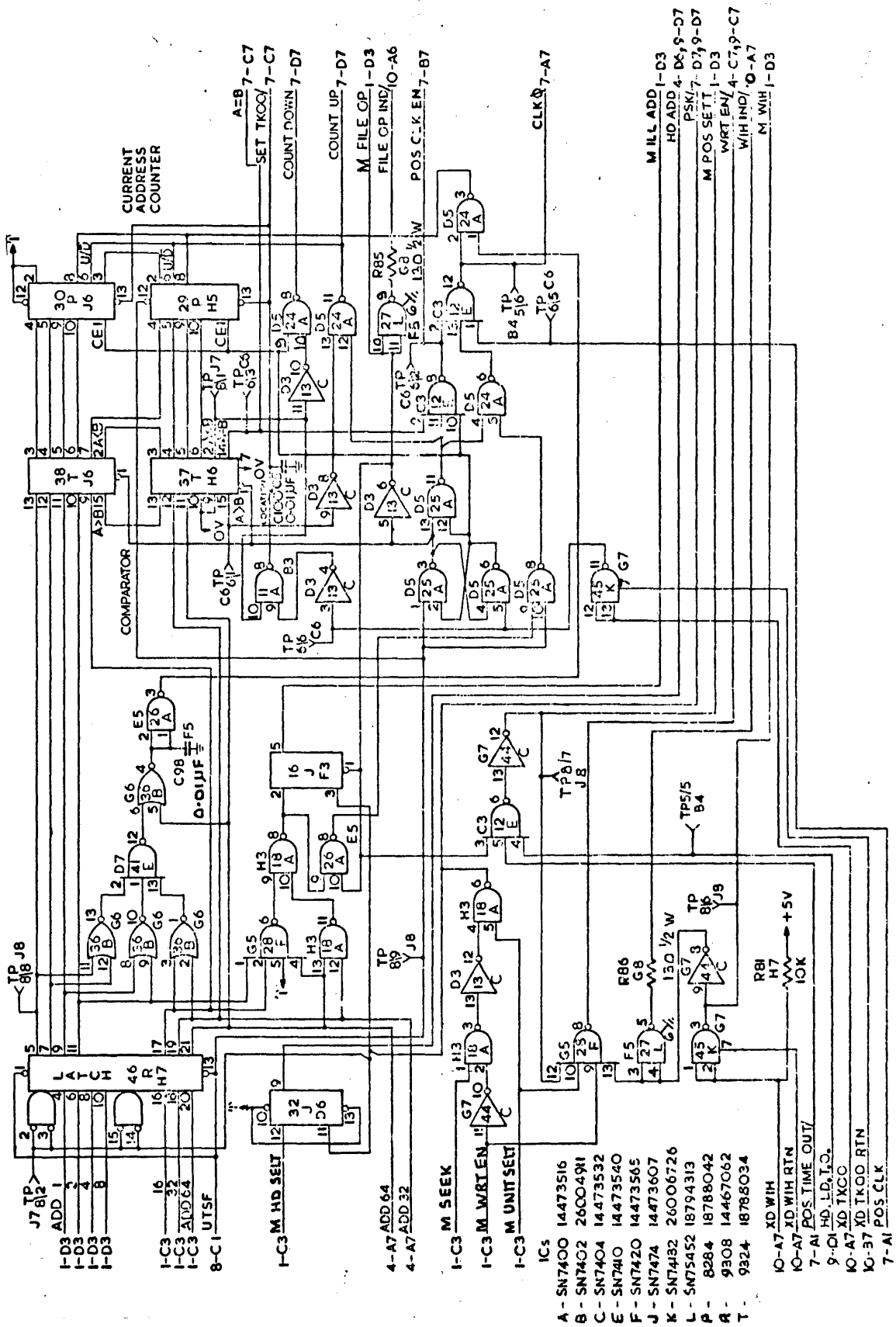


Figure 2–4. Schematic – Address Counter/Comparator

Functional Detail

STEPPER MOTOR DRIVERS

Refer to figure 2-5.

The stepper motor has 3 windings which are energized one at a time, in sequence. A winding is energized when the high-power Darlington transistor is switched on by a high at TP 7/5, 7/4 or 7/3. Selection is done by the stepper motor register and gates IC43. In order to limit the heat rise of the unit, power is removed from the motor when Position Settled signal goes TRUE, this is done by pins 11, 2 and 5 being made high.

The heads are held in position by the friction of the carriage.

Diodes 16, 17 and 18 and, the diodes internal to the transistors, provide protection from the high back-EMFs caused by the inductance of the motor coils.

STEPPER MOTOR REGISTER

The Stepper Motor Register energizes each of the three stepper motor windings in sequence. Both flip-flops start in a reset state at track 00. This state is made sure by a low to the reset inputs when SET TRACK 00/ goes low. With each clock pulse, the register counts up or down 1 place depending on the signal, COUNT UP or COUNT DOWN. Table 2-1 gives a truth table for the counter and drivers for every track.

Table 2-1. Stepper Truth Table

Track	IC35 pin 9	IC35 pin 8	IC35 pin 5	IC35 pin 6	TP 7/5	TP 7/3	TP 7/4
0	0	1	0	1	1	0	0
1	1	0	0	1	0	1	0
2	0	1	1	0	0	0	1
3	0	1	0	1	1	0	0
4	1	0	0	1	0	1	0
5	0	1	1	0	0	0	1
6	0	1	0	1	1	0	0
7	1	0	0	1	0	1	0
8	0	1	1	0	0	0	1
9	0	1	0	1	1	0	0
10	1	0	0	1	0	1	0
11	0	1	1	0	0	0	1
12	0	1	0	1	1	0	0
13	1	0	0	1	0	1	0
14	0	1	1	0	0	0	1
15	0	1	0	1	1	0	0
16	1	0	0	1	0	1	0
17	0	1	1	0	0	0	1
18	0	1	0	1	1	0	0
19	1	0	0	1	0	1	0
20	0	1	1	0	0	0	1
21	0	1	0	1	1	0	0
22	1	0	0	1	0	1	0
23	0	1	1	0	0	0	1
24	0	1	0	1	1	0	0
25	1	0	0	1	0	1	0
26	0	1	1	0	0	0	1
27	0	1	0	1	1	0	0
28	1	0	0	1	0	1	0
29	0	1	1	0	0	0	1
30	0	1	0	1	1	0	0
31	1	0	0	1	0	1	0
32	0	1	1	0	0	0	1
33	0	1	0	1	1	0	0
34	1	0	0	1	0	1	0
35	0	1	1	0	0	0	1
36	0	1	0	1	1	0	0
37	1	0	0	1	0	1	0
38	0	1	1	0	0	0	1
39	0	1	0	1	1	0	0
40	1	0	0	1	0	1	0
41	0	1	1	0	0	0	1
42	0	1	0	1	1	0	0
43	1	0	0	1	0	1	0
44	0	1	1	0	0	0	1

Track	IC35 pin 9	IC35 pin 8	IC35 pin 5	IC35 pin 6	TP 7/5	TP 7/3	TP 7/4
45	0	1	0	1	1	0	0
46	1	0	0	1	0	1	0
47	0	1	1	0	0	0	1
48	0	1	0	1	1	0	0
49	1	0	0	1	0	1	0
50	0	1	1	0	0	0	1
51	0	1	0	1	1	0	0
52	1	0	0	1	0	1	0
53	0	1	1	0	0	0	1
54	0	1	0	1	1	0	0
55	1	0	0	1	0	1	0
56	0	1	1	0	0	0	1
57	0	1	0	1	1	0	0
58	1	0	0	1	0	1	0
59	0	1	1	0	0	0	1
60	0	1	0	1	1	0	0
61	1	0	0	1	0	1	0
62	0	1	1	0	0	0	1
63	0	1	0	1	1	0	0
64	1	0	0	1	0	1	0
65	0	1	1	0	0	0	1
66	0	1	0	1	1	0	0
67	1	0	0	1	0	1	0
68	0	1	1	0	0	0	1
69	0	1	0	1	1	0	0
70	1	0	0	1	0	1	0
71	0	1	1	0	0	0	1
72	0	1	0	1	1	0	0
73	1	0	0	1	0	1	0
74	0	1	1	0	0	0	1
75	0	1	0	1	1	0	0
76	1	0	0	1	0	1	0
77	0	1	1	0	0	0	1
78	0	1	0	1	1	0	0
79	1	0	0	1	0	1	0
80	0	1	1	0	0	0	1
81	0	1	0	1	1	0	0
82	1	0	0	1	0	1	0
83	0	1	1	0	0	0	1
84	0	1	0	1	1	0	0
85	1	0	0	1	0	1	0
86	0	1	1	0	0	0	1
87	0	1	0	1	1	0	0

Functional Detail

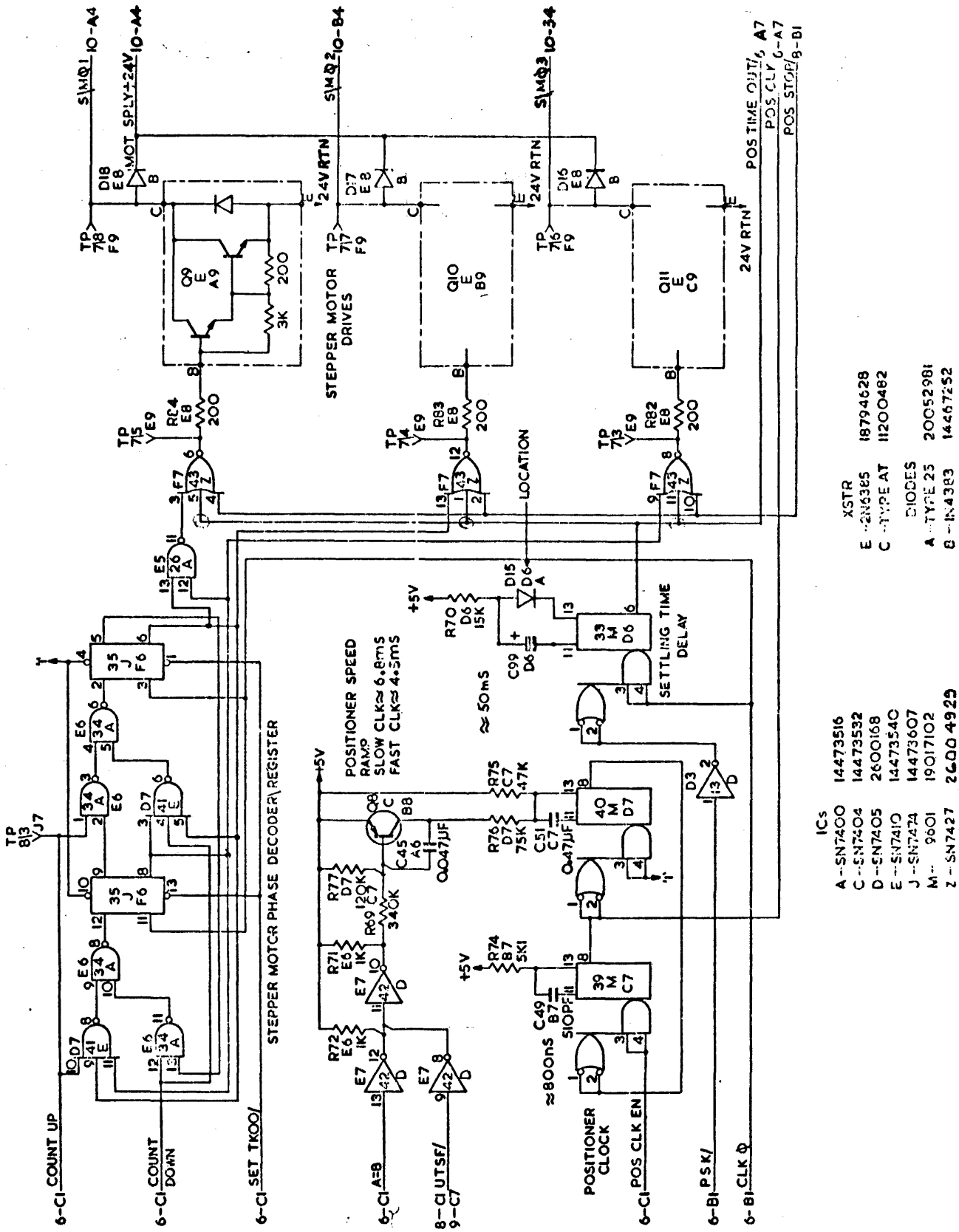


Figure 2–5. Schematic – Positioner Clock and Stepper Motor Drivers

STEPPER MOTOR

The stepper motor is made up of a stator with 12 poles, and a rotor with 8 poles (see figure 2-6). There are 3 coils, phase 1, 2 and 3 (Ø1, Ø2, Ø3). When the Ø1 coil is energized with +24 volts, a magnetic field is set up between the poles marked "1". The rotor will align itself to the position which gives the least reluctance to the magnetic flux that is teeth A, B, C and D will align with the "1" poles. The magnetic flux flows from A to B and from C to D. Any attempt to turn the rotor will be resisted by the magnetic force of alignment.

If Ø1 is de-energized and Ø2 energized the rotor will rotate 15° counter-clockwise so that teeth E, F, G and H align with the Ø2 poles. This is one step. Energizing Ø3 will step the rotor another 15° CCW so that A, B, C and D align with the Ø3 poles. Continuous energizing of the phases in the sequence 1-2-3, 1-2-3 will step the motor counter clockwise 15° per step. Similarly energizing in the sequence 3-2-1, 3-2-1 will step the rotor clockwise 15° per step.

In the Flexible Disk Drive application the stepper motor is used in slew mode so that the rotor does not settle between each step. The next phase is energized as soon as the rotor is approaching the last phase. In order to achieve this, the positioner clock is ramped, that is, it starts at 6.8 ms between pulses and is increased to 4.5 ms between pulses. This permits time for the carriage to accelerate from stationery to full speed without loosing step. This corresponds to 147 steps/sec and 222 steps/sec.

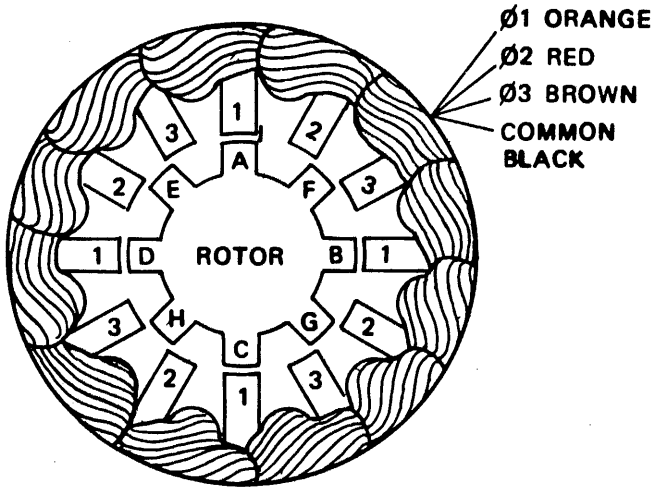
POSITIONER CLOCK (Refer to figure 2-5).

The positioner clock gives clock pulses to advance the stepper motor and current address counter. The frequency is ramped from 147 steps/sec to 222 steps/sec to permit for the extra time needed for acceleration of the rotor and carriage.

The clock is made up of two multivibrators (IC39 and IC40) connected to trigger each other. When the POSITIONER CLOCK ENABLE signal goes high, IC39 is triggered generating an 800 ns Positioner Clock pulse at pin 8 (TP 6/5). The trailing edge of this pulse triggers IC40 which generates a positive pulse at pin 8. The trailing edge of the pulse from IC40 triggers IC39. The process continues until POSITIONER CLOCK ENABLE goes low and inhibits IC39 from being triggered.

The time interval between pulses is determined by the period of IC40 which in turn is determined by capacitor C51, resistors R75 and R76 and transistor Q8. At the beginning of a carriage movement the stepper must be conditioned to run slow. This is done by A=B being high from a previous seek or UTSF/ being high before a disk is inserted. The high at IC42 pin 13 or 9 causes a high at 1C42 pin 10 which switches transistor Q8 off. The period of IC40 is therefore regulated by capacitor C51 and resistor R75 to 6.8ms.

Carriage movement can be started by inserting a disk or a seek pulse. When a disk is inserted and is up to speed, UTSF/ goes low. A = B is also low at this time due to the comparator output being disabled (refer to the comparator description). With both inputs low IC42 pin 11 goes high and pin 10 goes low causing transistor Q8 to switch on. Capacitor C45 causes transistor Q8 to switch on gradually bringing resistor R76 into parallel with resistor R75 so that the period of IC40 changes from 6.8ms to 4.5 ms. The same process occurs when seeking a new track, UTSF/ is already low and A = B goes low after the seek pulse. IC42 forms a positive OR gate or negative AND gate. Figure 2-7 illustrates the voltage at the collector of transistor Q8 and the POS CLK signal, the rise time of transistor Q8's collector is 25ms.



NOTE: STEPPER MOTORS SHOULD NOT BE DISASSEMBLED SINCE THE ACCURACY OF THE STOPS WILL BE REDUCED.

Figure 2-6. Stepper Motor

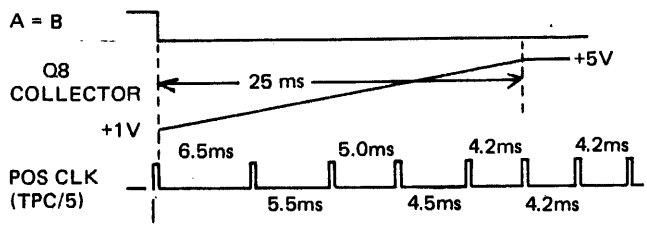


Figure 2-7 Positioner Clock Start-Up

CLOCK CONTROL.

Refer to figures 2–4 and 2–5.

The POS CLK EN signal is made high from the negative OR action of IC12 pin 8, in the conditions which follow:

1. When A = B is low. This occurs when a new track address has been latched into the address latches and is not equal to the present address of the carriage. When A = B clock pulses are stopped.
2. When File Op. Flip Flop is reset. This occurs from the time a unit is powered on until the disk is inserted and the heads settled on track 00.
3. UTSF/ and Track 00. This occurs if the disk is extracted and the carriage is on track 00. It causes the carriage to step away from track 00 so that the calibration sequence occurs correctly on the next disk insertion.

POS CLK EN enables the positioner clock to produce POS CLK pulses. POS CLK pulses are passed to the stepper motor register via IC12 pin 12. This gate prevents clock pulses reaching the stepper, stopping carriage movement, under the conditions which follow:

1. UTSF going Low. This occurs if the disk speed drops or the disk is extracted.
2. Illegal address and File Op. When the address latches contain an address greater than 87.

This is overridden by IC24 pin 4 permitting a Clock pulse if UTSF goes low while the carriage is on track 00.

DIRECTION CONTROL

The direction control circuit conditions the stepper motor register and the present address register to step in the correct direction. Two signals are produced: COUNT UP and COUNT DOWN

COUNT UP is produced by the conditions which follow:

1. A greater than B. This occurs when the new address is higher than the present address.
2. UTSF/* and Track 00. This occurs if the disk is extracted when the heads are on track 00. This causes the heads to step out beyond track 00 so that the calibration occurs correctly on the next disk inserted.

COUNT DOWN is produced by the conditions which follow:

1. A less than B. This occurs if the new address is lower than the present address, that is, the carriage must move away from the spindle.
2. File Op. Low. This occurs from power up or when a disk is removed until a disk is inserted and the heads have reached track 00.

POSITION SETTLED

The Position Settled signal gives information to the controller that the heads are settled on their new position and the pressure pad is engaged so that read or write operations may start.

Refer to figure 2-5.

PSK/ triggers IC33.

Positioner clock pulses, CLK Ø, retrigger IC33. Since the period between clock pulses (4.5ms) is much shorter than the period of the timer (50ms) the timer never times out but is constantly retriggered. This occurs until the desired track is reached and the CLK Ø pulses are stopped. 50ms after the last CLK Ø pulse, pin 6 goes high removing power from the stepper motor drivers and making the signal POS TIME OUT/ high.

POS TIME OUT/ is gated with File Op. and Head Load timeout to become the signal POS SETT. This signal goes to the common electronics where it will be gated onto the interface if this unit is selected. (UNIT SEL).

POSITIONER FLOW CHARTS

The charts which follow are intended to show the sequence of events during, Startup, Seek, Recalibrate and Disk extraction. On the left hand side of the flow chart the action is described, on the right hand side measurement criteria is provided.

START UP

INITIAL CONDITIONS

Motor is stopped	Disk not turning
No Index/Sector pulses	TP 5/4, 8/4, 8/5
Up to speed is low	TP 8/9 low
Address latches reset	IC46 outputs low
File op low	IC13 pin 6 low
File op indicator not lit	Visual
Comparison disabled	IC37 and 38 pin 1 low
Illegal address FF reset	IC16 pin 1 low
Positioner is away from track 00	TP 6/6 high
POS CLK EN true	IC25 pin 6 low; TP 6/2 high
COUNT DOWN true	IC 24 pin 8 high
Counter conditioned down	IC28 pin 6 low (TP 8/3)
TR 00 decoded inhibiting pulses to counter	IC26 pin 3 low IC24 pin 3 high
Clock running slow	6.8 mS pulses TP6/5

OPERATOR INSERTS DISK AND CLOSES DOOR

Motor Sw transfers	Disk turns
Index & sector pulses occur	TO 5/4, 8/4, 8/5 pulses
When disk up to speed UTSF sets	TP 8/9 high
CLK Ø pulses enabled	IC25 8 low IC12 pin 13 high. TP 5/6 pulsing.
Stepper register counts down	Stepper moves rearward
Pos Set timer triggered	IC33 pin 6 low

Functional Detail

Positioner reaches TR00 TR 00 transducer activated.	TP 6/6 Low
Counter and register reset	IC11 pin 8 low
File op FF set	IC25 pin 3 low, pin 6 high
File op indicator lit	Visual
Comparison enabled	IC38 & 37 pin 1 low
A = B is true	TP6/3 high
POS CLK EN false	TP 6/2 low
Further clock pulses inhibited	Carriage stops at TR 00

50 mS after last CLK pulse POS TIME OUT/ goes high	IC33 pin 6 high
Stepper motor coils de-energised	
POS SET true	IC44 pin 12 high

END

SEEK

INITIAL CONDITIONS

FILE op true	Indicator lit
A = B	TP 6/3 high
POS SET true	IC44 pin 12 high
POS CLK EN false	TP 6/2 low

SEEK PULSE

New address put on input of IC46	
Leading edge of SEEK clocks new address in	IC45 outputs hold new address
Illegal address decoded if address 87	IC18 pin 8 high
Trailing edge of SEEK does following:	
1. clock ILLEGAL ADD FF	IC16 pin 5 high if address is illegal
2. clock HD ADD FF	IC32 pin 9 low if upper head, high if lower head
3. trigger POS TIME OUT Timer	IC33 pin 6 low
Stepper motor coil energised	IC43, 11, 1, 2 and 5 low
If new head, solenoid energised. HD LD timer fired	IC12 pin 4 low for 115 mS
A = B low	TP 6/3 low
POS CLK EN true	TP 6/2 high
If A > B, COUNT UP high COUNT DOWN low Counter conditioned up	If TP 6/1 HI, TP 8/3 high IC24 pin 8 low TP 8/3 high
If A < B, COUNT DOWN high COUNT UP low Counter conditioned down	If TP 8/1 high, TP 8/3 low IC24 pin 8 high

1

1

Clock pulse occurs	Pulse on 6/5 and 5/6
Counter counts up or down 1 position	
Stepper register counts 1 up or down	Carriage moves 1 track
If A = B is still low	Wait next clock pulse

POSITION REACHED

A = B high	TP 6/3 high
POS CLK EN false	TP 6/2 low
No further clock pulses	Carriage stops, coils energised

50 mS after last clock POS TIME OUT/ goes high	IC33 pin 6 high
Stepper coils de-energised	
If HEAD LOAD TIME out complete POS SET true	IC44 pin 12 high

END

RECALIBRATION

Seek Track 00	IC26 pin 3 low track 00 decode
A < B because A = 00	TP 8/1 high
COUNT DOWN high	IC24 pin 8 high TP 8/3 low
A = B is low	TP 6/3 low
POS CLK EN true	TP 6/2 high

Clock pulses occur	1 μS pulse TP 6/5
Stepper motor register counts down	Stepper moves rearward

TR 00 transducer is activated	TP 6/6 low
Counter and Stepper motor reg reset	
A = B true	TP 6/3 high
POS CLK EN false	TP 6/2 low
Further Clk pulses inhibited	Stepper stops at track 00

50 mS after last clock IC33 pin 6 times out	POS SET high IC44 pin 12 high

Note: Counter is inhibited from couting down by IC24 pin 1 low. This holds A < B true until Track 00 transucer is cut.

Functional Detail

HEAD SELECT

The purpose of the Head Select circuitry is to enable the selected head by connecting its center tap to ground and to select the correct pressure pad solenoid to press the disk against the head.

Refer to figure 2-4

The signal "head select" is sent to both master and slave units, going onto flip-flop IC32 pin 12. If the unit is selected and a write is not in progress, a seek pulse will clock IC32 pin 11. This will set the flip flop in the same state as head select. This signal is named HD ADD.

Refer to figure 2-15.

If HD ADD is high, Q1 is switched on connecting the center tap of the lower head to ground. If HD ADD is low, Q2 is switched on connecting the center tap of the upper head to ground.

Refer to figure 2-8.

Gates IC17 pins 8 and 12 control the energizing of the upper or lower solenoids.

If HD ADD is high and the disk is up to speed and the conditions for energizing are satisfied then TP 7/2 is low and Q12 switched on energizing the upper solenoid.

If HD ADD is low and the disk is up to speed and the condition for energizing are met, Q13 is switched on energizing the lower solenoid.

HEAD LOAD SOLENOIDS AND TIMER

For correct operation of the recording head, the disk must be pressed against the head with a pressure of approximately 11 grams. This makes sure that the head gap is in good contact with the disk. This is made with a spring loaded pressure pad on the opposite side of the disk. The heads are offset to accomodate the pressure pads. Energizing the solenoid lowers the pad onto the disk. De-energizing the solenoid lifts the pad off the disk.

In order to lengthen the life of the media, the pressure pad is disengaged 5 revolutions after the end of Read or the end of Write, whichever is latest. In order to re-engage the pad a SEEK pulse or RD EN or WRT EN is needed.

Refer to schematic, figure 2-8.

Before a disk is inserted, and until the disk is up to speed, UTSF is low disabling gates IC17 pins 10 and 2. Neither solenoid can be energized. UTSF/ being high at this time sets all the flip-flops in the 5 bit shift register IC19 (data inputs pins 2, 3, 4, 6 and 7 are high and preset enable is high) UTSF being low resets flip-flop IC22 causing a high on pin 4 of IC11. If RD EN and WRT EN are false, pin 5 IC11 is also high placing a high on 'Serial in' of IC19.

INDEX is connected to the clock input pin 1, therefore, on each revolution the data is shifted one position and 'Serial in' is shifted in. Pin 10 output will stay high keeping the solenoids de-energized until a SEEK occurs.

A SEEK pulse sets flip-flop IC22 causing pin 6 to go low, this causes a low on the clear input of IC19, resetting all flip-flops and making pin 10 low. This enables pins 11 and 13 of IC17. The solenoid to be energized is selected by HD ADD, high makes IC17 pin 8 low energizing the upper solenoid, low makes IC17 pin 12 low energizing the lower solenoid.

Flip-flop IC22 stays set until either a read or write operation is performed.

RDEN/ or WRTEN/ going low causes a high on pin 3 IC22 resetting the flip-flop.

Pin 4 IC22 goes high. At the end of the Read or Write pin 5 also goes high placing high onto pin 9 serial in. This high gets shifted into the register on each index pulse.

Unless a new SEEK pulse is given IC19 pin 10 will go high after 5 revolutions, de-energizing the solenoid.

The solenoid takes a maximum of 60ms to pick. Therefore, as an indication to the controller that a Read or Write should not be attempted POSITION SETTLED is made false for 60ms following the energizing of either solenoid. IC15 and inverters IC14 pins 2 and 4 form an exclusive OR gate with a high out of IC15 pin 11 to trigger IC23 when either TP 7/2 or TP 7/1 goes low. C54 delays the waveform at TP 7/1 to make sure of a trigger pulse when switching heads.

The negative 60ms pulse appearing on TP 5/5 goes to IC12 pin 4 (see schematic, figure 2-4) causing POSITION SETTLED to go low for 60ms.

INDEX AND SECTOR PULSES

The purpose of sector pulses is to supply the controller with timing pulses corresponding to the beginning of each sector of information.

There are 32 sector pulses for each revolution of the disk. The sector pulses are equally timed 5ms apart. One revolution of the disk takes 165ms (370 rpm).

The index pulse informs the controller that the next sector pulse marks the beginning of Sector No. 1. Index occurs midway between Sector No. 32 and Sector No. 1. Index pulses occur every 165 ms.The index pulse is also used in the drive to detect when the disk is up to speed, and also to disengage the head pressure pad 5 revolutions after Reading or Writing in complete.

Index and Sector pulses are generated by holes punched in the disk allowing infra-red light to fall on a photo sensitive transistor as the disk rotates. There are 33 holes in the disk, 32 evenly spaced for sector and one extra midway between 2 sector holes for index.

Functional Detail

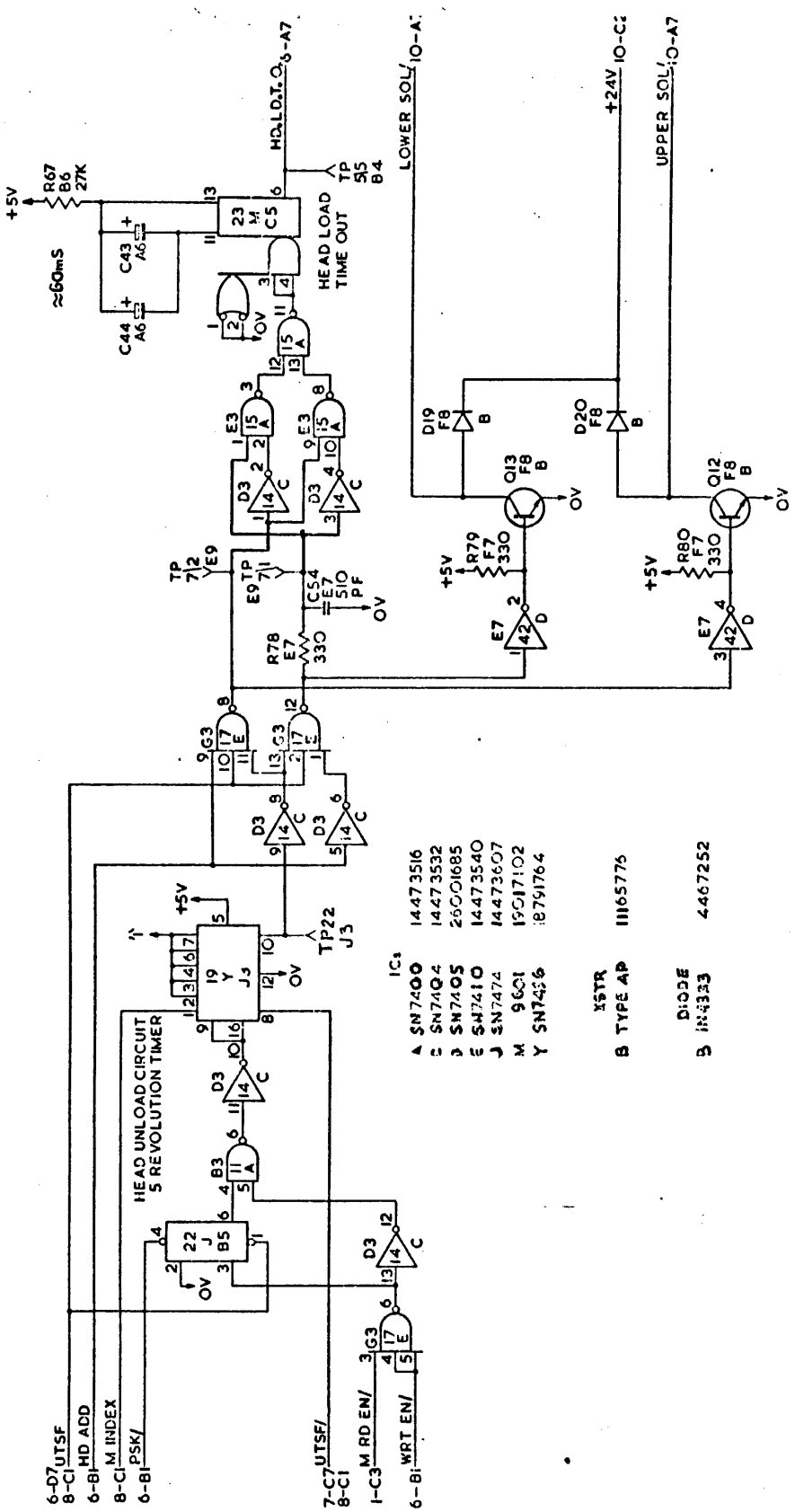


Figure 2–8. Schematic – Head Load Control

Functional Detail

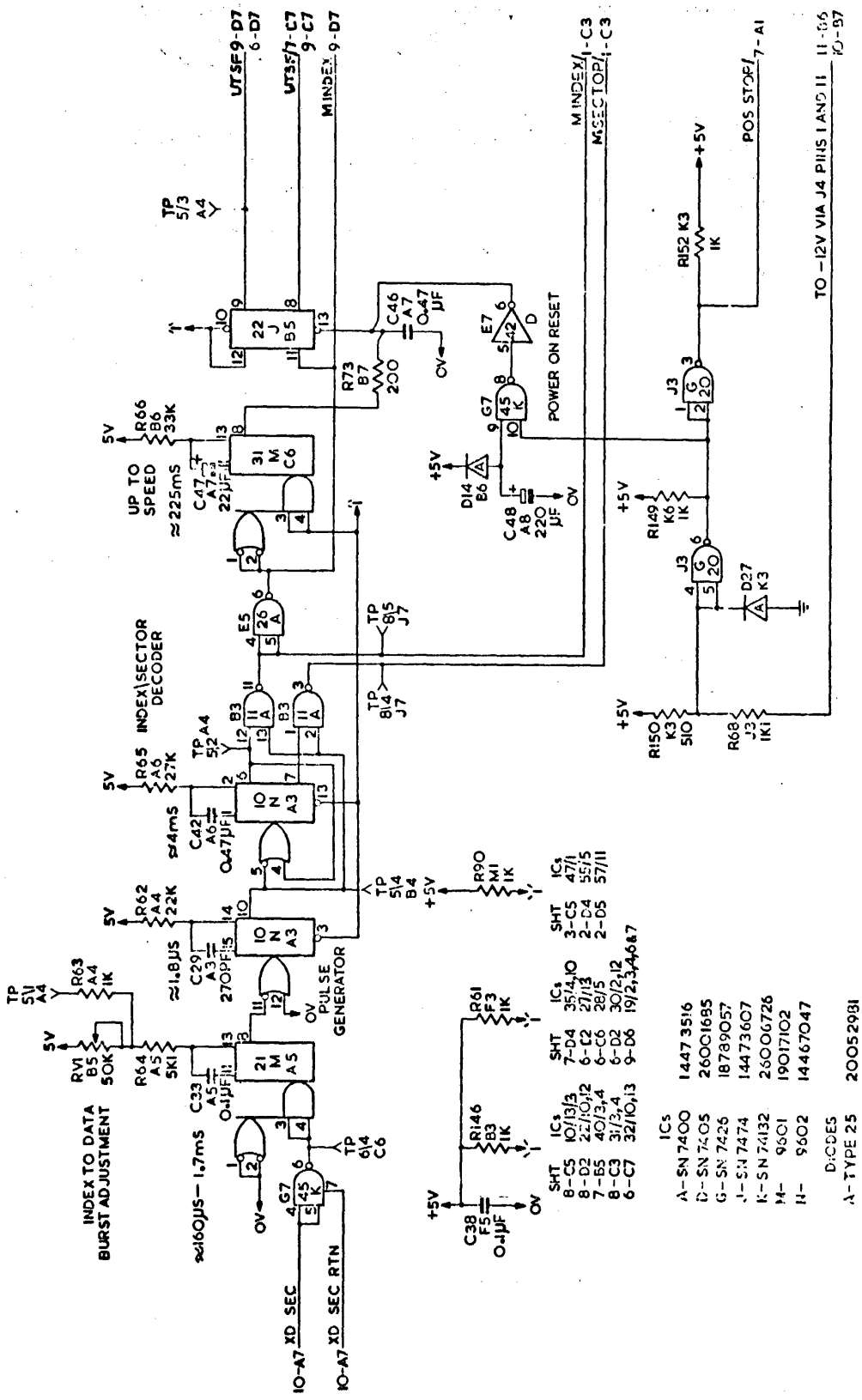


Figure 2–9. Schematic – Index/Sector Pulses

Discrimination of the index pulse is performed by the electronics.

Refer to figure 2-9 and figure 2-10.

As the disk rotates and a hole passes between the light source and the photo sensitive transistor, light falls on the transistor making the output fall towards 0V. At approx. +0.9V the schmitt trigger IC45 fires causing TP 6/4 to go high triggering IC21.

IC21 is an adjustable delay to delay Index and Sector pulses. Its purpose is to compensate for mechanical tolerances between the index/sector transducer and the magnetic heads. The delay is adjusted with the aid of the alignment disk so that the index and sector pulses occur at the same time relative to the data regardless of which drive the disk is read on.

At the end of the delay, pulse standardizer IC10 pin 10 is fired.

The negative edge of the standardized pulse fires the 4ms timer.

Pulses on TP 5/4 occurring outside the 4ms are decoded as SECTOR/ pulses TP 8/4. Pulses occurring during the 4ms are decoded as INDEX/ pulses TP 8/5.

UP TO SPEED (refer to figure 2-9)

When the unit is powered on, UTSF is held reset for 300ms minimum by C48 holding a low on IC22 pin 13. This is to prevent the flip-flop being set by spurious pulses occurring as the unit is powered on.

When a disk is inserted and the receiver lowered, the drive motor is switched on and the disk starts to turn. The leading edge of the first index pulse clocks IC22, however, because IC31 has not been triggered yet, the flip-flop is held reset by a low from IC31 pin 8 to IC22 pin 13. The trailing edge of the index pulse triggers IC31. While IC31 is timing out, the reset is removed from IC22 therefore if the next index pulse occurs within 225ms, UTSF is set. If the next index pulse occurs after 225ms, IC31 times out, holding IC22 reset.

During normal operation, index pulses occur 160ms apart, thus IC31 is constantly retriggered and never times out. If however, the speed of the disk drops and the index pulse takes longer than 225ms IC31 times out resetting IC22 with a low on pin 13.

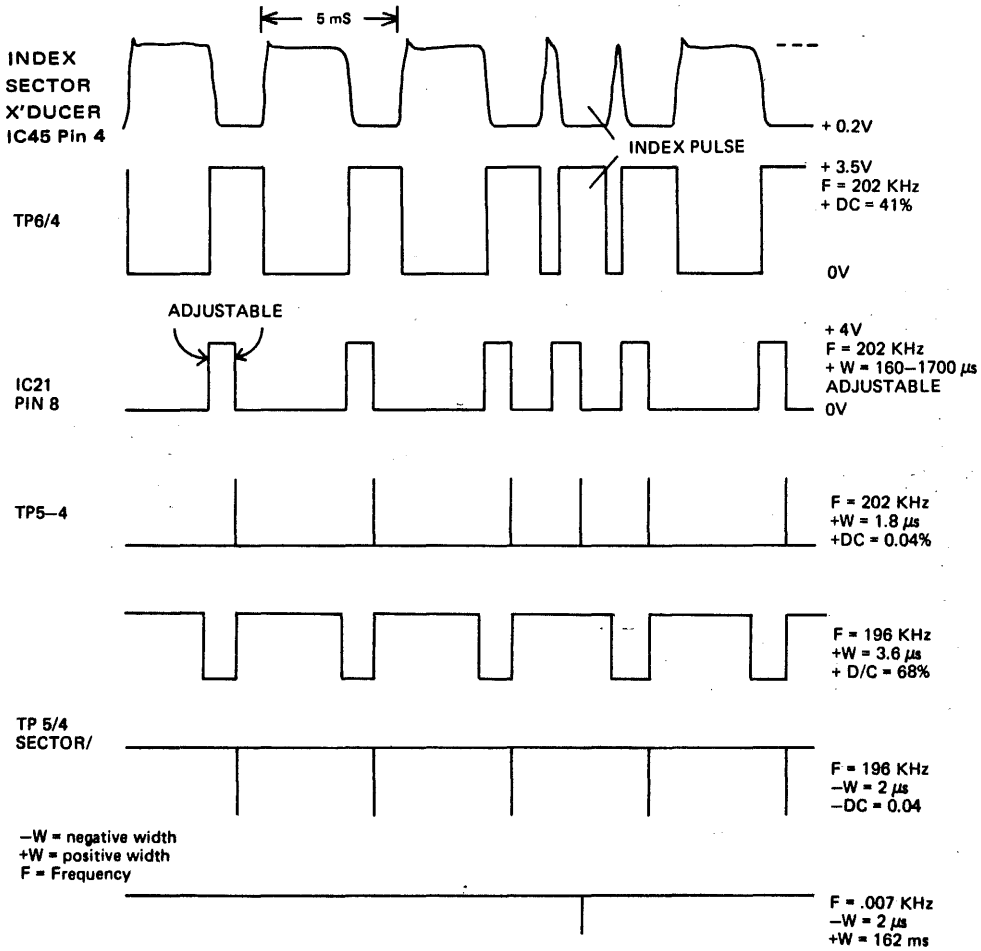


Figure 2–10. Index and Sector Generation

WRITE

GENERAL.

The unit writes data, Bit serial, MSB first onto the selected unit and surface when the signal WRT EN goes true. When the unit is not reading, the write clock is sent to the controller for its internal use. When writing is required, the controller supplies data on the WRT DATA line in bit serial NRZ, syncronized to the write clock. Formatting of the preamble, sync bytes, address, data, parity and postamble is a function of the controller or host system. In the drive unit, the NRX data has to be converted to MFM, sent to either the master or slave, and written on the disk. In addition, during Write, the erase current must be switched on to erase a 'guard band' on each side of the data.

This prevents noise pick up from previously recorded data in the event of a slight head misposition when reading the data back. Writing over previously recorded data destroys the old data due to the fact that the disk is saturated with magnetic flux. Refer to figure 2-11 for a block diagram of the Write function.

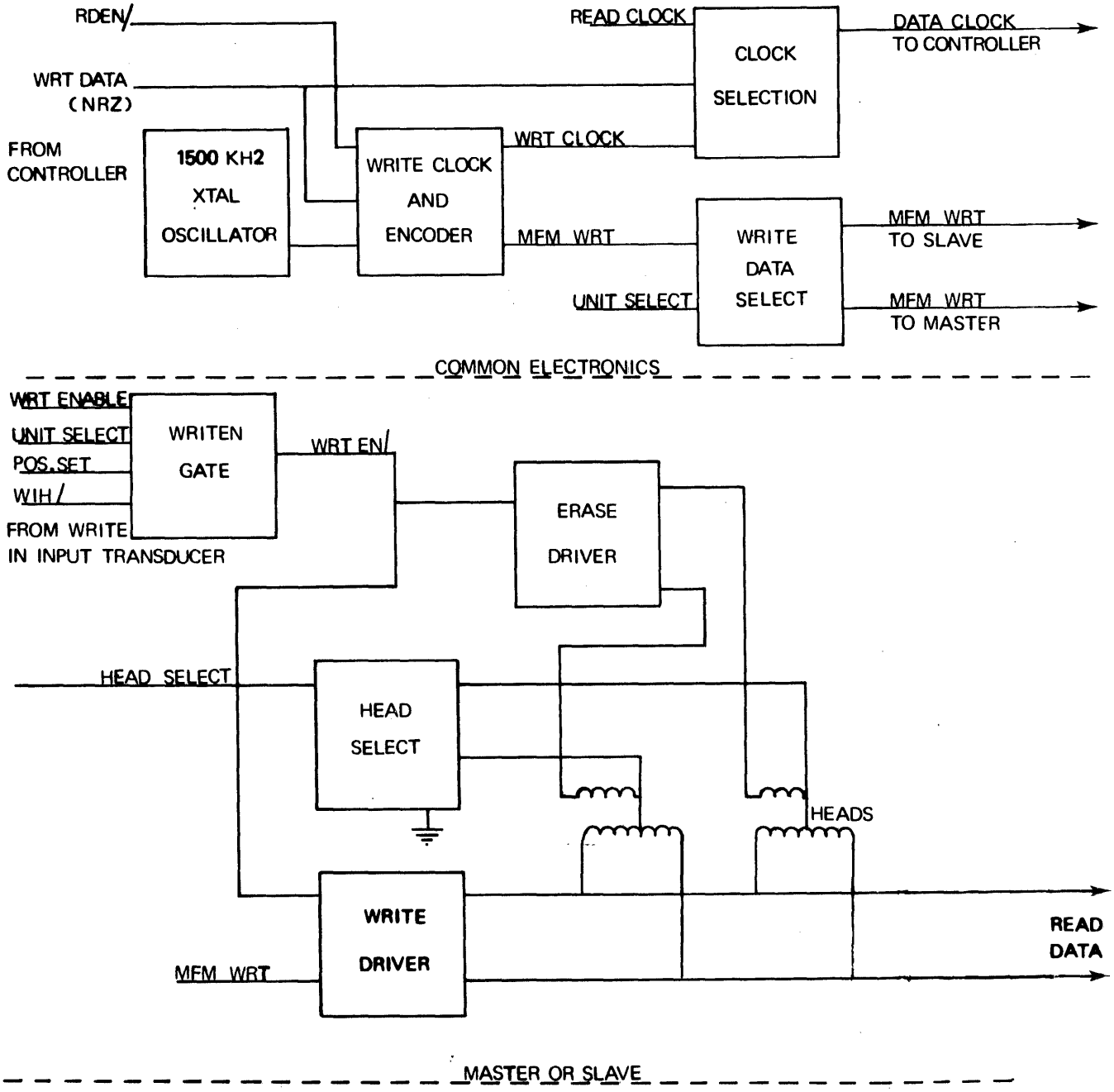


Figure 2–11. Write Block Diagram

Functional Detail

WRITE CLOCK

Refer to Figure 2-13 and timing diagram 2-12.

The Xtal clock runs continuously at a frequency of 1500 KHz. When RD EN is not true, that is, when not Reading, clock pulses are permitted to clock flip-flop IC47, dividing the frequency to 750 KHz. This signal goes to the phase lock loop circuitry to maintain the PLL syncronized. It also clocks IC54 which is a divider giving a 375 KHz WRT CLK signal on TP 9/2.

Refer to schematic figure 2-14. Whenever the unit is not Whenever the unit is not reading, WRT CLK pulses are gated through IC52 to become DATA CLK to the controller.

WRITE DATA ENCODE

Refer to figure 2-12 and 2-13.

MFM WRT pulses consist of a pulse at the beginning of a cell for a zero and a pulse at the center of a cell for a one. Where a zero follows a one, the zero pulse at the beginning of the cell is omitted. Gate IC46 pin 8 gates the 'ones' bits. Gate IC48 pin 6 gates the 'zero' bits.

NRZ data is clocked into flip-flop IC49 pin 5 on the leading edges of each WRT CLK pulse. This is shifted into IC49 pin 8 on the following clock pulse. Thus, the second FF always contains the state of the previous bit written, 'ones time' is when TP10/2 is low and TP 9/2 is low. If data is high at this time (TP 9/1) a pulse will be permitted through IC48 pin 8 and IC53 pin 8, 'zeros time' is when TP 10/2 is low and TP 9/2 is high. If data is low at this time IC48 pin 4 is high. Providing that the previous bit was not a one, IC49 pin 8 will be high permitting a zeros pulse through IC48 pin 6 to TP 9/4.

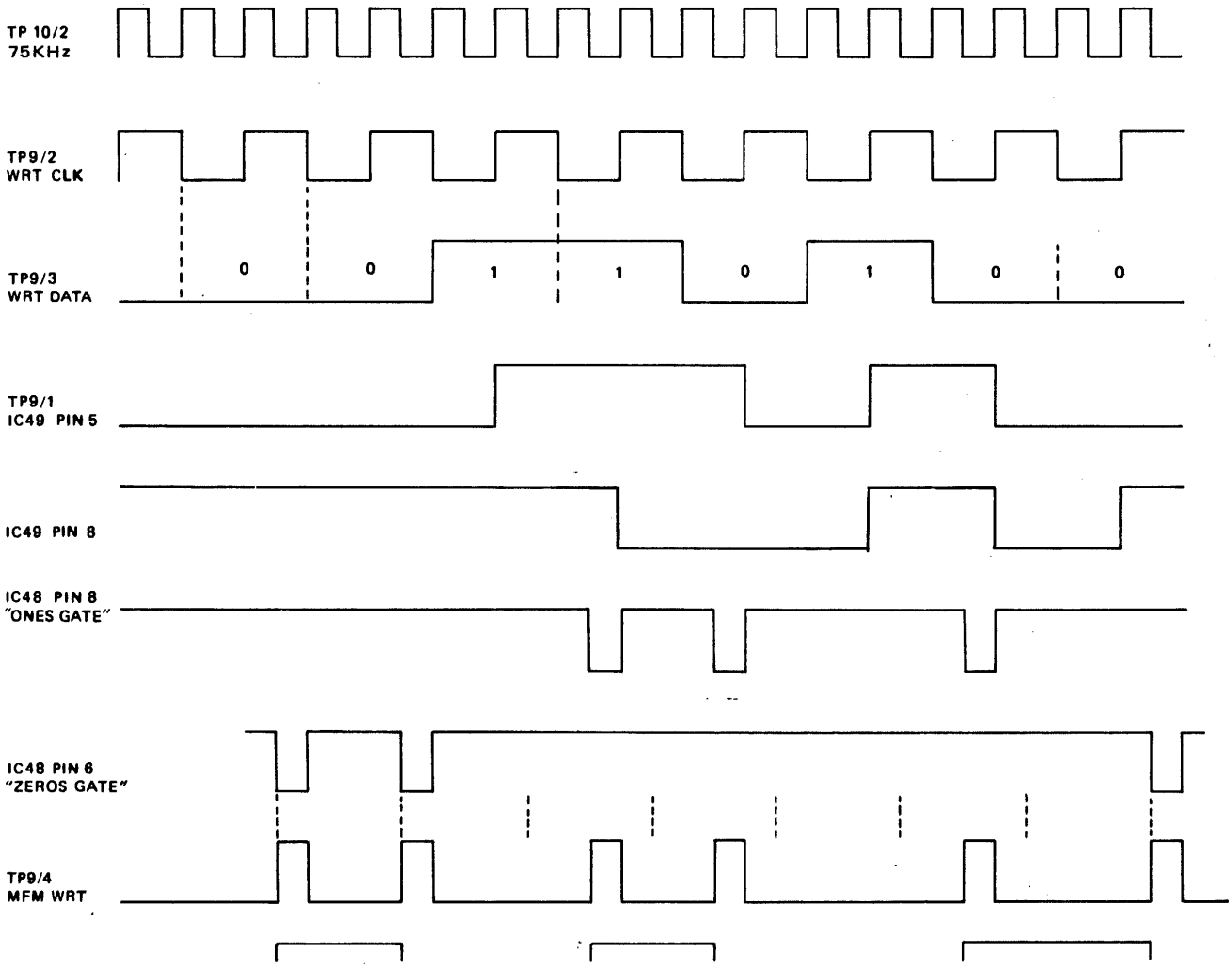


Figure 2–12. Write Timing

Functional Detail

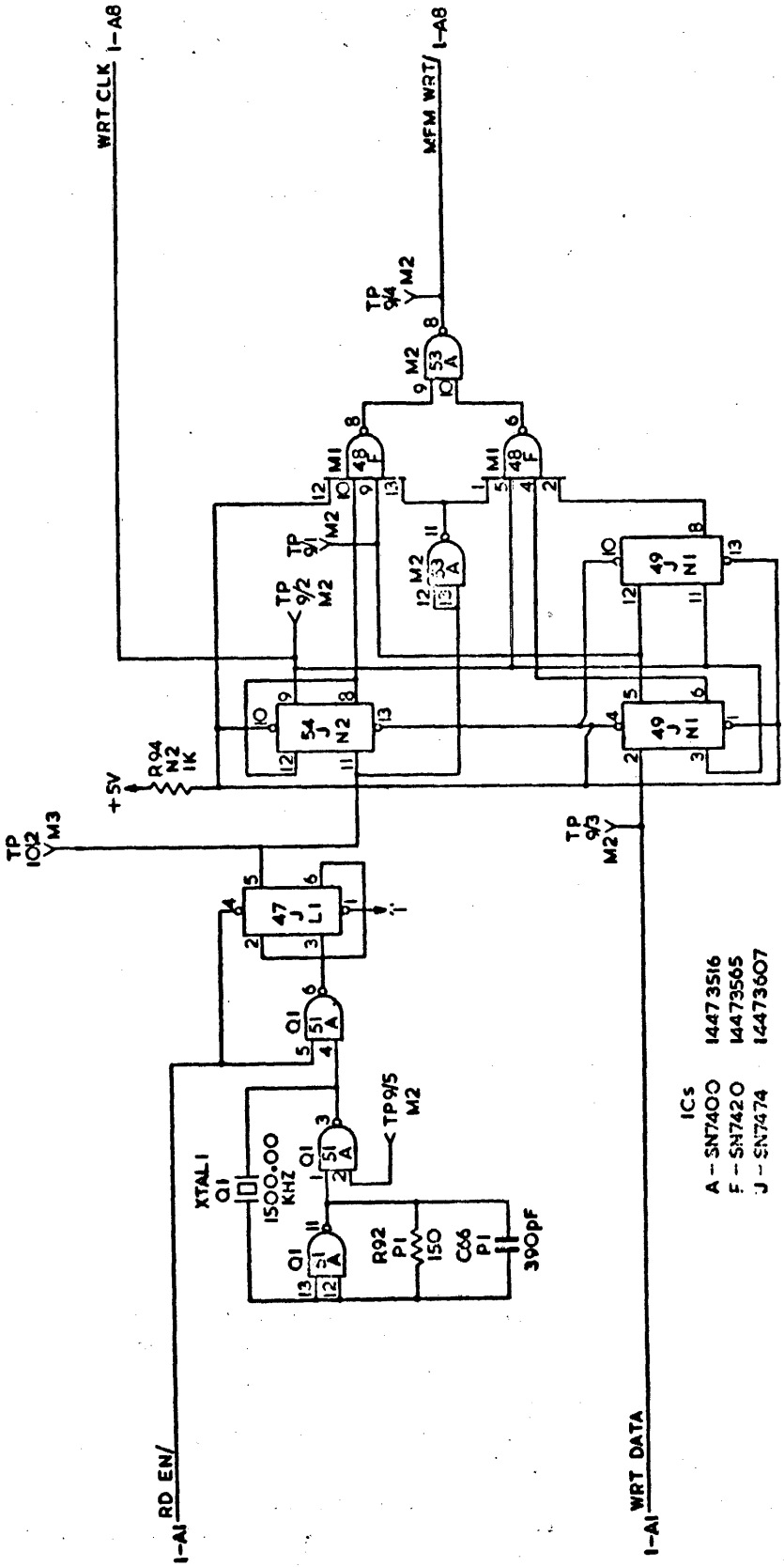


Figure 2–13. Schematic – Write Data Encoder

Functional Detail

UNIT SELECTION
Refer to figure 2-14.
MFM WRT pulses are gated to the master unit if UNIT SEL/ is false through IC62 pin 3, and to the slave if UNIT SEL/ is true through IC62 pin 11.

Refer to figure 2-4.
WRT EN is gated with UNIT SELECT, POSITION SETTLED, and WRITE INHIBIT/ to become WRT EN/ to the write and erase drivers.

WRITE INHIBIT
Refer to figure 2-4.
In order to prevent writing on a disk, the operator can remove the covering from the WRITE INHIBIT hole on the disk envelope. This allows light to fall on the photo sensitive transistor when the disk is inserted in the unit. TP 8/6 goes high and IC28 pin 13 goes low preventing WRT EN from reaching the write and erase drivers.

WRITE AND ERASE DRIVERS

Refer to figure 2–15.

When WRT EN/ goes false, the reset is removed from IC2 and gates IC3 pins 5 and 10 are enabled. IC2 pin 6 is true making IC3 pin 8 false. This switches on Q6. This causes current to flow from ground through Q1 or Q2 (depending upon HD ADD) through half of the recording head, through Q6 and the current source Q5 to +12 volts. This will magnetize the disk media in one direction

The positive going edge of the first MFM WRT pulse will set the flip flop IC2. This switches off Q6 and switches on Q7. This causes current to flow from ground, through Q1 or Q2, through the other half of the recording head, through Q7 and Q5 to +12 volts. This will magnetize the disk in the opposite direction.

The positive going edge of each MFM WRT pulse will complement IC2 changing the direction of magnetization of the disk. This will continue until WRT EN/ goes true. WRT EN/ going true will reset IC2 and disable gate IC3 pins 5 and 10. IC3 pins 6 and 8 will go true switching off Q6 and Q7.

Q5 is the current source for write drivers. Q4 and Q5 are identical transistors with identical emitter resistors. The current flow through Q4 will cause an identical current flow through Q5. Therefore by varying the current in Q4 the current in Q5 is varied. For any cylinder address below 32 both ADD64 and ADD32 will be false. This causes the output of gate IC3 to go false. The collector load for Q4 is then R19 to ground.

This allows the higher current to flow through Q4 and thus through Q5.

For cylinder address 32 or greater, ADD32 or ADD64 will be true.

This permits the output of gate IC3 to float. R19 then forms part of the collector load of Q4, thus reducing the current flow through Q4 and Q5.

At the same time as data is being written the erase winding is energized. This is to erase any old information at the edge of the new data and so provide a guard band. When WRT EN/ goes false Q3 is switched on. Current then flows from ground through Q1 or Q2, through the selected erase winding, through Q3 to +12 volts. C1 causes a delay to the switch on a switch off of Q3 to compensate for the distance between the information gap and the erase gap in the head.

READ HEAD SELECT
Refer to figure 2-15.
When the unit is not writing (WRT EN/) Q6 and Q7 are switched off. The diodes D9 and D10 prevent the capacitance of Q6 and Q7 affecting the input to the read amplifiers. The diode also prevents any feedback on the read amplifier circuit which could be caused by pickup in the emitter circuit of Q4 and Q5.

The centre connection of one of the heads is connected to ground through either Q1 or Q2. This is determined by the logic level of HD ADD. When the center connection is connected to ground, the diodes D7 and D6 or D9 and D8 are forward biased. The small AC voltage induced in the read head is passed through the forward biased diodes to the read amplifier.

READ CHANNEL
Refer to figure 2-16 and 2-18.
The output of the read head is taken to pins 1 and 2 of IC4. The resistors R27 and R28 and the diodes D11 and D12 form the clamp to prevent overloading the read channel during write operations. The gain of IC4 is 100. Following IC4 is a low pass filter to reject noise above 500 KHz.

Reference figure 2-17.
The signal TP14 is the positive output of IC4.

The delay line DL1 differentiates this signal to produce a signal with zero crossing times corresponding to the peaks of signal TP 14. This differentiated signal is amplified by IC7 and appears at TP16. IC8 is a comparator which produces a square wave output from the signal at TP16.

Functional Detail

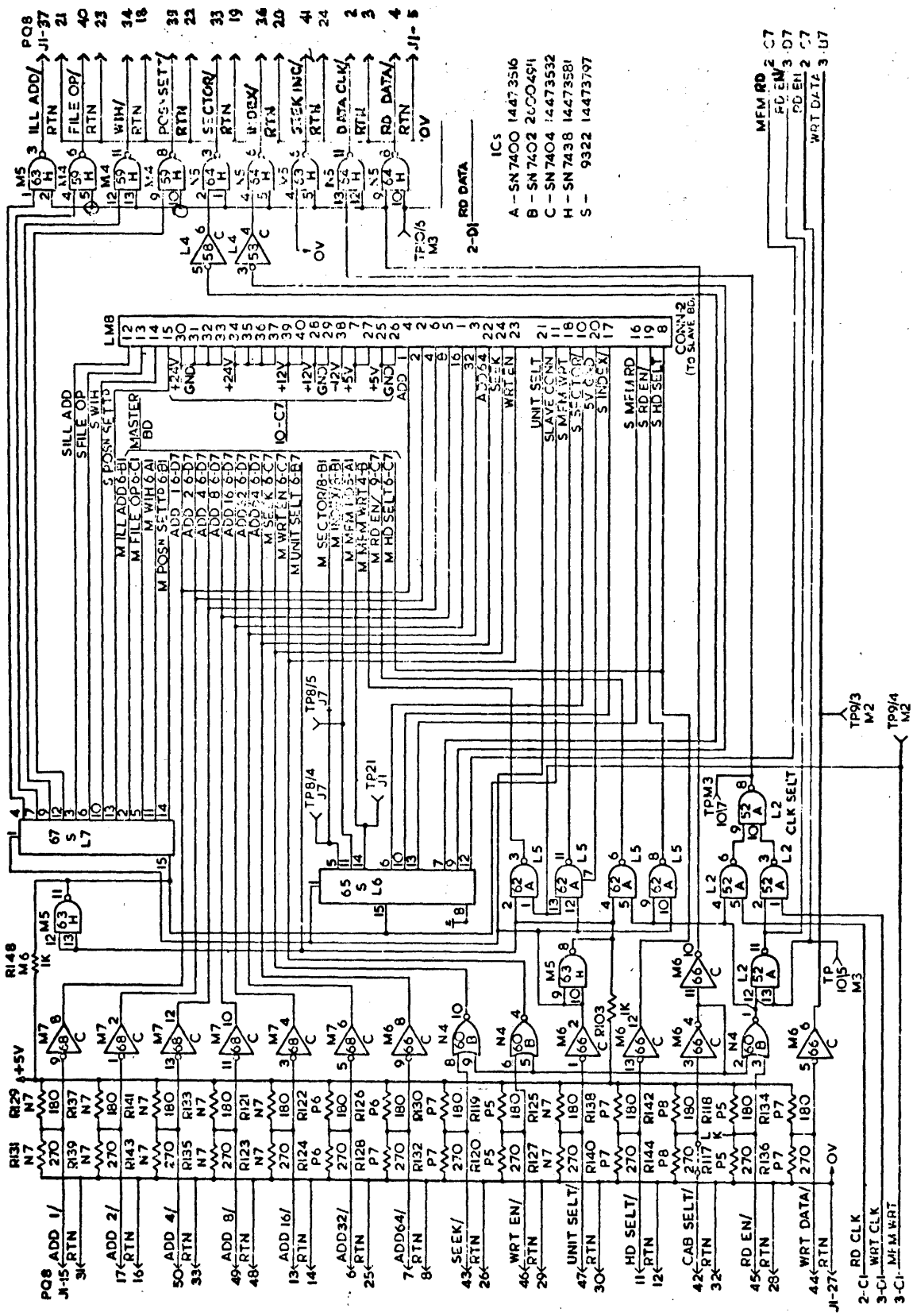


Figure 2–14. Schematic – External Interface Logic

Functional Detail

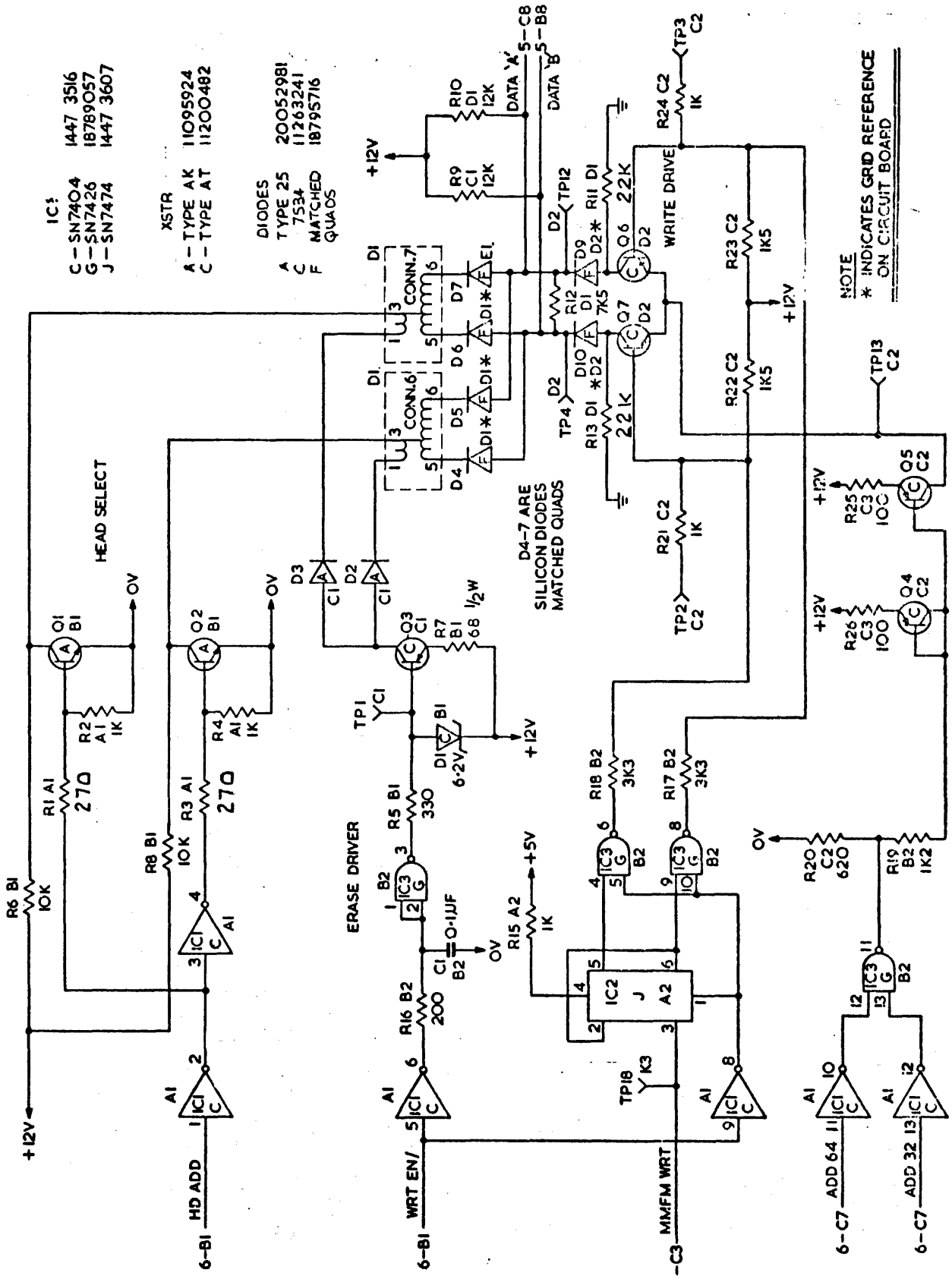


Figure 2–15. Schematic – Write Driver

DIGITAL FILTER

Refer to figure 2-16 and 2-18.
The purpose of the digital filter is to eliminate noise from the read signal and to produce MFM RD pulses of a standard pulse width. The gates IC6 perform and EX NOR between the comparator output and the latch output. The output of IC6 pin 8, R37 and C8 form a ramp generator. The transistors Q16, Q15 and Q17 are the pulse standerdizer.

A change in logic level at IC8 pin 7 will cause IC6 pin 8 to float (Open Collector Output). The capacitor C8 will charge causing the voltage on the base of Q16 to rise. When this voltage reaches approximately 5.5 volts, Q16 will switch on. When Q16 switches on, a negative pulse is applied to the base of Q15. This causes a positive pulse at the collector of Q15 which is inverted by Q17 to form the signal MFM RD.

The flip-flop IC5 complements on the positive edge of the MFM RD pulses. When IC5 complements, IC6 pin 8 goes low and should stay low until the next change of logic level at IC8 pin 7. A noise pulse at the output of IC8 will cause IC6 pin 8 to float for the duration of the noise pulse. The noise pulse will be too short to permit C8 to charge to 5.5 volts. Therefore Q16 will not be switched on and the noise will have no effect on MFM RD.

DATA DECODE.

GENERAL

The signal MFM RD is sent to the common electronics from the master unit and the slave. The function of the common electronics is to select the required MFM RD (master or slave) and decode the information from MFM to NRZ, also producing a data clock for use by the Control to strobe in the NRZ data into the registers/memories.

SELECTION

Refer to schematic 2-14.
Selection of the Read Data either from the master unit or the slave is achieved by multiplexor chip IC65.

Depending on UNIT SELECT, IC65 will permit the signal from pin 13 (slave) or pin 14 (master) to go to the data decoder.

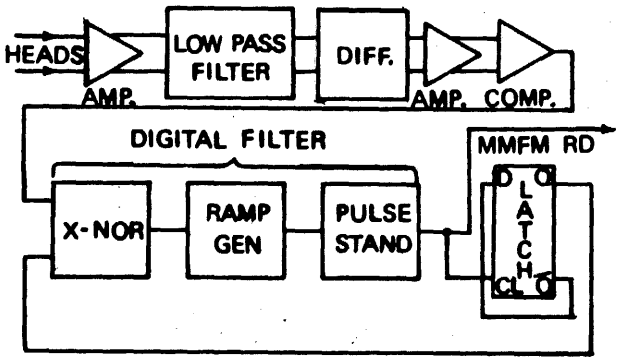


Figure 2–16. Read Block Diagram

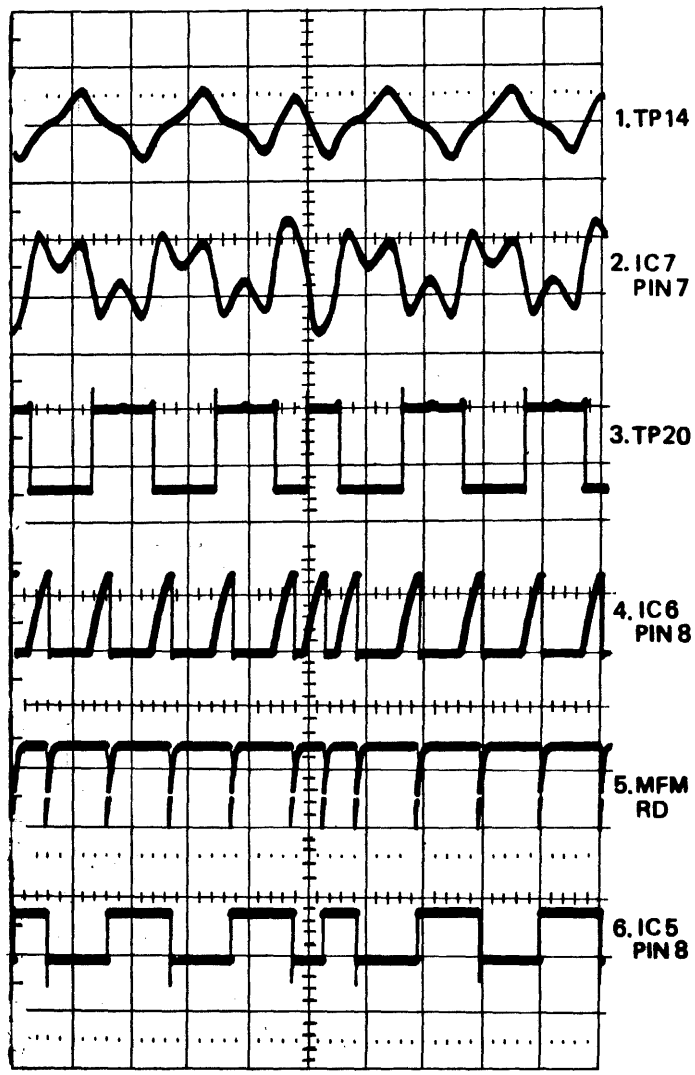


Figure 2–17. Read Channel Test Points

Functional Detail

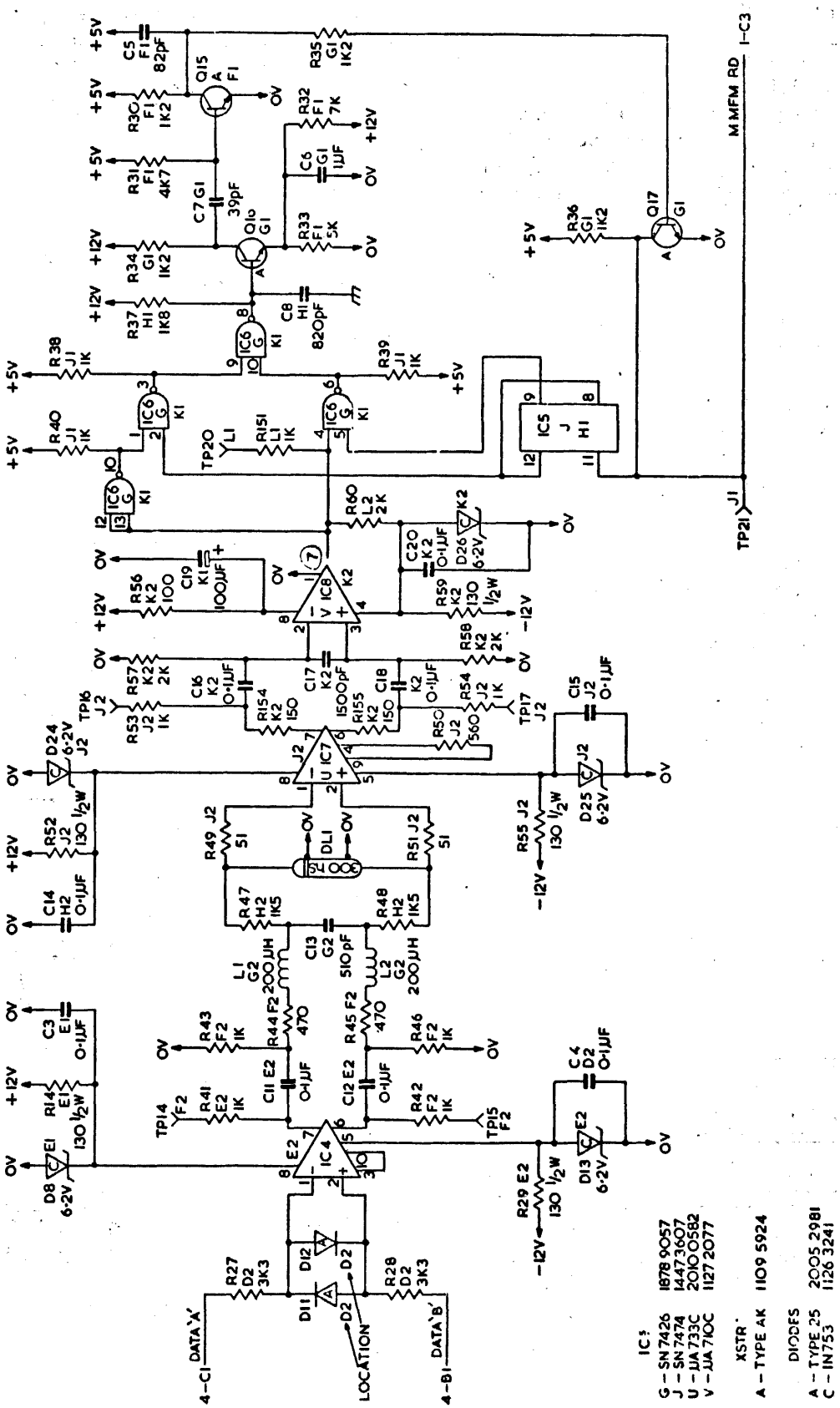


Figure 2–18. Schematic – Read Channel

Functional Detail

STANDARDIZER AND P.L.L.

Refer to schematic 2-21.

Approx. 100 microseconds after a sector pulse, READ ENABLE goes true from the controller permitting MFM RD pulses to trigger timer IC57 pin 6.

The purpose of this timer is to standardize the length of the read pulses. TP11/7 therefore has a 350 ns pulse occurring approximately 150 ns after each peak. This pulse train feeds onto pin 12 of the phase-locked-loop.

P.L.L.

The purpose of the phase-locked-loop is to provide a reliable source of timing pulses for use on decoding data and deriving the read clock.

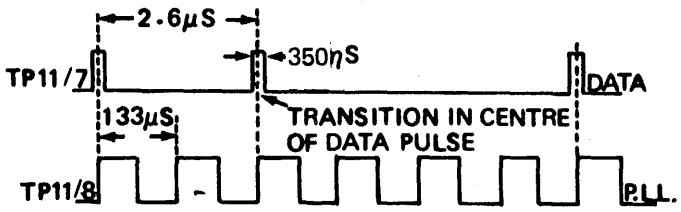


Figure 2–19. P.L.L./Data Relationship

The P.L.L. consists of an oscillator running at two times the maximum data rate and locked onto the data pulses coming from the disk. If the disk speeds up the P.L.L. frequency increases, if the data rate slows down the P.L.L. frequency decreases. The natural frequency is 750 KHz, this is adjusted with RV4. The natural frequency can be varied by the data by ± 6%.

Refer to figure 2-21.

The phase-locked-loop compares its frequency with the input data pulses and adjusts itself so that the output transition occurs midpoint of the input pulse. The speed of correction is determined by R112 and C80.

READ ENABLE DELAY

Before RD EN goes true, the low level resets the RD DATA flip-flop via IC50 pin 2 low, pin 3 high, pin 6 low. When RD EN goes true, it triggers timer IC57 pin 12. This causes the RD DATA flip-flop to be reset for a further 400 μSecs via a low pulse on IC50 pin 1 causing a low on IC56 pin 13.

This prevents data reaching the controller while the PLL locks up onto the preamble data. C64 maintains the reset from the time RD EN goes high to the time when the timer output goes low.

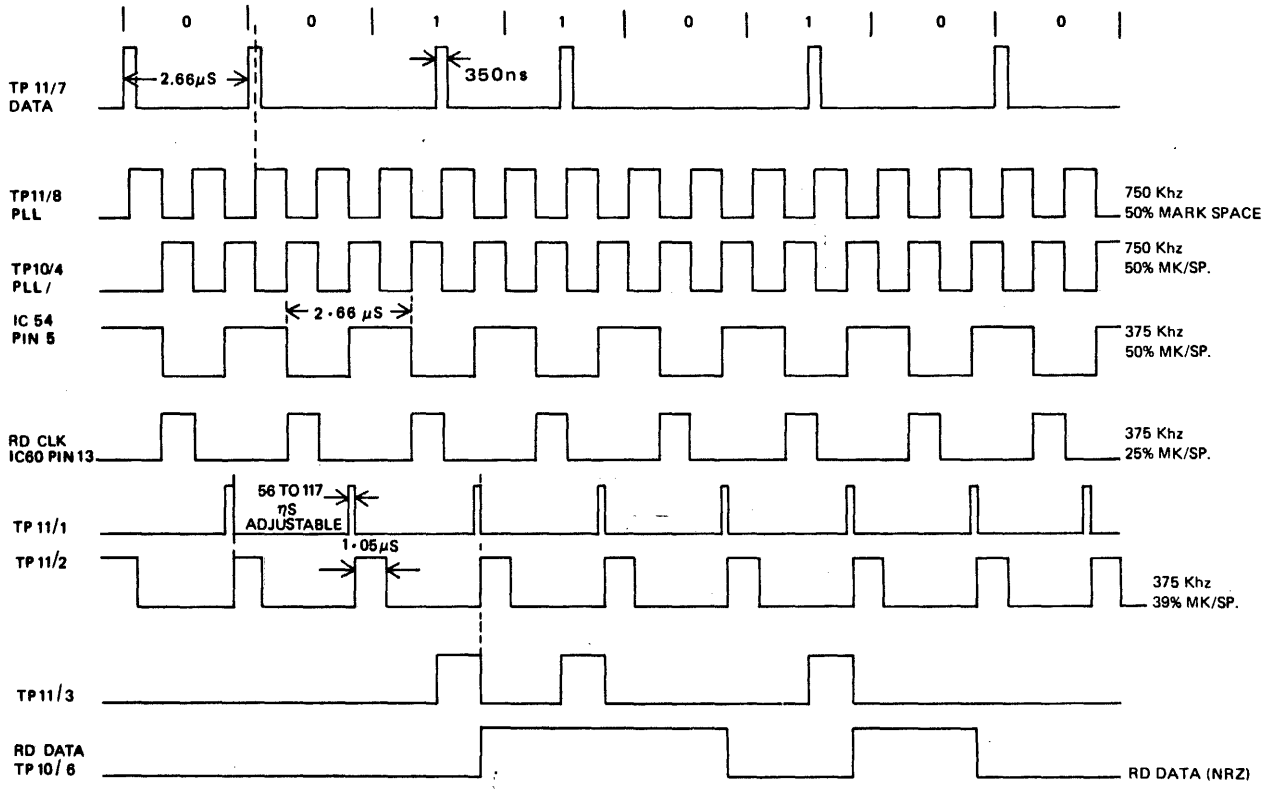


Figure 2–20. Data Decode Timing

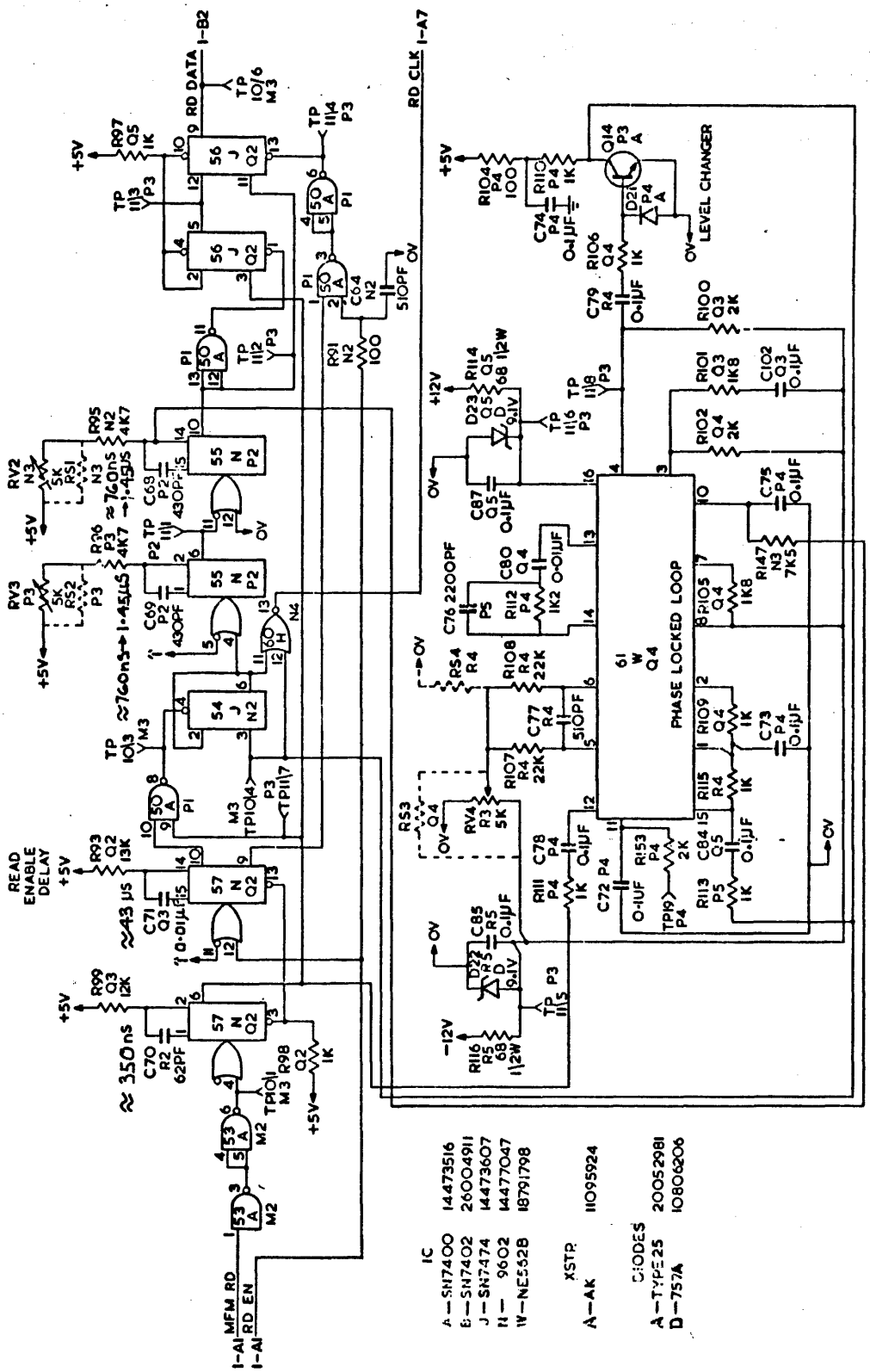


Figure 2–21. Schematic – Read Data Decode

READ CLOCK

The Read Clock is generated from the PLL, divider IC54 and gate IC60 pins 11, 12, 13. When RD EN goes true, timer IC57 pin 10 goes true for 400 μS. Data pulses occurring during this time will produce a low on IC50 pin 8 which presets flip-flop IC54. This ensures the correct phase of clock, since it is known that RD EN occurs during the preamble and the preamble consists of zeros.
Refer to Data Decode Timing Figure 2-20.
Read clock consists of a 666 μS pulse every 2.66 μS.

DATA WINDOW

The purpose of the data window is to provide a timing pulse for each bit cell.

MFM read pulses occurring during this period are taken as zeros and any pulses occurring outside are taken as ones. The mark/space ratio of the data window waveform is 39%, that is, 39% of the time is spent looking for zeros and 61% looking for ones.

This is to counteract the effect of peak shift affecting the 'ones' when a 'zero' pulse is omitted following a 'one' (see figure 2-22). Peak shift is caused by the effect of pulse crowding.

Flip-flop IC56 pin 5 is reset on the edge of every 'zero time' (TP11/2 high) and is set by a data pulse occurring during the 'ones time' (TP11/2 low). Note that the flip-flop is reset every zero time regardless of whether a data pulse occurred at that time, therefore correcting the lack of a zero pulse following a one which is characteristic of a MFM recording.

TP11/3 therefore has a pulse occurring on each one bit. Flip-flop IC56 pin 9 converts this to NRZ (see figure 2-21).

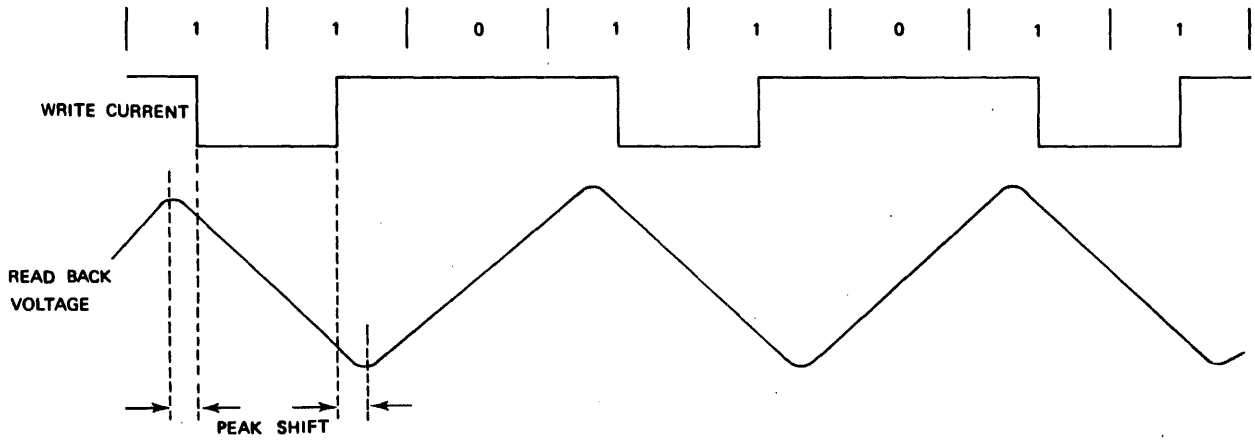


Figure 2–22. Worst Case Peak Shift

SECTION 3
CIRCUIT DETAIL

GENERAL

The type of logic used in the B9489 is Transistor-to-Transistor logic (TTL). The high level is +2 to +5 volts and the low level is +0.8 volts to 0 volts. Normally TRUE is considered as high and FALSE is low, however there are exceptions, particularly on the interface, where a low is TRUE and a high is FALSE. Such signals are generally marked (/) next to the signal name indicating that the function is active when the signal is low. On the card schematic a negation symbol (0) is used to indicate when a low activates a function. Figure 3–1 illustrates a typical exception.

The IC in figure 3–1 is triggered by a low on A or a high on B and is reset by a low on C.

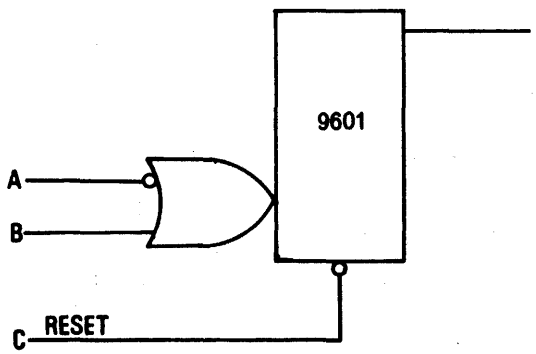


Figure 3–1. Logic Example

Table 3–1 contains a listing of modules used in the Mini Disk Drive the listing is referenced to illustrations, figure 3–2 through 3–28, in this section which provide a logic diagram of the modules.

Table 3–1. Index of Modules

FIGURE NO.	PART NO.	VENDOR NO.	DESCRIPTION
3–2	1447 3516	SN 7400	Quad 2-Input NAND Gate
3–3	2600 4911	SN 7402	Quad 2-Input NOR Gate
3–4	1447 3532	SN 7404	Hex Inverter
3–5	2600 1685	SN 7405	Hex Inverter with Open Collector Output
3–6	1447 3540	SN 7410	Triple 3-Input NAND Gate
3–7	1447 3565	SN 7420	Dual 4-Input NAND Gate
3–8	1878 9057	SN 7426	Quad 2-Input High Input Voltage Interface NAND Gate
3–9	1447 3581	SN 7438	Quad 2-Input Interface NAND Gate with Open Collector Output
3–10	2600 6726	SN 74132	Quad 2-Input NAND Gate Schmitt Triggers
3–11	2600 4929	SN 7427	Triple 3-Input NOR Gate
3–12	1879 4313	SN 75452	Dual NAND Driver
3–13	1447 3608	SN 7474	Dual D-Type Flip-Flops
3–14	1901 7102	ITT 9601 5D	Retriggerable Monostable Multivibrator
3–15	1447 7047	9602	Dual Retriggerable Monostable Multivibrator with Reset
3–16	1878 8042	8284	Hexadecimal Up/Down Counter
3–17	1446 7062	9308	Dual 4-Bit Latch
3–18	1447 3797	9322	Dual 2-Input Multiplexor
3–19	1878 8034	9324	5-Bit Comparator
3–20	2010 0582	733	Differential Amplifier
3–21	1127 2077	710	High Speed Differential Compactor
3–22	1879 1764	7496	5-Bit Shift Register
3–23	1879 1798	NE 562B	Phase Locked Loop
3–24		TIL 31 or 1A48B	Photo Emissive Diode
3–25		TIL 81 or 2B50B	Silicon Photo Transistor
3–26	1879 2127		Delay Line 300 ns
3–27	1879 4628	2N 6055 or TIP 640	High Power Transistor

Circuit Detail

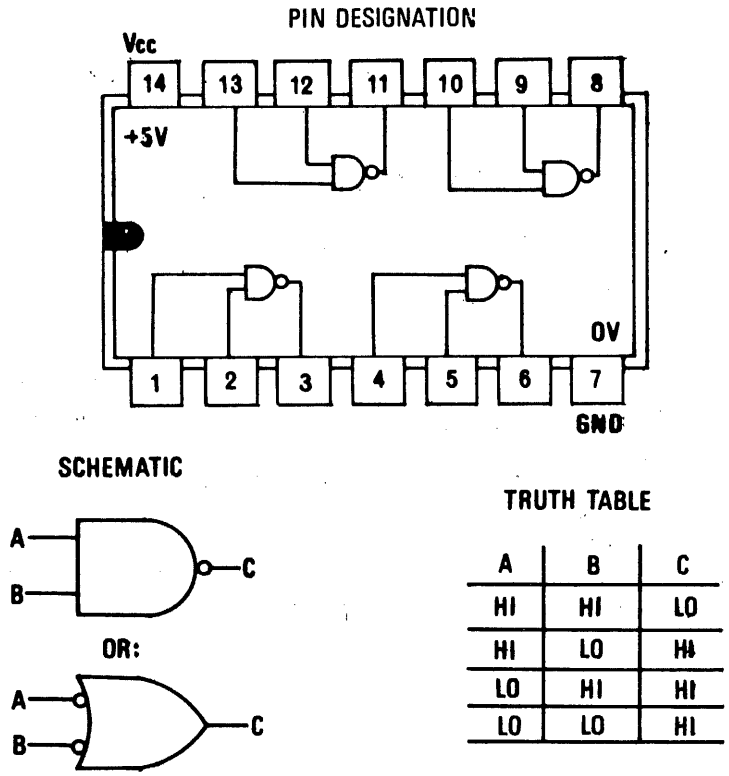


Figure 3–2. SN7400 Quad 2-Input NAND Gate

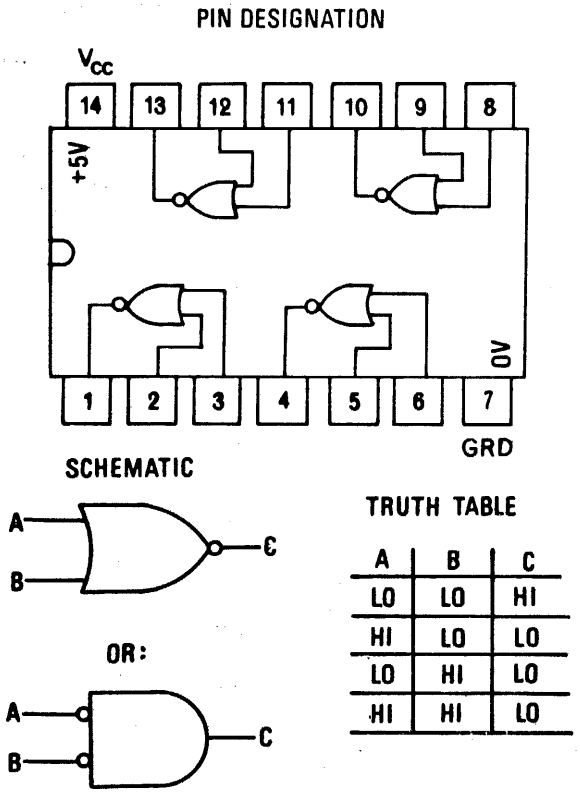


Figure 3–3. SN7402 Quad 2-Input NOR Gate

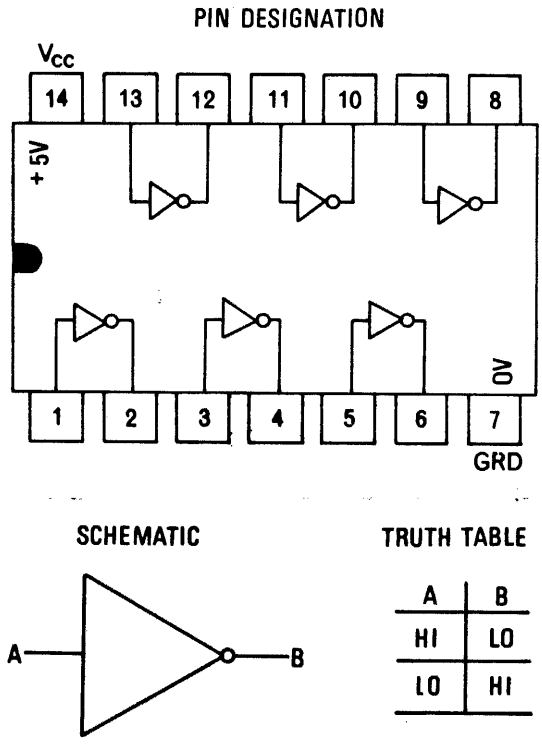
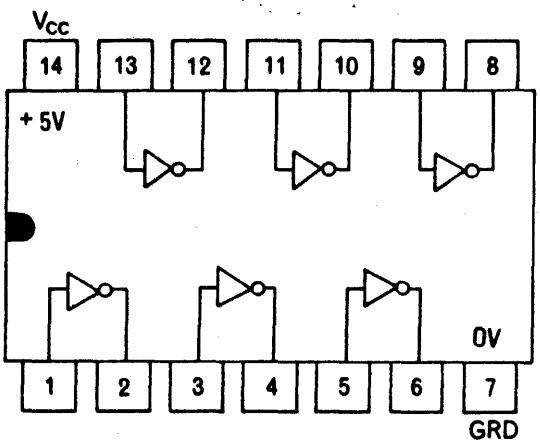


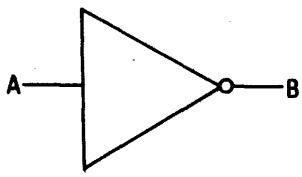
Figure 3–4. SN7404 HEX Inverter

Circuit Detail

PIN DESIGNATION



SCHEMATIC

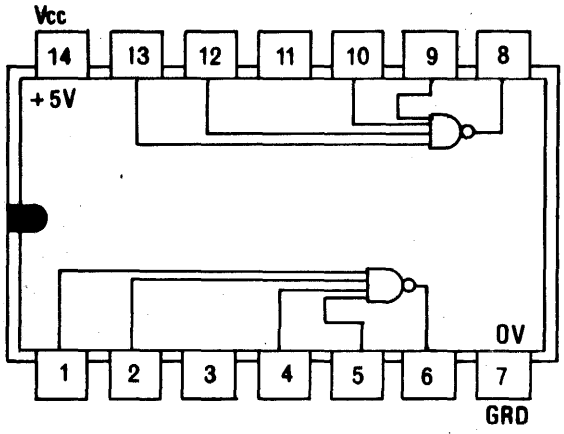


TRUTH TABLE

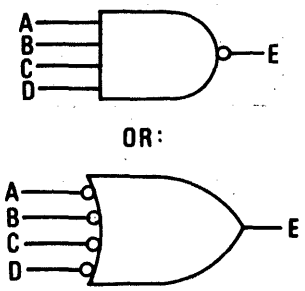
A	B
HI	LO
LO	Floating

Figure 3–5. SN7405 HEX Inverter with Open Collector Output

PIN DESIGNATION



SCHEMATIC



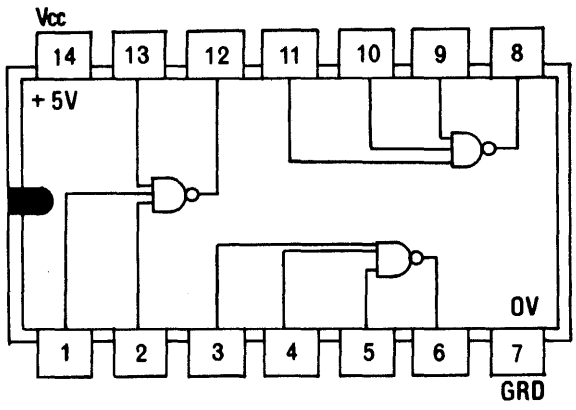
TRUTH TABLE

A	B	C	D	E
HI	HI	HI	HI	LO
LO	HI	HI	HI	HI
HI	LO	HI	HI	HI
HI	HI	LO	HI	HI
HI	HI	HI	LO	HI
LO	LO	LO	LO	HI

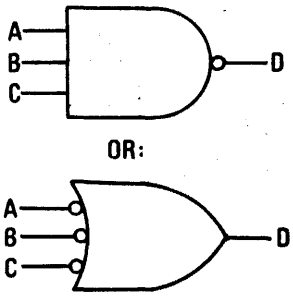
ALL HI = LO
ANY LO = HI

Figure 3–7. SN7420 Dual 4-Input NAND Gate

PIN DESIGNATION



SCHEMATIC



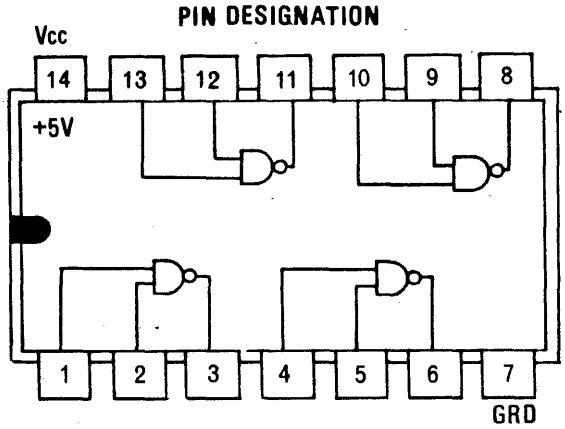
TRUTH TABLE

A	B	C	D
HI	HI	HI	LO
LO	HI	HI	HI
HI	LO	HI	HI
HI	HI	LO	HI
LO	LO	LO	HI

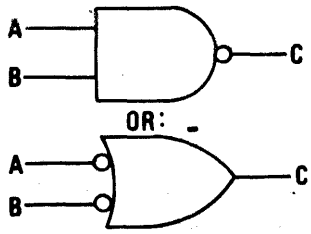
ALL HI = LO
ANY LO = HI

Figure 3–6. SN7410 Triple 3-Input NAND Gate

PIN DESIGNATION



SCHEMATIC

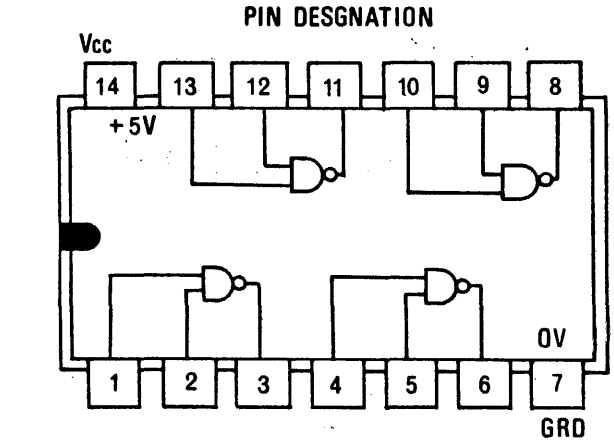


TRUTH TABLE

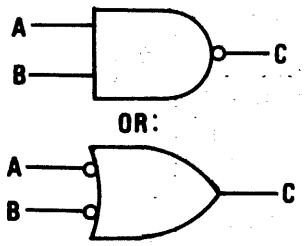
A	B	C
HI	HI	LO
HI	LO	FLOATING
LO	HI	FLOATING
LO	LO	FLOATING

Figure 3–8. SN7426 Quad 2-Input High Input Voltage Interface NAND Gate with open collector output.

Circuit Detail



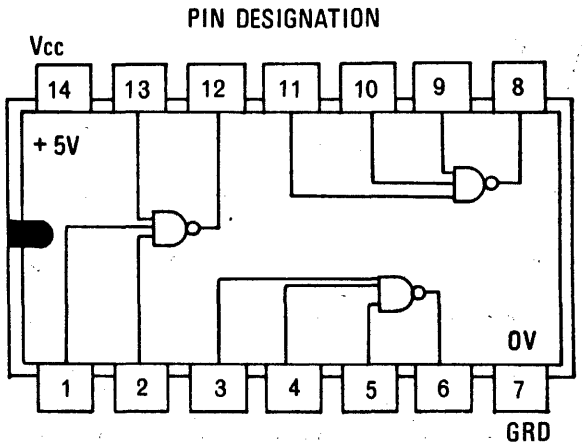
SCHEMATIC



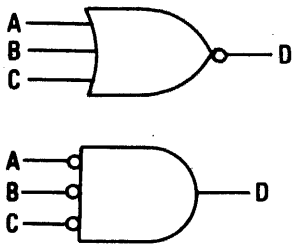
TRUTH TABLE

A	B	C
HI	HI	LO
HI	LO	Floating
LO	HI	Floating
LO	LO	Floating

Figure 3–9. SN7438 Quad 2-Input Interface NAND Gate with Open Collector Output



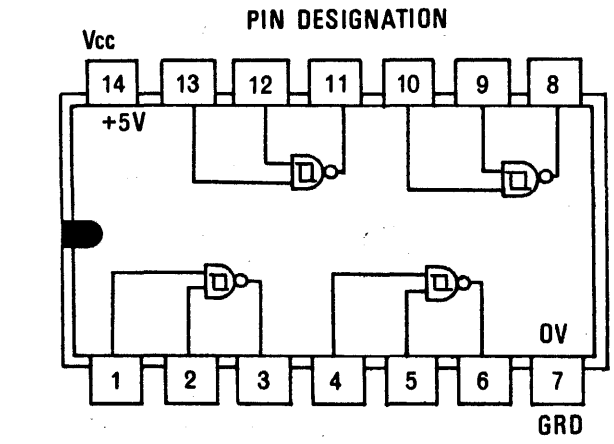
SCHEMATIC



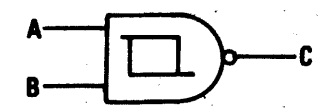
TRUTH TABLE

A	B	C	D
HI	HI	HI	LO
LO	LO	LO	HI
HI	LO	LO	LO
LO	HI	LO	LO
LO	LO	HI	LO

Figure 3–11. SN7427 Tripple 3-Input NOR Gate



SCHEMATIC

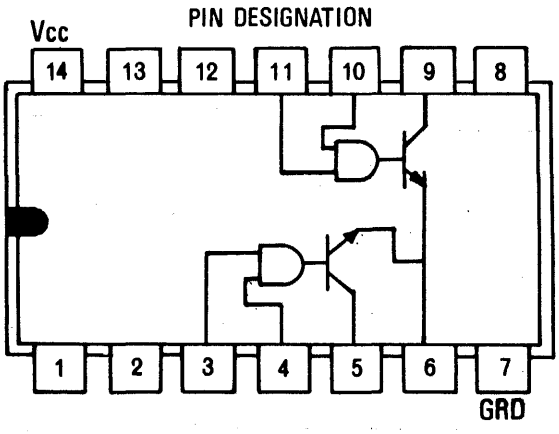


TRUTH TABLE

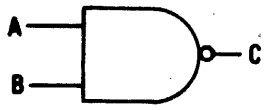
A	B	C
HI	HI	LO
HI	LO	HI
LO	HI	HI
LO	LO	HI

There is no "Grey area" with Schmitt triggers, the output goes low as soon as both inputs are above approx +1.7V and goes high if any input goes below approx +0.9V.

Figure 3–10. SN74132 Quad 2-Input NAND Gate Schmitt Triggers



SCHEMATIC



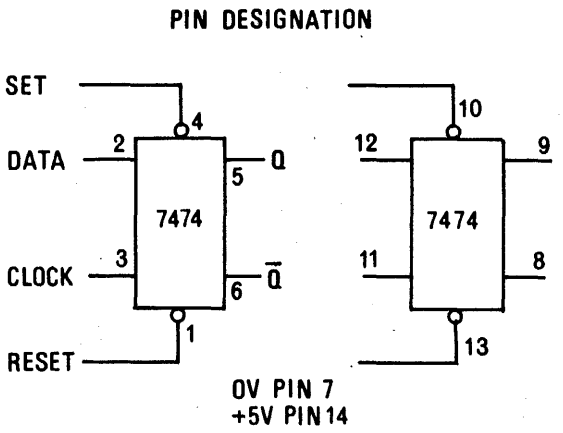
TRUTH TABLE

A	B	C
HI	HI	LO
HI	LO	HI
LO	HI	HI
LO	LO	HI

The 75452 is used to illuminate indicator lamps. Each circuit can sink 300mA to ground when either or both inputs are low.

Figure 3–12. SN75452 Dual NAND Driver

Circuit Detail



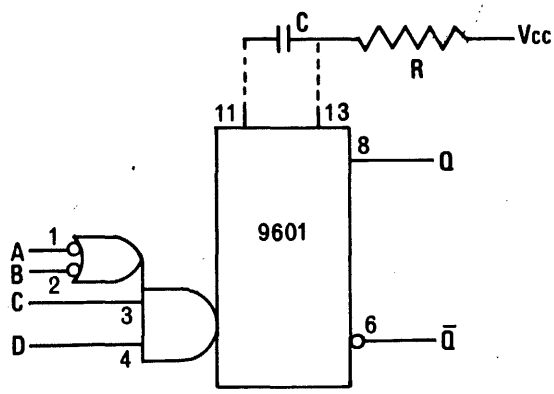
A low on "reset" resets the flip flop.

A low on "set" sets the flip flop.

The flip flop is triggered as the clock goes high, setting if Data is high, resetting if data is low.

SN7474 Dual D-type Flip Flop.

Figure 3–13. SN7474 Dual D-type Flip Flop

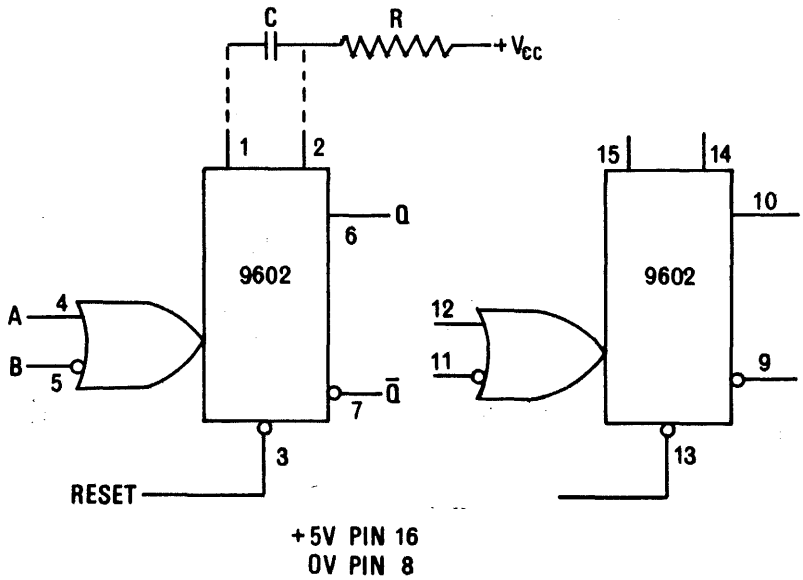


The multivibrator is triggered by (A + B) *C *D.

If the multivibrator is triggered, a high pulse occurs at Q and a low pulse occurs at Q for a period of time depending on R and C. If the timer is retriggered while it is timing out from a previous operation, the timer retriggers to give the full period pulse starting from the time of the second trigger. This may be disabled by joining Q to C or D. This prevents retriggering until the timer has timed out.

ITT9601 5D Retriggerable monostable multivibrator

Figure 3–14. ITT96015D Retriggerable Monostable Multivibrator



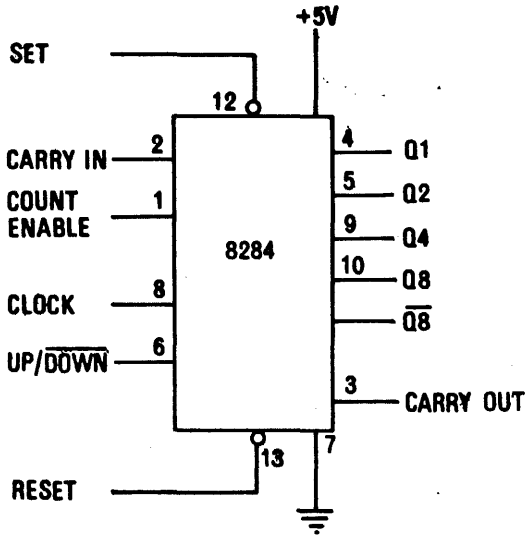
The multivibrator is triggered by a leading edge on A or a trailing edge on B. When triggered, a high pulse occurs on Q and a low pulse occurs on Q for a period of time depending on R and C.

An input pulse occuring before the timer has timed out will cause the timer to retrigger and become TRUE for the full period again.

The timer may be cut short and reset at any time by applying a low to "reset".

Figure 3–15. 9602 Dual Retriggerable, Resettable, Monostable Multivibrator.

Circuit Detail



The Hexadecimal up/down counter counts 0 through 15 and the output is 1, 2, 4 and 8 bits.

The "set" line going low sets the counter to 15.

The "reset" line going low resets the counter to 0.

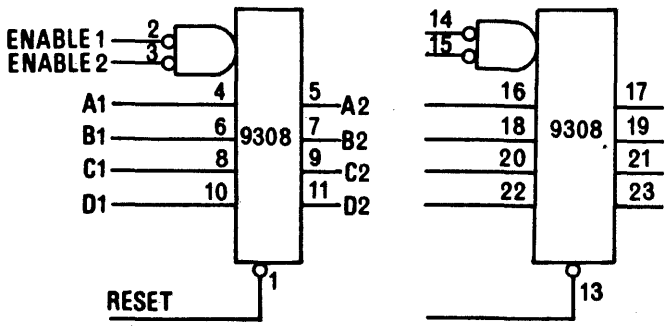
With "Carry In", "Set", "Reset" and "Count Enable" high, counting will occur on the trailing edge of each clock pulse.

The direction of counting is controlled by the signal up/down. High counts up, low counts down.

A high carry out is provided at 15 when counting up and at 0 when counting down.

To count more than 4 bits, 2 counters can be placed in series with the carryout of the first counter connected to the carry in of the second.

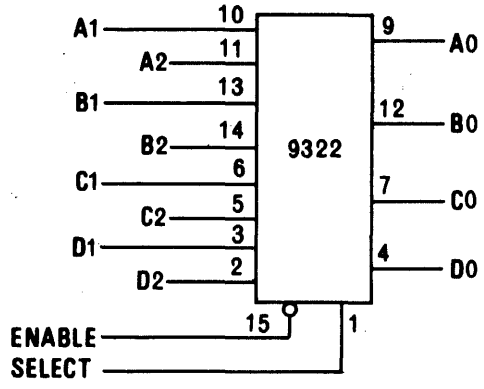
Figure 3–16. 8284 Hexadecimal Up/Down Counter



Both Enable 1 and Enable 2 must be low to latch the "2" outputs in the same state as their respective "1" inputs. If either "Enable" goes high the outputs are unaffected by the inputs.

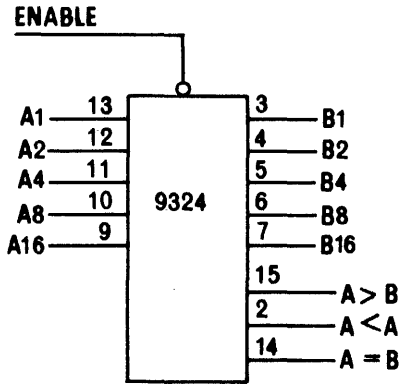
A low on "Reset" resets the 4 latches to low regardless of the enable lines.

Figure 3–17. 9308 Dual 4-bit Latch



If "Enable" goes low the "1" inputs OR "2" inputs may be gated to the "0" outputs depending on the "select" line. HIGH "select" gates the "1", LOW "select" gates the "2" inputs to the Output.

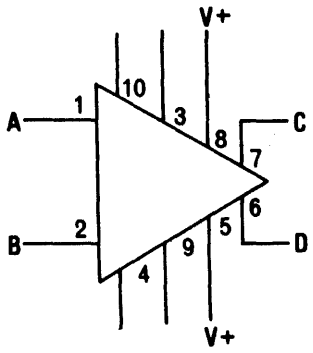
Figure 3–18. 9322 Quad 2-Input Multiplexor

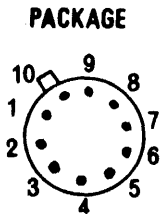


The "A" inputs are compared with "B" inputs. When "Enable" goes low, one of 3 outputs goes high, A > B, A < B or A = B, depending on the binary value of A and B.

Figure 3–19. 9324 5-Bit Comparator

Circuit Detail

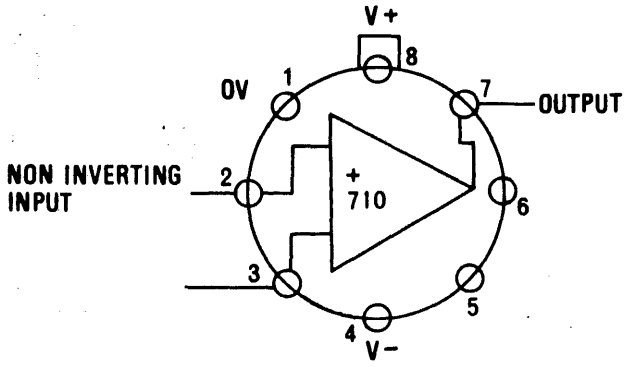




Differences in voltage AB are amplified and appear across C and D. Gains between 10 and 400 are possible by selecting resistances to be connected between pins 4 and 9 and pins 10 and 3.

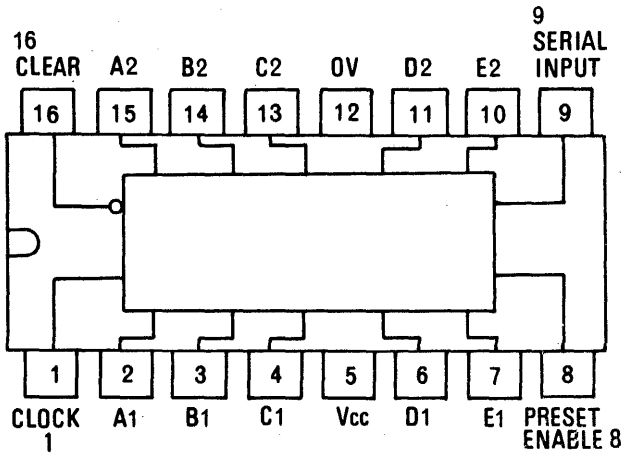
The 733 is selected for its gain stability, wide band with and low phase distortion.

Figure 3–20. 733 Differential Amplifier



The 710 is used for comparing the read voltage against a threshold. When the non-inverting input is more positive than the inverting input the output goes high (+3V). When the non-inverting input is more negative than the inverting input, the output goes low (–0.5V).

Figure 3–21. 710 High Speed Differential Comparator



The 7496 can be used as a serial to parallel converter, a parallel to serial converter or a 5 bit storage register.

A LOW on "Clear" will reset the flip flops so that A thru E2 are low provided that "Preset enable" is low.

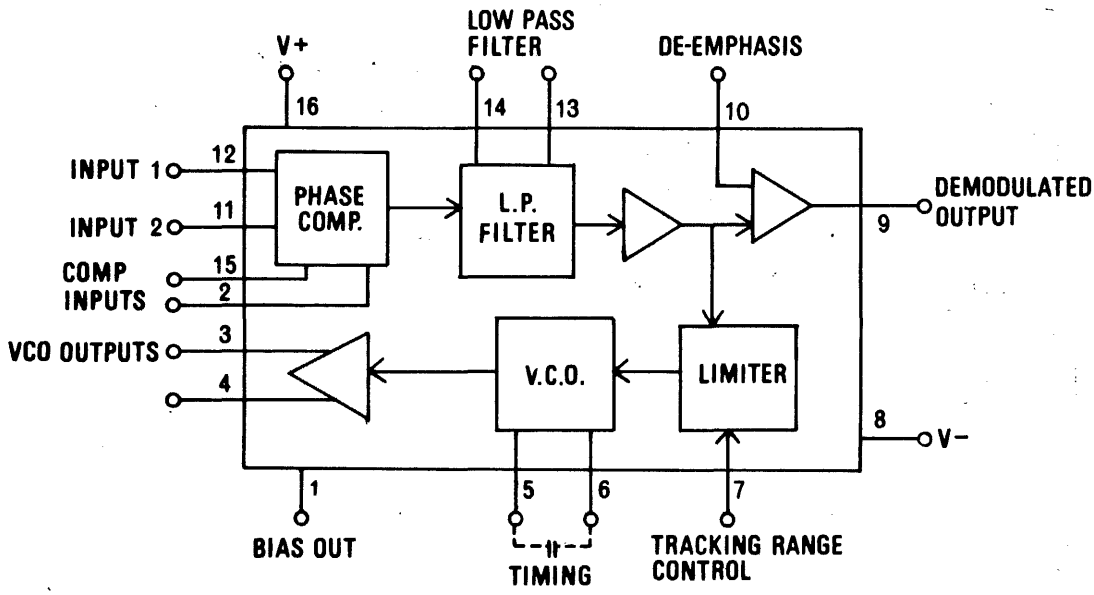
The flip flops can be preset by applying an input to A1 thru E1 and then making "Preset enable" high, provided "clear" is high. A high in sets the flip flop, a low in leaves it in its previous state.

Clear and Preset functions are independent of the clock.

The leading edge of a clock pulse will make the A2 output equal to the serial input, B2 = previous A2, C2 = previous B2, D2 = previous C2 and E2 = previous D2. Previous E2 is lost. When used in this mode, "clear" must be high and "preset enable" must be low.

Figure 3–22. 7496 5-Bit Shift Register

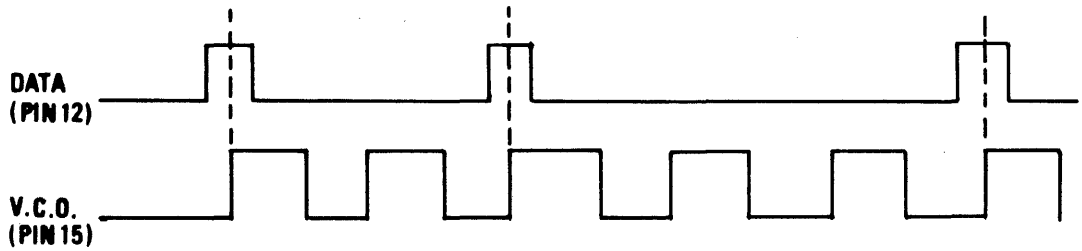
Circuit Detail



The purpose of the Phase Locked Loop is to provide an oscillator whose output Frequency is 2 times the frequency of bits being read off the disk and is locked onto the data, that is the oscillator must respond to variation in speed of the bits from the disk. This is used to generate clock pulses, data windows etc, during read.

Refer to the block diagram. The IC contains 2 sections:

1. Voltage controlled oscillator (V.C.O).
   The centre frequency of the oscillator is determined by the capacitance and voltage between pins 5 and 6. It can be further modified up to ±15% internally by the output of the Phase Comparator via the limiter.
2. Phase Comparator.
   Only 2 inputs of the phase comparator are used the other 2 being AC coupled to general. One input has data bits, the other is wired externally to the output of the V.C.O. The phase compensator adjusts the speed of the V.C.O. so that the V.C.O. transitions occur in the centre of the data input as illustrated in the timing diagram.

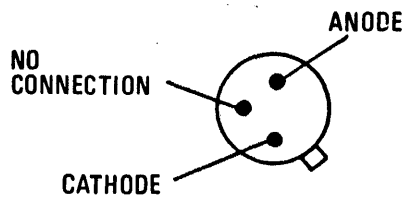


The speed of response is determined by the components across the low pass filter, pins 14 & 13. De-emphasis input and demodulated output are not used in the mini disk application. The tracking range control is tied to one value.

Pin 1 provides a bias voltage of +8V regulated output.

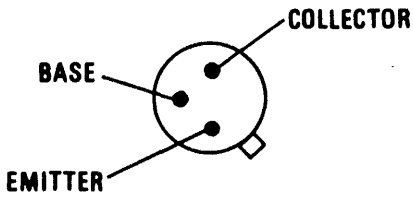
Figure 3–23. NE 562B Phase Locked Loop

Circuit Detail

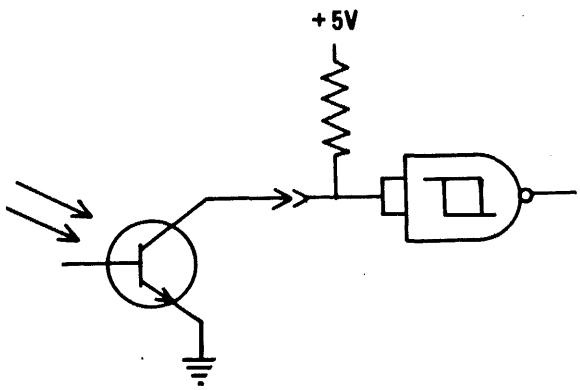


When forward biased, this diode emits infra-red radiation. Forward voltage drop is 1.8 volts max, forward current is 100 Ma. (approx).

Figure 3–24. TIL 31 or 1A48B Photo Emissive Diode.

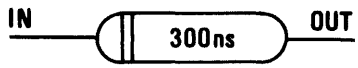


This device is a Silicon phototransistor. A lens in the cap of the device provides for high sensitivity.



When the infra-red light source shines on the lens, the transistor switches on giving a low level into the circuit. With no light the transistor is off, giving a high level in.

Figure 3–25. TIL 81 or 2B50B Silicon Photo Transistor



The delay line is an LC Network which delays any input pulse or AC waveform by 300 nano seconds.

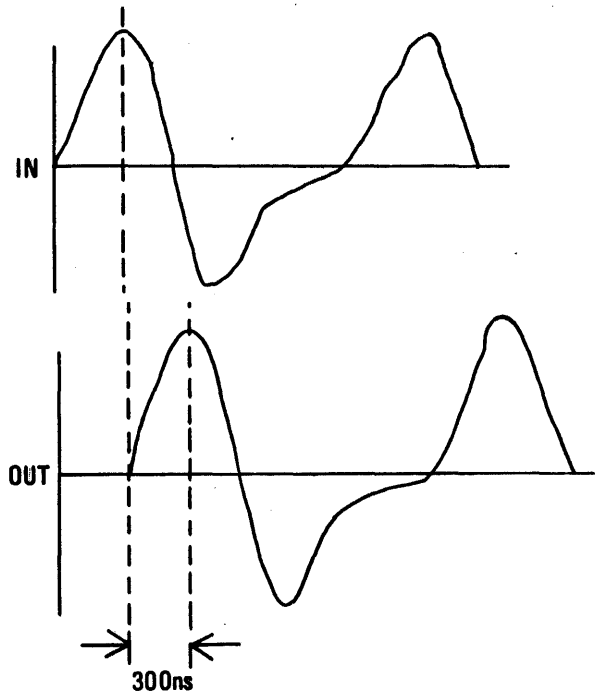
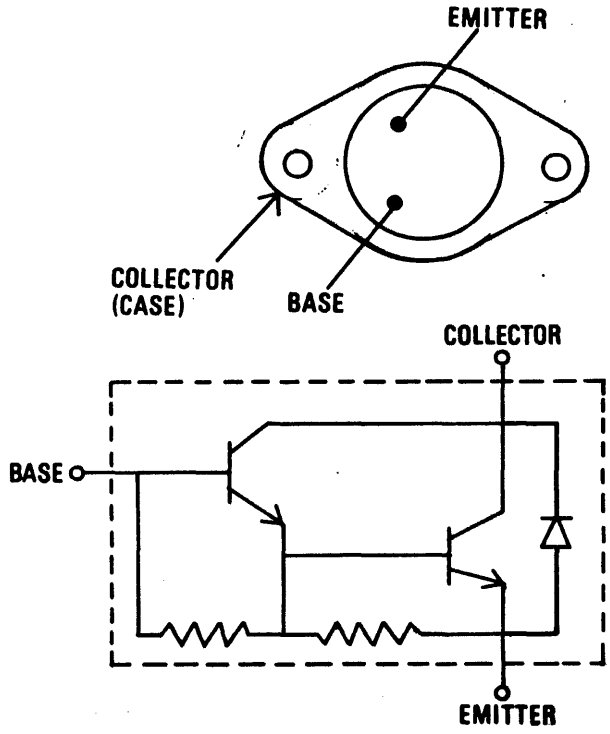


Figure 3–26. Delay line 300ns



This device is a high power Darlington NPN transistor for switching unclamped inductive loads.

Figure 3–27. High Power Transistor 2N6055 or TIP 640

SECTION 4
ADJUSTMENTS

INTRODUCTION

This section contains the test and adjustment procedures for the 9489 1 M BYTE Mini Disk Drive Unit. Some adjustments may be carried out using an oscilloscope, DTM 1000 or BDM 1250 as detailed.

All adjustments are factory set and ideally should NOT require re-adjustment unless parts have been disturbed or replaced. Verify that any adjustment is absolutely necessary before doing so.

SPECIAL TOOLS

The following special tools are required:

1880 7883 Alignment Disk.
1880 7917 Alignment Meter.
1880 7909 Stepper Motor Adjusting Tool.
1880 7891 Upper Head Adjusting Tool.

ALIGNMENT DISK

The alignment disk absorbs moisture from or releases moisture to the atmosphere depending upon the relative humidity of the atmosphere. This affects the accuracy of the alignment disk. For this reason, the alignment disk is written in a controlled environment (50% RH and 70° F or 20 ° C). The disk is sealed in a special container until required for use. Once the container is opened the alignment disk is only accurate for 6 minutes. Track to track alignment of the lower head must be performed within 6 minutes. After this time the alignment disk is known as an "alignment check disk" and may be used for all other adjustments requiring an "alignment check disk".

If the alignment disk is opened in a controlled environment (45% ± 5% RH and 68° F ± 5 ° F or 20 ° C ± 0.5 ° C) and never removed from that environment the 6 minutes time limit does not apply and the alignment disk may be used to perform track to track alignment of the lower head for a maximum of 5 times. It may also be used to perform all adjustments requiring an alignment check disk.

B 80 HEX KEYBOARD COLLATED TABLE

Certain options of the B 80 MTR require binary input for cylinder addresses and data.

This binary data may be entered 4 bits at a time by using the right-hand numeric keyboard on the B 80 console, as follows:

Table 4-1.

KEY SYMBOL	BINARY INPUT	HEX EQUIVALENT
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
00	1010	A
000	1011	B
C	1100	C
RE	1101	D
M	1110	E
	1111	F

ALIGNMENT TRACK SELECTION USING B 80 MTR

1. Select option 06 by depressing control keys PK5 and PK15.
2. When the MTR asks for the cylinder address, enter the required code from the table 4-2 using the console right-hand key board.
3. MTR option 06 continuously seeks between two addresses. When each cylinder address is indexed twice the mini-disk heads will remain at that address and the stepper motor will have seek pulses applied to it.

Table 4-2.

ALIGNMENT TRACK	KEY SYMBOLS HEAD 0	KEY SYMBOLS HEAD 1	HEX EQUIVALENT HEAD 0	HEX EQUIVALENT HEAD 1
0	0/0/0/0	0/0/2/0	0000	0020
1	0/0/4/0	0/0/6/0	0040	0060
2	0/0/8/0	0/0/00/0	0080	00A0
5	0/1/4/0	0/1/5/0	0140	0150
31		0/7/M/0		07E0
34		0/8/00/0		08A0
37		0/9/6/0		0960
40	0/00/0/0	0/00/2/0	0A00	0A20
43		0/00/M/0		0AE0
46		0/000/00/0		0BA0
49		0/C/6/0		0C60
52		0/RE/2/0		0D20
55		0/RE/M/0		0DE0
61	0/./4/0		0F40	

Alignment Meter Operating Instructions

For a full description of the meter operation see the media package supplied with the meter.

1. Check that the meter is set for the correct supply voltage and power up by connecting the line cord.
2. Allow the meter to stabilize for one hour.
3. Check the operation of the meter as follows.
   a. Connect the head plug to the calibrated socket and observe that the tri-bits present indicator is illuminated continously and that the meter is reading zero.
   (If the meter does not read zero, adjust the set zero control until the meter reading is zero).
   b. Switch the meter range to X10.
   c. Switch the calibrator offset to 0.001 inch.
   d. Move the calibrator switch to right and then left. Check that the meter swings both ways and reads 100 $\pm$ 10 each time.
   e. Switch meter range to X1.
   f. Switch calibrator offset to 100 μ inches.
   g. Move the calibrator switch to right then left. Check that the meter swings both ways and reads 100 $\pm$ 10 each time.

Adjustments

Backlash Nut Adjustment

This adjustment should only be required when the carriage block is removed or replaced.

The backlash nut pre-loads the carriage block against the lead screw of the positioner. If the backlash nut is set too slack, the positioner will have too much backlash. If the backlash nut is set too tight, the positioner will have too much friction. Either of these conditions can cause mispositioning of the heads.

The clearance between the backlash nut and the rear bush of the carriage block must be 0.03 to 0.06 inches.

Refer to figure 4-1.

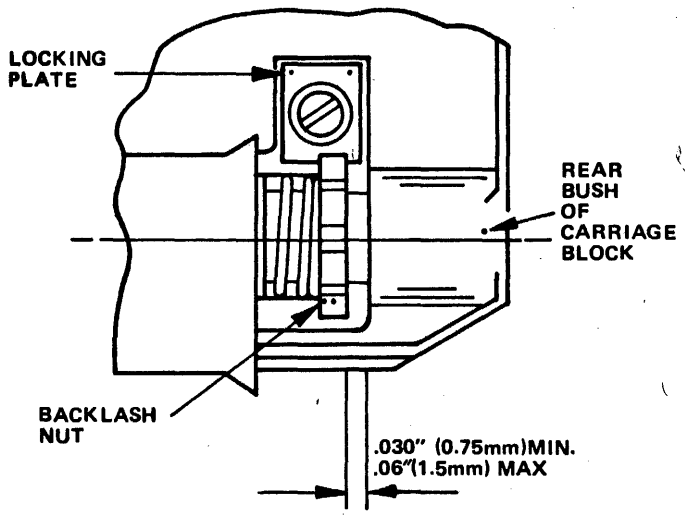


Figure 4-1. Backlash Nut Adjustment

Adjustment

1. Loosen the locking plate adjusting screw and slide the locking plate clear of the backlash nut.
2. Turn the backlash nut until there is a clearance of 0.03 – 0.06 inches between the backlash nut and the rear bush of the carriage block.
3. Insert the locking plate into a notch on the backlash nut.
4. Check the clearance between the locking plate and the bottom of the notch.

5. The minimum clearance between the locking plate and the bottom of the notch should be 0.02 inches. If not repeat steps 1 to 4 inclusive. Refer to figure 4-2.
6. Tighten the locking plate retaining screw.
7. Carry out the track to track alignment adjustment.

NOTE

Too much backlash will result in a noisy positioner, especially on single track seeks. Too much friction will cause the positioner to miss steps and/or buzz on track. After this adjustment the track to track alignment must be re-adjusted.

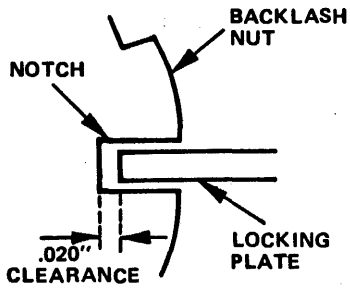


Figure 4–2. Locking Plate Clearance

Track to Track Alignment Check

When checking or performing track to track alignment the stepper motor must have pulses applied to it. These pulses ensure that the lead screw is electrically detented and will rotate when the stepper motor is rotated. In order to pulse the stepper motor, the drive must have seek pulses applied continuously. (For B 80 use, the MTR Option 06 must be used. This option continuously seeks between two addresses. If the same address is indexed twice, the mini-disk heads will remain at that address and the stepper motor will have pulses applied).

It is important not to connect or disconnect head leads while the alignment disk is in the unit otherwise degradation of the media will result.

NOTE 1

If the tri-bit present indicator is flashing on and off it is due to either:

1. Disk insertion error, or
2. Bad alignment disk, or
3. Pressure pad incorrectly aligned.

Check

Refer to Track to Track Alignment Check.

1. Check the alignment meter calibration as detailed under "Alignment Meter Operating Instructions".
2. Connect the alignment meter head lead into the lower head socket (CONN 6) of the unit.
3. Insert an alignment check disk into the unit with the label away from the blue release bar.
4. Seek track 00 Head 1. (Refer to Alignment Track Selection using B 80 MTR).
5. Seek track 43 head 1 and continue sending seeks to this address (Refer to Alignment Track Selection using B 80 MTR).
6. Note the meter reading. (If it is greater than 1500u inches then head 1 should be realigned as described under 'Track to Track Alignment Adjustment).
7. Remove the alignment check disk.
8. Connect the alignment meter head lead into the upper socket (Conn 7) of the unit.
9. Re-insert the alignment check disk with the label towards the blue release bar.
10. Seek track 00 head 0. (Refer to Alignment Track Selection using B 80 MTR).
11. Seek track 61 head 0 and continue sending seeks to this address. (Refer to Alignment Track Selection using B 80 MTR).
12. The meter reading should be within + 500 μ inches of that noted in Step 6 and of the opposite polarity.
13. If the meter reading is outside this range then Head 0 must be realigned as described under "Track to Track Alignment Adjustment".
14. Return the alignment check disk to its storage envelope.
15. Reconnect the head leads onto the PCB.

Track to Track Alignment Adjustment

This adjustment should only be required if one or more of the following are performed –

1. The carriage block is removed or replaced.
2. The stepper motor is removed or replaced.
3. The upper head is removed or replaced.
4. The spindle is removed or replaced.
5. The backlash nut is adjusted.

Track to Track Alignment

To overcome friction in the carriage block/lead screw/stepper motor, it is advisable to seek track 00 and back to the alignment track each time the stepper motor or upper head arm is moved. This is achieved by grounding TP5/4 and then removing the ground. (The up to speed signal UTSF goes low

while the ground is applied. When the ground is removed the drive will recalibrate to track 00). (However, the B 80 MTR is designed to loop on the failing instruction and will continue to send seek pulses to the selected address. The first time the ground is applied the B 80 will print a failure code).

The stepper motor adjustments can be more easily performed if there is grease on the face of the stepper motor in contact with the base plate. This will be required on some older units and on all units when a new stepper motor is fitted.

The steps requiring the use of the alignment disk unit must be performed within 6 minutes of opening the alignment disk package.

Adjustment

Refer to Track to Track Alignment.

1. Adjust the backlash nut as described under "Backlash Nut Adjustment".
2. The drive must be allowed to stabilize for 1 hour. Insert a disk, initialize it and then seek between tracks 00 and 85 for 1 hour. During this time the alignment meter must be switched on to allow it to stabilize. The alignment disk must be allowed to temperature stabilize by keeping it sealed in its container in the same room as the unit.
3. Check the alignment meter calibration as described under "Alignment Meter Instructions".

Head 1 Adjustment

(Using Alignment Check Disk).

4. Connect the alignment meter head lead into the lower socket (Conn 6) of the unit.
5. Install the stepper motor adjusting tool (P/N 1880 7909) onto the body of the stepper motor. (This can be done easily by removing the tool handle first).
6. Insert the alignment check disk (NOT the sealed disk) into the unit with the label away from the blue release bar.
7. Seek track 00, Head 1. (Refer to Alignment Track Selection using B 80 MTR).
8. Seek track 43, head 1 and continue sending seeks to this address. (Refer to Alignment Track Selection using B 80 MTR).
9. Slacken off the stepper motor clamp screws sufficiently to be just able to rotate the motor body when using the stepper motor adjusting tool.
10. Rotate the stepper motor in either direction (that is, clockwise and counter clockwise) until the tri-bits present indicator illuminates.
11. Looking from the rear of the unit, rotate the stepper motor clockwise until the tri-bits present indicator is extinguished.
12. Rotate the stepper motor slowly counter-clockwise until the tri-bits present indicator illuminates (the light must remain on continuously, and not flashing). Refer to Notes 1 and 2.
13. Continue rotating the stepper motor until a reading of $\pm$ 140 μ inches is obtained on the alignment meter. Frequently seek track 00 and back to track 43 while making this adjustment.
14. Tighten the stepper motor clamp screws progressively to 10 lb inches.
15. Seek to track 00 and then back to track 43, Head 1. (Refer to Alignment Track Selection using B 80 MTR).
16. Check that the tri-bits present indicator is illuminated and that a meter reading of $\pm$ 140 μ is obtained.
17. Repeat steps 15 and 16 several times and ensure that the conditions in step 16 are met every time. (If not repeat steps 7 to 17 inclusive).
18. Remove the stepper motor adjusting tool and the alignment check disk.

NOTE 2

When a seek is performed to track 00 and back to track 43 the tri-bits present indicator may not light. If the indicator does not light, the track 00 transducer requires adjustment. Proceed as follows:

a. Seek track 00, Head 1
b. Seek track 43, Head 1
c. Rotate the stepper motor until the tri-bits present indicator lights.
d. Clamp the stepper motor and adjust the track 00 transducer as described "Under Track 00 Adjustment".
e. After adjusting the track 00 transducer carry out the "track to track alignment adjustment" from step 6.

Head 0 Adjustment (Using Alignment Check Disk)

19. Fit the upper head adjusting tool P/N 1880 7891. (Turn adjusting screw into the upper head arm to allow recalibration when disk is put into the drive).
20. Connect the alignment meter head lead into the upper head socket (CONN. 7) of the unit.
21. Slacken the two upper head arm retaining screws nearest to the head. (The screws should be slackened just sufficiently to allow the upper head arm to be moved with finger pressure).
22. Insert the alignment check disk (not the sealed disk) with the label towards the blue release bar.

23. Seek track 00, Head 0. (Refer to Alignment Track Selection using B 80 MTR).
24. Seek track 61, Head 0 and continue sending seeks to this address. (Refer to Alignment Track Selection using B 80 MTR).
25. Move the upper head arm backwards and forwards by hand until the tri-bits present indicator is illuminated.
26. Move the upper head arm towards the rear of the unit until the tri-bits present indicator is extinguished.
27. Using the upper head adjusting tool (P/N 1880 7891) move the upper head arm SLOWLY towards the front of the unit until the tri-bits present indicator is illuminated. (The light must remain on continuously, and not flashing).
28. Continue moving the upper head arm until a meter reading of $\pm$ 140 μ inches is obtained. (Frequently seek track 00 and back to track 61 whilst making this adjustment).
29. Tighten the two retaining screws progressively to 6lb inches.
30. Seek track 00 and back to track 61, Head 0 (Refer to Alignment Track Selection using B 80 MTR).
31. Check that the tri-bits present indicator is illuminated and that a meter reading of $\pm$ 140 μ inches is obtained.
32. Repeat steps 30 and 31 several times and ensure that the conditions in step 31 are met every time. If not repeat steps 22 to 32 inclusive.
33. Remove the alignment check disk and upper head adjusting tool.
34. Reconnect the head leads onto the PCB.

NOTE

The upper head is now aligned to the lower head within 300 μ inches. Before continuing with the sealed alignment disk carry out a circumferential alignment check.

NOTE

The lower head must now be accurately aligned using the sealed alignment disk (P/N 1880 7883). Ensure that you are ready to perform the adjustment before opening the sealed package. Once the package has been opened the alignment must be performed within 6 minutes.

Head 1 Fine Adjustment (Using Sealed Alignment Disk)

35. Connect the alignment meter head lead into the lower head socket (CONN. 6) of the unit.
36. Install the stepper motor adjusting tool (P/N 1880 7909) onto the body of the stepper motor.
37. Remove the alignment disk from its sealed container and insert it into the unit with the label away from the blue release bar.
38. Carry out steps 7 to 17 inclusive within 6 minutes
39. Remove the alignment disk. (This disk may now be used as an alignment check disk and the label should be marked with a felt tipped pen to that effect).
40. Remove the stepper motor adjusting tool.
41. Reconnect the head leads onto the PCB.
42. Carry out a circumferential alignment.

Circumferential Alignment

This adjustment compensates for the mechanical tolerance between the index/sector transducer and the recording heads. (The procedure sets the interval between the start of an accurately recorded data burst and the next sector output from the index/sector decode circuit).

This adjustment should only be required if

1. The carriage block is replaced.
2. The upper head is replaced.
3. The stepper motor is replaced.
4. The spindle is replaced.
5. The backlash nut is adjusted.
6. Head 0 has been adjusted.
7. The index/sector transducer or light source is moved or replaced.
8. Any part of the index/sector delay monostable circuit is replaced.

Adjustment: Oscilloscope

1. Insert the alignment check disk (NOT a sealed disk) with the label towards the release bar.
2. Set the oscilloscope up as follows:

CHANNEL A	50 m VOLT/DIV - AC Coupled
CHANNEL B	2 VOLT/DIV - DC Coupled
ADD MODE	
TIMEBASE	20μ sec/div
EXTERNAL TRIGGER	TP 15 (DATA)

3. Connect the oscilloscope as follows

CHANNEL	TEST POINT
A	TP 15
B	TP8/4(SECTOR)

4. Seek track 40, head 0 (refer to Alignment Track Selection using B 80 MTR).
The waveform displayed should be as shown in figure 4-3.

5. Seek track 40, head 1 (refer to Alignment Track Selection using B 80 MTR). The waveform displayed should be as shown in figure 4-3.
6. The waveforms from both heads should be equidistant about 150 usec and within the range 150 ± 24 μsec.
7. Adjust RV1 until the sector pulse is 150 ± 24 μsec from the start of the data burst for each head.
8. If the adjustments for steps 4 to 7 cannot be achieved then the upper head arm should be realigned as detailed under Track to Track Alignment.

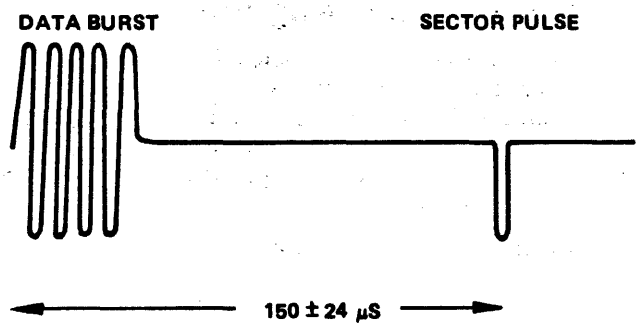


Figure 4-3. Oscilloscope Wave Forms

Adjustment: DTM 1000

1. Insert the alignment check disk (NOT a sealed disk) with the label towards the release bar.
2. Connect a 30 K ohm jumper resistor from +5 volts to the test point at the IC8 end of Capacitor C18. Refer to figure 4-4.

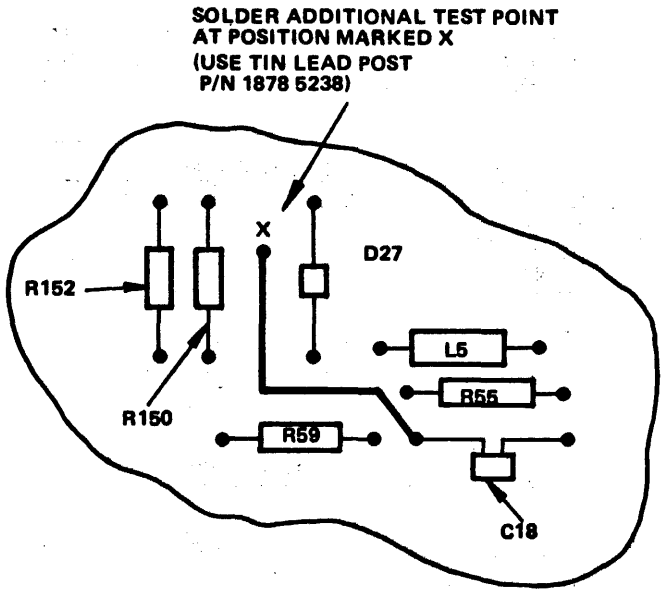


Figure 4-4. Component Layout Showing the Position of Recommended Test Point

3. Set up the DTM 1000 as follows

PROBE	TEST POINT	SLOPE
B	IC6 Pin 4 (location K1)	+ve
C	TP8/4 (Sector) (location J7)	+ve
FUNCTION:"INTERVAL BC"		

4. Seek track 40, head 0 and note the meter reading (refer to Alignment Track Selection using B 80 MTR).
5. Seek track 40, head 1 and note the meter reading (refer to Alignment Track Selection using B 80 MTR).
6. Adjust RV1 until the meter readings obtained from both heads are equidistant about 150μsec and within the range of 150 ± 24 μsec.
7. If the adjustment for steps 4 to 6 cannot be achieved then the upper head arm should be realigned as detailed under Track to Track Alignment.

NOTE

To aid future circumferential alignment adjustments using the DTM 1000 or BDM 1250 it is recommended that a test point be soldered on the track leading from Capacitor C18, at the point marked X, between resistor R150 and diode D27 (refer to figure 4-4). A 30K ohm jumper resistor can then be connected between this test point and the +5 volt line as per step 2 of the adjustment procedure. For the test point use tin lead post P/N 1878 5238.

Adjustment: BDM 1250

1. Insert the alignment check disk (NOT a sealed disk) with the label towards the release bar.
2. Connect a 30K ohm jumper resistor from +5 volts to the test point at the IC8 end of capacitor C18. (Refer to figure 4-4).
3. Set up the BDM 1250 as follows

PROBE	TEST POINT	SLOPE
B	IC6 Pin 4 (location K1)	+ve
C	TP8/4 (Sector) (Location J7)	+ve
FUNCTION: "TIME B→C"		

4. Seek track 40, head 0 and note the meter reading (refer to Alignment Track Selection using B 80 MTR).
5. Seek track 40, head 1 and note the meter reading (refer to Alignment Track Selection using B 80 MTR).

6. Adjust RV1 until the meter readings obtained from both heads are equidistant about 150 μsec and within the range 150 $\pm$ 24 μsec.
7. If the adjustment for steps 4 to 6 cannot be achieved then the upper head arm should be realigned as detailed under Track to Track Alignment.

Track 00 Adjustment:

The track 00 transducer defines the position of track 00. One phase of the stepper motor is assigned as the track 00 phase. Any incorrect adjustment of the track 00 transducer will cause a position error which is a multiple of 3 tracks away from the required track.

The adjustment should only be required if:

1. The carriage block is replaced.
2. The upper head is replaced.
3. The lower head is realigned.
4. The stepper motor is replaced.
5. The spindle is replaced.
6. The backlash nut is adjusted.
7. The track 00 transducer PCB is replaced.
8. Any part of the track 00 circuit is replaced.

NOTE

If any of the items (1) through (6) are performed, the Track to Track Alignment must be checked before adjusting the track 00 transducer.

NOTE

When making any adjustments make sure that the vane can pass through the transducer without touching it.

Adjustment

1. Check the alignment meter calibration as detailed under "Alignment Meter Operating Instructions".
2. Connect the alignment meter head lead into the lower head socket. (Conn. 6) of the unit.
3. Insert an alignment check disk into the unit with the label away from the blue release bar.
4. Seek Track 43, Head 1 (refer to Alignment Track Selection using B 80 MTR).
5. Check that the tri-bits present indicator is illuminated. If tri-bits are present go to step 9. If tri-bits are not present go to step 6.
6. Seek the following tracks until tri-bits are present – 46, 40, 49, 37, 52, 34, 55, 31 (refer to Alignment Track Selection using B 80 MTR). Loosen the mounting screws of the track 00 transducer PCB. If tri-bits are present at a track higher than 43 move the track 00 transducer PCB towards the spindle. If tri-bits are present at a track lower than 43, move the track 00 transducer PCB away from the spindle.
7. Tighten the mounting screws.
8. Seek Track 00 (refer to Alignment Track Selection using B 80 MTR) and then go to step 4.
9. Alternately seek between track 02 and track 01 (refer to Alignment Track Selection using B 80 MTR).
10. DTM 1000 or BDM 1250.
    Set up the DTM 1000 or BDM 1250 as follows:

PROBE	TEST POINT	SLOPE
A	TP 6/6	–VE
FUNCTION: WIDTH		

Oscilloscope
Set up the oscilloscope as follows:

PROBE	TEST POINT	SLOPE
A	TP 6/6	–VE
AMPLITUDE	2 VOLT/DIV	
TIMEBASE	0.5 ms/DIV	
TRIGGER	CHANNEL A	

11. Check for a negative going pulse width of between 2.5 ms to 3.0 ms at TP 6/6.
    a. If the pulse width is less than 2.5ms loosen the PCB mounting screws and move the PCB by a small amount towards the spindle.
    b. If the pulse width is greater than 3ms loosen the PCB mounting screws and move the PCB by a small amount away from the spindle.
12. Tighten the PCB mounting screws.
13. Seek from track 00 to track 43 at least five times, checking for tri-bits at track 43 each time (refer to Alignment Track Selection using B 80 MTR).
14. If the tri-bit present indicator does not illuminate at track 43, then repeat the adjustment procedure.

Phase Locked Loop and Data Windows

These adjustments are required to provide the correct RD CLK, and data windows for data decoding.

NOTE

These adjustments are required if any of the components on sheet 2 of the master drive Test and Field documents are replaced (except IC 53, IC 57 and their related components).

NOTE

On units below S/N B200450-018 the value of C75 must be changed before adjusting the PLL. Replace C75 with a 1000 pF capacitor P/N 1877 1618.

NOTE
On units below S/N B205950-018 (Glenrothes) and S/N 15165236 (Guadalajara) LIN 2141-010 must be fitted after the replacement of the phase locked loop (PLL) IC, before the adjustments can be carried out.

Phase Locked Loop Adjustment

Oscilloscope

1. Insert the alignment check disk (NOT a sealed disk) with the label towards the release bar, into the master drive.
2. Seek track 05, either head and read continuously. (Refer to Alignment Track Selection using B 80 MTR).
3. Connect the oscilloscope as follows:

PROBE	TEST POINT
A	IC61 (PLL) end of C75 *
CHANNEL A	1 Volt/div
TIMEBASE	5 msec/div
EXTERNAL TRIGGER	TP 8/5 (Index)

* NOTE
Fitting a chip-clip to IC61 may cause a slight change in its operating characteristics.

4. The waveform should be as shown in figure 4-5. Incorrect waveforms are shown in figure 4-6.

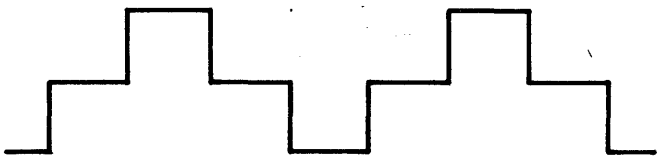


Figure 4-5. Correct Waveform

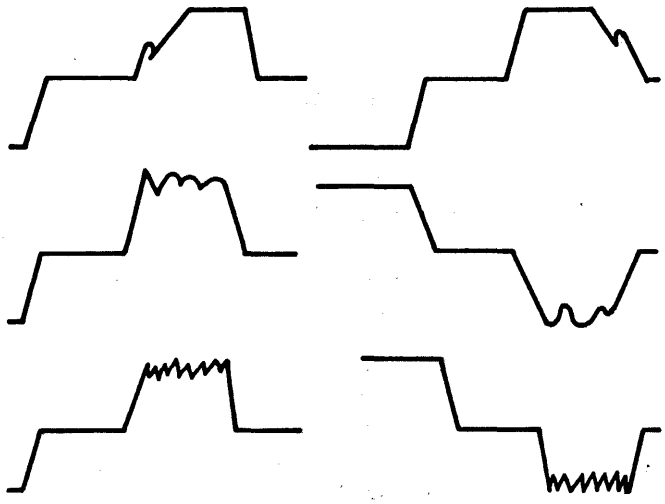


Figure 4-6. Incorrect Waveforms

5. Adjust RV4 until the waveform shown in figure 4-5 becomes unstable as shown in figure 4-7(a).
6. Counting the number of turns, adjust RV4 until the waveform becomes unstable as shown in figure 4-7(b).
7. Adjust RV4 in the opposite direction by the number of turns divided by 2. The waveform should be as shown in figure 4-5 with RV4 adjusted to its mid-range position.

Figure 4-7. Unstable Waveforms

DTM 1000 or BDM 1250

1. Connect the DTM 1000 or BDM 1250 up as follows

PROBE	TEST POINT
A	TP 11/1 (PLL OUTPUT)
FUNCTION: FREQUENCY	

2. Connect test point TP 21 (MFM RD) to 0 Volts.
3. Adjust RV4 until a meter reading of 415 ± 10kHz is obtained.

Data Window Adjustment

Oscilloscope

1. Disconnect the Master/Slave inter-connecting cable (connector 2) at the Master Drive Unit.
2. Connect jumper leads to the following points on the master board.

FROM	TO
PIN 11 (CONN 2)	PIN 31 (CONN 2)
TP 10/2	PIN 16 (CONN 2)

3. Set up the Oscilloscope as follows:

CHANNEL A	2 VOLT/DIV	DC COUPLED
CHANNEL B	2 VOLT/DIV	DC COUPLED
ADD MODE		
TIMEBASE	0.5 µS/DIV	
INTERNAL TRIGGER		

4. Connect the oscilloscope as follows:

PROBE	TEST POINT	SLOPE
A	TP 11/2	+VE
B	TP 11/7	+VE

5. Select drive 2 (slave) using the MTR or disk exercizer.

6. Adjust RV2 until the pulse width at test point TP 11/2 is 1.24 ± 0.1μs.
7. Adjust RV3 until the leading edge of the pulse at test point TP 11/7 occurs – midway along the pulse on test point TP 11/2 (figure 4–8(a)).

NOTE

For boards with artwork revision K, invert Channel B to obtain the same display as in figure 4-8(b). Adjust RV3 until the lagging edge of the pulse at test point TP 11/7 occurs midway along the pulse on test point TP 11/2

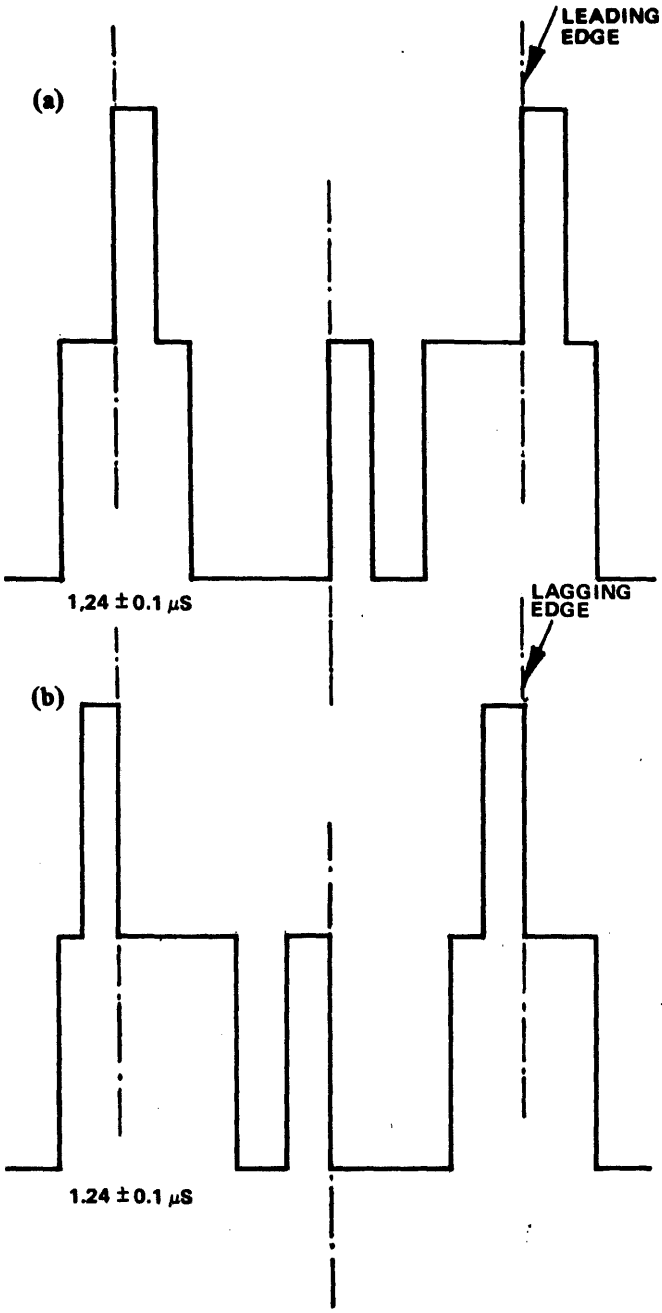


Figure 4-8. Data Window Adjustment

8. Remove all jumper leads and reconnect the master/slave inter-connecting cable (connector 2).

DTM 1000

1. Disconnect the Master/slave inter-connecting cable (Connector 2) at the Master drive unit.
2. Connect jumper leads to the following points on the master board.

FROM	TO
PIN 11 (CONN 2)	PIN 31 (CONN 2)
TP 10/2	PIN 16 (CONN 2)

3. Select Drive 2 (Slave) using the MTR or Disk Exerciser.
4. Set up the DTM 1000 as follows:

PROBE	TEST POINT	SLOPE
A	TP 11/2	+VE
FUNCTION: "WIDTH"		

5. Adjust RV2 until a meter reading of 1.24 ± 0.1μS is obtained.
6. Set up the DTM 1000 as follows:

PROBE	TEST POINT	SLOPE
B	TP 11/2	+VE
C	TP 11/7	+VE
FUNCTION: "INTERVAL BC"		

7. Adjust RV3 until a meter reading of 0.62 ± 0.05μS is obtained.
8. Remove all jumper leads and re-connect the master/slave interconnecting cable (connector 2).

BDM 1250

1. Disconnect the Master/Slave inter-connecting cable (connector 2) at the Master Drive Unit.
2. Connect jumper leads to the following points on the Master Board.

FROM	TO
PIN 11 (CONN 2)	PIN 31 (CONN 2)
TP 10/2	PIN 16 (CONN 2)

3. Select Drive 2 (Slave) using the MTR or disk exerciser.
4. Set up the BDM 1250 as follows:

PROBE	TEST POINT	SLOPE
A	TP 11/2	+VE
FUNCTION: "WIDTH"		

5. Adjust RV2 until a meter reading of 1.24 ± 0.1μS is obtained.

6. Set up the BDM 1250 as follows:

PROBE	TEST POINT	SLOPE
B	TP 11/2	+VE
C	TP 11/7	+VE
FUNCTION: "TIME B→C"		

7. Adjust RV3 until a meter reading of 0.62 ± 0.05μS is obtained.

8. Remove all jumper leads and re-connect the master/slave interconnecting cable (connector 2).

SECTION 5
MAINTENANCE PROCEDURES

REMOVAL AND REPLACEMENT PROCEDURES

FASCIA

Removal

Remove nuts securing the four corners of the fascia to the baseplate. Gently remove fascia from baseplate.

Replacement

Fascia door and receiver open. Carefully refit fascia to baseplate. Fit the nuts securing the four corners of the fascia to the baseplate.

RECEIVER

Removal

Remove fascia.
Remove head-lifting plate.
Remove pressure pad lifting arm from pressure pad solenoid.
Release receiver from pivot pins.

Replacement

Fit receiver on to pivot pins.
Fit pressure pad lifting arm onto pressure pad solenoid.
When the pressure pad solenoid is energized there should be clearance between the lifting arm and the pressure pad.
Fit head lifting plate.

STEPPER MOTOR AND CARRIAGE

Removal

Disconnect stepper motor from PCB.
Remove backlash nut locating plate.
Remove screw and washer from the end of the lead screw.
Remove the three screws securing the stepper motor.
Carefully screw the lead screw out of the carriage and backlash nut.

Replacement

Locate carriage onto guide rail.
Fit lead screw through casing
Place carriage onto lead screw.
Screw backlashsnut onto lead screw.
Fit compression spring onto lead screw.
Screw lead screw into carriage block.
Compress the spring by one full turn of the backlash nut.
Fit locking plate.
Fit screw and washer into end of lead screw.
Connect stepper motor to PCB.
Perform head adjustments.

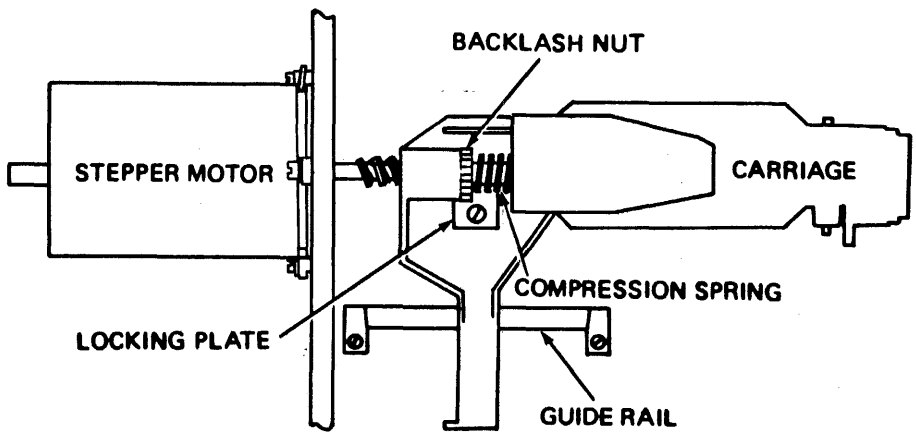


Figure 5–1. Stepper Motor and Carriage Assembly

HEAD SOLENOIDS

These can be removed after removal of the receiver.

LAMPS

Removal

Press together the sides of the lamp cover and remove. The lamps are removed using extractor tool, part number 1622 9825.

Replacement

Push the lamp into the holder.
Push on the lamp cover.

PRESSURE PADS

The pressure pads can be removed or replaced by spreading the pressure pad arms over the pivot pin.

DRIVE BELT

This is always fitted with the soft side next to the pulley.

To convert from 50Hz to 60Hz or from 60Hz to 50Hz remove the motor pulley and refit as shown in figure 5–2.

PREVENTIVE MAINTENANCE GUIDE

Every 1500 hours running time or 1 year whichever comes earlier, replace pressure pads and motor drive belt.

Lubrication is not required for any part.

FAULT FINDING

Faults are traced to the failed component using the MTR procedures.

RECOVERY OF CONTAMINATED DISKS

Contaminants may cause loss of data bits by damaging the surface of the disk. A contaminated disk may transfer the contamination to the drive and affect its ability to transfer data correctly.

If a disk has been mishandled and contamination has occurred, the following procedure may be followed:

1. Remove the contamination from the disk.
   If the contamination is a liquid, swab-up with a folded tissue, using as little force as possible.
   If the contamination is a powder (such as cigarette ash or dust) carefully shake it off.
2. Load the "cleaned" disk into a drive and copy the data onto a new disk.
3. The "cleaned" disk must be thrown away.

If the contamination has reached the recording surface, cleaning is unlikely to remove all the contamination.

Cleaning of disks should not be necessary if the handling procedures (section 1 page 8) are followed.

CERTIFIED DISKS

It is important to use Burroughs certified disks.

Non-certified disks may have too much peak-shift and cause read errors.

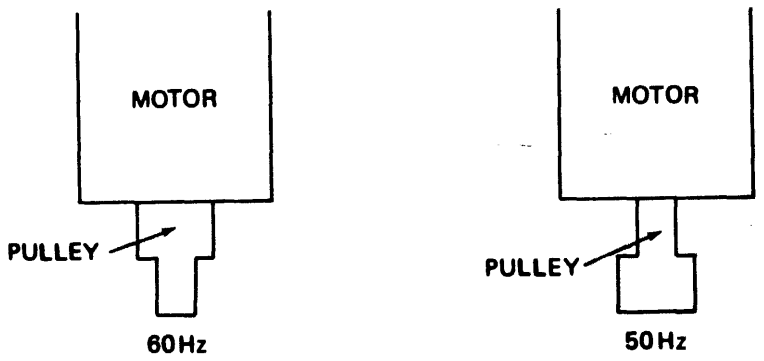


Figure 5–2. 50/60Hz Conversion

Table 5–1. PCB Test Points

NAME	DESCRIPTION	TEST POINT
+ 24V		J3 PINS 1, 6
+ 12V		J3 PIN 5
+ 5V		J3 PIN 8
– 12V		J3 PINS 4, 9
+ 24V GND		J3 PIN 2
+ 5V GND		J3 PIN 7
±12V GND		J3 PIN 3
ADD 1 thru ADD 64	CYLINDER ADDRESS LINES 1 THRU 64	PQ 8
A < B	ADDRESS COMPARATOR OUTPUT	TP 8/1
A = B	ADDRESS COMPARATOR OUTPUT	TP 6/3
A > B	ADDRESS COMPARATOR OUTPUT	TP 6/1
CAB SELT	CABINET SELECT	PQ 8
CLK Ø	CLOCK PHASE	TP 5/6
COUNT DOWN	COUNT DOWN	IC24 PIN 8
COUNT UP	COUNT UP	IC24 PIN 11
DATA CLK	DATA CLOCK	TP 10/7
FILE OP	FILE OPERATIONAL	IC13 PIN 6
FILE OP IND	FILE OPERATIONAL INDICATOR	IC27 PIN 5
HD ADD	HEAD ADDRESS	IC32 PIN 9
HD.LD.T.O.	HEAD LOAD TIME OUT	TP 5/5
HD SELT.	HEAD SELECT	PQ 8
ILL ADD	ILLEGAL ADDRESS	IC16 PIN 5
INDEX	INDEX PULSES	TP 8/5
LOWER SOL	LOWER PRESSURE PAD SOLENOID	Q 13
MFM RD	MILLER FREQUENCY MODE READ	TP 1/2
MFM WRT	MILLER FREQUENCY MODE WRITE	TP 9/4
POS CLK	POSITIONER CLOCK	IC39 PIN 8
POS CLK EN	POSITIONER CLOCK ENABLE	TP 6/2
POSN SETT	POSITIONER SETTLED	IC44 PIN 12
POS STOP	POSITIONER STOP	IC PIN
POS. TIME OUT	POSITIONER TIME OUT	IC33 PIN 6
PSK	POSITIONER SEEK	TP 8/2
RD CLK	READ CLOCK	IC60 PIN 13
RD DATA	READ DATA	TP 10/6
RD EN	READ ENABLE	TP 10/5
RTN	RETURN LINE FOR INTERFACE SIGNALS	PQ 8
SECTOR	SECTOR PULSES	TP 8/4
SEEK	SEEK COMMAND	PQ 8
SEEK INC.	SEEK INCOMPLETE	NOT USED
SET TK00	POSITIONER AT TRACK 00	IC11 PIN 8
S/MØ 1	STEPPER MOTOR PHASE 1	TP 7/8
S/MØ 2	STEPPER MOTOR PHASE 2	TP 7/7
S/MØ 3	STEPPER MOTOR PHASE 3	TP 7/6
WIH	WRITE INHIBIT	TP 8/6
WIH IND	WRITE INHIBIT INDICATOR	IC27 PIN 3
WRT CLK	WRITE CLOCK	TP 9/2
WRT DATA	WRITE DATA	PQ 8
WRT EN	WRITE ENABLE	PQ 8
UNIT SELT	UNIT SELECT	PQ 8
UPPER SOL	UPPER PRESSURE PAD SOLENOID	Q 12
UTSF	UP TO SPEED FLIP-FLOP	TP 5/3
XD SEC	SECTOR TRANSDUCER	J4 TP 6/4
XD SEC RTN	SECTOR TRANSDUCER RETURN	J4
XD TK 00	TRACK 00 TRANSDUCER	J4 TP 6/6
XD TK00 RTN	TRACK 00 TRANSDUCER RETURN	J4
XD WIH	WRITE INHIBIT TRANSDUCER	J4 TP 8/6
XD WIH RTN	WRITE INHIBIT TRANSDUCER RETURN	J4
750 KHz		TP 10/2

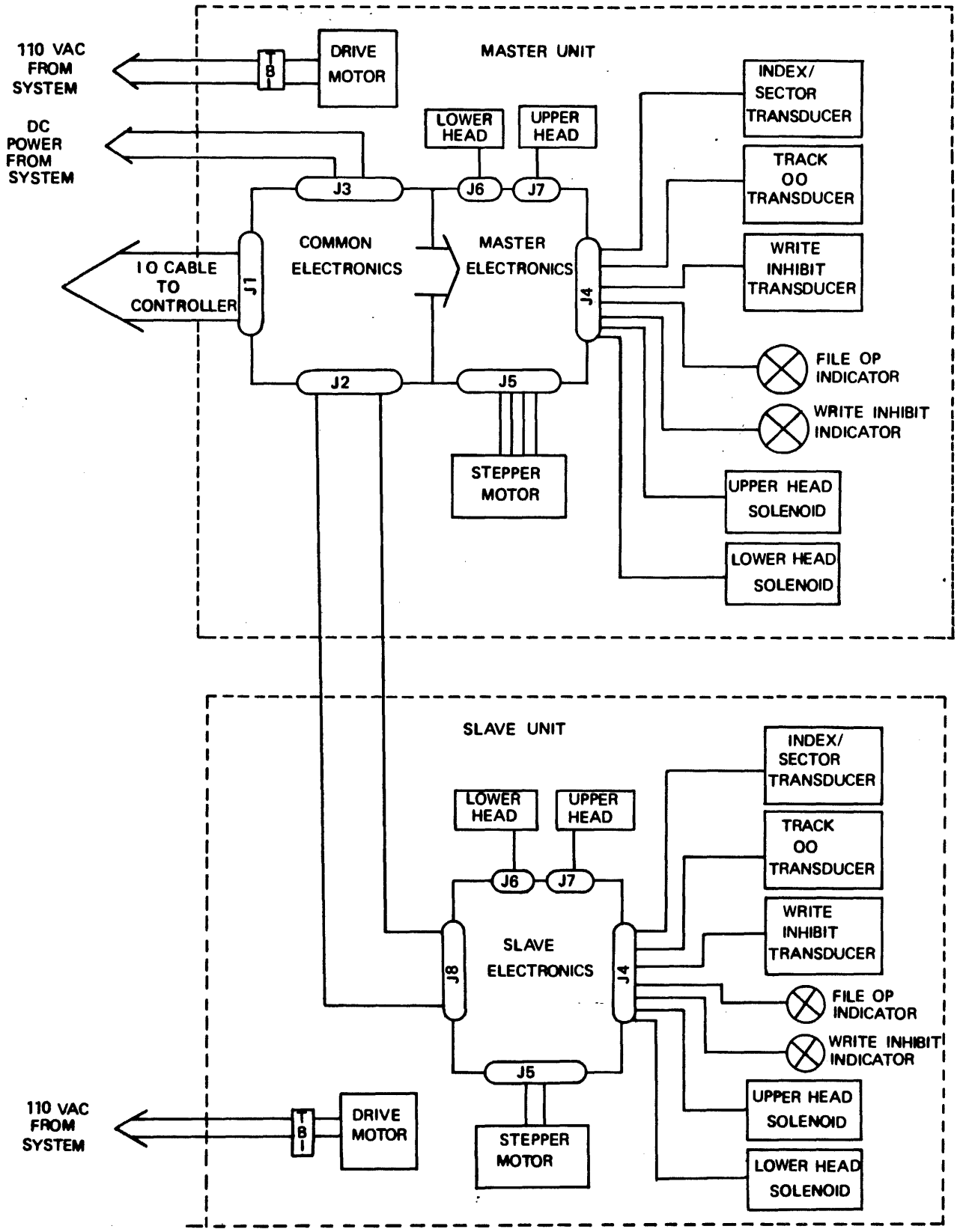


Figure 5–3. Connection Block Diagram

SECTION 6

INSTALLATION PROCEDURES

INSTALLATION PROCEDURES

Unpack the unit and check for any damage. Check the following items:

The motor pulley should be set for the correct mains frequency (see section 5).
The drive belt should be fitted with the soft side nearest to the pulleys.
The spring should be fitted correctly to the pressure pad arm.
The pressure pad arm should be on the correct side of the solenoid lever.
All plugs should be correctly fitted.
All PCB mounting screws should be tight.

For a master unit connect the I/O cable, DC power cable and AC power cable to the host system.

For a slave unit connect the 40 way cable from master to slave and connect the AC power cable to the host system.

Check all power supply voltages to be within ± 10%.

Perform host system confidence tests.

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE INDEX		NO. R2141 (REV 000)
		STYLE/MODEL A/B 9489	PAGE 1 OF 1
ORIGINATOR: T.I.O. GLENROTHES		TOP UNIT NO. * SEE BELOW.	
		DATE 28 February 1978	

* TOP UNIT NUMBERS

1878 9347	1881 2651
1879 4503	1881 0192
1881 2644	1881 0184

RIN NO.	DATE	TITLE
001	11-29-76	A.C. CONNCETOR.
002	11-29-76	INDICATOR LAMP FAILURE.
003(REV)	5- 1-77	MAINTENANCE TEST ROUTINE.
004	6-29-77	HEAD BONDING.
005	9-26-77	INDEX TO DATA BURST ADJUSTMENT.
006	10-26-77	TRIBIT ALIGNMENT METER DOCUMENTATION.
007	2-28-78	HEAD LEAD RELIABILITY HAZARD.
008	2-28-78	MODIFIED ANNULUS AND STUD.

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FOR F.E. TECHNICAL MANUAL FORM 2102141

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This package includes RIN 2141-001 thru -008

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B.D.S.	No. R2141-001
		STYLE/MODEL B9489-1/2	PAGE 1 OF 2
ORIGINATOR: I.T.I.O. GLENROTHES		TOP UNIT NO. 1878 9354	
STD. INSTALL. TIME 0.5 HR	UNITS AFFECTED Below B201987-018	UNIT DESCRIPTION 1 M BYTE MINI-DISK	
TITLE A.C. Connector for Mini-Disk			DATE 29 November '76

TYPE OF CHANGE ☐ FUNCTIONAL ☒ IMPROVED MAINTAINABILITY ☐ IMPROVED RELIABILITY

INSTALLATION IS MANDATORY

PREREQUISITE:

None.

CONDITION:

Shock hazard when the unit is disconnected from the host system.

CORRECTION:

Install AC Power cable and connector provided by this RIN.

PARTS REQUIRED:

Part Number	Description	Quantity	U.S. Unit List Price
1881 1547	AC Power Cable	1	$11.179
1446 9738	Female Connector	1	$ 0.545
1877 7599	Pin	3	$ 0.09

PROCEDURE:

1. Ensure that power is removed from the host system.

2. Remove the AC cable from the AC Terminal Block (B9489 Illustrated Parts Catalog, Form 2102158, item C Plate 5).

3. Install the AC Power Cable (1881 1547) as follows (Refer to Figure 1).

   Install the ground wire (Green) on the stud between the terminal block and the base casting.
   Install the live wire (Black) in TB3.
   Install the neutral wire (White) in TB4.

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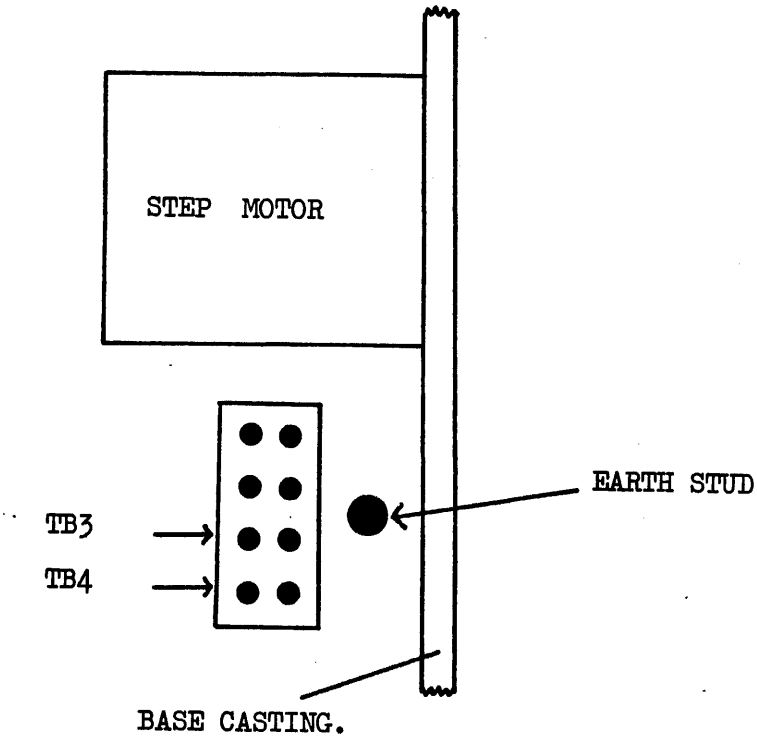

Figure 1

4. Install one pin (1877 7599) onto each of the wires on the AC Cable from the host system.

5. Install the pins into the female connector (1446 9738) as shown in Fig. 2.

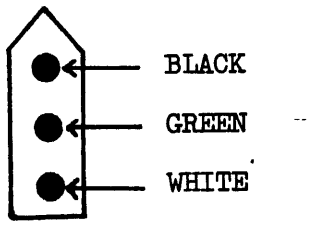

Figure 2

6. Connect the AC power cable connector to the female connector.

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B.D.S.	No. R2141-002
		STYLE/MODEL B9489-1/2	PAGE 1 OF 2
ORIGINATOR: I.T.I.O.GLENROTHES.		TOP UNIT NO. 1878 9354	
STD INSTALL. TIME 0.5 HR.	UNITS AFFECTED B202000-018	UNIT DESCRIPTION 1 MBYTE MINI DISK	
TITLE INDICATOR LAMP FAILURE.			DATE 29 November, 1976
TYPE OF CHANGE ☐ FUNCTIONAL	☐ IMPROVED MAINTAINABILITY	☒ IMPROVED RELIABILITY	

PREREQUISITE

None.

CONDITION

Early failure of indicator lamps.

CAUSE

Excessive voltage applied to lamps.

CORRECTION

Install 220Ω resistors in series with lamps in place of 130Ω resistors at R85 and R86.

PARTS REQUIRED

PART NUMBER	DESCRIPTION	QTY.	U.S. UNIT LIST PRICE
1876 6170	220Ω ½ W 2% Resistor.	2	$ 0.494

Update the schematic as shown in figure 1.

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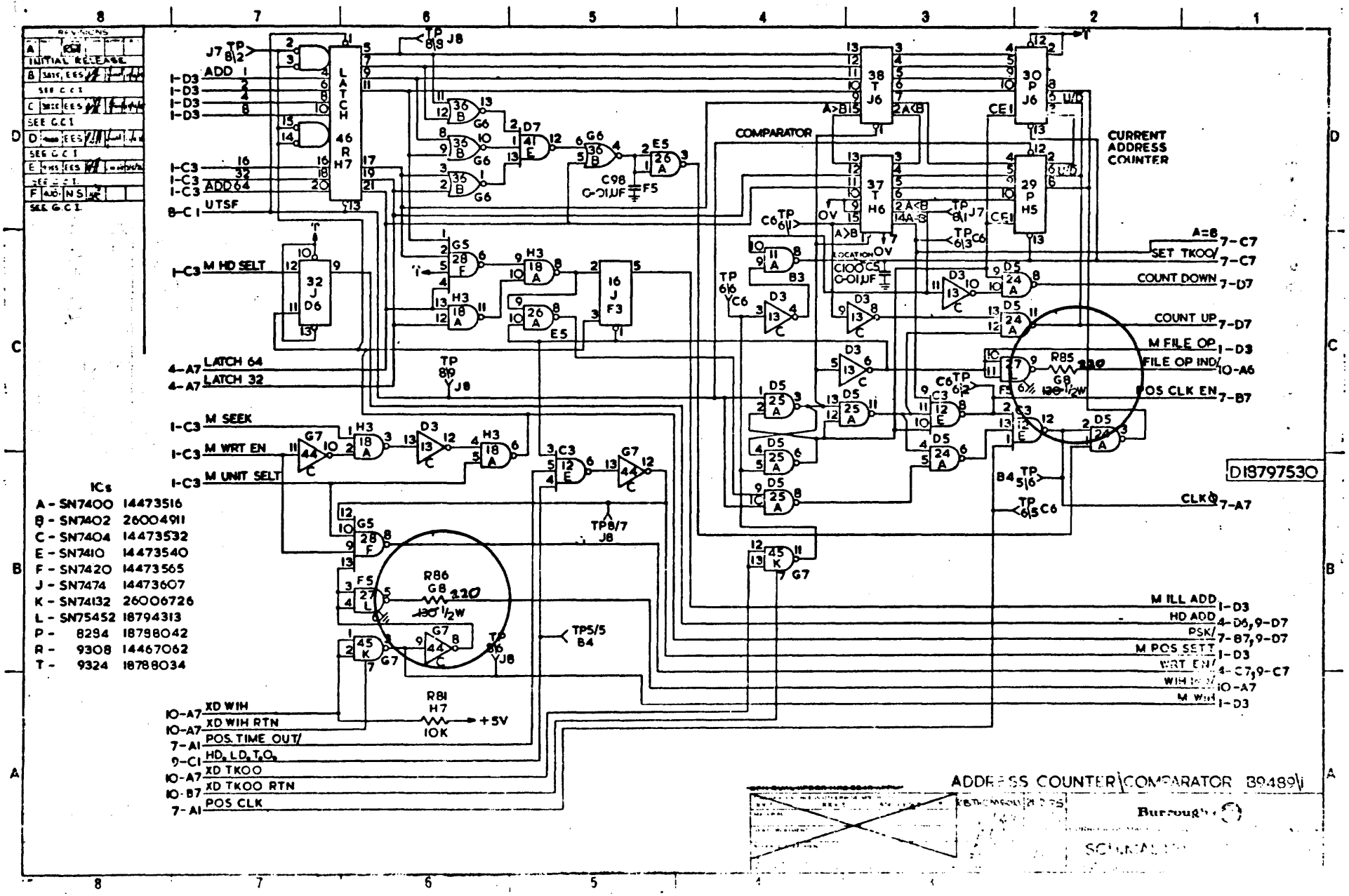
ADDRESS COUNTER\COMPARATOR 89489\
D18797530
CURRENT ADDRESS COUNTER
COMPARATOR
LATCH 46 R H7
38 T J6
30 P J6
37 T H6
29 P H5
32 J D6
16 J F3
ADD 1
ADD 2
ADD 4
ADD 8
ADD 64
UTSF
M HD SELT
LATCH 64
LATCH 32
M SEEK
M WRT EN
M UNIT SELT
XD WIH
XD WIH RTN
POS TIME OUT/
HD, LD, T, O,
XD TKOO
XD TKOO RTN
POS CLK
A=B 7-C7
SET TKOO/ 7-C7
COUNT DOWN 7-D7
COUNT UP 7-D7
M FILE OP 1-D3
FILE OP IND/ 10-A6
POS CLK EN 7-B7
CLK 7-A7
M ILL ADD 1-D3
HD ADD 4-D6,9-D7
PSK/ 7-B7,9-D7
M POS SETT 1-D3
WRT EN/ 4-C7,9-C7
WIH 10-A7
M WIH 1-D3
+5V
ICs
A - SN7400 14473516
B - SN7402 26004911
C - SN7404 14473532
E - SN7410 14473540
F - SN7420 14473565
J - SN7474 14473607
K - SN74132 26006726
L - SN75452 18794313
P - 8294 18798042
R - 9308 14467062
T - 9324 18788034

FIGURE 1.

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B80	NO. R2141-003 Rev
		STYLE/MODEL B9489-1/2	PAGE 1 OF 1
ORIGINATOR: ITIO GLENROTHES		TOP UNIT NO. 1 878 9354	
STD INSTALL. TIME 0.5 HRS	UNITS AFFECTED ALL	UNIT DESCRIPTION 1 MBYTE MINI DISK	
TITLE MAINTENANCE TEST ROUTINE			DATE 1 May 1977

TYPE OF CHANGE ☐ FUNCTIONAL ☒ IMPROVED MAINTAINABILITY ☐ IMPROVED RELIABILITY

PREREQUISITE There are no special requirements.

✓ CONDITION 1) Unable to run MTR without dummy head.

✓ CORRECTION 1) Assemble dummy head.

PARTS REQUIREMENTS

Part Number	Description	Quantity	U.S. Unit List Price
1268 1847	Resistor 10 ohm ½W	3	$0.25
1881 4194	Connector	1	$4.021
1879 5047	Terminal	4	$0.19

PROCEDURE

1) A dummy head is required.

2) This should be assembled using the parts listed in Parts Requirements.

3) Assemble the resistors and the terminals into the connector as shown in Fig. 1.

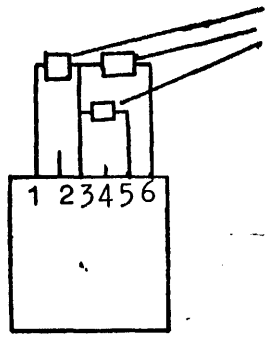

Figure 1.

✓ Note: MTR Procedures are released (Form 2011300).

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Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B-80	NOR 2141-004
		STYLE/MODEL A/B 9489	PAGE 1 OF 6
ORIGINATOR: T.I.O. GLENROTHES.		TOP UNIT NO. * SEE BELOW	
STD. INSTALL. TIME 2 HRS. APPROX.	UNITS AFFECTED ** SEE BELOW	UNIT DESCRIPTION 1 MB MINI-DISK DRIVE	
TITLE HEAD BONDING			DATE 29 June 1977
TYPE OF CHANGE ☐ FUNCTIONAL	☐ IMPROVED MAINTAINABILITY		☐ IMPROVED RELIABILITY

* TOP UNIT NOS.

1878 9347	1881 2651
1879 4503	1881 0192
1881 2644	1881 0184

** UNITS AFFECTED

All units below S/N 206685-018. This RIN does not affect these units below S/N 203500-018 which have been returned to Glenrothes for rework under the update program. The change can be identified by examining the point where the head is joined to the carriage block. If there is an extra fillet of white adhesive present, then there is no need to fit this RIN. If you have any doubt, then please contact your local Technical Support Group.

THIS RIN IS MANDATORY

PREREQUISITE: NONE

CONDITION: The head becomes detached from the carriage block.

CAUSE: Adhesive failure.

CORRECTION: Add an extra fillet of epoxy adhesive to the back of the head.

TOOLS REQUIRED: Cloths , cleaning material.

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PARTS REQUIRED

PART NO.	DESCRIPTION	QTY	U.S.LIST PRICE
1881 7817	Head Bonding Kit	1	$ 28.11

NOTE:

1. The kit consists of the following individual items:
   - Dual compartment sachet containing adhesive and hardener.
   - Disposable plastic syringe.
   - Cleaning wad.
2. The adhesive has a shelf life of approx. 6 months.
3. After installation, it is necessary to allow a period of 6 hours in a warm atmosphere for adhesive to harden. You should therefore plan the work last thing in the evening. The mini-disk can then be left overnight in the B80 with power switched on.
4. The utmost care must be taken not to allow any adhesive to contaminate adjacent areas.
5. Do not use excess adhesive as it may run into the pad arm mechanism.
6. The majority of time required for this RIN is for removing/replacing the minidisk in the B80. If therefore, the B80 has 2 minidisk drives, the RIN should be installed on both drives at the same time.
7. The kit contains sufficient material for 4 drives.

INSTALLATION:

1. Remove minidisk drives from the B80.
2. Remove the metal cover and the printed circuit board from the minidisk drives.
3. The adhesive sachet has 2 compartments. One compartment contains the adhesive and the other the hardener. The adhesive and hardener are separated from each other by the plastic clip. See figure 1 for details.

INSTALLATION

4. Pull out the plastic clip. Thoroughly mix the adhesive and hardener by squeezing and kneading the sachet for at least 3 minutes.

5. Remove the plastic tube which covers the syringe nozzle. Install the nozzle onto the syringe.

6. Remove the plunger from the syringe. Cut a corner off the sachet, and squeeze the adhesive mixture into the syringe barrel.

7. Replace the syringe plunger. Gently squeeze the plunger over a cloth until adhesive starts to ooze from the nozzle. Wipe the nozzle clean.

8. Rotate the stepper motor lead screw until the back of the upper head can be accessed through the chassis.

9. Taking the utmost care, squeeze the adhesive from the syringe to make a continuous strip where the back of the head meets the carriage block. See figures2 thru 5 for details.

DO NOT USE EXCESS ADHESIVE

10. Use the cleaning wad to remove any spots of adhesive from adjacent areas.

11. Turn the unit over, and repeat steps 8 thru 10 for the lower head.

12. Make a final inspection to ensure the adhesive has not contaminated adjacent surfaces.

13. Replace the metal cover and printed circuit board.

14. Follow steps 8 thru 13 for the other mini disk drive.

15. Re-install drives into the B80.

16. Power up the B80 and leave for at least 6 hours for the adhesive to harden. (This may conveniently be done overnight).

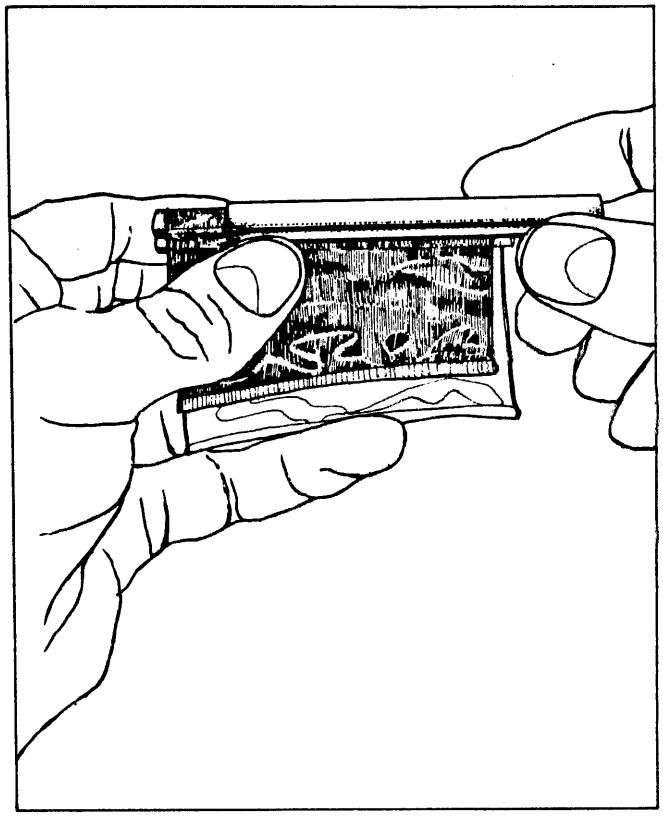

Figure 1. Removing Separator Clip from Sachet

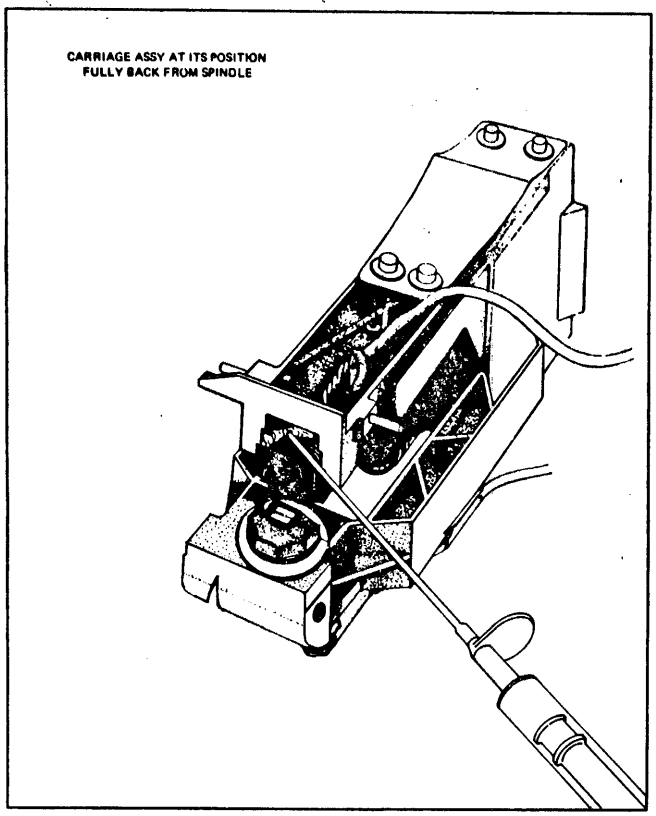

Figure 2. Applying Adhesive to Upper Head

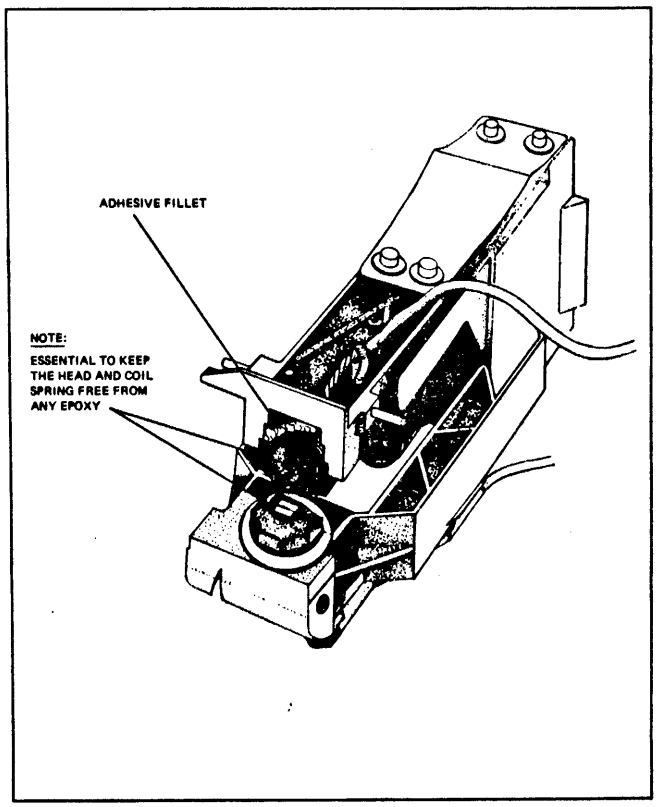

Figure 3. Upper Head – Adhesive Fillet in Place

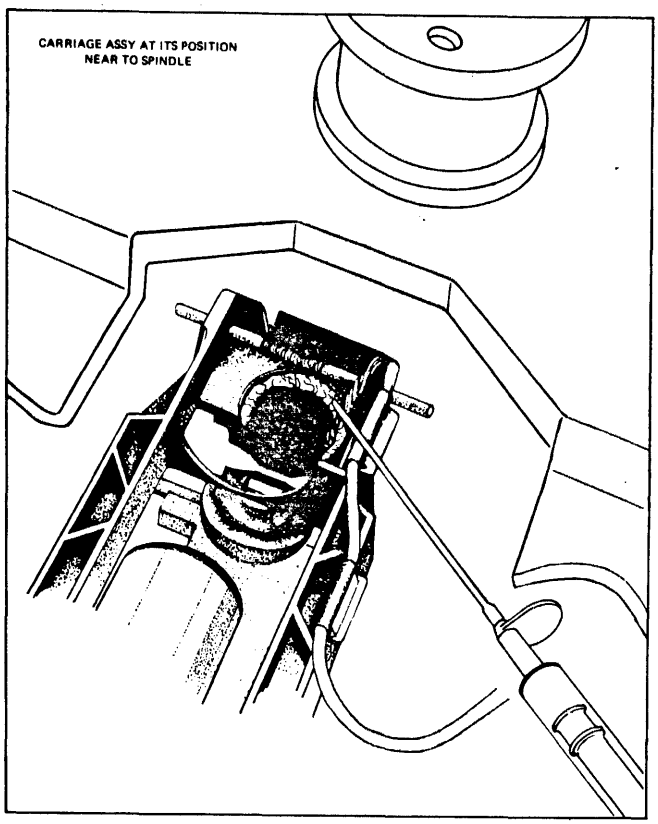

Figure 4. Applying Adhesive to Lower Head

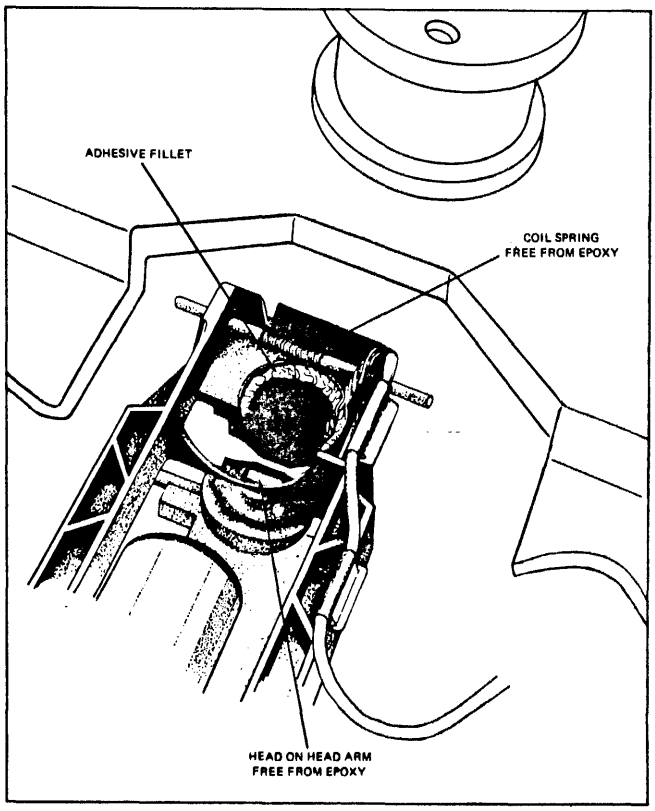

Figure 5. Lower Head – Adhesive Fillet in Place

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B 80	NO. R2141 - 005
		STYLE/MODEL A/B 9489	PAGE 1 OF 3
ORIGINATOR: GLENROTHES.		TOP UNIT NO. * SEE BELOW	
STD INSTALL. TIME 1.0 HR.	UNITS AFFECTED **	UNIT DESCRIPTION 1 MB MINI DISK DRIVE.	
TITLE INDEX TO DATA BURST ADJUSTMENT. G.C.I. 4612			DATE 26 October 77
TYPE OF CHANGE ☐ FUNCTIONAL	☒ IMPROVED MAINTAINABILITY	☐ IMPROVED RELIABILITY	

* TOP UNIT NOS.

1878 9347	1881 2651
1879 4503	1881 0192
1881 2644	1881 0184

** UNITS AFFECTED

This change applies only to units in which boards with Revision K artwork are fitted.

PREREQUISITE : None.

CONDITION: Failure to adjust the index to data burst adjustment to specification.

CAUSE: Quoted range of index to data burst adjustment (650 us to 1.7 ms) insufficient to cover mechanical tolerances.

CORRECTION: Give Revision K boards the same adjustment range (160 us to 1.7 ms) as boards with previous revision levels.

PART REQUIRED

PART NUMBER	DESCRIPTION	QUANTITY	U.S. UNIT LIST PRICE
2155 6337	50K POT	1	$ 15. 067
1876 5156	RESISTOR 2 K	1	$ 0. 290
1876 9877	CAPACITOR 0.047 uF	1	$ 3. 261

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INSTRUCTIONS:

1. Switch off power to host system.
2. Remove disk drive from host system.
3. Remove revision K board from drive.
4. Replace potentiometer RV1 at location B 6 with a 50K pot.
5. Replace resistor R64 at location A5 with a 2K ohm resistor.
6. Replace capacitor C33 at location A5 with a 0.047uF capacitor.
7. Refit revision K board to drive.
8. Refit disk drive to host system.
9. Switch on Power to Host system.
10. Carry out circumferential alignment procedure.
11. Amend the schematic drawing to reflect change. (Refer to Figure 1)

INDEX TO DATA BURST
ADJUSTMENT

160 uS to 1.7 mS.

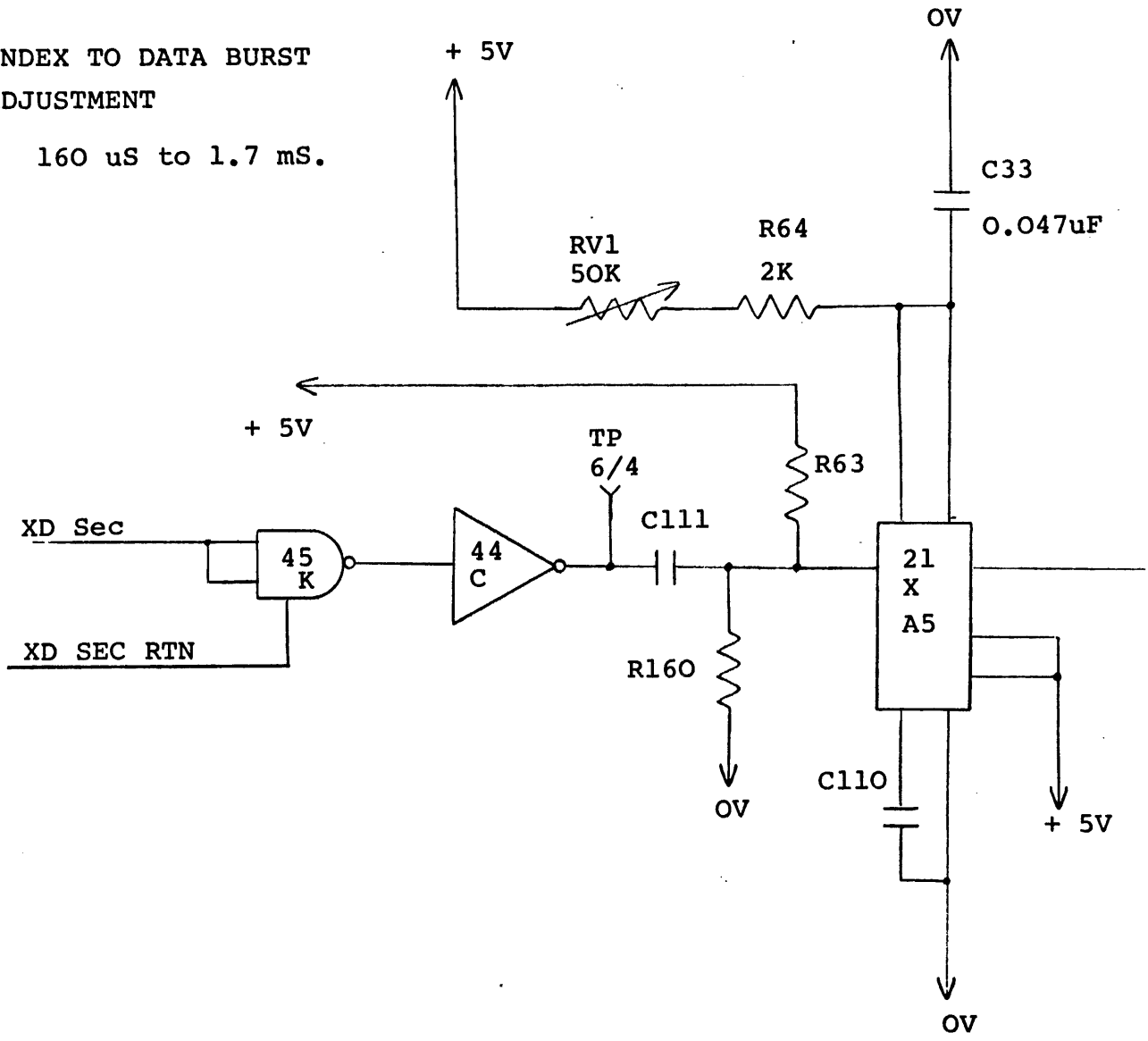

FIGURE 1

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B 80	NO. R 2141-006
		STYLE/MODEL A/B 9489	PAGE 1 OF 7
ORIGINATOR: T.I.O.GLENROTHES.		TOP UNIT NO. *SEE BELOW	
STD INSTALL. TIME N/A	UNITS AFFECTED ALL	UNIT DESCRIPTION 1MBYTE MINIDISK DRIVE	
TITLE TRIBIT ALIGNMENT METER DOCUMENTATION.			DATE 26 October 1977
TYPE OF CHANGE ☐ FUNCTIONAL	☒ IMPROVED MAINTAINABILITY	☐ IMPROVED RELIABILITY	

* TOP UNIT NUMBERS

1878 9347	1881 2651
1879 4503	1881 0192
1881 2644	1881 0184

PREREQUISITE: None.

CONDITION: No documentation for alignment meter.

CORRECTION: Documentation included in this RIN.

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TRIBIT ALIGNMENT METER

PARTS LIST

1880 7917 COMPLETE ALIGNMENT METER.
1881 2412 COMPLETE P.C.B. ASSEMBLY.

PART NUMBER	DESCRIPTION
1881 2420	TRANSFORMER
1881 4129	CASE
1881 4137	NEON LAMP
1881 4147	L.E.D.
1635 1637	SWITCH
1881 4152	SWITCH, D.P.D.T.
1881 4236	INSULATING TERMINAL.
2006 7641	GROMMET.
1881 4384	GROMMET, SLEEVED.
1881 4160	METER.
1103 6019	STANDOFF.
1446 8490	FUSE HOLDER.
1881 4178	FUSE, 1A.
1879 8280	TERMINAL BLOCK.
1881 4186	FUSE 500mA
1881 4194	CONNECTOR HOUSING.
1879 5047	FIXED TERMINAL.
1881 4202	WAFER ASSEMBLY.
1880 0466	POLARIZING PEG.
1447 1718	LUG.
1323 9397	CLIP
1105 7932	SCREW 6/32" x 0.375"
1256 0397	SCREW, ¾" P.H.
1257 4125	HEX NUT WITH LOCKWASHER.
1256 5206/	

PART NUMBER	DESCRIPTION
1256 5206	NUT
1256 7426	LOCKWASHER
1256 8036	PLAIN WASHER
1881 4103	POT 4.7K
1881 6595	LOCKING NUT.
1112 0599	CABLE TIE.
1881 8021	TRANSFORMER BRACKET.

ELECTRICAL COMPONENTS

PART NUMBER	DESCRIPTION
1446 7245	DIODE IN 4448
1105 9052	DIODE ZENER IN 751A
1446 7278	DIODE IN 935.9V
1319 0095	DIODE TYPE IN 752A
1881 4046	BRIDGE RECTIFIER.
1881 2396	PCB ARTWORK
1881 4061	TERMINAL POST
1881 4079	HEATSINK
1256 0330	SCR PHD 4-40 x .230
2157 8547	9602
1447 3607	IC 7474 D D-TYPE
1447 3516	IC 7400 Q 2-INP ND
1447 3540	IC 7410 T 3-INP ND
1880 1829	IC 7416 HEX INVTR.
1879 4610	IC DUAL ANLG SWTCH
1879 9650	IC LM 339 D
1880 1191/	

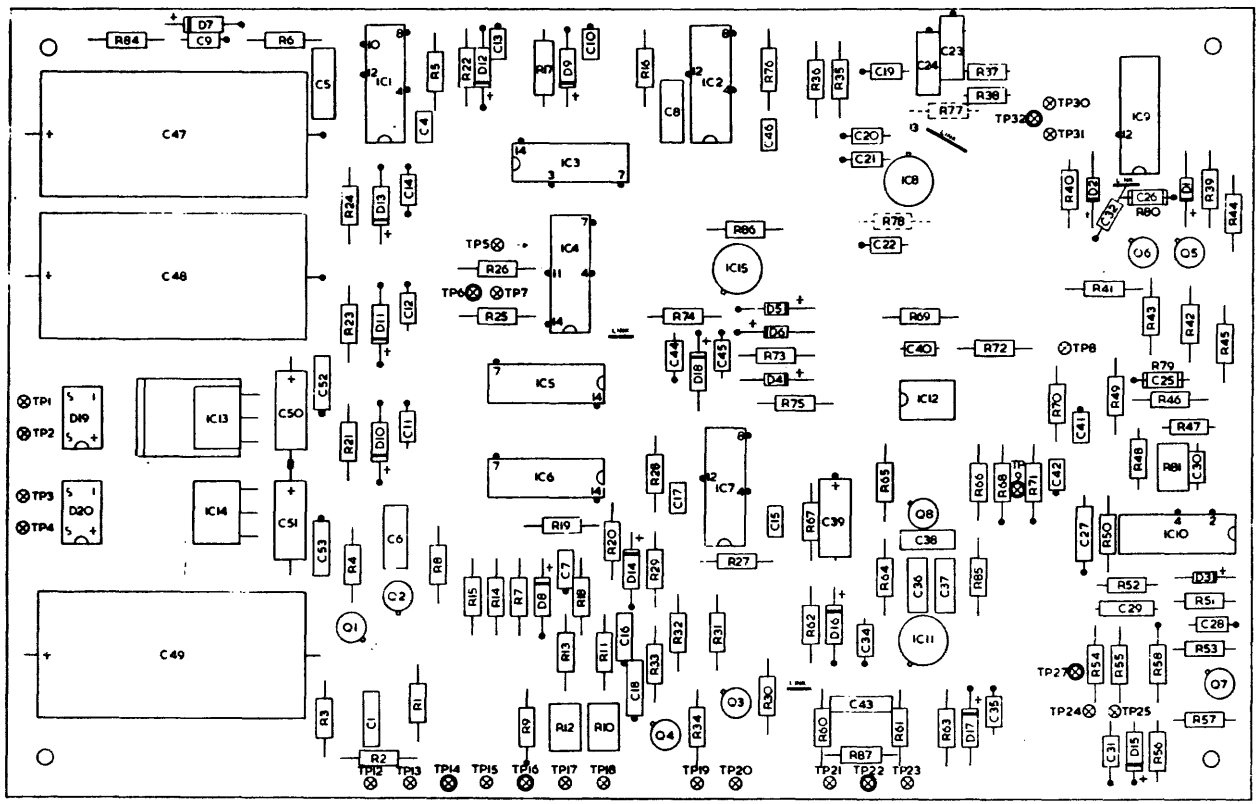
PART NUMBER	DESCRIPTION
1880 1191	IC 747E DUAL OP AMP
2010 0582	IC 733C DIFF AMP
1881 4087	IC NE531 V
1881 4095	IC REG 7812UC
1127 2077	IC 710C VOLT COMP
1446 7187	TRANS 2N2007A
2208 6813	TRANS 2N2222A
2470 7051	TRANSISTOR 2N4092
1876 4597	RESISTOR
1876 4779	RES 51 OHMS QW 2%
1876 6113	RES 120 OHM 1/2W
1876 6154	RES 180 OHM 1/2W
1876 6170	RES 220 OHMS HW 2%
1876 6196	RESISTOR 270 1/2W
1876 4969	RES 330 OHMS QW 2%
1876 4985	RES 390 OHMS QW 2%
1876 5008	RES 470 OHMS QW 2%
1876 5024	RES 560 OHMS QW 2%
1876 5081	RES 1K QW 2%
1876 5172	RES 2K4 QW 2%
1876 5255	RES 5K1 QW 2%
1876 5271	RES 6K2 QW 2%
1876 5297	RES 7K5 QW 2%
1876 5321	RES 10K QW 2%
1876 5305	RES 8K2 QW 2%
1876 5396	RES 20K OHMS 2% QW
1876 5446	RES 33K QW 2%
1876 5487	RES 47K QW 2%
1876 5529	RES 68K QW 2%
1876 5545	RES 82K 2% QW
1876 5560	RES 100K QW 2%
1876 5636/	

PART NUMBER	DESCRIPTION
1876 5636	RES 200K QW 5%
1265 6856	RES 1MEG QW 5%
1876 5412	RES 24K QW 2%
2155 6311	POT 20K
2155 6337	POT 50K QW
2155 6352	POT 200K
1881 4111	CAP 2.2PF 50V CER
1877 2194	CAP 100PF 500V
1877 2269	CAP 200PF
1877 2343	CAP 430PF 500V
1877 2426	CAP 820PF 300V 5%
2300 5697	CAP. .01 F 50V
1877 1402	CAP 022MF 80V
1877 1469	CAP 0.068MF 80V
1876 9893	CAP 0.10UF 50V
1876 9950	CAP 1.0UF 50V
1876 9976	CAPACITOR, 2.2U20%C
1876 7624	CAP 15 MF
1881 4038	CAP 2200UF 25V ELE

DO NOT SCALE # IN DOUBT ASK

A EES 1 INITIAL RELEASE

E 1881 2404



TERMINAL POSTS INDICATED THUS— ⊗ TP

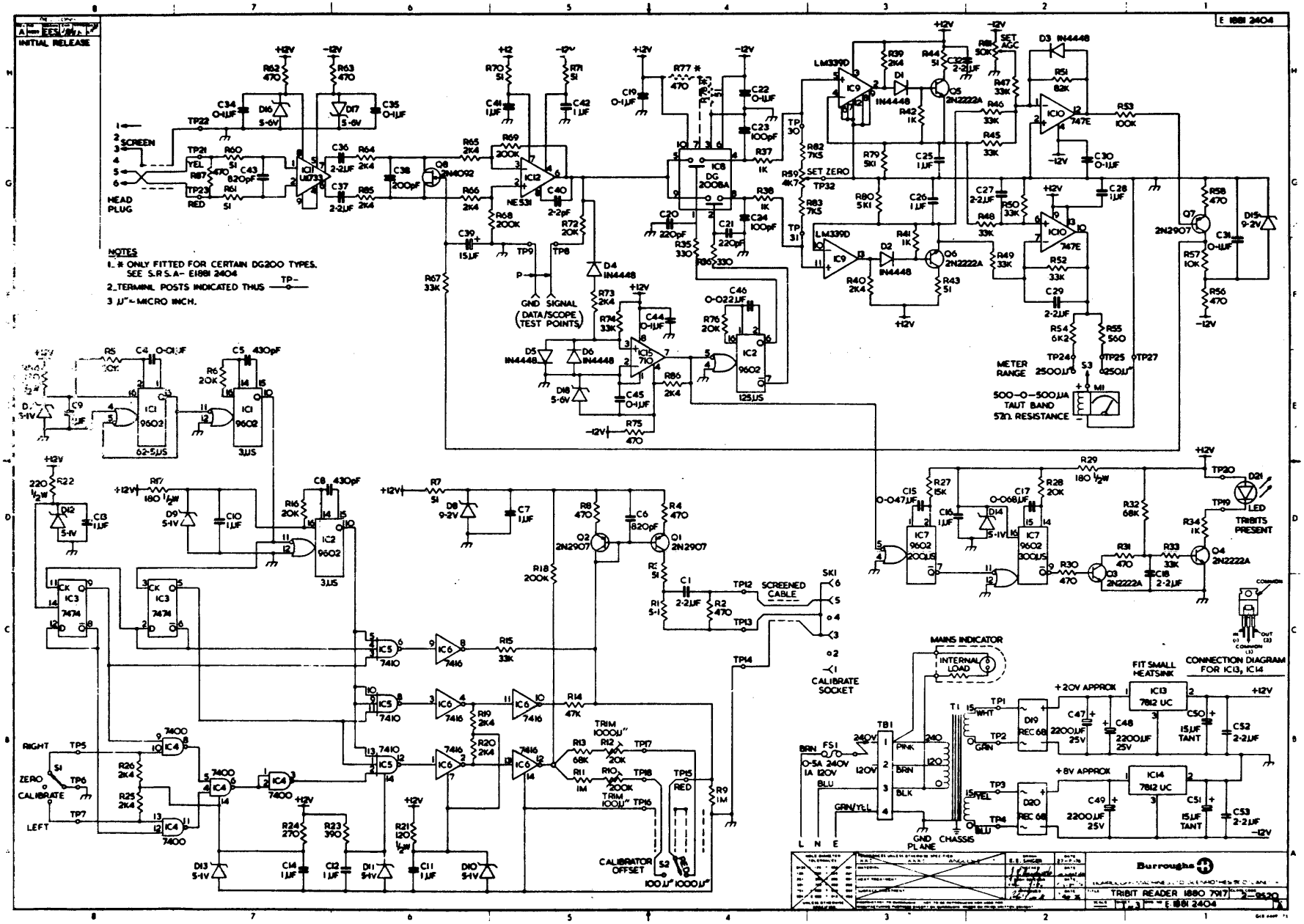
TERMINAL POSTS INDICATED THUS ⊗ TO BE SOLDERED ON TOP FACE OF BOARD

COMPONENT TERMINAL POINTS SHOWN THUS:— ● TO BE SOLDERED ON TOP FACE OF BOARD

SEE SCHEMATIC E-1681 2404 SHEET 1 OF 3

Burroughs

TRIBIT READER ASSY 1880 7917 2-7045
E 1881 2404 A



RIN R 2141-006
PAGE 7 of 7
DATE 25 October 1977

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B80, B800	NO. R2141-007
		STYLE/MODEL A/B 9489	PAGE 1 OF 3
ORIGINATOR: T.I.O.GLENROTHES.		TOP UNIT NO. * SEE BELOW.	
STD. INSTALL. TIME 0.5 HR	UNITS AFFECTED * *	UNIT DESCRIPTION 1 MB MINI DISK DRIVE	
TITLE HEAD LEAD RELIABILITY HAZARD. (G.C.I. 5025)			DATE 28 February 1978
TYPE OF CHANGE ☐ FUNCTIONAL ☐ IMPROVED MAINTAINABILITY ☒ IMPROVED RELIABILITY			

THIS RIN IS MANDATORY

* TOP UNIT NOS.

1878 9347	1881 2651
1879 4503	1881 0192
1881 2644	1881 0184

** UNITS AFFECTED.

Units shipped from Guadalajara Plant with Ser. No 151647476 and below.

PREREQUISITE: None

CONDITION: Head leads have a tendency to break in the vicinity of the clamps securing the leads to the carriage assembly and casting. This can result in hard or intermittent read/write failures.

CORRECTION: Removal of clamps from the carriage assembly and casting to eliminate the reliability hazard.

INSTRUCTIONS:

1. Switch off the power to the Host System.
2. Remove the side panel of the Disk Drive unit to obtain access to the carriage assembly.
3. Remove clamp (P/N 1881 0846) that secures head leads to the carriage assembly.
4./

F.E. Dist. Code BL

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INSTRUCTIONS contd.

4. Remove clamps (P/N 1880 9632 & 1880 9640) that secure the head leads to the casting in the vicinity of the carriage assembly.

5. Refit the side panel of the Disk Drive unit.

6. Switch on the power to the Host System.

7. Carry out functional check of the System.

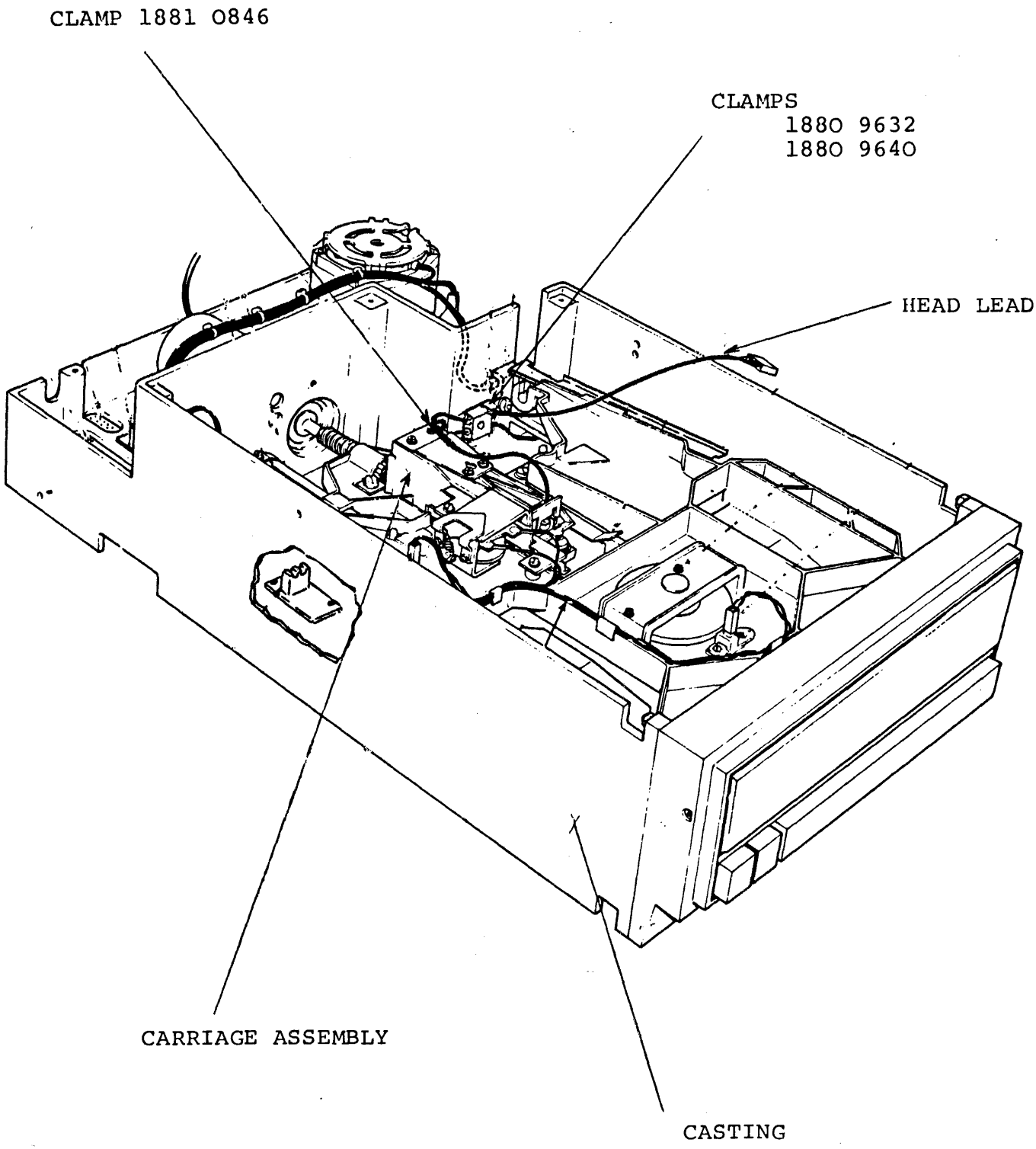

FIGURE 1 : SHOWING THE POSITION OF THE CLAMPS.

Burroughs FIELD ENGINEERING	RELIABILITY IMPROVEMENT NOTICE	SYSTEM SERIES B80, B800	NO. 2141-008 (REV)
		STYLE/MODEL A/B 9489	PAGE 1 OF 3
ORIGINATOR: T.I.O. GLENROTHES.		TOP UNIT NO. * SEE BELOW.	
STD. INSTALL. TIME 0.5 HR.	UNITS AFFECTED **	UNIT DESCRIPTION 1 MB MINI DISK DRIVE.	
TITLE MODIFIED ANNULUS TO PREVENT DISK SLIPPAGE (GCI 4895)			DATE 1 May 1978
TYPE OF CHANGE ☐ FUNCTIONAL ☐ IMPROVED MAINTAINABILITY ☒ IMPROVED RELIABILITY			

* TOP UNIT NOS.

1878 9347	1881 2651
1879 4503	1881 0192
1881 2644	1881 0184

** UNITS AFFECTED

Below Ser. No. 209689-018

PREREQUISITE: None.

CONDITION:
1. Heavy score marks around the disk center "hard hole" to show possible disk slippage.
2. Read errors caused by disk slippage.

CORRECTION: Replace the annulus and stud with a modified version. This design modification improves the unit's capability to drive higher friction disks.

PARTS REQUIRED:

PART NUMBER	DESCRIPTION	QTY.	U.S. UNIT LIST PRICE
1882 3377	ANNULUS KIT	1	$ 13.22

INSTRUCTIONS:/

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INSTRUCTIONS:

1. Switch off the power to the Host System.
2. Remove the side cover of the Disk Drive Unit to obtain access to the cartridge receiver.
3. Press the release bar to open the door and release the cartridge receiver.
4. Set the annulus to an angle and move one side of the annulus below the cartridge receiver locating surface.
5. Remove the spring and stud. (See Figure 1)
6. Remove the annulus.
7. Install the new bearing (P/N 1881 8195) to the new annulus (P/N 1880 9335)
8. Insert the new annulus and put in a position as in Step 4.
9. Insert the new stud (P/N 1881 9771) into the new bearing and then put the spring over the stud.
10. Move the annulus until the side located on the lower side of the cartridge receiver goes through the slot and is located on the top side of the cartridge receiver.
11. Close the door and check for the correct location of the annulus on the spindle drive surface.
12. Replace the side cover to the Disk Drive unit.
13. Switch on the power to the Host System.
14. Check the operational performance of the System.

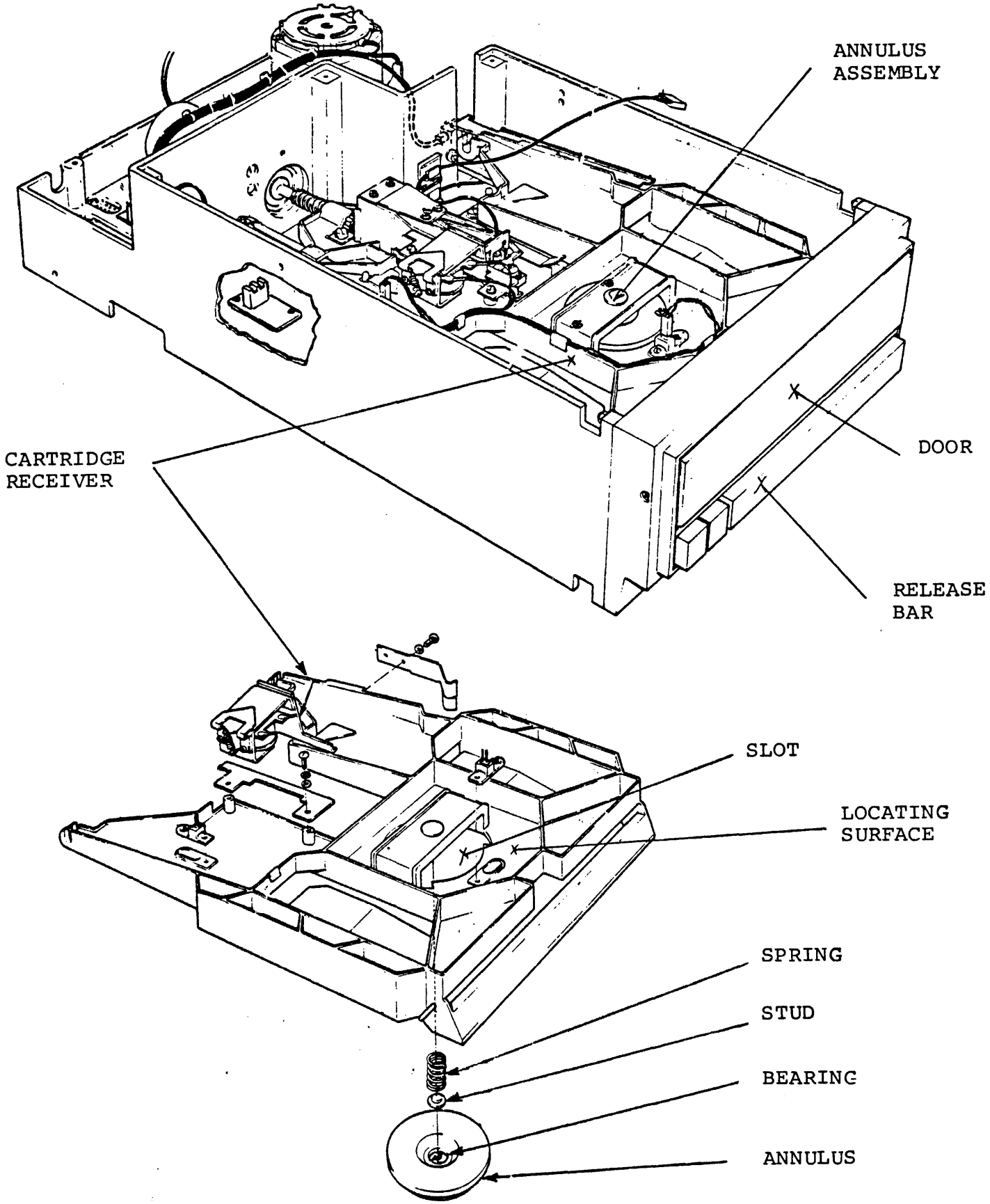

FIGURE 1 : CARTRIDGE RECEIVER AND ANNULUS ASSEMBLY.

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE INDEX		NO. L2141-000 (Rev)
		STYLE/MODEL A/B 9489	PAGE 1 OF 1
ORIGINATOR: TIO GLENROTHES		TOP UNIT NO. * SEE BELOW	
		DATE 19 September 1977	

* TOP UNIT NUMBERS

1878 9347	1881 2644
1879 4503	1881 2651
1881 0184	1881 0192

LIN NUMBER	DATE	TITLE
001	5.8.77	Improvement to Read Channel
002	5.8.77	Improved Maintainability
003	5.8.77	Switched Filter
004	5.8.77	Write Enable Delay, Possible Clock/Head Address modification.
005	5.8.77	False Write Enable Indication
006	9.19.77	Missing Artwork on REV K Slave Boards.

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Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES BDS	No. L2141-001
		STYLE/MODEL B9489-1/-2	PAGE 1 OF 5
ORIGINATOR ITIO GLENROTHES		TOP UNIT NO. 1878 9354	
STD. INSTALL. TIME 0.5 HR	UNITS AFFECTED * See below	UNIT DESCRIPTION 1.2 M BYTE MINI-DISK DRIVE	
TITLE IMPROVEMENT TO READ CHANNEL			DATE 8 May 1977

INSTALLATION IS MANDATORY

Units affected - B200198-018 thru B200800-018.

NOTE Some units will be returned to Glenrothes plant for rework that will incorporate this change. Reworked units will have a coloured label applied to the ID label. Consult your local technical support group before applying this LIN.

PREREQUISITE Printed Circuit Board Artwork must be revision G H or J for Master Board and revision G or J for Slave Board.

CONDITION Intermittent read errors.

CAUSE Incorrect frequency response of read amplifier.

CORRECTION Make the following changes to the read amplifier.

PARTS REQUIREMENTS

Part Number	Description	Quantity	U.S. Unit List Price
1103 0046	200 uH Choke	2	$5.90
1876 5008	470 ohms ¼W 2% Resistor	2	$0.224
1877 2392	620 pF Capacitor	1	$1.658

PROCEDURE

1) Identify the artwork revision of the PCB. The revision letter is shown after the part number for the artwork. The P/N for the artwork for Master PCBs is 1879 4792. This is etched on the PCB at L1. The P/N for the artwork for Slave PCBs is 1879 4800. This is etched on the PCB at L1. For Master PCB revision H or J and Slave PCB revision J go to Step 2.

   For Master PCB revision G go to Step 9.

   For Slave PCB revision G to to Step 11.

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Revision H and J Master and Revision J Slave

2. Cut two tracks and add two wires as shown in Figure 1.

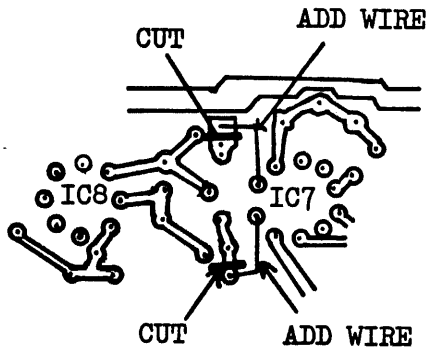

FIGURE 1.

3. Remove the following components.
R53, R54, R154, R155, TP16, TP17, C17, C13.
Retain C13 (510pF) for future use.

4. Fit two 470 Ω resistors (P/N 1876 5008) as shown in Figure 2.

5. Fit two 200 uH Chokes (P/N 1103 0046) as shown in Figure 2.

6. Fit the 510pF Capacitor (removed in Step 3) in the C17 position.

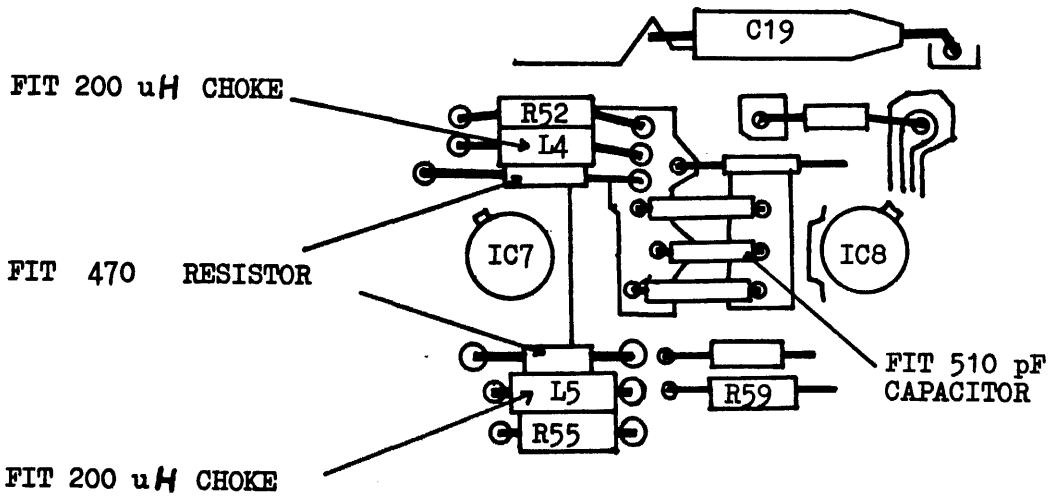

FIGURE 2.

7. Fit the 620 pF Capacitor (P/N 1877 2392) in the C 13 position.

8. Update the schematics as shown in Figure 3.

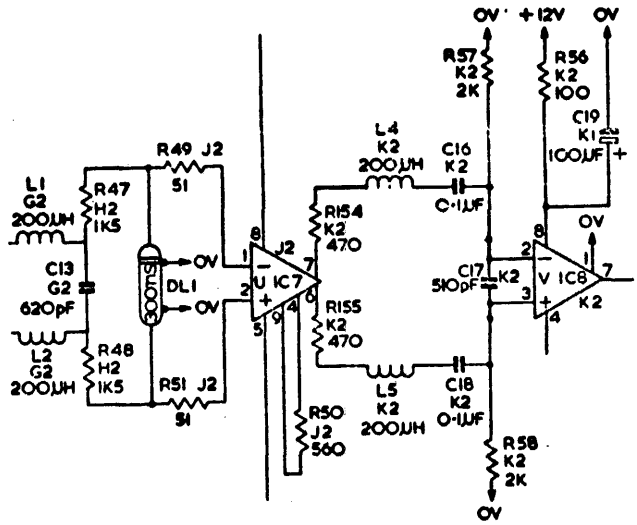

FIGURE 3.

REVISION G MASTER

9. Remove R53, R54, R57, R58, R154, R155, C13, C16, C17 C18 as shown in figure 4.

Retain C13 (510pF) for future use.

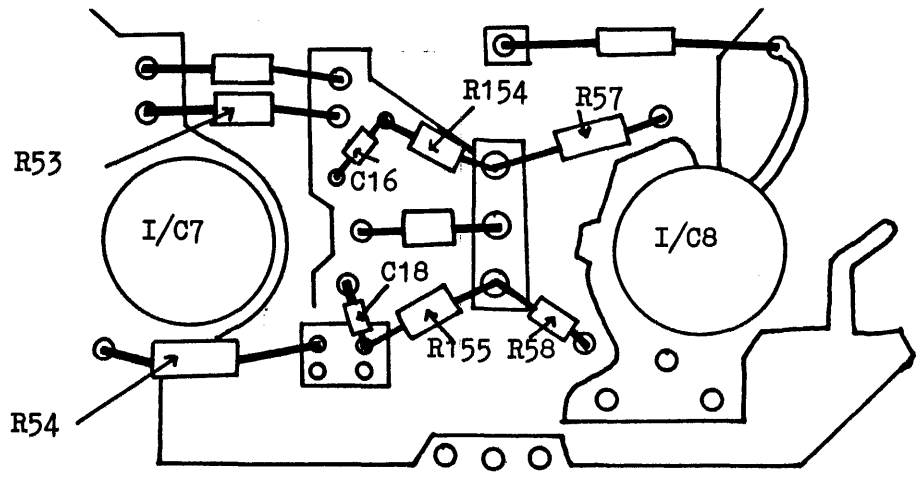

FIGURE 4.

10. Go to Step 12.

REVISION G SLAVE

11. Remove C13, C16, C18, R53, R54, R57, R58, TP16, TP17.
    Retain TP16, TP17, R57, R58, C13, C16, C18 for future use.

12. Cut four tracks and add two wires as shown in Figure 5.

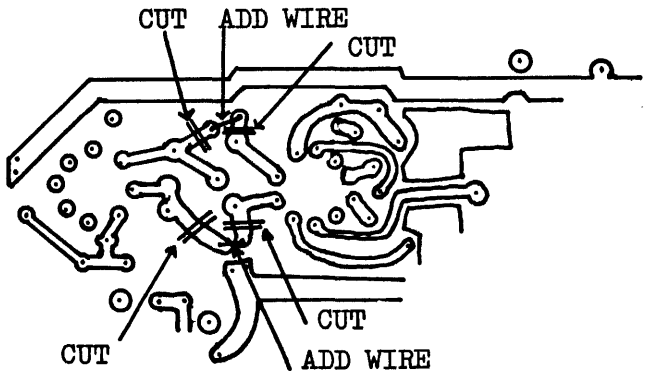

FIGURE 5.

13. Fit two 470 Ω resistors P/N 1876 5008 in the R53, R54 positions as shown in Figure 6.

14. Fit the two test points (TP16, TP17) in the right hand holes of the C16 and C18 positions (The holes nearest to I/C8)
    These test points will now be called the C16 and C18 pins.

15. Fit a 2KΩ resistor (R57 removed in Step 11) between R57 right-hand hole (hole nearest to I/C8) and the C16 pin.

16. Fit a 2K Ω resistor (R58 removed in Step 11) between R58 right-hand hole (hole nearest to I/C8 and the C18 Pin.

17. Fit a o.1 uF Capacitor (C16 removed in Step 11) between the R57 left hand hole (nearest to I/C 7) and the C16 Pin.

18. Fit a 0.1 uF Capacitor (C18 removed in Step 11) between the R58 left hand hole (nearest to I/C 7) and the C18 pin.

19. Fit a 510 pF Capacitor (C13 removed in Step 11) in the C17 position.

20. Fit a 200 uH choke (P/N 1103 0046) between the C16 left-hand hole (nearest to I/C 7) and the TP16 hole. Keep the choke leads as short as possible.

21. Fit a 200 uH choke (P/N 1103 0046) between the C18 left-hand hole (nearest to I/C7) and the TP17 hole.

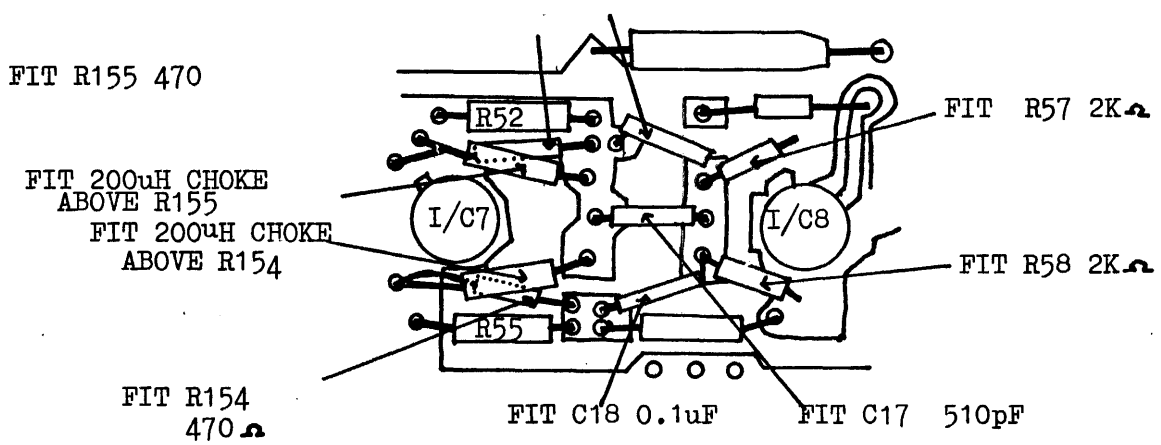

FIGURE 6.

22. Fit a 620pF capacitor (1877 2392) in the C13 position.

23. Update the schematics as shown in figure 3.

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES BDS	No. L2141-002
		STYLE/MODEL B9489-1/2	PAGE 1 OF 2
ORIGINATOR: ITIO GLENROTHES		TOP UNIT NO. 1878 9354	
STD. INSTALL. TIME Less than 1.5 Hrs	UNITS AFFECTED * See below	UNIT DESCRIPTION 1 M BYTE MINI-DISK	
TITLE IMPROVED MAINTAINABILITY			DATE 8 May 1977

INSTALLATION IS MANDATORY

* Units affected - up to serial number B200197-018

NOTE Some units will be returned to Glenrothes plant for rework that will incorporate this change. Reworked units will have a coloured label applied to the ID label. Consult your local technical support group before applying this LIN.

PREREQUISITE Unit must NOT be one of those listed at the end of this LIN. PCB artwork must be revision DE or F.

CONDITION Difficulty in maintaining the unit due to the large amount of rework on the PCB.

CORRECTION Install a new PCB.

PARTS REQUIREMENTS

Part Number	Description	Quantity	U.S. Unit List Price
1881 3840 or	Master PCB	1	$1212.39
1881 3857	Slave PCB	1	$ 832.93
1881 1448	Carriage Assy	1	$ 757.46

PROCEDURE

1) Check that the artwork revision (etched at location L1) is DE or F.

2) Install the new PCB.

3) Perform circumferential alignment as shown in ATI 130405.

4) Check PLL and data window adjustments. (Note: these are factory pre-set and should not require adjustment).

5) If read errors occur replace the carriage assembly and perform all adjustments.

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If the unit is one of those listed below DO NOT install this LIN.

B200006-018
B200008-018
B200017-018
B200065-018
B200066-018
B200071-018
B200085-018
B200087-018
B200094-018
B200095-018
B200100-018
B200101-018
B200103-018
B200105-018
B200110-018
B200118-018
B200120-018
B200124-018
B200125-018
B200133-018
B200134-018
B200147-018
B200148-018
B200151-018
B200154-018
B200156-018
B200163-018
B200171-018
B200187-018

BMG branches with one of these units should contact T.I.O. Central for further instructions. International branches with one of these units should contact I.T.I.O. Glenrothes for further instructions.

T.I.O. CENTRAL
Burroughs Corporation,
World Headquarters,
DETROIT
MICHIGAN.

I.T.I.O.
Burroughs Machines Ltd.,
Viewfield Industrial Estate,
Glenrothes,
Fife,
SCOTLAND.

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B80	NO. L2141-003
		STYLE/MODEL B9489-17-2	PAGE 1 OF 6
ORIGINATOR: ITIO GLENROTHES		TOP UNIT NO. 1878 9354	
STD. INSTALL. TIME 0.75 Hr	UNITS AFFECTED * See below	UNIT DESCRIPTION 1 M BYTE MINI-DISK	
TITLE SWITCHED FILTER			DATE 8 May 1977
INSTALLATION IS MANDATORY			

* Units affected - B200198-018 thru B201400-018.
- 15163006-8 thru 15163057-1.

NOTE Some units will be returned to Glenrothes plant for rework that will incorporate this change. Reworked units will have a coloured label applied to the ID label. Consult your local technical support group before applying this LIN.

PREREQUISITE L2141-001, L2141-002.

CONDITION Intermittent read errors at outer tracks.

CAUSE Incorrect frequency response of the read amplifier.

CORRECTION Install a switched filter. This filter lowers the cut-off frequency of the read amplifier at addresses 0 thru 31.

PARTS REQUIREMENTS

Part Number	Description	Quantity	U.S. Unit List Price
1877 1287	2200 pF Capacitor	2	$2.70
1269 9377	Wire solid 20 gauge	3 ft	$0.08/ft

PROCEDURE/

F.E. Dist Code BS

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FOR LIBRARY BINDER 343

FOR F.E. TECHNICAL MANUAL FORM 2102141

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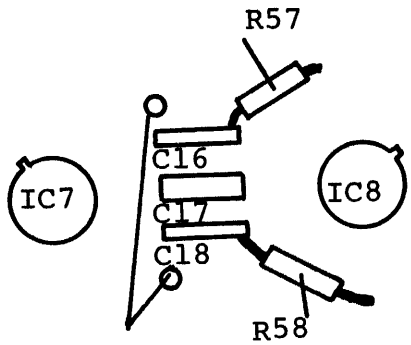
PROCEDURE.

1. Identify the artwork revision level of the circuit board. This is shown at location L1. For revisions H and J go to Step 2. For revision G go to Step 12.

2. Remove the non ground end of R57 from the PCB and connect it to the C16 lead as shown in Figure 1.

3. Remove the non ground end of R58 from the PCB and connect it to the C18 lead as shown in Figure 1.



NEW CAPACITORS MOUNTED THRU PADS
PREVIOUSLY OCCUPIED BY R57 and R58

FIGURE 1.

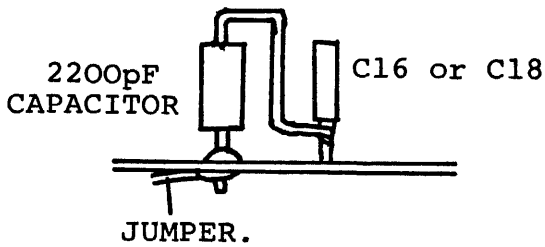


FIGURE 2.

4. Refer to Figures 1 and 2. Install a 2200pF Capacitor (P/N 1877 1287) vertically into the hole vacated by R57 in step 2.

5. Connect the other lead of the 2200 pF capacitor to the lead of C16.

6. Install a 2200 pF capacitor (P/N 1877 1287) vertically into the hole vacated by R58 in Step 3.

7. Connect the other lead of the 2200pF Capacitor to the lead of C18.

8. Install the following jumpers.

   IC1 Pin 12 to IC20 Pin 12.

   IC1 Pin 10 to IC20 Pin 9.

9. Install the following jumpers

   IC20 pin 10 to IC20 Pin 12 (Refer to Figure 3)
   IC20 pin 9 to IC20 Pin 13

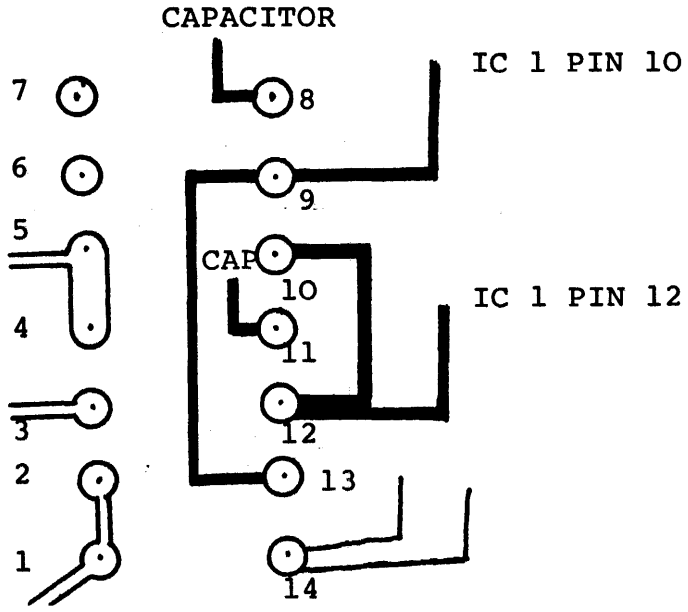


FIGURE 3

10. Install the following jumpers (Refer to figures 1, 2 and 3) IC20 Pin 8 to the PCB end of the Capacitor installed in steps 4.

    IC20 Pin 11 to the PCB end of the capacitor installed in steps 6.

11. Modify the schematics as shown in figures 4 and 5.

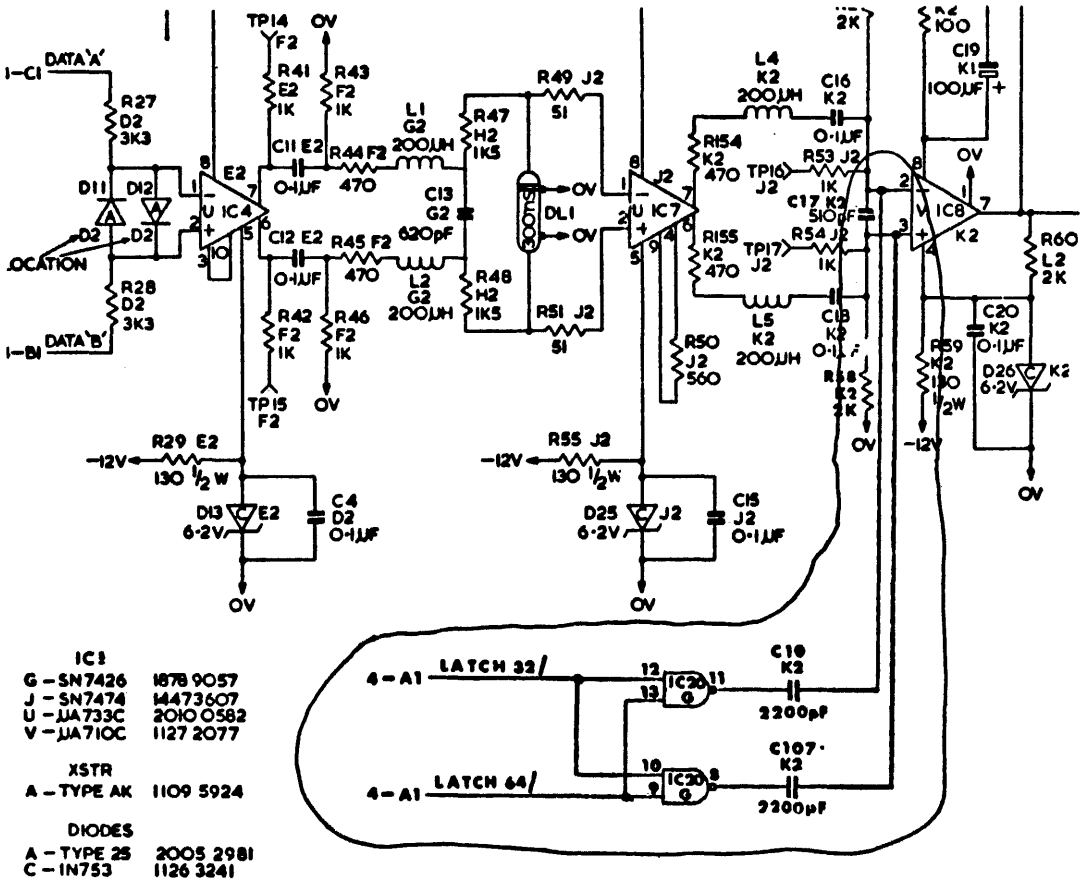


FIGURE 4

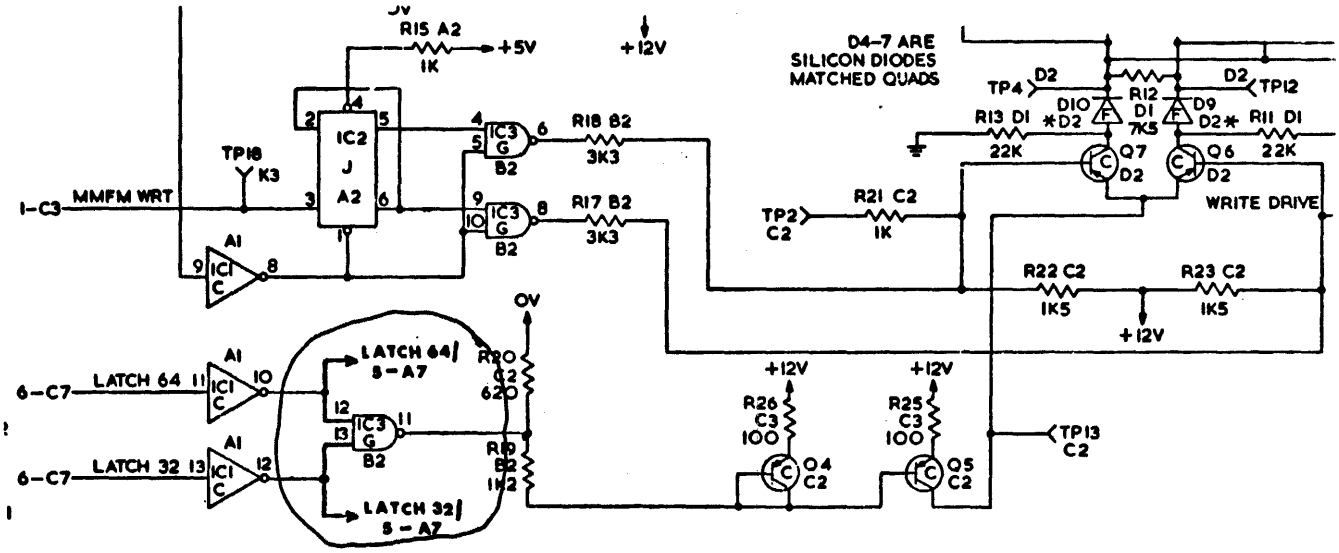


FIGURE 5

12. Check that artwork is at Revision G.

13. Install one 2200 pF capacitor (P/N 1877 1287) to each leg of C17 as shown in figure 6.

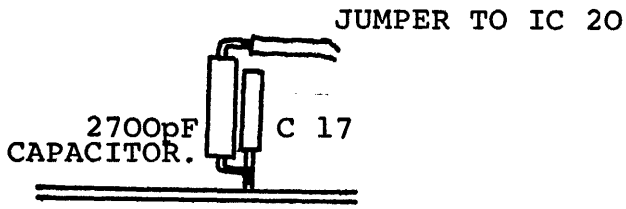


FIGURE 6

14. Install the following jumpers (Refer to Figure 3)

    IC1 Pin 12 to IC20 Pin 12.

    IC1 Pin 10 to IC20 Pin 9.

15. Install the following jumpers

    IC20 Pin 10 to IC20 Pin 12.

    IC20 Pin 9 to IC20 Pin 13.

16. Install the following jumpers (Refer to Figure 3 and 6)

    IC 20 Pin 8 to one capacitor installed in step 14.

    IC20 Pin 11 to the other capacitor installed in step 14.

17. Update schematics as shown in figures 4 and 5.

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B80	NO. L2141-004
		STYLE/MODEL B9489-1/-2	PAGE 1 OF 6
ORIGINATOR: ITIO GLENROTHES		TOP UNIT NO. 1878 9354	
STD. INSTALL. TIME 1 HOUR	UNITS AFFECTED * Below	UNIT DESCRIPTION 1 M BYTE MINI DISK	
TITLE WRITE ENABLE DELAY, POSSIBLE CLOCK AND HEAD ADDRESS MODIFICATION			DATE 8 May 1977
INSTALLATION IS MANDATORY			

* Units affected - Below B203500-018
- Below 15163057-1

NOTE Some units will be returned to Glenrothes plant for rework that will incorporate this change. Reworked units will have a coloured label applied to the ID label. Consult your local technical support group before applying this LIN.

PREREQUISITE LIN L2141-001, L2141-002 and L2141-003.

CONDITION Incomplete edge erase at end of sector. Possibility of heads moving or address select changing before the end of erase.

CORRECTION Install the changes provided in this LIN.

PARTS REQUIREMENTS

Part Number	Description	Quantity	U.S. Unit List Price
1876 4910	Resistor 200 ohms ¼w	1	$ 0.972
1876 5362	Resistor 15k ohms ¼w	1	$ 0.972
1876 5479	Resistor 43k ohms ¼w	1	$ 0.972
1876 5545	Resistor 82k ohms ¼w	1	$ 0.972
1874 7616	Capacitor 2.2 µF	1	$ 3.619
1876 9919	Capacitor 0.22 µF	1	$10.989
1877 0578	Capacitor 6.8 µF	1	$ 3.10
1269 9377	Wire solid 20 Gauge	2 ft	$ 0.08/ft

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PROCEDURE.

1. Check that the PCB artwork revision (located at L1) is at Revision G, H or J.

2. Replace C1 by a 2.2 μF capacitor (P/N 1876 7616). Observe the polarity of the capacitor and install as shown in figure 1.

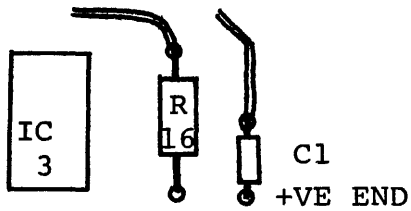

FIGURE 1.

3. Update the schematic as shown in figure 2

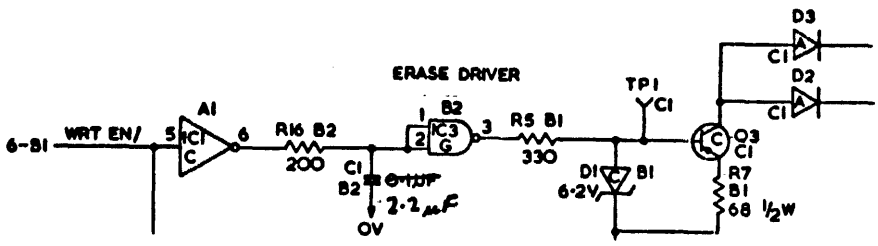

FIGURE 2.

4./

4. Replace C49 by a 0.22 μF capacitor (P/N 1876 9919)

5. Replace R74 by a 15KΩ resistor (P/N 1876 5362)

6. Replace R75 by a 43KΩ resistor (P/N 1876 5479)

7. Replace R76 by a 82 KΩresistor (P/N 1876 5545)

8. Update the schematic as shown in figure 3.

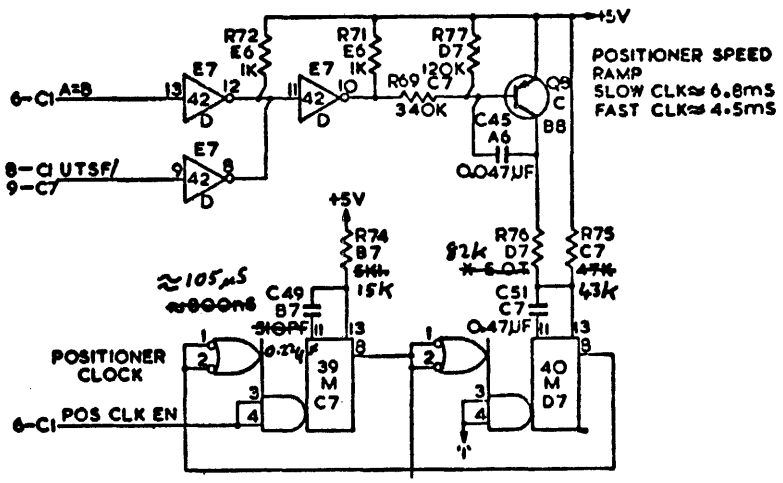

FIGURE 3

9. Cut the etching on both sides of the PCB between pins 3 and 4 of IC 33.
NOTE: check with a suitable meter to ensure that the etching has been cut completely

10. Cut the etching on the non-component side of the board at the rear of IC 33 (location D6) as shown in figure 4.

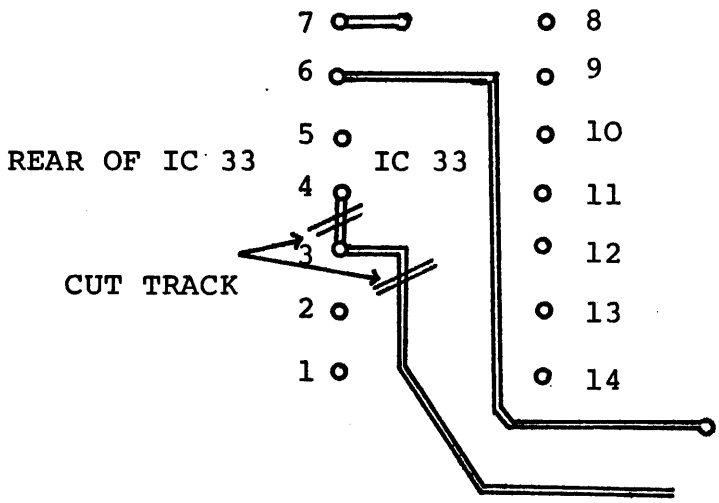

FIGURE 4.

11. Install a jumper wire from IC40 Pin 6 to IC 33 Pin 3.

12. Install a jumper wire from IC24 Pin 6 to IC33 Pin 4.

13. Update the schematic as shown in figure 5.

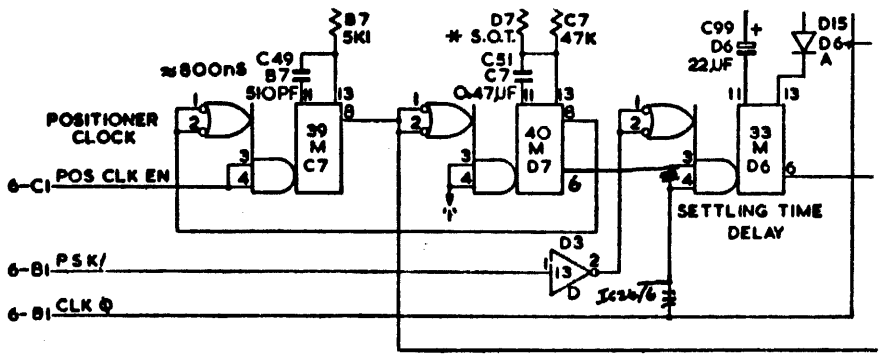

FIGURE 5

14. Cut the etching on the component side of the PCB at location G3 as shown in Figure 6.

15. Install a 200Ω resistor (P/N 1876 4910) on the component side of the PCB as shown in Figure 6.

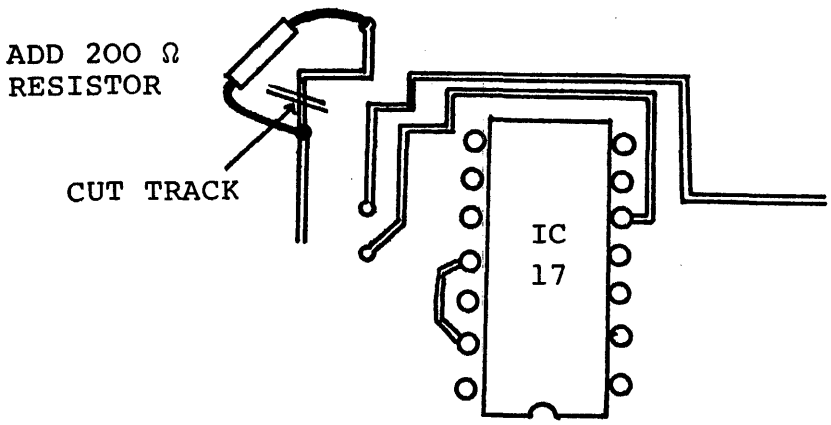

FIGURE 6.

16. Install a 6.8µF capacitor (P/N 1877 0578) on the component side of the PCB at Location A2 as shown in figure 7.

NOTE: Observe polarity of the Capacitor.

17. Update the schematics as shown in figure 8.

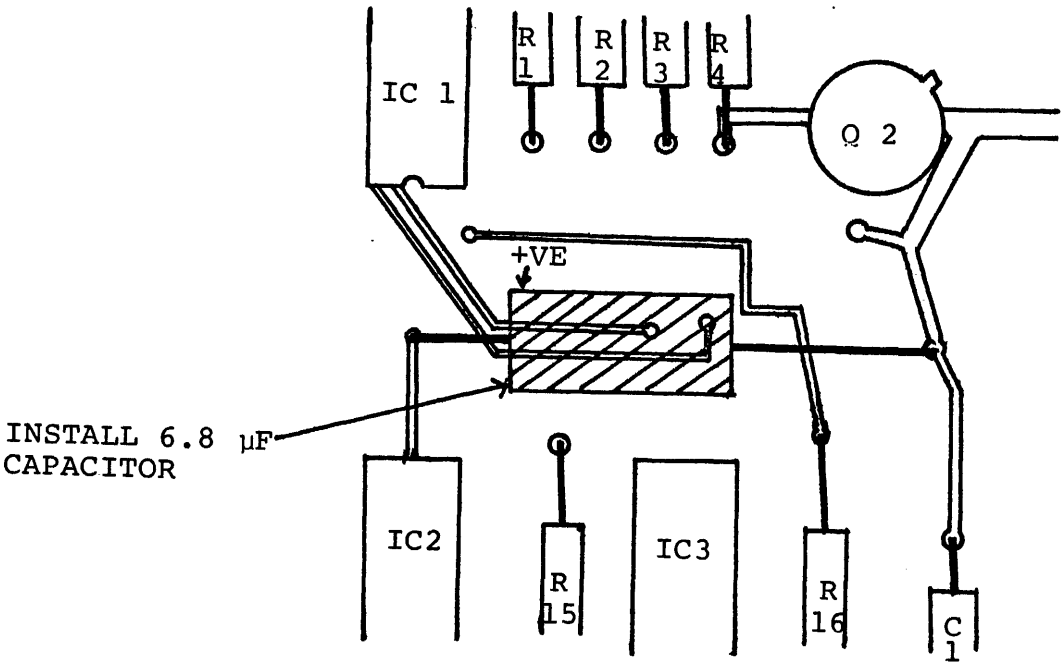

FIGURE 7.

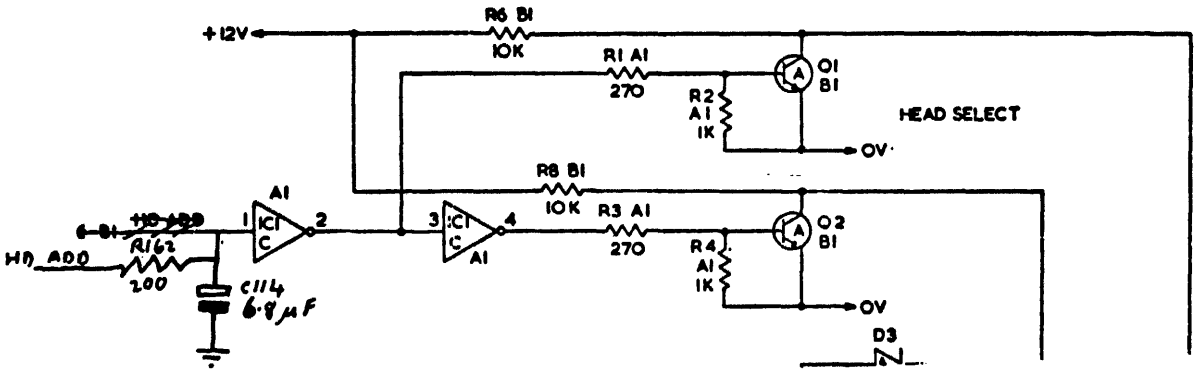

FIGURE 8

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B80	No. L2141-005
		STYLE/MODEL B9489-1/-2	PAGE 1 OF 2
ORIGINATOR: ITIO GLENROTHES		TOP UNIT NO. 1878 9354	
STD. INSTALL. TIME 0.25 HR	UNITS AFFECTED * See below	UNIT DESCRIPTION 1 M BYTE MINI-DISK	
TITLE FALSE WRITE ENABLE INDICATION			DATE 8 May 1977

INSTALLATION IS MANDATORY

* Units affected - All units with artwork revision GH or J.

NOTE Some units will be returned to Glenrothes plant for rework that will incorporate this change. Reworked units will have a coloured label applied to the ID label. Consult your local technical support group before applying this LIN.

PREREQUISITE PCB artwork must be at revision G, H or J.

CONDITION Write Enable indicator lights when door is open and there is no media present.

CAUSE WIH transducer alignment may cause insufficient light to fall on the sensor when the door is opened.

CORRECTION Gate WIH with FILE OP. The Write Enable indicator will not light until the FILE OP indicator is lit. To maintain compatibility with units with artwork revision K and greater and to avoid operator confusion, this change must be installed on all units.

PARTS REQUIREMENTS

Part Number	Description	Quantity	U.S. Unit List Price
1269 9377	Wire solid 20 gauge	1 ft	$0.08/ft

PROCEDURE

1) Cut the etching between pins 1 and 2 of IC45.
2) Add a wire from IC27 pin 10 to IC45 pin 1.
3) Update the schematics as shown.

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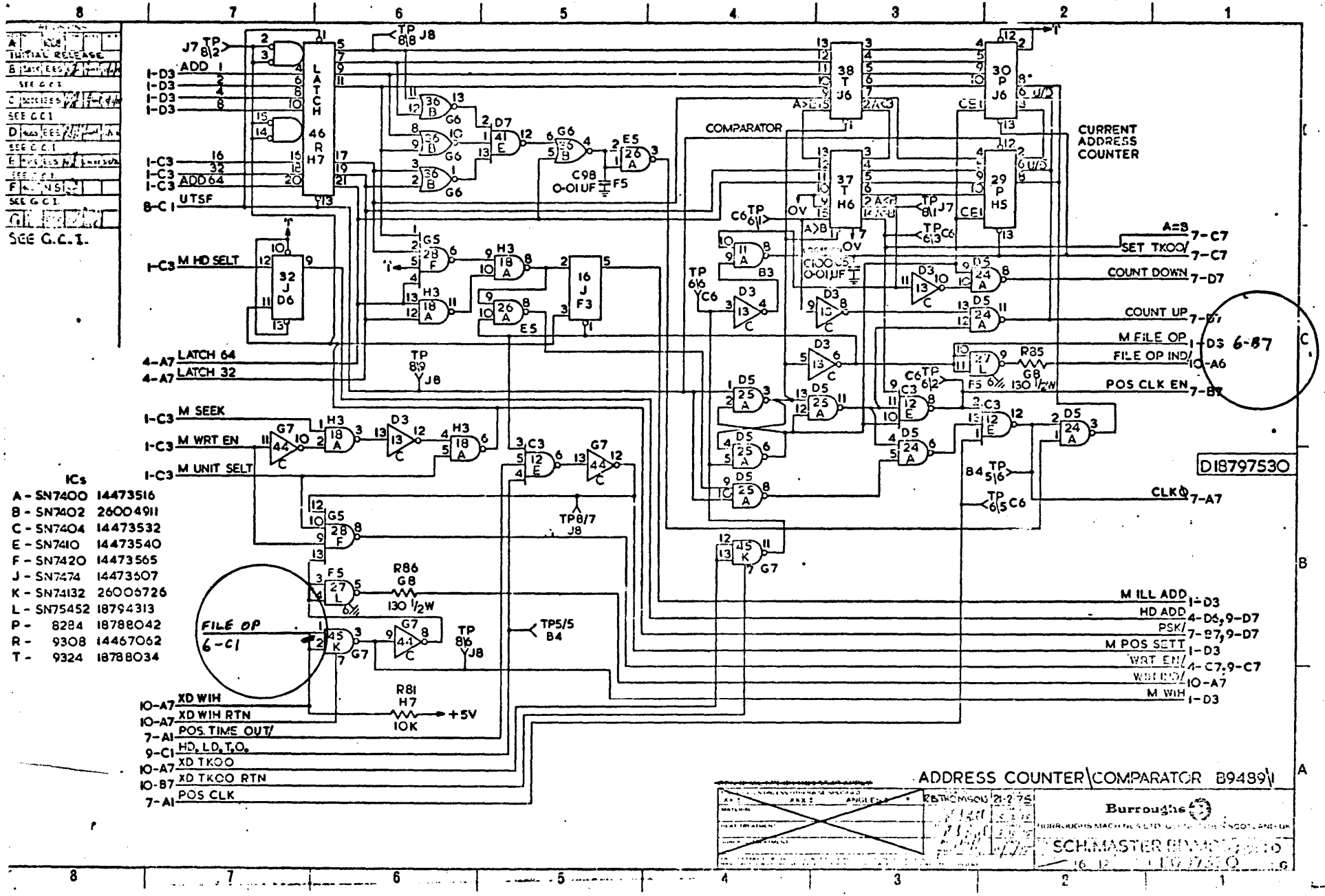
ADDRESS COUNTER\COMPARATOR B9489\1
D18797530
CURRENT ADDRESS COUNTER
COMPARATOR
FILE OP 6-C1
SEE G.C.I.
ICs
A - SN7400 14473516
B - SN7402 26004911
C - SN7404 14473532
E - SN7410 14473540
F - SN7420 14473565
J - SN7474 14473607
K - SN74132 26006726
L - SN75452 18794313
P - 8284 18788042
R - 9308 14467062
T - 9324 18788034
I-D3 ADD 1
I-D3 2
I-D3 4
I-D3 8
I-C3 16
I-C3 32
I-C3 ADD64
8-C1 UTSF
I-C3 M HD SELT
4-A7 LATCH 64
4-A7 LATCH 32
I-C3 M SEEK
I-C3 M WRT EN
I-C3 M UNIT SELT
10-A7 XD WIH
10-A7 XD WIH RTN
7-A1 POS TIME OUT/
9-C1 HD, LD, T, O,
10-A7 XD TKOO
10-B7 XD TKOO RTN
7-A1 POS CLK
A=B 7-C7
SET TKOO/ 7-C7
COUNT DOWN 7-D7
COUNT UP 7-D7
M FILE OP 1-D3
FILE OP IND/ 10-A6
POS CLK EN 7-B7
CLK 7-A7
M ILL ADD 1-D3
HD ADD 4-D6,9-D7
PSK/ 7-B7,9-D7
M POS SETT 1-D3
WRT EN/ 4-C7,9-C7
WRT DO/ 10-A7
M WIH 1-D3
C98 0-01UF F5
C100 0-01UF
R81 H7 10K +5V
R86 G8 130 1/2W
R85 G8 130 1/2W
TP8/7 J8
TP5/5 B4
LATCH 46 R H7
38 T J6
30 P J6
37 T H6
29 P H5
32 J D6
16 J F3
Burroughs
SCHMASTER BOARD
LIN L2141-005
Page 2 of 2

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B80	No. L2141-006
		STYLE/MODEL A/B 9489-2	PAGE 1 OF 2
ORIGINATOR: TIO GLENROTHES		TOP UNIT NO. 1879 4503	
STD. INSTALL. TIME 0.5 HOURS	UNITS AFFECTED * SEE BELOW	UNIT DESCRIPTION 1 M BYTE MINIDISK DRIVE (SLAVE)	
TITLE MISSING ARTWORK ON REV K SLAVE BOARDS			DATE 19 September 1977
INSTALLATION IS MANDATORY			

* UNITS AFFECTED - All slave units with P.C.B. artwork revision K.

PREREQUISITE: P.C.B. artwork must be revision K.

CONDITION: Errors during recalibration.

CAUSE: Missing capacitor ground (C100, location C5).

CORRECTION: Add the necessary grounding link.

TOOLS REQUIRED: Soldering iron
Wire cutters.

PARTS REQUIRED:

Part Number	Description	Qty.	U.S.List Price
1269 9377	26 A.W.G. Wire	2 ins	$0.02

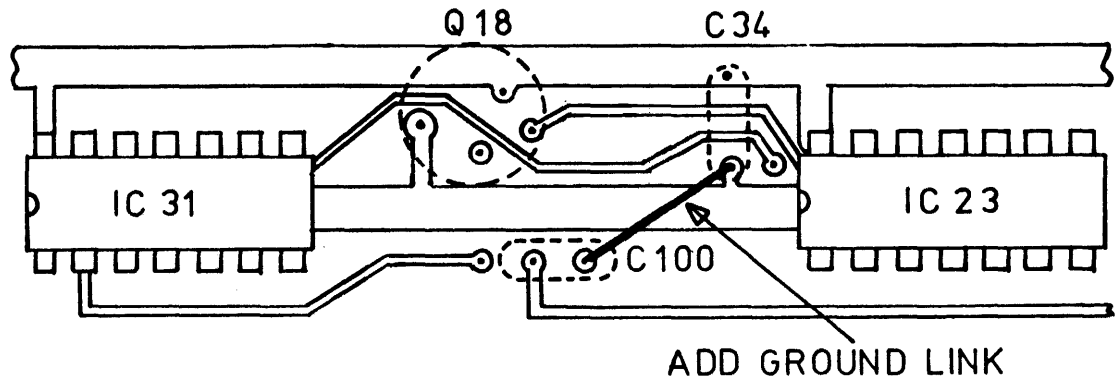

FIGURE 1 COMPONENT SIDE REWORK

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PROCEDURE

1) Remove the slave unit from the B-80.

2) On component side, location C5, add a jumper wire between the end of C100 nearest IC 23 and the ground at C34. (Refer Figure 1)

3) Replace drive in the B-80 and run an operational check.

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B800 only	NO. L2141-007
		STYLE/MODEL B9489	PAGE 1 OF 2
ORIGINATOR: T.I.O. GLENROTHES		TOP UNIT NO. *	
STD. INSTALL. TIME: 0.5 HR.	UNITS AFFECTED ALL	UNIT DESCRIPTION 1 MB MINI DISK DRIVE UNIT	
TITLE: INCREASED VALUE FOR READ ENABLE DELAY(GCI 5159)			DATE: 12 May 1978
INSTALLATION IS MANDATORY			

NOTE:- This LIN need not be removed if Drive Units are subsequently fitted to a B80 System.

* TOP UNIT NUMBERS

1878 9347	1881 2644
1879 4503	1881 2651
1881 0184	1881 0192

PREREQUISITE: None.

CONDITION: The present value of Read Enable Delay (43 us) is insufficient to allow the Phase Locked Loop to lock-on.

CORRECTION: The Read Enable Delay is increased from its nominal value of 43 us to 150 us

PARTS REQUIREMENTS:

PART NUMBER	DESCRITPION	QTY.	U.S.UNIT LIST PRICE
1876 5487	Resistor 47K, ¼W	1	$ 0.251

INSTRUCTIONS:-

1. Switch off the power to the Host System.
2. Remove the disk drive unit from the Host System.
3. Remove the master board from the drive unit.
4. /

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INSTRUCTIONS cont.

4. Replace resistor R 93 at location 2Q with a 47K ohm resistor.
5. Refit the master board to the drive unit.
6. Refit the disk drive unit to the Host System.
7. Switch on the power to the Host System.
8. Carry out an operational check of the System.
9. Amend the schematics to reflect the change.

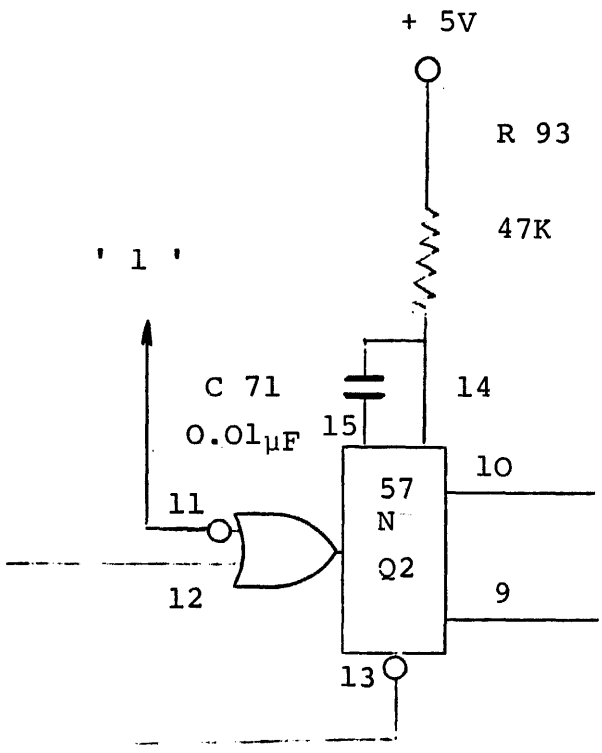

FIGURE 1: READ ENABLE DELAY (150 µs)

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B 800 - Only	NO. L2141-008
		STYLE/MODEL B 9489	PAGE 1 OF 2
ORIGINATOR: T.I.O. GLENROTHES		TOP UNIT NO. *	
STD. INSTALL. TIME 0.5 HR.	UNITS AFFECTED ALL	UNIT DESCRIPTION 1 MB MINI DISK DRIVE - UNIT.	
TITLE INDEX/SECTOR PULSE DURATION (G.C.I. 4986)			DATE 30 May 1978
INSTALLATION IS MANDATORY			

NOTE:- This LIN need not be removed if Drive units are subsequently fitted to a B80 system.

* TOP UNIT NUMBERS

1878 9347	1881 2644
1879 4503	1881 2651
1881 0184	1881 0192

PREREQUISITE: None.

CONDITION:- The present value for the Index/Sector pulse duration is too long.

CORRECTION:- The Index/Sector pulse duration is decreased from its nominal value of 1.8 µs to 1 µs.

PARTS REQUIREMENTS:-

PART NUMBER	DESCRIPTION	QTY	U.S.UNIT LIST PRICE
1876 5321	RESISTOR 10K, ¼W	1	$ 0.269

INSTRUCTIONS:/

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INSTRUCTIONS:

1. Switch off the power to the Host System.
2. Remove the disk drive unit from the Host System.
3. Remove the P.C.B. from the drive unit.
4. Replace resistor R62 at location A4 with a 10K ohm resistor.
5. Refit the P.C.B. to the drive unit.
6. Refit the disk drive unit to the Host System.
7. Switch on the power to the Host System.
8. Carry out an operational check of the System.
9. Amend the schematics to reflect the change.

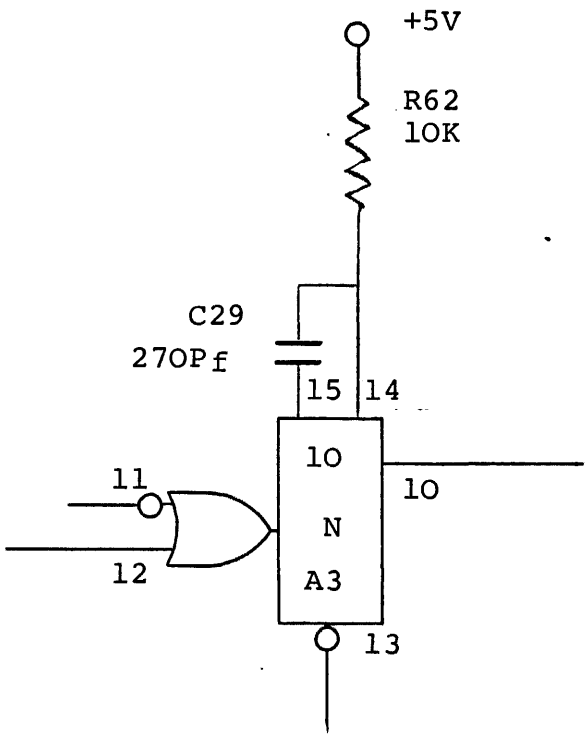

FIGURE 1: INDEX/SECTOR 1 µs PULSE GENERATOR.

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B80, B800	NO. L 2141-009
		STYLE/MODEL B9489	PAGE 1 OF 3
ORIGINATOR: T.I.O. GLENROTHES		TOP UNIT NO. *	
STD. INSTALL. TIME 1 HOUR	UNITS AFFECTED **	UNIT DESCRIPTION 1 M BYTE MINI DISK DRIVE UNIT	
TITLE READ ERRORS AFTER WRITE (G.C.I. 4720)			DATE 21 NOVEMBER 78
INSTALLATION IS MANDATORY			

* TOP UNIT NOS.

1878 9347	1879 4503
1881 2644	1881 2651
1881 0192	1881 0184

** UNITS AFFECTED BELOW SER NO. 207000 (GLENROTHES UNITS)
BELOW SER NO. 15165236 (GUADALAJARA UNITS)

PREREQUISITE: Revision'K' circuit board, level 10 and below.

CONDITION: Errors in read after write.

CAUSE: The erase current decay is generating noise on read data.

CORRECTION: Modify the circuit to reduce the write enable delay and to limit the rate of decay of the erase current.

PARTS REQUIRED

PART NUMBER	DESCRIPTION	QTY	UNIT LIST PRICE
1876 4969	Resistor 330 ohms, 2%	1	$0.34
1876 5206	Resistor 3.3K, 2%	1	$0.34
1877 1030	Capacitor 0.47µF,10% 35V	1	$1.87

PROCEDURE

A. Remove the circuit board from the Master and/or the Slave Unit and perform the following changes on the board(s).

1. Remove the capacitor C115, from location C1.

2. Remove the capacitor C116, from location C1.

3./

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PROCEDURE cont.

A. 3. Remove the diode D1, from location B1.

4. Remove the resistor R161, from location A6.

5. Install the resistor R161,P/N 1876 5206,at Location A6.

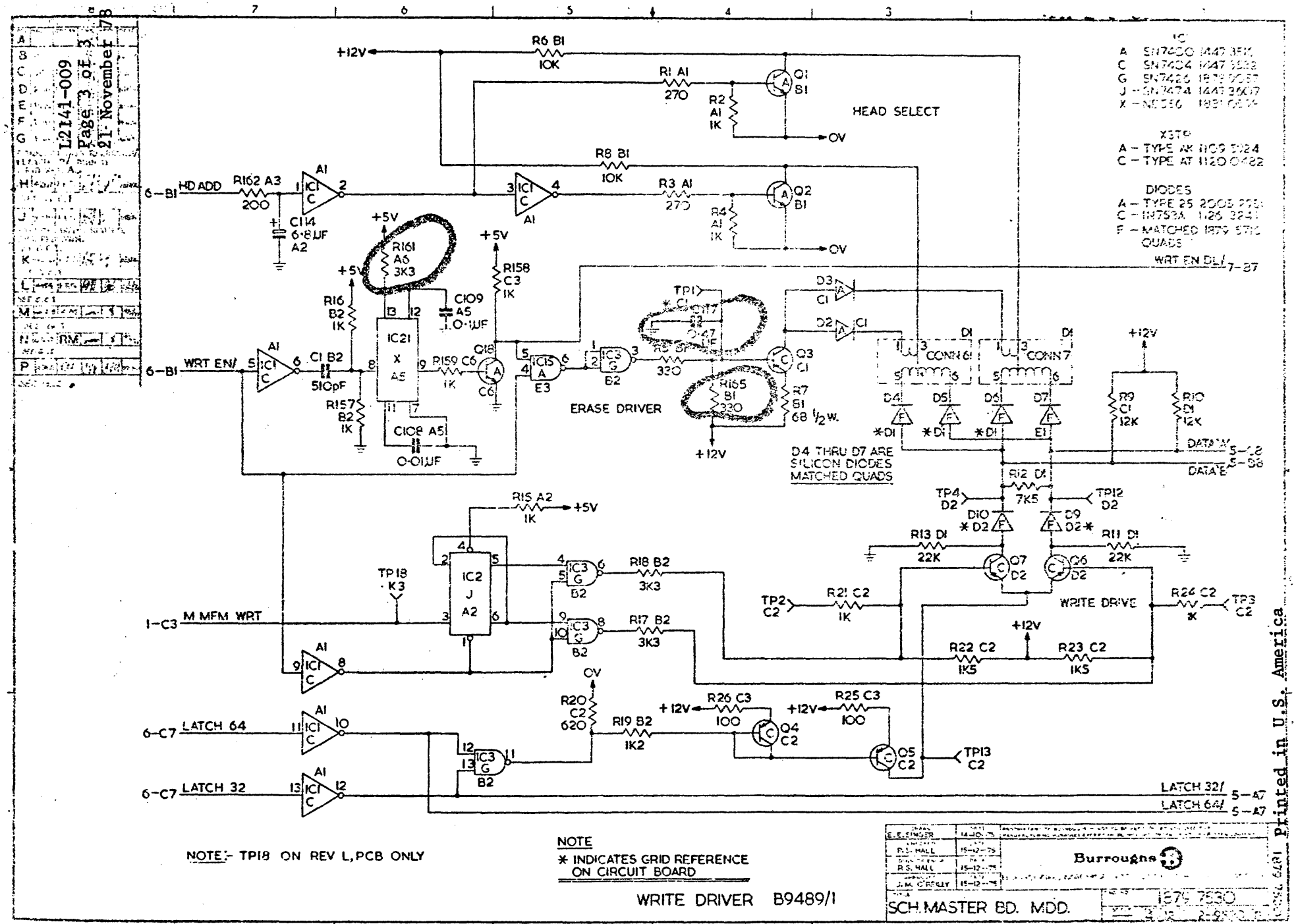
6. Install the resistor R165,P/N 1876 4969, at Location B1 (in place of D1)

7. Install the capacitor C117, P/N 1877 1030, from TP-1 to OV (Ground)

B. Replace the circuit board in the Master and/or the Slave Unit.

C. Perform an operational check of the system.

D. Update page 4 and/or Page 2 of the Master and/or Slave Logic schematic as shown on Page 3 .


L2141-009 Page 3 of 3 21 November 78
+12V
R6 B1 10K
R1 A1 270
R2 A1 1K
Q1 B1
HEAD SELECT
OV
R8 B1 10K
R3 A1 270
R4 A1 1K
Q2 B1
6-B1 HD ADD
R162 A3 200
C114 6·8µF A2
+5V
R161 A6 3K3
R158 C3 1K
R16 B2 1K
C109 A5 0·1µF
IC21 X A5
WRT EN/
C1 B2 510pF
R159 C6 1K
Q18 C6
R157 B2 1K
C108 A5 0·01µF
IC1 A E3
IC3 G B2
TP1 C1
C117 B2 0·47µF
R5 B1 330
R165 B1 330
Q3 C1
R7 B1 68 1/2W.
ERASE DRIVER
D3 C1
D2 C1
CONN6
CONN7
D4 D5 D6 D7 E1
*D1
R9 C1 12K
R10 D1 12K
DATA W 5-28
DATA E 5-58
D4 THRU D7 ARE SILICON DIODES MATCHED QUADS
R12 D1 7K5
TP4 D2
TP12 D2
D10 *D2
D9 D2*
R13 D1 22K
R11 D1 22K
Q7 D2
Q6 D2
WRITE DRIVE
R15 A2 1K
TP18 K3
IC2 J A2
1-C3 M MFM WRT
R18 B2 3K3
R17 B2 3K3
TP2 C2
R21 C2 1K
R24 C2 *
TP3 C2
R22 C2 1K5
R23 C2 1K5
R20 C2 620
R19 B2 1K2
R26 C3 100
R25 C3 100
Q4 C2
Q5 C2
TP13 C2
6-C7 LATCH 64
6-C7 LATCH 32
LATCH 32/ 5-A7
LATCH 64/ 5-A7
WRT EN DL/ 7-B7
IC
A SN7400 N
C SN7404 N
G SN7426 N
J SN7474 N
X NE556 N
XSTR
A - TYPE AK 1109 5224
C - TYPE AT 1120 0482
DIODES
A - TYPE 25 2005 2251
C - IN753A 1126 3241
F - MATCHED 1879 5711 QUADS
NOTE:- TP18 ON REV L,PCB ONLY
NOTE
* INDICATES GRID REFERENCE ON CIRCUIT BOARD
WRITE DRIVER B9489/1
E.E.FINGER
P.S. HALL
P.S. HALL
J.M. O'REILLY
Burroughs
SCH. MASTER BD. MDD.
1879 7530
Printed in U.S.A. America

Burroughs FIELD ENGINEERING	LOGIC IMPROVEMENT NOTICE	SYSTEM SERIES B80, B800	NO. L2141-010
		STYLE/MODEL B 9489	PAGE 1 OF 3
ORIGINATOR: T.I.O.GLENROTHES		TOP UNIT NO. *	
STD. INSTALL. TIME 1 HOUR	UNITS AFFECTED **	UNIT DESCRIPTION 1 M BYTE MINIDISK DRIVE UNIT	
TITLE TO ALLOW USE OF UNSELECTED PHASE LOCKED LOOP I.C.			DATE 7 August 1978

INSTALLATION IS MANDATORY

* TOP UNIT NOS.

1878 9347 1879 4503
1881 2644 1881 2651
1881 0192 1881 0184

* UNITS AFFECTED: Below Ser. No. 205950 (Glenrothes Units)
Below Ser. No. 15165236 (Guadalajara Units)

PREREQUISITE: Revision 'K' circuit board, level 10 and below.

CONDITION : Difficult to adjust the Phase Locked Loop and Data Window.

CAUSE: Unselected phase locked loop integrated circuit.

CORRECTION: Modify the circuit to allow the replacement of the phase locked loop integrated circuit.

PARTS REQUIRED:

PART NUMBER	DESCRIPTION	QTY.	UNIT LIST PRICE $
1876 5156	Resistor 2K, 2% ¼W	1	$ 0.34
1876 5412	Resistor 24K,2% ¼W	1	$ 0.34
1877 2087	Capacitor 39pF, 5% 500V	1	$ 0.68
1877 2335	Capacitor 390pF,5% 500V	1	$ 1.36
1877 2392	Capacitor 620pF,5% 300V	1	$ 1.70

PROCEDURE:

A. Check the Phase Locked Loop and Data Window adjustment as per A.T.I. 130405. (REV)

B. Remove the circuit board from the Master Unit and perform the following changes on the board.

1. Remove the resistor R112 from location P4.
2./

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PROCEDURE cont.

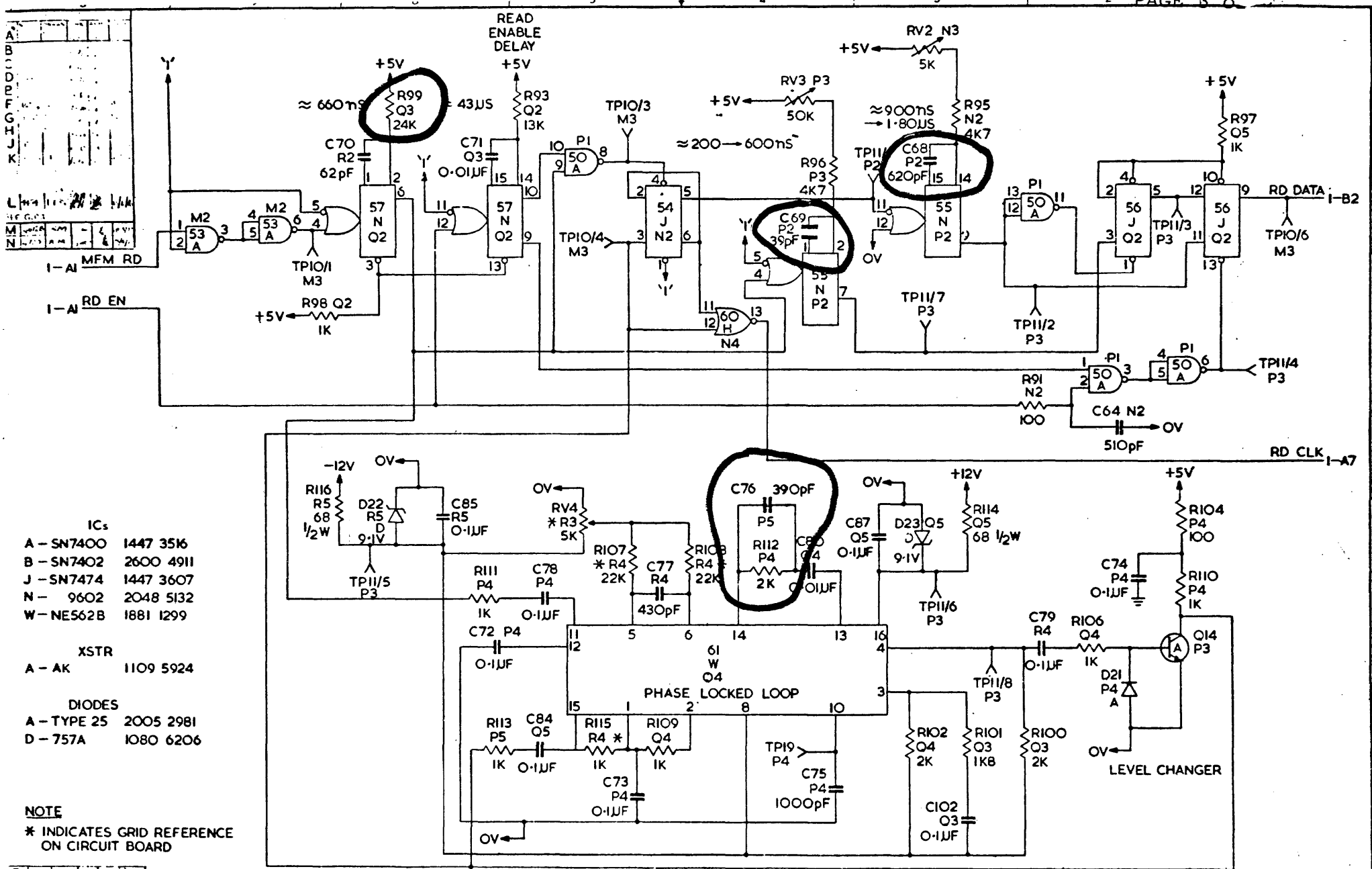
B.

2. Remove the capacitor C76 from Location P5.
3. Remove the resistor R99 from Location Q3.
4. Remove the capacitor C68 from Location P2.
5. Install the resistor R112, P/N 1876 5156 at Location P4.
6. Install the capacitor C76, P/N 1877 2335 at Location P5.
7. Install the resistor R99, P/N 1876 5412 at Location Q3.
8. Install the capacitor C68, P/N 1877 2392 at Location P2.
9. Install the capacitor C69, P/N 1877 2087 at Location P2. (between pins 1 and 2 of I.C. 55.)

C. Replace the circuit board in the Master Unit.

D. Perform the Phase Locked Loop (P.L.L.) and Data Window adjustments as per A.T.I. 130405.(REV).

E. Update page 2 of the Logic Schematic as shown on page 3 of 3



ICs	
A – SN7400	1447 3516
B – SN7402	2600 4911
J – SN7474	1447 3607
N – 9602	2048 5132
W – NE562B	1881 1299

XSTR	
A – AK	1109 5924

DIODES	
A – TYPE 25	2005 2981
D – 757A	1080 6206

NOTE

* INDICATES GRID REFERENCE ON CIRCUIT BOARD

NOTE: TP19 ON REV L, PCB ONLY

DRAWN R.B. THOMSON	DATE 17-2-75	PROPRIETARY TO BURROUGHS - NOT TO BE REPRODUCED NOR USED FOR MANUFACTURING PURPOSES EXCEPT ON BURROUGHS ORDER OR PER CONTRACT
CHECKED P.S. HALL	DATE 15-12-75	Burroughs
ENGINEERING P.S. HALL	DATE 15-12-75	
APPROVED J.M. O'REILLY	DATE 15-12-75	

READ DATA DECODE B9489/1

SCH. MASTER BD. MDD.

DWG NO 1879 7530

SIZE A | SCALE 2-5520 | SHEET 3 OF 5

1879 7530