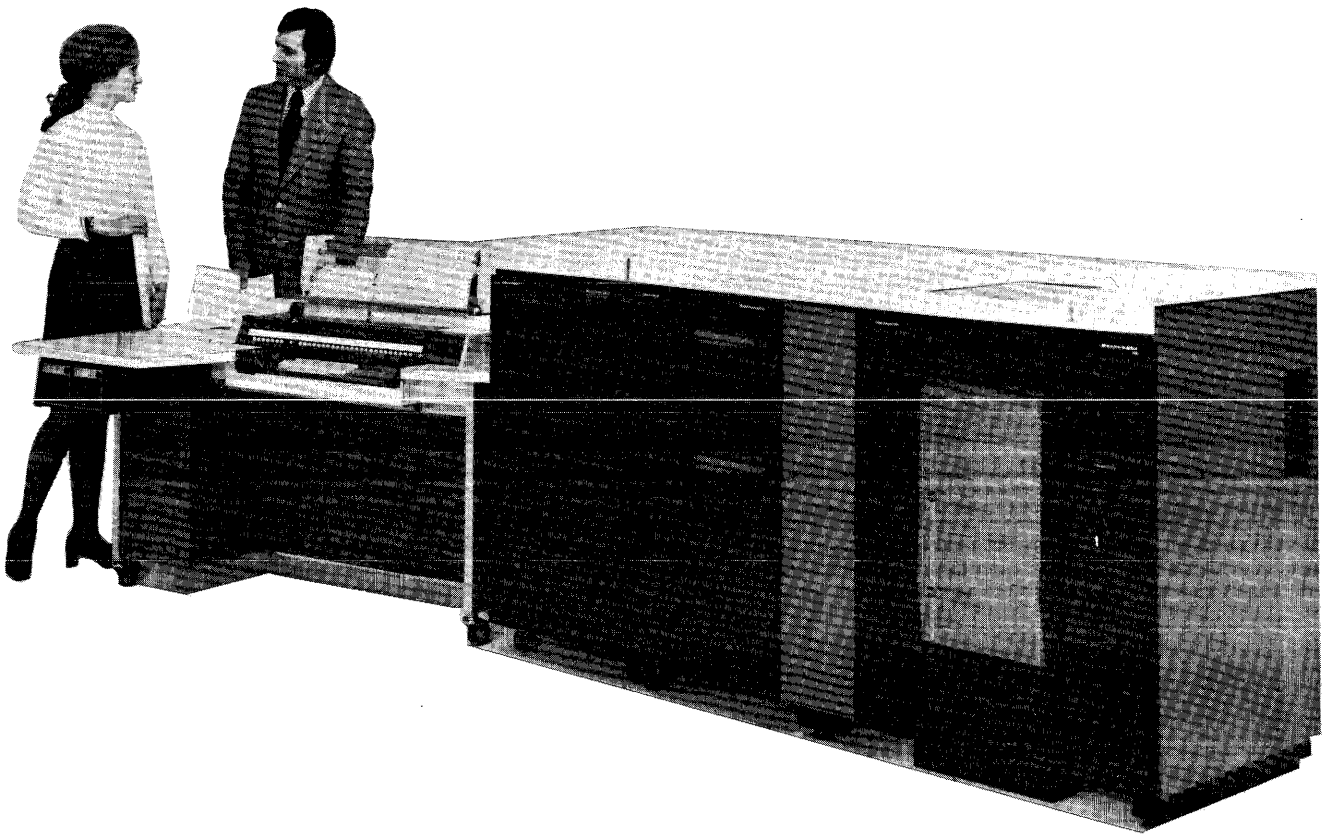
Burroughs

B 705/711 SYSTEMS



Performance Oriented Training Course

Printed in U. S. America 3-5-75

Form 1083441

BURROUGHS CORPORATION
FIELD ENGINEERING TRAINING
DETROIT, MICH.

BMG . . . . . COURSE NO: 320600
INTERNATIONAL . . . . . COURSE NO: 394482

B705/711 COURSE TABLE OF CONTENCE

TABLE OF CONTENCE

COURSE MATRIALS

For each Field Engineer

B700 F.E.T.M.
B700 S.O.G.
B700 REF. MAN.
SERIES B700 HANDBOOK

Available in lab.

B700 M.T.R.
B700 F.T.&R.

COURSE OUTLINE

TITLE: B705/711 SYSTEMS

DESIGNATION: 320600

LENGTH: 112 HOURS

OBJECTIVE: At the conclusion of the course, the Field Engineer should be able to analyze, isolate, and repair electronic or mechanical failure in the B705/711 system. This should be accomplished with little or no assistance.

SUBJECT MATTER:

Ref: New Product Announcement and T.M. Sec. I	I. INTRODUCTION A. Application B. Characteristics	LEC. 0.5 LAB **0.0**
Ref: Micro Base Computer Systems	II. SYSTEM CONCEPT A. Programming B. High Level Language C. Compilers D. System Language E. Micro Programming Language	LEC. 1.5 LAB 0.0
Ref:	III. SYSTEM DEMONSTRATION A. Utilities B. Application Program	LEC. 0.0 LAB 1.0
Ref: Ref. Man, Sec. I, and T.M. SecI	IV. SYSTEM SOFTWARE A. System Language 7 B. Interpreter	LEC. 2.0 LAB 0.0

COURSE OUTLINE

SUBJECT MATTER:
-CONTINUED-

Ref: Ref. Man. Sec. V,VIII and T.M. Sec I and S.O.G. 2

V. SYSTEM INITIALIZATION — LEC. 2.0 LAB 2.0

- A. Cold Start
- B. Warm Start
- C. Re-Start
- D. Memory Allocation
- E. Disk Allocation
- F. Operation

Ref: S.O.G. and Ref. Man.

VI. SYSTEM OPERATION — LEC. 4.0 LAB 8.0

- A. System Power On
- B. Console/SPO
  1. Functions
  2. Operation
     - a. Keyboard
       - (1) PK's
       - (2) Alpha/Numeric
       - (3) Numeric
     - b. Memory Loader
- C. DISK
  1. Cautions
  2. Back-up
- D. Optional Peripherals
- E. Systems Messages
  1. Error Messages
  2. Recovery Procedures
- F. Utilities
- G. Object Program Card Formats
- H. Break-Out/Resume
- I. Discontinue/Wait
- J. Trace
- K. Dump

Ref: T.M. SecI,III, VI AND Trng. Supp.

VII. FUNCTIONAL BLOCK DIAGRAM — LEC. 4.0 LAB 0.5

- A. Backplane Layout
- B. C.P.U./T.P.U.
- C. Processor Logic Register Diagram
- D. Operational Block Diagram

COURSE OUTLINE

SUBJECT MATTER:
-CONTINUED-

Ref:	T.M. Sec III and F.T.&R	VIII.	DOCUMENTATION A. F.T.& R B. Logic Elements C. MTR D. RIN, TIN, LIN, CARES	LEC. 2.0 LAB 2.0
Ref:	T.M. Sec II and F.T.&R.	IX.	POWER A. Functional Block B. AC 1 & 2 C. Power Supply D. Adjustments E. Troubleshooting and Hints F. B721	LEC. 4.0 LAB 6.0
Ref:	T.M. Sec V	X.	F.E. BOARDS A. Functional Description B. Operation C. Troubleshooting	LEC. 3.0 LAB 2.0
Ref:	T.M. Sec II	XI.	CORE MEMORY A. General Description B. Ferro-Magnetic Principles C. Addressing D. Write E. Read F. Parity Generation and Checking G. Memory Power H. Adjustments I. Troubleshooting and Hints	LEC. 6.0 LAB 8.0
Ref:	B721 T.M. Sec II	XII.	I. C. MEMORY A. General Description B. Addressing C. Write D. Read E. Parity Generation and Checking F. Adjustments G. Troubleshooting and Hints	LEC. 2.0 LAB 8.0

COURSE OUTLINE

SUBJECT MATTER:
-Continued-

Ref:	T.M. Sec. II	XIII.	LOADER INTERFACE CONTROL (705/711/721) A. Paper Tape Format B. Functional Description C. Timing D. Troubleshooting and Hints	LEC. 2.0 LAB 8.0
Ref:	T.M. Sec. II	XIV.	LOADER INTERFACE CONTROL (771) A. 80 Col. Card Format B. Functional Description C. Timing D. Troubleshooting and Hints	LEC. 2.0 LAB 2.0
Ref:	T.M. Sec. II and Handbook	XV.	B7MPL A. Types of MICROS B. Nano Breakdown C. Timing	LEC. 4.0 LAB 8.0
Ref:	T.M. Sec. II and B700 Handbook	XVI.	I/O COMMUNICATIONS A. Functional Description B. Functional Detail 1. CPU 2. PSU 3. I/O Control	LEC. 2.5 LAB 2.0
Ref:	T.M. Sec II, B700 Handbook and Trng. Supp.	XVII.	MICRO PROGRAMMING A. Mighty Mouse B. Your Program	LEC. 3.0 LAB 5.0
Ref:	All	XVIII.	UNIT TROUBLESHOOTING A. Installation	LEC. 2.0 LAB 7.0

COURSE OUTLINE

Prepared by: Small Systems Planning Group *
(Originator)

Submitted by: W. L. Sobel
(Project Supervisor)

Approved by: Houston P. Smith
Manager, Field Engineering Training Development

Approved by: S. L. Turney III Date 2-3-75
Manager, Field Engineering Training

* Bill Sobel
John Mitchell
Steve Wheatley
Dave Rutkowski

SYSTEM INITIALIZATION

Ref: All	1. POWER ON THE B700 AND MAKE ALL UNITS READY.
Ref: S.O.G. Sec. 3	2. INITIALIZE A BLANK DISK CARTRIDGE.
Ref: S.O.G. Sec. 1, 2	3. GIVEN AN INITIALIZED DISK CARTRIDGE, PERFORM A SYSTEM COLD START.
Ref: S.O.G. Sec. 1	4. GIVEN A DISK CARTRIDGE CONTAINING SYSTEM SOFTWARE, CHANGE THE SYSTEM CONFIGURATION BY PERFORMING A WARM START.
Ref: S.O.G. Sec. 1	5. GIVEN A DISK CARTRIDGE CONTAINING SYSTEM SOFTWARE, PERFORM A RESTART.
Ref: S.O.G. Sec. 3	6. GIVEN A DISK CARTRIDGE CONTAINING SYSTEM SOFTWARE, CREATE A BACKUP CARTRIDGE.

SYSTEM OPERATION

Ref: S.O.G.	7. DURING SYSTEM OPERATION, RESPOND TO ERROR MESSAGES WITH THE PROPER RECOVERY PROCEDURE.
Ref: S.O.G. Sec. 5	8. DEMONSTRATE YOUR ABILITY TO EXECUTE ANY LOAD UTILITY.
Ref: S.O.G. Sec. 6	9. DEMONSTRATE YOUR ABILITY TO EXECUTE ANY DUMP UTILITY.
Ref: S.O.G. Sec. 7	10. DEMONSTRATE YOUR ABILITY TO EXECUTE ANY LIST UTILITY.
Ref: S.O.G. Sec. 8	11. DEMONSTRATE YOUR ABILITY TO EXECUTE ANY COPY UTILITY.
Ref: S.O.G. Sec. 9	12. DEMONSTRATE YOUR ABILITY TO PERFORM MEDIA CONVERSION.
Ref: S.O.G. Sec. 4	13. GIVEN AN UNSORTED DATA FILE, PERFORM A MANUALLY INITIATED SORT OF THAT FILE.
Ref: B700 Handbook	14. GIVEN A PROGRAM OBJECT DECK, DETERMINE THE FOLLOWING: A. PROGRAM NAME B. DISK SPACE REQUIRED C. PERIPHERALS REQUIRED D. TYPE OF COMPILER USED E. INTERPRETER TO BE USED
Ref: B700 Handbook	15. GIVEN AN APPLICATIONS PROGRAM, SUCCESSFULLY LOAD THAT PROGRAM TO DISK.
Ref:	16. EXECUTE THE PROGRAM THAT WAS LOADED FROM THE PREVIOUS OBJECTIVE. (NOTE: THIS WILL BE REFERRED TO AS PROGRAM # 1 FOR THE FOLLOWING FOUR OBJECTIVES.)

SYSTEM OPERATION

Ref: S.O.G. Sec. 3

17. WHILE EXECUTING PROGRAM # 1 CAUSE PROGRAM # 2 TO EXECUTE WITHOUT DESTROYING PROGRAM # 1. (NOTE: PROGRAM # 2 TO BE SPECIFIED BY LAB INSTRUCTOR).

Ref: S.O.G. Sec. 3

18. PERFORM A PARTIAL TRACE OF PROGRAM # 2 USING WAIT MODE.

Ref: S.O.G. Sec. 3

19. CAUSE PROGRAM # 2 TO DISCONTINUE EXECUTION.

Ref: S.O.G. Sec. 3

20. RESUME THE EXECUTION OF PROGRAM # 1.

REF: S.O.G. Sec. 3

21. FROM THE TRACE PREVIOUSLY OBTAINED, DETERMINE THE FOLLOWING FOR ANY GIVEN INSTRUCTION:
    - A. S-LEVEL SEG. NUMBER
    - B. WORD/CHAR. LOCATION OF NEXT INSTRUCTION.
    - C. THE INSTRUCTION.
    - D. CONTENTS OF THE ACCUMULATOR
    - E. CONTENTS OF THE INDEX REGISTERS
    - F. VALUE OF THE FLAG WORD
    - G. DESTINATION

Ref: S.O.G. Sec. 3

22. PERFORM A SYSTEM DUMP OF VIRTUAL MACHINE MEMORY.

SYSTEM OPERATION

Ref: S.O.G. Sec. 3

23. FROM THE SYSTEM DUMP PREVIOUSLY OBTAINED, FILL IN THE VALUES OF THE REGISTERS IN THE WORKSHEET BELOW.

REGISTER	VALUE
ACCUMULATOR	
REMAINDER	
INDEX REGISTERS	
LSR	
DBR	
LPKR	
LPNR	
LLCR,LRCR,LLLR,LRLR	
SEG	
FLAGS	
RETURN TO STACK 1, 2	
RETURN FROM STACK	
PBAS	
SBAS	
SRJC	
SRJS	

DOCUMENTATION

Ref: T.M. Sec. III, V, and VI.
F.T. &R Documentation

24. USING THE F.T.&R DOCUMENTATION, LOCATE ANY GIVEN CARD, COMPONENT, AND CABLE IN THE SYSTEM. 15 minutes Min

Ref: T.M. Sec. III, & V
F.T.& R. Documentation

25. USING THE F.T.&R DOCUMENTATION LOCATE EACH OF THE FOLLOWING:
    A. AC1 & AC2
    B. CG & CD
    C. LIC
    D. NM
    E. SM
    F. MCU
    G. CU
    H. LU
    I. I/OC

Ref: T.M. Sec. III
F.T.&R Documentation

26. GIVEN ANY LOGIC TERM, LOCATE A PIN WHERE THE SIGNAL MAY BE OBSERVED.

MU 05/07

Ref: T.M. Sec. III
F.T.&R Documentation

27. GIVEN ANY LOGIC TERM, LIST ITS ORIGIN AND DESTINATION.

Ref: MTR Listing

28. GIVEN ANY MTR REQUIRING A PROGRAM, DETERMINE FROM THE OPERATORS INSTRUCTIONS EACH OF THE FOLLOWING:
    A. INSTRUCTION ADDRESS
    B. INSTRUCTION HEX CODE
    C. B7MPL STATEMENT FOR INSTRUCTION

Ref: T.M. Sec. III

29. IDENTIFY BY NAME ANY CIRCUIT SYMBOL IN THE SCHEMATICS, AND DETERMINE ITS OUTPUT WITH GIVEN INPUTS.

DOCUMENTATION

Ref: Introduction to Field Engineering	30. DEMONSTRATE YOUR ABILITY TO PROPERLY FILL OUT A FORM 14
Ref: RINS/LINS	31. DETERMINE THE RIN/LIN STATUS OF ANY B700 SYSTEM AND INSTALL ANY OUTSTANDING RINS OR LINS.

POWER (OBJECTIVES TO BE DONE ON 711 & 721)

Ref: T.M. Sec. VI F.T.&R	32. LOCATE ALL POWER SUPPLY FUSES AND CIRCUIT BREAKERS IN THE SYSTEM.
Ref: T.M. Sec. F.T.&R	33. LOCATE THE POWER SUPPLY CONNECTION WHICH SUPPLY VOLTAGES TO THE BACK-PLANE.
Ref: T.M. Sec. IV F.T.&R	34. PERFORM THE POWER SUPPLY ADJUST-MENTS.
Ref: T.M. Sec. II F.T.&R.	35. ISOLATE AND REPAIR TO THE FAILING COMPONENT ANY POWER SUPPLY MAL-FUNCTION.

F.E. CARDS

Ref: T.M. Sec. V
MTR Listing

36. EXECUTE THE FE MTR.

Ref: T.M. Sec. V

37. EXECUTE THE MEMORY TEST BY PROCEEDING FROM SEQUENCE COUNT TO SEQUENCE COUNT.

Ref: T.M. Sec. V

38. USING FEMTR DISPLAY THE FOLLOWING THE FE CARD INDICATORS.
    A. INCR
    B. MPM
    C. FEAC
    D. MIR

Ref: T.M. Sec. V

39. AT ANY SPECIFIED SEQUENCE AND ADDRESS COUNT IN THE FEMTR, DETERMINE THE EXPECTED VALUE OF MPM.

Ref: T.M. Sec V

40. PERFORM ANY SPECIFIED FUNCTION ON THE FE CARDS.

CORE MEMORY
B705/711/771

Ref: T.M. Sec. VI F.T.&R	41. LOCATE AND DESCRIBE THE FUNCTION OF EACH OF THE FOLLOWING: A. CONTROL BOARD B. ADDRESS BOARD C. DIGIT BOARD D. CORE STACK
Ref: T.M. Sec. VIII F.T.&R	42. CONFIGURE THE CPU BACKPLANE FOR ANY GIVEN MEMORY ADDRESS LIMIT.
REF: T.M. Sec. IV, VI, & VIII F.T.&R	43. INSTALL AN ADDITIONAL MEMORY MODULE.
Ref: T.M. Sec. IV F.T.&R	44. PERFORM ALL CORE MEMORY ADJUSTMENTS.
Ref: T.M. Sec. II F.T.&R	45. USING THE FEMTR AND A SIGNAL WORK-SHEET. OBSERVE AND RECORD THE REQUIRED INFORMATION .
Ref: T.M. Sec. II B700 Handbook F.R.&R	46. FOR ANY GIVEN CORE MEMORY ADDRESS LOCATE EACH OF THE FOLLOWING: A. MODULE B. X DRIVER SWITCH C. X COMMON SWITCH D. Y DRIVER SWITCH E. Y COMMON SWITCH
Ref: T.M. Sec. II F.T.&R	47. FOR ANY GIVEN MEMORY DATA BIT, LOCATE EACH OF THE FOLLOWING: A. INHIBIT DRIVER B. SENSE AMPLIFIER
Ref: All	48. GIVEN ANY CORE MEMORY MALFUNCTION, ISOLATE AND REPAIR THE FAULTY CIRCUIT.

B721

Ref: T.M. Sec. II F.T.&R	49. FOR ANY GIVEN MEMORY ADDRESS LOCATE THE MEMORY CHIPS SELECTED.
Ref: T.M. Sec. II F.T.&R	50. FOR ANY GIVEN MEMORY DATA BIT, LOCATE THE CHIPS IN WHICH IT IS STORED.
Ref: T.M. Sec. VI FT&R	51. INSTALL AN ADDITIONAL MEMORY MODULE.
Ref: T.M. Sec. VIII F.T.&R	52. CONFIGURE THE CPU BACKPLANE FOR ANY GIVEN MEMORY ADDRESS LIMIT.
Ref: All	53. GIVEN ANY MEMORY MALFUNCTION, ISOLATE AND REPAIR THE FAULTY CIRCUIT.

LIC

Ref: MTR Listings

54. LOAD AND EXECUTE THE MEMLDR MTR.

55. ISOLATE ANY PROBLEM IN THE L.I.C. TO FAILING THE COMPONENT AND REPAIR THE PROBLEM.

B7MPL

Ref: MTR Listings	56. USING THE MTR LISTINGS DETERMINE THE SPECIFIC FUNCTION OF ANY GIVEN MICRO INSTRUCTION.
Ref: MTR Listings	57. GIVEN A STRING OF MICRO INSTRUCTIONS DETERMINE WHEN THE EXECUTION OF EACH MICRO WILL OCCUR.
Ref: System Doc. Sec. II B700 Tech. Man.	58. GIVEN ANY BIT OF ANY WORD IN NPM LOCATE THE CHIP IN WHICH THE BIT IS STORED AND LOCATION WHERE IT CAN BE MONITORED.
	59. DETERMINE IF ANY GIVEN MICRO WAS EXECUTED PROPERLY.
Ref: FEMTR	60. USING MTR PROCEDURES ISOLATE AND REPAIR FAILURES IN NANO MEM.
Ref: MTR Listings	61. LOAD AND EXECUTE THE PROCESSOR MTR TEST.
Ref: MTR Listings	62. LOAD AND EXECUTE THE BARREL SWITCH MTR.
Ref: MTR Listings	63. LOAD AND EXECUTE THE MEMORY CONTROL UNIT MTR TEST.

B7MPL

Ref: MTR Listings	64. LOAD AND EXECUTE DATA PROGRAM MEMORY MTR TEST.
Ref: MTR Listings	65. SINGLE CLOCK THROUGH ANY GIVEN MTR PROGRAM AND FROM ANY POINT INDICATE THE NEXT INSTRUCTION TO BE EXECUTED.
Ref: MTR Listings	66. GIVEN PROBLEMS IN THE CPU LOCATE AND REPAIR FAILURE.
Ref:	67. DEMONSTRATE HOW TO LOAD DATA/ PROGRAM MATERIAL WITH THE MEM/MOD-IFY ROUTINE.
Ref: MTR Listings	68. USING THE CONSOLE MTR TEST ISOLATE FAILURES IN THE PSU TO THE FAILING COMPONENT AND REPAIR THE MALFUNCTION.
	69. USING COLD START 80 ISOLATE AND REPAIR FAILING COMPONENTS IN THE PSU.

MICRO PROGRAMMING

Ref: Sec. II, Tech. Man.
B700 Handbook

70. WRITE AND EXECUTE A MICRO PROGRAM TO DISPLAY THE VALUE OF "B721" IN MIR.

Ref: Sec. II, Tech. Man.
B700 Handbook

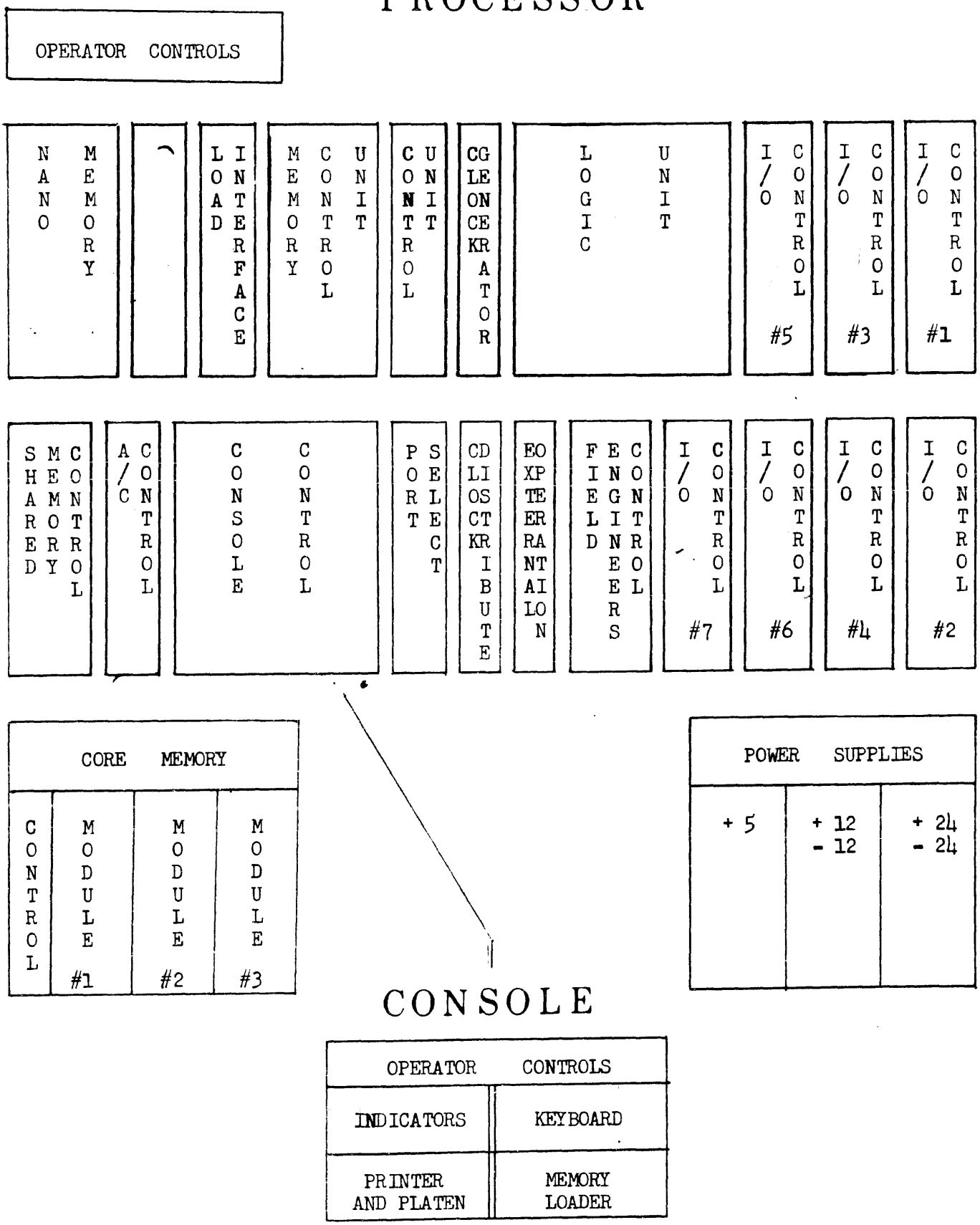
71. WRITE AND EXECUTE A MICRO PROGRAM TO EXERCISE A CONSOLE FUNCTION.

INSTALLATION

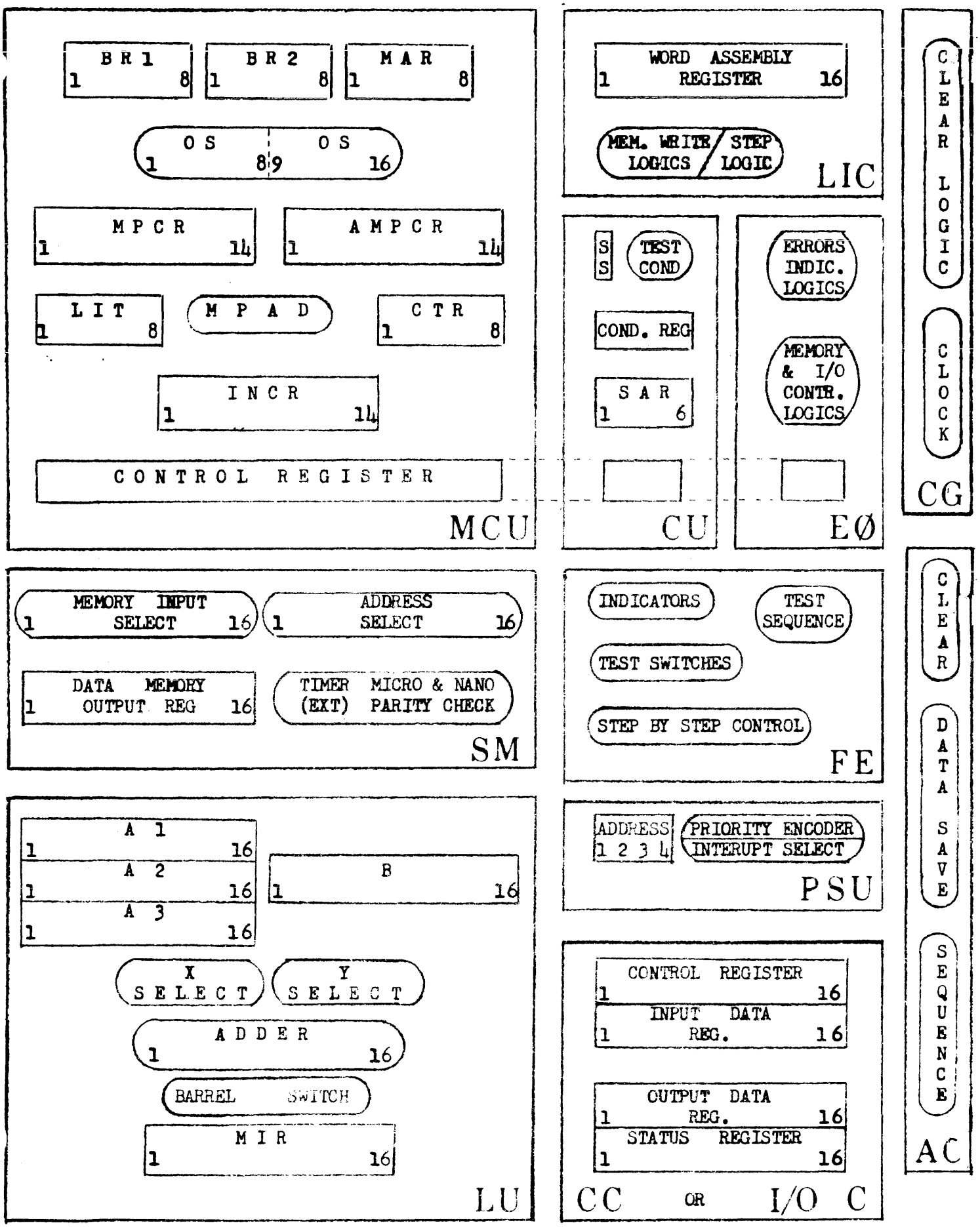
Ref: T.M. Sec. VI

72. DEMONSTRATE YOUR ABILITY TO INSTALL AND CHECK OUT A B700 SYSTEM.

PROCESSOR



PROCESSOR LOGIC CARD BLOCK PICTURE



PROCESSOR LOGIC REGISTER BLOCK DIAGRAM

CSTRT80
B700 UNIVERSAL 80 COLUMN HEX CARD LOADER

INSTRUCTIONS:

1. LOAD MIGHTY-MOUSE TAPE THRU HARDWARE LOADER.
2. PLACE PACKED HEX OBJECT DECK IN CARD READER (DPCS) .
3. CARD DECK MUST HAVE END CARD (NON-BLANK IN COLUMN 13).
4. CONSOLE KEYBOARD ENABLED TO DEPRESS NUMERIC KEY WHOSE VALUE = THE I/O CONTROL OF THE 80 COLUMN READER.

NOTES:

1. DATA FIELD ON CARD = COLUMNS 17 THRU 80.
2. CORE MEMORY ADDRESS TO STORE INFORMATION IN COLUMNS 15 AND 16.
3. CARD PARITY IN COLUMN 9.
4. IF PARITY ERROR DETECTED CSTRT80 STOPS IN A WAIT CONDITION WITH ALL "D" INDICATORS ON THE CONSOLE LIT.
5. AFTER ALL CARDS LOADED PROGRAM CONTROL TRANSFERS TO ADDRESS 0000.

EXPLANATORY NOTE:

" AS SOON AS THE NOSE GETS THE NEWS, THE TUMMY MOVES THE TAIL, AND THE FLEAS GO ALONG FOR THE RIDE."

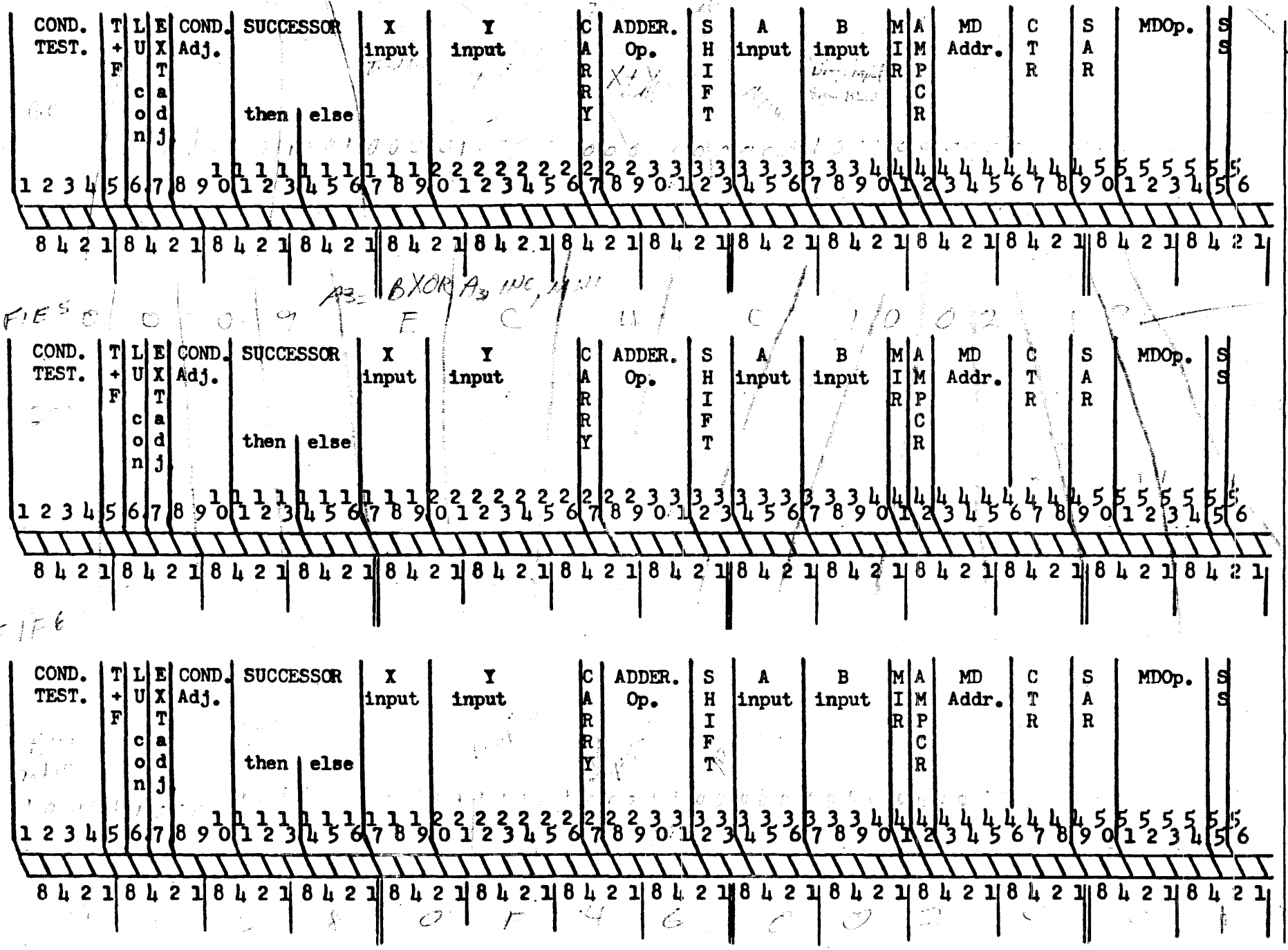
MICRO ADDR.	MICRO CODE		TRANSLANG STATEMENT
		NOSE.	
0000	F08F		BR2 = LITL.
0001	C807		SAR = 8, LIT = 7
0002	F060		B = AMPCR
0003	0881		AMPCR = NUM. CON. IND.
0004	F0E2		MIR = BC.
0005	F098		DW2
0006	8045		CPCR = IKE-the FLEA-1
0007	F126		A2 = LIT and B
0008	F02B		A2 = A2 - 1
0009	F026		A2 = A2 L
000A	803D		CPCR = MIKE-the-FLEA-1
000B	F041		A3 = AMPCR
000C	001A		AMPCR = TAIL
000D	F007		A1 = AMPCR
000E	1FBF		AMPCR = @1FBF@
000F	F0CA		LCTR
0010	E039		LIT = 57
		TUMMY.	
0011	F0D2		MAR1 = A3
0012	F1E3		MR1, MIR = B
0013	F1F1		WHEN RDC BEX, MAR1 = A1
0014	F0F3		MW1
0015	F04C		A3 = A3 + 1
0016	F012		A1 = A1 + 1
0017	F1B8		INC IF NOT COV SKIP
0018	5FBF		MPCR = @1FBF@
0019	4010		MPCR = TUMMY - 1

```
                TAIL.
001A    F090            BR2 = A2
001B    F0CA            LCTR
001C    C806            SAR = 8, LIT = 6
001D    9FEB            CPCR = @1FEB@
001E    F0C8            INC IF COV SKIP
001F    5FC2            MPCR = @1FC2@
0020    F054            A3 = B000
0021    9FEB            CPCR = @1FEB@
0022    9FEB            CPCR = @1FEB@
0023    9FEB            CPCR = @1FEB@
0024    9FEB            CPCR = @1FEB@
0025    9FEB            CPCR = @1FEB@
0026    F0FF            0 EQV B
0027    F09D            IF ABT SKIP
0028    5FE7            MPCR = @1FE7@
0029    9FEB            CPCR = @1FEB@
002A    9FEB            CPCR = @1FEB@
002B    F0E2            MIR = B C.
002C    9FEB            CPCR = @1FEB@
002D    F08B            BBI B
002E    F0D5            MAR1 = B

002F    F0CA            LCTR
0030    C81E            SAR = 8, LIT = 30
0031    9FEB            CPCR = @1FEB@
0032    F0E2            MIR = B C
0033    9FEB            CPCR = @1FEB@
0034    F08B            BBI B
0035    F0E1            MIR = B
0036    F0F3            MW1
0037    F0D7            MAR1 = BMAR + 1
0038    F0C8            INC IF COV SKIP
0039    5FD6            MPCR = @1FD6@
003A    F03D            A3 EQV B000
003B    F09D            IF ABT SKIP
003C    5FEF            MPCR = @1FEF@ PAR. ERR.
003D    1FBF            AMPCR = TAIL - 1
            MIKE-the-FLEA
003E    F08E            BR2 = A2 or B100
003F    F1D5            MIR = B001 + 1
0040    F098            DW2
0041    F0C9            JUMP.
0042    F08E            BR2 = A2 or B100
0043    F0E7            MIR = B001
0044    F098            DW2
0045    7FFF            MPCR = 0000 - 1
            IKE-the-FLEA
0046    F0FC            WHEN SRQ STEP
0047    F097            DR2 BEX
0048    F049            A3 = A3 XOR B
0049    F0C9            JUMP.
```

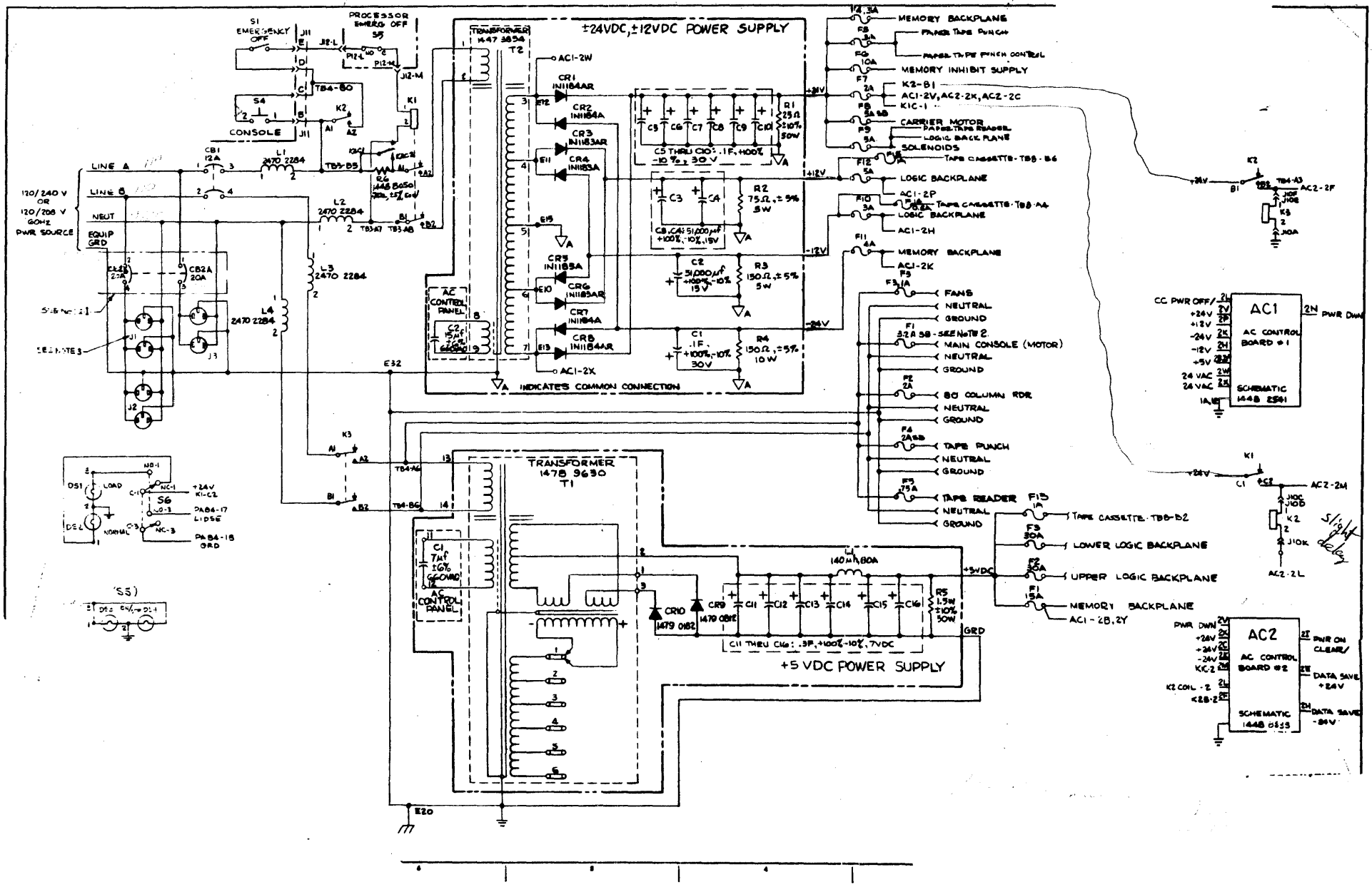
PARITY ERROR

```
004A    F08F        BR2 = LIT L
004B    C807        SAR = 8, LIT = 7
004C    F0EE        MIR = LIT L
004D    E082        LIT = 130
004E    F089        B = LIT
004F    E0FF        LIT = 255
0050    F08B        BBI = B
0051    F0E1        MIR = B
0052    F098        DW2
0053    F000        WAIT
0054    4000
```

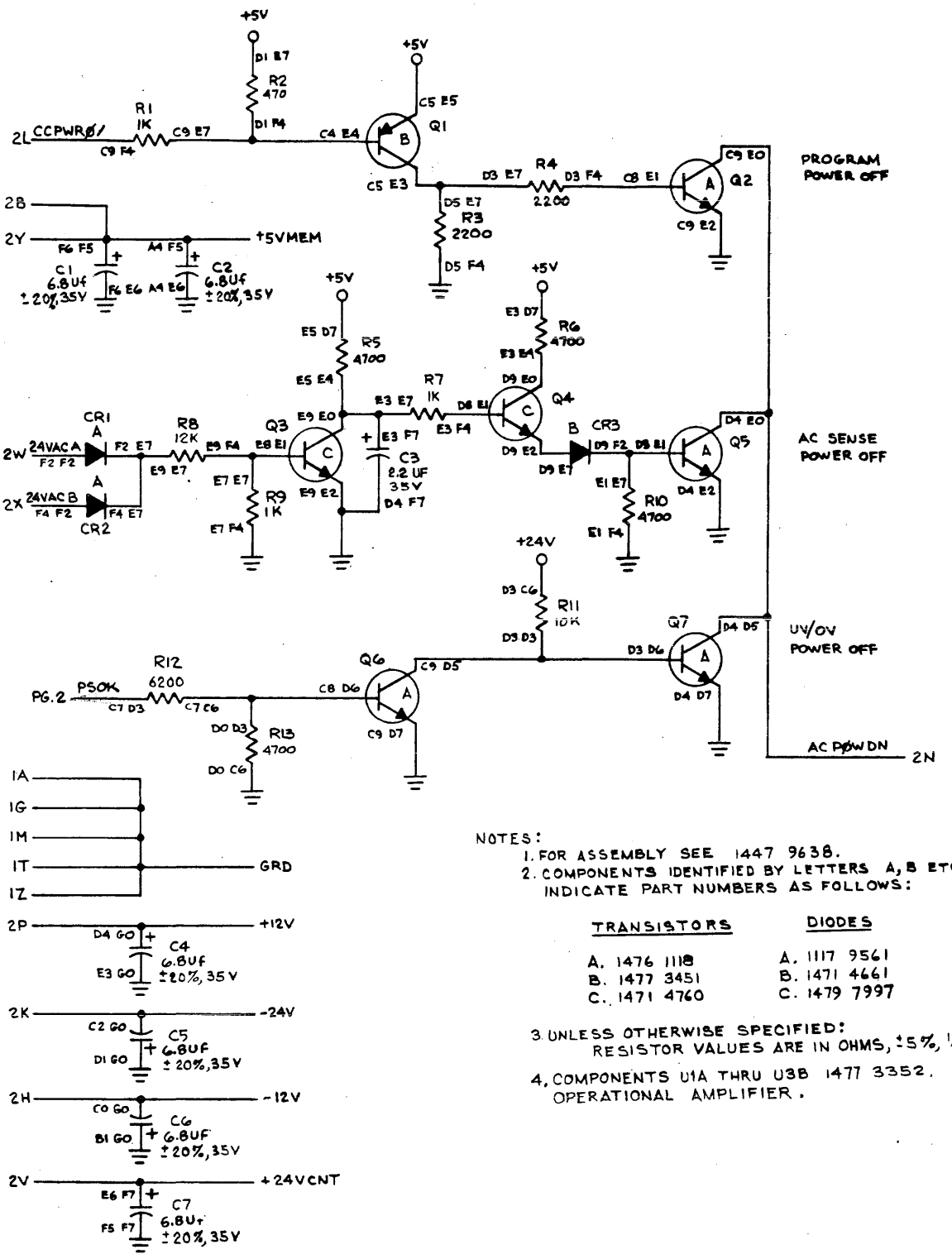


NANO MEMORY WORD WORKSHEET

B700 SYSTEMS



SCHEMATIC A/C CONTROLS



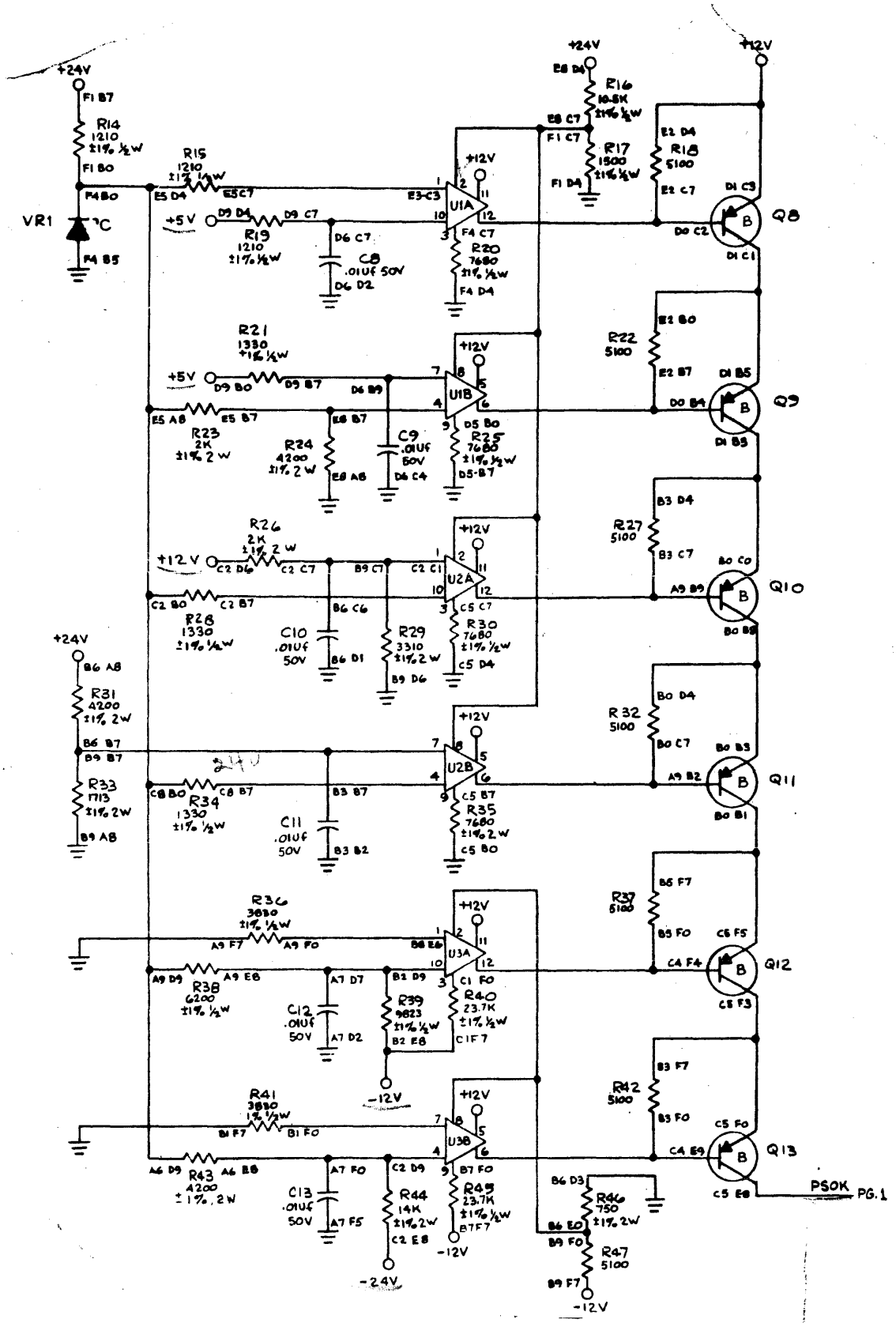
NOTES:

1. FOR ASSEMBLY SEE 1447 9638.
2. COMPONENTS IDENTIFIED BY LETTERS A, B ETC INDICATE PART NUMBERS AS FOLLOWS:

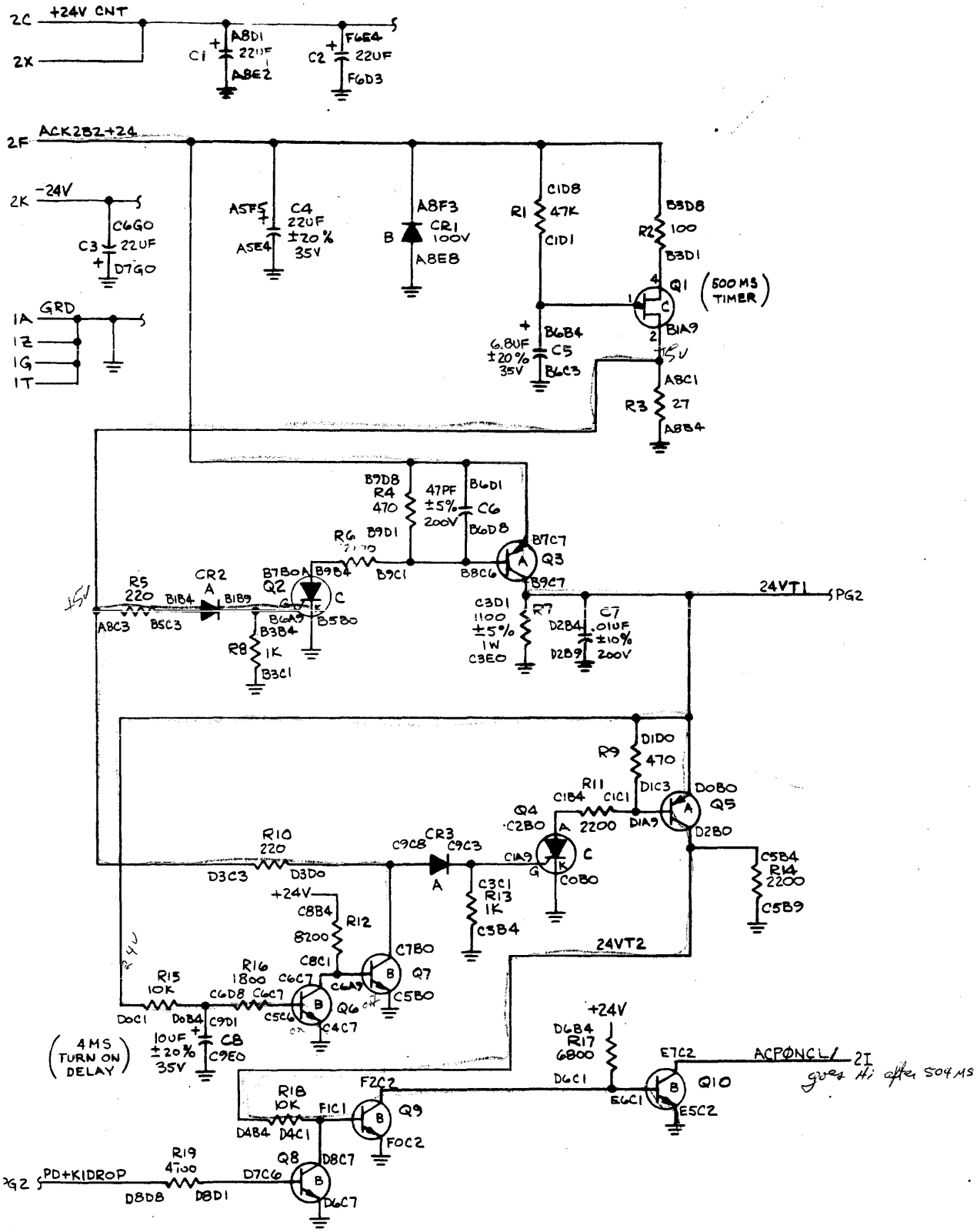
TRANSISTORS	DIODES
A. 1476 1118	A. 1117 9561
B. 1477 3451	B. 1471 4661
C. 1471 4760	C. 1479 7997

3. UNLESS OTHERWISE SPECIFIED: RESISTOR VALUES ARE IN OHMS, ±5%, 1/2 W.
4. COMPONENTS U1A THRU U3B 1477 3352. OPERATIONAL AMPLIFIER.

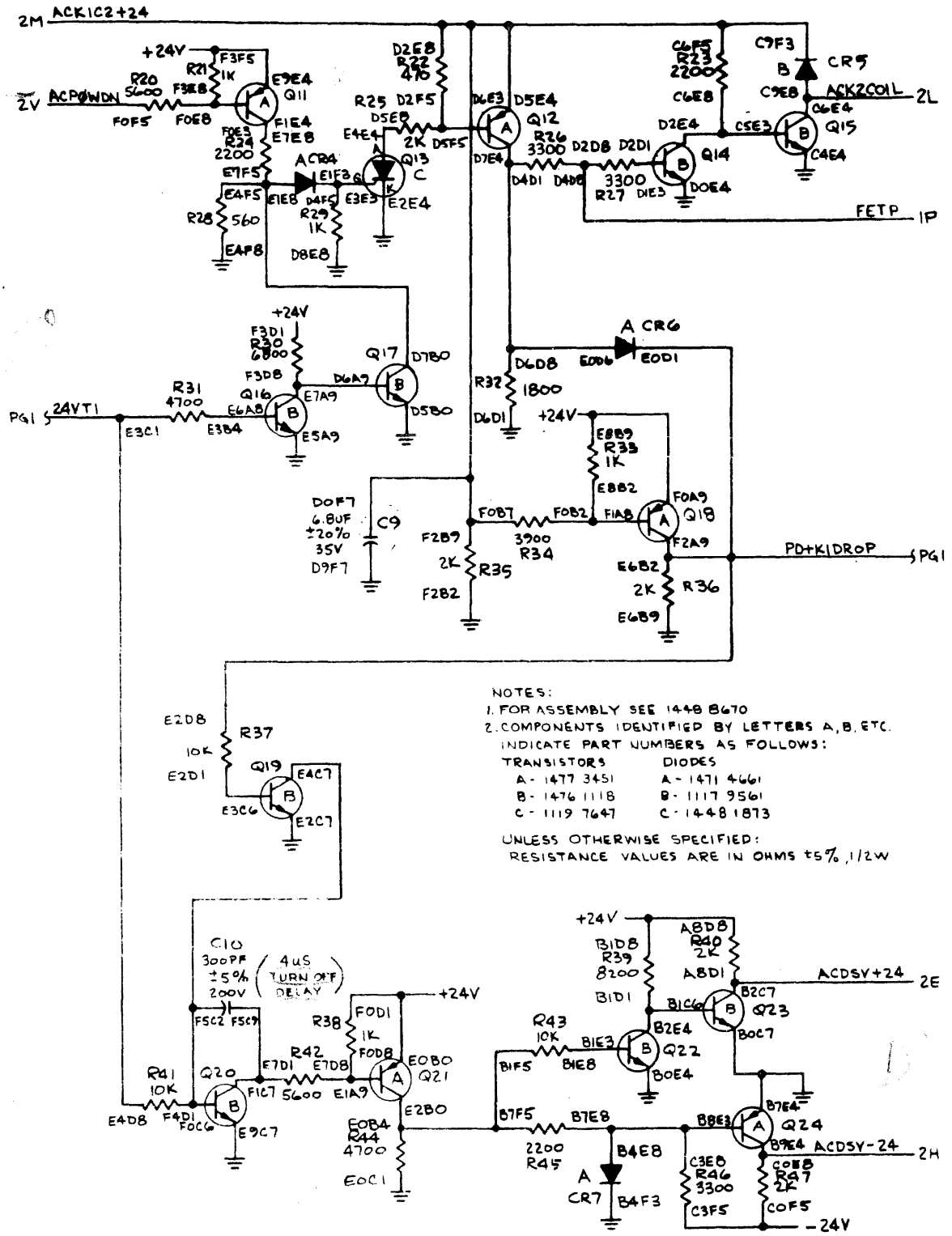
AC1-1

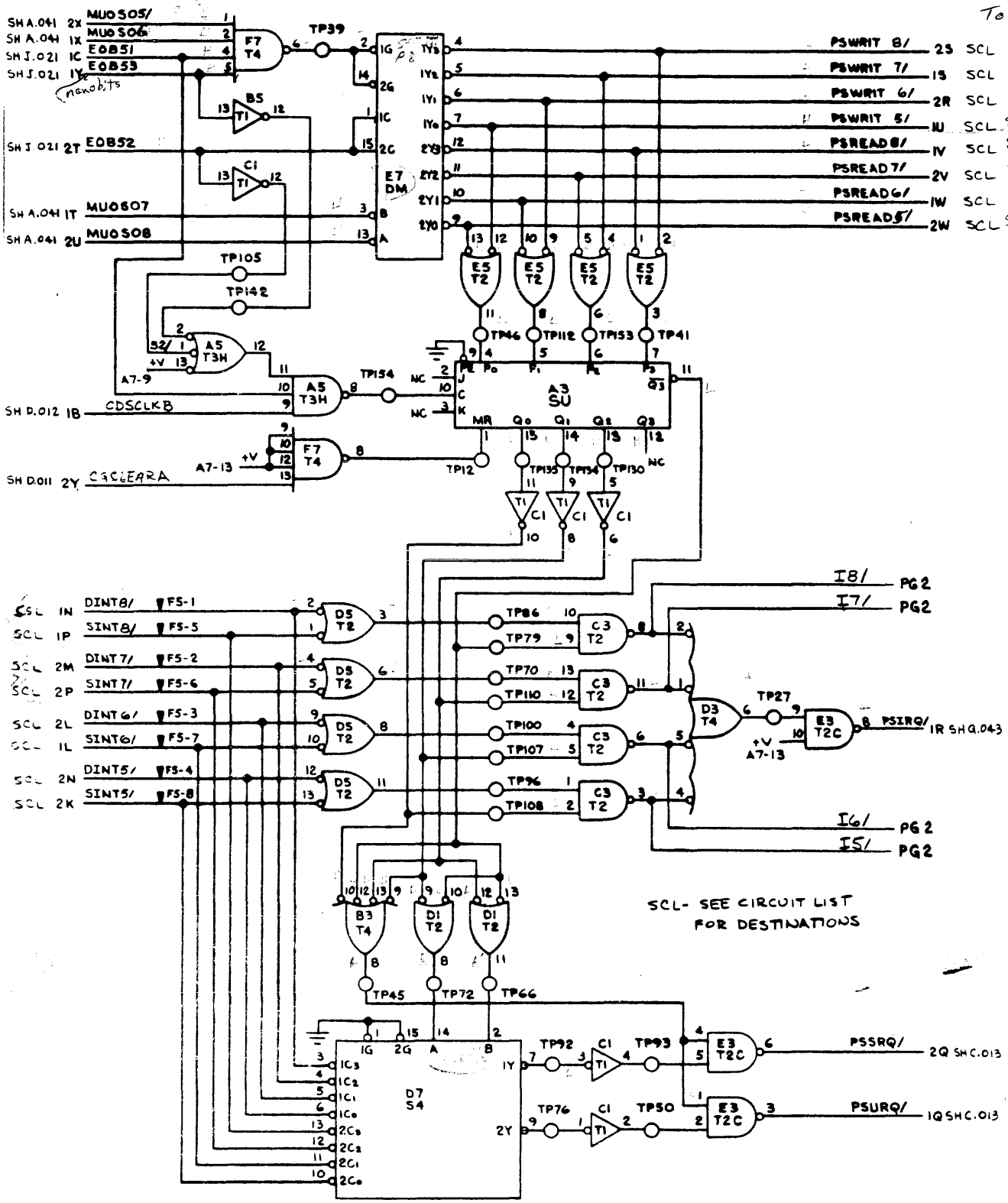

+24V
+12V
+5V
-12V
-24V
VR1
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
C8
C9
C10
C11
C12
C13
U1A
U1B
U2A
U2B
U3A
U3B
Q8
Q9
Q10
Q11
Q12
Q13
PSOK
PG.1

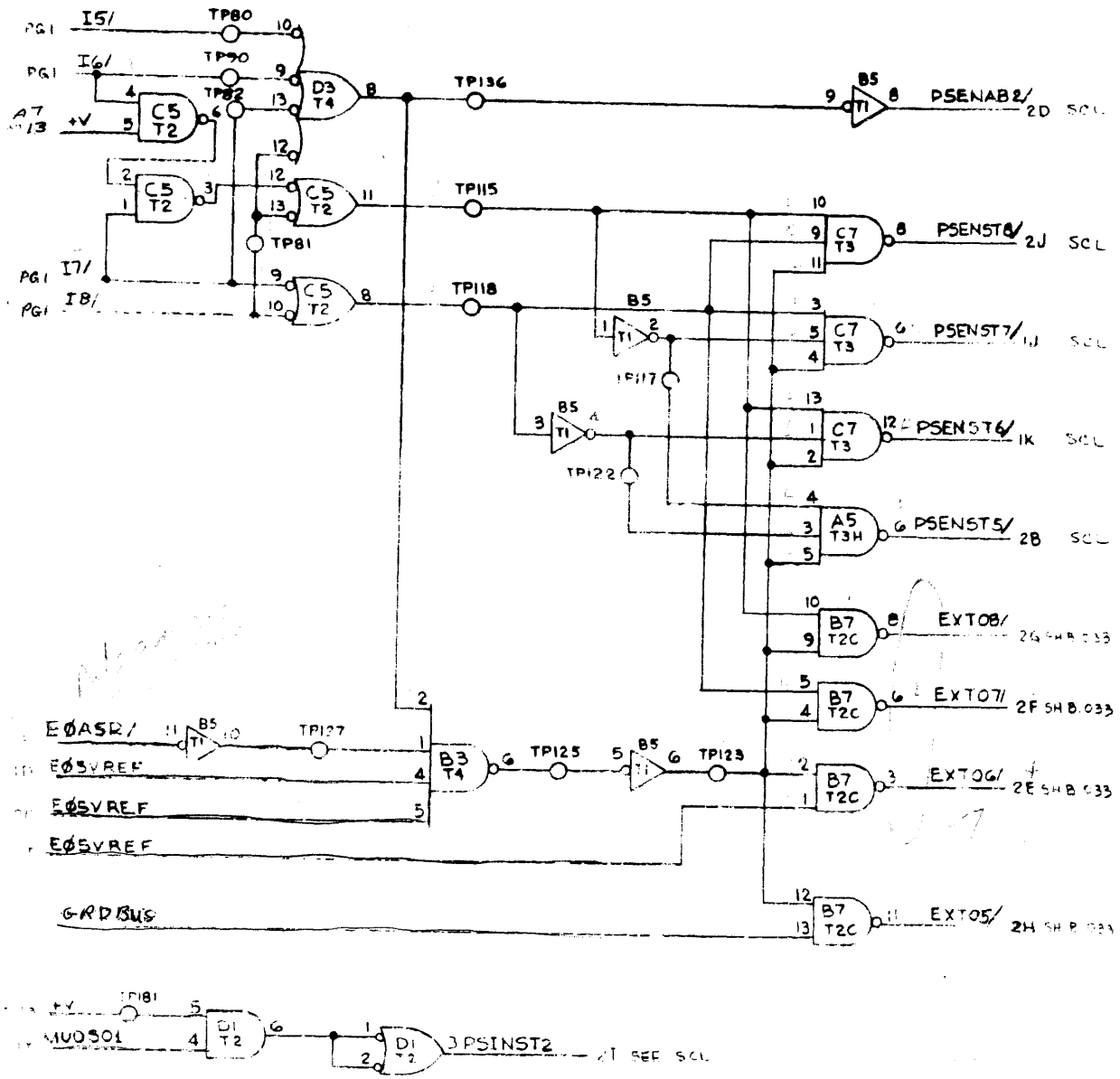
AC1-2


2C +24V CNT
2X
C1 A8D1 22UF A8E2
C2 F6E4 22UF F6D3
2F ACK2B2+24
2K -24V
C6G0
C3 22UF
D7G0
1A GRD
1Z
1G
1T
A5F5 C4 22UF ±20% 35V A5E4
A8F3 CR1 100V A8E8
R1 47K C1D8 C1D1
R2 100 B3D8 B3D1
Q1 (500 MS TIMER)
B6B4 6.8UF ±20% 35V C5 B6C3
B1A9
A8C1
R3 27 A8B4
B7D8 R4 470
47PF ±5% 200V C6 B6D1 B6D8
R6 B9D1
B7C7 Q3
B9C7
R5 220 B1B4 B1B9
CR2 A
Q2 C
B7B0A B9B4 B9C1 B8C6
B6A9 B5B0
B3B4 R8 1K B3C1
C3D1 1100 ±5% 1W C3E0
R7 D2B4
C7 .01UF ±10% 200V D2B9
24VT1 PG2
A8C3 B5C3
R9 470 D1D0 D1C3
R11 C1B4 C1C1 2200 D1A9
Q5 D0B0 D2B0
Q4 C2B0 A C
C0B0 G K
C5B4 R14 2200 C5B9
R10 220 D3C3 D3D0
C9C8 CR3 C9C3 A
C3C1 R13 1K C3B4
+24V C8B4 R12 8200 C8C1
C7B0 Q7 C5B0
24VT2
R15 10K D0C1 D0B4
R16 1800 C6C7 C6D8 C6C7 C6A9
Q6 C5C6 C4C7
C9D1 C8 10UF ±20% 35V C9E0
(4MS TURN ON DELAY)
+24V D6B4 R17 6800 D6C1
E7C2 ACPONCL/ 2I goes Hi after 504MS
Q10 E6C1 E5C2
F2C2 R18 10K F1C1
Q9 D4B4 D4C1 F0C2
Q8 D8C7 D7C6 D6C7
R19 4700 D8D8 D8D1
PG2 PD+KIDROP

AC2-1


2M ACK1C2+24
+24V
R21 1K
R20 5600
ACPOWDN
2V
Q11
R25 D2F5
2K
R22 470
Q12
R26 3300
Q13
ACR4
R24 2200
R28 560
R29 1K
D8E8
C6F5 R23 2200
C9F3
CR5
ACK2COIL
2L
Q15
Q14
3300 R27
FETP
1P
+24V
F3D1 R30 6800
Q17
Q16
R31 4700
24VT1
PG1
A CR6
R32 1800
+24V
R33 1K
C9
6.8UF ±20% 35V
D9F7
R34 3900
R35 2K
R36 2K
PD+KIDROP
PG1
R37 10K
Q19
NOTES:
1. FOR ASSEMBLY SEE 1448 B670
2. COMPONENTS IDENTIFIED BY LETTERS A, B, ETC. INDICATE PART NUMBERS AS FOLLOWS:
TRANSISTORS
A - 1477 3451
B - 1476 1118
C - 1119 7647
DIODES
A - 1471 4661
B - 1117 9561
C - 1448 1873
UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS ±5%, 1/2W
C10 300PF ±5% 200V
4uS TURN OFF DELAY
R38 1K
R42
Q20
R41 10K
Q21
R44 4700
+24V
R39 8200
R40 2K
ACDSV+24
2E
Q23
R43 10K
Q22
Q24
ACDSV-24
2H
2200 R45
CR7
R46 3300
R47 2K
-24V


SH A.041 2X MUOSO5/
SH A.041 1X MUOSO6
SH J.021 1C E0B51
SH J.021 1Y E0B53
nanobits
SH J 021 2T E0B52
SH A.041 1T MUO607
SH A.041 2U MUOSO8
F7 T4
B5 T1
C1 T1
TP39
TP105
TP142
A5 T3H
TP154
CDSCLKB
SH D.012 1B
A7-9
+V
A7-13
F7 T4
SH D.011 2Y CGCLEARA
TP12
E7 DM
PSWRIT 8/ 2S SCL 8
PSWRIT 7/ 1S SCL 7
PSWRIT 6/ 2R SCL 6
PSWRIT 5/ 1U SCL 5
PSREAD8/ 1V SCL 8
PSREAD7/ 2V SCL 7
PSREAD6/ 1W SCL 6
PSREAD5/ 2W SCL 5
E5 T2
TP46
TP112
TP153
TP41
A3 SU
TP135
TP134
TP130
NC
SCL IN DINT8/ FS-1
SCL IP SINT8/ FS-5
SCL 2M DINT7/ FS-2
SCL 2P SINT7/ FS-6
SCL 2L DINT6/ FS-3
SCL 1L SINT6/ FS-7
SCL 2N DINT5/ FS-4
SCL 2K SINT5/ FS-8
D5 T2
TP86
TP79
TP70
TP110
TP100
TP107
TP96
TP108
C3 T2
D3 T4
TP27
E3 T2C
PSIRQ/ IR SH Q.043
I8/ PG2
I7/ PG2
I6/ PG2
I5/ PG2
B3 T4
D1 T2
TP45
TP72
TP66
SCL- SEE CIRCUIT LIST FOR DESTINATIONS
D7 S4
TP92
TP93
PSSRQ/ 2Q SH C.013
TP76
TP50
PSURQ/ 1Q SH C.013


PG1 I5/
TP80
PG1 I6/
TP90
TP82
+V
C5 T2
D3 T4
TP136
B5 T1
PSENAB2/
2D SCL
TP115
TP81
PG1 I7/
PG1 I8/
TP118
C7 T3
PSENST8/
2J SCL
PSENST7/
PSENST6/
1K SCL
TP117
TP122
A5 T3H
PSENST5/
2B SCL
B7 T2C
EXT08/
EXT07/
2F SH B 033
EXT06/
2E SH B 033
EXT05/
2H SH B 033
EØASR/
EØSVREF
EØSVREF
EØSVREF
TP127
TP125
TP123
B3 T4
GRDBUS
+V
TP181
MUOSO1
D1 T2
PSINST2
SEE SCL

PS1-2

DC FUSES

FUSE #	VOLTAGE	SIZE	BURROUGHS PART #	DESCRIPTION
F1	+5	15A	1447 7103	Memory
F2	+5	30A	1447 7111	Upper Logic (F)
F3	+5	30A	1447 7111	Lower Logic (D)
F4	+24	3A	1321 8557	Memory
F5	+24	3A	1321 8557	Paper Tape Punch and Control
F5P	+24	7A	1674 1365	Memory Inhibit Power Supply
F6	+24	10A	1447 7145	Memory Inhibit Power Supply
F7	+24	2A	1321 8631	K2, K1, AC1, AC2
F8	+24	5ASB	1341 0873	Carrier Motor
F9	+24	5A	1447 7095	Paper Tape Rdr, Logic Backplane, Solenoids
F10	-12	3A	1321 8557	Backplane, ACI
F11	-24	4A	1323 8100	Memory Backplane, ACI
F12	+12	5A	1447 7095	Logic Backplane, ACI
F13	+5	1A	1343 0939	Tape Cassette
F14	-12	5A	1321 8540	Tape Cassette
F15	+12	1A	1343 0939	Tape Cassette

AC FUSES

F1	3.2 ASB	1343 1010	Decoder Motor
F2	2A	1321 8631	80 Column Card Reader
F3	1A	1343 0939	Fans
F4	2ASB	1009 5511	Tape Punch
F5	.75 A	1343 0921	Tape Reader

B700 PROCESSOR REVIEW 1

1. What is the normal condition of the ACPOWDN signal? (high or low)
2. Where is the DATA SAVE CIRCUIT and what function of memory does it affect?
3. Which Loader Interface signal depends on the start code to activate it and which timing signal is produced as a result?
4. What signal initiates any memory cycle?
5. Which register addresses MPM; DPM?
6. Determine the following for memory address: 0D8B and 35F9

    a. actual word address
    b. X driver switch
    c. X common switch
    d. Y driver switch
    e. Y common switch
    f. module

7. Which memory timing signals determine the direction of current flow in the X and Y address lines?
8. Which memory timing signal is unique to a CLEAR/WRITE memory cycle; READ/RESTORE?
9. List the three sources of data to memory.
10. Where is parity generated and checked for data going to memory and from memory?
11. Indicate the condition of the following to write a '1' bit to memory.

    a. data buffer (set or reset)
    b. inhibit driver (on or off)

12 Indicate the condition of the following to read a '0' bit from memory.

    a. sense amp (pulse of no pulse)
    b. data buffer (set or reset)

B700 PROCESSOR REVIEW 2

1. How many NANO instructions in the B711?
   How many are used?
2. What 4 conditions of the Arithmetic Logic Unit can be tested with NANO bits 1 thru 4?
   Define the 4 conditions tested?

   List 1 NANO instruction that tests for 1 of these conditions?
3. What NANO bits define the successor for a instruction?
   Define a successor and it's use?
4. How would the instruction BFTO affect the bits of the B register? (NANO bits 20 thru 26)
5. What 2 means of addressing core memory do we have?
   What type of information is addressed by each method?
6. What area of the processor logic determines port priority?
7. What kind of information is contained in each column of an 80 column packed hex card as read in by CSTRT80?
8. Micro instruction = FOC5. List the nano instruction addressed and state in general terms what the nano instruction will do when executed?.
9. Define: SRQ =
   URQ =
   IRQ =
10. How many ALU functions are used in the B711?
11. What is the 16 bit data word to turn on the console "D" indicators for a "MPM" error?
12. Write a simple program to put the address of port #5 in BR1 (or BR2) with the INSTR bit on.
13. How many type II instructions in the B711? 6
14. What is the difference between MW1 to MW2?
    and MR1 to MR2?
15. Briefly explain the function of each micro instruction listed.

    a. 8514
    b. 1A62
    c. 40D3

B700 I/O REVIEW 3

1. How many I/O channels maximum in the B711 processor?

2. If an IRQ occurs, how does the proc find out the address of the channel that generated it?

3. What determines that channels 5-8 have higher priority then channels 1-4?

4. What conditions produce a Sint in the console control?

5. What type of information is the proc sending or receiving from an I/O control under the following conditions?
   a. DW control bit on =
   b. DW control bit off =
   c. DR control bit on =
   d. DR control bit off =
   e. ASR =

6. 80 column card reader status word = 0004, what does it mean?

7. If an IRQ occurs, how does the proc know if it was the result of a DINT or SINT in the I/O control?

8. Briefly explain the functions of the Port Select Cards?

9. What conditions produce a DINT in the console control?

10. What MTR test checks out the P.S.U.?

11. Write a small program to address the console and enable the printer.

12. A console keyboard data word = 0078, what key was depressed?

MPM 1-18	LOC.
MPM 01 (10)	1RL
MPM 01 (10)	1TL
MPM 08 (17)	2TL
MPM 08 (17)	2VL

INHIBIT DRIVERS

	LOC.
IHB 01 10	2JU
IHB 02 11	1KU
IHB 03 12	2MU
IHB 04 13	1NU
IHB 05 14	2QU
IHB 06 15	1RU
IHB 07 16	2TU
IHB 08 17	1UU
IHB 09 18	NOT USED

SHARED MEM DATA

	LOC.
SMDTM 01 (10)	2KL
SMDTM 02 (11)	2LL
SMDTM 03 (12)	2ML
SMDTM 04 (13)	2NL
SMDTM 05 (14)	1JL
SMDTM 06 (15)	1KL
SMDTM 07 (16)	1LL
SMDTM 08 (17)	1ML

SENSE LINES

	LOC.		LOC.	
SO1	1JU	SO1	1IU	(10)
SO2	2LU	SO2	2KU	(11)
SO3	1MU	SO3	1LU	(12)
SO4	2PU	SO4	2NU	(13)
SO5	1QU	SO5	1PU	(14)
SO6	2SU	SO6	2RU	(15)
SO7	1TU	SO7	1SU	(16)
SO8	2VU	SO8	2VU	(17)
SO9		SO9	NOT USED	

ENABLE SIG	LOC.
EOMDOS	2XL
RESET-N	1YL
WRITESTR-N	2JL
READSTR-N	2CL
IHBT-N	1BL

+5VDC	+15VDC	-15VDC
1FL	2DU	2DL
2FL	1DU	
1XU	1EU	
2XU	1EL	
2ZU	2EU	
	2EL	

DIGIT BOARD WORK SHEET

Y COMMON DRIVERS 0-15 LOC.	SIG
1QL	Yc 0
2RL	Yc 1
1RL	Yc 2
2SL	Yc 3
AWL	Yc 13
1WL	Yc 14
2XL	Yc 15

ADDRESS LINES Y COMMON DRIVERS LOC.	BIT
1DL	09
2FL	10
1FL	11

Y COMMON DRIVERS READ & WRITE LOC.				
2YU	READ	T	8K	Yc 9-15
1YU	WRITE	T	8K	
2XU	READ	T	4K	Yc 0-8
1XU	WRITE	T	4K	

X & Y DRIVER WORK SHEET

Y POS & NEG DRIVERS 0-7 LOC.		
2HL	YPD	0
1HL	YND	0
1NL	YPD	7
2PL	YND	7

ADDRESS LINES YP & ND LOC.	BIT
1GL	06
2BL	07
2DL	08

Y POS & NEG DRIVERS LOC.		
2GL	Yd	WRITE
1ZU	Yd	READ

	Xc 0-8 DRIVERS	
LOC.		
1FU	Xc	0
2FU	Xc	1
1BU	Xc	6
2BU	Xc	7

X & Y DRIVER WORK SHEET

ADDRESS LINES
XP&ND

LOC.	BIT
1RU	00
2RU	01
2SU	02

X COMMON DRIVERS

LOC.		
1VU	Xc	WRITE
2VU	Xc	READ

X POS & NEG DRIVERS

LOC.		
2TU	XP&ND	READ
1TU	XP&ND	WRITE

	LOC.
+ 5VDC	1AL
	1GU
+15VDC	2GU
	1VL
	2UL

	LOC.
	1EL
-15V	2EL
	1VU
	2UU

X & Y DRIVER WORK SHEET