B 0115 80 COL. CARD READER CONTROL

(FOR B700 SYSTEMS)

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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INTRODUCTION

The B0115 80-Column Card Reader Device Dependent Port (DDP), hereinafter called the Card Reader I/O Control (IOC), provides the interface between the B9115 and B9116 card readers and the system processor. The Card Reader IOC provides the necessary control functions and buffering for the transfer of information read from 80-column punch cards.

The Card Reader IOC acts upon receipt of control words from the processor, performs the operation specified and, upon completion of the operation, generates and sends to the processor a status word containing operating status and/or error information. The Port Select Unit (PSU) controls the synchronization of the IOC interface with the processor.

OPERATION INITIATION

The initiation of an information transfer between the processor and an IOC is essentially the same for all devices, the only difference being in the device address contained in the base register (BR1 or BR2) of the processor output select gates. The PSU decodes three-bit groups from the processor to clearly define the requested operation. The command field (nanobits 51 through 54) contains information which determines whether a device read or a device write operation is to be performed. The four least-significant bits of BR1 or BR2 contain the specific device address, and the most significant bit of BR1 or BR2, in conjunction with the command type, indicates the word type (control, data, or status).

WORD FORMATS AND DESCRIPTIONS

Communications between the processor and the IOC are carried out by the transfer of control words, data words, or status words. The word formats are contained in Figure I-1 and described in the following paragraphs.

B0115 CARD READER IOC/DDP WORD FORMATS

	MSB 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	LSB 16
CONTROL WORD	---	---	---	---	---	---	---	---	---	---	---	ENABLE INTER	READ BIN	CLEAR	READ NORM	TERM
DATA WORD, NORMAL	CON-TROL CHECK								DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
DATA WORD, BINARY	---	---	---	---	DATA 11	DATA 10	DATA 9	DATA 8	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3	DATA 2	DATA 1	DATA 0
STATUS WORD	DATA REQ	---	---	DEV ADDR 4	DEV ADDR 3	DEV ADDR 2	DEV ADDR 1	DEV ADDR 0	---	---	---	---	---	TROU-BLE	---	RDY

NOTE: DEVICE ADDRESS BITS OF STATUS WORD ARE INSERTED AT PSU

Fig. I-1. 80-COLUMN CARD READER IOC WORD FORMATS

CONTROL WORD

The operation of the card reader is initiated by the transfer of a control word from the processor to the card reader IOC. This word contains control field which defines the operation to be performed by the card reader. The contents of the control word are as follows:

MIR Bit(s)	Function
1-11	Not used.
12/	Enable Interrupts: enables interrupts from the IOC to the processor. If the start switch is pressed while this bit is in the reset state, the IOC prevents the ready status bit from being set (and causing the resulting status interrupt to be delayed) until a control word with the enable interrupts bit set is received from the processor. The enable interrupts bit is reset upon receipt of a control word with this bit equal to zero, or upon the issuance of a system clear command by the processor.
13/	Read Binary: this bit initiates a card read cycle in the binary mode, causing data to be read from the IOC buffer in 12-bit parallel fashion and transferred to the processor without conversion. This bit is not honored if a card read cycle is in process.
14/	Clear: this bit turns off the read binary or read normal command.
15/	Read Normal: this bit initiates a card read cycle in the normal mode, causing data to be read from the IOC buffer in 12-bit parallel fashion and converted and transferred to the processor in 8-bit code. This bit is not honored if a card read cycle is in process.
16/	Terminate: this bit causes termination of data transfer by disabling data interrupts to the processor. The terminate bit is used to control the number of characters to be fetched from the 80-column buffer and is honored only during data transfers from the buffer to the processor. This bit resets the buffer address register and inhibits further data interrupts.

DATA WORD

Data transfer between the IOC and the Processor is in 8-bit or 12-bit parallel fashion, where bit 16 is considered the least significant bit. The normal data word consists of 8 bits of data and a control check bit; the binary data word consists of 12 bits of data. The contents of the data word (normal mode) are as follows:

EXT Bit(s)	Function
1/	Control Check; indicates that a control check character was detected in the character available on the data lines.
2-8	Not used.
9-16/	Data; used to transfer 8 bits of data from the IOC to the processor.

The bit correlation between the 8-bit processor interface and the 12-bit card reader interface is as follows:

Data Word Bit	Contents	Card Reader Bit
16 (octal 1)	Binary equivalent	RDI1L
15 (octal 2)	of card rows	RDI2L
14 (octal 4)	1 through 7.	RDI3L
		RDI4L
		RDI5L
		RDI6L
		RDI7L
13 (binary 8)	Card row 8	RDI8L
12 (binary 1)	Card row 9	RDI9L
11 (binary 2)	Card row 0	RDI0L
10 (binary 4)	Card row 11	RDI11L
9 (binary 8)	Card row 12	RDI12L

Bit positions 16 through 14 of the data word contain, in octal form, the number of the card row (1 through 7) in which the punched hole appears. Normally, there will be only one hole punched in rows 1 through 7. When more than one hole is punched in these rows, however, it indicates that the character is a control check character. Bit positions 13 through 9 represent the binary number received from the card reader in rows 8 through 12.

The contents of the data word (binary mode) are as follows:

EXT Bit(s)	Function
1-4	Not Used
5-16/	Data; used to transfer 12 bits of data from the IOC to the processor.

The bit correlation between the 12-bit processor interface and the 12-bit card reader interface is as follows:

Data Word Bit	Contents	Card Reader Bit
16 (binary 1)	Card row 1	RDI1L
15 (binary 2)	Card row 2	RDI2L
14 (binary 4)	Card row 3	RDI3L
13 (binary 8)	Card row 4	RDI4L
12 (binary 16)	Card row 5	RDI5L
11 (binary 32)	Card row 6	RDI6L
10 (binary 64)	Card row 7	RDI7L
9 (binary 128)	Card row 8	RDI8L
8 (binary 256)	Card row 9	RDI9L
7 (binary 512)	Card row 0	RDI0L
6 (binary 1024)	Card row 11	RDI11L
5 (binary 2048)	Card row 12	RDI12L

Bits 16 through 5 of the data word represent respectively the binary number received from the card reader corresponding to card rows 1 through 12.

STATUS WORD

The contents of the status word are as follows:

EXT Bit(s)	Function
1/	Data Request; indicates that the IOC is ready to transmit the next character. This status condition follows the data interrupt to the processor. Set whenever a data interrupt is present; reset when the data interrupt is honored.
2-3	Not used.
4-8/	Device Address; these bits are inserted by the PSU.
9-13	Not used.
14/	Trouble: indicates that the card reader detected a read-check resulting from a light or dark check error, or a double strobe comparison error, during a card read cycle. This bit is set, along with the status interrupt signal, after 80-columns of data are loaded into the buffer from the card reader. This condition does not prevent data interrupts. If the processor does not require the data, it issues a terminate command to reset the existing data interrupt and inhibit further interrupts. This bit is not reset until appropriate operator action (a run-out) is performed.
15	Not used.
16/	Ready: set along with the status interrupt signal, when the start switch on the control panel is pressed and the card reader is ready for operation. Reset upon receipt of a read command from the processor, and set again after the IOC reads the 80th column from the card reader if no trouble status or not-ready condition exists.

IOC OPERATION

The IOC operation is controlled by the commands and instructions issued by the processor as described in the following paragraphs.

DATA BUFFER

The IOC contains an 80-column buffer into which data is received from the card reader. This buffer is designed to allow for 12-bit parallel data transfers to the processor.

CONTROL WORD

If the instruction signal and the write signal are received in coincidence from the PSU, it indicates to the IOC that the information on the data lines from the processor is a control word.

DATA WORD

If the instruction signal is absent when a read or write signal is received from the PSU, it instructs the IOC to place a data word on the data lines to the processor.

READ STATUS

If the instruction signal and the read signal are received in coincidence from the PSU, it instructs the IOC to place all status indicators on the data lines to the processor.

TERMINATE

When a control word with the terminate bit set is received from the processor, the IOC disables the present data interrupt and also any subsequent data interrupts to the processor.

READ BINARY

The read binary command causes the IOC to energize the start-card-cycle level to the card reader, thus initiating the card read cycle. The 12-bit parallel transfer of column data from the card reader to the IOC buffer proceeds automatically; each transfer is preceded by a strobe signal from the card reader. Data is stored in sequential locations of the 80-column buffer in the IOC. (The transfer of data to the buffer is terminated by the 80th read strobe from the card reader.) The IOC next sends a data interrupt to the pro-

cessor to inform the processor that data is ready in the IOC for transfer to the processor. The processor returns a read signal when ready, causing the 12 bits of data in the first buffer location to be placed on the data lines to the processor. This process is repeated until the buffer is empty or a terminate command is issued by the processor.

READ NORMAL

The function of the read normal command is the same as that described for the read binary command except that, in this instance, the 12-bit data read from the IOC buffer is converted to 8-bit code prior to its transfer to the processor.

STATUS INTERRUPT

All status bits are returned to the processor in response to an enable status or read status instruction from the processor. The following conditions generate a status interrupt:

a. The device was in a ready state and went into a not ready state. This can occur at any time.
b. A read check was detected during a card read cycle. The interrupt is generated at the end of the cycle that loads the IOC data buffer.
c. Initially, when the start button is pressed and the device is ready. Once the device is in the ready state, pressing the start button does not generate an interrupt until the device has become not ready.

NOTE: The status interrupt is not sent to the processor until the enable interrupts control bit in the IOC is set.

CONTROL CHECK

If, while operating in the read normal mode, the IOC detects more than one hole punched in lines 1 through 7 from the card reader, the IOC sets bit 1 of the data word and returns this condition to the processor in coincidence with the data character in which the multiple punch (control character) was detected. Bit 1 of the data word is always 0 when operating in the read binary mode.

READY

The following conditions cause the ready status bit to be set:

a. Initially, when the start button is pressed and the device is ready.
b. The end of the data transmission, if the device is ready and no read check was detected during the card read operation.

The following conditions cause the ready status bit to be reset:

a. The receipt or a read command, either read normal or read binary.
b. A change in the device status from ready to not ready.

CARD READER CHARACTERISTICS

The B0115 Card Reader IOC provides the interface between the system processor and either the B9115 (300 CPM) or B9116 (600 CPM) card reader. The reader is housed in a cabinet which contains the card reading mechanism, logic electronics, and a stacker pocket, and operates from a 120-volt, 60-Hz, single-phase power source.

INPUT HOPPER

The input hopper has a capacity of 1,000 cards. Cards are loaded into the hopper face down, with the 9-edge toward the rear of the hopper. A card weight is required to ensure reliable feeding whenever the height of the card stack in the hopper falls below one inch. Because no weight is required for card stacks above one inch, cards can be added while the unit is operating as long as the card stack has not diminished below this point.

CARD FEEDER

The card feeder supplies cards at a rate of 300-CPM for the B9115 reader and 600-CPM for the B9116 reader. Failure to feed a card causes the unit to stop after all cards in transit have been read and stacked. Detection of a feed error causes a feed check indicator lamp on the control panel to light. The feeder is so designed to prevent double feeding of cards.

READ STATION

The read station is capable of reading rectangular holes in 80-column punched cards. The cards are read serially, one column at a time, beginning with column 1 and continuing through column 80. The information read is transmitted over 12 data lines to the IOC. A dark and a light check of the read station is performed during each card-read cycle, and the card reading accurracy is monitored on a column-by-column basis. A detected malfunction causes the read check indicator on the control panel to light.

STACKER

The card reader has one stacker with a capacity of 1,000 cards. The cards are stacked in the same sequence as they are fed through the reader. When a full pocket condition occurs, an indicator over the stacker becomes lit. Cards can be removed from the stacker while the unit is in operation.

JAM DETECTION

A card jam can involve not more than two cards, and can be conveniently cleared by the operator. Card handling malfunctions are indicated during the card cycle in which they occur. Feeder jams do not affect the information transfer from the preceding card.

SHUT DOWN

The transport mechanism stops when a not-ready condition occurs. The stop is delayed, however, until all cards in process have been read and stacked.

NOT READY

The occurrence of a not-ready condition causes the card reader to ignore any new commands until the condition is corrected and the start button is pressed. Conditions which cause the card reader to enter the not-ready state are as follows:

a. Power off.
b. Interlocks open.
c. Unit/System switch in unit position.
d. Stacker full.
e. Feed check.
f. Transport jam.
g. Stacker jam.
h. Stop switch pressed.
i. Ready station and hopper empty.
j. Read check.

If any of the (d) through (j) conditions occur while a card is being read, the reader goes into the not-ready state upon completion of the card cycle.

READ CHECK

When the read check condition is detected during a card cycle, it indicates either that cards are punched off registration or the read station is malfunctioning. The following conditions may cause a read check:

a. Light Check. This condition occurs if any of the read station output signals indicate a dark condition at the beginning of an input feed operation.
b. Dark Check. This condition occurs if any of the read station output signals indicate a light condition when the leading edge of the card is covering the read station.
c. Double Strobe Check. As each card passes through the read station, each column is strobed twice. A check error occurs if the information read by the second strobe does not compare with that read by the first strobe.

OPERATOR CONTROLS

The controls are located on the front panel of the card reader and perform the following functions:

a. Power. Pressing the power switch turns on the DC power supplies. This switch does not turn on the motor, however, and the unit remains in a not-ready state.
b. Start. Pressing the start switch resets the not-ready status indicator, starts the feed motor (if all ready conditions are met), and feeds a card into the ready station (if empty). When the card hopper is empty, pressing and holding the stop switch while pressing the start switch (in that order) runs the card out of the ready station into the stacker.
c. Stop. Pressing the stop switch causes a not-ready condition. If this switch is pressed while a card is being processed, the stop is delayed until after the card is read and stacked and the next card is moved to the read station.

OPERATOR INDICATORS

External indicators are located on the unit and perform the following functions:

a. Read Check; Indicator is lit when a read error is detected. To restart after a read check, remove all cards from hopper and hold stop switch while pressing start switch (in that order), to run card out of ready station into stacker. Remove the last two cards from the stacker and place them into hopper. Replace cards removed from hopper and press start switch.
b. Feed Check. Indicator is lit when there is a feed check. To clear a feed check, lift transport cover to clear jammed cards. Reinsert unread cards in front of the cards in the hopper, close cover, and press start switch.
c. Transport Jam. Indicator is lit when a transport jam or stacker jam occurs.
d. Full Stacker. Indicator is lit when stacker is full, interlocks are not closed, or stacker jam exists. If the reader is not ready and has an empty hopper with a card in the ready station, the full stacker indicator blinks on and off.

INTERFACE BETWEEN B0115 IOC AND CARD READER

The signal interface between the Card Reader IOC and the B9115/B9116 Card Reader is provided by adapter cable assembly 1449 4892 and card reader cable assembly 2471 3059.

The logic levels in the B0115 IOC are as follows:

a. Logical True: 3.0 ± 0.45 volts.
b. Logical False: 0 volts to +0.45 volts.

Figure I-2 is a block diagram of the signal interface. Refer to the signal glossary for a description of the signals.

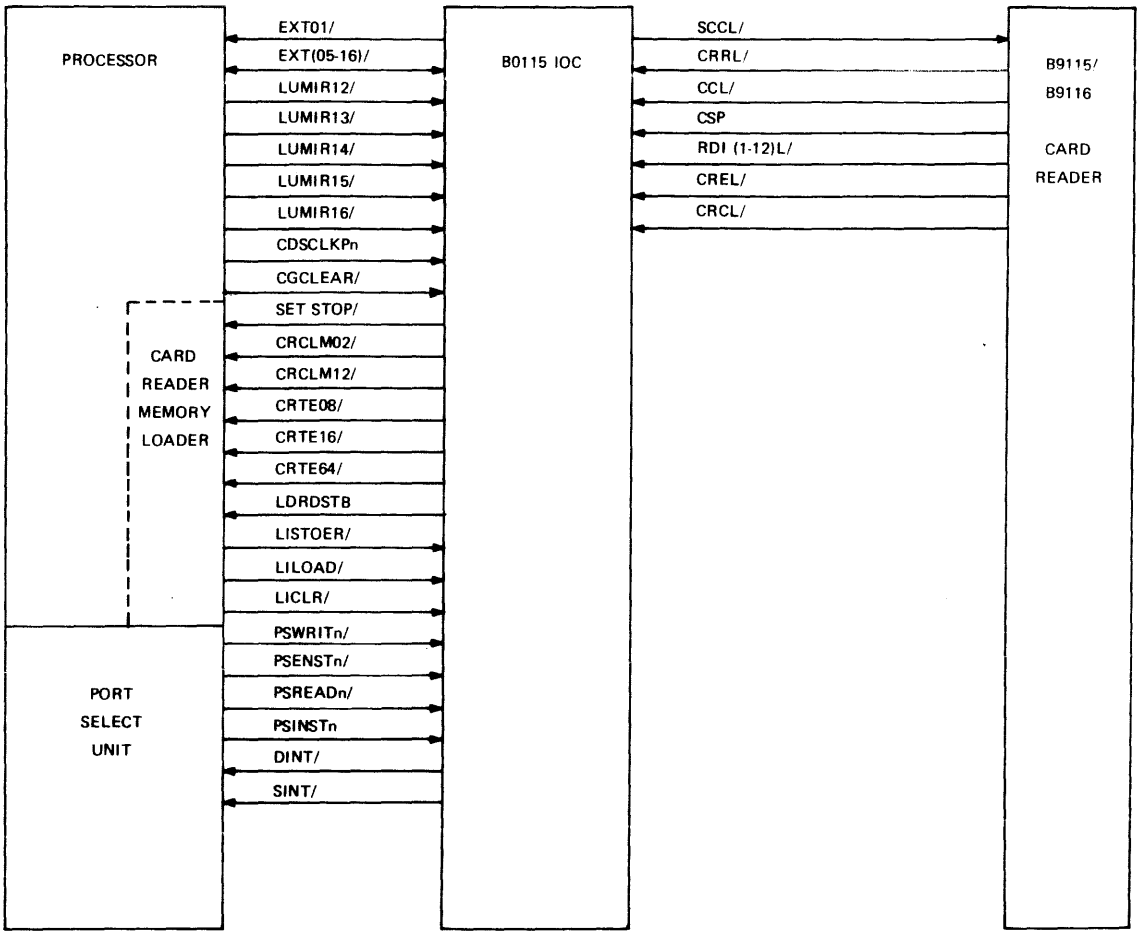

Fig. I-2 B0115 CARD READER IOC SIGNAL INTERFACE, BLOCK DIAGRAM

GLOSSARY OF SIGNAL NAMES

The glossary contains a list of signal names along with a description of the function performed. Also included is a logic drawing sheet number from the IOC FT&R document, which indicates the signal source, or logic function performed.

SIGNAL NAME	LOGIC DRAWING	FUNCTION
		Signals from IOC to Card Reader
SCCL/	1449 5246 (P. 1)	Start Card Cycle Level. This signal causes a single card to leave the ready station and pass through the read station into the stacker. Signal SCCL/ remains active (low) until signals CCL/ and CRRL/ become active (low). Note: To maintain rated card throughput, SCCL/ must follow CCL/ by 133 milliseconds or less for the B9115 (300 CPM) card reader and by 33 milliseconds or less for the B9116 (600 CPM) card reader. Signal SCCL/ is not acknowledged before time necessary for rated throughput.
		Signals from Card Reader to IOC
CRRL/	1449 5212 (P. 2)	Card Reader Ready Level. When active (low), informs the IOC that the card reader is ready to accept SCCL/. High when any not-ready condition occurs.

SIGNAL NAME	LOGIC DRAWING	FUNCTION
CCL/	1449 5212 (P. 1)	Card Cycle Level (67 milliseconds nominal). Indicates that a card is moving from the ready station to the stacker. This signal is active (low) from the time that the start card cycle is accepted until after the 80th column strobe pulse is sent.
CRCL/	1449 5212 (P. 2)	Card Read Continue Level. This signal becomes low (active) when the start push button is pressed.
CREL/	1449 5212 (P. 2)	Card Read Error Level. When low (active), indicates either that card is punched off registration or the read station is malfunctioning. Under these conditions, CREL/ becomes active a minimum of 200 microseconds before signal CCL/ goes high.
CSP	1449 5246 (P. 2)	Column Strobe Pulse (20 microseconds nominal). Strobes read information level signals and indicates to the IOC when card column has been read. Regardless of card length, there are 80 column-strobe-pulses generated and sent to the IOC.
RDInL/ (n=1-12)	1449 5154 (P. 1)	Read Information Levels (640 microseconds nominal). There are 12 read information levels. A low (active) level at column strobe time represents a punched hole.
		Signals from Processor to IOC
CDSCLKPn	1449 5154 (P. 2) 1449 5188 (P. 3)	System clock pulses regenerated and distributed to IOC logics.
CGCLEAR/	1449 5246 (P. 2)	System clear signals generated from system clear pushbuttons, completion of F.E. test sequence, or system power-on clear.
LUMIR (12-16)/	1449 5246 (P. 1-2)	Output data from processor memory information register (MIR) to card reader IOC. Bits 12 through 16 of control word.
	NOTE:	The following signals are transmitted from the Card Reader Memory Loader Interface Control to the IOC. Refer to the B700 Processor technical manual, form 1064482, for a description of the loader interface control (LIC).
LICLR/	1449 5212 (P. 1)	Used to generate address counter clear signal (CRTCLR/). Active low.
LILOAD/	1449 5246 (P. 1)	Used to indicate processor is in load mode. Sets start card cycle flip-flop. Active low.
LISTOER/	1449 5246 (P. 1)	Used to indicate either a stop request or an error. Clears start card cycle flip-flop. Active low.
		Signals from PSU to IOC
PSENTn/ (n=1-8)	1449 5246 (P. 2)	Enable status signal to IOC to permit status information to be placed on EXT lines to processor.
PSINSTn (n=1-2)	1449 5246 (P. 1)	Signals used to signify to IOC either that data on MIR lines is a control instruction, or that status information is to be returned on EXT lines.
		Signals from IOC to Processor
EXTnn/ (nn=01-16)	1449 5188 (P. 2)	External signal bus to processor EXT01/ used as bit 1 of data word (normal) and also as bit 1 of status word. (See Figure I-1.)
	NOTE:	The following signals are transmitted from the IOC to the Card Reader Memory Loader Interface Control in the processor. Refer to the B700 Processor technical manual, form 1064482, for a description of the loader.
CRCLM02/	1449 5188 (P. 3)	Card-column 2 decode. Used by loader to initiate sequence check.

SIGNAL NAME	LOGIC DRAWING	FUNCTION
CRCLM12/	1449 5188 (P. 3)	Card-column 12 decode. Indicates number of 16-bit words in cards.
CRTE08/	1449 5188 (P. 3)	Address counter equals 8. Used to initiate LRC check.
CRTE16/	1449 5188 (P. 3)	Address counter equals 16. Used to indicate start of data field.
CRTE64/	1449 5188 (P. 3)	Address counter equals 64.
LDRDSTB	1449 5246 (P. 2)	Loader Read Strobe. Used to shift data into loader.
SETSTOP/	1449 5246 (P. 1)	Set Stop (in loader). Generated when stop flip-flop (B5-5) is set as a result of change in status of card reader from ready to not ready.
PSREADn/ (n=1-8)	1449 5246 (P. 2)	Read signal to IOC. When active (low), the IOC places either status information or data on the EXT lines.
PSWRITn/ (n=1-8)	1449 5246 (P. 1)	Write to IOC signal. When active (low), the IOC receives either control information or data on the MIR lines.
		Signals from IOC to PSU
DINT/	1449 5212 (P. 1)	Data interrupt signal from IOC to PSU (active low).
SINT/	1449 5212 (P. 3)	Status interrupt signal from IOC to PSU (active low).

Functional Detail

B0115 OPERATIONS

The B0115 Card Reader IOC is a standard four-card buffered IOC which has been permanently assigned to location DDP1 in the processor. The card reader reads cards one column at a time and transmits the data, over 12 data lines in parallel, to the IOC. The IOC, under firmware control, transfers the information to the processor in either the binary or normal mode. (Refer to Section III of the B700 Processor Manual, form 1064482, for a description of the integrated circuit (IC) chips used in the B0115 IOC.)

In binary mode, the 12 bits of data received in parallel from the card reader are transferred, without conversion, to the processor. In normal mode, the 12 bits are converted to 8-bit code by routing bits 1 through 7 through an octal encoder to generate octal bits 1, 2, and 4. The resulting 8-bit code is then transferred to the processor.

READ OPERATION

When a read operation is to be initiated, the processor enables the control levels to the PSU and the Card Reader IOC. To enable a read operation, PSU signal levels PSINSTn must be high and PSWRITn/ must be low. Signal LUMIR12/ must also be low to enable the generation of either the status interrupt signal (SINT/) or the data interrupt signal (DINT/). To select the mode of operation, signal LUMIR13/ (binary) or signal LUMIR15/ (normal) must be low. (It is assumed that the card reader is in a ready state at this time.) When the card reader ready level signal (CRRL/) is received from the card reader it causes the ready level flip-flop (D7-2) to be set, along with the start flip-flop (D7-12) and the ready flip-flop (B3-1). When the ready flip-flop is set, signal CRRDY is generated and used to set the ready status bit (EXT16/) in the status word to the processor.

As a read operation may be performed in either binary or normal mode, the operation for each mode is described separately.

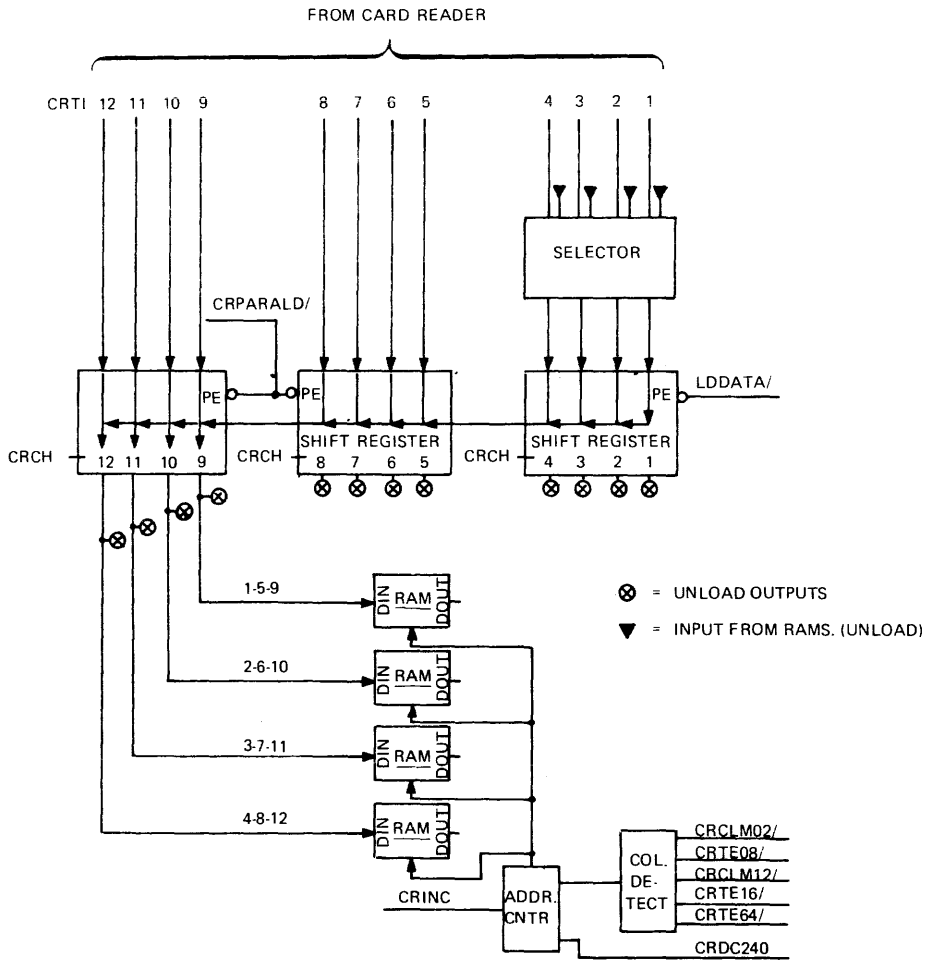

Fig. II-1 BUFFER LOAD OPERATION

BINARY MODE OPERATION

A read operation is initiated in the binary mode after the processor determines that the card reader is in a ready state and sends a control word containing signals LUMIR12/ and LUMIR13/ to the IOC. Signal LUMIR12/ is inverted to generate signal MIR12, which is gated with signal WTINST to set the enable-interrupt flip-flop (C3-8) and generate signal ENINT. (Refer to IOC FT&R documents, logic drawing 1449 5246, pages 1 and 2.) Signal LUMIR13/ is inverted and gated with signals WTINST and BUSY/ to generate signal RDB/ and also to set the read binary flip-flop (B7-1) and generate signal RDBIN. Signal RDBIN is used in the multiplexers to select the four bits of input data to be switched in parallel to the appropriate output terminals. (Refer to IOC FT&R document, logic drawing 1449 5188, page 1.) Signal RDB/ is used to generate the start-card-read signal STCRDRD/. Signal STCRDRD/ sets the start-card-cycle flip-flop (B7-8) and generates the start-card-cycle-level signal SCCL/, which is transmitted to the card reader to begin the movement of the first card from the ready station to the read station. As the card movement begins, the card-cycle-level signal (CCL/) is generated in the card reader and transmitted to the IOC, where it is used to set the card-cycle-level flip-flop (C7-2) and generate signal CCLF/. Signal CCLF/ is used to clear the start-card-cycle-level flip-flop (B7-10) at the end of the 80th column.

As the card is read by the card reader, each column produces a strobe signal (CSP) which is sent to the IOC. For each strobe signal received, the IOC produces a read-strobe signal (RDSTB), a parallel-enable/write-enable signal (CRPEWE), and an address-counter-increment signal (CRINC), respectively (in 1-microsecond steps), by shifting signal CSP through the column strobe shift register (B3-13, 14, 15). (Refer to IOC FT&R document, logic drawing 1449 5246, page 2.) Signal RDSTB is gated with the card-read signal (CRDRD) to produce the parallel-load signal CRPARALD/ which, in turn, gates the 12 bits of data into the three shift registers in parallel (Figure II-1). Signal RDSTB is also gated with signal LILOAD (inverted LILOAD/) to generate the loader read strobe signal (LDRDSTB), which is used to shift the data into the card reader memory loader in the processor. The parallel-enable/write-enable signal (CRPEWE) is gated with the card read signal (CRDRD) to generate the write enable signal (CRWE/), which causes bits 9 through 12 to be loaded into the random access memory (RAM). The address counter increment signal (CRINC) now steps the address counter in preparation for the next four bits (5 through 8) to be loaded into the RAM.

The shift signal (CRSHIFT/), gated with signal CDSCLKPn, generates four shift clock pulses (SHFTCLK/) and moves up the data in the shift registers. A second write-enable signal (CRWE/) is now generated, and bits 5 through 8 are loaded into the RAM in address 1. At this time, a second address-counter-increment signal (CRINC) is generated and steps the address counter to 2. A second CRSHIFT/ signal produces four more shift clock pulses (SHFTCLK/, Figure II-2) and the data in bits 1 through 4 is now moved to the top of the shift register. As a third CRWE/ signal is generated, bits 1 through 4 are loaded into the RAM in address 2. The third CRINC signal now increments the RAM address counter up to 3 in preparation for the next column of data from the card reader. This process is repeated for each of the 80 columns of the card being read.

After the 80th column is read, the RAM address counter contains the count of 240. This condition produces signal CRDC240 (Figure II-3) which sets the CT240 flip-flop (B7-2) and generates signal CRD240. Signal CRD240, in turn, sets the data flip-flop (C3-1) and generates signal DATA which is gated with signals INC and SHIFT/ to set the DINT flip-flop (C5-1). The reset side output of the DINT flip-flop is inverted and gated with the enable-interrupt signal (ENINT) to produce signal DINT/, which is sent to the processor to indicate to the processor that the buffer is full. After this cycle, signal DINT/ is sent to the processor for each column of data read from the card reader.

The address counter is now reset to 0 by signal CRTCLR/, which is produced by signal CT240/. (Refer to IOC FT&R document, logic drawing 1449 5212, page 1.) Following this, the data in RAM address 0 is shifted back into the shift registers (Figure II-4). The CRD240/ signal is now used to produce the same signals that were produced by signal CSP during the card read operation. When three CRINC signals are produced, the data in the shift registers equals column 1 of the card read, and the address counter is stepped to 3. The processor can now send a data read instruction (PSREAD/) to produce signal CRENDATA and gate the data onto the EXT lines to the processor. (Refer to IOC FT&R document, logic drawing 1449 5188, page 2.) A DINT/ signal is again sent to the processor and the next column of data begins the transfer from the RAM to the shift registers. This process continues until the address counter reaches a count of 240 and resets the data flip-flop, thereby inhibiting the generation of more DINT/ signals to the processor. At this time, a new SCCL/ signal is sent to the card reader to start the next card cycle and repeat the entire reading process for the next card.

If any trouble develops during a card read operation, a SINT/ signal instead of a DINT/ signal is sent to the processor at address count 240 and the data read from that card is ignored. When this occurs, the card must be reread.

When the status of the card reader changes from ready to not ready, the low signal level applied to B5-2 allows the stop flip-flop (B5-3) to be reset by the leading edge of signal CLK/. This condition generates signal SETSTOP/, which is transmitted to the processor to set the stop flip-flop in the memory loader interface control.

Functional Detail

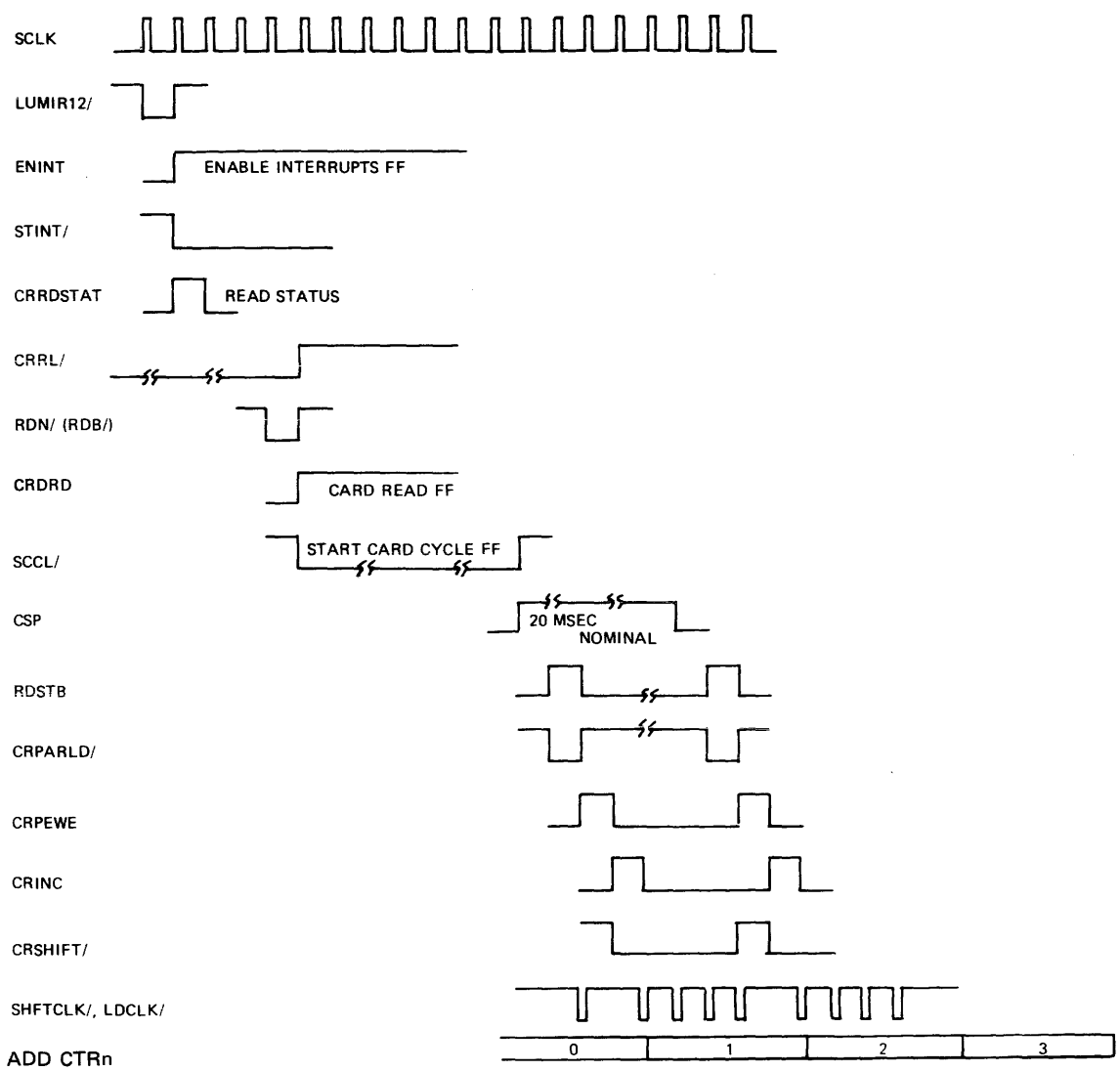

Fig. II-2 BUFFER LOAD TIMING, FIRST COLUMN

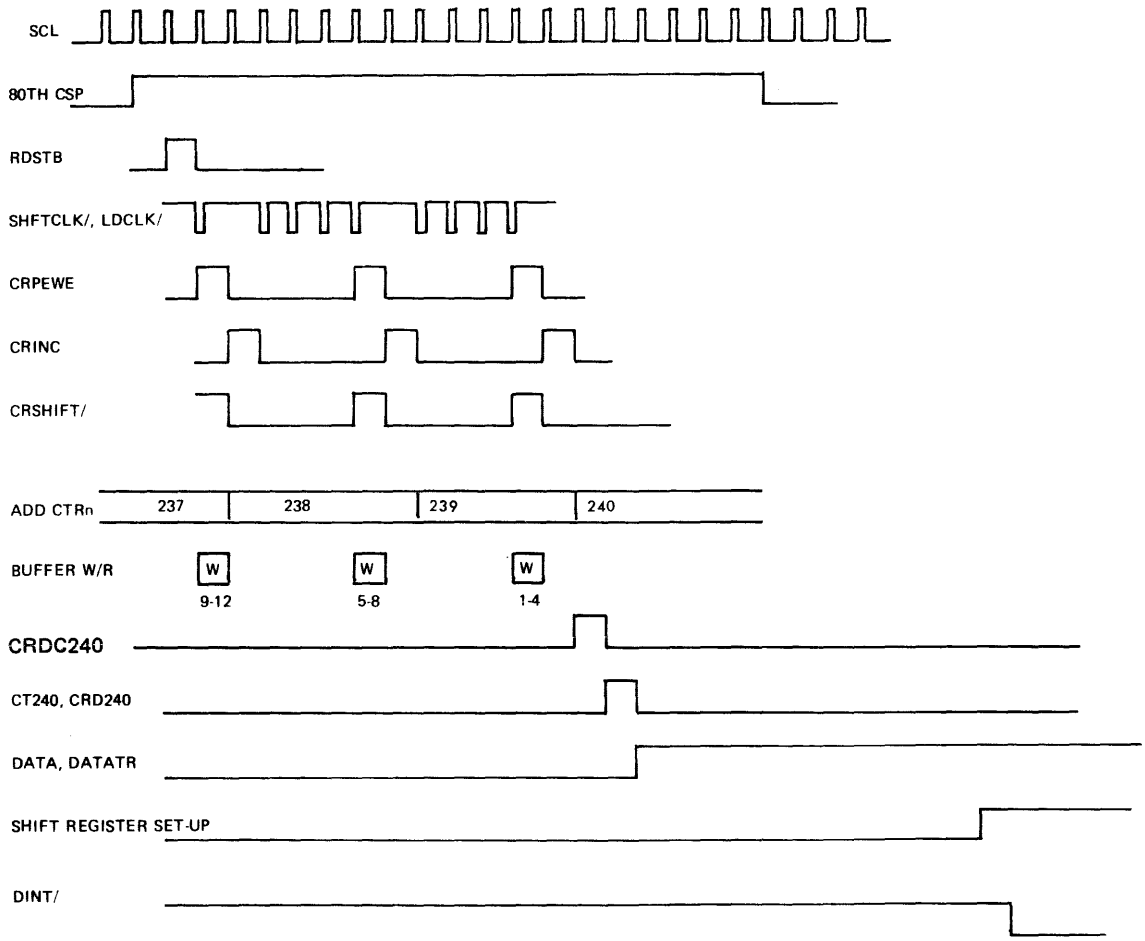

Fig. II-3 BUFFER LOAD TIMING FOR LAST COLUMN AND FIRST DATA INTERRUPT

NORMAL MODE OPERATION

A read operation is initiated in the normal mode when the processor sends, to the IOC, a control word containing signals LUMIR15/ and LUMIR12/. Signal LUMIR15/ is inverted and gated with signal WTINST and BUSY/ to generate signal RDN/ and also to set the read normal flip-flop (C7-8). C7-8 generates signal RDNORM, while signal LUMIR12/ enables the generation of either SINT/ or DINT/. Signal RDN/ is used to produce signal STCRDRD/, which sets the start-card-cycle flip-flop (B7-8) to initiate the start-card-cycle-level signal (SCCL/) and initiate the movement of the first card in the reader from the ready station to the read station. This action starts the same card reading procedure described for binary mode operation with the exception that, when the RAM unloading operation takes place, bits 1 through 7 are gated into an octal encoder (enabled by signal RDNORM) to produce signals OCT1, OCT2, and OCT4. (Refer to IOC FT&R document, logic drawing 1449 5154, page 2.) These signals, along with signals CRCH8 through CRCH12, are placed on the EXT lines to the processor, thus changing a 12-bit data word to an 8-bit data word.

CONTROL CHECK

In normal mode, a validity check is made on data bits 1 through 7 to ensure that only one hole has been punched. If more than one hole has been punched, the data is recognized as a control check character and the control check signal (CONCK) is generated. (Refer to IOC FT&R document, logic drawing 1449 5188, page 1.) During data transfer, signal CONCK is used to generate signal EXT01/ in the data word to inform the processor of the detection of the control check character.

STATUS INTERRUPT

A Status Interrupt (SINT/) signal informs the processor of a change which has occurred in the status of the card reader. For the card reader IOC, the Status Interrupt is initiated by a not-ready condition (Figure II-5). The processor reads the status bits when signal PSINST is high and

signal PSREAD/ is low, or signal PSENT/ is low. Either of these conditions generates signal CRRDSTAT which resets the SINT flip-flop and also enables the EXT lines. There are three status conditions gated to the EXT lines as follows:

a. Data Request. This status condition follows the data interrupt to the processor and informs the processor that the IOC is ready to transmit the next character. Data Request is set whenever a data interrupt is present and reset when the data interrupt is honored.

b. Trouble. This status condition indicates that the card reader detected a read-check resulting from a light or dark check error (or a double strobe comparison error) during a card read cycle. This bit is set, along with the status interrupt signal, after 80 columns of data are loaded into the buffer from the card reader. This condition does not prevent data interrupts.

c. Ready. This status signal is generated when the start switch on the control panel is pressed and the card reader is ready for operation. It is reset upon receipt of a read command from the processor and set again after the 80th column of the card has been read and no trouble exists.

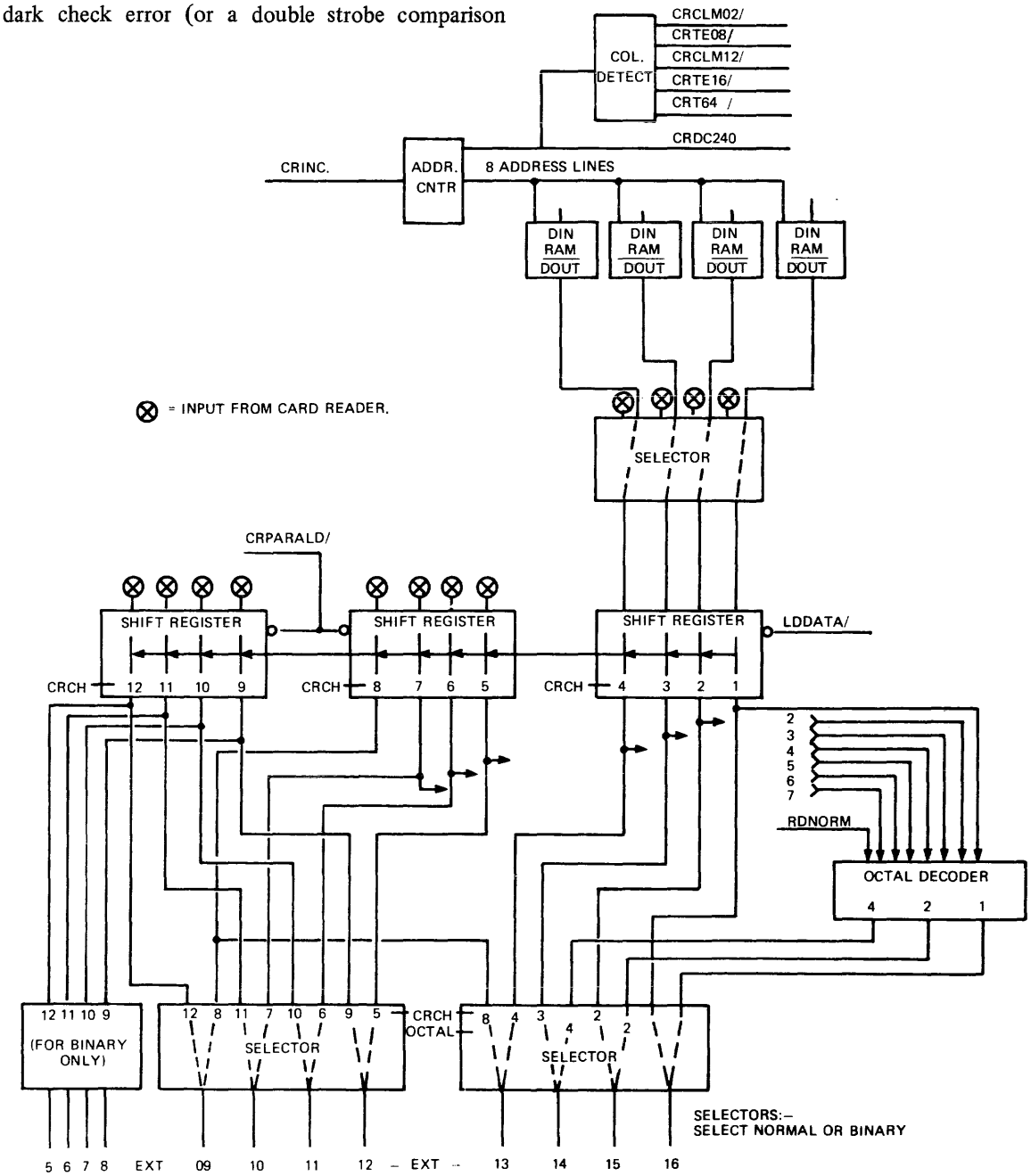

Fig. II-4 BUFFER UNLOAD OPERATION

Functional Detail

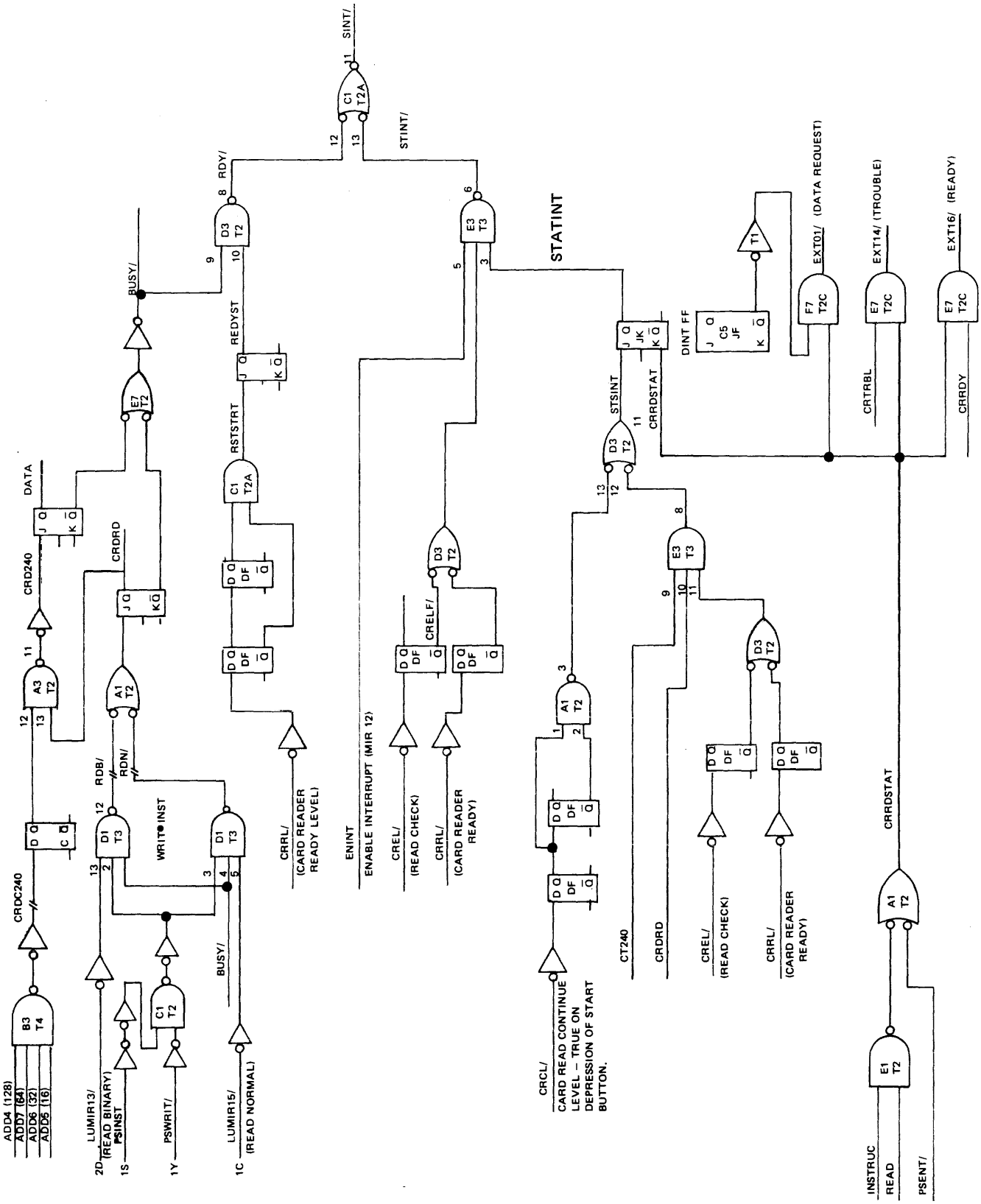

Fig. II-5 STATUS INTERRUPT, LOGIC DIAGRAM

Maintenance Procedures

INTRODUCTION

The B0115 Card Reader IOC is maintained by running the Card Reader Maintenance Test Routine (CR9115MTR), 2601 4274. A program listing, complete operating instructions, and a failure dictionary are included in the Operator Instructions listing, 2601 4266. (The test deck part number is 2601 7608.) Additional manual diagnostic operations, using this technical manual, FT&R documentation, and test equipment may be required to further diagnose and repair failures if the MTRs do not locate the defective component/circuit.

MAINTENANCE AIDS AND EQUIPMENT

The following maintenance aids are required to implement the MTRs and perform maintenance on the Card Reader IOC:

a. Field Engineering (F. E.) cards FE-1 through FE-4.
b. MTR meter.
c. Tektronix Model 453 oscilloscope.
d. Card extender kit (1447 7102).
e. Applicable MTRs.
f. Special maintenance tools (insertion/extraction, wire wrap/unwrap, pin extractor, and card puller tools).
g. Frontplane connectors (two-each 1534 3940).

The Processor Technical Manual, form 1064482, Section V, contains descriptions and identification/application data for the F. E. cards, MTR meter, and card extender kit.

MAINTENANCE TEST ROUTINES (MTRS)

When the Card Reader IOC MTR (CR9115MTR) is implemented, it detects and diagnoses failures within the IOC, or validates the operation of the Card Reader. It cannot diagnose a failure in the Card Reader, but can be interpreted to indicate or point to a failure in the Card Reader. Refer to Section V of the Processor Technical Manual, form 1064482, for a description of the MTR implementation and diagnostic process.

Installation Procedures

INSTALLATION

When the card reader is used as a memory loader in the B777 Processor, the B0115 Card Reader IOC must be installed in control location numbered DDP1. (DDP1 interfaces directly with the Memory Loader Interface Control in the processor.) When a standard card reader interface is used, the Card Reader IOC may be installed in any of the seven interchangeable control locations (DDP1 through DDP7) in the B771 or B772 Processor. Table VI-1 contains installation reference data for the B771/B772 systems.

After installing the IOC P. C. cards, install frontplane connectors (1534 3940) to adjacent cards as follows:

a. CRT1 and CRT2.
b. CRT3 and CRT4.

On the wiring side of the card backplane, slide the large template (1448 2400) over the backplane pins for the DDP location used for this IOC. This identifies those pins to conform to the overlay circuit list contained in documentation package 1449 4900.

On the wiring side of the I/O connector backplane corresponding to the selected DDP location, slide the small template (1448 8712) over the backplane pins.

Next, attach the plug of the IOC adapter cable (1449 4892) to the appropriate I/O connector (J91 through J97) and mount the connector block on the other end of the adapter cable to the adapter panel. (Use the hardware provided.)

Mark the adapter panel decal (1448 6757) to indicate the location in the adapter panel in which the connector block was installed. Attach the decal containing the IOC identification and serial number to the configuration plate in the space indicating the DDP location used for this IOC.

After installation is completed, check the +5 volt supply as instructed in FT&R document Vol. 1, pages 179 through 182, or Section IV of the B700 Processor Manual, form 1064482. To ensure proper operation, run the B0115 IOC MTR (CR9115MTR, 2601 4274). If initial installation of system, run memory, processor, and console MTRs to verify system operation prior to running the IOC MTR.

TABLE VI-1. CARD READER IOC INSTALLATION INFORMATION (B771 SYSTEMS)

CARD			DDP Number and Card Location (B771 Processor)						
Type	Part No.	Function	1(J90)*	2(J96)*	3(J95)*	4(J94)*	5(J93)*	6(J92)*	7(J91)*
CRT1	1449 5139	Control	DL7	DW6	FV4	DV4	FU2	DU2	DP1
CRT2	1449 5162	Data 9-16	DL4	DW3	FV1	DV1	FT9	DT9	DN8
CRT3	1449 5196	Data 1-8	DL1	DW0	FU8	DU8	FT6	DT6	DN5
CRT4	1449 5220	Special	DK8	DV7	FU5	DU5	FT3	DT3	DN2

* I/O connector numbers in parentheses