B0111 80 COL. CARD READER DDP

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

Burroughs

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√ CHANGES OR ADDITIONS

On "Revised" pages, the check mark (√) shown to the left of items or subject titles indicates changes or additions since last issue.

GENERAL

The B0111 DDP provides the interface between the A9114 Card Reader and the system computer.

The Card Reader DDP acts upon control words from the Processor, performs the operation specified and communicates with the Processor by sending data or status interrupts. The Port Select Unit will control the synchronization of the DDP and the Processor.

In operating the B0111 DDP, the Processor will do a device write, a device read or an address status request. Below are device operation tables.

DEVICE OP'S		CONTROL BITS (MIR)	COMMENT
DW	OSI & Dev. Addr.	MIR16/	Terminate
DW	OSI & Dev. Addr.	MIR15/	Pick
DW	OSI & Dev. Addr.	MIR14/	Dev. Clear
DW	Dev. Addr.	MIR16/, 15/ OR 14/	Not Allowed
DR	OSI & Dev. Addr.		Read Status
DR	Dev. Addr.		Read Data
ASR			Read Addr. of Device and Enable Status

OSI and Device Address are located in the Base Register, either BR1 or BR2 as selected by DW1 or DW2, or DR1 or DR2.

The Processor device operations will be enabled to the Port Select Unit as selected by the address contained in the OS lines. The OS lines also select the DDP which will receive the operation by selecting the write or read line, depending on whether a DW or DR OP. is to take place for that device.

The Address Status Request operation (ASR) selects the highest priority DDP that is sending an Interrupt Request (IRQ). ASR will enable the Enable Status Line to that DDP and insert the address of the DDP in the Ext Lines along with the status bits that were inserted by the DDP. The ASR operation takes place at the PSU. The DDP sends Data and Status Interrupts to the Port Selected Unit which will select an IRQ, SRQ or an URQ to be sent to the Processor. The Processor will act upon these conditions with a device operation as previously shown.

INTERRUPT	UNSELECTED	SELECTED	CONDITION
DINT	*		IRQ
DINT		*	SRQ
SINT	*		IRQ
SINT		*	URQ

WORD FORMATS

There are three word formats used with card read operations. See Fig. 1.

1. Control Word – Card reader operation is initiated by the transfer of a control word on the MIR lines from the Processor to the DDP. The control word contains three operation bits; the other bits of the MIR are not used. The operation bits are as follows:

MIR	DEFINITION
16	Terminate – This operation is used to control the number of characters to be fetched from the 80-character buffer. The terminate operation will be honored only during the data transmission portion of the card read cycle. This operation will reset the Buffer Address Register and inhibit further data interrupt.
15	Pick or Read Card – This operation initiates a card read cycle. This operation will not be honored if a card read cycle is in process.
14	Device Clear – This operation resets the read cycle when the Processor detects a card jam or the input hopper is empty.

2. Data Word – The DDP transfers the data from the Card Reader to the Processor on the Ext. lines 16 through 9. The other Ext. bits are not used.

EXT	DEFINITION
16	OCTAL 1 (OCT1)
15	OCTAL 2 (OCT2)
14	OCTAL 4 (OCT4)
13	Card Column 8 (CC8)
12	Card Column 9 (CC9)
11	Card Column 0 (CC0)
10	Card Column 11 (CC11)
09	Card Column 12 (CC12)

NOTE: Card Columns 1 through 7 are encoded in an OCTAL fashion.

3. Status Word – The DDP transfers the status bits on to Ext. Lines to the Processor.

EXT	DEFINITION
16	Ready – This bit is set initially by the Restart Switch on the Card Reader if the No Feed is not set. Ready is also set after the data transmission portion of the card cycle is complete or after a terminate operation.
15	No Feed – This bit is set and reset by the No Feed Switch on the Card Reader.
14	Trouble – This bit is set after a card is loaded into the buffer if during the check trouble time any of the photo cells do not detect its light source. Trouble does not inhibit a data interrupt from setting.
13	Status Leading Edge Cell – This bit is set by the Leading Edge Cell Detector in the Card Reader.
12	Status Early Feed Cell – This bit is set by the Early Feed Cell Detector in the Card Reader.
11	Not Used.
10	Not Used.
09	Not Used.

Introduction and Operation

B0111 CARD READER DDP WORD FORMATS

MIR EXT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CONTROL WORD	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	DEV. CLR.	PICK OR READ CARD	TERM
DATA WORD	0	0	0	0	0	0	0	0	CC12	CC11	CC0	CC9	CC8	OCT4	OCT2	OCT1
STATUS WORD	DR	0	0	DA	DA	DA	DA	DA	0	0	0	SEFC	SLEC	TRBL	NO FEED	RDY

NOTE: 0 = NOT USED
Ø = DON'T CARE
DA IS GENERATED BY PSU

FIGURE I-1 WORD FORMATS

08 Device Address – These bits are generated by the PSU in response to a device read for status or an ASR operation.
07
06
05
04
03 Not Used.
02 Not Used.
01 Data Request – This bit is set whenever a data interrupt is present.

CARD READER DDP SIGNAL LINES
INTERNAL NAMES

CRACLR/ Clear
CRBSY/ Busy
CRBUOCT1 Buffered Outputs of Memory Representing the First Eight Bits of Data
CRBUOCT2
CRBUOCT4
CRBUCC8
CRCKTRBL Check Trouble
CRCSO/ Outputs of the Address Counter for each group of 16 Addresses
CRCS16/
CRCS32/
CRCS48/
CRCS64/
CRCT=80/ Address Counter is equal to 80
CRCTRCLR/ Counter Clear for Increment and Address Counter
CRDATATR Data Transmission Flip-Flop Output, Will be True when Data is being Transmitted to the Processor.
CRENDATA/ Enable Data to the Ext. Lines
CRINCR Increment Address Counter
CRNOFEED Status from Card Reader
CRRDATA/ Read Data, Will be True when Data is being Transmitted from the DDP to the Processor.
CRRDCRD Read Card, Will be True when Data is being Transmitted from the Card Reader to the DDP
CRREADY Ready Status
CRSDT Set Data Transmission Flip-Flop
CRSEFC Early Feed Cell Status
CRSLEC Leading Edge Cell Status
CRSTAT Enables Status Bits to the Ext. Lines
CRSTINT Status Interrupt Flip-Flop Output
CRSTINH Reset the Inhibit Flip-Flop
CRTRBLE Output of the Trouble Flip-Flop
CRWRITE/ Enables the Data from the Card Reader into the Memory
CRXADD1/ Outputs of the Address Counter, Counts for each group of 16
CRXADD2/
CRXADD4/
CRXADD8/
CRXLEC/ Leading Edge Cell Level

CARD READER TO DDP

CC12 8 Bits of Data to the DDP
CC11
CC0
CC9
CC8
OCT4
OCT2
OCT1
EFC/ Output of Early Feed Cell
LEC/ Output of Leading Edge Cell
NOFD Output of No Feed Switch
SC123 Strobe Counter Output
TROUBL Output of Trouble Circuit
GO/ Output of Start Circuit

Introduction and Operation

DDP TO CARD READER

CRRC0/ Enables Strobes from the Card Reader until the Strobe Counter reaches a Count of 7

CRRC1/ Pick Command to the Card Reader

PROCESSOR TO DDP

LUMIR16/ Control Bit for Terminate Operation

LUMIR 15/ Control Bit for Pick Operation

LUMIR14/ Control Bit for Device Clear Operation

DDP TO PROCESSOR

CREXT01/ Ext. Line 1 to the Processor, used only in the Status Word as Data Request

CREXT09/ Ext. Line 9 to the Processor, used only in the Data Word for Data Bit CC12

CREXT10/ Ext. Line 10 to the Processor, used only in the Data Word for Data Bit CC11

CREXT11/ Ext. Line 11 to the Processor, used only in the Data Word for Data Bit CC0

CREXT12/ Ext. Line 12 to the Processor, used for Data Bit CC9 and Status Bit SEFC

CREXT13/ Ext. Line 13 to the Processor, used for Data Bit CC8 and Status Bit SLEC

CREXT14/ Ext. Line 14 to the Processor, used for Data Bit OCT4 and Status Bit TRBL

CREXT15/ Ext. Line 15 to the Processor, used for Data Bit OCT2 and Status Bit NO FD

CREXT16/ Ext. Line 16 to the Processor, used for Data Bit OCT1 and Status Bit Ready

PORT SELECT UNIT TO THE DDP

CLEAR Clear

ENST/ Enable Status

INST Instruction

READ/ Read

SCLK Clock

WRITE Write

DDP TO THE PORT SELECT UNIT

CRDINT/ Data Interrupt

CRSINT/ Status Interrupt

See Fig. 2

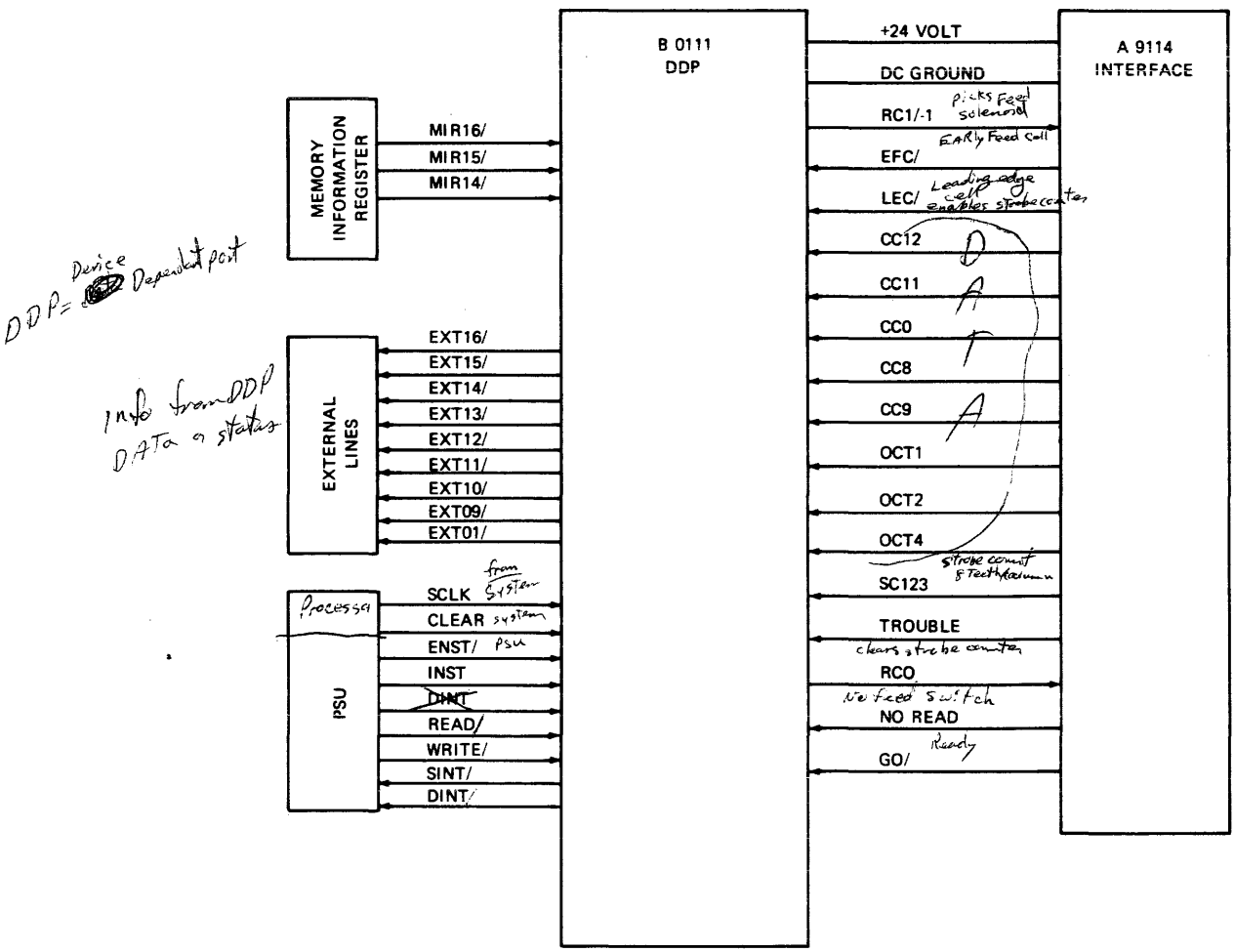


Fig. I-2 INTERFACE

Functional Detail

GENERAL

The B0111 DDP will normally be in the unselected state. The DDP becomes selected when the Processor initiates an operation. If the DDP is ready for operation, the Ready Status bit will be true and a Status Interrupt will be sent to the PSU. The PSU will generate an IRQ to be sent to the Processor. When the Processor tests for an IRQ, the Processor will generate an ASR to the PSU. The PSU will generate the address of the highest priority device sending an IRQ. When the B0111 DDP address is sent to the Processor, the DDP will send the status bits to the Processor on the Ext. Lines.

The Status Ready is generated by the level GO/ being false from the Card Reader when the data transmission cycle is completed or when a terminate operation is completed. Initially, Ready is generated by GO/ being false. GO/ enables a single shot to clock the Pready flip-flop. The Pready flip-flop is set by BSY/ being true. The Q output of the Pready FF will set the Ready flip-flop with the next SCLK. See Figure I.

The Q output of the Pready FF, PREADYF/, being false will set the Status Interrupt flip-flop at the same time the Ready FF is set. See Figure II. The output of the Status Interrupt FF, CRSINT/, goes to the PSU. The PSU will generate an IRQ to the Processor. When the Processor responds to the IRQ from the DDP, the Processor will initiate an ASR operation. ASR will enable the ENST/ to go false from the PSU to the DDP. ENST/ being false will enable level CRSTAT. CRSTAT will enable Ready to Ext. Line 16. The Processor receives the status and will respond with a Pick operation. The Processor will initiate a DW operation and insures that the instruction bit and the device address are contained in the Base Register 1 or 2. The MIR lines will contain the control word, MIR15/ is false for a Pick operation. DW and the OS lines go to the PSU to select the write line for the B0111 DDP along with the INST level.

MIR15/ False, WRITE/ False and INST True will enable level SPICK/ to go false. SPICK/ being false will reset the Ready flip-flop (see Figure I) and sets the Pick and Read Card flip-flops. See Figure III. The Pick FF will cause level CRRC0/ to go false to the Card Reader. The Pick FF will also cause level CRRC1/ to go false to the Card Reader. CRRC1/ being false will enable the Pick Solenoid in the Card Reader.

The first card is picked into the Read Station, where the Early Feed Cell detects the card. The Early Feed Cell level, EFC/, will go false and reset the Pick FF which will cause level CRRC1/ to go true, disabling the Pick Solenoid in the Card Reader. EFC/ False will also keep CRRC0/ false now that the Pick FF was reset. CRRC0/ False inhibits the Strobe Counter from sending level SC123 until it has reached a count of 7. As the card continues on to the Read Station, the Leading Edge Cell detects the leading edge of the card and causes level LEC/ to go false to the DDP. LEC/ False will also enable the Strobe Counter to count and enable SC123 after a count of 7. When SC123 goes true, the Increment Counter will be enabled. The Increment Counter consists of three FF, A, B and C. SC123 will set the A FF with the SCLK. The A FF output will set the B FF with the next SCLK.

The B FF will set the C FF with the next SCLK. See Figure I. The output of the Read Card FF, CRRDCRD, will cause level CRWRITE/ to go false when the A FF is set. CRWRITE/ False will allow the data from the Card Reader to be stored in memory. When A FF and B FF are set, CRRDCRD will enable the Increment Write Gate, INCWR. INCWR will enable the Increment Gate, INCR. INCR will allow the Address Counter to count up the address for the next word of data from the Card Reader. The Address Counter will be incremented up to 80. The reading of the first card is completed. Level CT-80/ False will set the Inhibit FF which will inhibit the Increment Counter. As the card passes by, the Leading Edge Cell, LEC/, will go true. LEC/ going true will enable a single shot to set the Check Trouble FF, CKTRBL. CKTRBL will enable the setting of the Trouble FF if trouble exists in the Card Reader. See Figure II. CKTRBL FF will also set the SDT FF, Set Data Transmission FF. The output of the SDT FF will be gated as SDT and SDT/. SDT True will set the Data Transmission FF and SDT/ False will set the Data Interrupt FF. SDT will also enable the setting of the Trouble FF if Trouble exists in the card reader. See Figures II, I and IV.

The Data Interrupt will go to the PSU and raise an IRQ to the Processor. When the Processor responds to this IRQ, the Processor will do an ASR operation. The status bits will be enabled to the Ext. Lines. Data Interrupt will be enabled to EXT01/. See Figure VI. The Processor responds by doing a Device Read, insuring that the address of the DDP is in the Base Register. The Instruction Bit is not set for this operation. The PSU will enable the read line to the B0111 DDP. The READ/ level will reset the Data Interrupt FF and cause the read data levels RDDATA to go true and RDDATA/ to go false.

RDDATA will cause ENDATA/ to go false which will enable the first word of data from the memory to the Ext. Lines. See Figure VI. RDDATA/ False enables the Increment Counter. When the A FF is set, the Increment Read Gate will be enabled by the output of the Data Transmission FF, DATATR. The INCWR and the CRWRITE Gates were disabled when SDT reset the Read Card FF. INCRD will enable the INCR Gate to increment the address counter to the next address. When the B FF is set, the SDINT Gate will be enabled to set the Data Interrupt FF. The Processor responds to this DINT by doing another device read operation. This routine continues until the Address Counter is equal to 80. CT=80/ False will set the Inhibit FF which will inhibit the Increment Counter.

CT=80/ False will also set the Ready FF and reset the Data Transmission FF. DATATR will go false causing BSY/ to go true. BSY/ True will set the Pready FF which will set the Status Interrupt FF. The Processor will respond to this SINT by doing a device write operation and sending a Pick control word to the DDP. When the Processor does a Pick operation and there are no cards in the hopper, the DDP will not respond with a DINT. The Processor on not receiving a DINT will read the status bits. If the EFC and LEC status are not present, the Processor will send a Device Clear Operation to the DDP.

The Processor may issue a terminate operation at any time during the transmission of data from the DDP. The Processor will issue a device write, insuring that the device address and the instruction bit are set in the Base Register. The Processor will issue the control word on the MIR lines. MIR16/ will be false for the terminate operation. MIR16/ False, WRITE/ False and INST True will enable the Terminate Gate, the output being TERM/. TERM/ being false will reset the Data Transmission FF and inhibit the Data Interrupt FF from setting. TERM/ False will set the Inhibit FF and set the Ready FF. The Processor can now pick another card. See Figures II-1 and II-4.

The Processor will issue a Device Clear Operation when a card read cycle is issued and the input hopper is empty or a card jam has occurred. These two conditions are detected by the Processor programmatically. A time-out condition checks the time between a Pick operation and a Data Interrupt. The Processor will check the status bits, Early Feed Cell and Leading Edge Cell. If a time-out condition occurs, the Processor will issue a Device Clear Operation. The Processor will do a Device Write with the Instruction Bit and the device address set in the Base Register. The MIR lines will contain the control word with Bit 14/ False. MIR14/ False, WRITE/ False and the Instruction Bit level, INST True, will enable the Clear level. The Clear level, DRVCLR, will reset the Pick and Read Card FF. See Figure II-3.

Functional Detail

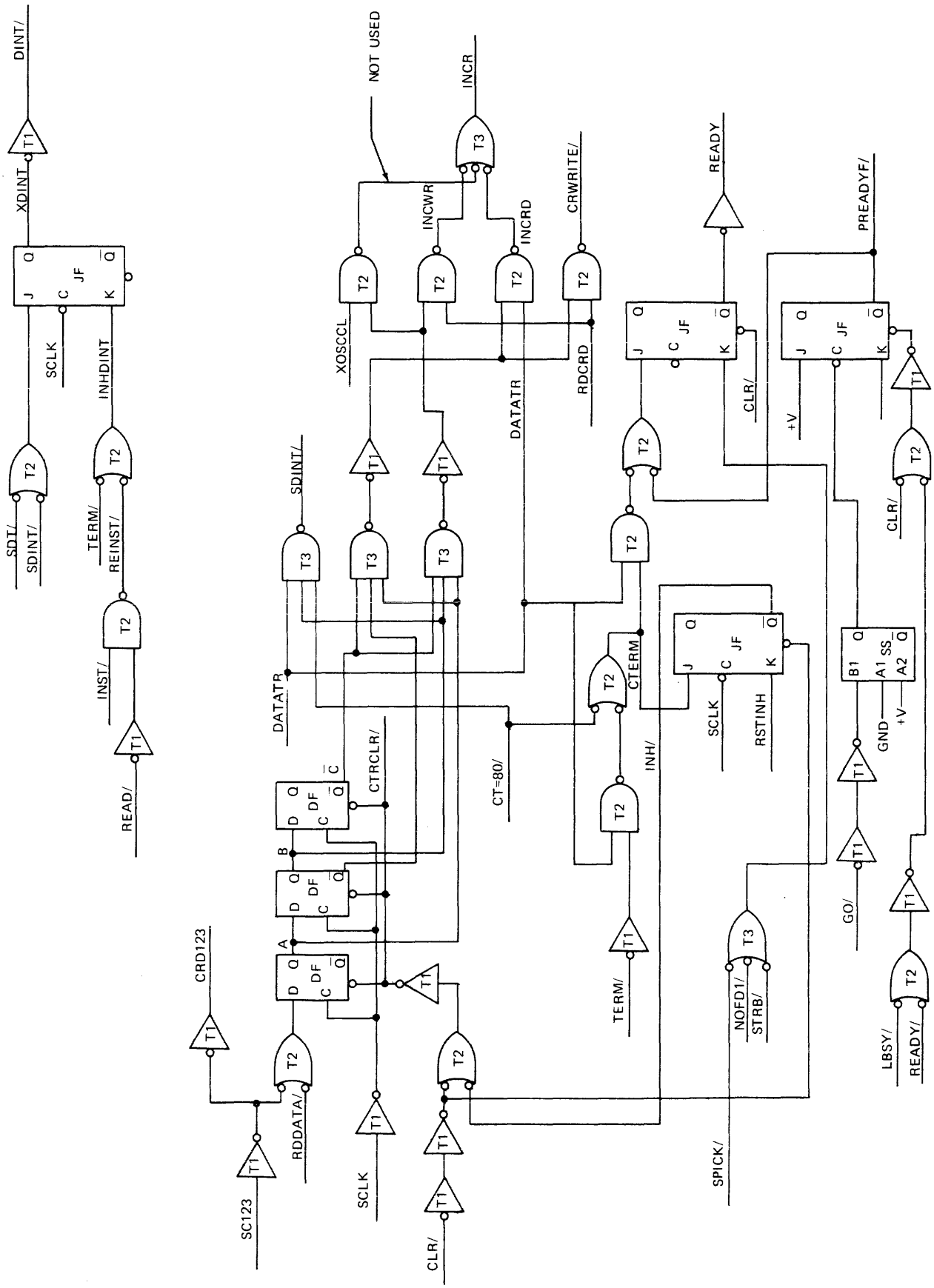


Fig. II-1

Functional Detail

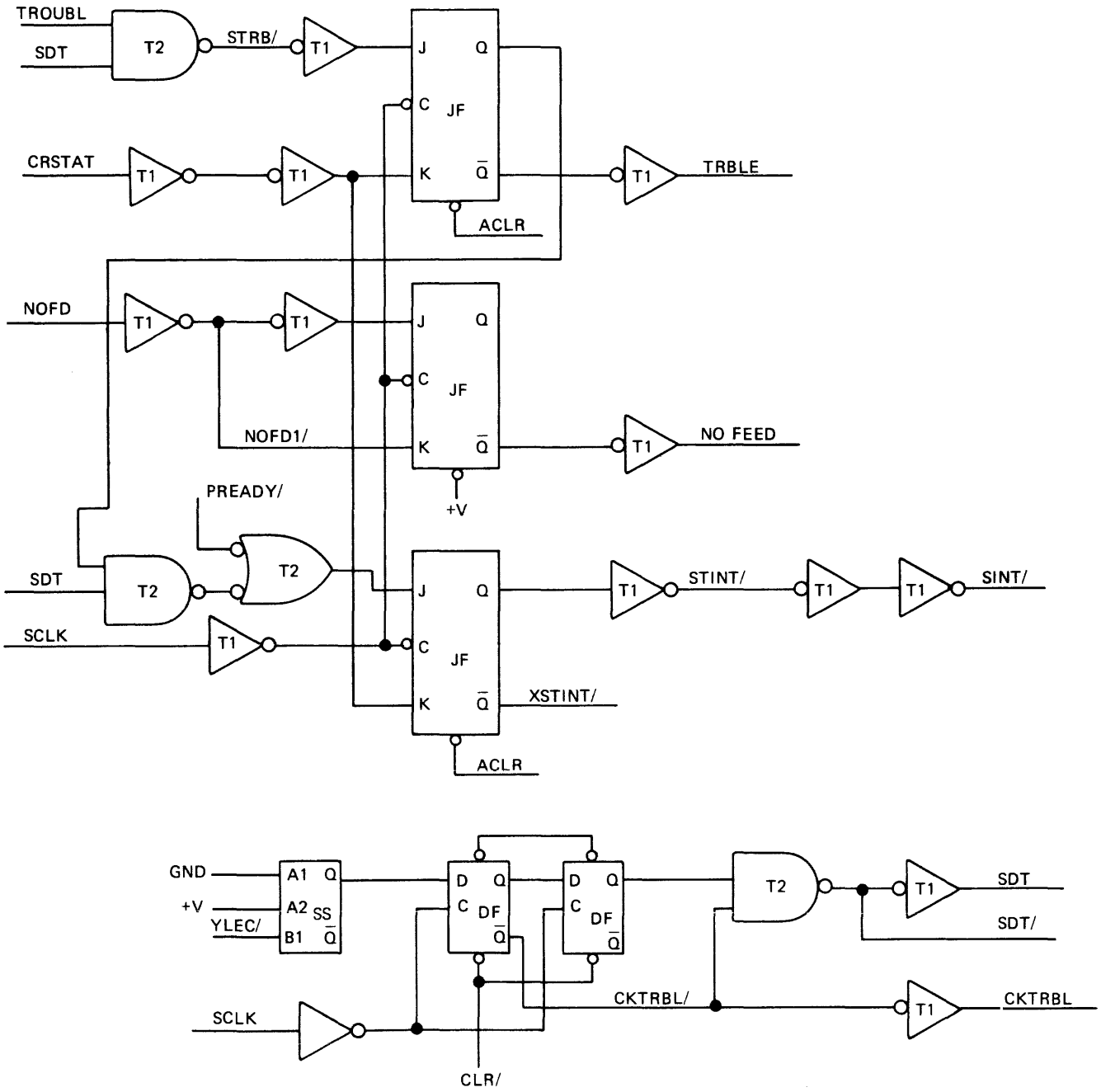


Fig. II-2

Functional Detail

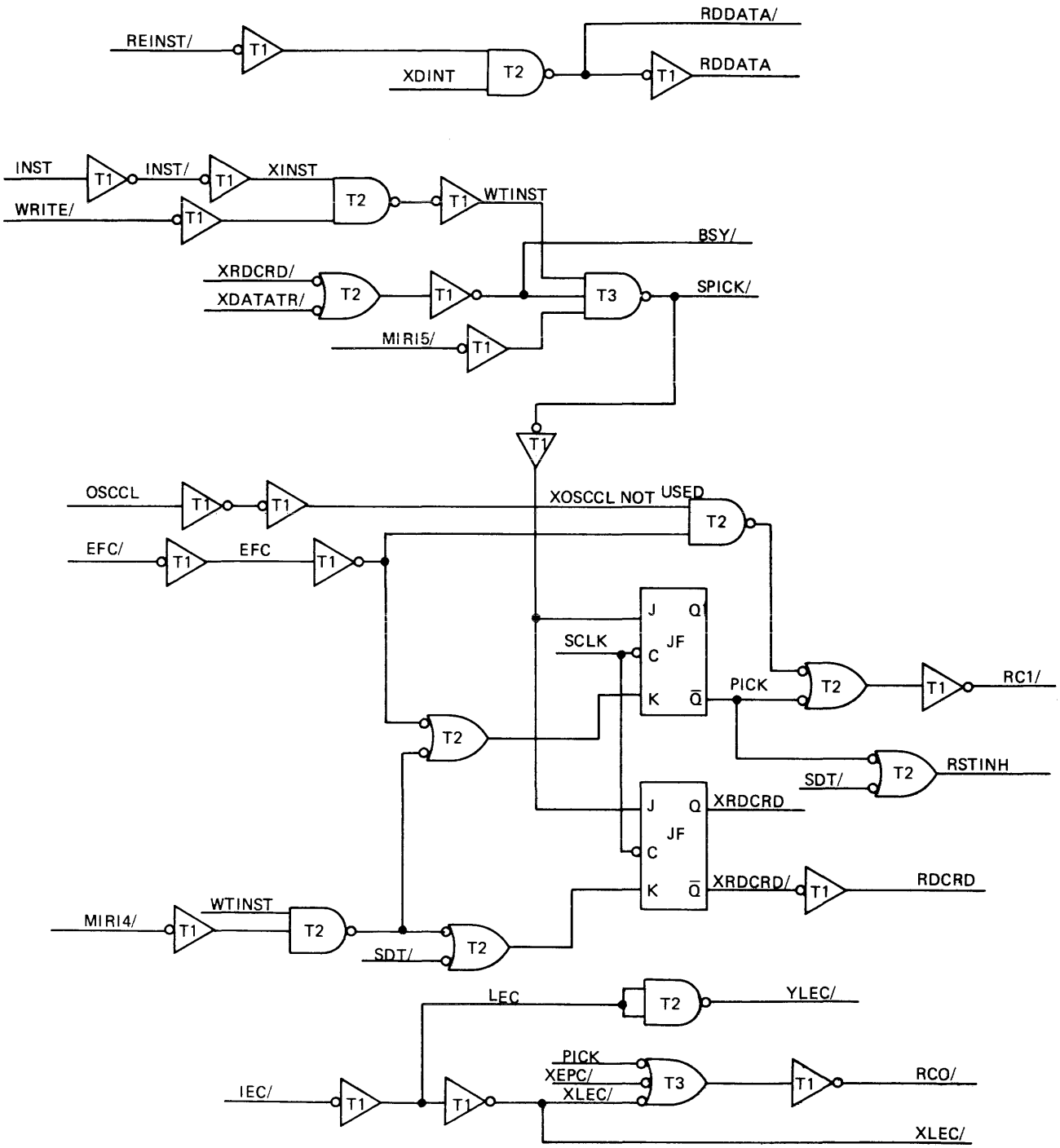


Fig. II-3

Functional Detail

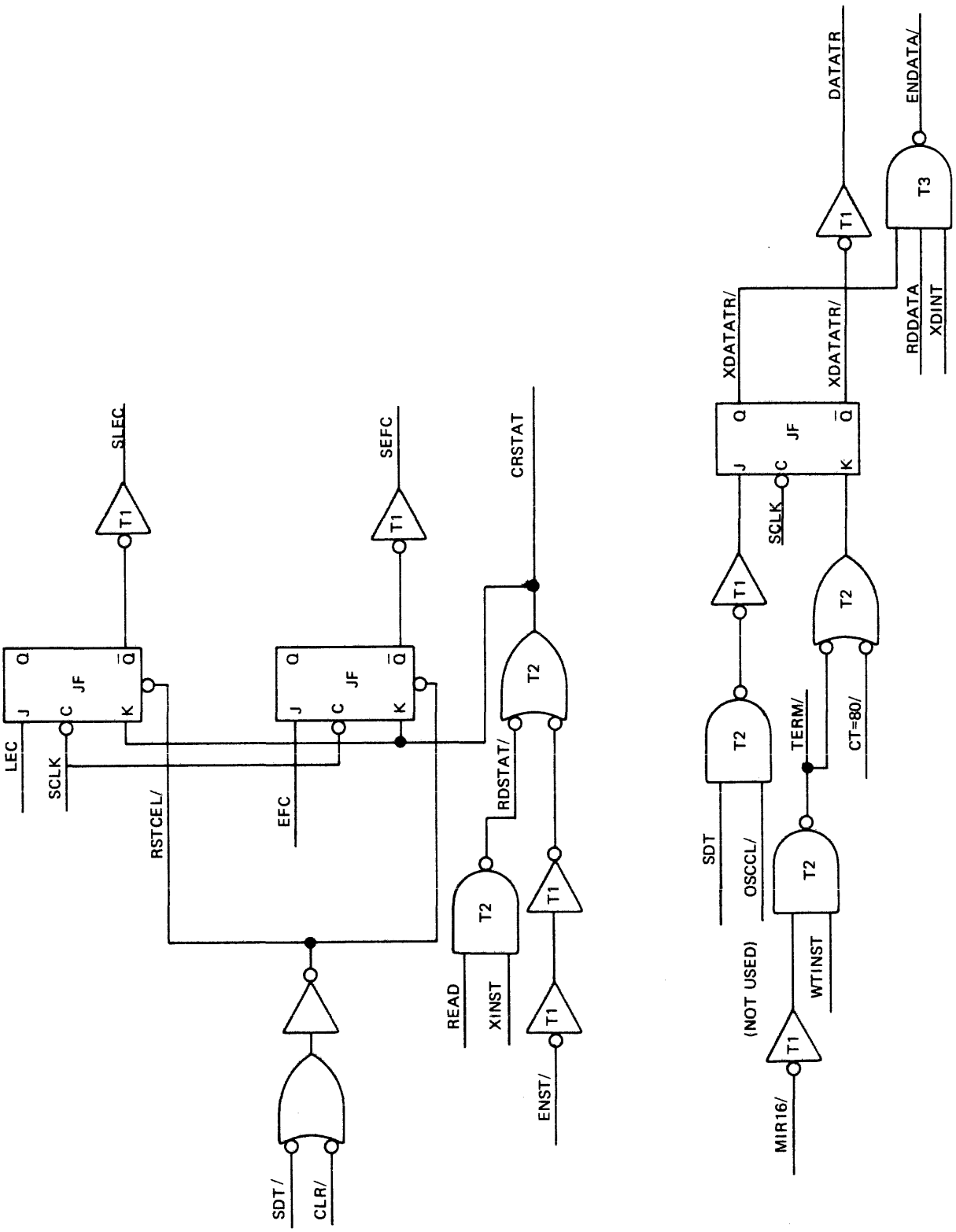


Fig. II-4

Functional Detail

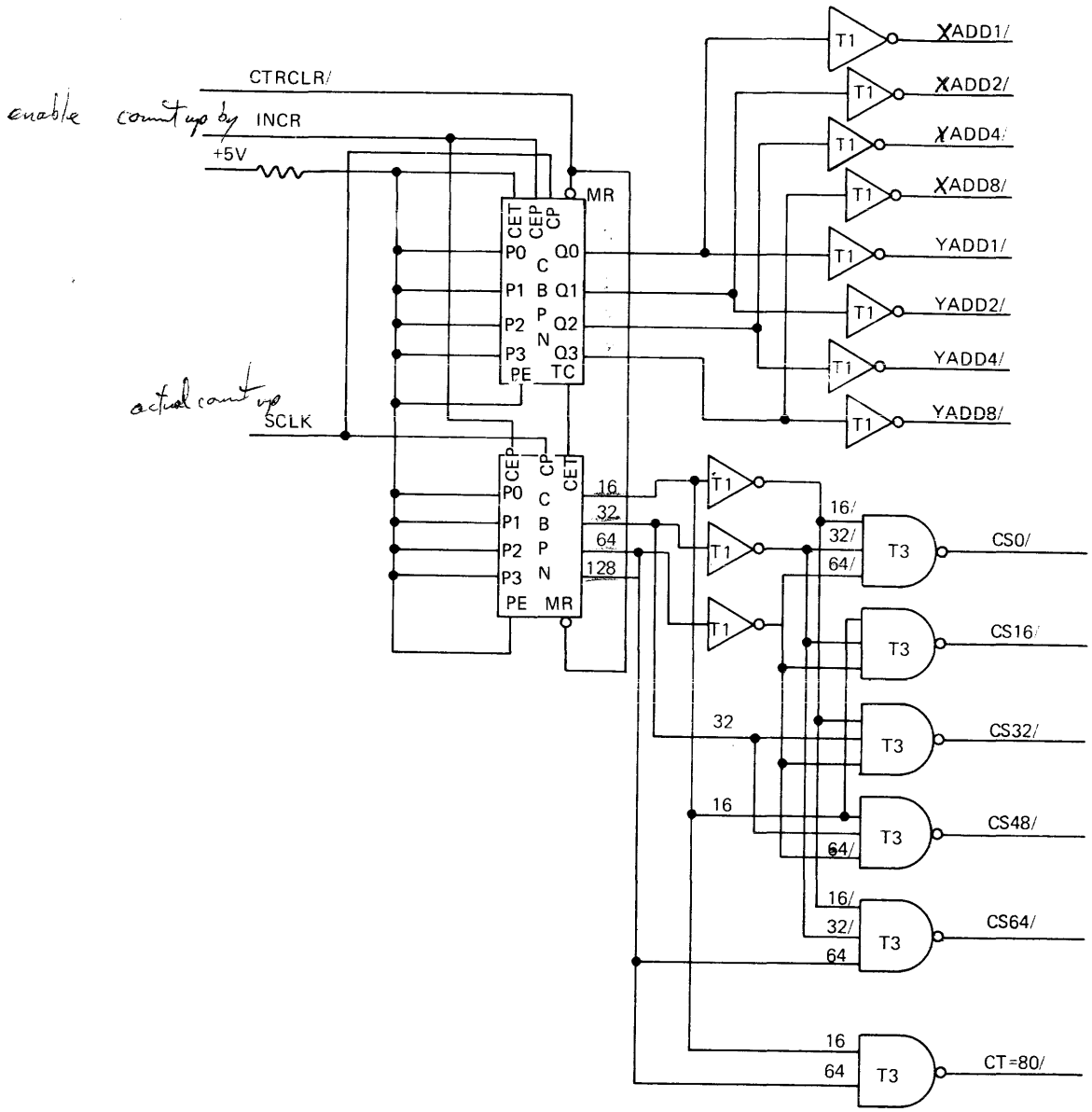


Fig. II-5

Functional Detail

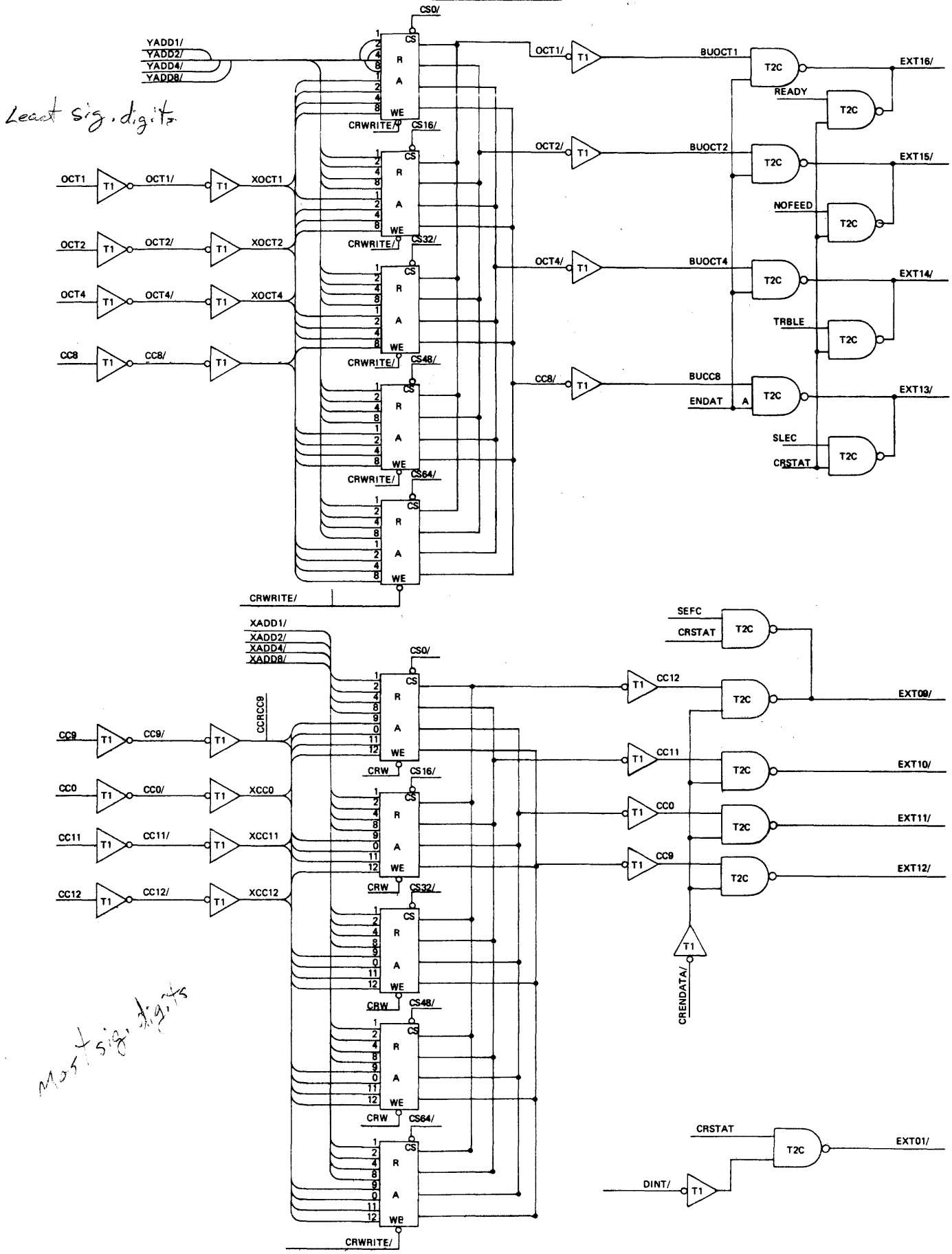


Fig. II-6

Functional Detail

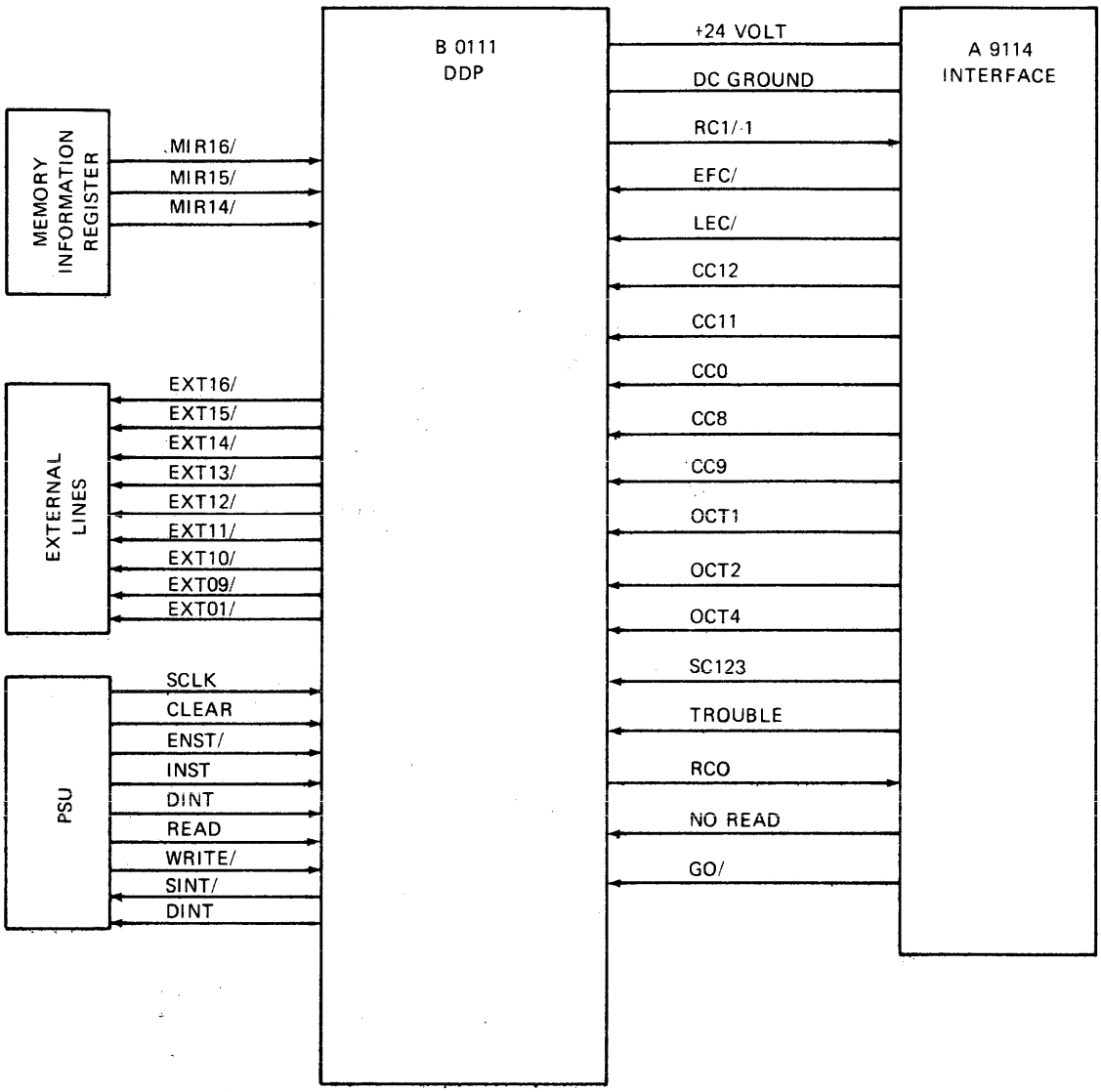


Fig. II-7 INTERFACE

B0111 CARD READER DDP WORD FORMATS

MIR / EXT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
CONTROL WORD	Ø	Ø	Ø.	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	DEV. CLR.	PICK OR READ CARD	TERM
DATA WORD	0	0	0	0	0	0	0	0	CC12	CC11	CC0	CC9	CC8	OCT4	OCT2	OCT1
STATUS WORD	DR	0	0	DA	DA	DA	DA	DA	0	0	0	SEFC	SLEC	TRBL	NO FEED	RDY

NOTE: 0 = NOT USED
Ø = DON'T CARE
DA IS GENERATED BY PSU

Fig. II-8 WORD FORMATS

Circuit Detail

INTRODUCTION

Section III contains the detailed description of the circuits used in the B0111 DDP. The subsections that follow explains the basic electronic functions of all the Transistor-Transistor Logic (TTL) circuits used in the B0111 DDP.

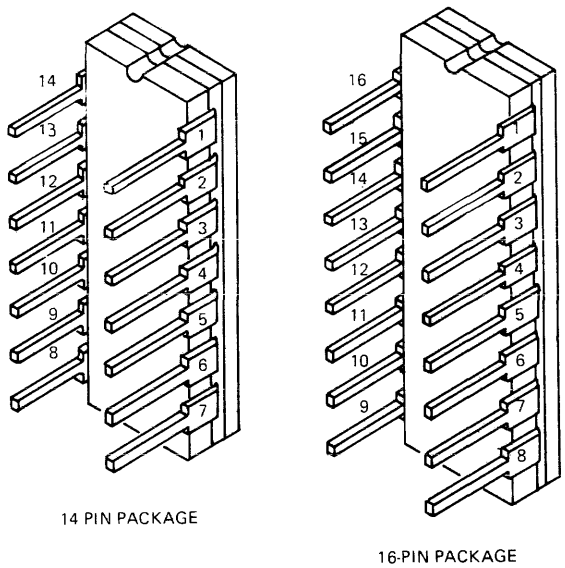


Fig. III-1 14 AND 16 PIN CHIPS

TRANSISTOR-TRANSISTOR LOGIC (TTL)

The TTL Electronic Componets known as chips are DUAL-IN-LINE packages with either 14, 16 or 24 pins; only the 14 and 16 pin chips are used in the B0111 DDP. See Figure III-1. The supply voltage for the chips is +5.0 volts. A Logical True Level (high level) is between +2.4 volts and +5.25 volts, and a Logical False Level (low level) is between 0 volts and 0.4 volts.

RA MEMORY CHIP

The RA Memory Chip, PT. NO. 1447 3672, provides full 640 bit capacity (16 word x 14 bit array), complete address decoding, and a wired-or-output capability which permits a variety of small-to-medium sized buffer memories to be constructed for memory expansion purposes. The RA Memory Chip pin configuration and block diagram is shown in Figure III-2.

In the B0111 DDP the RA Memory Chips are used for storing the data from the 80 column read from the card reader. The RA's are used in two groups of 5, to make two 80 word x 4 bit memory configuration. All address input lines, Data Input lines and the Write Enable lines are connected in parallel for each group of RA's. The Chip Select Input (CS) selects which RA of each group is to be selected. The Data Out Lines (DOn) represent the inversion of the Data Input Lines (DIn).

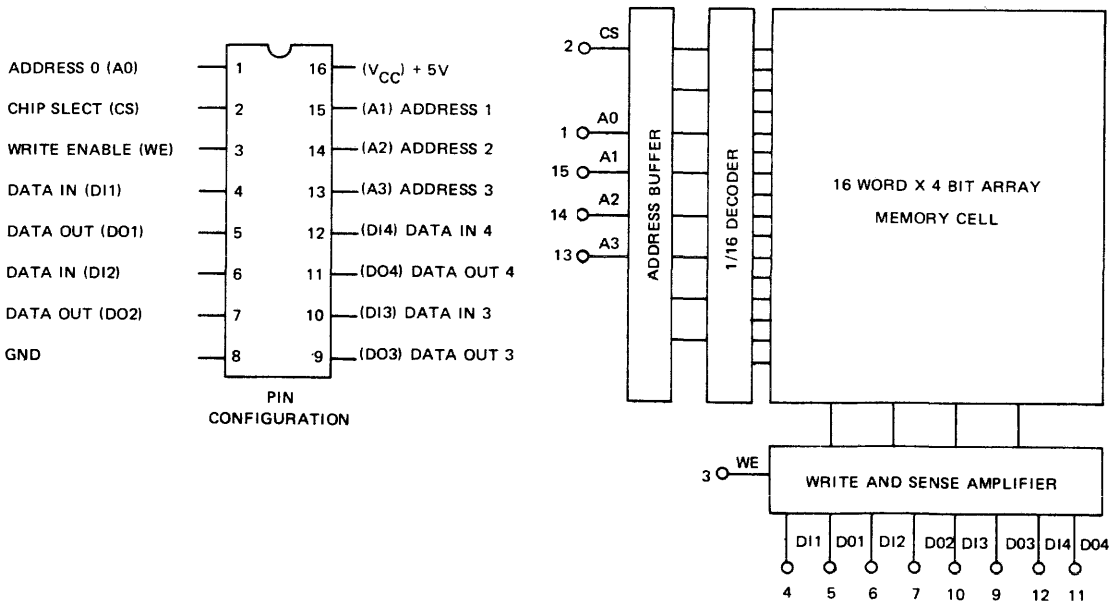
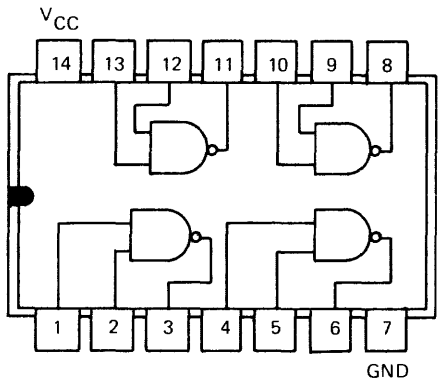


Fig. III-2 14473672 RA MEMORY CHIP PIN CONFIGURATION AND BLOCK DIAGRAM

Circuit Detail

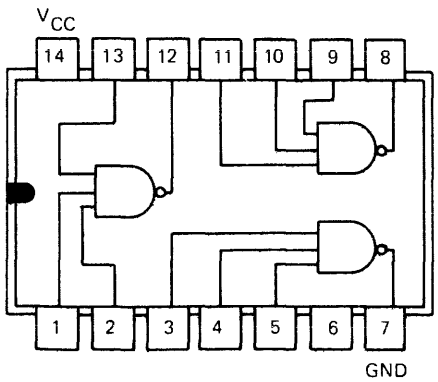
T2, T2C AND T3 NAND GATE AND NAND BUFFER

The various Nand Gates and Nand Buffer chips used in the B0111 DDP are shown in Figure III-3. The Nand Gates and Buffers are either 2 or 3 input gates. The T2C series Nand Gate chips are Open-Collector Output Gates and are used for wire or functions. Whenever a Nand Gate is used from this chip, the output of the gate will be connected for a wire or function. A general statement of operation for all Nand Gate circuits used in the B0111 DDP is that a high level output is produced by any low level input and a low level output is provided when all inputs are high. The only difference between the Nand Gate and the Nand Buffer is that the buffer has a higher drive capability.



T2 1447 3516
QUADRUPLE 2-INPUT POSITIVE
NAND GATES

T2C 1447 3581
QUADRUPLE 2-INPUT POSITIVE
NAND GATES
OPEN COLLECTOR



T3 1447 3540
TRIPLE 3-INPUT POSITIVE
NAND GATES

Fig. III-3 NAND GATES

T1 HEX INVERTER

The T1 Hex Inverter contains 6 inverters gates as shown in Figure III-4. The T1H is used when fast gating times are required. These gates are standard inverter whereby a high level output is produced by a low level input and a low level output is produced by a high level input.

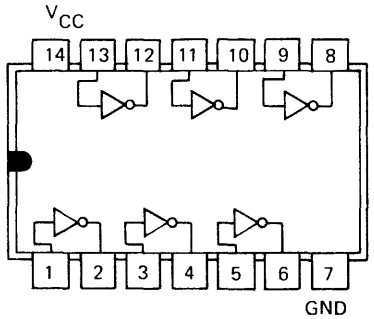


Fig. III-4 T1 14473532. T1H 14797971
HEX INVERTER

DF DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP

The DF Dual D Type Edge Triggered Flip-Flop Chip, PT. NO. 1447 3607, as shown in Figure III-9, contains 2 flip-flops. The functional block diagram for each FF is shown in Figure III-10. These FF have a direct clear and a preset inputs and complementary Q and Q outputs. Input information is transferred to the outputs on the positive edge of the clock pulse. A low level signal to the preset input sets Q to a logical 1 level. A low level signal to the clear input sets Q to a logical 0 level. The preset and clear inputs to each FF are independent of the clock.

JF DUAL J-K MASTER SLAVE FLIP-FLOP

The JF Dual J-K Master Slave FF Chip, PT. NO. 1447 3615, is shown in Figure III-7. These J-K FF are based on the master slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master.
2. Enter information from the J-K inputs to the master.
3. Disable J&K inputs.
4. Transfer information from master to slave.

A low level signal applied to the clear input sets Q output to a logical 0. The clear signal is independent of the clock. Refer to Figure III-8 for the functional logic of this chip.

Circuit Detail

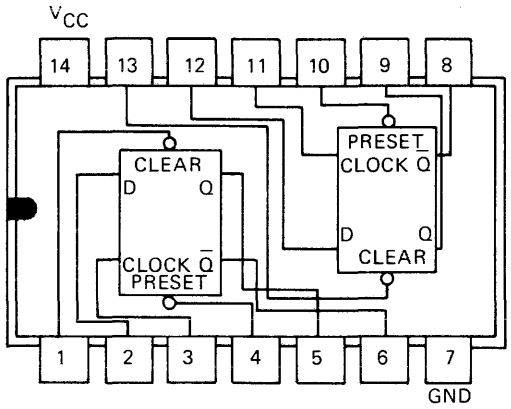


Fig. III-5 DF 14473607

TRUTH TABLE
(EACH FLIP-FLOP)

INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

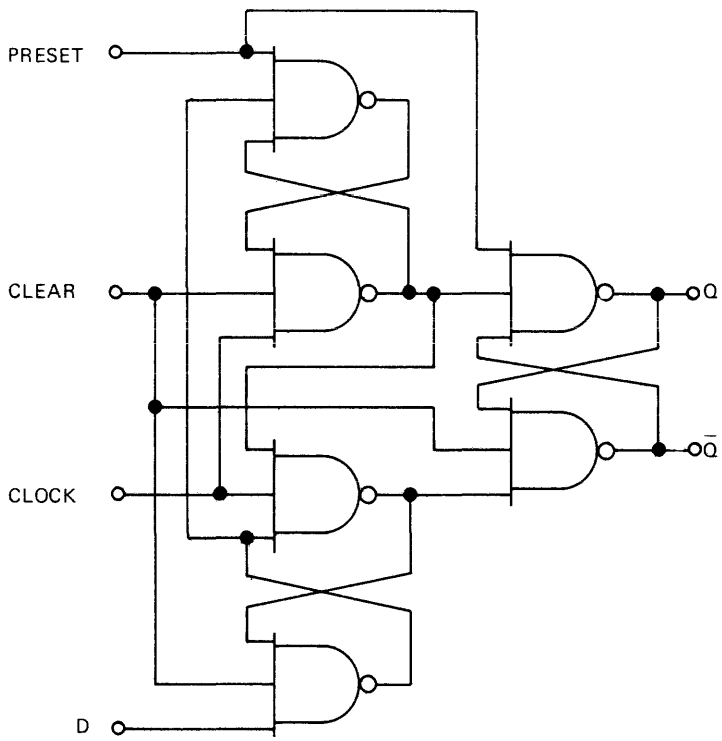


Fig. III-6 DF FUNCTIONAL LOGIC

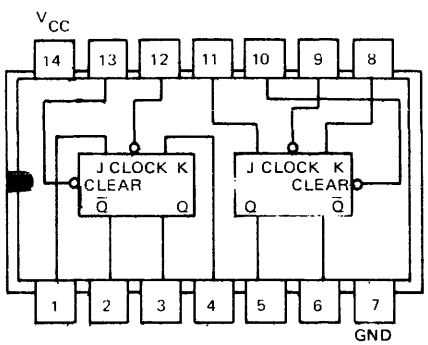
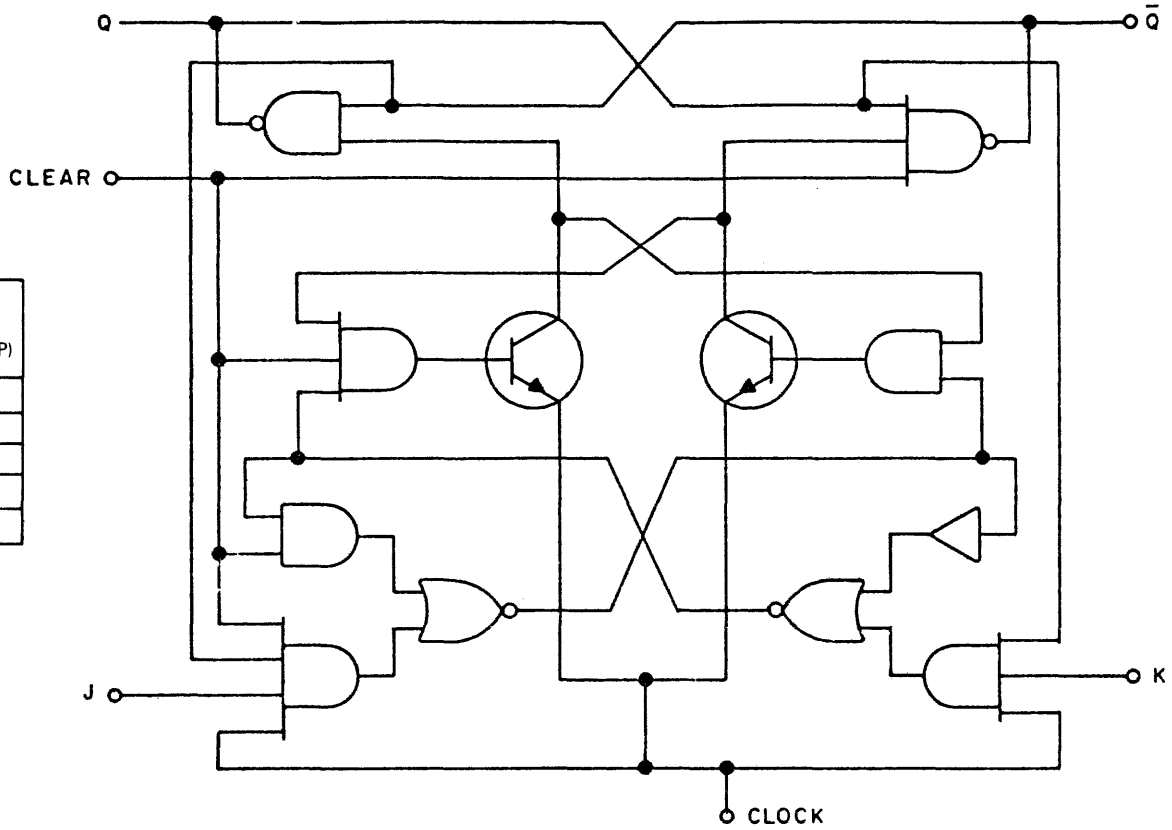


Fig. III-7 JF 14473615

Circuit Detail



TRUTH TABLE (EACH FLIP-FLOP)

J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Fig. III-8 JF FUNCTIONAL LOGIC

TRUTH TABLE

INPUT			OUTPUT
A1	A2	B	
1	1	1	INHIBIT
0	X	0	INHIBIT
X	0	0	INHIBIT
0	X	1	ONE SHOT
X	0	1	ONE SHOT
X	0	1	ONE SHOT
0	X	1	ONE SHOT
X	1	0	INHIBIT
1	X	0	INHIBIT
1	1	1	INHIBIT
1	1	1	INHIBIT
X	0	0	INHIBIT
0	X	0	INHIBIT

NOTE: X INDICATES THAT EITHER A LOGICAL 0 OR 1 MAY BE PRESENT.

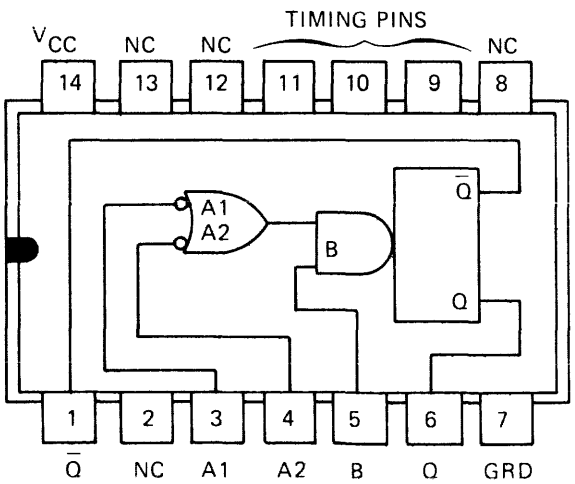


Fig. III-9 SS 14473706

Circuit Detail

SS MONOSTABLE MULTIVIBRATOR CHIP

The SS Monostable Multivibrator Chip, PT. NO. 1447 3706 and Truth Table are shown in Figure III-9. The SS features D-C triggering from positive or gated negative going inputs with an inhibit facility provided. Both positive and negative going output pulses are provided with a full fan-out of up to 10 normalized loads.

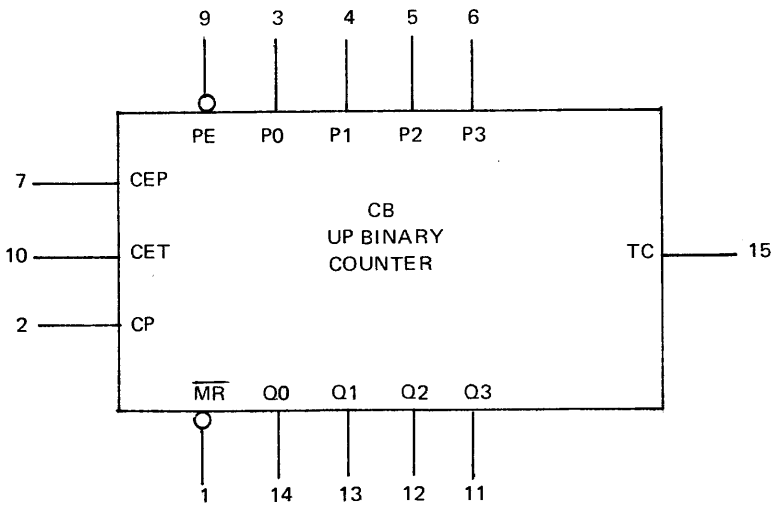
Negative Edge-Triggered Inputs at A1 and A2 allow the one-shot multivibrator to be triggered when either or both inputs are at a logical 0 level and the B input is at a logical 1 level. The B input is a positive Schmitt-Trigger Input, which allows jitter free triggering from inputs with slow transition times.

Whenever the B input is at a logical 1 level and both the A1 and A2 inputs are at a logical 1 level, the output is inhibited. The output is also inhibited whenever the B input is at a logical 0 level. Refer to Figure III-9. Once the one-shot multivibrator is triggered, the output is independent of further transitions of the input pulse and relies only on the External Timing Componet (RC Netword) added to the circuit. The output pulse length may be varied from 40 nanoseconds to 40 seconds by selection of the appropriate timing componets. With no external timing componets added to the circuit, an output pulse of 30 nanoseconds can be obtained.

CB UP BINARY COUNTER

The CB UP Binary Counter Chip, PT. NO. 1447 3771, is shown in Figure III-10. This chip is a Four Bit Synchronous Binary UP Counter with Synchronous Parallel Load Facility, overriding Asynchronous Master reset, and Carry Lookahead logig for high speed multistage operation. This counter is synchronous, with the counter output changing state after the low level to high level transition of the clock pulse. When conditions for counting are satisfied, a clock pulse will change the counter to the next state of the binary sequence. When the Parallel Enable (PE) input is a low level, the Parallel Inputs determine the next state of the counter synchronously with the clock pulse. Mode selection is accomplished as shown in Figure III-15. However, a restriction is placed on the manner of selection.

The transition of signal CEP or CET from a high level to a low level, or of signal PE from a low level to a high level, may only be done when signal CP is a high level. By using the Two Count Enable Inputs (CEP&CET) and Terminal Count (TC) output, multi-stage synchronous counting is obtained, with operating speeds equivalent to that of a single stage. When the synchronous master reset is active outputs Q0 through Q3 are unconditionally reset.



PIN NAMES

$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
Cp	Clock Active High Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
TC	Terminal Count Output

Fig. III-10 CB 14473771

Circuit Detail

MODE SELECTION

$\overline{PE}$	CE (COUNT ENABLE)	MODE
1	1	COUNT UP
1	0	NO CHANGE
0	X	PRESETTING

Where CE = CEP*CET 1 = High Voltage Level
0 = Low Voltage Level
X = Don't Care Condition

Fig. III-11 CB MODE SELECTION

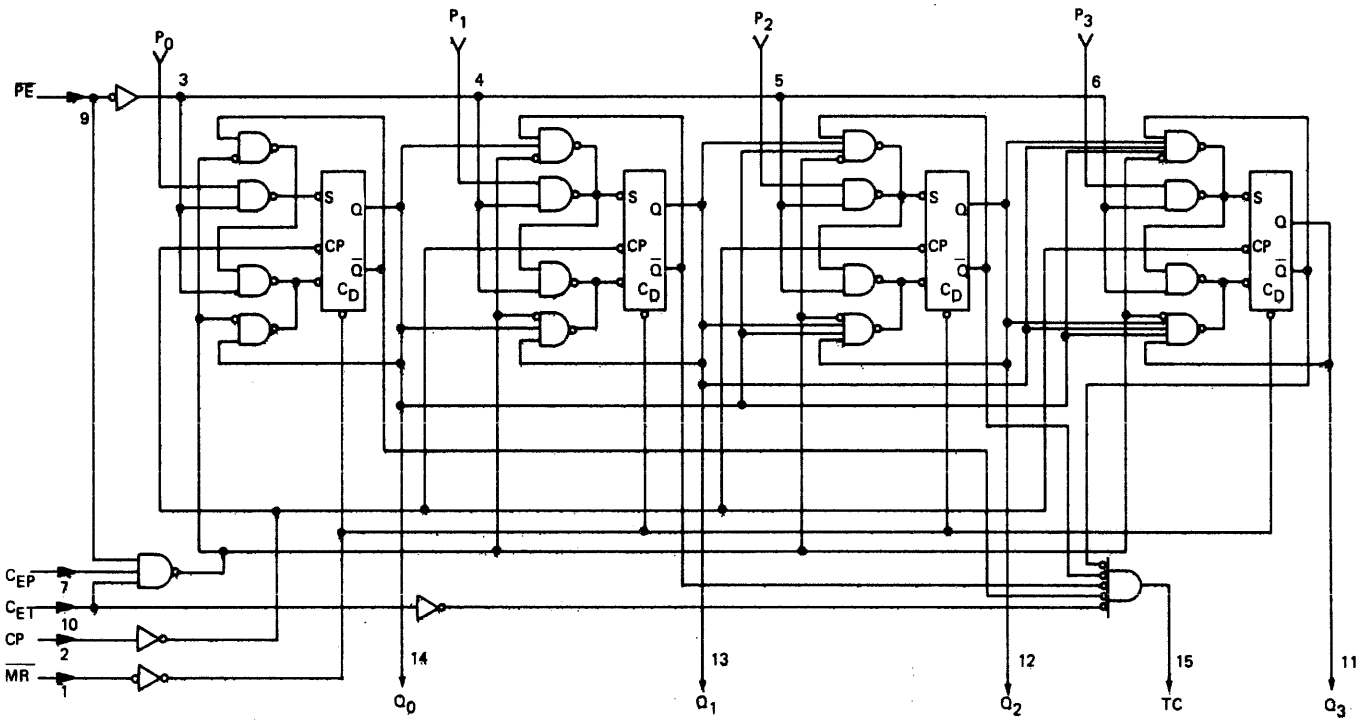
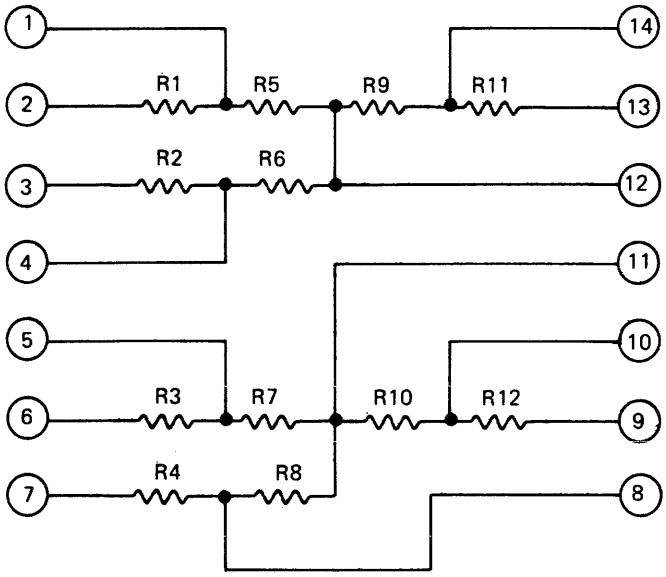


Fig. III-12 CB FUNCTIONAL LOGIC

Circuit Detail



RESISTOR NO.	RESISTANCE (25°C)	MAX. OPERATING POWER DISSIPATION (70°C)
R1, R2, R3 R4, R11, R12	402 Ω ±2%	125 MW
R5, R6, R7 R8, R9, R10	237 Ω ±2%	250 MW

Fig. III-13 RESISTOR MODULE 14475396

Maintenance Procedures

INTRODUCTION

The B0111 DDP is maintained by running the I/O Confidence Test and if a failure occurs, by running the CR 80 MTR Diagnostic.

The CR 80 MTR also includes a Test Deck that will be used when running the Confidence Test and MTR.

The CR 80 MTR performs the following tests:

1. Read and Check Sequential Data
2. Read and Check all Ones Data
3. Read and Check all Zeroes Data
4. Read and Check Checker Board Data

The following tests are for Signal Tracing:

1. Read all cards
2. Loop on a Device Write Operation

The CR 80 MTR will diagnose all failures in the B0111 DDP but will only indicate a failure in the A9114.

Tools required for CR 80 MTR:

1. MTR Meter
2. Extender Kit may be necessary if failure is not diagnostic

It should be noted that for proper diagnosis of the B0111 DDP and A9114, all previous Confidence Tests must be run.

Installation Procedures

INTRODUCTION

The B0111 80 column card reader DDP may be installed in any of the 7 interchangeable control locations. The locations are numbered DDP1 to DDP7. See Table I for installing the B0111 DDP.

TABLE I

DDP NO.	CARD FUNCTION	B/P LOCATION	B0111 80 Col. DDP	B0111 Cable Loc.
1	CONTROL	FW6	CR1- 1447 8747	J97
	DATA 9-16	FW3	CR2- 1447 5719	
	DATA 1-8	FW0	CR3- 1447 7509	
	SPECIAL	FV7	CR4- 1448 8223	
2	CONTROL	DW6	CR1- 1447 8747	J96
	DATA 9-16	DW3	CR2- 1447 5719	
	DATA 1-8	DW0	CR3- 1447 7509	
	SPECIAL	DV7	CR4- 1448 8223	
3	CONTROL	FV4	CR1- 1447 8747	J95
	DATA 9-16	FV1	CR2- 1447 5719	
	DATA 1-8	FU8	CR3- 1447 7509	
	SPECIAL	FU5	CR4- 1448 8223	
4	CONTROL	DV4	CR1- 1447 8747	J94
	DATA 9-16	DV1	CR2- 1447 5719	
	DATA 1-8	DU8	CR3- 1447 7509	
	SPECIAL	DU5	CR4- 1448 8223	
5	CONTROL	FU2	CR1- 1447 8747	J93
	DATA 9-16	FT9	CR2- 1447 5719	
	DATA 1-8	FT6	CR3- 1447 7509	
	SPECIAL	FT3	CR4- 1338 8223	
6	CONTROL	DU2	CR1- 1447 8747	J92
	DATA 9-16	DT9	CR2- 1447 5719	
	DATA 1-8	DT6	CR3- 1447 7509	
	SPECIAL	DT3	CR4- 1448 8223	
7	CONTROL	DT0	CR1- 1447 8747	J91
	DATA 9-16	DS7	CR2- 1447 5719	
	DATA 1-8	DS4	CR3- 1447 7509	
	SPECIAL	DS1	CR4- 1448 8223	

The A9114 needs Adapter Cable 1448 0354. This cable connects to the proper DDP port.