B 1700

DISK CARTRIDGE CONTROL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

INTRODUCTION AND OPERATION

FUNCTIONAL DETAIL

CIRCUIT DETAIL

ADJUSTMENTS

MAINTENANCE PROCEDURES

INSTALLATION PROCEDURES

RELIABILITY IMPROVEMENT NOTICES

OPTIONAL FEATURES

Printed in U.S. America 9-15-72

For Library Binder 114
Form 1058310

AA38664672

INDEX

Page No.

INTRODUCTION AND OPERATION – SECTION I

Control Operations 5
Control to Disk Cartridge Interface Levels 3
Disk Pack Control Mnemonic Glossary 6
General Operation 1
Initializing the Cartridge 3
Operations 1
Pause Operation 3
Read Burroughs Format 2
Read/Write Immediate 3
Read/Write Index 2
Standard Burroughs Format 1
Test Operation 3
Write Burroughs Format 2

FUNCTIONAL DETAIL – SECTION II

Basic Data Flow 5
Detailed Flow 21
General Buffer Control 13
I/O Descriptors 1
Test OP 1
Pause OP. 1
Read OP. 1
Write OP. 2

Page No.

Logic Description 16
Operation 6
Registers and Logic Description 4
Result Information 2
Simplified Flows 6

MAINTENANCE PROCEDURES – SECTION V

Confidence Routine 1
Hardware Testpoints 8
How to Load Cartridge Test 1
I/O Debug Routine 3
Index Sector Timing 15
Interface Testpoints 13
Test Procedures 6
Run Instructions 1

INSTALLATION PROCEDURES – SECTION VI

Electrical Installation 2
Logic Preparation 1
Peripheral to I/O Adapter Panel Cabling 1
Physical Installation 1

Printed in U. S. America 9-15-72

For Form 1058310

INTRODUCTION

The Disk Cartridge Control provides for the attachment of the B9480-2 Dual Disk Cartridge Drive to the B1700. It operates as a 1 x 2 or a 1 x 4 Exchange depending upon whether 1 or 2 dual drives are attached. See Figure I-1.

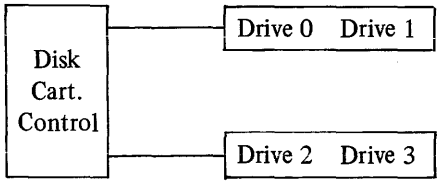


Fig. I-1 CONFIGURATION

GENERAL OPERATION

The Disk Cartridge Control provides for six basic read/write operations. In addition to a normal read or write, the control may perform a Read Index, Read Immediate, Write Index or Write Immediate. Most of the data transfers between control and disk will be via the normal read and write operation codes with the other codes used primarily for initialization of the disk.

The Disk Cartridge Control operates in the sector mode only using the Burroughs Standard format for the data. The disk sector or area to be read or written is specified by a fourteen bit (expandable) File Address. The addresses range binarily from 0 through 12991 for the cartridge used on this control. There are 32 sectors per track and two tracks per cylinder, one on the upper surface of the disk and one on the lower surface.

Each platter has a total of 203 cylinders of which 200 may be used with the other three used as spares. It is a function of the software to recognize which cylinders are spare and not address those cylinders.

STANDARD BURROUGHS FORMAT

The Control will read/write standard Burroughs format except when a read/write immediate or read/write index is commanded. Standard Burroughs format is shown in Figure I-2 along with the times associated with each portion for the 2200 BPI disk.

Sector — ADDRESS – 2 Bytes — Sector

PREAMBLE		Cylinder Track Sector	DATA	LPC	POSTAMBLE
33 Bytes	1 Byte	0-202 0-1 0-31	180 Bytes	1 Byte	25 Bytes
170.28 us	00011110				
	5.16 us	10.32 us	928.8 us	5.16 us	130.28 us

1250 us

Fig. I-2 STANDARD BURROUGHS FORMAT

OPERATIONS

The following paragraphs are intended to give a brief description of the six disk read/write operations along with the Test and Pause Operations. A detailed flow is provided in Section II of this manual along with a description of the various OP Codes and the Result Descriptor returned at the end of the operations.

WRITE BURROUGHS FORMAT

The Write Burroughs Format OP-Code is intended for normal storage of information on the disk. The Processor first must send the OP Code to the Control where it is stored in the OP Register. Having received the OP Code, the Control will advance to a status where it can receive the File Address from the processor. With the File Addressed stored, the processor then proceeds to send the data to the Control. Data is not immediately written onto disk but rather stored in one of the four 16 x 100 MOS Shift Registers. It should be noted that the data transfer occurs for two bytes (16 bits) at a time rather than the standard one byte per transfer which is used in most controls. If the processor reaches an end address ehreby it determines that all the data has been transferred, it will send a Terminate Command. The Terminate Command will allow the disk to proceed in the operation. If the Terminate Command is not received prior to filling a buffer the disk will proceed with the write operation and the processor must recognize this with the status count which is returned at every data transfer time during Phase B of the cycle.

Assuming one buffer is filled or a Terminate received, the control proceeds to receive the three Reference Address Bytes which it stores in an Address Memory. At this point several actions can occur. If a Terminate had not been received, the control will set a Service Request and proceed to send the Reference Address back to the processor when the processor has recognized the service request. This can be done as the disk has four of the MOS Shift Registers and only one is full at this time. While the Control allowed the service request to be generated and allows more data to be received, it also proceeds to start the writing of the previous buffer load onto disk.

Before the actual write occurs however, the Control determines by reading addresses from the disk that the cylinder address read from the disk compares with the cylinder address which has been placed in the File Address Register. If the cylinder address compares, the Control waits for sector coincidence at which time the write can begin. The write operation actually writes the address back onto the disk along with the sync pattern and the data. The Control also will generate a Longitudinal Parity Character to be written at the end of the 180 bytes of data.

The Longitudinal Parity Character (LPC) is an odd sum of the bits. If the cylinder address did not compare the Control would initiate a seek and terminate the operation by storing a Result Descriptor. It would be a function of the Processor to wait for the seek to complete itself and re-initiate the same write command in order to cause the data to be written. The Control will continue writing data on disk until a Terminate Command is received.

READ BURROUGHS FORMAT

The Read Burroughs Format OP-Code is intended for normal reading of information from the disk. Like the Write OP, the control first receives the OP Code and File Address from the Processor which are stored in their respective registers. Having received the File Address, the disk control will receive the three Reference Address Bytes and store them in Address Memory. It is at this point the actual disk operations begin with the Control determining in the same manner that the cylinder address in the File Address Register compares with the cylinder address being read from the disk. If they do not compare the operation is terminated and a seek is executed prior to storage of the Result Descriptor. If the cylinder addresses do compare then sector coincidence is sought at which time data may be read from disk and stored in the 16 x 100 MOS Shift Register. When one of the buffers (16 x 100 MOS Shift Registers) is full, a Service Request is generated by the control.

The Processor having recognized the service request, will transfer in the reference address bytes and begin reading the data from the buffer two bytes at a time. While the processor is emptying the buffer, the control is continuing the read and filling the other three MOS Shift Registers. While the buffer is being unloaded the processor may determine that it has received all the data required and send a Terminate Command, at which time the operation is completed and a result descriptor stored. If the buffer is emptied and a terminate is not received, the control will receive the Reference Address back from the Processor and store it in Address Memory. The control proceeds back to a point where it can determine if another buffer is full and generate a service request to empty the buffer. In any event the read will continue until a Terminate Command is received.

READ/WRITE INDEX

The Read and Write Index commands will perform in a similar manner as the Read/Write Burroughs format. Major differences are that the read/write does not occur for a specific sector but for the first sector following the index pulse received from the disk. Read/Write Index does imply a seek in that a cylinder address is given. The second major difference is on the data transfers. The read will read all data from the sector including preamble and store the information in Processor memory and the write must receive all data from the memory including preamble.

READ/WRITE IMMEDIATE

Read/Write Immediate performs similar to the Read/Write Index operations except that a seek is not implied. Reading or Writing will occur immediately following the first sector pulse received from the disk.

TEST OPERATION

The Test Operation is performed to test various status conditions of the disk which may normally be checked with the read/write operations also. The Test Operation in addition to checking the disk status such as not ready, seeking, position not settled to give a few examples also will return a control I/D to the Processor. The Processor can use the Control I/D to determine what type of control is on a specific channel such as Card Reader Control, Line Printer Control or Disk Control to mention a few.

PAUSE OPERATION

The Pause Operation is used primarily as a convenience to the Processor for the I/O operations. To give an example assume that the disk has just completed a read operation and has stored a Result Descriptor. Before that same OP Code can be performed again (software controlled and not a hardware restriction) the processor must be assurred that the data has been handled. The software can do this by handling the data and clearing the result descriptor which was stored. If the processor therefore finds the Result Descriptor not cleared, rather than issuing the Read Command again, it sends a pause command to the disk. After the disk has been in a pause for the period of time required, it sends a Result Descriptor to the processor. Due to the soft I/O Driver the Result Descriptor is not stored; however, the SR serves as a reminder to the Processor that it is waiting to perform an active operation.

INITIALIZING THE CARTRIDGE

A new cartridge does not have any sector addresses written on the disk. Before Standard Burroughs Format can be written on the disk, it must be initialized by having the sector addresses written on the cartridge.

The initialization procedure is performed by using the various Read/Write commands. The Read/Write Index commands have been specifically developed for the initialization procedure.

CONTROL TO DISK CARTRIDGE INTERFACE LEVELS (REFER TO FIGURE I-3)

Logical "1" is signified by a voltage level between 0 and 0.5 volts; logical "0" by a voltage level between +3 and +5 volts.

CYLINDER ADDRESS

Cylinder Address is transmitted on eight lines. These lines are strobed into an 8-bit address register by the Cylinder Seek Execute pulse to be internally decoded. Each cylinder is addressed by the following binary notation:

	Decimal Cylinder	Binary Address
	000	00 000 000
	001	00 000 001
	002	00 000 010
200 Cylinders		
	198	11 000 110
	199	11 000 111
3 Spares	200	11 001 000
	201	11 001 001
	202	11 001 010

CYLINDER SEEK EXECUTE

This line provides a pulse that strobes the address information into the 8-bit address register in the file unit. This pulse initiates the Cylinder Seek Action.

HEAD SELECT

This line selects the top disk surface when in the "true" state and the bottom disk surface when in the "false" state.

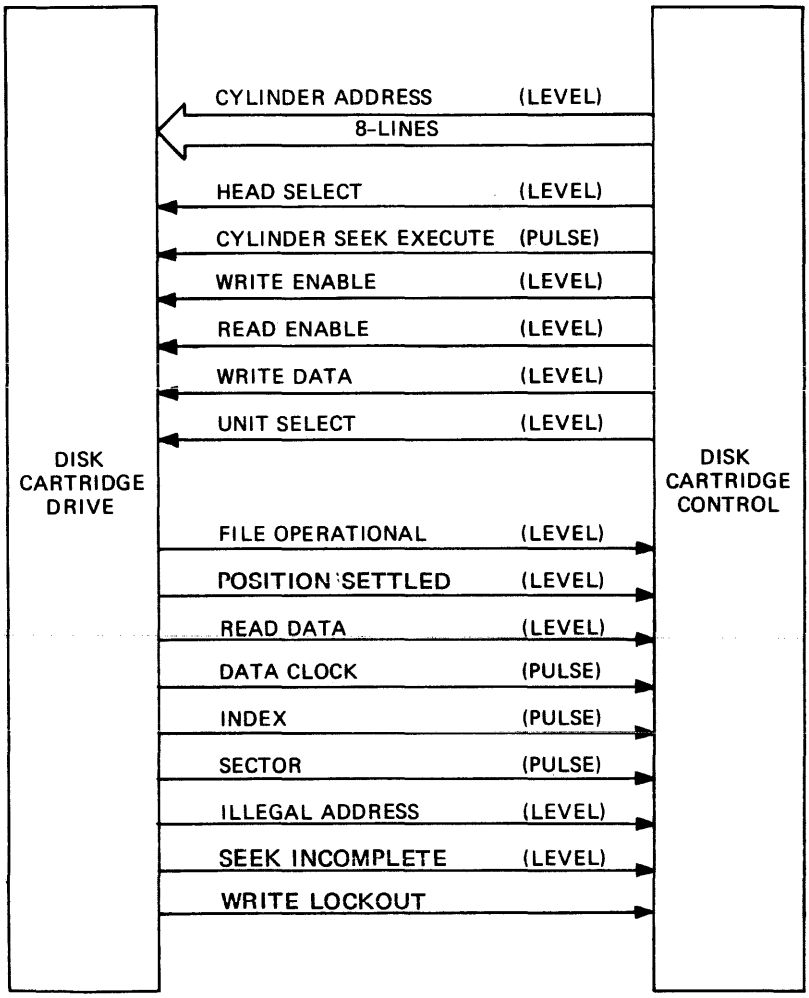


Fig. I-3 CONTROL TO DISK CARTRIDGE INTERFACE

WRITE DATA

The Write Data line carries the serial-by-bit NRZ write data from the control.

WRITE ENABLE

This line turns on the write amplifiers and edge erase. The line must go "false" after the write operation has been completed.

READ ENABLE

This line enables the read discriminator circuits. When the line is in the "true" state, the discriminator output will be placed on the Read Data and Clock lines.

WRITE LOCKOUT

This line indicates to the control that the Write Lockout plug has been pushed up in the Disk Cartridge, will disable writes.

FILE OPERATIONAL

This line indicates to the control that the Disk Drive is ready for operation. When the Drive has achieved operational speed, all interlocks and safety circuits are satisfied, and the line goes to a "true" level.

POSITION SETTLED

This line supplies a level to the control indicating that the heads are positioned and stabilized. The Drive is then ready to accept read or write commands.

READ DATA

The Read Data line transmits serial-bt-bit NRZ read data to the controller. The level of this line is maintained for the entire bit period.

CLOCK

This line transmits the 1.55 MHz write or read clock for the data. The clock output is used by the controller to strobe the data.

INDEX

The Index line supplies a pulse for the index reference point on the disk. The index pulse is used to synchronize Read/ Write Index Operations.

SECTOR

This line supplies a pulse at the beginning of each sector.

ILLEGAL ADDRESS

This line supplies a level when the cylinder address is greater than 202 during a Cylinder Seek Execute command. A valid address and a new Cylinder Seek Execute Pulse will reset the Illegal Address Line.

SEEK INCOMPLETE

This line supplies a true level 200 milliseconds after the Cylinder Seek Execute Pulse "if" The Seek Complete line indicates that an address has not been executed. This line will be reset by the next Seek Execute Pulse.

UNIT SELECT

Unit Select consists of one line. When in the "true" state the functions applicable to access, control, and data transmission of one drive is selected. When in the "false" state the functions applicable to access, control and data transmission of the other drive is selected.

CONTROL OPERATIONS

The Disk Cartridge Control responses to four commands: Read, Write, Test and Pause. These operations are detailed in Section II.

The control will transfer 16 bits of data at a time between the processor and the control. Data in the control is stored in four 100 x 16 buffers. These buffers may be loading while another buffer is unloading or vice versa. This allows the processor to communicate with the disk control at a rate up to 1.55 megabits per second.

PERIPHERAL OPERATION

The B9480-2 consists of two separate disk cartridge drives with a common power supply. The operation of the two drives are independent of each other. The Disk Cartridge Control may communicate with one drive at a time.

Storage (Full Track)	2,457 M Bytes
(180 Byte Format)	2,304 M Bytes
Average Access Time	90 M Sec
Disk Surfaces	2
Tracks Per Inch	100
Rotation Rate	1500
Number of Cylinders	200+3 Spare
Number of Tracks per Cylinder	2
Number of Sectors per Track	32
Sector Data Size	180 Bytes
Transfer Rate (Bits/sec)	1.55 MHz
Bits per Inch	2200

Fig. I-4 B9480-2 DISK DRIVE CHARACTERISTICS

DISK PACK CONTROL MNEMONIC GLOSSARY

ADDRF	ADDRESS FLIP-FLOP is set when a sync pattern is detected from the Disk Pack to indicate "Address Mode".
ADF	ADDRESS FLIP-FLOP is set when the Control is entering the operation required to determine the Disk-OP and find the correct address.
ASEL	A SELECT is true when the address unit portion selects either Unit 0 or Unit 1 which are both on Disk Pack Drive "A".
BITR=n	BIT RING is a counter which is used to count the number of bits accumulated in the Shift Register for a disk read operation or the number of bits shifted from the Shift Register to disk for the disk write operation.
BLKCTR	BLANK COUNTER is used during preamble time to insert a 32-64 usec delay after Read Enable has been sent to the Disk Pack.
BSEL	"B" SELECT is true when the unit portion of the Disk address is selecting either Unit 2 or Unit 3 which are located on Disk Pack Drive "B".
BUFCT	BUFFER COUNTER is a counter which indicates which of the four MOS Buffers in the Disk Control are to be either loaded or emptied depending upon the operation being performed.
BUFCT=n	BUFFER COUNTER EQUAL "N" where N=A, B, C or D.
BUFFUL	BUFFER FULL LEVEL is a level indicating all four buffers are full.
BUFFULF	BUFFER FULL FLIP-FLOP is a flip-flop set as a result of Buffer Full Level. (BUFFUL)
BUFRDY	BUFFER READY is a level indicating at least one of the four buffers contain information.
BUFSEMP	BUFFERS EMPTY is a level indicating all four of the MOS Buffers are empty.
CCERR	CYCLIC CHECK ERROR is true during a Disk Read operation if the Cyclic Check Character is not correct at the end of the sector being read.
CCR	CYCLIC CHECK REGISTER is a register used to accumulate a character which will be written at the end of each sector. The character written, referred to as cyclic check character, will be a longitudinal parity character. During a read operation the control will accumulate the character and compare it to the CCR character written on the disk. If the two characters do not compare, a parity error has occurred.

CHAF	CHANNEL ACTIVE FLIP-FLOP is set when a command is on the Exchange lines and the channel number corresponds to that of the Disk Pack Control indicating that the control is "active".
CHANHI	CHANNEL HIGH is true if the command at Command Active time (CA) is for the Disk Pack Control.
CLEAR	CLEAR when true will cause the Disk Pack Control to reset all registers, counters and miscellaneous flip-flops.
CLKENBn	CLOCK ENABLE BUFFER N comes true to enable the Shift Register Clock in order shift the MOS Buffer. N=one of the four buffers (A,B,C or D).
CLRCHAN	CLEAR CHANNEL is a flip-flop which sets to allow the Disk Pack Control to reset all flip-flops, counters and registers. CLRCHAN is a reset of a system CLEAR
CNTLMSK	CONTROL MASK is returend during a Test Service Request command from the processor indicating the Disk Control Service Request Flip-Flop is set. The Control Mask is a bit returned which corresponds with the channel number of the Disk Pack Control.
CNTOUT	COUNT OUT is set to enable the Out Counter to count the number of 16 bit words being read from one of the four MOS Buffers.
COMACT	COMMAND ACTIVE is a one clock period pulse received from the Processor when a command is placed on the Exchange. (Note: COMACT corresponds to CA in the I/O Sub-System Technical Manual description)
COMCODEL	COMMAND CODE LATCHES are the latches which are used to store the command received from the processor at command active time.
COMP1	COMPARE ONE is true when the number of buffers emptied is equal to the number of buffers that was loaded.
COMPF	COMPARE FLIP-FLOP is set when COMP1 (See above) is true and a terminate command has been received indicating the end of the operation.
COMP≠	COMPARE NOT EQUAL is true when the CCR accumulated on a Disk Read operation is not the correct bit configuration.
COMP.A COMP.B	COMPARE"A" and COMPARE "B" are two comparitors used to compare the address received from the processor to the address being read from the disk in order to indicate when the disk read/write can begin. They are also used to compare for a CCR error.
COMP=	COMPARE EQUAL is true when the address received from disk is equal to the address obtained from the Processor.
CONV	CONTROL VARIANT is true when the command from the Processor is one of the control variants commands.
COUNTL	COUNT LEVEL is true to enable the "In Counter" which counts the number of words being stored in one of the four MOS Buffers.
CTLNPH2	CTL "N" Phase Two is the output of the Shift Register Clock Logic which indicates the logic is in the initialized state. "N" is equal to one of the four buffers A,B,C or D.
CYL8-1F	CYLINDER FLIP-FLOPS is that part of the File Address Register which stores the cylinder portion of the address received from the Processor.
CYL=F=	CYLINDER EQUAL FLIP-FLOP is true when the cylinder address received from the disk is equal to the cylinder address contained in the cylinder portion of the File Address Register.
DATAF	DATA FLIP-FLOP is set when an address compare occurs which will take the control out of the "Address Mode" and place it in the "DATA MODE".
DPBUF	DUMP BUFFER is true to allow the shift of data from the buffer designated either placing data on the disk or sending information to the Processor.
DPCNTR	DUMP COUNTER counts the number of buffers which have been "dumped" (emptied).
DPEF	DISK PARITY ERROR FLIP-FLOP is set to report in the Result Descriptor that a parity error has occurred on the Disk Read operation.
DTOT1F DTOT2F	DISK TIME OUT FLIP-FLOPS are set as a result of the Index Pulse from the disk and are used to prevent the Control from "hanging up" if the correct disk address cannot be found in one to two revolutions of the disk after the seek has been completed.
DUMPN	DUMP BUFFER "N" where N=A,B,C or D and is used to address the buffer which is to be/being unloaded.
EXCHnn	EXCHANGE where nn=00-23 are the twenty-four exchange lines between the control and processor.
EXCEPT.	EXCEPTION is set to cause the exception bit in the Result Descriptor to be on if an error condition is detected or if the unit is not ready (See Result Descriptor).

EXITF	EXIT FLIP-FLOP is set to indicate the end of a disk operation either as a result of an error or all buffers empty and a terminate command received.
FAR+1	FILE ADDRESS REGISTER PLUS ONE is true to upcount the register by one at the end of an operation to keep the File Address in sync with the address being written on disk or read from disk.
FINJSTF	FINISH JUSTIFY FLIP-FLOP is set as a result of a terminate received while loading a buffer and will cause the data in the buffer to be right justified.
FINJSTN	FINISH JUSTIFY BUFFER "N" is true to cause a justification of the appropriate buffer as a result of (FINJSTF).
FL.OPL	FILE OPERATION LEVEL is true to indicate that the disk is ready for operation. This means that power is on, all interlocks are closed and a pack is inserted in the device.
FSFF	FIRST SECTOR FLIP-FLOP is used on a disk write operation to upcount only the sector portion of the file address in order to write the correct sector address on disk while writing the preamble.
HDSET	HEAD SETTLED is true when a continuous sector write causes the disk to cross from the top of the disk to the bottom and indicates only an address search is to occur and not a seek.
HEADF	HEAD FLIP-FLOP is a portion of the File Address Register and when reset indicates the address is on the top side of the disk and when reset indicates the address is on the bottom side of the disk.
HEADFF	HEAD FLIP-FLOP "F" is used in conjunction with HEADF in the incrementing of an address where a crossover from the bottom of a disk to the top (next track) is required. In this case the seek will only require a movement of one track and the control will wait for the seek to complete and continue the operation.
ILL.ADD	ILLEGAL ADDRESS is true when the cylinder address is greater than 202 during a seek execute to the disk. A valid address and a new seek execute will reset the Illegal Address line.
INCT+1	IN COUNTER PLUS ONE is used to count the characters (two characters at a time) that are stored in the MOS SHIFT BUFFER. These characters may be received either from the disk or the processor.
INXDF	INDEX FLIP-FLOP is set during a Write Immediate or Write Index command at SC=05. On the Write Index it is set when an Index Pulse and a Sector Pulse have been received from the disk. On the Write Immediate it is set with the first sector pulse from the disk. In either of the above cases it indicates that the write is to start.
INXF	INDEX FLIP-FLOP is set with the reception of an Index Pulse from the disk. The position settle signal must also be true.
INXP	INDEX PULSE is received from the disk once per revolution and indicates index time.
IN89	IN 89 is a count of the "IN COUNTER" and indicates 89 words (178) bytes have been loaded into the MOS Buffer located within the disk control.
IN100	IN 100 is a count of the "IN COUNTER" and indicates 100 words (200 Bytes) have been stored in the MOS Buffer located within the disk control.
IOS	INPUT/OUTPUT SEND is a level produced by the Control when the data transfer between the Processor and Control is from the Control to the Processor. I/O Send enables the necessary logic in the Distribution Card within the I/O Base or an I/O Base Extension.
IR0-7	INPUT REGISTER BITS ZERO THRU SEVEN is a portion of the register which holds information to be loaded into the MOS Buffer.
IR8-15	INPUT REGISTER BITS EIGHT THRU FIFTEEN is a portion of the register which holds information to be loaded into the MOS Buffer.
JPNA0	JUMPER UNIT A0 is wired true to indicate unit A0 is present.
JPNA1	JUMPER UNIT A1 is a wired true to indicate unit A1 is present.
JPNB0	JUMPER UNIT B0 is wired true to indicate Unit B0 is present.
JPNB1	JUMPER UNIT B1 is wired true to indicate Unit B1 is present.
JUSTCT+1	JUSTIFY COUNTER PLUS ONE is true to upcount the Justify Counter which is used to justify the data stored in the MOS Buffer.
JUST10	JUSTIFY COUNTER EQUAL TEN is true when the counter has reached a count of ten.
JUSTN	JUSTIFY BUFFER "N" is true to indicate the buffer specified by "N" is to be justified. "N" is equal to buffers A thru D.
JUSTF	JUSTIFY FLIP-FLOP is set to indicate that a buffer has been loaded and justification is necessary.
LDBUF	LOAD BUFFER is true if one of the four MOS Buffers is to be loaded and the function of LDBUF is to enable the clock to the buffer.

LDCNTR	LOAD COUNTER points at the buffer which is to be loaded.
LOADN	LOAD BUFFER "N" where "N" is equal to A thru D is the count of the LOAD COUNTER. This is the address of the buffer to be loaded.
LOADN-1	LOAD BUFFER MINUS ONE indicates that a justification of the buffer previously loaded (N-1) must occur.
MAEF	MEMORY ACCESS ERROR FLIP-FLOP is set if on a disk write operation the buffers are empty and a write is to occur or if on a read the buffers are full and more data is to be read.
MOS015	MOS BUFFER ZERO THRU FIFTEEN is the output of the MOS Buffers.
OPREG	OPERATION CODE REGISTER is that register where the disk operation (disk command) is stored.
OUTCTR+1	OUT COUNTER PLUS ONE is used to count the words (two bytes) that are read from the MOS Buffer.
OUTREG	OUTPUT REGISTER is that register which is used to temporarily store data that has been read from the MOS Buffer.
OUT89	OUTPUT COUNTER EQUAL 89 indicates the OUT COUNTER has counted 89 words (178 bytes) which have been read from the buffer.
OUT90	OUTPUT COUNTER EQUAL 90 indicates 90 words have been read from the buffer as counted by the Out Counter.
PAUSE	PAUSE indicates that a Pause operator has been received and stored in the OP Register.
POS.SET	POSITION SETTLE indicates that the heads are in position and not moving (seeking).
PRES	PRESENT is true if the unit selected by the disk address is present. The unit is determined present by a jumper which is wired (See JPNAn and JPNBn).
P1N	PHASE ONE BUFFER N is an output from the clock generator for the MOS Buffer where N is equal to the buffer selected.
P3N	PHASE THREE BUFFER N is an output from the clock generator for the MOS Buffer where N is equal to the buffer selected.
RABYTEN	REFERENCE ADDRESS BYTE N indicates in the flows that the reference address (3 bytes) is on the exchange and should be written into or read from Reference Address Byte Memory. N is equal to either one, two or three.
RDENF	READ ENABLE FLIP-FLOP is set to allow a disk read to occur. Either a read of address or data.
RDOP	READ OPERATION indicates the disk operation to be performed is a read; may be a standard read, read immediate or read index.
RD.IMM	READ IMMEDIATE is true to indicate that the operation is a Read Immediate.
RD.INX	READ INDEX is true to indicate that the operation is a Read Index.
READ	READ is true if the operation is the standard Burroughs format disk read operation.
READOUT	READ OUT is true if the contents of the MOS Buffer is to be read (transferred) to the Processor.
REFWR	REFERENCE WRITE is true to allow the Reference Address Bytes to be written into the special memory for the Reference Address.
REPSCOM	RESPONSE COMPLETE is true during the second portion of a Processor transfer command. (eg. Command Active and then Response Complete).
SC=RD	SEQUENCE COUNTER EQUAL READ is a sub-state of Sequence Count equal Three and is entered in order to read the disk after all the timeouts have been completed. SC=RD is for reading the addresses in order to determine when the actual read of data can occur or when a write can occur.
SC=RI	SEQUENCE COUNT READ INFORMATION is true at either Sequence Count Two or Four when actual data is to be read from the disk.
SC=WR	SEQUENCE COUNT EQUAL WRITE is true at Sequence Count Five for either a Write Immediate or Write Index in order to allow data to be written onto disk. The normal Burroughs Write occurs at SC=06.
SECF	SECTOR FLIP-FLOP is set as a result of receiving a Sector Pulse (SECP) from the disk.
SECP	SECTOR PULSE is received from the disk to indicate the beginning of a disk sector. (either 32 or 64 per revolution depending upon packing density of 2200 or 4400 bits per inch)
SECRCO	SECTOR CARRY OUT is true when adding one to the Sector portion of the File Address and the Sector Address is presently equal to 31. Completion of the add will result in a Sector address of 00.
SECR+1	SECTOR PLUS ONE is true to upcount only the sector portion of the File Address.

SECR-1	SECTOR MINUS ONE is true to downcount only the sector portion of the File Address. This operation is used on a disk write which must detect the address (sector) prior to the actual sector to be written.
SEC5-1F	SECTOR FLIP-FLOPS FIVE THROUGH ONE is the sector portion of the File Address Register. The five flip-flops give a total of thirty-two sector address combinations.
SEEK.EX	SEEK EXECUTE is a command sent to the disk to cause it to perform a seek operation. This is a result of the cylinder addressed not comparing to the address in the File Address Register.
SHFOKF	SHIFT "OK" FLIP-FLOP is set in order to count the IN COUNTER while storing data in the MOS Buffer.
SHIFTNI	SHIFT BUFFER "N" IN is produced to cause a shift of the MOS Buffer while storing data in the buffer or justifying the data in the buffer. "N" is equal to buffer A,B,C or D.
SHIFTNO	SHIFT BUFFER "N" OUT is produced to cause a shift of the MOS Buffer while reading data from the buffer. "N" is equal to A,B,C or D.
SKCTR+1	SEEK COUTNER PLUS ONE is enabled to cause a seek execute to be sent to the disk and delay the control logic in order to allow the seek in the disk to start as to not receive a false (erroneous) position settle signal.
SKSET	SEEK SET occurs when a FAR+1 causes the logic to address the next cylinder and thus a seek must occur. In this instance the control will wait for the seek to complete and continue the operation.
SKSTSNF	SEEK STATUS FLIP-FLOP is set to report a seek in progress by the disk. This occurs if the Cylinder Address in the File Address Register does not compare with the cylinder address read from disk. A seek is executed and reported in the Result Descriptor by using the SKSTSNF as the indicator.
SRTBLKF	START BLANK FLIP-FLOP is set to allow the Blank Counter to count during the VFO (Variable Frequency Osciliator) timeout. This occurs at the beginning of every operation prior to reading the addresses from the disk in order to determine address coincidence.
SRTDP	START DISK OPERATION is set to allow the Sequence Counter to advance from SC=00 in order to start the disk operation. Start Disk Operation occurs at Status Count equal to 10.
SRVRQF	SERVICE REQUEST FLIP-FLOP is set when the disk control needs service from the Processor. Service is needed for example if the disk is reading and a buffer becomes full or if writing and a buffer is emptied.
SRn	SHIFT REGISTER "N" is the register which shifts bit serial data to the disk or accumulates bit serial data from the disk. The Shift Register is divided into two sections, SR1 and SR2, each section containing eight bits or a total of sixteen flip-flops.
STC	STATUS COUNTER is the main counter or controlling logic within the Disk Pack Control. The value of the Status Counter is returned to the processor at Response Complete time of several operations in order to allow the processor to determine what point of the sequence the control is presently executing.
STRCNTF	START COUNT FLIP-FLOP is set to allow the OUT COUNTER to count the information being taken from the MOS Buffer.
SYNC	SYNC is true during SC=RD if a sync pattern (00011110) is decoded.
SYNCF	SYNC FLIP-FLOP is set as a result of SYNC (see above) being true indicating a sync pattern has been decoded.
TERM	TERMINATE is true if a Terminate Command is decoded on the Exchange Lines (see above) is for the Disk Control.
TEST	TEST is true if the operator in the OP Register is a Test OP rather than a read or write OP.
TESTR/	TESTER NOT is true if the Card Tester is not connected to the Disk Control cards.
TRKZROF	TRACK ZERO FLIP-FLOP is set if the disk address is illegal or if the seek is incomplete.
TESTCLR	TEST AND CLEAR is the Test and Clear command from the Processor as decoded on the Exchange lines.
TESTSRV	TEST SERVICE REQUEST is the Test Service Request command from the Processor as decoded on the Exchange lines.
TSTSTS	TEST STATUS is the Test Status command from the Processor as decoded on the Exhange Lines.
UNITnF	UNIT FLIP-FLOPS are the portion of the File Address Register which indicate which unit is selected. "N" is equal to unit zero or unit one.
WDCTR	WORD COUNTER is used in order to synchronize the control with the disk. Basically it allows the control to keep track of where the disk is within a sector such as address time, sync character time, data time or longitudinal parity time. The word counter may be set to a specific value, may be upcounted or downcounte for each 16 bits (1 word).
WRENABLE	WRITE ENABLE is a level to the Reference Address Memory within the control and must be false to allow the reference address to be written. The term REFWR will cause Write Enable to go false.

WRENF	WRITE ENABLE FLIP-FLOP is set to allow the Disk Write operation to occur.
WR.IMM	WRITE IMMEDIATE is true to indicate that the operation is a write immediate.
WR.INX	WRITE INDEX is true to indicate that the operation is a Write Index.
WRITE	WRITE is true if the operation decoded in the OP-REGISTER is the normal write operation Burroughs format.
WR.LKA	Level from Dual Drive A. When true indicates the selected unit (0 or 1) has the write lock out plug removed from the Disk Cartridge. (Write lockout)
WR.LKB	Level from Dual Drive B. When true indicates the selected unit (2 or 3) has the write lock out plug removed from the disk cartridge (Write lockout).
WRLKOT	WRITE LOCK OUT is set if the unit selected is write locked out. WRLKOT is set irregardless of the operation.
WRLKT	WRITE LOCKED OUT is set if the Write Lock Out Flip-Flop (WRLKOT See above) is set and the operation designated is a Write OP.
WROP	WRITE OPERATION is true if the operation decoded in the OP Register is one of the Write-OPS such as Write Burroughs Format, Write Index or Write Immediate.
WRTDSK	WRITE DISK is true at Sequence Count Five or Six in order to allow the contents of the Buffer to be emptied onto the disk.
XFERIN	TRANSFER IN is the Transfer In Command received form the Processor and decoded on the Exchange Lines at Command Active (CA) time.
XFERINL	TRANSFER IN LATCH is used to hold the Transfer In Command which has been decoded on the Exchange Lines at Command Active (CA) time.
XFROTA	TRANSFER OUT A is the Transfer Out A Command received from the Processor and decoded on the Exchange Lines at Command Active (CA) time.
XFROTAL	TRANSFER OUT A LATCH is used to hold (latch) the Transfer Out A Command which has been decoded on the Exchange Lines from the Processor at Command Active (CA) time.
1BUFUL	ONE BUFFER FULL indicates that one of the four MOS Buffers is full.
1USB	ONE MICRO SECOND BUS is the bus from the processor and occurs every one micro second and is true for one clock period.
100IN	ONE HUNDRED IN is true if 100 Input Buffer Clocks have occurred.
1024USB	ONE THOUSAND-TWENTY-FOUR MICRO SECOND BUS is a pulse which is true for one clock period at an interval of every 1024 micro seconds.
3BUFUL	THREE BUFFERS FULL indicates that three of the four MOS Buffers are full.
4USB	FOUR MICRO SECOND BUS is a pulse which is true for one clock period, occurring at a rate of every four micro seconds.

I/O DESCRIPTORS

The Disk Cartridge Control is capable of executing one of the four basic I/O Descriptors (also referred to as OP-CODES). Each of the descriptors are 24 bits in length. The following is a key for the variables within the descriptors:

1. nnn The three most significant bits of the OP are decoded for a read/write/pause or test.
2. M.V. The two bits in this position define the variables within a read or write op as to whether the operation is a Burroughs Format, Index or Immediate.
3. (.) The periods represent blank bits with no significance; these bits however should be set to zero.
4. UU The state of UU is to indicate which of the four units is selected in the case where two or more units are attached to the control.

TEST OP

100 . . . . . UU

Fig. II-1

Test the Control for the following conditions and return the Control Identification to the Processor during result status time.

1. Drive Ready
2. Drive Busy
3. Timeout of Seek Operation
4. Seek Complete Status
5. Seeking Status

PAUSE OP

100001 . . . . . .

Fig. II-2

The Disk Control will, on a Pause operation, pause for a period of approximately 8 milliseconds and at that time return a Service Request. Upon having the service request recognized the control will return a Result Descriptor with the operation complete bit set. (Refer to Section I of this manual for a further description of the Pause OP function). Pause, in the Disk Control is actually a variant of the TEST OP.

READ OP

000M.V . . . . . UU

Fig. II-3

The Read OP will cause data to be read from disk and stored into memory from the address specified by the File Address or according to the variants (immediate). The File Address implies that a seek must be performed and if indeed a seek must be executed the read operation is terminated and a Result Descriptor is returned. A complete segment is read by the disk in all cases however, the control need not transfer the complete sector of data to the Processor. The following is a description of the Read OP variants:

M.V=00 Read Burroughs Format which means only 180 bytes of information is read and stored in memory.

01 Undefined

10 Read Index; causes a read to occur immediately following the sector pulse which follows the index pulse for the cylinder in the File Address.

11 Read Immediate; causes a read to occur immediately following the next sector pulse. A seek is not performed.

WRITE OP

010M.V . . . . . UU

Fig. II-4

The Write OP will cause data to be written onto disk at the specified File Address or according to the variants. Data is read from memory and written to the disk. A complete sector must be written by the control therefore, if a terminate is received prior to completion of a sector, the control supplies zero bits to fill the sector. The following is a description of the variants for the WRITE OP:

M.V=00 Write Burroughs Format of 180 bytes to disk.

01 Undefined

10 Write Index; write immediately following the sector pulse which follows the index pulse. All data including preamble must come from memory. A seek operation is implied.

11 Write Immediate; write immediately following the next sector pulse. All data including preamble must come from memory. A seek is not implied.

RESULT INFORMATION

Upon completion of the specified operation, a 24 bit Result Descriptor otherwise referred to as Result Status Word, is generated by the Control and available for the Processor. The Processor must generate the sequence to transfer the Result Descriptor to one of the Processor's registers for storage in memory. Chart II-1 shows the twenty-four bits of the Result Descriptor along with the position on the Exchange that the bits will occupy at the transfer time. The final column is a description of each bit and shows which of the basic four OP CODES will cause the bit to be sent.

Functional Detail

BIT	BUS POSITION	DESCRIPTION
1	7	Operation Complete
2	6	Esception
3	5	File Not Operational (R+W+T+P)*
4	4	Disk Read Error (R)
5	3	Reserved
6	2	Reserved
7	1	Write Locked Out (W+T)
8	0	Reserved
9	7	Reserved
10		
10	6	Unit Present
11	5	Reserved
12	4	Timeout, Illegal Address, Seek Incomplete
13	3	Position Settled (T)
14	2	Reserved
15	1	Seeking (T)
16	0	Reserved
17	7	Operation Complete
18	6	Control I/D Bit = 0
19	5	Control I/D Bit = 0
20	4	Control I/D Bit = 1 (T)
21	3	Control I/D Bit = 1 (T)
22	2	Control I/D Bit = 1 (T)
23	11	Control I/D Bit = 0
24	0	Reserved

* P=PAUSE OP
R=READ OP
T=TEST OP
W=WRITE OP

RESULT DESCRIPTOR

DISK CARTRIDGE CONTROL – REGISTERS AND LOGIC DESCRIPTION

The following is a description of the various registers, buffers and major sections of logic contained within the Disk Cartridge Control. The portions of logic defined below are listed in alphabetical order.

ADDRESS MEMORY

Address Memory is used in the Control to store the Reference Address, Bytes 1, 2 and 3 until such time as the Reference Address is to be sent back to the Processor.

CTL & MOS CLOCK LOGIC

The Disk Cartridge Control contains four distinct sets of CTL & MOS CLOCK LOGIC which corresponds to the four MOS Buffers contained within the control. The clock logic is used to read/write/shift data into the MOS Buffers and produce the required timing for performing these functions.

DUMP SELECT

The Dump Select Logic is used to select which of the MOS Buffers is to be unloaded at a particular time. Dump Select logic will select either Buffer A, B, C or D. The Dump Select Logic will automatically select Buffer A if the Control is cleared.

FILE ADDRESS REGISTER (FAR)

The File Address Register receives and stores the address on disk where the read/write operation is to occur. FAR is upcounted at each sector and keeps in sync with the sector which is actively being read/written. The FAR Register consists of nine Cylinder Flip-Flops, one Head Flip-Flop and five Sector Flip-Flops. The FAR+1 input is to the Sector Flip-Flop portion of the register.

IN COUNTER

The In Counter is used to record the number of "words" stored in a particular buffer. A word is defined as two bytes or 16 bits in this control. The In Counter can therefore be used to notify when the data must be right justified (terminate or buffer full) and can notify the control when another buffer must be selected.

INPUT LATCH

The Input Latches (16) are the direct input to the MOS Buffers. It is the function of these latches to hold the data while the clock generator is producing the required timing to write the data in the buffer selected.

JUSTIFY COUNTER

The Justify Counter is used to justify the data in a buffer whenever a Terminate Command has not been received. The Justify Counter will notify the Control when it reaches a count of ten, indicating that data has been right justified by ten words and is ready for output either to the Processor or Disk depending upon the operation being performed by the Control at the time.

LOAD SELECT

The Load Select Logic is used to address the buffer that is to be loaded. A Channel Clear will set the Load Select Logic to address Buffer A and each time the IN COUNTER reaches a count of 90 words, the Load Select will be upcounted to select the next buffer.

MOS SHIFT REGISTER

The Disk Cartridge Control contains four MOS Shift Registers sometimes referred to as MOS Buffers. The MOS Shift Registers are 16 x 100 buffers and are used to store data which has been read from disk or store data from the processor prior to writing disk.

OP REGISTER

The OP Register is used to store the Disk OP for the operation that is to occur such as Read, Write, Pause or Test.

OUT COUNTER

The Out Counter is used to count the words which have been read (dumped) from a MOS Shift Register. The Out Counter when it reaches a Count of 90 will cause the Buffer Dump Select Logic to address the next buffer.

OUTPUT LATCHES

The Output Latches (16) receive the output of the MOS Shift Register and store the word prior to the data being sent to the Processor or in the case of a disk write it stores the data prior to transfer to the Shift Register (SRn).

SEQUENCE COUNTER (SC=n)

The Sequence Counter is used during the actual read/write portion of a disk descriptor to sequence the read/write operation. The Sequence Counter is used in conjunction with the Status Counter (STC).

SHIFT REGISTER 1 and SHIFT REGISTER 2 (SRn)

Each of these shift registers are eight bits in length and combine to form a single 16 bit shift register. The 16 bit shift register is used to shift bit serial data to the disk in the case of a write operation and used on a read to accumulate the bit serial data read from disk.

STATUS COUNTER (STC)

The Status Counter is used to sequence the major events of an operation within the Control. During Phase B of each cycle, the status count is returned to the Processor and used by the soft I/O Driver to enable it to keep in sync with the events occurring within the control.

BASIC DATA FLOW

The paragraphs on basic data flow are intended to show a general flow of the data through the disk cartridge control for the read and write operations. Along with the descriptions are diagrams which should be read from left to right.

WRITE (Refer to Figure II-5)

The processor on a disk write operation will transfer the data two bytes at a time (16 bits) over the exchange with a series of Transfer Out A Commands. Data is placed on exchange lines 15-0 and is present only for a brief period of time (250 nsec) during phase A of the cycle. The data therefore must be temporarily stored in a series of latches prior to input into the MOS Shift Registers.

The data having been stored in the Input Latches, a sequence will be triggered to transfer the data from the latches to the buffer and shift the contents of the buffer to the right (output). Each word (two bytes) is received and transferred in this manner until all data has been received for the sector to be written at which time the MOS Shift Register must be right justified as it is a 16 x 100 buffer and a sector consists of only 90 words (180 bytes). At the appropriate time the data is read from the buffer and stored in the Output Latches from where it will be transferred to the disk Shift Register (SR).

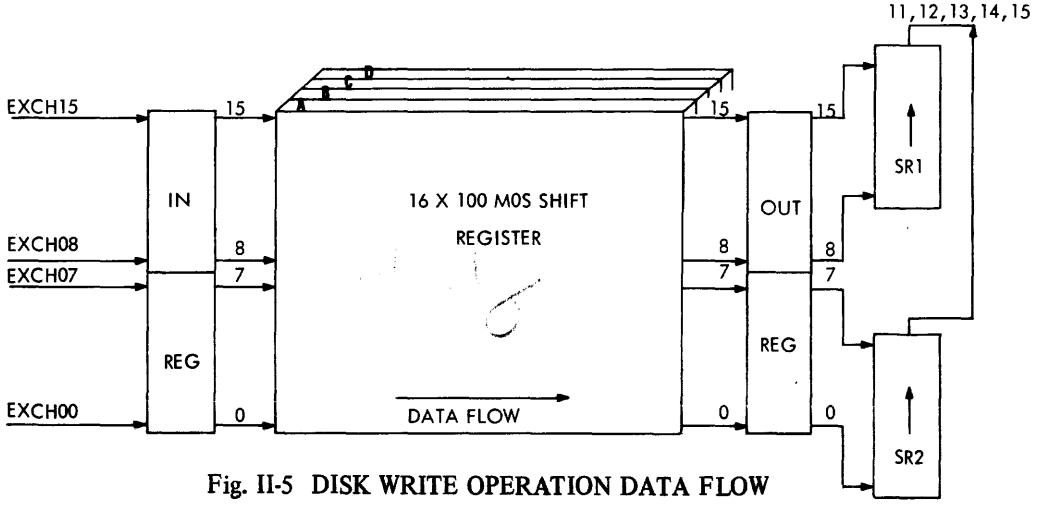


Fig. II-5 DISK WRITE OPERATION DATA FLOW

Data is read and transferred to SR with a parallel transfer of 16 bits. The data which was on Exchange Lines 15-8 will be placed in SR1 and the data which was on Exchange Lines 7-0 will be placed in SR2. Data from that point will be shifted bit serially from SR1 and then SR2 to the disk where it can be written in a bit serial fashion.

READ (Refer to Figure II-6)

The Disk Cartridge Control on the Disk Read operation must accumulate the bit serial data from the disk in a shift register. The register used to accumulate the bit serial data is Shift Register 1 and Shift Register 2 which combine to form one sixteen bit shift register or in the case of a disk read, bit accumulator. The disk write operation, as you will recall, wrote first bit 15 then 14 and so on down the line onto the disk.

The read operation will therefore first read bit 15 and place the bit read in SR1. When bit 14 is read, bit 15 will be shifted up and this will continue until eight bits are contained in SR1 at which time the remaining eight bits will be read and shifted into SR2 in a like manner. The Control having read 16 bits will then transfer the data to the input latches of the 16 x 100 MOS Shift Register. Data from that point will be shifted parallel into the MOS Shift Register and as subsequent words are read from disk the contents of the MOS Shift Register will be right justified. When the buffer becomes full with the 90 words, data will be right justified by 10 more positions and finally the first word read will appear in the Output Latches. Upon receiving a Transfer In command from the Processor, data will be read from the Output Latches and transferred to the Processor as 16 bit parallel data via the Exchange Lines.

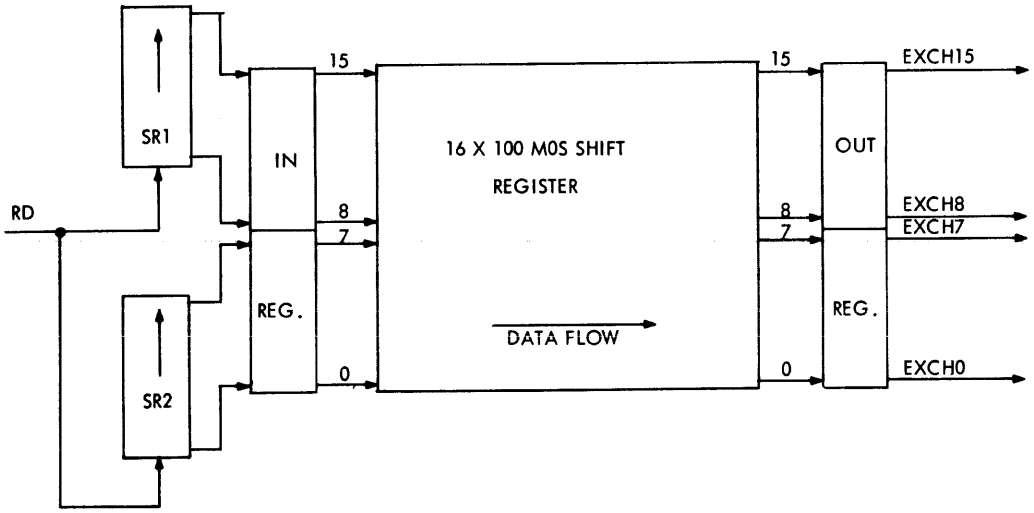


Fig. II-6 DISK READ OPERATION DATA FLOW

SIMPLIFIED FLOWS

Each of the four Disk Cartridge Control OP-CODES have a particular sequence of events that occur. These events are controlled by both a Status Counter (STC) and a Sequence Counter (SC). Figures II-7 through II-11 are used to illustrate the flow of events for each of the basic OP-CODES and variants along with error conditions which can alter the normal sequence. Figure II-7 is used to illustrate these error conditions such as File In-Operative, Illegal Address, Seek Incomplete or Write Lockout. Note that all these conditions are not actually errors but rather conditions that will prevent a read or write from occurring. The following paragraphs give a brief description of the actions which occur at each STC and SC.

STC00 Upcount the Status Counter and clear the OP Register
STC01 Receive Byte 1 of OP
STC02 Receive Byte 2 of OP
STC03 Receive Byte 3 of OP
STC04 Receive Byte 1 of File Address (Not Used)
STC05 Receive Byte 2 of File Address (Cylinder Address bits 9-3)
STC06 Receive Byte 3 of File Address (Cylinder Address bits 2-1, Head Address and Sector Address 5-1)

STC07 Receive Reference Address Byte 1 and store in Address Memory.
STC08 Receive Reference Address Byte 2 and store in Address Memory.
STC09 Receive Reference Address Byte 3 and store in Address Memory.
STC10 Perform operation and make various exit decisions based upon OP-CODE. Set Service Request when required.
STC11 Transfer Reference Address Byte 1 to Processor
STC12 Transfer Reference Address Byte 2 to Processor
STC13 Transfer Reference Address Byte 3 to Processor
STC14 Load MOS Buffer for Disk Write Operation.
STC15 Send data to Processor for Disk Read Operation.
STC16 If Read-OP send last word to Processor or if Write-OP load last word from Processor into MOS Buffer. Exit according to OP-CODE and whether a Terminate has been received.
STC17 Not used
STC18 Send Reference Address Byte 1 to Processor
STC19 Send Reference Address Byte 2 to Processor
STC20 Send Reference Address Byte 3 to Processor
STC21 Send Result Descriptor Byte 1 to Processor
STC22 Send Result Descriptor Byte 2 to Processor
STC23 Send Result Descriptor Byte 3 to Processor and clear control.
SC=00 Initialize miscellaneous flip-flops and exit to Sequence Count One.
SC=01 Seek Execute if Write Index, Read Index, Illegal Address or previous seek incomplete and new operation.

Decrement sector address if write in order to find sector coincidence prior to actual sector to be written.

Make decision for exit to SC=03, SC=05 or SC=00.
SC=02 Read Disk and load buffers for Read Index or Read Immediate.
SC=03 Determine cylinder equal, sector coincidence, pause for Pause-OP, ~~and VFO~~ timeout.
SC=04 Read Disk and load buffers for Read Burrough's Format.
SC=05 Write 1 sector for Write Index or Write Immediate.
SC=06 Write disk for Write Burrough's Format.

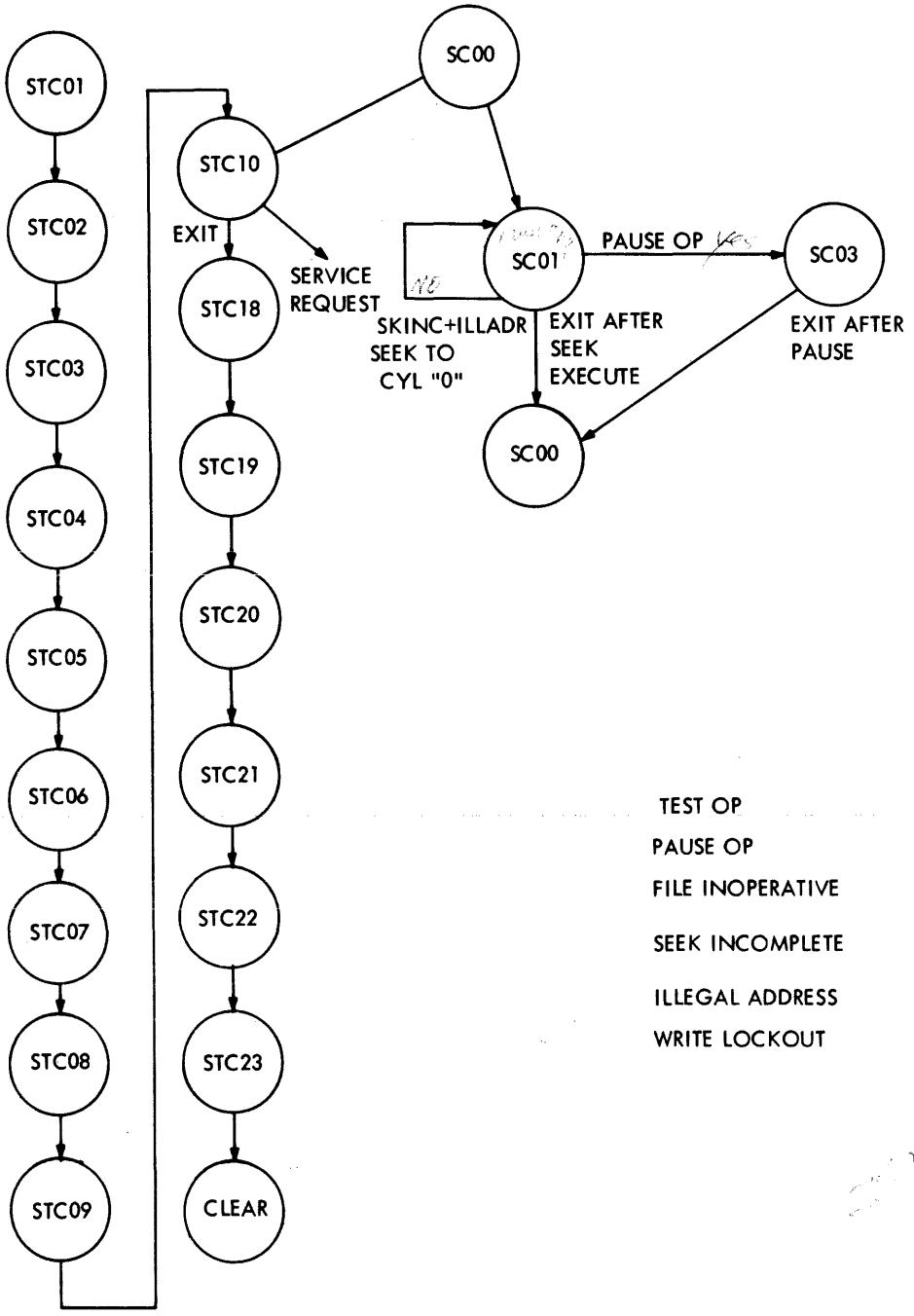


Fig. II-7 NON READ/WRITE OP

Functional Detail

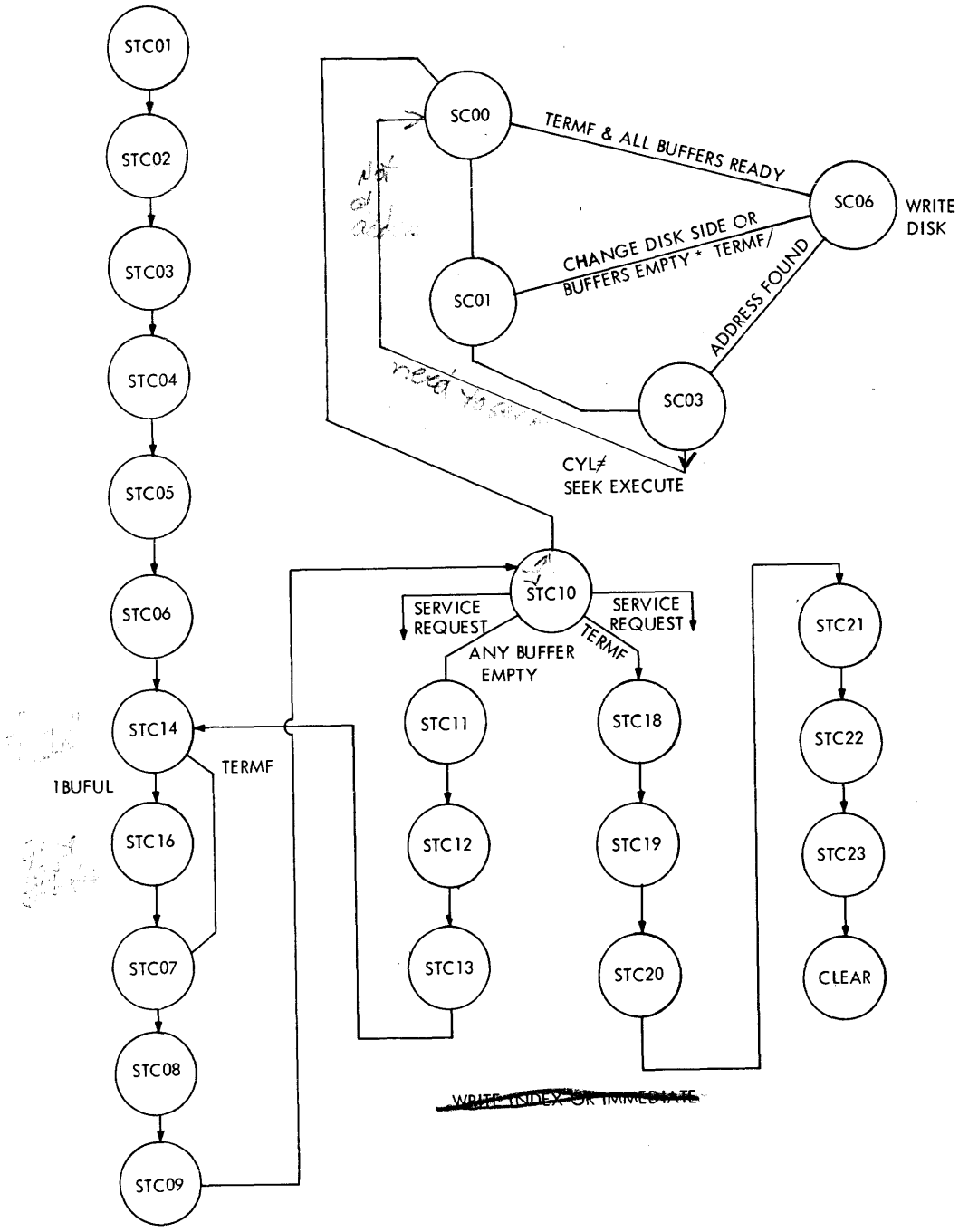


Fig. II-8 WRITE BURROUGHS FORMAT

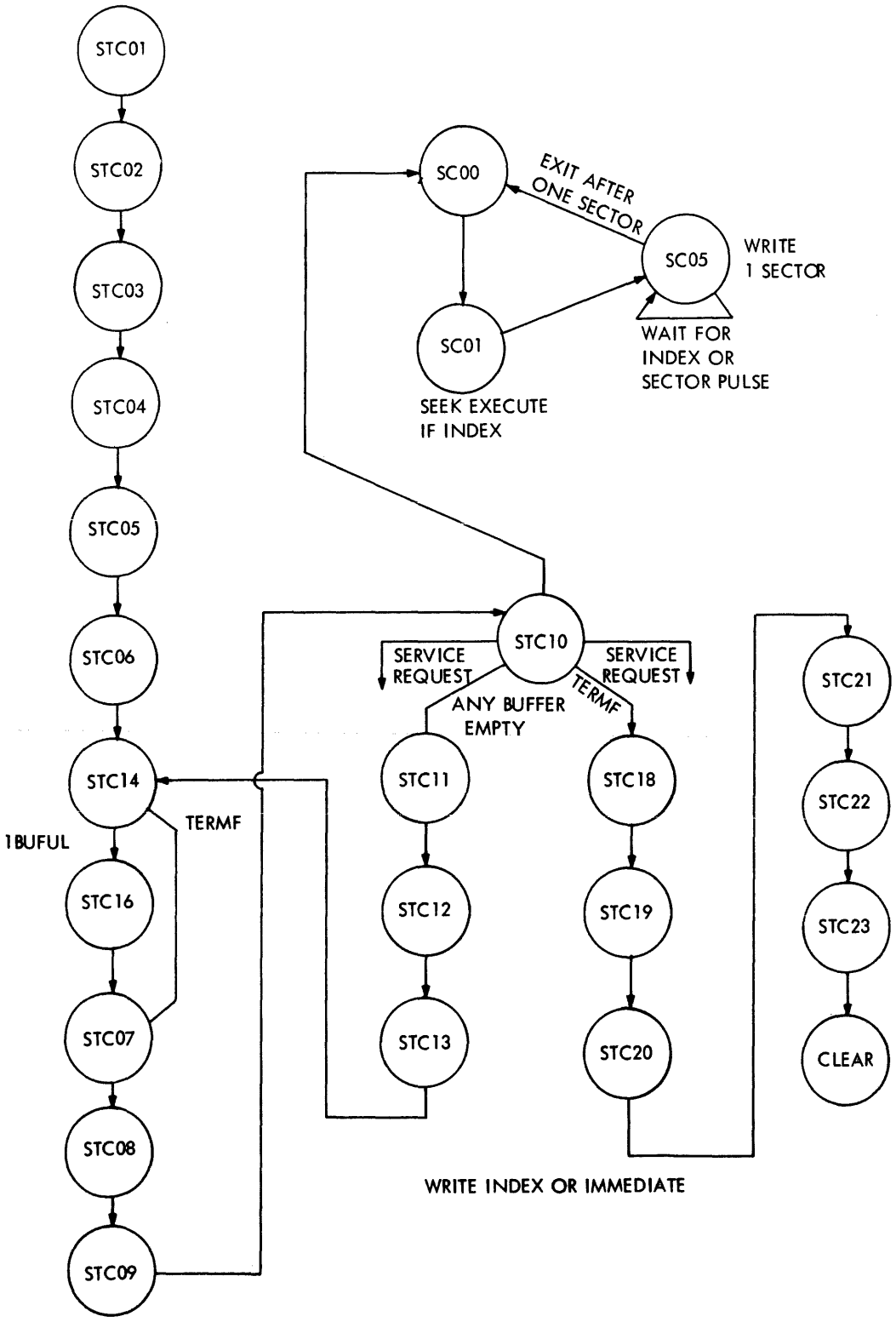


Fig. II-9 WRITE INDEX OR IMMEDIATE

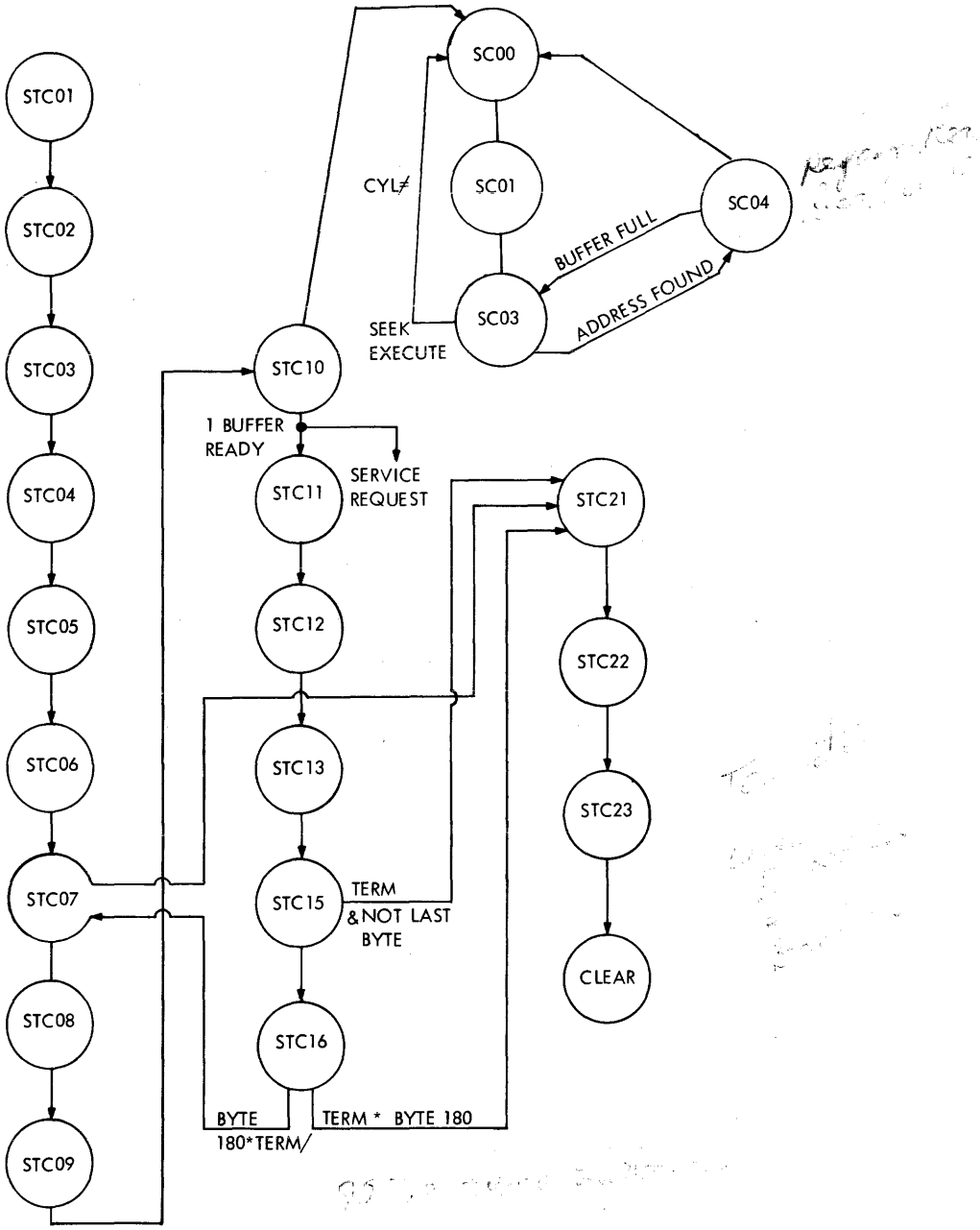


Fig. II-10 READ BURROUGHS FORMAT

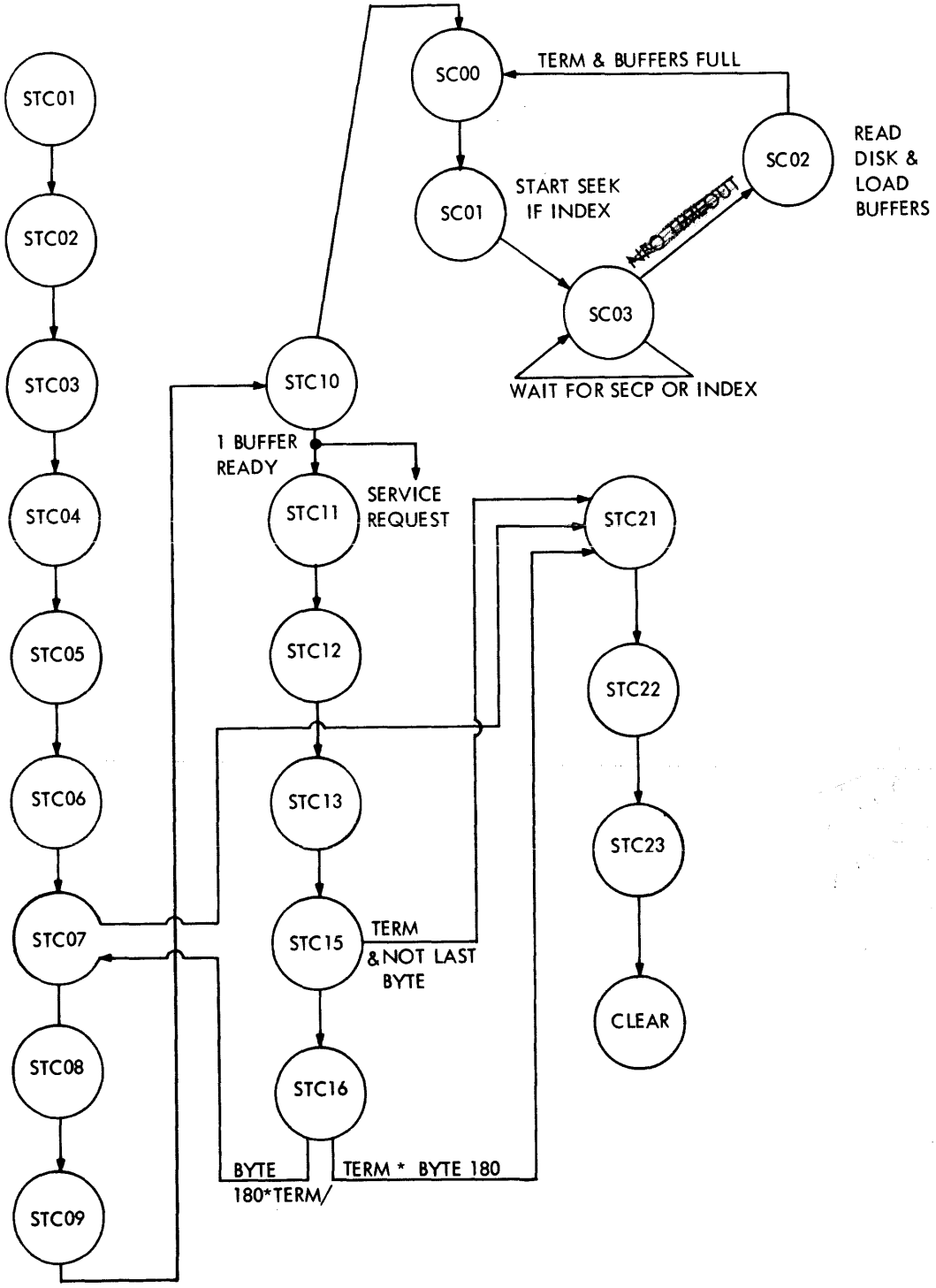


Fig. II-11 READ INDEX OR IMMEDIATE

GENERAL BUFFER CONTROL

The Disk Cartridge Control is a multiple buffer, input/output control. The Disk Cartridge Control contains four – 16 x 100 MOS Shift Registers and the associated logic to select the buffer to be used. The following paragraphs are to generally describe the clocking logic for one of the buffers, buffer load select and buffer dump select. Before continuing it is necessary to define load and dump. Load is defined as the time that a buffer is being filled or loaded with data. Load applies to both a disk read when data is read from disk or to a disk write when data is read from the processor and stored in the buffer. Dump is defined as the time a buffer is being emptied or dumped. Dump is applicable to a disk write when data is being "dumped" onto the disk or on a disk read when data is "dumped" to the processor.

BUFFER CLOCK

The Buffer Clock Logic for Buffer A is shown in Figure II-12. It should be noted that the inputs to the CTL Clock are shown in the flows at STC (Status Count) ANY or SC (Sequence Count) ANY time. The CTL Clock is the input to the MOS Clock Driver which supplies the MOS true and false voltage levels to the MOS Buffer. The following is a general description of each of the gates which will produce a clock to shift/load/dump the MOS Buffer.

GATE A

Gate A is enabled at Status Count 15 or 16 in order to allow data from the MOS Buffer to be transferred to the Processor for a Disk Read operation.

GATE B

Gate B is enabled during a Write Burrough's Format operation to cause data to be transferred to the Output Register and subsequently written on disk.

GATE C

Gate C is enabled for a Disk Write Immediate or Write Index to cause data to be shifted to the Output Register to be written onto disk.

GATE D

Gate D is enabled for a Read Index operation to cause the data read from disk to be transferred (loaded) into the MOS Shift Register.

GATE E

Gate E is enabled during a Disk Write operation at the time data is being read from the Processor and loaded into the MOS Shift Register.

GATE F

Gate F is enabled for a normal Read Burrough's Format to allow the data read to be stored into the MOS Shift Register.

GATE G

Gate G is enabled when a buffer that is being loaded receives a Terminate Command from the Processor. Gate G will allow a shift to occur in order to right justify the data within the MOS Shift Register.

GATE H

Gate H is enabled when a buffer has been loaded with 90 words and must be shifted in order to right justify the data by 10 places.

Functional Detail

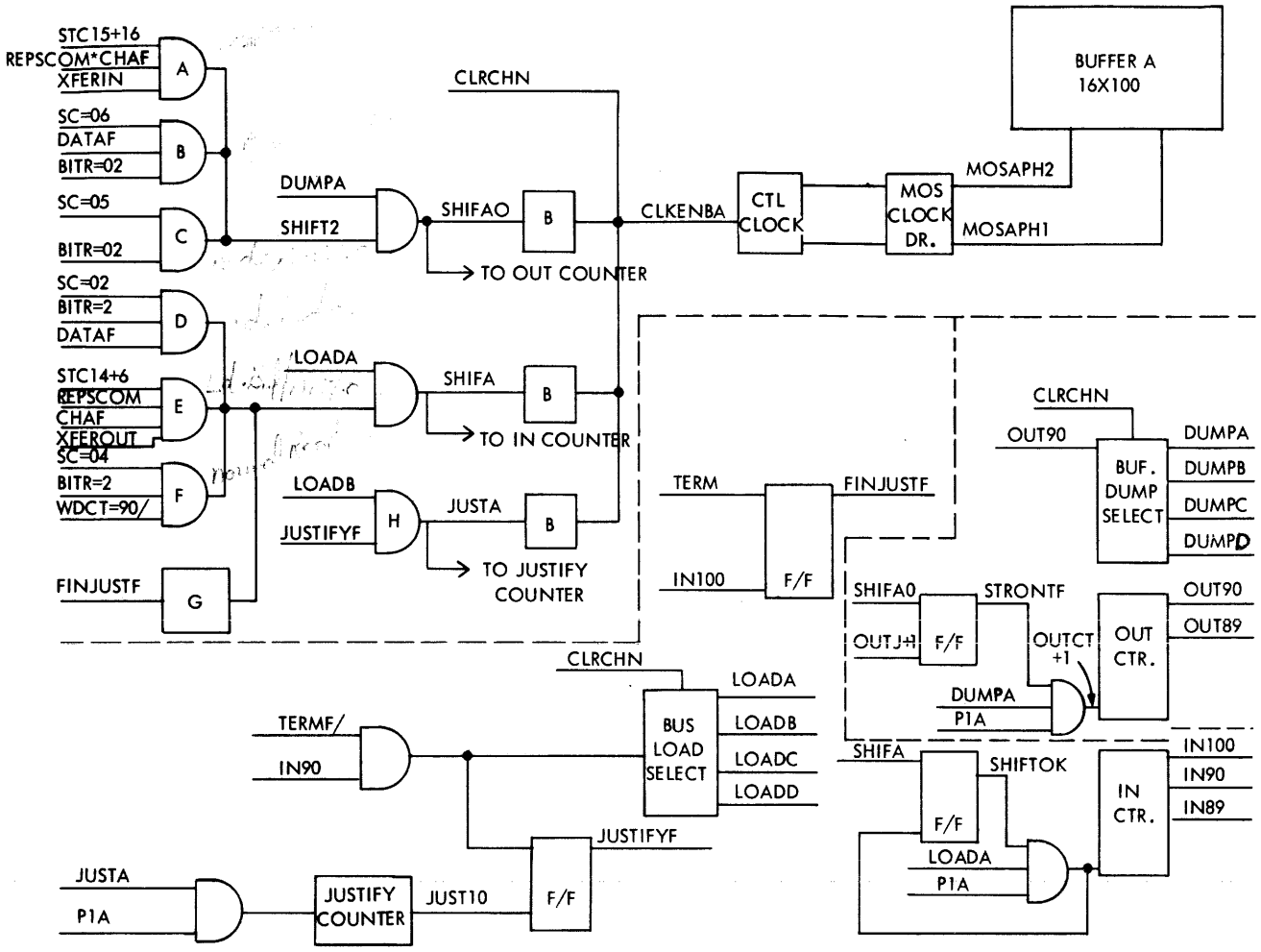


Fig. II-12 BUFFER CONTROL LOGIC

BUFFER LOAD

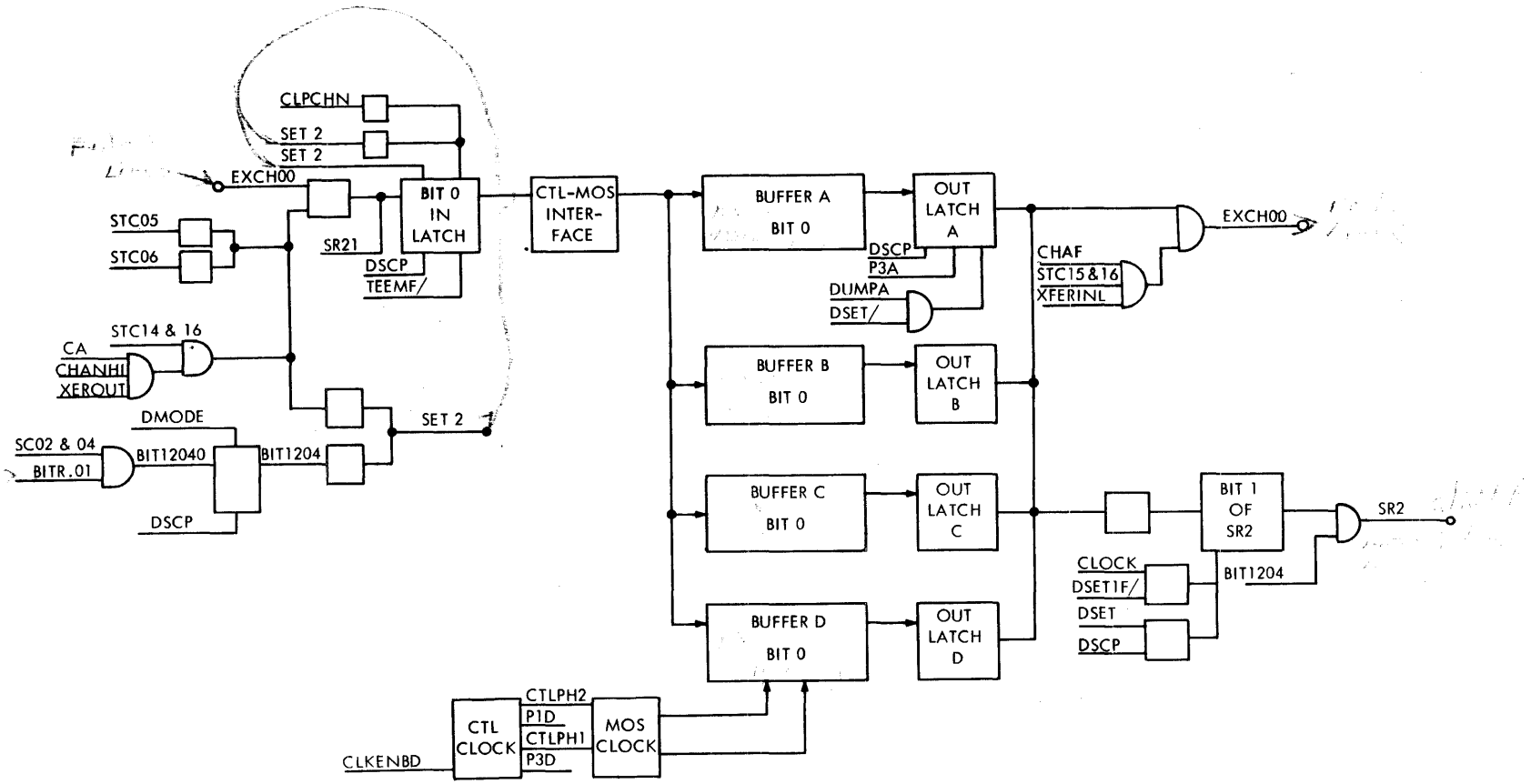
The Buffer to be loaded is selected by the Buffer Load Select logic. The load selection logic initially selects Buffer A as the Clear Channel resets the logic. The Load Select is upcounted each time the IN COUNTER counts 90 words received and no terminate received. The Load Select and In Counter are shown in Figure II-12. The In Counter is upcounted as a function of Load and an output (P1A) of the CTL Clock each time a word is loaded. Note that when the IN COUNTER reaches a count of 90, the Justify Flip-Flop is set in order to allow the data loaded to be right justified and allow the Justify Counter to count the data justify sequence. If a terminate is received prior to having input 90 words, the finish Justify F/F is set to cause the Justify and will reset when the In counter reaches a count of 100 indicating the data has been completely justified.

BUFFER DUMP

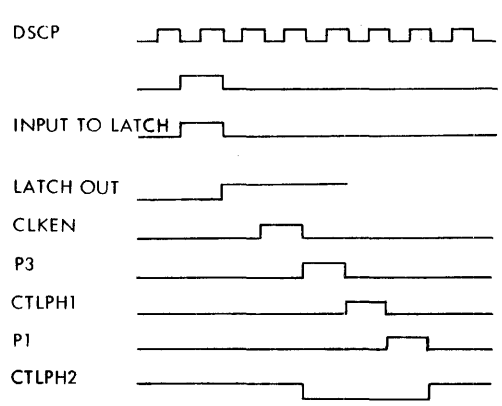
The Buffer to be dumped is selected by the Buffer Dump Select logic which can be seen in Figure II-12. The Dump Select is upcounted each time the OUTCOUNTER reaches a count of 90 words. Initially the Dump Select is set to Buffer A with a Clear Channel. The Out Counter is counted as a function of Dump and an output of the CTL Clock OP1A), each time a word is dumped.

BUFFER DATA IN/OUT

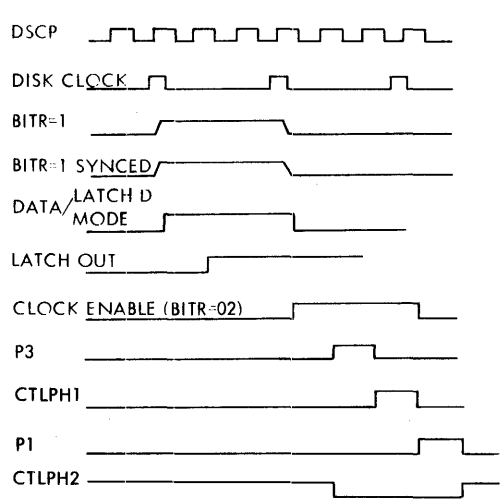
Shown in Figure II-13 is a diagram of the four MOS Shift Registers and the associated logic which pertains to data in and data out. Also shown in the diagram is the timing of the Disk Write data input and Disk Read Data input. It should be noted that the write input is primarily a function of the system clock while the read input must be synced with the disk read clock. The CTL and MOS Clock Logic has been described in the paragraphs pertaining to Buffer Clock and Figure II-18 with the outputs of the CTL Clock to be further described in the paragraphs on Logic Description.



MOS BUFFER DATA FLOW



WRITE INPUT TIMING



READ INPUT TIMING

Fig. II-13 MOS BUFFER DATA FLOW

LOGIC DESCRIPTION

The following diagrams with their associated descriptions show various sections of logic ocntained with the Disk Cartridge Control. Each of these sections are described within the flow charts in Section II of this manual and these paragraphs are written both to introduce and supplement the logic contained in the flows. Also described in these paragraphs will be timing diagrams pertinent to various operations.

BASIC PROCESSOR/CONTROL INTERFACE TIMING

Figure II-14 is a baisc timing diagram showing the relationship of Command Active and Response Complete which are the result of Processor issued commands. Command Active is also referred to as Phase A of the cycle and Response Complete as Phase B.

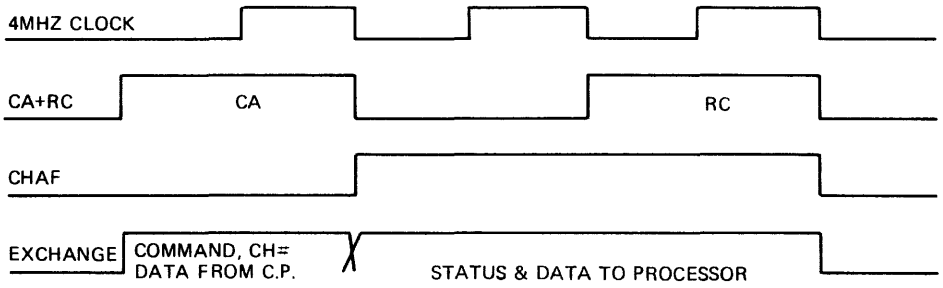


Fig. II-14 BASIC INTERFACE TIMING

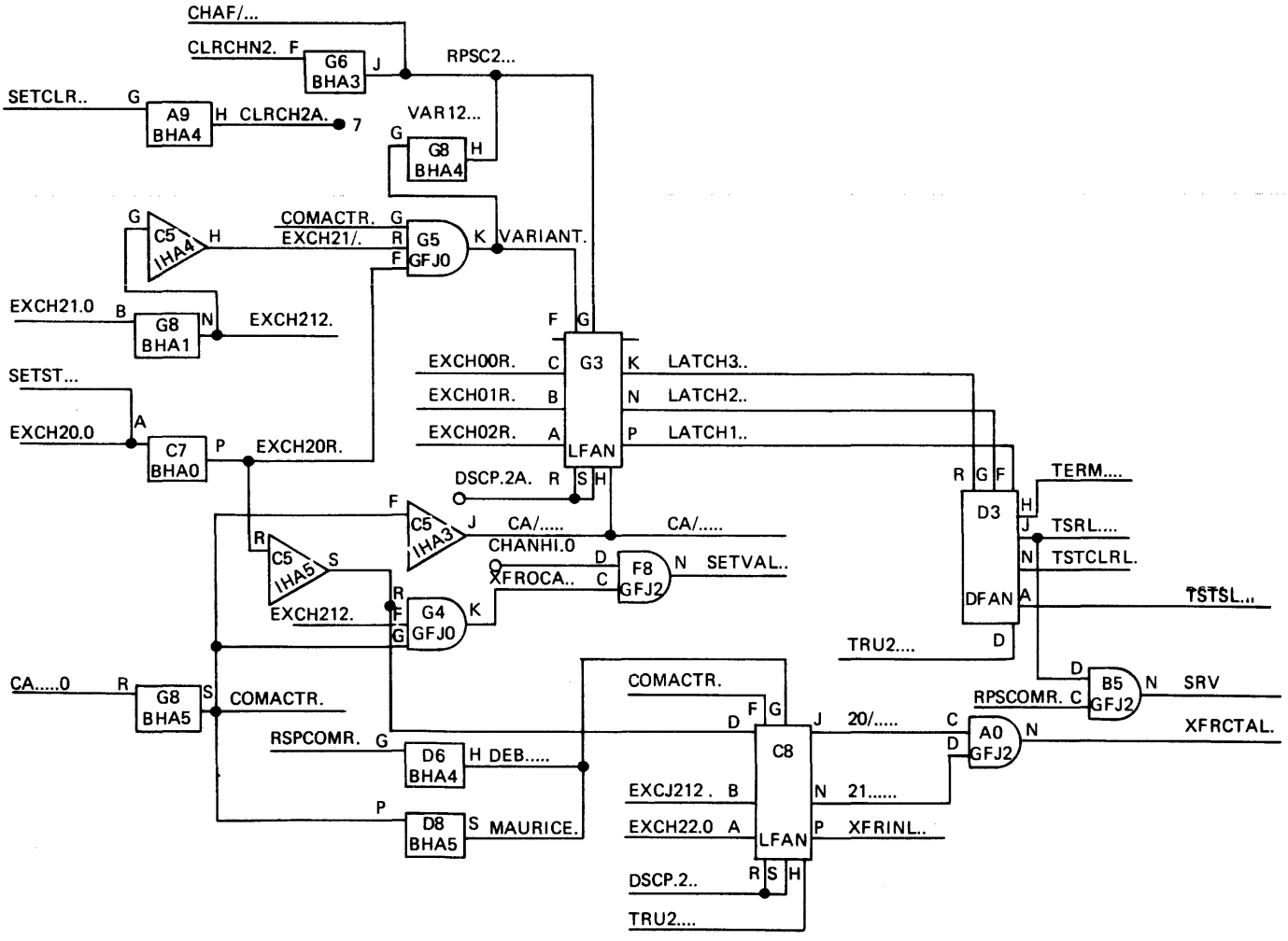


Fig. II-15 COMMAND REGISTER

COMMAND AND COMMAND VARIANT LATCHES

The Command and Command Variant Latches are used to hold the command which has been placed on the Exchange Lines from the Processor. Figure II-15 is a schematic of these Registers.

OP REGISTER

The OP Register or referred to as OP Latches are used to hold the Disk OP Code which has been sent from the Processor along with the variant bits. Note that the latch outputs are decoded to indicate the operation to be performed. Refer to Figure II-16. Read and Write are decoded separately and the variants are decoded to indicate Burroughs Format, Immediate or Index.

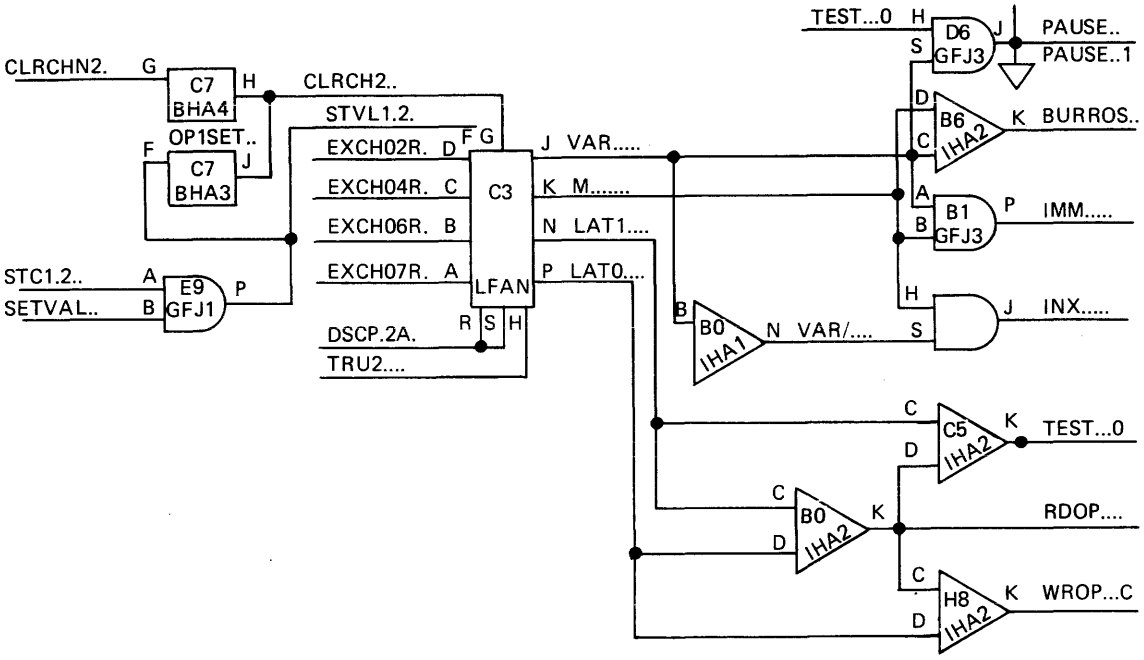


Fig. II-16 OP CODE REGISTER

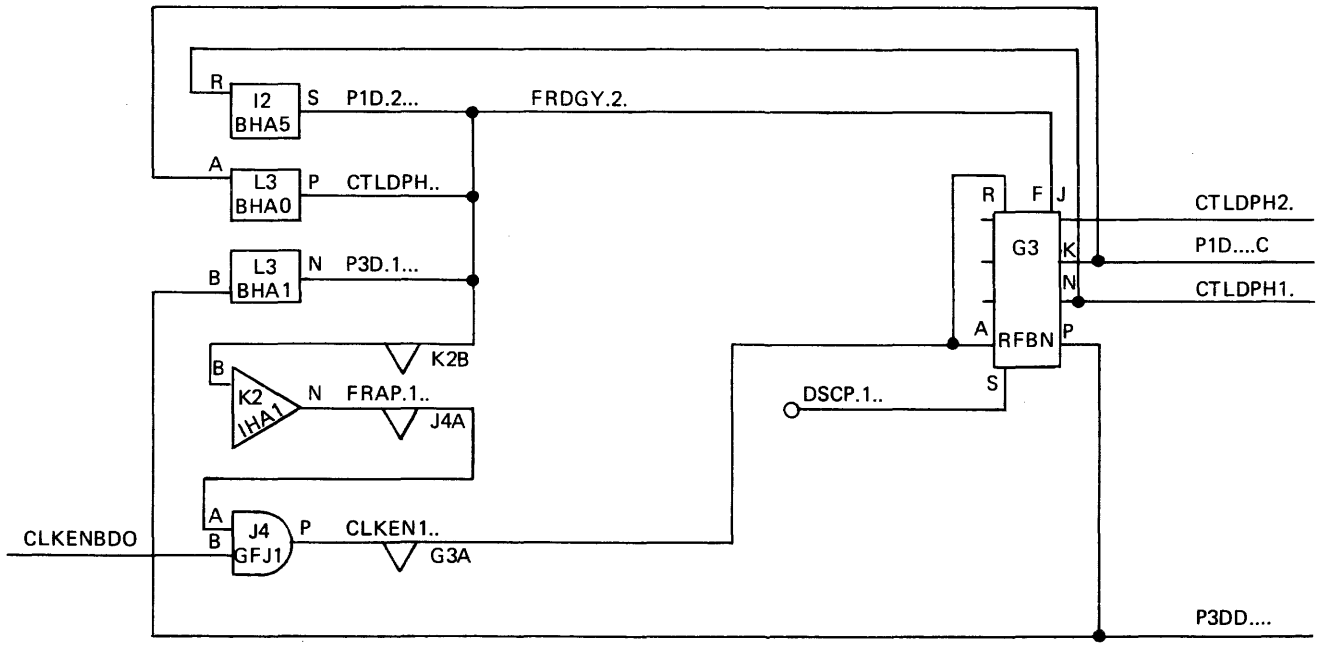


Fig. II-17 BUFFER D CLOCK LOGIC

SHIFT REGISTER CONTROL

Figure II-17 is a schematic diagram of the Shift Register Control Logic for Buffer D. The Shift Register Control is enabled in order to produce the clocking terms necessary to read/write/shift the MOS Shift Register. There is a separate Shift Register Control for each of the MOS Shift Registers contained within the Disk Cartridge Control.

OPERATION

Quiescently the term CTL-PH2 is true and P1D . . . . 0, CTLDPH1 and P3DD . . . . are false. When either data is to be stored or if the buffer data is to be shifted, the term CLKENBDO (Clock Enable Buffer "D") must come true. When CLKENBDO come true, the 4 Bit Register (RFBN) element will be placed in the "D" Set mode. On the trailing edge of the clock, P3DD . . . sets and CTLDPH2 resets. Through a buffer P3DD produces a term FRDGY .2. which places the RFBN element in the shift-up mode. Each clock that occurs will therefore cause a shift up until CTLDPH2 is again true at which time P1D . . . . 0, CTLDPH1. and P3DD . . . . will be false and thus remove the shift-up mode from the RFBN element. The terms CTLDPH2 and CTLDPH1 are sent to the MOS Clock Driver logic where they will allow the actual MOS clocks to be produced. The timing of the above operation and production of the MOS clocks are shown in Figure II-18.

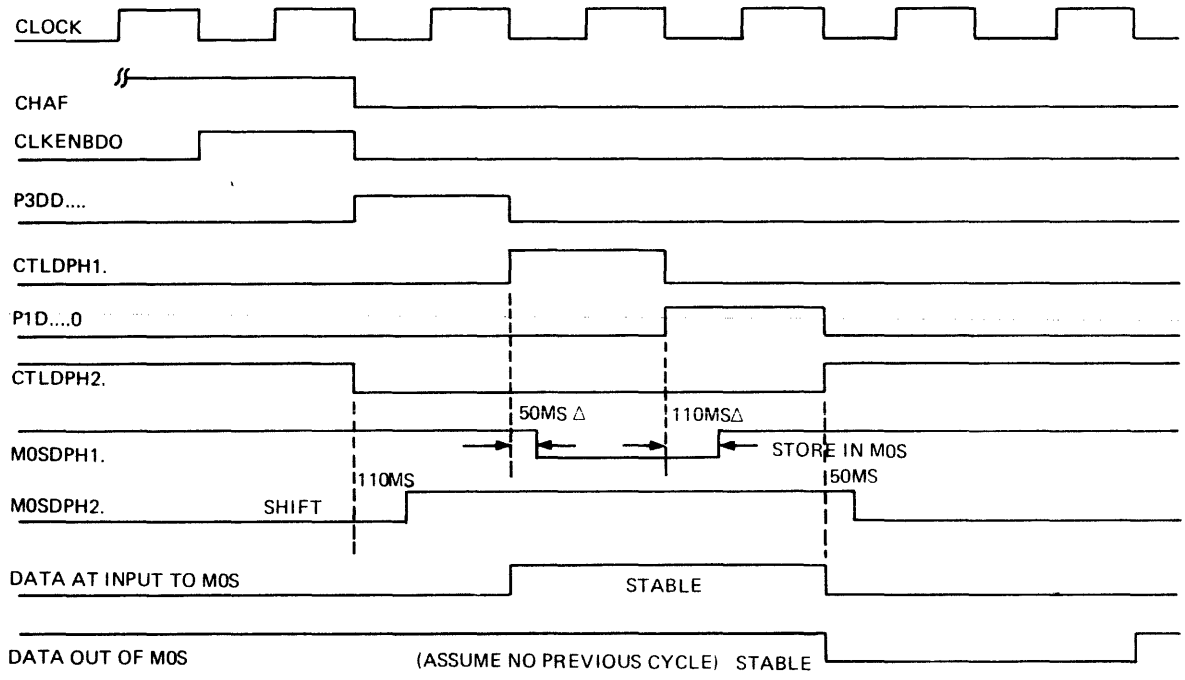


Fig. II-18 SHIFT REGISTER CONTROL TIMING

ADDRESS MEMORY

The Address Memory in the Disk Cartridge Control which consists of two-64 bit memory elements (RFCN), is used to store the Reference Address Bytes which are sent by the processor for all disk operations. Figue II-19 is a schematic of the Address Memory. The addressing terms for the elements are a combined decoding of the Status Counter. An example is the term SC71118. which is true at STC7, STC11 and STC18. The remaining terms may be decoded in a similar manner. The Write Enable term (WRENBLE.) must be false in order for a write to occur and true for a read.

Functional Detail

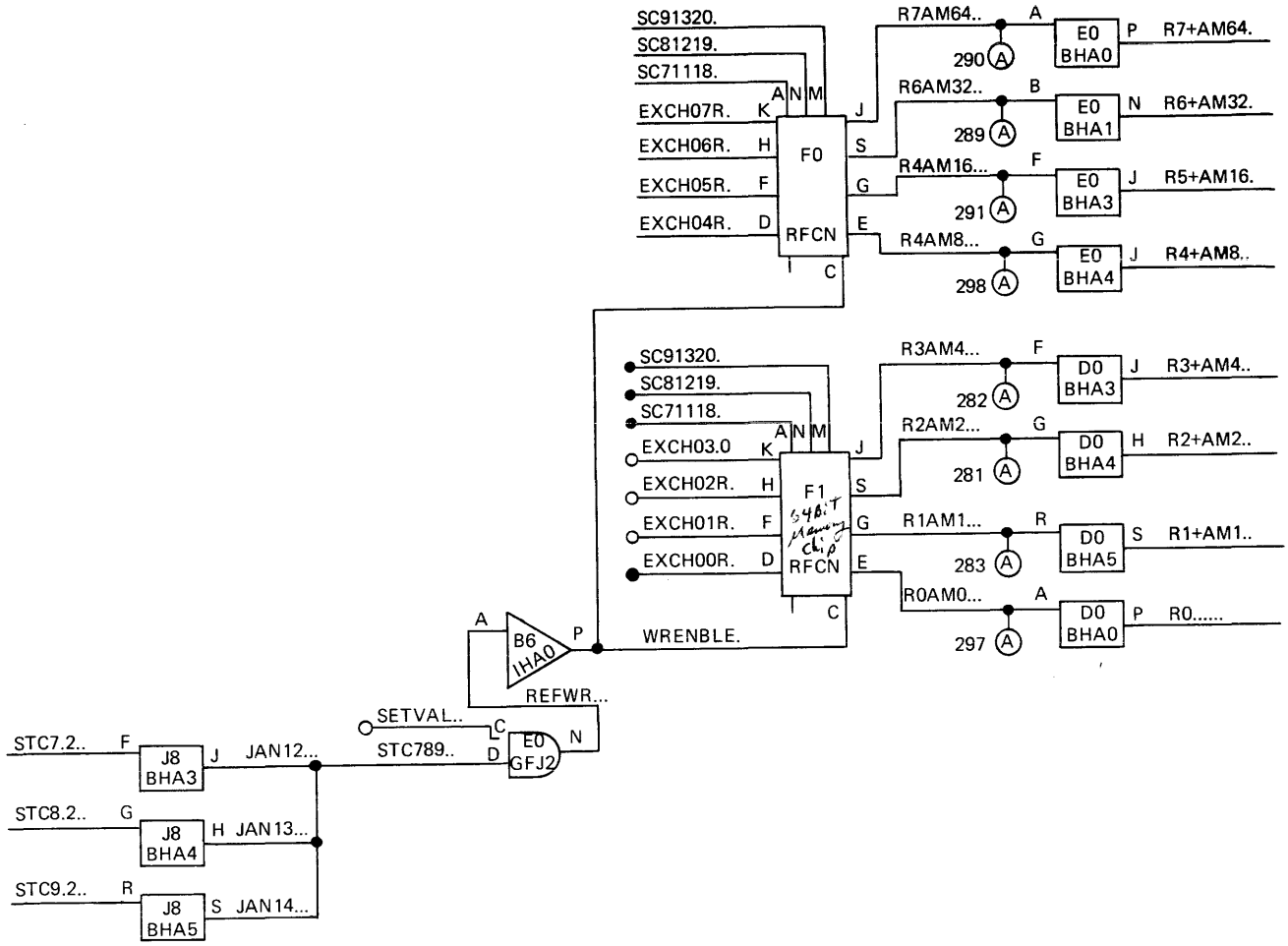


Fig. II-19 ADDRESS MEMORY

DISK SHIFT REGISTERS 1 and 2 (SR1 and SR2)

The Disk Shift Registers are used to accumulate the bit serial data from the disk in the case of a read or used to shift bit serial data to the disk on a write. Figure II-20 is a schematic of Shift Register 2. The "D" Set mode is used when setting data to be written onto disk into the Shift Registers and the Shift Mode is used when shifting data to/from the Shift Register. The input/output mnemonics for the Shift Register correspond to the Shift Register (one or two) and the bit position within the register. Example: SR23 . . . . may be decoded as Shift Register 2 and bit 3. The clocking term CLOCK . 1 . is a function of the read/write clock from the disk and CLRCK . 1 . is a function of the normal system clcok and a clear channel for clearing of the shift register.

READ TIMER

The Read Timer is used at Sequence Count 3 for various timing operations. One function that it performs is the delay for the Pause operation of approximately eight milliseconds. It is used on read operations to insert various required delays of 28 to 32 microseconds in one case and in another a delay of 64 to 96 microseconds. The logic is shown in the Sequence Count 3 flow and Figure II-21 is a diagram of the actual Read Timer and associated logic. For operation of the Read Timer refer to the SC=03 flows contained within this manual.

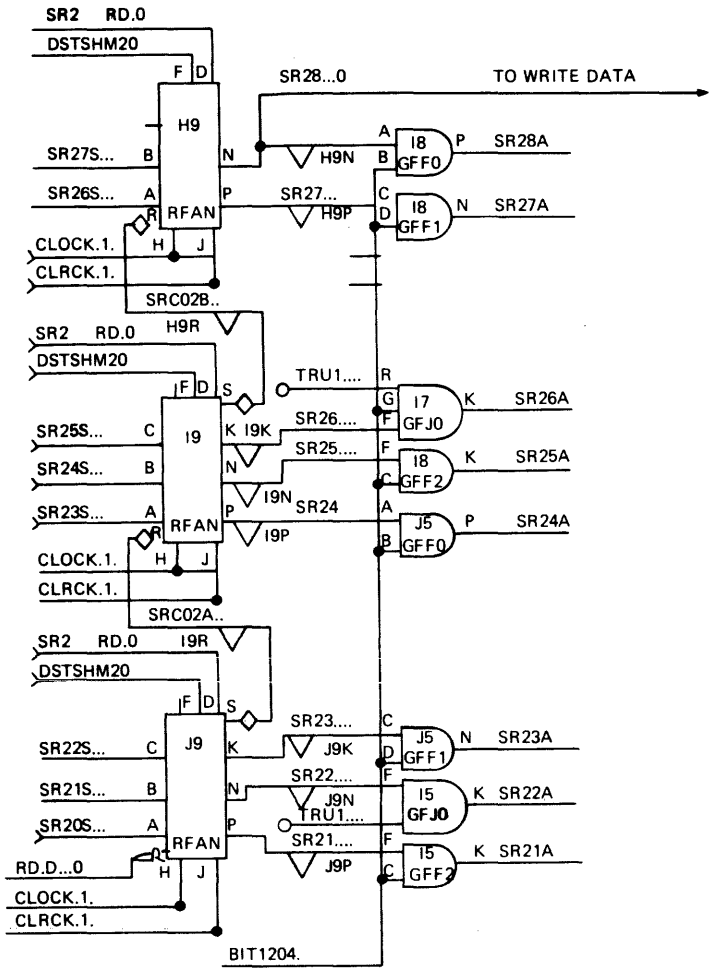


Fig. II-20 SHIFT REGISTER 2

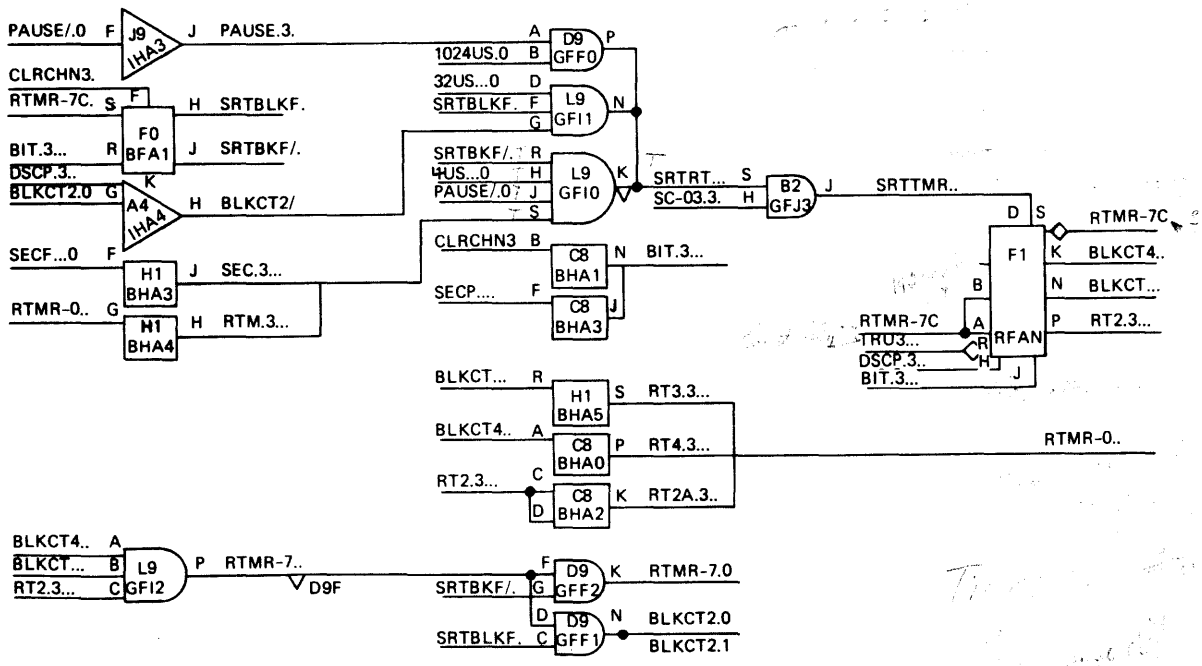


Fig. II-21 READ TIMER

DETAILED FLOW

STATUS COUNT ANY (STCAN)

CHAF ← 1	COMACT*(CHANHI+TSR)
CHAF ← 0	REPSCOM
CHANHI	COMACT*(JPRCHP* EXCH16-19 + TESTR)
XFROTA	COMACT*EXCH21* EXCH20/
XFROTAL	COMACT*XFROTA
XFERIN	COMACT*EXCH22
XFERINL	COMACT*XFERIN
CONV	COMACT*EXCH21/ *EXCH20
TSTSL ← 1	CONV*EXCH00* EXCH01/*EXCH02/
TSTCLRL ← 1	CONV*EXCH00* EXCH01*EXCH02/
TSRL ← 1	CONV*EXCH00* EXCH02
TSRL 1	TSR*COMACT

Status Count Any is a flow of logic terms which can occur at any Status Count.

The Channel Active Flip-Flop is set with Command Active and the command on the Exchange Lines is for the Disk Control as indicated by Channel High (CHANHI). The CHAF is also set for a Test Service Request Command which is not specifically addressed to any channel.

During phase B of the cycle as indicated by Response Complete (REPSCOM), the Channel Active Flip-Flop is reset in preparation for another command.

Channel High is true if the command on the Exchange Lines 16 thru 19 is for the Disk Cartridge Control. The Control Number is assigned via a jumper chip. Channel High is also true if the Card is placed in the tester in which case the term TESTR is true. This is done to allow the logic to function in the Card Tester.

The term XFROTA (Transfer Out A) is true if the command on the Exchange Lines is a Transfer Out A Command.

The Transfer Out A Command is latched to hold the condition in order to allow the logic to perform the required functions.

The term XFERIN (Transfer IN) is true if the command on the Exchange Lines is a Transfer In Command from the Processor.

The Transfer In Command is latched to hold the condition in order to allow the logic to perform the required functions for the Transfer In command.

With Command Active, if the Command is a Control Variants command such as Test Status, Clear and Test Status or Terminate Data then the Control Variant Register will be set with Exchange Lines zero thru three which indicate which of the above mentioned commands is on the Exchange.

If the Control Variant Command is a Test Status as decoded on the Exchange, set the Test Status Latch.

If the Control Variant Command is a Test and Clear as decoded on the Exchange, set the Test and Clear Latch.

TSR level is generated if Control Variant Command is Test Service Request.

If the Control Variant Command is a Test Service Request, set the Test Service Request Latch.

STCAN (Continued)

TERM	CONV*EXCH00/* EXCH01*EXCH02*CHAF	The Terminate Command on the exchange lines brings TERM true.
TERMF ← 1	TERM*CHAF	The Terminate Flip-Flop is set with TERM and Channel Active.
CMDCDLATCH ← 0	CHAF/	With the Channel Active Flip-Flop reset, clear the Command Code Latches (TSTSL, TSTCLRL, TSRL and TERMF).
EXH1620 ← STC116F	CHAF*TSRL/	If the Channel is active and as long as the command is not a Test Service Request, the Status Count is returned to the Processor on the Exchange Lines 16 thru 20.
EXCH2-4 ← 1	CHAF*(TSTSL+ TSTCLRL)	If the Processor has commanded either a Test Status or Clear and Test Status, the Channel Identification number (001110) is returned along with the status.
EXCH015 CHNLMSK	CHAF*SRF*TSRL *TESTR/*JPRCHP	Gate the Service Request bit to the Exchange Lines.
IOS ← 1	CHAF	I/O Send is enabled in order to allow the Control to send data to the Processor during phase B of the cycle.

SEQUENCE COUNT ANY (SCANY)

EXITF ← 0 SC ← 00	EXITF	If the Exit Flip-Flop is set to terminate an operation, the Control is returned to Sequence Count Zero and the Exit Flip-Flop is reset.
TRKZROF ← 1	((ILL.ADD+SK.INC) *ASEL+BSEL)	Track Zero Flip-Flop is set if an Illegal Address has been sent or seek is incomplete. Track Zero prevents the Control from initiating a disk operation.
ASEL	UNIT1F/	If UNIT Select 2 bit in OP is false, set ASEL.
BSEL	UNIT1F	If UNIT Select 2 bit in OP is true, set BSEL.
FAREG ← 0	TRKZROF	If the track zero is set then the File Address Register is cleared and the Control returned to sequence count 1 in order to make the appropriate exit.
SC ← 1	TRKZROF*PAUSE/	
BITR=2F ← 1	BITR=1	
BITR=2F ← 0	BITR=2F	

GENERAL

CLKENBN	SHIFIN+JUSTN +SHIFON+CLRCHN +TSTRSHF	Clock Enable (CLKENBN) to the addressed MOS Shift Register is enabled to produce clocks which will allow the MOS Shift Register to shift. The enabling logic is Shift In which is true for a buffer load, Justify which is true during a buffer load to right justify the data, Shift Out which is true for a dump when the buffer is being unloaded and Clear Channel which will produce shift clocks in order to shift out or clear the data in the buffer.

GENERAL (Continued)

P3N ← 1	CLKENBN*(CTLNPH1/ +PIN/+P3N/) +(TESTER*CLRCLK)	With Clock Enable and if the clock generator is not already in a sequence as indicated by CTLNPH1/* P1N/*P3N/, set P3N to
CTLNPH1 ← P3N	P3N	With P3N set, set CTLNPH1 as the clock generator is in the shift up mode. See Section II Logic Description for a description of the clock generator and timing.
P1N ← CTLPH1	CTLNPH1	Continue the clock generator timing which is still in the Shift Up mode.
CTLNPH2 ← P1N	P1N	Continue the clock generator timing which is in the Shift Up mode. Setting of CTLNPH2 will complete the clocking sequence and the data within the MOS Shift Register will have been right justified by one position. By producing Clock Enable another sequence will start to enable further storage and shifting of data.
BFSCT+1	(IN100+JUST10) *((IN100/+JUST10/) *OUT90/)	The Buffer Select Counter is used to count the number of buffers (MOS Shift Registers) in use. IN100 is true if a terminate was received prior to reception of 180 bytes or 90 words and therefore the buffer is justified until the IN Counter reaches a count of 100 (IN100). JUST10 is true if 180 bytes or 90 words have been received and the Justify Counter indicates that the buffer has been right justified by 20 bytes or 10 words (JUST10). In either case the buffer is full and the Buffer Select Counter is upcounted to indicate a buffer has been loaded and justified.
BFSCT-1	OUT90*((IN100/ +JUST10/)*OUT90/)	The Buffer Select Counter is decremented when a buffer has been unloaded as indicated by Out 90.
BUFSEMP	BFSCT=0	If the Buffer Select Counter is equal to zero then the Buffers are empty (BUFSEMP).
BUFRDY	BFSCT≠0	With the Buffer Select Counter at some count other than zero then a Buffer is ready (BUFRDY).
3BUFULL	BFSCT=3	The Buffer Select Counter being equal to three, 3 buffers are full (3BUFULL).
1BUFULL	BFSCT=1	The Buffer Select Counter being equal to one, 1 buffer is full.
BUFSFLF ← 1	3BUFULL*IN90	With 3 Buffers Full (3BUFULL) and the fourth buffer having received 90 words as indicated by the IN Counter (IN90) then all buffers are full (BUFSFLF) and thus the Buffers Full Flip Flop is set.
BUFSFLF ← 0	OUT90	When the Out Counter has counted 90 words then one of the buffers has been emptied. If the Buffers Full Flip-Flop (BUFSFLF) was set, reset it.

LOAD

Load is the sequence when the buffers or MOS Shift Register is being loaded with either data from the Processor or data from the Disk.

SHIFIN	LOADN*(STC1416* REPSCOM*XFROTAL* CHAF+BITR=2*((SC=02 *DATAF+WDCT=90/ *SC=04)+FINSHF)
FINJSTF ← 1	TERMF*INCT≠0*JUST1F/
FINJSTF ← 0	IN100
JUSTN	LOADN+1*JUST1F
JUST1F ← 1	IN90*TERMF/

Shift In (SHIFIN) is true to produce clock enable for the storing of data in the MOS Shift Registers. On a disk write operation the control loads the data to be written at Status Counts 14 or 16 with a Transfer Out Command as indicated by the logic STC1416* REPSCOM*XFROTAL*CHAF.

The loading of the buffers for a Read Index is accomplished at SC=02 after 16 bits have been read and transferred from the input bit register to the input latches for the MOS Shift Register.

The loading of the Buffers for a Read Burroughs formal is performed at SC=04 with BITR=02 which indicates that 16 bits have been accumulated and transferred to the input latches. When the Word Count reaches 90 then the Shift In is disabled by WDCT=90/ indicating all 180 bytes have been read.

If a terminate had been received, FINJUSTF would set and produce shift

The Finish Justify Flip-Flop (FINJSTF) is set to produce shift pulse to justify the data in the MOS Shift Register if a terminate command is received prior to having completely loaded a buffer. If the buffer is already being justified by JUST1F then there is no need to set FINJSTF, thus the logic JUST1F/. If the In Counter is at zero then there is no data in the buffers to justify thus the logic INCT≠0.

The IN Counter having reached a count of 100 (IN100) the justification of the data is complete therefore reset the Finish Justify Flip-Flop.

When a buffer is loaded with 90 words then the LOADN+1 logic is true to enable the loading of the next buffer. JUST1F is set when the buffer was loaded with the 90th word and therefore the term JUSTN is true to the buffer just loaded in order to produce shift clocks to justify the buffer.

Justify Flip-Flop is set to produce JUSTN for justification of the data. There are two means provided to justify the buffer; the normal way is for IN90 and TERMF/ which indicates 180 bytes have been loaded and a terminate not received. The second means is if a terminate is received prior to receiving 180 bytes. In this case the Finish Justify Flip-Flop is set to cause the justify to occur.

LOAD (Continued)

JUST1F ← 0	JUST10	When the Justify Counter has counted ten justify buffer clocks, reset the JUST1F and the justify is complete.
JUSTCTR+1	LOADN*JUST1F*P1N	Upcount the Justify Counter with each P1N from the Clock Generator as long as JUST1F is set.
JUST10		10 Right Justify Clocks have been counted by the Justify Counter.
LOADN		Load "N" is true for the buffer that is receiving data where "N" is equal to A,B,C or D.
LOADA	LOADD*(IN90*TERMF/ +IN100 +CLRCHN)	Load Buffer A is true if buffer D has been loaded and a terminate has not been received as indicated by the logic LOADD*IN90*TERMF/ or if Buffer D has been loaded and a terminate has been received as indicated by the logic LOADD and IN100. Any time a Clear Channel (CLRCHN) occurs, reset the buffer load select logic to cause a load of Buffer A.
LOADB	LOADA*(IN90*TERMF/ +IN100)	Load Buffer B if Buffer A has been loaded.
LOADC	LOADB*(IN90*TERMF/ +IN100)	Load Buffer C if Buffer B has been loaded.
LOADD	LOADC*(IN90*TERMF/ +IN100)	Load Buffer C if Buffer C has been loaded.
INCT+1	LOADN*SHFOKF*P1N	Upcount the IN Counter plus one as each word is loaded into a buffer.
SHFOKF ← 1	SHIFIN*IN100/	With Shift In true (SHIFIN), and IN100/, set SHFOKF to allow the IN Counter to upcount by one.
SHFOKF ← 0	INCT+1	With the logic enabled to upcount the In Counter plus one, the clock will reset the SHFOKF flip-flop and upcount the IN Counter.
INCT ← 0	IN90*TERMF/+IN100	The In Counter is reset to zero if it has counted 90 words and a terminate has not been received. If a terminate has been received, the IN Counter will count to 100 in order to allow the data received to be justified completely to the right.
IN88	88 Input Buffer Clocks	Input 88 (IN88) is true if 88 input Buffer Clocks have been generated.

LOAD (Continued)

IN90	90 Input Buffer Clocks
IN100	100 Input Buffer Clocks

Input 90 (IN90) is true if 90 input Buffer Clocks have been generated.

Input 100 (IN100) is true if 100 input Buffer Clocks have been generated.

DUMP

Dump is the sequence when the MOS Shift Register is being emptied either to disk in the case of a disk write or to the Processor in the case of a disk read.

SHIFON	DUMPN*(STC1516*CHAF *REPSCOM*XFRINL +BT2SYNF*(SC=06 *DATAF+SC=05))
BT2SYNF	BIT2SF/*B12SYNF
BIT2SF ← 1	BIT2SYNF
BIT2SF ← 0	BIT2SYNF/
BIT2SYN ← 1	BITR=2F
BIT2SYNF ← 0	BITR=2F/
DUMPN	
DUMPA	DUMPD*OUT90+CLRCHN

Shift Out (SHIFON) is true to cause Clock Enable (CLKENB) to generate clocks in order to empty the MOS Shift Register.

On a Disk Read the information is sent to the Processor at Status Count 15 or 16 with a Transfer In Command.

On a Disk Write, data is sent or shifted out to the output latches at Sequence Count 5 or 6 at Bit Ring equal two and the Data Mode Flip-Flop (DATAF) set. Sequence Count 5 is for a Write Index and Sequence Count 6 for a normal Write Burroughs format.

The purpose of the following 5 logic boxes is to Sync the Bit Rint Counter with System Clock.

Dump "N" is true for the buffer that is being emptied where "N" is equal to A,B,C or D.

Dump Buffer "A" is true if Buffer D has been emptied as denoted by DUMPD*OUT90 or if a channel clear (CLRCHN) occurs to reset the Dump Logic.

DUMP (Contined

DUMPB	DUMPA*OUT90	Dump Buffer "B" if Buffer "A" has been dumped as denoted by DUMPA*OUT90.
DUMPC	DUMPB*OUT90	Dump Buffer "C" if Buffer "B" has been emptied as denoted by the logic DUMBB*OUT90.
DUMPD	DUMPC*OUT90	Dump Buffer "D" if Buffer "C" has been emptied as denoted by the logic DUMPC*OUT90.
OUTCT+1	DUMPN*P1N*STRCNTF	Upcount the Out Counter by one for each clock that causes a word to be shifted out of the MOS Shift Register.
STRCNTF ← 1	(STC1516*REPSCOM*XFERIN *CHAF)+BITR=2*(SC=06 *DATAF +SC=05)	The Start Count Flip-Flop (STRCNTF) is set to allow the Out Counter to count. At Status Count 15 and 16 the logic is enabled as the data is to be sent to the Processor with a series of Transfer In Commands. With BITR=2 and with the SC=05 or 06 then the data is being sent to the disk for a write operation.
STRCNTF ← 0	OUTCT+1	With the logic generated to upcount the Out Counter, the clock that occurs will reset the Start Count Flip-Flop and upcount the Out Counter.
OUTCT ← 0	OUT90	The Out Counter is reset to a count of zero when it has reached the maximum count of 90.
OUT88		88 Output Buffer Clock have occurred.
OUT90		90 Output Buffer Clocks have occurred.

STC00

STC+1 OPREGL ← 0		If the Status Counter is set to zero with a Clear Channel, the logic is enabled to go to Status Count One and clear the OP-Register Latches.

STC01

OPREGL ← EXCH7-0	COMACT*CHANHI XFROTA	During Status Count One, the first byte of the OP Code is received on Exchange Lines 0 through 7 and placed in the OP Register Latches.
STC+1	REPSCOM*CHAF *XFROTAL	During phase B of the cycle the status is sent to the processor (See common logic) and the Status Counter is counted to 02.

STC02

STC+1	REPSCOM*CHAF *XFROTAL

Nothing received at STC02 but the status is returned to the Processor at Phase B of the Cycle.

STC03

UNIT1-0F ← EXCH1-0	COMACT*CHANHI *XFROTA
STC+1	REPSCOM*CHAF *XFROTAL

Byte 3 of the OP Code is received at Status Count 3, Byte 3 contains the Unit number which is placed in the Unit Flip-Flops.

At phase B of the cycle the Status Counter is upcounted to 04 and status is returned to the processor.

STC04

STC+1	REPSCOM*CHAF *XFROTAL

During Status Count 4, Byte 1 of the File Address is received which is not significant at this time. Status is returned to the Processor during phase B of the cycle.

STC05

CYL9-3 ← EXCH6-0	COMACT*CHANHI*XFROTA
STC+1	REPSCOM*CHAF *XFROTAL

Byte 2 of the File Address is received at Status count 5. Byte 2 contains a portion of the cylinder address and is set into Cylinder Flip-Flops 9 thru 3. The Cylinder Flip-Flops are a portion of the File Address Register.

Phase B of the cycle, sent status to the processor and count the status count to 6.

STC06

CYL2-1F ← EXC7-6 HEADF ← EXCH5 SEC5-1F ← EXCH4-0	COMACT*CHANHI *XFROTA
STC ← 14	REPSCOM*CHAF *XFROTAL*WROP
STC+1	REPSCOM*CHAF* XFROTAL*WROP/

Byte 3 of the File Address is received at Status Count 6. The remaining portion of the cylinder address is stored in the cylinder flip-flops, the disk side is stored in the Head Flip-Flop (HEADF) and the sector address is stored in the sector flip-flops. All are a part of the File Address Register.

If the disk operation is a write then exit to Status Count 14 to start loading the data in the Buffers.

If the operation is not a write op then at Phase B of the cycle exit to STC07 to load the Reference Address Byte 1. Also during phase B of the cycle, the Status is returned to the Processor.

STC07

ADDMEM1 ← EXCH7-0 WRENBLE	COMACT*CHANHI XFROTA

At Status Count 7, Reference Address Byte One is received and stored in an Address Memory with Write Enable being true. Because the disk control has multiple buffers the Reference Address is stored in an area separate from the data.

STCOT (Continued)

STC+1	REPSCOM*CHAF *XFROTAL
STC ← 21	REPSCOM*CHAF *TERMF*RDOP

Exit to Status Count 8 to receive Byte 2 of the Reference Address.

If the OP is a Read and a Terminate Command is received at this time, exit to Status Count 21 to return the Result Status bytes. Terminate would be received at this time as a result of the Control having sent data to the processor at Status Count 15 and 16 and then determining that it has received all the data required. The Terminate would therefore have to be recognized at STC07.

STC08

ADDMEM2 ← EXCH7-0 WRENBLE	COMACT*CHANHI *XFROTA
STC+1	REPSCOM*CHAF XFROTAL

Reference Address Byte 2 is stored in Address Memory location 2.

At Phase B of the cycle, upcount the Status Count to 9 and return the status to the processor.

STC09

ADDMEM3 ← EXCH7-0 WRENBLE	COMACT*CHANHI *XFROTA
STC+1	REPSCOM*CHAF *XFROTAL

Reference Address Byte 3 is stored in Address Memory Location 3.

At Phase B of the cycle, upcount the status count to 10 and return status to the processor.

STC10

SC ← 1	SC=0*(TSTNY/+TRKZROF) *(POS.SET+PAUSE)
STC+1	WROP*TERMF/*BUFSFLF/ *TRKZROF
SRF←1	WROP*TERMF/*BUFSFLF/
	+RDOP*BUFRDY*TERMF/
	+PAUSE*EXITF

At Status Count 10 if the operation is a Write and if the Buffers are not all full as indicated by the Buffers Full Flip-Flop being reset then set the Service Request Flip-Flop and exit to STC11 to send the Reference Address and subsequently obtain more data from the Processor.

If the operation is a Read and a buffer is ready with data, set a Service Request provided a Terminate Command had not been received.

If the operation is a Pause, exit to Status Count 18 with the logic shown in the STC 18 block and set the Service Request Flip-Flop. The Exit Flip-Flop for the Pause is set at SC=3 upon completion of the pause.

STC10 (Continued)

SRF ← 1	EXITF*(RDOP/+FLOPNL/ +TRKZROF+PRES/ +POSSET/DTOT2F)
EXITF ← 1	SC=0*PAUSE/ *(POSSET/+TEST +WR.LKT+PRES/+FLOPML)
STC+1	RDOP*BUFRDY* TRKZROF/
STC ← 18	EXITF*(RDOP/+PRES/ +FLOPNL/+DTOT2F +TRKZROF/ +POSSET/

Exit Flip-Flop is set to cause the control to exit the operation and set a service request.

EXITF*RDOP/ would be true if the operation is a Pause or Test OP.

EXITF*FLOPNL/ would be true if the disk is not operational due to for an example a cartridge not in the unit.

TRKZROF*EXITF would cause an exit if an illegal address had been received or if a previously initiated seek was not complete.

EXITF*POSSET/ provides an exit if upon entry the Position Settle signal from the disk is not true.

EXITF*DTOT2F provides an exit if the address cannot be found in one and a half revolutions of the disk.

The Exit Flip-Flop may be set at Status Count 10 if the operation is not a pause and the Position Settle (POSSET/) signal is false, if the operation is a write and the write lockout signal is true (WR.LKT=WROP* WRLKOT), if the operation is a Test OP or if the Unit is not present (PRES/).

Exit to Status Count 11 if the operation is a read and the Buffer Ready signal is true indicating that at least one buffer has data for the Processor.

If the Exit Flip-Flop is set, exit is provided to STC18 under the following conditions:

1. EXITF*RDOP/ indicates the operation is a Pause, Test or Write with the Lockout signal true.

2. EXITF*PRES/ indicates the unit selected is not present.

3. EXITF*FLOPNL/ indicates the Disk is not operational due to a disk not inserted, interlock open etc.

4. EXITF*DTOT2F indicates that the location addressed could not be found due an error condition.

5. EXITF*TRKZROF indicates an illegal address or a seek is not complete from a previous operation.

6. EXITF*POSSET/ indicates that upon entry to STC10 the position settle is not true.

STC11

EXCH7-0 ADDMEM1	CHAF*XFERINL
SRF ← 0 STC+1	CHAF*XERINL *REPSCOM

At Status Count 11 with a Transfer In command, Reference Address Byte 1 is read from Address Memory 1 and placed on the Exchange Lines to the Processor.

During Phase B of the Transfer In Command, the Service Request Flip-Flop is reset and the Status Counter upcounted.

STC12

EXCH7-0 ← ADDMEM2	CHAF*XERINL
STC+1	CHAF*XFERINL *REPSCOM

At Status Count 12 with a Transfer In Command, Reference Address Byte 2 is read and placed on the Exchange Lines to the Processor.

During Phase B of the cycle, the Status Count is upcounted and status returned to the Processor in the normal manner.

STC13

EXCH7-0 ADDMEM3	CHAF*XFERINL
STC ← 15	CHAF*XFERINL *REPSCOM*RDOP
STC+1	CHAF*XFERINL *REPSCOM*WROP

Reference Address Byte 3 is read and sent to the Processor.

If the operation is a Read OP, exit to Status Count 15 to send data to the Processor.

If the operation is a Write OP, exit to Status Count 14 to load a buffer with data from the processor.

STC14

INLATCH ← EXH0-15	COMACT*CHANHI *XFROTA*TERMF/
STC+2	CHAF*XFROTAL *WROP*IN88 *REPSCOM
STC ← 07	CHAF*REPSCOM*TERMF
OUTLATCH ← MOS	DUMPN*P3N

During a write operation, 16 bits of data are transferred from the processor and placed into the Input Latch for the MOS Shift Register for storage. (Refer to STCNY+SCNY logic at load time for description of the load sequence)

At this time the 89th word has just been received by the control. The IN Counter is equal to 88 and has not been upcounted to 89 until the data is stored in the MOS Shift Register. Exit to STC16 to receive the last word (two bytes).

While loading the buffers for a disk write at STC14, if a Terminate Command is received exit to Status Count 7 to receive the Reference Address.

STC15

OUTREG ← MOSN0-15	DUMPN*DSET/*P3N

With the buffer dump term true and a clock from the clock generator, take the output of the MOS Shift Register and store it in the Output Register.

STC15 (Continued)

EXCH0-15 ← OUTREG	DUMPN*XFERINL*CHAF	With a Transfer in Command from the processor, place the data on the Exchange Lines at Phase B time.
STC+1	CHAF*RDOP*XFERINL *REPSCOM*OUT88	Exit to Status Count 16 to send last word (two bytes) to the Processor for a Read OP.
STC ← 21	CHAF*REPSCOM *TERM*RDOP	If a Terminate Command is received for the Read OP, exit to Status Count 21 to send the result status word byte 1.

STC16

EXCH0-15 ← OUTREG	DUMPN*XFERINL*CHAF	The last word is read from the MOS Shift Register with a Transfer In and sent to the Processor via the Exchange.
OUTREG ← MOSN0-15	DSET/*P3N	
INREG ← EXCH15-0	COMACT*CHANHI *XFROTA*TERMF/	During a Write OP, the last word is loaded into the MOS Shift Register at this time. With the Transfer Out Command from the Processor, store the last word in the INPUT Register.
STC← 07	CHAF*XFERINL*RDOP REPSCOM*TERMF/	Having emptied a buffer for a Read OP if a terminate command has not been received, exit to Status Count 7 to receive the Reference Address.
STC ← 21	CHAF*RDOP*TERMF *REPSCOM	If a Terminate Command is received, exit to Status Count 21 as the Processor has received all the data from the disk required.
STC ← 07	CHAF*REPSCOM*WROP *(XFROTAL+TERMF)	On a Disk Write OP if a Terminate or Transfer Out Command is received at this time, exit to Status Count 7 to load the Reference Address.

STC18

EXCH7-0 ← ADDMEM1	CHAF*XFERINL	Send Reference Address Byte 1 to the Processor with a Transfer In Command.
SRF ← 0 STC+1	CHAF*REPSCOM*XFERINL	Reset the Service Request and exit to Status Count 19 to send Reference Address Byte 2.

STC19

EXCH7-0 ← ADDMEM2	CHAF*XFERINL	Reference Address Byte 2 is read from the Address Memory and sent to the Processor with a Transfer In Command.
STC+1	CHAF*REPSCOM*XFERINL	Upcount the Status Count to 20 in order to exit and send Reference Address Byte 3.

STC20

EXCH7-0 ← ADDMEM3	CHAF*XFERINL	Reference Address Byte 3 is read from Address Memory and sent to the Processor with a Transfer In Command.
STC+1	CHAF*REPSCOM*XFERINL	Set the Status Count to 21 in order to send the Result Status byte 1 to the Processor.

STC21

EXCH07 ← 1	CHAF*XFERINL	Set the Operation Complete Bit with a Transfer In Command from the Processor.
EXCPBIT	FLOPNL/+DPEF+WRLKOT *(TEST+WROP)+PRES/ +DTOT2F+TRKZROF +(SKSTSN*TEST)	Set the Exception Bit flag to cause the exception bit to be returned to the Processor.
EXCH06 ← 1	EXCPBIT*CHAF*XFERINL	Send the Exception Bit with a Transfer In Command from the Processor.
EXCH05 ← 1	FLOPNL/*CHAF*XFERINL	If the Unit is not ready as indicated by File Operational Level (FLOPNL/) being false, send the Not Ready bit.
EXCH04 ← 1	DPEF*CHAF*XFERINL	If the Disk Parity Error Flip-Flop (DPEF) is set due to a read error from disk, set the Read Error bit.
EXCH01 ← 1	WRLKOT*(WROP+TEST) *CHAF*XFERINL	If the Disk is write locked out, send the condition in the result status if the OP is a Test or Write.
STC+1	CHAF*XFERINL*REPSCOM	Exit to STC22 to send Byte 2 of the Result Status word.

STC22

EXCH06 ← 1	PRES	If the disk unit selected is present, return the present bit.
EXCH04 ← 1	(DTOT2F+TRKZROF) *CHAF*XFERINL	If the address could not be found (DTOT2F) or if the address was illegal or a seek in progress (TRKZROF) then set EXCH04.
EXCH03 ← 1	POS.SET*TEST *CHAF*XFERINL	If the operation is a TEST and the Position Settle signal (POS.SET) is true then the seek is complete.
EXCH01 ← 1	SKSTSN*TEST *CHAF*XFERINL	With a Test Op and the SKSTSN (Seek Status) set, the seek is not complete therefore, set the seeking bit of the Result Status.
STC+1	CHAF*XFERINL*REPSCOM	Upcount the Status to 23 with the Transfer In Command at Phase B time.

STC23

EXCH07 ← 1	CHAF*PAUSE/ *(TEST+TEST/* SKSTSNF/) *(POSETF+DTOT2F+ TERMF*RDOP)+FL.OP/) *XFERINL	Bit 17 is set except when seeking or when a Pause OP.
EXCH04 ← 1 EXCH03 ← 1 EXCH02 ← 1	CHAF*XFERINL*TEST	If the OP is a TEST, sent the Control I/D (001110) to the Processor.
CLRCHN ← 1	CHAF*XFERINL*REPSCOM	Clear the control in preparation of a new operation. Status Count is returned to zero.

SC=00

CYL=F ← 1 REDNF ← 0		Initialize Cylinder Equal and Read Enable Flip-Flops.
ADF ← 1	STC10	When Status Count 10 is reached set the Address Flip-Flop in preparation for a disk operation. ADF is used for a WRITE-OP at Sequence Count 01 to decrement the sector address in the FAR Register by 1.
SC+1	SC ← 1	The Sequence Count replaced by one (SC ← 1) logic is enabled at STC10 if the operation is not a TEST-OP or if Track Zero Flip-Flop is set indicating a previous illegal address or seek incomplete and Position Settle is now true or a PAUSE OP has been sent by the Processor.
SKCTR ← 0	POS.SET*SKCTR=7	If the Seek Counter has been counted by a previous seek operation and the seek is complete at indicated by Position Settle, reset the Seek Counter in preparation for the new operation.
POSETF/ ← 1	POS.SET/	If the Position Settle Level is false, set the Position Settle Not Flip-Flop (POSSETF/).

SC=01

FSFF ← 1		If a disk write is to occur the First 'Sector Flip-Flop will be used at SC=06 to upcount the Sector address. The address would have been previously decremented and therefore the increment at SC=06 would restore the address to the original state.
SECREG-1	WRITE*ADF	If a write operation is to occur, the sector portion of the File Address is decremented by one. This is required in order to find sector coincidence one sector prior to the actual sector to be written in order to allow a correct amount of head switching time from read to write.

SC=01 (Continued)

ADF ← 0	ADF	ADF is reset to prevent further decrementing of the Sector Register.
SKCTR+1	1USB*SKCTR≠7 *(WR.INX+RD.INX +TRKZROF*PAUSE/)	If the Seek Counter is not at a count of seven and the operation is a Write Index, Read Index or if it is not a Pause OP and Track Zero Flip-Flop is set, upcount the Seek Counter by one with each one micro-second clock. Track Zero (TRKZROF) would be set if a previous seek was not complete. If teh address was illegal a seek would be executed for cylinder zero as TRKZROF will cause the FAR Register to be cleared.
SEEK.EX	SKCTR=2	With the Seek Counter equal to two send a seek execute command to the disk.
EXITF ← 1	TRKZROF*SKCTR=7 +WRITE*TERMF*BUFSEMP *INCTR=0*JUST1F/ +RDOP*TERMF	Set the Exit Flip-Flop with Track Zero and Seek Counter equal to seven which indicates a seek has been initiated. WRITE*TERMF*BUFSEMP cause an exit for a write operation with a terminate command received and all buffers are empty. RDOP*TERMF causes an exit for a read operation and a Terminate Command is received. EXITF will cause the Sequence Counter to be set to SC=00.
SC ← 03	PAUSE+TRKZROF/ *(RD.INX*SKCTR=7 +READ+RD.IMM +WRITE*BUFRDY)	Exit to SC=03 for a PAUSE-OP, READ INDEX and a seek has been initiated, READ-OP, READ IMMEDIATE or a Write-OP and a buffer is ready with data to be written.
SC ← 05	TRKZROF/*BUFRDY *(WR.INX*SKCTR=7 +WR.IMM)	Exit to Sequence Count 5 if a buffer is ready and the OP is a Write Index with the seek having been initiated or if the OP is a Write Immediate.
INCF 0 POSETF/ 1	INCF POS.SET/	If the Position Settle Load is false, set the Position Not Settled Flip-Flop.

SC=02

BITR+1		The control is in synchronization with the Disk Read Clock at SC=02 and therefore with each disk clock, the Bit Ring Counter is counted by one (BITR+1) for each bit from the disk.
SR1IN ← RD-D SR1(N+1) ← SR1(N)	BITR8F/	The first eight bits of a word are received with Bit Ring Eight F/F reset (BITR8F/) and subsequently the Read Data is placed in SR1 which is in a shift up mode at that time in order to accumulate the bit serial read data from the disk.

SC=02 (Continued)

SR2IN ← RD-D SR2(N+1) ← SR2(N)	BITR8F	The second eight bits of the word are received with BITR8F which will allow the data to be read into SR2 and places SR2 in a shift up mode to receive the bit serial data read from the disk.
DATAF	BITR=15	The Data Flip-Flop is set with the first word received at SC=02 in order to allow the Shift clock to be generated to start storing the data in one of the MOS Shift Registers.
INLATCH8-15 ← SR1	BITR=8	With Bit Ring equal to eight, one byte (½ word) has been received and is transferred to the input latches of the MOS Shift Register.
INLATCH0-7 ← SR2	BITR=1	With Bit Ring equal to one, the second byte of the word has been received and is ready to be transferred to the input latches of the MOS Shift Register.
BLKCT2 ← 0	SECP	If an exit does not occur after the first sector, with the next sector pulse, clear the Blank Count 2 Flip-Flop.
EXITF ← 1	BUFSFLF+RDOP* TERMF	Set the Exit Flip-Flop if the buffers are full or if a Terminate Command is received.

SC=03

INXSYN ← 1	INXP*DISK CLOCK *POSSET	With an Index Pulse from the disk and a system clock, set the Index Sync Flip-Flop to synchronize the index time to the clock.
INXF ← 1 INXSYN←0	INXSYN	If the Position Settle signal is true along with Index Sync, set the Index Flip-Flop.
SECF ← 1	SECP*POS.SET* (RD.INX/+INXF)	The Sector Flip-Flop is set with a Sector Pulse from the disk provided the operation is not a Read INdex or if the Index Flip-Flop is set.
RTMR+1	(PAUSE*1024USB) +(PAUSE/*4USB* SRTBKF/*(SECF +RTMR≠0))+ (SRTBKF*BLKCT2/ *32USB)	The Read Timer is upcounted by one for the following conditions: 1. If the OP is a Pause then the Read Timer is used with each 1024 USB in order to cause a Pause of approximately 8 milliseconds. Exit occurs at RTMR=7. 2. If the OP is not a Pause then the Read Timer is upcounted by one with each 4USB provided the Start Blank Flip-Flop is not set. The count is started by a sector pulse (beginning of sector) and continued by the RTMR≠0 term. The counting of RTMR at this time is to insert an approximate delay of 25usec before sending Read Enable to the disk which is a requirement made by the disk. 28-32 suec delay.

SC=03 (Continued)

RTMRCO	RTMR=7*SRTBKF/ *4USB*PAUSE/
RTMR ← 3 SRTBLKF ← 1	RTMRCO
INXF ← 0 SECF ← 0	RTMR≠0
RDENF ← 1	RTMR=7*SRTBKF/
BLKCT2	SRTBLKF*RTMR=7
SRTBLKF ← 0	SECP
DSETCOM	SYNCF/
DSET2F ← 0	DSETCOM
DSET1F ← 1	DSETCOM*DSET2F/
D.SET	COMACT/*CHAF/ *DSET1F*DSET2F/

3. When the initial delay of 25usec has been inserted, the Start Blank Flip-Flop will set and the Read Timer jammed to a count of three. With this, the Read Timer will be upcounted until it reaches a count of seven at which time the term BLKCT2 will be true to cause the count to terminate. Counting was done every 32 micro seconds with 32USB. This further delay is to prevent the control from looking at data from the disk during the blank data time of the preamble. Delay is 64 to 96 micro seconds.

With the Read Timer equal to seven and the mode line (add) true as indicated by SRTBKF/*4USB*PAUSE/, the Read Timer Carry Out term is true.

With Read Timer Carry Out true, the logic is true to jam the read timer to a count of three and to set the Start Blank Flip-Flop.

With the Read Timer not equal to zero, reset the Index and Sector Flip-Flops.

Set the Read Enable Flip-Flop the first time the Read Timer reaches a count of seven.

The second time the Read Timer reaches a count of seven the Start Blank Flip-Flop will have been set and therefore the term Blank Count 2 will be true to prevent further counting of the Read Timer and allow the control to enter SC=RD.

With the next sector pulse, reset the Start Blank Flip-Flop which will enable a new timer sequence for the next sector.

"D" SET CONTROL MODE is true if a sync character has not been previously detected. The sequence of the following "D" Set Flip-Flops is to allow the address contained in FAR to be placed in the SR Register where a compare will occur for the addresses read from disk. The timing of the "D" Set terms is necessary so that the transfer will not allow data from the MOS Buffers to be on the SR input lines at the same time.

If DSETCOM is true then reset DSET2F.

Set DSET1F is a sync character has not been detected.

If Command Active is not true and Channel Active is not true with the sync character not yet found, D.SET is true to place the address in the SR1 and SR2 Registers.

SC=03 (Continued)

SR1 ← CYL9-3F SR2 ← CYL2-1F SR2 ← HEADF SR2 ← SEC5-1F DSET2F ← 1	D.SET
DSET1F ← 0	DSET2F
LDSETN ← 1	ADDRF*LOADN
LDSETN ← 0	SECP
EXITF ← 1	(RTMR=4*PAUSE +DTOT2F) +(RDOP*TERMF)
SC=RD	BLKCT2
POSETF/ ← 1	POS.SET/

With D.SET, place the address into SR1 and SR2 and set the DSET2 Flip-Flop.

Reset DSET1 with DSET2F true.

The above sequence will occur continually at SC=03 until the sync character is found at which time DSETCOM will be made false.

LOAD SET for Buffer "N" is made true with the Address Flip-Flop set and a buffer to be loaded. LDSETN is used at SC=04 only and will be used to set the Disk Parity Error Flip-Flop if a read error occurs on data from the disk.

The next sector pulse to occur will reset the Load Set Flip-Flop.

The Exit Flip-Flop is set for a Pause OP completed, timeout which indicates the address count not be found in the required time or if the OP is a Read and a Terminate Command is received. Setting the Exit Flip-Flop returns the SC to 00.

When the Blank Counter is equal to two which indicates that the required delays which were accomplished by the Read Timer counting, have been made then Sequence Count Read is entered to read the address from disk to determine address coincidence. SC=RD is a sub-state of SC=03.

If the Position Settle Lead is false, set the Position Settle Not F/F.

SC=RD

SC ← 2	RD.IMM+RD.INX
CCR ← RD-D	
CCR(N+1)-CCR(N)	SYNCF/

If the operation is a Read Immediate or Read Index then a search for address coincidence is not required and therefore the Sequence Count is set to two in order to begin reading.

Read Data from disk is placed in the least significant bit position of the Cyclic Check Register as the CCR will be used to compare for a sync character.

As long as the sync character is not detected, shift the contents of CCR up one position with each data bit and clock from the disk.

SC=RD (Continued)

SYNC	CORRECT BIT PATTERN	
SYNCF ← 1	SYNC*SYNCF/	When a sync character (00011110) if found in the CCR Register, the term SYNC is true.
BITR ← 0	SYNC*SYNCF/ +ADDRF*COMP≠	With the sync character found, set the SYNC Flip-Flop.
WDCT ← 91	SYNC*SYNCF/	When the sync character is found, clear the bit ring counter or in the address mode if a compare of bits is false then clear BITR. BITR will be used to count the bits per word wwhich are read from disk or written to disk.
CCR ← 0	SYNC*SYNCF/ +SECF	Word Counter is set to 91 in order to count the 91 words (1 address word and 90 data words) read from disk.
ADDRF ← 1	SYNC*SYNCF/	The CCR Register is cleared with the sync pattern in order to start building a CCR character of the data read from disk in order to determine if an error exists. CCR is also cleared at the beginning of a new sector with SECF.
BITR+1	SYNCF	Address Flip-Flop is set when the sync pattern is found and will allow comparison of data from disk (addresses) in order to determine address coincidence.
COMP.A ← RD-D COMP.B ← SR-B	ADDRF	With the Sync Flip-Flop set, each disk clock received will upcount the Bit Ring plus one.
SR-B ← SR1 SR1(N+1) ← SR1(N)	ADDRF*BITR8F/	With the Address Flip-Flop set, the Read Data Bit is sent to Comparitor A and the corresponding address bit which is contained in SR is sent to Comparitor B.
SR-B ← SR2 SR2(N+1) ← SR2(N)	ADDRF*BITR8F	With the Bit Ring 8 Flip-Flop reset, data from SR1 is used as SR-B data and with each disk clock, the contents of SR1 are shifted up.
WDCT-1	BITR=15*SYNCF	With the Bit Ring 8 Flip-Flop set, data from SR2 is used as SR-B data and with each disk clock, the contents of SR1 are shifted up.
ADDRF ← 0	WDCT=91 *BITR=15 +ADDRF*COMP≠	With the Bit Ring equal to 15 indicating 16 bits have been read, down count the Word Counter by one. The Address Flip-Flop is reset at the end of the address as indicated by the logic WDCT=91*BITR=15. With ADDRF set and if any bit in the address does not compare, reset the Address Flip-Flop.
DATAF ← 1	READ*WDCT=91 *COMP=*SYNCF *BITR=15	If the address compares then the DATA Flip-Flop is set to enter the data mode.

SC=RD (Continued)

SKSTNF ← 0	(READ*WDCT=91 *BITR=15 *SYNCF*COMP= +TERMF)	Reset the Seek Status Flip-Flop if a compare occurs indicating a seek is not going to occur or reset Seek Status if a terminate is received at this time.
CYL=F ← 0	COMP≠*ADDRF *(BITR8F/ +BITR8F* BITR4F/ *BITR2F/)	Reset the Cylinder Equal Flip-Flop if the cylinder address does not compare. Cylinder portion occurs for the most significant six bits of the cylinder address with BITR8/ and the least significant two bits are read with BITR=8 and BITR=9, thus the logic BITR8F*BITR4F/*BITR2F/.
SYNCF ← 0 WDGT ← 0 ADDRF	COMP≠*ADDRF+SLIP	The Sync Flip-Flop is reset if a compare did not occur or if the buffers become full and another sector is to be read.
SLIP ← 1	+TERMF/ *BUFSFLF *BITR=15 *WDCT91 *COMP= *SYNCF *READ	SLIP is true if all buffers are full and Disk Read is still enabled. Allows processor to empty a buffer and pick disk data back up.
RDENF ← 0	COMP≠*ADDRF +SECF	Read Enable is reset if a compare does not exist or at the beginning of the next sector.
SKSTSNF ← 1	CYL=F/	If the Cylinder Equal Flip-Flop is not set, then set the Seek Status Flip-Flop which has the function of reporting a seek operation at Result Descriptor store time.
SKCTR+1	(SKSTNF/ *CYL≠F/ +SKCTR=0 *1USB *SKCT≠7)	Start the Seek Counter with Cylinder not equal and continue counting it with each 1 micro second clock as long as it is not at a count of seven.
SEEK.EX	SKCTR=2	With the Seek Counter equal to two, send a Seek Execute command to the disk which will cause the address in the control to be sent and start a seek operation.
SKCTR ← 0	SKCTR=7 *POS.SET	If at a count of seven Position Settle is true, clear the Seek Counter.
FAR+1 ADF ← 0	ADF	If SC=03 and SC=RD was entered from SC=04 which indicates a previous sector read, upcount FAR+1 (File Address) and reset ADF.
BLKCT2 ← 0	SECP*PAUSE/	The Sector pulse which occurs will clear the Read Timer and thus the term BLKCT2 will go false.
DTOT+1	INXSYN*POS.SET	Disk Time-out timer is counted by one with each index pulse received from disk.

SC=RD (Continued)

DTOT2F ← 1	DTOT=4
EXITF ← 1	SKSTNF *HEADFF/ *SKCTR=7 +DT0T2F
CYL=F ← 1	SKCTR=7
SC ← 04	READ*WDCT=90
SC ← 06 HEADFF ← 0 ADF ← 1	WRITE*WDCT90
HEADFF	

If four index pulses have been counted, set DTOT2F to terminate the search for the address and thus complete the operation.

SET the EXITF if the Cylinder Address did not compare and a seek has been executed. This is done provided the seek is not from a previous operation which requires a seek from one cylinder to the next. EXITF is set for a timeout error or if a terminate is received.

Exit to Sequence Count 04 to read disk if the address has compared.

Exit to Sequence Count 06 to write disk if the address has compared and reset the Head Flip-Flop if set.

The Head Flip-Flop is set so that when a sector is completed and the control returns to SC=03 to read the next address, if the cylinder address does not compare an exit will not occur. A seek to the next track is executed and the control does not exit but in this one case will wait for the seek to complete and thus continue the read operation.

SC=04

BITR+1	SYNCF
SR1IN ← RD-D	DATAF* BITR8F/
SR1(N+1) ← SR1(N)	
SR2IN ← RD-D	DATAF*BITR8F
SR2(N+1) ← SR2(N)	
CCR ← RD-D ⊕ CCR7F	BLKCT2
CCR(N+1) ← CCR(N)	(READ*SYNCF *ADDRF/) +(SYNCF/ *BLKCT2)

At SC=04 the control is still using the disk read clock and therefore each time a clock is received, with SYNCF set, the Bit Ring counter is upcounted by one.

Bit serial read data is placed in SR1 as long as Bit Ring 8 is reset indicating byte 1 of the word is being read

Shift the data in SR1 up with DATAF set and BITR8F/.

Shift the bit serial read data into SR2 with BITR8F.

Shift up the data in SR2 with each bit received.

Read Data is exclusive or'd with CCR7F and placed in the CCR Register least significant portion. This is done to build an LP Character to compare with the character written on disk.

Shift data up in the CCR Register as long as SYNCF is set.

CCR is shifted up at this time in order to clear the data contained as the control will go back to SC=03 to obtain a sync character in the CCR. Data input at these shift times is inhibited.

SC=04 (Continued)

WDCT-1	BITR=15 *DATAF	Each time the Bit Ring reaches a count of fifteen, decrement the Word Counter.
DATAF ← 0	WDCT=1 *BITR=15	With the last bit having been received, reset the data flip-flop which will allow the CCR Character to be read.
FSFF ← 0	WDCT=1	If this was the first sector, then with Word Count equal one, reset the first sector flip-flop which if not the first sector would have been previously reset.
COMP.A ← RD-D COMP.B ← CCR7F	DATAF/ *SYNCF	Set the Read Data bit to Comparitor A and the CCR7 output to Comparitor B for a bit by bit compare.
SYNCF ← 0	DATAF/*BITR7	Reset the Sync Flip-Flop having received the CCR (Parity) Character.
ADF ← 1	SYNCF/	Set ADF at the end of the read which will allow the control to exit to SC=03 and at SC=03 it will be used to upcount the File Address Register.
DPENF ← 1	LDSETN*ERR	If an error occurs on the read of a segment (CCR not correct) then Disk Parity Error for the buffer that has been loaded is set. LDSETN was made true for the buffer to be loaded as SC=03.
DPEF ← 1	DPENF*DUMPN	The Disk Parity Flip-Flop which is used to indicate a parity error is set only if the buffer that is dumped contains a parity error.
SC ← 03	ADF	Exit to SC=03 to insert delays and look for sector coincidence for the next sector to be read and/or initiate a seek if required.
EXITF ← 1	RDOP*TERMF	If a Terminate Command is received, set the Exit Flip-Flop.

SC=05

SECF ← 1	SECP*(WR.IMM+INXF *WR.INX)	The Sector Flip-Flop is set at this time to start the Write Immediate or Write Index operation.
INXF ← 1	INXSYN	Index Flip-Flop is set with an Index Pulse received from the disk provided the Position Settle signal line is also true.
INXDF ← 1	SECF*SECP/*(WR.IMM +WR.INX*INXF)	With the Sector Flip-Flop set and the Sector Pulse no longer true, the Indexed Flip-Flop is set. (Functions of INXDF are described under INXDF flows)
SECF ← 0	INXDF	With the logic true to cause a set of INXDF, the clock that occurs will reset the Sector Flip-Flop.

SC=05 (Continued)

INXF ← 0	INXDF*INXP/	The synchronized INXF is reset at this time.
OUTN015 ← MOSN015	DUMPN*P3N	The output of the MOS Shift Register is parallel gated to the Output Register.
SR1 ← OUTLTCH8-15	INXDF *DUMPN	With the logic true to allow the INXDF to set, set the first character to be written onto disk into Shift Register 1. Subsequent characters are loaded with INXDF set. (See INXDF flows).
SHIFTON	BT2SYNF*DUMPN	Shift OUT Buffer "N" is set to cause a shift of the data in the Shift Register with the Bit Ring counter equal to two and Dump "N" true.
SKCTR ← 0	POS.SET*SKCTR=7	The Seek Counter is reset with Position settle and Seek Counter as the maximum count.
EXITF ← 1	SECF*DATAF	Exit Flip-Flop is set at the end of one sector to terminate the operation.
INXSYN ← 1	INXP*POS.SET*DISK CLOCK	INDEX SYNC Flip-Flop is set with the Index Pulse to synchronize the Index pulse to system clock.
INXSYN ← 0	INXSYN	After one clock time, reset the Index Sync Flip-Flop. Reset Pulse+F/ if set.
POSETF/← 0		
WRENF ← 1	DATAF	Data Flip-Flop is set to enter the data mode of the Write Index or Write Immediate operation. DATAF will allow Write Enable to set. Write Enable is set with DATAF and allows the write clock to be enabled in the disk.
WR-D ← SR-B BITR+1 DATAF ← 1	INXDF	Control is now in sync with disk clock. With each clock received, send a write data bit and upcount the Bit Ring Counter.
SR-B ← SR1 SR1(N+1) ← SR(N)	BITR8F/*INXDF	With Bit Ring Eight Flip-Flop reset, the contents of SR1 is sent to the Shift Register Bus and shifted up with each disk write clock.
SR-B ← SR2 SR2(N+1) ← SR2(N)	BITR8F*INXDF	With Bit Ring Eight Flip-Flop set, the contents of SR2 is sent to the Shift Register Bus and shifted up with each disk write clock.
SR1 ← OUTLTCH8-15	BITR=12*DUMPN *INXDF	With Bit Ring Equal to twelve, the contents of SR2 is being written onto disk thus SR1 may be loaded with a new byte.
SR2 ← OUTLTCH0-7	BITR=1*DUMPN *INXDF	With Bit Ring equal to one, the contents of SR1 is being written onto disk thus, SR2 may be loaded with a new byte.

SC=05 (Continued)

INXDF ← 0 WRENF ← 0	SECP	The next Sector Pulse resets INXDF and WRENF to terminate the write operation.

SC=06

RDENF ← 0 WRENF ← 1 CYL=F ← 0	SECF	The Control waits at SC=06 for the first sector pulse which will reset Read Enable and set Write Enable. Cylinder Equal Flip-Flop is reset.
SYNCF ← 0	CYL=F*SECF/	On initial entry to SC=06, the Sync Flip-Flop is reset as it is no longer required.
SECF ← 1	SECP	With a sector pulse from disk, set the Sector Flip-Flop.
SECR+1	ADF*FSFF	With ADF and First Sector Flip-Flop upcount the Sector Address portion of FAR. This is done as on the disk write the Sector Address was decremented in order to find the sector prior to the first sector to be written. At this time the Sector address is restored to the original value.
FAR+1	ADF*FSFF/	At the end of a sector, ADF is set and with FSFF/ the File Address Register is upcounted in order to keep synchronized with the address that is to be written.
ADF ← 0	ADF	ADF is reset after one clock period.
ADRF ← 1 WDCT ← 108 BITR ← 0 SYNCF ← 1	SECF*SYNCF/	At the beginning of the disk write operation, set the Word Counter to 108 which is the number of words to be written. 180 data bytes 2 address bytes 33 preamble bytes 1 sync byte 216 total bytes or 108 words ADDRF is set and will be used to write the Longitudinal (Cyclic Check Character) Parity Character at the appropriate time. SYNCF is set and will enable the counting of the Bit Ring counter with each disk write clock.
COMP1	LOADN=DUMPN *BUFRDY/	Compare 1 is true if the buffer to be loaded is equal to the buffer being dumped with Buffer Ready Not. This indicates the buffers are emtpy.
COMPF ← 1	COMP1*DATAF*TERMF	Set the compare flip-flop if the buffers have been emptied and a Terminate Command has been received. COMPF is used to exit the operation.
BITR+1	SYNCF	With SYNCF set, each disk clock will allow the Bit Ring Counter to be upcounted.

SC=06 (Continued)

WDCT-1	BITR=15*SYNCF *WDCT≠1	Each time the Bit Ring Counter reaches a count of 15 indicating a word has been written, decrement the word counter.
CCR ← SYNC	WDCT=92*BITR=2	The sync character (00011110) will be written on disk starting at WDCT92 and Bit Ring 8 Flip-Flop set, therefore set the sync character in the CCR Register from where it will be sent as write data at the appropriate time.
SR1 ← CYL9-3F SR2 ← CYL2-1F SR2 HEADF SR2 SEC5-1F	D.SET	Load the address in FAR which is to be written onto disk into the Shift Registers. D.SET is a result of a sequence to allow FAR to the input of SR without the data being received from the processor interferring.
DSETCOM	SECF	With SECF true "D" SET CONTROL MODE is made true.
DSET1F ← 1	DSETCOM*DSET2F/	DSET1F is set with DSETCOM true and DSET2F/.
D.SET	COMACT/*DSET1F *DSET2F/*CHAF/	With a command not on the exchange and the channel not active, D.SET is made true to transfer the address from FAR to the Shift Register.
DSET2F ← 1	D.SET	Set DSET2F to prevent a double transfer.
DSET1F ← 0	DSET2F	Reset DSET1F with DSET2F.
DSET2F ← 0	DSETCOM	Reset DSET2F.
SECF ← 0	WDCT=92	When the Word Counter has been decremented to a count of 92, reset the Sector Flip-Flop.
WR-D ← CCR7F CCR(N+1) ← CCR(N)	WDCT=92*BITR8F +SYNCF*ADDRF/	The CCR Register is used to supply Write data and is shifted with the disk clock. WDCT=92*BITR8F will find the sync character in CCR to be written and SYNCF*ADDRF/ will allow the CCR (LPC) to be written.
DATAF ← 1	WDCT=91*BITR=15	Starting at a Word Count of 90 the 180 bytes of data is to be written therefor DATAF is set to gate data from the MOS Shift Register as write information.
WR-D ← SR-B	DATAF+WDCT=91	Contents of SR is write data with DATAF set or at WDCT=91 to write the address word (two bytes).
CCR ← SR-B ⊕ CCR7F	DATAF	The Shift Register Bus is exclusive or'd with CCR7F to for the CCR character to be written at the end of the sector.
CCR(N+1) ← CCR(N)	DATAF+BITR8F *WDCT=92	CCR Register is shifted up with each disk clock. Shifting is done with DATA in order to accumulate the CCR Character. Shifting is done at WDCT=92* BITR8F to allow the sync character to be written.

SC=06 (Continued)

SR-B ← SR1 SR1(N+1) ← SR1(N)	BITR8F/*(WDCT=91 +DATAF)	Shift Register Bus is the contents of SR1 with the Word Counter equal to 91 with BITR8F/ which is the time the first byte of the address is written. With DATAF*BITR8F/ the byte to be written of the 180 byte sector is from SR1. Each disk clock allows the contents of SR1 to be shifted up.
SR-B ← SR2 SR2(N+1) ← SR2(N)	BITR8F*(WDCT=91 +DATAF)	Shift Register Bus in the contents of SR2 with the Word Counter equal to 91 and BITR8F/ which is the time the second byte of the address is written. With DATAF*BITR8F, the byte of data to be written is contained in SR2. Each disk clock allows the contents of SR2 to be shifted up at this time.
DATAF ← 0 ADDRF ← 0	WDCT=1*BITR=15 *SYNCF	The last data bit is being written on disk of the 180 bytes of data; reset Data Flip-Flop and Address Flip-Flop which will allow the CCR to be written as the next character.
SYNCF ← 0	ADDRF/*BITR=7 *SYNCF	Sync Flip-Flop is reset after the CCR Character has been written and inhibits further counting of the Bit Ring Counter and decrementing of the Word Counter.
FSFF ← 0	WDCT=91	When the Word Counter reached a count of 91 the First Sector Flip-Flop reset as its function of restoring the Sector Counter had been performed.
ADF ← 1	WDCT=1*SYNCF/ *FSFF/	ADF is set in order to upcount the File Address Register at the end of the sector write and to set INCF.
EXITF ← 1	SECF*COMPF*SYNCF/	The Exit Flip-Flop is set to end the operation after the sector has been completed and all buffers
SR1 ← OUTLTCH8-15	BITR=12*(DATAF +WDCT=91)	While SR2 is being shifted onto disk at Bit Ring 8 through 15, SR1 is loaded with a new byte of data or at Word Count 91 is loaded with an address byte.
SR2 ← OUTLTCH0-7	BITR=1*DATAF	With data being sent to disk from SR1 at Bit Ring 0 thorugh 7, SR2 is loaded with a new byte of data.
SHIFTON	DATAF*BITR=2*DUMPN	Shift is set to allow a shift of the data in the MOS Shift Register which is selected (See SC+STC ANY logic flows for DUMP).
OUTLTCH ← MOSN015	DUMPN*P3N	Output of the Shift Register is sent to the Output Latches at P3 time of the MOS Clock Generator.
CYL=F ← 1	WDCT=1*SYNCF/*SECF/	Cylinder Equal Flip-Flop is set so that if a seek is required, CYL=F will be in its initialized state.

SC=06 (Continued)

HEADFF ← 1	HEADF	If the HEADF portion of the File Address Register is set, set HEADFF to remember HEADF was set so that if the FAR+1 finds HEADF on and a sector address of 31 the required seek to the next track is remembered.
SC ← 1 ADF ← 1	(HEADFF*HEADF/) +(BUFSEMP*TERMF/ *SYNCF/*INCF)	Exit is made to sequence count 1 to allow a seek to the next cylinder with HEADFF*HEADF/ or exit is made if the buffers are empty and a terminate has not been received. This allows a slipped revolution and thus time to fill a buffer with new data. ADF is set to cause a decrement of the sector address as the operation will be regarded as a first sector operation.
WRENF ← 0 BLKCT2 ← 0	SECP	With the next sector pulse, Write Enable is turned off and Blank Count 2 reset.
INCF ← 1	ADF	INCF is set with the ADF which was produced as a result of WDCT=1*SYNCF/*FSFF/.
INCF ← 0	INCF	INCF is set for one clock period only and is reset. INCF is used to allow the logic to exit back to SC=01 if necessary and to set ADF for use at SC=01.
POSETF/ ← 0		Clear POSETF/ if set.

SECTION IV

There are no adjustments for the disk cartridge control.
Refer to I/O Base Section IV for clock adjustments.
Refer to Disk Cartridge Control Section VI for determining the control channel number.
Refer to Disk Cartridge Control Section VI for wiring the configuration chip.

Maintenance Procedures

INTRODUCTION

The purpose of this section is to provide directions and aids in maintaining the Disk Cartridge Control.

PREVENTIVE MAINTENANCE

There is no preventive maintenance for the Disk Cartridge Control. Refer to the B9480-2 Technical Manual for the Disk Drive PM.

SPECIAL MAINTENANCE TOOLS REQUIRED

Disk Cartridge Test Routines
B 1700 Field Card Tester
Tektronix 453A Oscilloscope or equivalent
Tripplet 630 VOM or equivalent

MAINTENANCE CONCEPT

B 1700 controls are soft controls. No offline capability is built into the control. The B 1700 Maintenance concept is centered around the use of test routines used in conjunction with the Field Card Tester. Hardware testpoints are provided for conventional trouble shooting.

TEST ROUTINES

There are two test routines for the disk cartridge control. The first test is basically a confidence routine tape. There are several other features on this tape.

One section of this routine initializes the cartridge. The other sections are for maintenance of the Disk Drive.

The second test tape is called the I/O Debug Routine. This is a MIL program and is much more flexible than the SDL Disk Pack Test listed above. This routine is used for general disk cartridge trouble shooting.

CONFIDENCE ROUTINE

The Disk Cartridge Confidence Routine does the following:

0. Program starts by doing indexed writes and indexed reads. On read back the Read Data is compared with what was written.
1. Program initializes the selected drives cartridge. Note that this section may be used at any time to initialize a new cartridge.
2. Writes Burroughs format of a selected sector length and does a read compare of the data.
3. Does partial segment read and writes, arm movement testing, pause OP test and system interaction test.
4. Dump the selected disk sector to the printer.

The following sections of the Disk Pack Test are for maintenance of the disk drive.

5. Seek a selected cylinder and track address, ignoring exception conditions.
6. Alternate between two selected cylinder addresses.
7. Write or read of a selected cylinder and track address. Compare the data.

HOW TO LOAD DISK CARTRIDGE TEST

1. Place processor in the MTR mode and ready the SPO, Line Printer and Disk Cartridge Drive.
2. Insert Disk Pack Test into the Cassette drive.
3. Depress start.
4. After the Cassette halts, place the processor in the RUN mode and again depress start.

RUN INSTRUCTIONS

1. The Disk Cartridge Routine listing gives run instructions.
2. The SPO prints out special instructions as the program proceeds.

RESULTS

Refer to Test Procedures to analyze the failure.

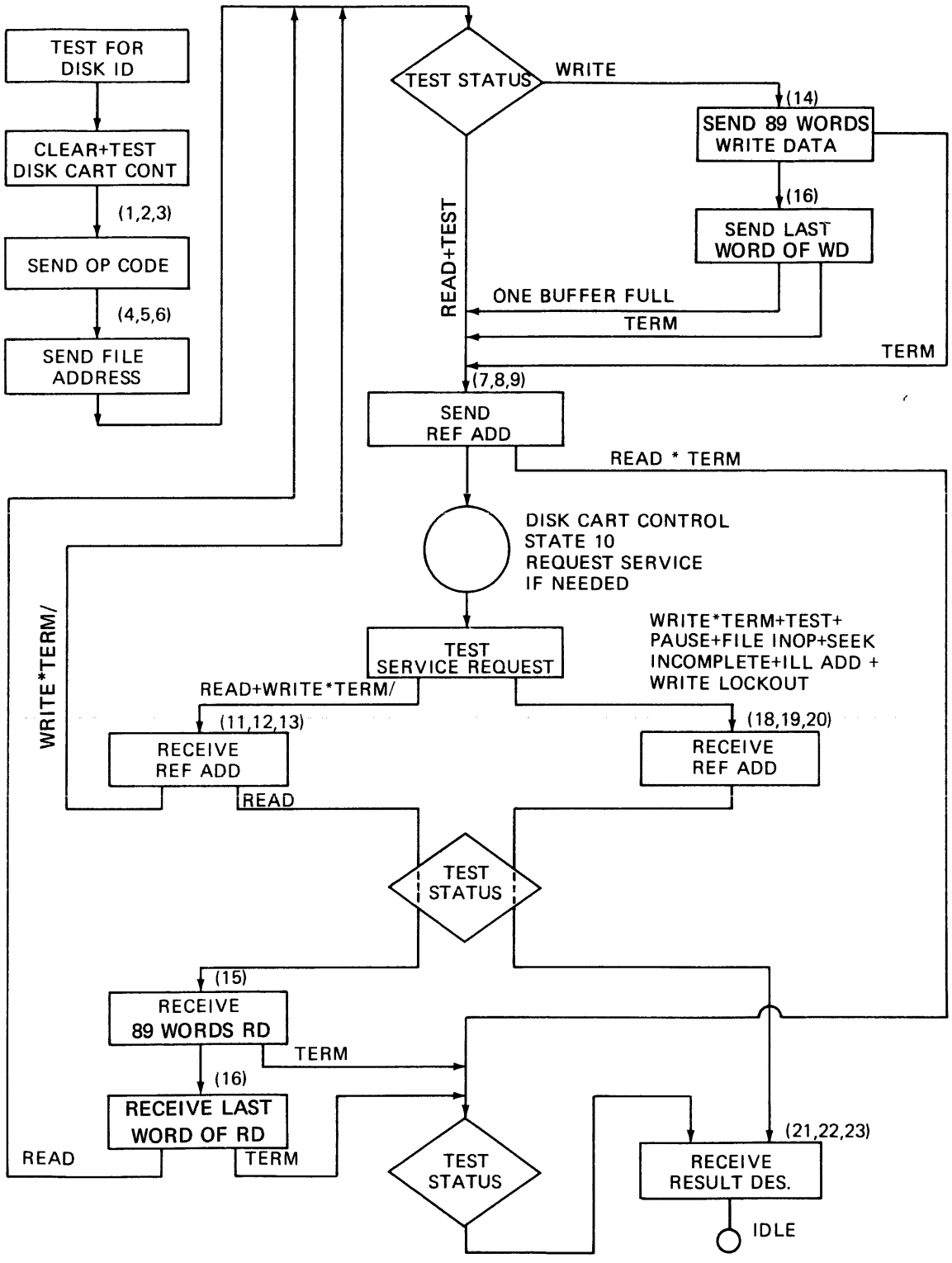


Fig. V-1 PROCESSOR TO DISK CARTRIDGE CONTROL FLOW

I/O DEBUG ROUTINE

GENERAL

This program is a general purpose trouble shooting routine written in MIL. Figure V-1 is a block diagram of the processor to Disk Cartridge Flow. Disk Cartridge Control states are shown in parenthesis. The OP code and control ID have to be loaded into specified registers. In addition for disk the file address is loaded.

This program has several features unique to disk. These are the ability to write index with a sync pattern (used to initialize) and the ability to increment file address by a specified factor.

Instructions for loading the registers, displaying certain registers and selecting program toggles are given in the program listing.

STEPPING

Two means of stepping are provided. If the program toggle step is selected the processor is kept in the run mode and start is depressed. The processor halts with the data sent out to the exchange lines in one register and the data read into another register. This halt occurs for every transfer to the I/O.

The other means of step is obtained by placing the mode switch to step. There are certain levels in the disk control that are true for CA time only. By using this step procedure and the program listing the F.E. can step the control to the proper sequence and observe hardware testpoints.

USING HALTS

The I/O Debug Routine contains a number of No-ops that can be changed to a halt. These locations are placed at subroutine levels to enable the operator to halt after a certain function such as transfer out OP code. Figure V-1 is a relative breakdown of these subroutines. For example, if the reference address was being transferred back to the Processor in error the F.E. could place a halt after the Ref Add is transferred in. He would then check the proper register for the Ref Add.

DATA LENGTH

Refer to Table V-2 for the data length to enter in the FL Register. Table shows the six sections of FL in hex.

TRACE OPTION

This program toggle traces the disk operation on the Line Printer. The trace shows the state of the 24 exchange lines in hex. For each I/O operation the listing gives three sets of states. The first group is at CA time. The second at RC and the third is a status indicator (does not reflect exchange lines). The I/O Debug program, if the trace toggle is selected, does a test at the end of each RC time to determine what state the control went to. This is reported in the third set of figures along with a number showing the count of the operation.

```
100001 01002C 010000  * 110001 000000 010001  * 120001 000000 010002  * 130001 010090 010003  *
140001 000000 010004  * 150001 01001C 010005  * 150003 01001C 010006  * 250080 010000 020007  *
250000 020000 030008  * 250000 030000 040009  * 250000 040000 05000A  * 250000 050000 06000B  *
250000 060000 07000C  * 150001 07001C 07000D  * 250000 070000 08000E  * 250041 080000 09000F  *
250070 090000 120010  * 100005 000020 120011  * 450000 120000 130012  * 450000 130041 140013  *
450000 140070 150014  * 150001 15001C 150015  * 150001 15001C 150016  * 450000 1500F0 160017  *
450000 160050 170018  * 450000 17009C 010019  * 150003 01001C 01001A  *
```

Fig. V-2

I/O Commands in Hex (Channel 0 is assumed)	
Test	100001
Test + Clear	100003
Test SR	100005
Terminate Data	100006
Transfer In	400000
Transfer Out	200000

Table V-1
I/O Commands in Hex

EXAMPLE OF A TEST OP TO DISK
(Refer to Fig. V-1, Fig. V-2 and Table V-1)

Step	Time Period	Exchange Line Decode
0	CA	Test status of channel zero
	RC	SPO responds with ID and status (01)
1	CA	Test status of channel one
	RC	No device is on channel one
2	CA	Test status of channel two
	RC	No device is on channel two
3	CA	Test status of channel three
	RC	Line Printer responds with ID and status (01)
4	CA	Test status of channel four
	RC	No device is on channel four
5	CA	Test status of channel five
	RC	Disk responds with status (01) + ID
6	CA	Clear and Test to Disk (Ch 5)
	RC	Disk responds with status (01) + ID
7	CA	Transfer out 1st byte of OP code to Disk
	RC	Disk responds with status (01)
8	CA	Transfer out 2nd byte of OP Code
	RC	Disk responds with status (02)
9	CA	Transfer out 3rd byte of OP code to Disk
	RC	Disk responds with status (03)

EXAMPLE OF A TEST OP TO DISK (continued)
(Refer to Fig. V-1, Fig. V-2 and Table V-1)

Step	Time Period	Exchange Line Decode
10	CA	Transfer out 1st byte of File Add to Disk
	RC	Disk responds with status (04)
11	CA	Transfer out 2nd byte of File Add
	RC	Disk responds with status (05)
12	CA	Transfer out 3rd byte of File Add
	RC	Disk responds with status (06)
13	CA	Test the State of the Disk
	RC	Disk responds with ID and status (07)
14	CA	Transfer out the Reference Address byte one
	RC	Disk responds with status (07)
15	CA	Transfer out Reference Add byte two
	RC	Disk responds with status (08)
16	CA	Transfer out Reference Add byte three
	RC	Disk responds with status (09)
17	CA	Test Service Request
	RC	Disk responds by tieing exchange 05 true
18	CA	Transfer in command to Disk
	RC	Disk responds with 1st byte of Ref Add and Status (18)
19	CA	Transfer in command to Disk
	RC	Disk responds with 2nd byte of Ref Add and status (19)
20	CA	Transfer in Command to Disk
	RC	Disk responds with 3rd byte of Ref. Add. and Status (20)
21	CA	Test status Command to Disk
	RC	Disk responds with ID and Status (21)
22	CA	Test status Command to Disk
	RC	Disk responds with ID and status (21)
23	CA	Transfer In Command to Disk
	RC	Disk responds with 1st byte of Result Descriptor and status (21)
24	CA	Transfer in Command to Disk
	RC	Disk responds with 2nd byte of Result Descriptor and status (22)
25	CA	Transfer in Command to Disk
	RC	Disk responds with third byte of Result Descriptor and status (23)
26	CA	Clear and Test Command to Disk
	RC	Disk responds with ID and Status (01)

FILE ADDRESS

Figure V-3 shows the values of File Address when loaded into the processor.

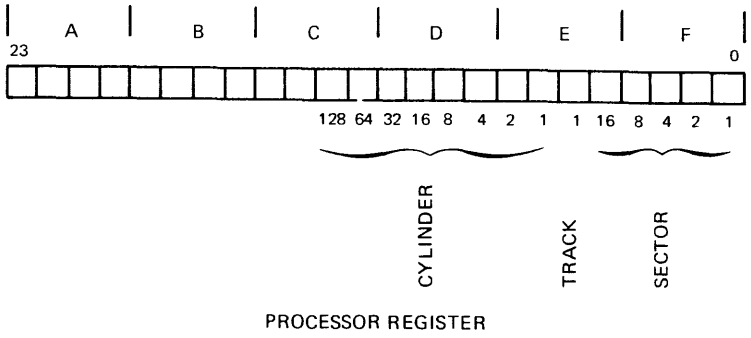


Fig. V-3 FILE ADDRESS LOADING

TEST PROCEDURES

Disk Control trouble shooting should follow these basic steps.

VISUAL CHECKS (Refer to Disk Cartridge Cont. Section VI)

1. Assure that the disk control cards have been loaded into the correct slots.
2. Assure that the Disk Cartridge Drive cabling to the control is proper.
3. Assure that a channel number jumper chip has been installed and that no two controls have the same channel number.
4. Assure that the unit present jumper chip is wired properly.

RUN CONFIDENCE ROUTINE

1. Before running the Disk Cartridge Confidence Routine be assured that processor and Memory are functioning properly. If necessary run the processor and memory confidence routines.
2. Run the Disk Cartridge Confidence routine. (Refer to paragraph on Confidence Routine).

TYPES OF FAILURES FROM THE CONFIDENCE ROUTINE

1. Routine will not run.
2. Not Ready Section fails.
3. Index read or write failure.
4. Initialize failure.
5. Burroughs format Read or write failure.
6. Pause OP failure.
7. Arm movement failure.
8. No failure.

DECISION

1. If confidence routine passed, attempt to recreate original problem.
2. For a failure, proceed to the Field Card Tester.
3. Test Disk cards in the Field Card Tester. (Refer to B 1700 Field Card Tester Manual).
4. If a problem is found and repaired, re-run confidence routine.
5. If Disk cards check OK in the Card Tester, or the problem cannot be resolved, go to the next paragraph.
6. Determine if both units of the dual drive have the problem. If not, the trouble probably lies in the drive as all interface lines except unit select are common.

USE OF I/O DEBUGGING ROUTINE

This step involves the running of the I/O Debug routine. For operation of the I/O Debug Routine refer to the paragraphs describing it and to the program listing.

Attempt to analyze the failure of the confidence routine and relate it to particular circuitry of the Disk Cartridge control. Set up the I/O Debug Routine to test this failing function.

For example if the confidence routine failed on all read-writes over 3 sectors in length but ran satisfactory on 3 sectors or less in length, the problem area would be the fourth data buffer. Set up the Debug Routine to do a Burroughs write with a data field length equal to 4 buffers.

Table V-2
Data Length for Specified Sector Lengths

Sector Length	F.L. Register	Sectors	Bits	Sectors	Bits
1	0005A0	21	007820	41	00E6A0
2	000B40	22	007BC0	42	00EC40
3	0010E0	23	008160	43	00F1E0
4	001680	24	008700	44	00F780
5	001C20	25	008CA0	45	00FD20
6	0021C0	26	009240		
7	002760	27	0097E0		
8	002D00	28	009D80		
9	0032A0	29	00A320		
10	003840	30	00A8C0		
11	003DE0	31	00AE60		
12	004380	32	00B400		
13	004920	33	00B9A0		
14	004EC0	34	00BF40		
15	005460	35	00C4E0		
16	005A00	36	00CA80		
17	005FA0	37	00D020		
18	006540	38	00D5C0		
19	006AE0	39	00DB60		
20	007080	40	00E100		

PROCESSOR TO DISK TRANSFER PROBLEMS

For a problem between the processor and disk control use the I/O Debug Routine.

Several features of this program may be used quite successfully here. The step program toggle shows the path taken by the control after each transfer. The trace program toggle runs a trace of the operation on the line printer. This may be used to determine which data on the exchange lines is in fault. For example, the disk control is not returning a Service Request in STC10. The program would, in the step mode, step the control to state 10 and loop waiting for the SR interrupt. Using the trace option, the trace would show the exchange line transfers to STC10 and would end here. These would both be indications of no SR. To trouble shoot the actual problem in the control step to STC-10 and examine the SR generation circuitry. Figure V-1 is a good reference here.

DISK CONTROL TO DISK DRIVE TRANSFER PROBLEMS

This type of problem should be trouble shot while looped in a Read or Write. Burroughs format should be used unless the problem prevents it.

1. First step should be to check all clocks (index, sector, and data clock.)
2. IMPORTANT: Sync scope with index at all times while scoping transfers from disk to control. Also any internal scoping of the control involving disk signals.
3. Determine if both units of the dual-drive have the problem. If not the trouble probably lies in the drive as all lines except unit select are common.

4. Decide what OP code should be used. For example, a Burroughs Read or Write can be used only when valid sync patterns have been written on disk. A problem involving writing the sync pattern therefore must be trouble shot in a Write index OP.
5. Make use of the interface testpoints to determine whether drive or control is at fault.

DISK DRIVE MAINTENANCE

The last three sections of the confidence routine allow for preventive maintenance of the disk drive. This can be used in aligning a head, checking Servo timers or to lock on a read compare of a track.

For other maintenance purposes use the I/O Debug Routine to manipulate the disk drive. The I/O Debug may also be used for the PM as well.

HARDWARE TESTPOINTS

DISK CARTRIDGE CONTROL – CARD 1
FRONTPLANE CONNECTORS

$X
Testpoints

A MOSEX001	I MOSEX081	R
B MOSEX011	J MOSEX091	S CHANHI . 1
C MOSEX021	K MOSEX101	T COMACT. 1
D MOSEX031	L MOSEX111	U
E MOSEX041	M MOSEX121	V
F MOSEX051	N MOSEX131	W
G MOSEX061	P MOSEX141	X
H MOSEX071	Q MOSEX151	Y
		Z

#X
Not Used

$Y
Not Used

#Y
Not Used

DISK CARTRIDGE CONTROL – CARD 2
FRONTPLANE CONNECTORS

$X
Testpoints

A STC01F . 1	I RD . IMM . 1	R TEST 1
B STC02F . 1	J WR . INX . 1	S PAUSE . . 1
C STC04F . 1	K WR . IMM . 1	T WRITE . . 1
D STC08F . 1	L CHAF . . . 1	U EXITF . . 1
E STC16F . 1	M BUFSEMP 1	V SR 1
F TERMF . 1	N IN100 . . . 1	W BUFSFLF 1
G RD . INX 1	P 3BUFULL 1	X CLKENBC 1
H READ . . 1	Q 1BUFULL 1	Y CLKENBD 1
		Z OUT90 . . 1

#X
Not Used

$Y
Not Used

#Y
Not Used

DISK CARTRIDGE CONTROL – CARD 3
FRONTPLANE CONNECTORS

$X
Not Used

#X
Testpoints

A BITR=8 . . 1	I INXF . . . 1	R WRENF . . 1
B BITR=15 . 1	J INXDF . . 1	S RDENF . . 1
C WDCT=92 1	K ADDRF . . 1	T BLKCT2 . 1
D DPEF . . . 1	L CYL=F . . 1	U SEEK.EX . 1
E DATAF . . 1	M TRKZROF 1	V SEEK.EX . 1
F SYNCF . . 1	N RD-D . . . 1	W SYNC . . . 1
G SECF 1	P FSFF . . . 1	X BITR=7 . . 1
H INXP 1	Q ADF 1	Y WR-D . . . 1
		Z EXCPBIT . 1

$Y
Interface Levels to B9480-2
Dual Drive A

A UNTSELA 1	I CYL1 1	R RD-DA . . 1
B CYL8 . . . 1	J HD.SELA 1	S CLOCKA . 1
C CYL7 . . . 1	K SEEKEXA 1	T INXPA . . 1
D CYL6 . . . 1	L WRENA . . 1	U SECPA . . 1
E CYL5 . . . 1	M RDENA . . 1	V ILADDA . 1
F CYL4 . . . 1	N WR-DA . . 1	W INCPLC . . 1
G CYL3 . . . 1	P FL.OPA . . 1	X WR.LKA . 1
H CYL2 . . . 1	Q POSETA . 1	Y
		Z CYL9 . . . 1

#Y
Interface Levels to B9480-2
Dual Drive B

A UNTSELB 1	I CYL1A . . 1	R RD-DB . . . 1
B CYL8A . . 1	J HO.SELB . 1	S CLOCKB . 1
C CYL7A . . 1	K SEEKEXB 1	T INXPA . . 1
D CYL6A . . 1	L WRENB . . 1	U SECPB . . 1
E CYL5A . . 1	M RDENB . . 1	V ILADDA . 1
F CYL4A . . 1	N WRDA . . 1	W INCPLB . 1
G CYL3A . . 1	P FL.OPB . . 1	X WR.LKB . 1
H CYL2A . . 1	Q POSETB . 1	Y
		Z CYL9A . . 1

BACKPLANE CONNECTOR DISK CARTRIDGE CONTROL CARD 1

	0		1
	C3	Backplane	C4
	+4.75V		+4.75V
	EXCH00 . 0	B	EXCH01 . 0
	EXCH02 . 0	C	EXCH03 . 0
	EXCH04 . 0	D	grnd
	EXCH05 . 0	E	EXCH06 . 0
	EXCH07 . 0	F	EXCH08 . 0
	EXCH09 . 0	G	EXCH10 . 0
X Connector	EXCH11 . 0	H	EXCH12 . 0
	EXCH13 . 0	I	EXCH14 . 0
	EXCH15 . 0	J	grnd
	EXCH16 . 0	K	EXCH17 . 0
	EXCH18 . 0	L	EXCH19 . 0
	EXCH20 . 0	M	EXCH21 . 0
	EXCH22 . 0	N	EXCH23 . 0
	CYL9FD . 0	P	CYL8FD . 0
	4US 0	Q	grnd
	1US 0	R	CYL7FD . 0
	32US . . . 0	S	CYL5FD . 0
	1024US . . 0	T	TRLZROF0
	CYL4FD . 0	U	CYL6FD . 0
	CHANHI . 0	V	CYL3FD . 0
	SCPM6 . . 0	W	grnd
	CYL2FD . 0	X	PIC 0
	PID 0	Y	CYL1FD . 0
	-12	Z	SR28. . . . 0
	BIT8204 . 0	A	-12V
	CLKENBD0	B	IOS 0
	TERMF/ . 0	C	CLRB 0
	HDSET . . 0	D	grnd
	HEADF . . 0	E	RC 0
	CLRCHAN0	F	CA 0
	DSTSHM2 0	G	SR 0
	SETMOS . 0	H	SPARE 10
	SR18 0	I	PWRON 0
	DSET1F/ . 0	J	grnd
Y Connector		K	CLRCLK . 0
	BIT1204 . 0	L	+12V
	CLKENBA0	M	PIA 0
	D . SET . . 0	Q	grnd
	DSTSHM 10	R	CLOCK . 0
		S	STVAL6 . 0
	STVAL5 . 0	T	RD-D 0
	STC1416 . 0	U	BUFDPOF 0
	BUFDP1F 0	V	FAR+1. . . 0
	SEC-1 . . . 0	W	grnd
	SHFSR1 . 0	X	SR2 RD 0
	CLKENBC 0	Y	SRVRQN . 0
	-2V	Z	-2V

BACKPLANE CONNECTOR DISK CARTRIDGE CONTROL CARD 2

	0		1
	C6	Backplane	C7
	+4.75V	A	+4.75V
	EXCH00 . 0	B	EXCH01 . 0
	EXCH02 . 0	C	EXCH03 . 0
	EXCH04 . 0	D	grnd
	EXCH05 . 0	E	EXCH06 . 0
	EXCH07 . 0	F	READ . . 0
	ADF 0	G	SC4F 0
	SC2F 0	H	SC1F 0
X Connector		I	DPEF . . . 0
	EXCPBIT . 0	J	grnd
	MAEF . . . 0	K	DSET1F/ . 0
	POS . SET 0	L	RIMR=7 . 0
	EXCH20 . 0	M	EXCH21 . 0
	EXCH22 . 0	N	SYNCF/ . 0
	BLKCT2 . 0	P	SECF. . . . 0
	SRVRQN. 0	Q	grnd
		R	SKCTR=7. 0
	DTOT2F . 0	S	SKSTN . . 0
	EXCH16 . 0	T	TRKZROF0
	WRLKOT. 0	U	3EXIT . . . 0
	CHANH1 . 0	V	BITR=2 . . 0
	SCPM7 . . 0	W	grnd
	DATAF . . 0	X	PIC 0
	PID 0	Y	WDCT90/. 0
	-12V Z	Z	DSETCOM 0
	EXCH17 . 0	A	-12V
	CLKENBD 0	B	IOS 0
	FLOPNL/. 0	C	CLRB . . . 0
	HDSET . . 0	D	grnd
	HEADF . . 0	E	RC 0
	UNITOF . 0	F	CA 0
	UNITIF . . 0	G	SR 0
	SETMOS . 0	H	SPARE . 10
	BUFSFLF 0	I	PWRON . . 0
	BUFSEMP 0	J	grnd
	WROP 0	K	TEST 0
	WR . IMM 0	L	+12V
	CLKENBA 0	M	P1A 0
	WR . INX 0	N	TERMF/ . 0
	CLKENBB 0	P	P1B 0
	RD . IMM. 0	Q	grnd
	RD . INX . 0	R	PAUSE/ . . 0
	EXCH19 . 0	S	STVAL6 . 0
	STVAL5 . 0	T	WRITE . . 0
	STC1416 . 0	U	BUFDPOF 0
	BUFDP1F 0	V	STC10 . 20
	EXCH18 . 0	W	grnd
	BUFLDOF 0	X	BUFLD1F 0
	CLKENBC 0	Y	CLRCHAN0
	-2V	Z	-2V

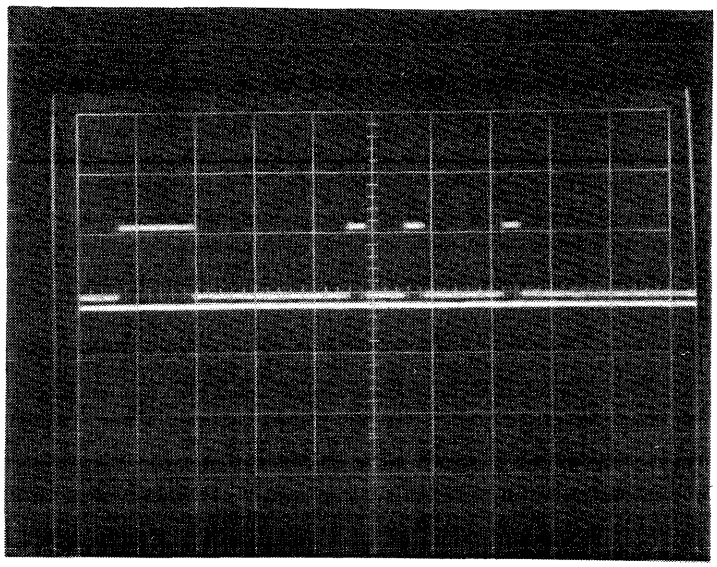
BACKPLANE CONNECTOR DISK CARTRIDGE CONTROL CARD 3

	0		1
	D0	Backplane	D1
	+4.75V	A	+4.75V
	CYL9FD . 0	B	CYL8FD . 0
	CYL7FD . 0	C	CYL6FD . 0
	CYL5FD . 0	D	grnd
	CYL4FD . 0	E	CYL3FD . 0
	CYL2FD . 0	F	READ . . . 0
	ADF 0	G	SC4F 0
	SC2F 0	H	SC 0
	BITR=15 . 0	I	DPEF . . . 0
	EXCPBIT. 0	J	grnd
	MAEF . . . 0	K	DSET1F/. 0
	POS . SET 0	L	RIMR=7 . 0
	CYLIFD . 0	M	
		N	SYNCF/ . 0
	BLKCT2 . 0	P	SECF . . . 0
	4US 0	Q	grnd
X Connector	IUS 0	R	SKCTR=7. 0
	32US . . . 0	S	SKSTSN. . 0
	1024US . . 0	T	TRKZROF0
	WRLKOT. 0	U	3EXIT . . . 0
		V	BITR=2 . . 0
	SCPM8 . . 0	W	grnd
	DATAF . . 0	X	BIT8204 . 0
	BIT1204 . 0	Y	WDCT90/. 0
	-12V	Z	DSETCOM0
		A	-12V
	DSTSHMI .0	B	DSTSHM2 0
	FLOPNL/. 0	C	CLRB. . . . 0
	DHSET . . 0	D	grnd
	RD-D . . . 0	E	SR18 0
	CLRCHAN0	F	SR28 0
	UNITIF . . 0	G	FAR+IM . 0
	FAR+1 . . 0	H	UNITOF . 0
	BUFSFLF 0	I	PWRON . 0
	BUFSEMP 0	J	grnd
	WROP . . . 0	K	TEST 0
	WR . IMM. 0	L	+12V
	SHFSR1. . 0	M	SR2-RD . . 0
	WR . INX. 0	N	TERMF/ . 0
	STC10 . . 20	P	CLOCK . 0
Y Connector	RD . IMM. 0	Q	grnd
	RD . INX . 0	R	PAUSE/ . . 0
		S	CLRCLK . 0
	HEADF . . 0	T	WRITE . . 0
	DTOT2F . 0	U	BUFDOPF 0
	BUFDP1F 0	V	SEC-1 . . . 0
		W	grnd
	BUFLDOF0	X	BUFLD1F 0
	DSETCOM0	Y	UNIT1F . 0
	-2V	Z	-2V

INTERFACE TESTPOINTS

The following testpoints are shown to assist the F.E. in determining if data on disk is written and/or read properly. All points shown are at testpoints on Card 3 of the disk control. Note that at these testpoints the signals are the inverse of actual interface lines.

Figure V-4 shows the sync pattern for cylinder 4, Track 1, Sector 1. Data written is all zeroes.

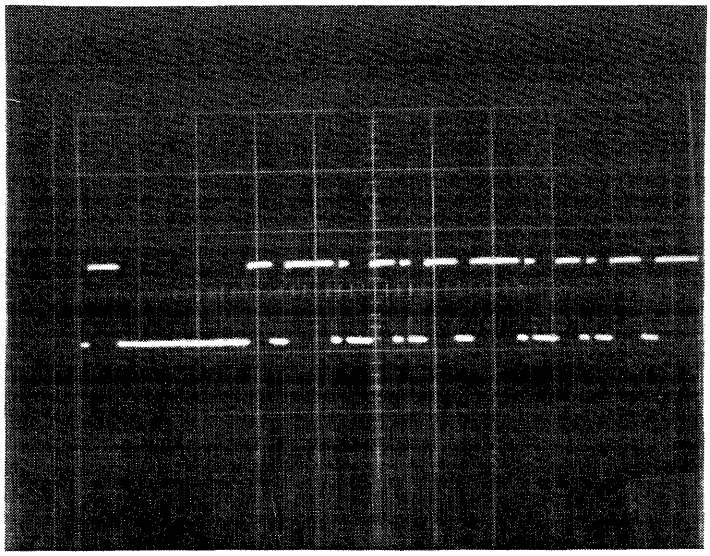


Scope Setup
External Sync on index (TP CD 3 #HX)
Channel 1 – Write Data (TP CD 3 #YX)
A delayed by B Timebase
Delay Time Set to 1ms/cm
Sweeptime Set to 2us/cm
Vertical Set to 2V/cm

Sector 1 data will be found approximately 2ms from index.

Fig. V-4 WRITE DATA SYNC PATTERN

Figure V-5 shows a Burroughs Read of cylinder 0, Track 0, Sector 0. Data being read is the sync pattern followed by X, Y, Z.

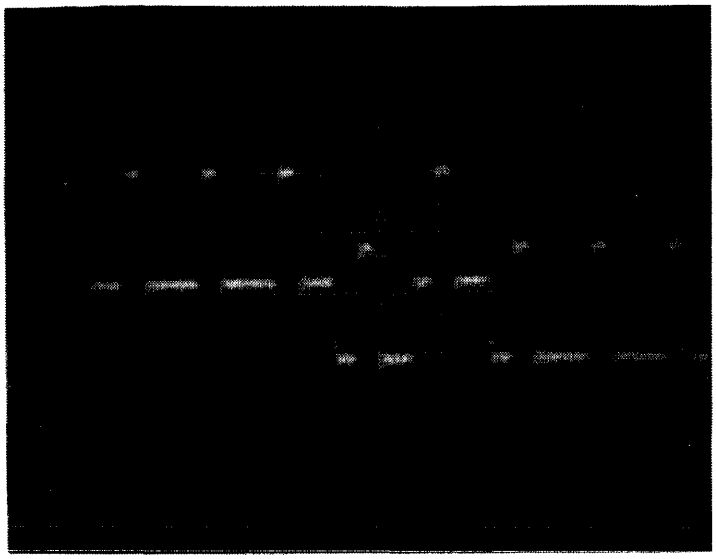


Scope Set Up
External Sync on index (TP Cd 3 #HX)
Channel 1 – Read Data (TP Cd 3 #NX)
A delayed by B Timebase
Delay Time Set to .5ms/cm
Sweeptime Set to 5us/cm
Vertical Set to 2v/cm

Sector 0 data will be found approximately .65ms from index.

Fig. V-5 READ DATA

Figure V-6 shows the relationship of Read Clock (Disk Clcok) with Read Data. The narrow tall pulse is Read Clock.



Scope Set Up
External Sync on index (TP CD 3 #HX)
Channel 1 – Read Data (TP CD 3 #NX)
Channel 2 – Disk Clock (Backplane Pin YD1P0
A delayed by B Timebase)
Channel Select to Chop
Delay Time Set to .5ms/cm
Sweeptime Set to .5us/cm
Vertical Set to 2v/cm

Fig. V-6 READ DATA/READ CLOCK

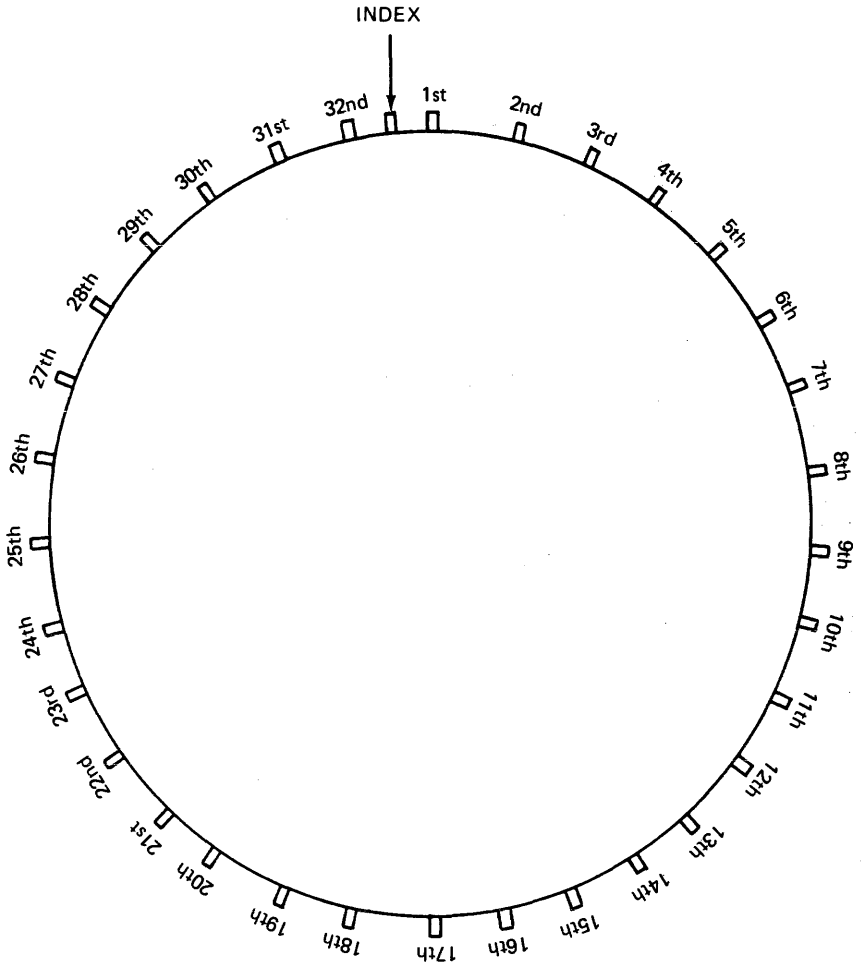
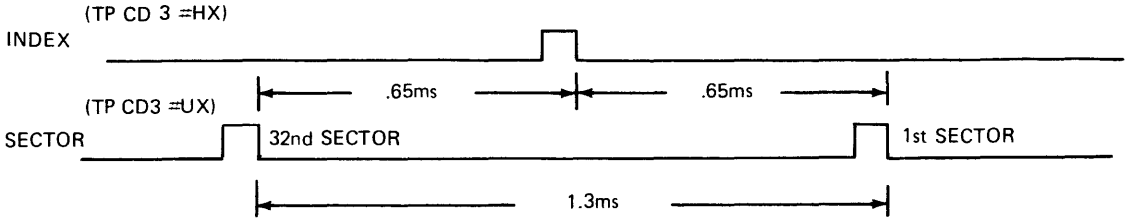


Fig. V-7 INDEX/SECTOR TIMING



INTRODUCTION

This section provides information to install and check out a Disk Cartridge control.

LOGIC PREPARATION

The processor communicates with an I/O control by addressing the controls unique channel number. During a service request by a control the channel is used to determine priority in the event two or more controls need service. Priority is determined by high order number first. Channel number for a particular control will vary depending on system configuration. In addition, for Disk a configuration chip must ve viewed.

CHANNEL NUMBER ADJUSTMENT

Jumper chip HO of Card 1 should be wired to reflect the desired Disk Cartridge channel number. Refer to I/O Base Section VI for typical system control numbers and an example for wiring the jumper chip. Jumper chip KO of Card 1 is for wiring in a channel number from 8 to 15. At present only 8 channels (0 - 7) are used.

CONFIGURATION ADJUSTMENT

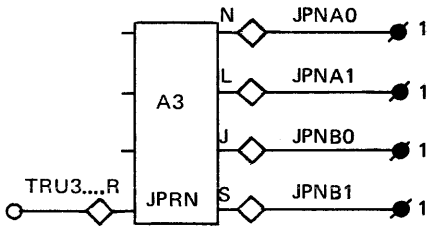


Fig. VI-1 CONFIGURATION JUMPER CHIP

Jumper chip A3 of card 3 is wired to reflect the number of Disk Drives attached to the control and to which frontplane connector the devices are attached.

Under normal operation 1 to 2 Dual Disk Drives are connected to the control. When Dual Drive A is installed pins N and L of chip A3 should be bussed to pin R of A3 (Refer to Fig. VI-1). This allows the control to service a Dual Disk Drive at frontplane connector $Y. With a Dual Disk Drive connected to frontplane connector #Y pins J and S of A3 will be bussed to pin R.

The OP CODE selects as Unit 0-A0, Unit 1-A1, Unit 2-B0 and Unit 3-B1.

PHYSICAL INSTALLATION

The Disk Cartridge Control will be installed in the I/O Base and cabled to the I/O Adapter Panel. The B9480 Disk Cartridge Drive is a free standing unit placed to the left of the console. The Disk Cartridge Drive is cabled to the I/O Adapter Panel.

CARD LOADING

The Disk Cartridge Control is contained on three cards. Slots 1, 2 and 3 of the I/O Base are dedicated to the Disk Cartridge Control. Card 1 is installed in slot 3, Card 2 in slot 2 and Card 3 in slot 1. Refer to I/O Base Section VI for more information.

PERIPHERAL TO I/O ADAPTER PANEL CABLING

The Disk Cartridge Drive cable is connected at the bottom rear. Snug cable around back of Drive and route over to the trough at the end of the table. Route cable through the trough and up to the I/O Adapter Panel. Extra cable length must be coiled up and tied neatly. Install the cable receptacle into the I/O Adapter Panel.

CONTROL TO I/O ADAPTER PANEL CABLING

Disk Cartridge Control has the ability to control two B9480-2 Dual Disk Cartridge Drives. Frontplane connector $Y is wired for units 0 and 1 and frontplane connector #Y for unis 2 and 3. Present system configuration calls for one Dual Drive. This Drive will be connected to connector $Y and designated as units 0 and 1.

Route the Disk Cartridge Control Adapter cable from frontplane connector $Y straight down to the trough at the bottom of the I/O Base. From the trough drop the cable straight down and into the table assembly. Route over and up to the I/O Adapter Panel. Plug the connector into the data cable receptacle and tighten down.

ELECTRICAL INSTALLATION

AC POWER

Route the Dual Disk Drive AC power cord alongside the previously laid data cable. Insert through trough at the end of the table and plug into a standard power receptacle on the AC Power Distribution Assembly.

PERIPHERAL/CONTROL CHECKOUT

Upon completion of the Dual Disk Drive installation run the Disk cartridge confidence routine and associated test routines to assure proper operation.

Note: New Disk Cartridges have no track addresses written. These cartridges must be initialized.

NVERSION INSTRUCTIONS FOR B1700 I/O BASE AND I/O BASE EXTENSION OR USING DISK CARTRIDGE CONTROL I OR DISK CARTRIDGE CONTROL II.

no change from DCC II to DCC III

PURPOSE

This instruction provides the necessary information to convert from an I/O Base (2205 0975) or I/O Base Extension (2205 0983) to an I/O Base II (2211 1322) or I/O Base Extension II (2211 1330).

REASON

The I/O Base or I/O Base Extension is used with Disk Cartridge Control I (2200 5730). The I/O Base II or I/O Base Extension II is used with Disk Cartridge Control II (2208 2887). The Disk Cartridge Control I and II cannot be interchanged without the appropriate backplane conversion.

INSTALLATION TIME: Approximately .75 hours.

CONVERSION INSTRUCTIONS

CONVERSION OF AN I/O BASE TO AN I/O BASE II:

The following instructions apply to the conversion of the I/O Base (2205 0975) or I/O Base Extension (2205 0893) to an I/O Base II (2211 1322) or I/O Base Extension II (2211 1330). This allows the use of Disk Cartridge Control II (2208 2887).

Make the following wiring changes:

		FROM	TO	LEVEL
DELETE	D.SET..O	XC6R	YC3Q	1
"	DSETCOMO	XC7Z	XD1Z	1
"	32US...O	XCOS	XC3S	2
ADD	BUFLDOFO	YC3S	YC6X	2
"	BUFLD1FO	YC3K	YC7X	2
"	DSETCOMO	YC3Q	YDOS	1
"	SC2+4..O	YC4N	YDOW	1

Relabel the backplane assembly from 2205 1924 to 2209 3736.

CONVERSION OF AN I/O BASE II TO AN I/O BASE:

The following instructions apply to the conversion of the I/O Base II (2211 1322) or I/O Base Extension II (2211 1330) to an I/O Base (2205 0975) or I/O Base Extension (2205 0983). This allows the use of Disk Cartridge Control I (2200 5730).

Make the following wiring changes:

		FROM	TO	LEVEL
DELETE	SC2+4..O	YC4N	YDOW	1
"	DSETCOMO	YC3Q	YDOS	1
"	BUFLD1FO	YC3K	YC7X	2
"	BUFLDOFO	YC3S	YC6X	2
ADD	32US...O	XCOS	XC3S	2
"	DSETCOMO	XC7Z	XD1Z	1
"	D.SET..O	XC6R	YC3Q	1

Relabel the backplane assembly from 2209 3736 to 2205 1924.

cut along dotted line

cut along dotted line

BURROUGHS CORPORATION
DATA PROCESSING PUBLICATIONS
REMARKS FORM

TITLE: B1700 DISK CARTRIDGE CONTROL TECHNICAL MANUAL

FORM: 1058310
DATE: 9-15-72

CHECK TYPE OF SUGGESTION:

☐ ADDITION ☐ DELETION ☐ REVISION ☐ ERROR

GENERAL COMMENTS AND/OR SUGGESTIONS FOR IMPROVEMENT OF PUBLICATION:

FROM: NAME _____ DATE _____
TITLE _____
COMPANY _____
ADDRESS _____
_____

STAPLE

FOLD DOWN SECOND FOLD DOWN

BUSINESS REPLY MAIL
First Class Permit No. 817, Detroit, Mich. 48232

Burroughs Corporation
Burroughs Place
Detroit, Michigan 48232

attn: Systems Documentation
Technical Information Organization, TIO – Central

FOLD UP FIRST FOLD UP