Unisys A 17

PRODUCT DESCRIPTION

In November 1987, Unisys Corporation finally ended user speculations and announced the long-expected high-end A 17 mainframe. March 1988 marks the third anniversary of the introduction of the previous high-end system, the A 15. The long wait was certainly worthwhile. According to the vendor, the price/performance of the new system is improved up to 30 percent over the A 15. The Relative Performance Measurement (RPM) of the A 17 ranges from 1,000 (20 MIPS) for the Model F to 3,600 (72 MIPS) for the Model N. The A Series now offers an even more extensive power range; growth potential is 144 times from the A 1 to the A 17. The A 17 uses the Master Control Program/Advanced System (MCP/AS) operating system and is object code compatible with the Unisys B 5000, B 6000, B 7000, and the entire A Series. This broad range of object code-compatible systems provides an ideal upward migration path for users of earlier Unisys systems.

PRODUCT ANNOUNCED: The new, very large scale A 17 System is the most powerful member of the Unisys A Series mainframe product line. The A 17 System is available in five models and is designed for very large on-line database transaction processing. The A 17 models are configured with from one to four processors and 48 to 288 megabytes of main memory. The A 17 operates under the MCP/AS operating system and is object code compatible with current A Series and B 5000, B 6000, and B 7000 Series systems.

COMPETITION: IBM 3090 and 3090 plug-compatible systems.

DATE ANNOUNCED: November 4, 1987.

SCHEDULED DELIVERY: Second-quarter 1988.

Among the most significant new hardware technology features on the A 17 is the Resource Management Module (RMM), which provides improved system throughput, greater connectivity options, and higher I/O bandpass. An optional component of the RMM is the Global Disk Cache. This feature allows frequently or recently accessed portions of the disk subsystem to reside in main memory. Access to this memory-resident data takes place at memory speed, reducing effective I/O time to nearly zero and resulting in an average performance improvement of 40 percent. The Global Disk Cache option evolved from, and is complementary to, the Software Disk Cache option on the A 12 and A 15. Users of Software Disk Cache can upgrade to the Global Disk Cache via the A 17 option.

The combination of the Global Disk Cache, the high processing speed of 2,000 I/Os per second of the RMM, and MLI channels with a burst data transfer rate of 8 megabytes per second makes the A 17 an ideal system for banks, financial institutions, and other businesses requiring strong on-line database transaction processing.

RELATIONSHIP TO CURRENT PRODUCT LINE: The A 17 is now the most powerful system in the Unisys ➢

The Unisys A 17 consists of five models with from one to four central processors and a main memory ranging from 48 to 288 megabytes. The new Resource Management Module provides the A 17 with faster system throughput and a higher I/O bandpass.

Unisys A 17

A Series mainframe lineup. The A 17 uses the MCP/AS operating system used throughout the A Series product line, thereby protecting user investments in both hardware and software. All A Series systems are object code compatible; users can move from the smallest A 1 to the largest A 17 system without costly software conversion. The A 12 and A 15 models are field upgradable to the A 17 with upgrade kits.

The A 17 has extensive peripheral options. In addition to new peripherals, existing peripheral subsystems from previous A Series systems can be used with the A 17. Among the storage devices available are the B 9494-12, B 9494-24, and MD8 Turbo Disk disk subsystem and the BT3200 Series, B 9495-82, B 9495-32, B 9495-33, and B 9495-22/23/24 tape subsystems. The A 17 supports four lines of workstations: the T27, ET 1100, BTOS Family, and PC/IT and PC/MicroIT. The T27 can function as either a system console or independent workstation. The BTOS PCs operate with the MS-DOS operating system and connect to both Unisys and IBM mainframes. The PC/IT and PC/MicroIT can interface with specially designed software on the A Series to provide multiple window access into mainframe-based software.

COMPETITIVE POSITION: IBM still holds the lion's share of the computer market, but Unisys has about 50 percent of the non-IBM-compatible computer market. The vendor had a very strong third quarter in 1987, with revenues of $2.22 billion and a net income of $129.7 million. Unisys closed out the year with the shipment of an A 15JX mainframe, part of an approximate $22 million order from the U.S. Department of Commerce, Patent and Trademark Office.

The A 15, and now the A 17, are the only American-made mainframes in the same class as the IBM 3090. In the Unisys long-term marketing strategy, price/performance plays an important role in gaining market share. For example, a fully configured two-processor A 17 Model H with 48 megabytes of memory is priced at $4,427,000. In comparison, a two-processor IBM 3090 Model 200E with 64 megabytes of main memory, a 64K-byte buffer per processor, and 32 channels costs $4,100,000. The required processor controller, two power units, coolant distribution unit, and two system consoles add another $336,590 to the price for a total of $4,436,590. All basic system components are included in the purchase price of the A 17. Water cooling is not required because the system uses air-cooled ECL gate arrays. Air cooling saves money and floor space, prime concerns in any computer installation. □

BASIC SPECIFICATIONS

MANUFACTURER: Unisys Corporation, P.O. Box 500, Blue Bell, Pennsylvania 19424. Telephone (215) 542-4011. Canada: Unisys Canada, 2001 Sheppard Avenue East, North York, Ontario M2J 4Z7. Telephone (416) 495-0515.

MODELS: Unisys A 17, Models F, H, J, L, N.

CONFIGURATION: The A 17 System consists of three major components: the Central Processor Module VI (CPMVI), the Memory Subsystem Module II (MSMII), and the Resource Management Module (RMM).

The A 17 Model F consists of one CPM; one MSM with a storage capacity of 48 megabytes, expandable in 24-megabyte increments to 288 megabytes; one RMM with from two to seven Message Link Interface (MLI) Port Adapters; two Input/Output (I/O) cabinets with two I/O Base Modules each; five high-speed Data Link Processors (DLPs) and eight low-speed DLPs per I/O Base Module; a Maintenance Subsystem with a maintenance console; and two operator display terminals.

The dual-processor A 17 Model H configuration is identical to the Model F but has three to seven MLI Port Adapters.

The A 17 Models J, L, and N are partitionable systems featuring a second MSM with an additional 48 megabytes of memory. The additional partition memory can also be upgraded to 288 megabytes. Model J has two CPMs, Model L three CPMs, and Model N has four CPMs. All models have two RMMs and from 4 to 14 MLI Port Adapters.

CENTRAL PROCESSOR AND MEMORY: The Central Processor Module utilizes Very Large Scale Integration (VLSI), Emitter Coupled Logic (ECL) gate array technology. Microcode is used as the source of control for operator execution. The CPM is functionally subdivided into five relatively independent submodules: the Program Control Unit (PCU), the Reference Unit (RU), the execution Unit (EU), the Write Unit, and the Memory Access Unit. Operations are distributed through the five concurrent submodules, allowing execution order to be determined by resource availability rather than code sequence order. This technique is made possible by having the PCU translate operators from a stack context to a three-address (two inputs, one output) context, using the Central Data Buffer (CDB) as the addressed storage. Concurrency is increased by concatenating some very simple operators and distributing complex operators over several submodules.

The Memory Subsystem Module is based on 256K-bit chip technology and consists of two Memory Storage Units (MSUs) and a single Memory Control Module (MCM). An MSU contains from one to six memory storage boards, each with 24 megabytes for a total memory capacity of 288 megabytes. The MCM includes a purgeless cache mechanism which extends the memory subsystem to the requestors' cache memories. The MCM ensures that only one master of the data, referenced by a main memory address, exists in the system at any one time. The A 17 uses a 60-bit word which consists of 48 data bits, 4 control bits, and 8 error-correcting bits. The MCM contains the necessary logic to control the detection and correction of single-bit errors and the detection of multiple-bit errors. Periodically, the MCM issues a command to the storage units to correct any soft errors that may exist in memory.

INPUT/OUTPUT SUBSYSTEM: The new Resource Management Module consists of the Input/Output Processor (IOP), the Task Control Processor (TCP), and the MLI Port Adapters. The IOP is responsible for the logical aspects of initiating and terminating I/O operations, thereby relieving the burden from the CPM. The TCP takes over the task management functions from the CPM freeing the processor to concentrate on user work. The new RMM design also provides greater I/O bandpass and I/O connectivity than previously available. The RMM is capable of processing up to 2,000 I/Os per second with no more than a 20 percent utilization of the I/O processor. Each RMM can support up to seven MLI Port Adapters. Each MLI Port Adapter provides two MLI channels; each MLI channel can transfer data in parallel at 8 megabytes per second.

Each MLI Port Adapter connects to an I/O Base Module. Two I/O Base Modules are housed in an independent I/O cabinet; two I/O cabinets are standard for each system. The I/O Base Modules contain a series of specialized DLPs that are responsible for the transfer of data to and from the peripheral subsystem. There is a special DLP for each type of peripheral subsystem. Some DLPs can service multiple peripherals of the same type through standard

Unisys A 17

peripheral exchanges. Each DLP includes a microprocessor, a peripheral interface, and a quantity of local memory.

Either one or two RMMs may be configured in an A 17 System. Partitionable models contain two RMMs. When a dual RMM system is operated as a single system image under the control of a single operating system, only one of the TCPs and IOPs will be active. The MLI Port Adapter channels in both RMMs are used.

COMMUNICATIONS: The Data Communications DLPs (DCDLPs) are located in the I/O Base Modules with each DCDLP controlling four communications lines. The DCDLPs are designed for entry-level data communications. For more extensive data communications requirements, the A 17 supports Network Support Processors (NSPs). Local area networks and wide area networks can also be implemented with the Integrated Communications Processor DLP (ICPDLP), the Communications Processor Local Area Network (CPLAN), the front-end Communications Processor CP2000, and the Network Architecture Version 2 (BNAv2).

The dedicated Maintenance Subsystem executes hardware diagnostic test routines and performs system configuration and initialization. It also provides software power control and monitoring of all mainframe cabinets, power loss recovery, dynamic error logging of mainframe failures, and remote access for most maintenance functions.

SOFTWARE: The Master Control Program/Advanced System (MCP/AS), designed to support the advanced architecture of the A Series family of computers, is the operating system used by the A 17. The system architecture is derived from hardware and software designed as an integral unit to provide virtual memory, variable-size memory areas, compiler-oriented hardware, reentrant code, dynamic resource allocation, and multiprogramming. Programs running under the MCP/AS can address the entire main memory, up to 288 megabytes. The MCP/AS operating environment supports the Mirror Disk and Memory Disk features. Mirror Disk is the parallel functioning of two to four disks where all the units are exact copies of each other. With Memory Disk, some portion of the system's main memory may be used as a disk unit.

Among the software products available for the A 17 are productivity tools that include Network Control, Message Control, Data Management, Work Management, Report Management, File Management, Network Management, Security, and Text Editing. InterPro and Logic and Information Network Compiler II (LINC II) software provide enhanced levels of programmer and user productivity. The InterPro software modules include Menu Assisted Resource Control (MARC), Interactive Data Communications Configurator (IDC), Screen Design Facility (SDF), Communications Management System (COMS), Advanced Data Dictionary System (ADDS), and Extended Retrieval with Graphics Output (ERGO). The LINC II fourth-generation language generates complete on-line, realtime systems, including programs, database description, screen formats, transaction management, and network management.

The A 17 supports a wide range of high-level and interpreter languages including APL, Algol, Basic, Cobol 68 and 74, Fortran 66 and 77, Pascal, PL/1, and RPG II.

PRICING: The only hardware prices available from the vendor at press time were for the five A 17 models. For prices on peripherals please refer to the price list following the A 15 report on Page 70C-944YT-501. All software is unbundled, but pricing was not available. The standard Unisys leasing and support agreements apply to the A 17 System.

EQUIPMENT PRICES

		Purchase Price ($)
Basic Configuration		
A 17F	Basic System; includes one central processor module, one memory subsystem module with 48 megabytes of memory, one resource management module, two I/O cabinets, one maintenance subsystem with console, and two operator display terminals	3,132,000
A 17H	Basic System; includes two central processor modules, one memory subsystem module with 48 megabytes of memory, one resource management module, two I/O cabinets, one maintenance subsystem with console, and two operator display terminals	4,427,000
A 17J	Basic System; includes two central processor modules, two memory subsystem modules with 48 megabytes of memory, two resource management modules, two I/O cabinets, one maintenance subsystem with console, and two operator display terminals	5,665,000
A 17L	Basic System; includes three central processor modules, two memory subsystem modules with 48 megabytes of memory, two resource management modules, two I/O cabinets, one maintenance subsystem with console, and two operator display terminals	7,310,000
A 17N	Basic System; includes four central processor modules, two memory subsystem modules with 48 megabytes of memory, two resource management modules, two I/O cabinets, one maintenance subsystem with console, and two operator display terminals ■	8,995,000