## 6.23 B 5000 PARALLEL PLATE PACKAGES

### INTRODUCTION

The basic operations of the standard Parallel Plate Packages used in the B 5000 system are described in this section. Included in this description is an explanation of the characteristics and use of these packages in the B 5000 system.

The description by no means exhausts the subject. It is only meant to give anyone who might work with these packages a general idea of their operation and use in the B 5000 system.

The following is a table of the B 5000 Parallel Plate Packages described in this text.

TABLE 6.23-1. PARALLEL PLATE PACKAGES

| DESCRIPTION | SCHEMATIC NO. |
|---|---|
| SWITCH I | C-80661 |
| FLIP-FLOP 20-70 | C-1182424 |
| B.O. & LINE DRIVER | C-1182507 |
| CLOCK OSCILLATOR & SQUARE AMP. | C-1182681 |
| MULTI 5.5μs | C-11833100 |
| MULTI 20μs | C-11833118 |
| MULTI 115μs | C-11833126 |
| MULTI 300μs | C-11833134 |
| MULTI 2.0ms | C-11844719 |
| MULTI 4.9ms | C-11833142 |
| MULTI 55ms | C-11833159 |
| MULTI 85ms | C-11833167 |
| DC LOCAL CLOCK DRIVER | C-11832771 |
| DELAY A 30μs | C-11833175 |
| DELAY A 77μs | C-11837143 |
| DELAY C 1.5μs | C-10025518 |
| DELAY C 10μs | C-10025476 |
| DELAY C 10ms | C-11836681 |
| DRIVER 50-90 | C-11836392 |
| SYNCHRONIZER | C-11844735 |
| COMPRESSOR | C-11844743 |
| DOUBLE DRIVER 90 | C-11918307 |
| INVERTER DRIVER 90 | C-11902400 |
| FLIP-FLOP AMPLIFIER | C-11900347 |

## 6.24 FLIP-FLOP 20-70

### GENERAL DESCRIPTION

The high speed, 20-70, flip-flops are intended for use as active elements in current steering diode logic circuitry operating at frequencies up to 2 megacycles. It serves both as a one-bit memory and as a current amplifier.

### BLOCK DIAGRAM DESCRIPTION

The basic high speed flip-flop is shown as a block diagram in Figure 6.24-1. The flip-flop has two input sides, 1 and 0, two corresponding outputs, and a clock line. The outputs are complements of one another, when one output is true, the other is false. An input signal may be in either of two states, true or false.

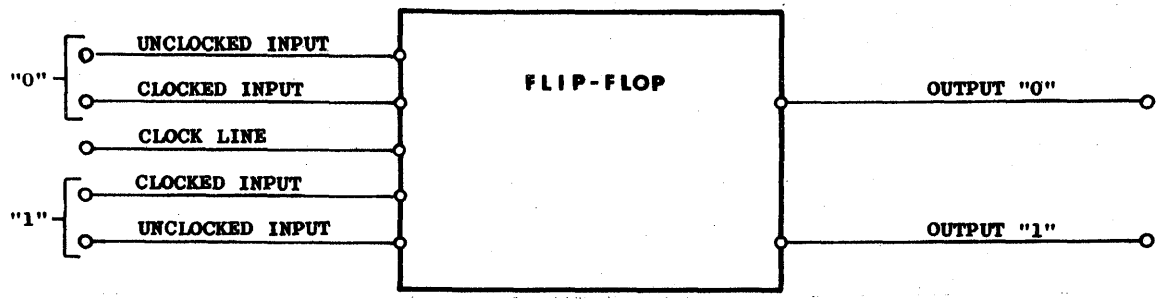



FIGURE 6.24-1. FLIP-FLOP BLOCK DIAGRAM

A false input signal will have no affect on the condition of the flip-flop. A true input signal will determine the state of the flip-flop at the next clock time.

The effect of a true input signal on the flip-flop depends upon which side, 0 or 1, it appears. If it appears on the 0 side, the flip-flop will switch to the "0 State" within a few tenths of a microsecond. If the flip-flop is already in the "0 State", it will remain there. Similarly, a true input signal on the 1 side will cause the flip-flop to switch to the "1 State". If the flip-flop is already in the "1 State", it will remain there. A true signal may occur at either of the two inputs on a side; the unclocked input or the clocked input. If the signal occurs at the unclocked input, it will unconditionally set the flip-flop to the corresponding state. If the signal occurs on a clocked input, it will not set the flip-flop unless the clock is simulataneously true.

If both clocked inputs are true when the clock is true, the flip-flop will complement. That is, it will go from the stable state it is in to the other stable state.

STATIC CONDITIONS

The analysis of the flip-flop can be simplified by first studying its two stable states. The circuit of Figure 6.24-2 shows only those components essential to these states. Since a DC condition is represented, capacitors are shown as open circuits and the delay line is shown as a resistor.

The flip-flop is shown in the "0 State". Since Q2 is in saturation, $V_{c2}$ is only a few tenths of a volt more negative than $V_2$. The collector current, $I_{c2}$, will adjust itself to maintain this condition.

There are two resistor networks running from $V_1$ to the collector of Q2. The first network consists of RD2A and R1A. The resistance ratio is such that when Q2 is in saturation, $V_{b3}$ is more positive than ground. Therefore, the base of Q3 is back biased, Q3 is OFF, and the 0 output is true.

The second network consists of resistors R4A and R5A. This resistance ratio is such that the base of Q1 is more positive than $V_2$, so that Q1 is held OFF. When Q1 is OFF, $V_{c1}$ is approximately -6V. This voltage is determined by the resistance of R3, R4 and RD2.

The resistance of RD2 is such that when Q1 is OFF, $I_2$ is much greater than $I_1$. The resulting $I_{b4}$ is enough to hold Q4 in saturation and thereby make the 1 output false.

The value of R4 is such that $I_4$ is much larger than $I_5$ when Q1 is OFF. The resulting $I_{b2}$ is sufficient to hold Q2 in saturation. Therefore, if Q2 is made to saturate, the circuit alone will maintain Q2 in saturation.

R2 = R2A, R3 = R3A, etc.

Q1 and Q2 are interchangeable, as are Q3 and Q4. A signal applied to the 1 input will force Q1 into saturation. From symmetry it is apparent that once Q1 saturates, the circuit will maintain it in saturation. In this state, Q3 will also be in saturation while Q2 and Q4 will be OFF.

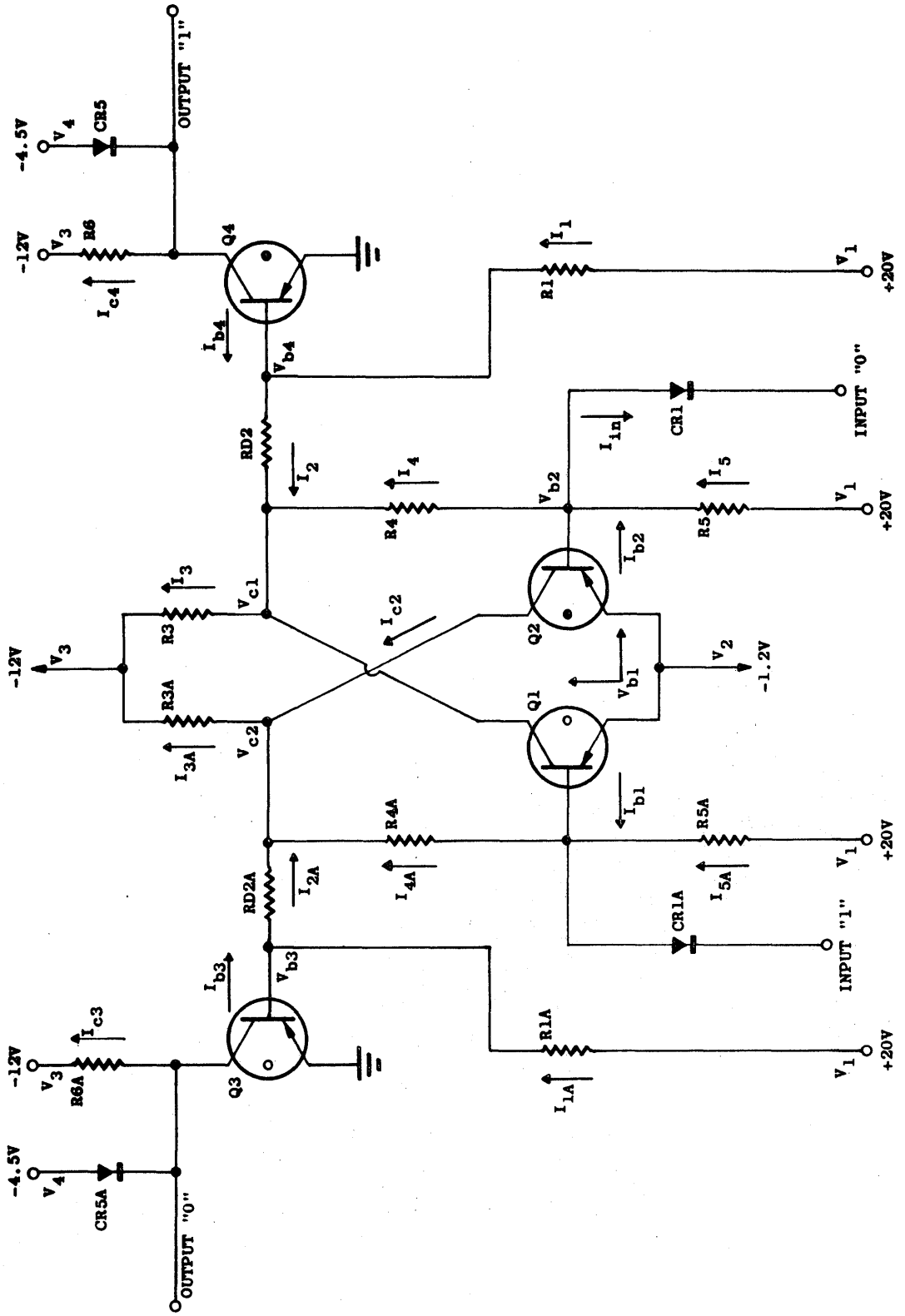



FIGURE 6.24-2. FLIP-FLOP STATIC CONDITION

SWITCHING

Refer to Figures 6.24-3 through 6.24-7.

The process followed by the circuit in going from one stable state to the other is described below. Refer to Figures 6.24-4 through 6.24-7 while going through this description. The amplitudes and timing shown in these figures are only nominal.

Until time, $T_0$ the flip-flop is in the "1 State", and all voltages and currents have attained a steady state value. At $T_0$ a current pulse $I_{in}$, is drained from the 0 input. This current is sufficient to drive Q2 into saturation. As Q2 goes from cut off to saturation, $V_{c2}$ rises towards $V_2$. As $V_{c2}$ changes, $I_{4A}$ decreases and capacitor $C_{7A}$ discharges, inducing a negative $I_{7A}$. Sometime during the rise of $V_{c2}$, $I_{7A}$ becomes greater than $I_{4A} - I_{5A}$. At this time, the base of Q1 becomes back biased and Q1 starts turning OFF.

As Q1 goes off, $V_{c1}$ goes negative. This charges C7 thereby inducing $I_7$. $I_4$ is also increased. Both of these currents provide more base drive to Q2.

As Q2 went into saturation, the voltage across RD2A, a series resistance delay element, was decreased by several volts. The delay characteristics of the element prevent the current $I_{2A/0}$ from changing for a time $T_d$ after the change in voltage on the input. After that time $I_{2A/0}$ decreases and stops supplying the base current $I_{b3}$.

Meanwhile, the change in $V_{c1}$ increases the voltage across RD2, a component identical to RD2A. The amplitude of $I_{2/0}$ cannot change for the same time $T_d$, but after this, time increases rapidly to its upper limit. As this current change occurs the base emitter diode of Q4 is forward biased and the base current $I_{b4}$ starts to flow.

By the time $T_1$ the inside transistors, Q1 and Q2 have exchanged states. Q1 is OFF, Q2 is in saturation. The input current $I_{IN}$ may be turned OFF at this time or even before. After $T_1$, the base current in Q3 decreases and Q3 starts to turn OFF. Simultaneously, the base current in Q4 increases and Q4 starts to turn ON. As Q4 turns ON $V_{c4}$ rises towards ground and as Q3 turns OFF, $V_{c3}$ heads for $V_3$ due to $I_{6A}$, but is clamped by CR5A at around -5V.

Finally Q4 is in saturation and Q3 is OFF. Q4 is maintained in saturation by the current $I_{2/0}$ which is now larger than $I_1$. Q3 is held OFF because its base is back-biased. The flip-flop has reached its second stable state, the "0 State".

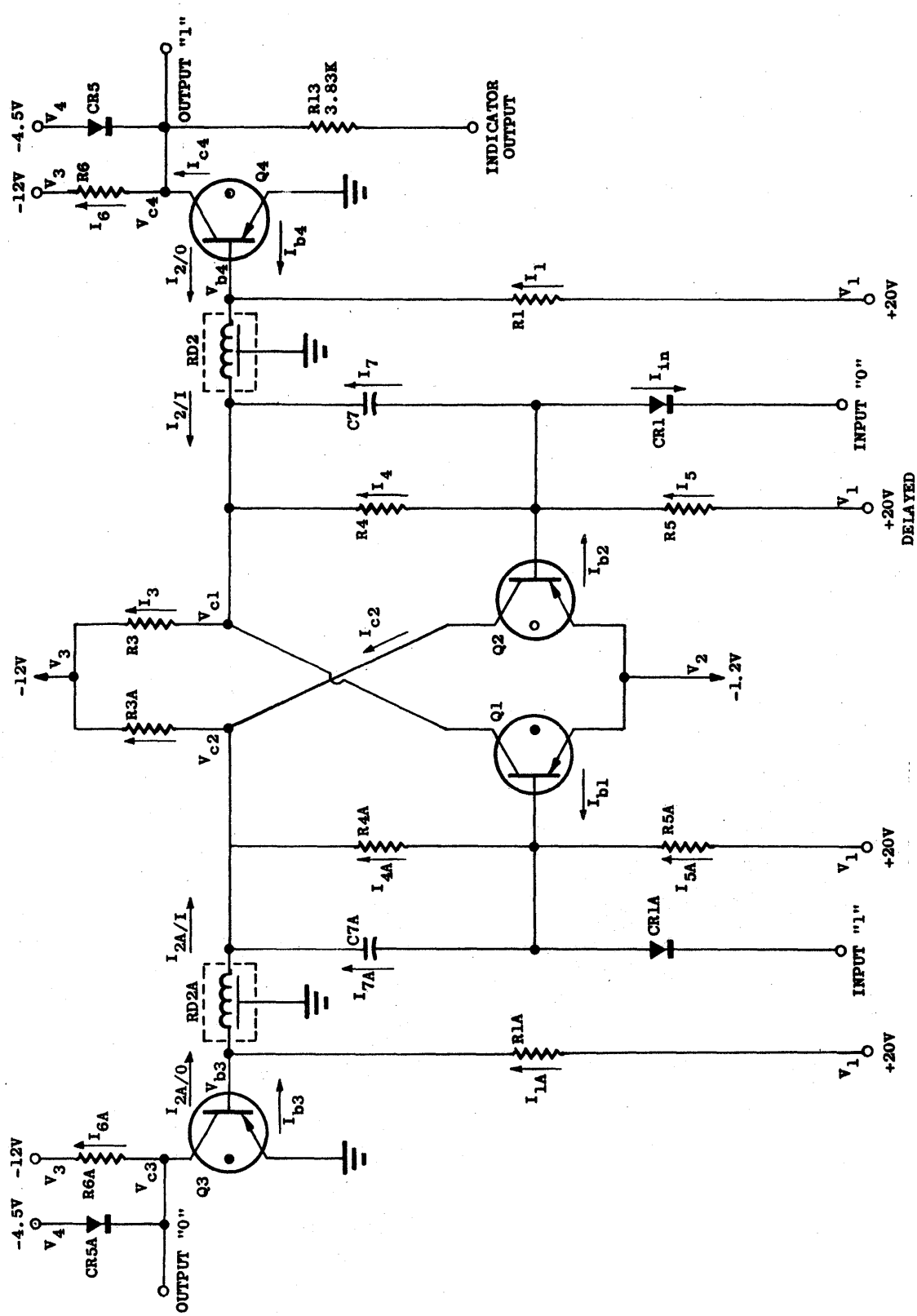



FIGURE 6.24-3. SWITCHING ANALYSIS SCHEMATIC OF THE FLIP-FLOP

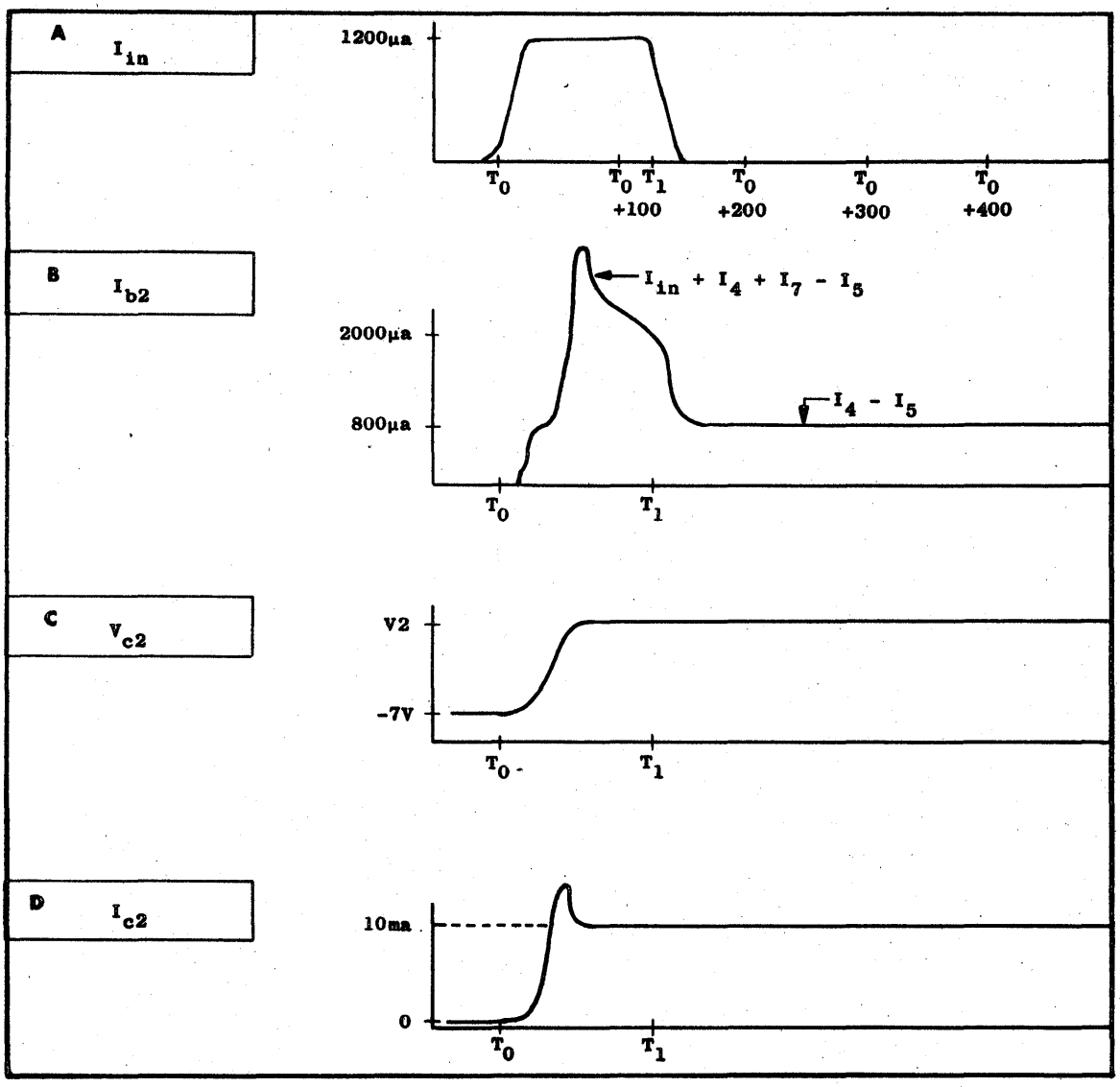



FIGURE 6.24-4. Q2 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

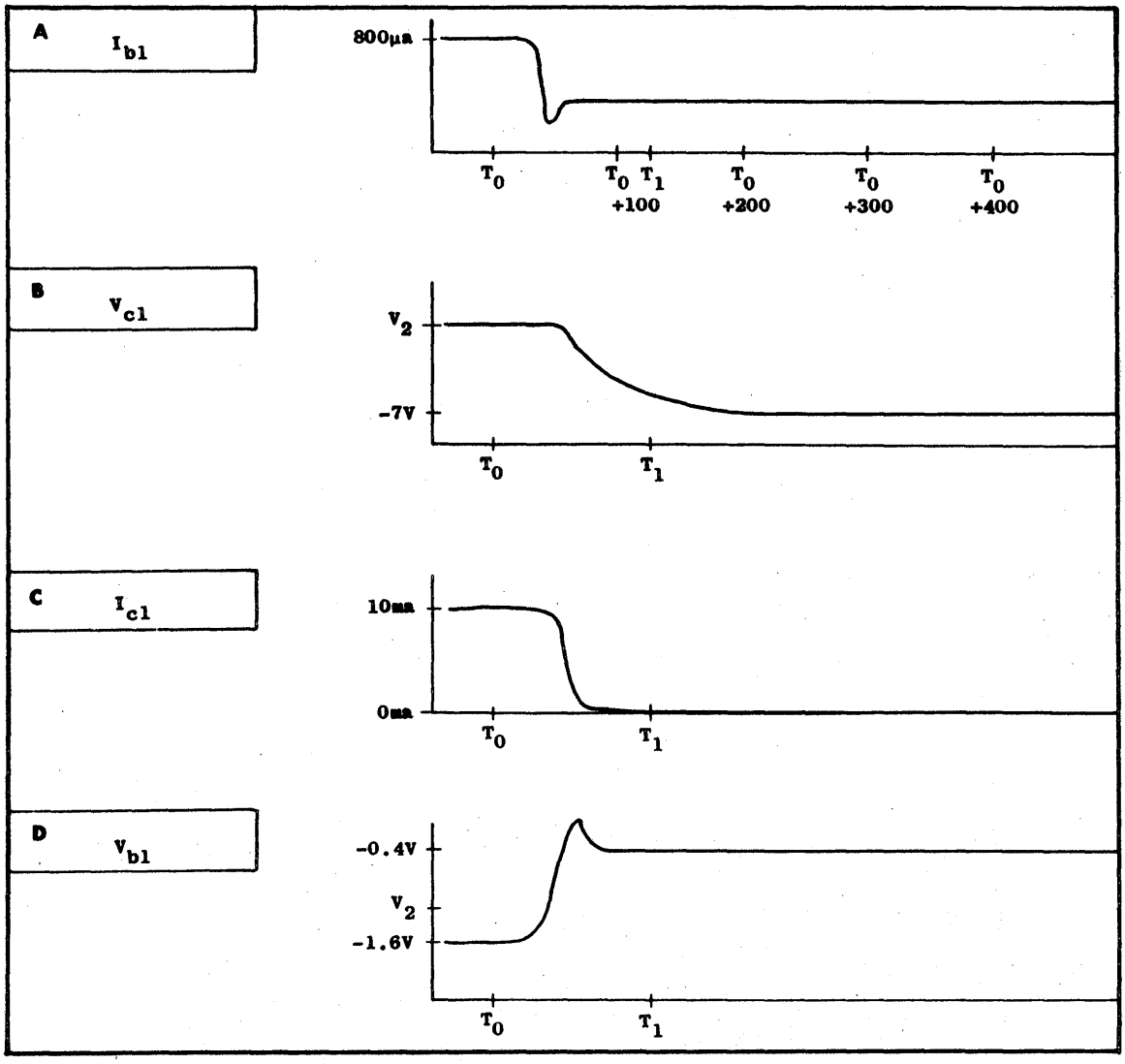



FIGURE 6.24-5. Q1 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

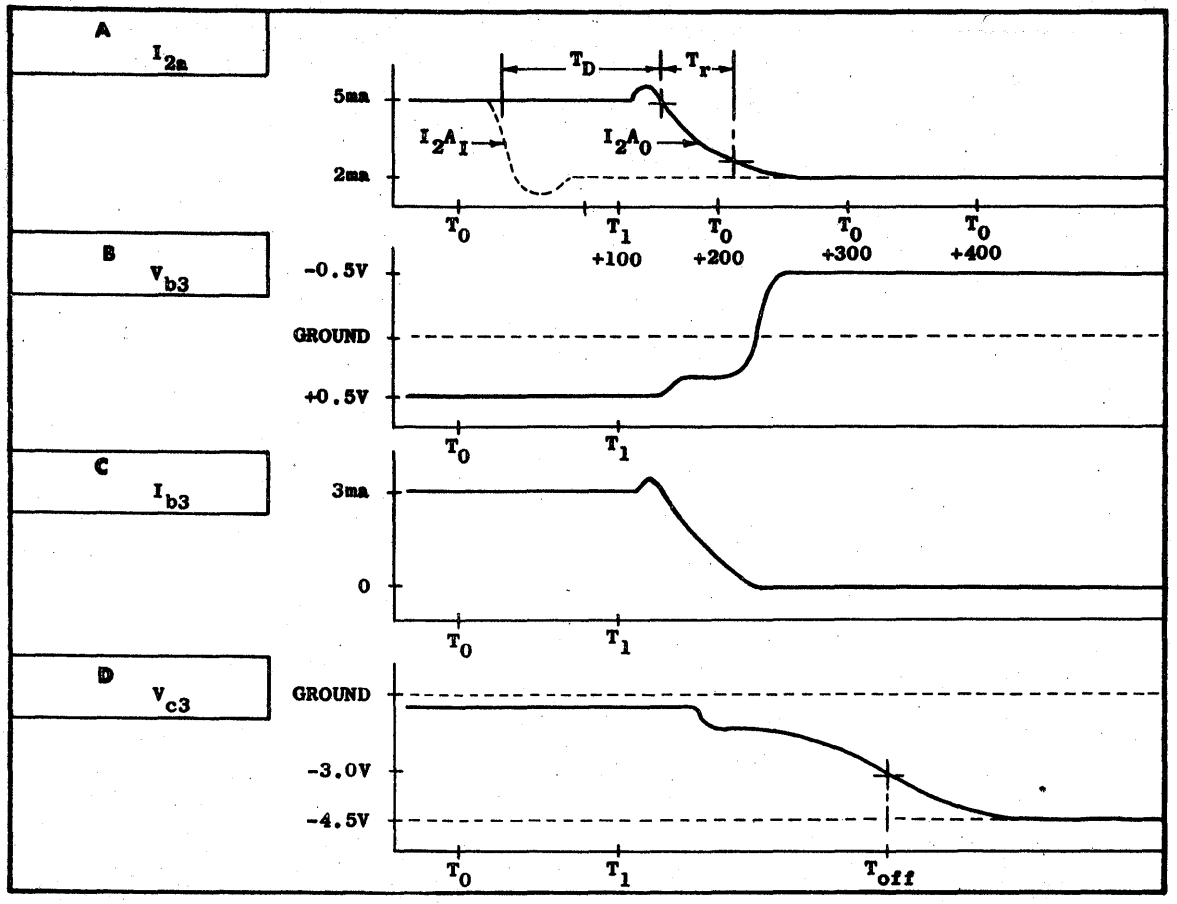



FIGURE 6.24-6. Q3 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

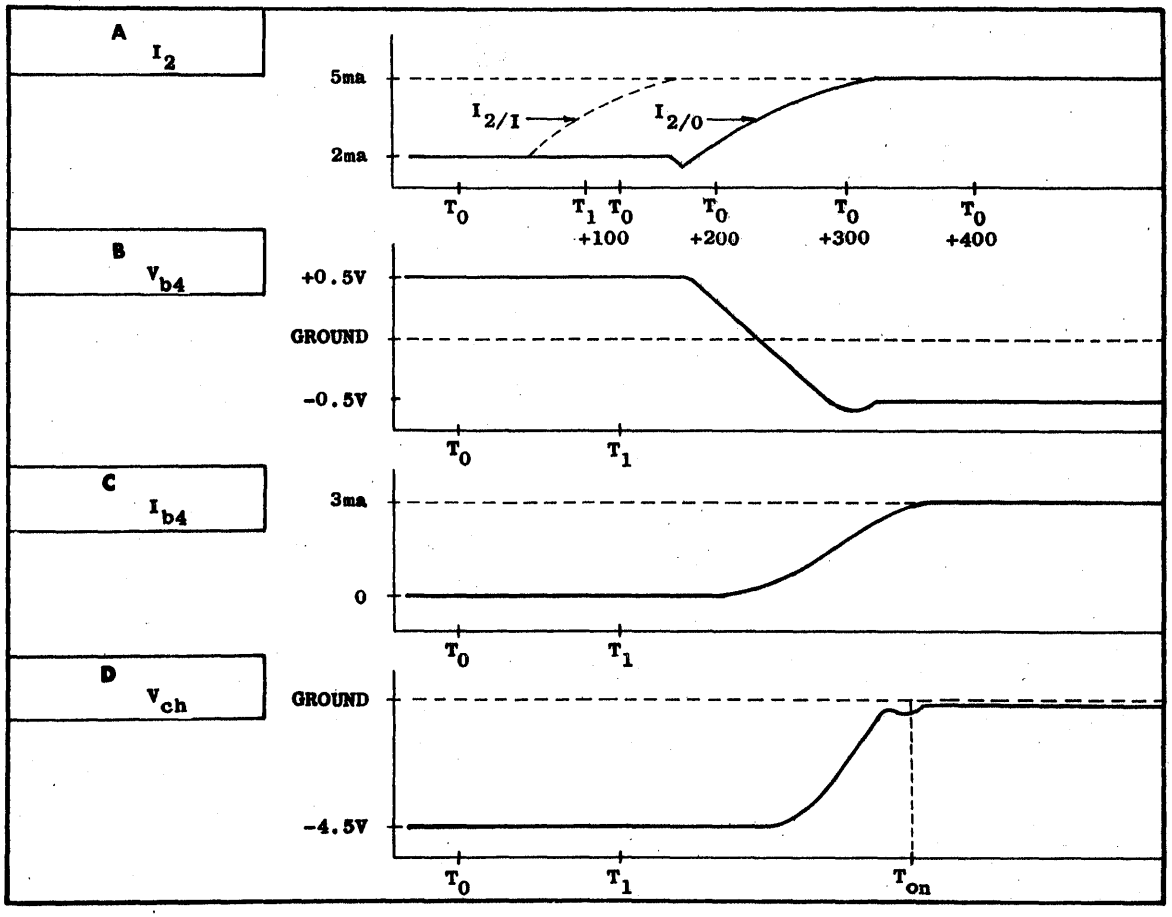



FIGURE 6.24-7. Q4 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

INPUTS

The input signals in Figure 6.24-2 and Figure 6.24-3 are shown as coming in through diodes CR1 and CR1A. These are the unclocked inputs. When the gate attached to one of these inputs goes true, the associated transistor will be driven into saturation and the flip-flop will be set. Figure 6.24-8 shows the arrangement of diodes for both the clocked and unclocked inputs on each side.

Each clocked input line is connected to three diodes. On the 0 side (base of Q2) the diodes are CR2, CR3, and CR4. On the 1 side (the base of Q1), the diodes are CR2A, CR3A and CR4A. In order to turn ON Q1 through the clocked input, CR2A must conduct the input current. CR2 must do likewise in order to turn Q2 ON.

Assume that 1 clocked input is true $I_{IN}$ (1) is applied. If the clock is false, $V_{c1}$ will be -0.6V. Therefore, $V_{in}$ (1) cannot go more negative than -0.9V since CR3A will supply a current equal to $I_{in}$ (1) at that voltage. If the clock is true during the time $I_{in}$ (1) is present, CR3A is back biased and CR2A conducts, driving Q1 into saturation.

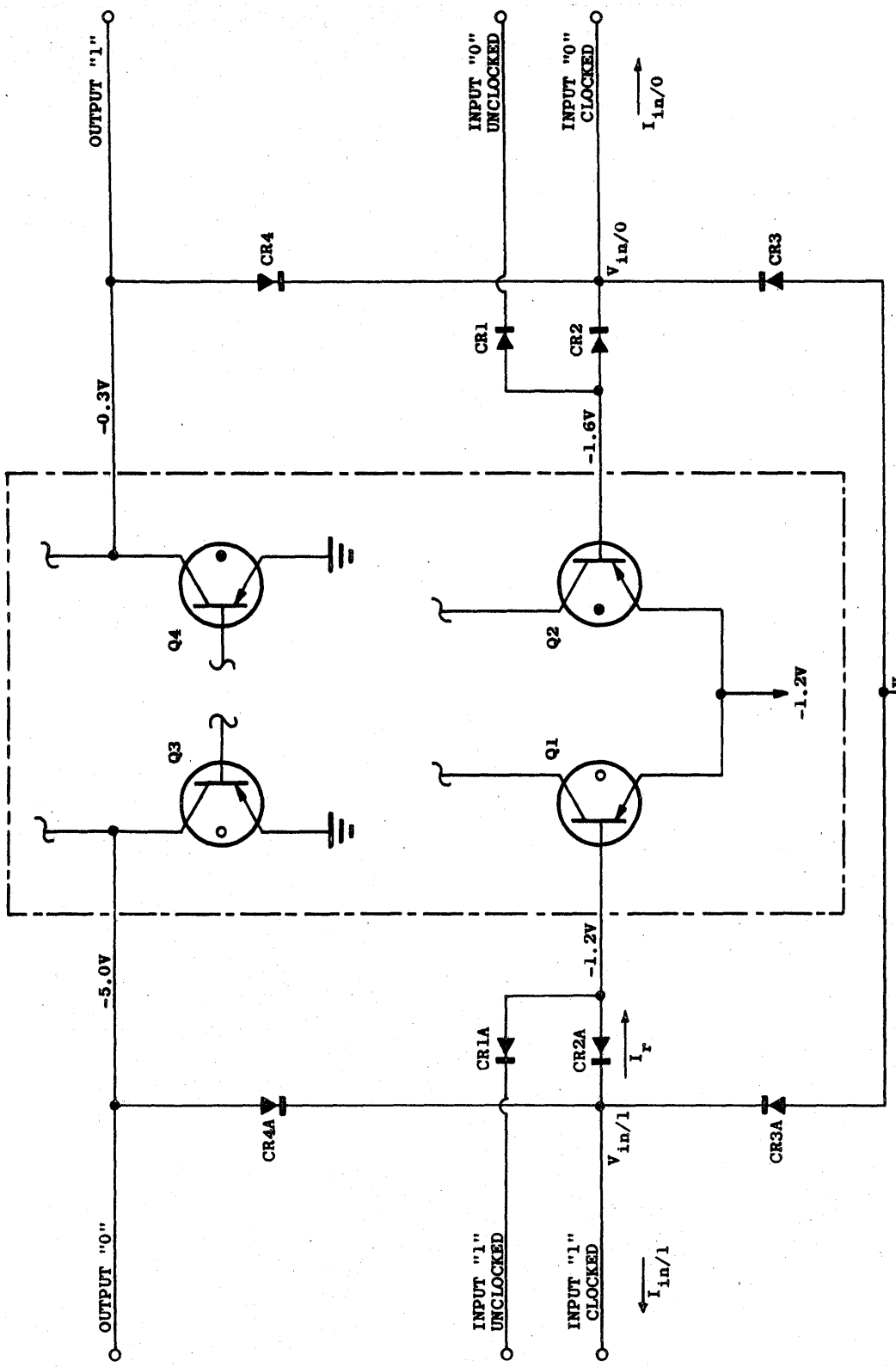



FIGURE 6.24-8. INPUT GATING SCHEMATIC

If instead $I_{in}$ (0) drives the 0 clocked input (trying to set the flip-flop to the "0 State") CR2 cannot conduct, even at clock time, as CR4 clamps $V_{in}$ to -0.6V. However, if Q4 is in saturation, the flip-flop is already in the "0 State".

If $I_{in}$ (1) and $I_{in}$ (0) are applied simultaneously and the clock is also true, the flip-flop will complement, that is, it will change state. If the flip-flop is in the "0 State", then CR2 will not see $I_{in}$ (0) due to the clamping effect of CR4, but CR2A will conduct $I_{in}$ (1). The flip-flop would therefore switch to the "1 State". If the flip-flop started in the "1 State", it would switch to the "0 State".

## LOGICAL OUTPUTS

There are two logical outputs per flip-flop. These outputs are logical complements of one another.

When an output is false, it must supply currents to the gates attached to it. These currents are usually the major part of the collector current through the saturated transistor. When an output is true, the output transistor is OFF. The collector resistor and the -12V Supply pull the output voltage negative until it is clamped by the diode to the -4.5V Supply.

## INDICATOR OUTPUTS

The resistor $R_{ind/A}$ may be connected to neon indicator light drivers. These lights will visually indicate the state of a flip-flop.

## SEQUENCING POWER SUPPLIES ON

The flip-flop will be in the "0 State" immediately after the power is turned ON if the supplies are activated in the sequence +20V, -1.2V, -4.5V, -12V, then +20V delayed.

When the -12V Supply is turned ON, the collectors of Q1 and Q2 will start to go negative. As the collector of Q1 goes negative, Q2 will get the base current and start conducting since it has no cut off current. However, though the collector of Q2 may go a little negative, Q1 will not go on because of the cut off current supplied by +20V Supply through R5A. Since Q1 is held OFF, Q2 will go into saturation. When +20V delayed goes ON, Q2 will be in saturation and Q1 will be cut off (the 0 state). In this condition, the cut off current through R5 cannot affect the state of the flip-flop.

## MANUAL CONTROL

The flip-flops can be set to either state through a manual switching operation which is completely decoupled from the logical inputs. This operation is performed on the input normally connected to the +20V delayed input. R5 in conjunction with an external switching arrangement can supply drive current to manually SET and RESET the flip-flop.

Figure 6.24-9 shows an arrangement which will provide this manual SET/RESET feature. $S_1$ is a make before break switch normally set to position B. While the switch is in this position the flip-flop can be used in a normal fashion by the machine.

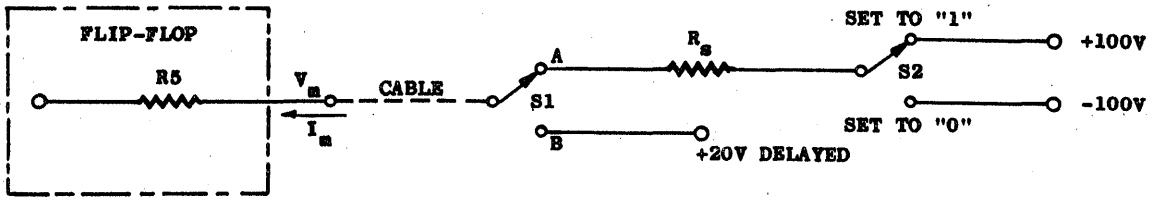



FIGURE 6.24-9. MANUAL CONTROL SWITCH

To manually set the flip-flop to the "1" or "0 State", $S_2$ is set to the appropriate position. $S_1$ is momentarily set to position A and returned to position B. By the time $S_1$ is returned to position B, the flip-flop will be in the desired state.

If $S_2$ were connected to the -100V Supply, then an $I_{IN}$ would be induced through R5 which would drive Q2 into saturation and force the flip-flop to the "0 State".

$S_1$ is a make before break switch. If it were not, then in the interval that no contact was made at either A or B, the connection to R5 would be open circuited. At this time the flip-flop would have no noise threshold on the 0 input and might be spuriously set to an undesired state.

## POWER SUPPLY VOLTAGES

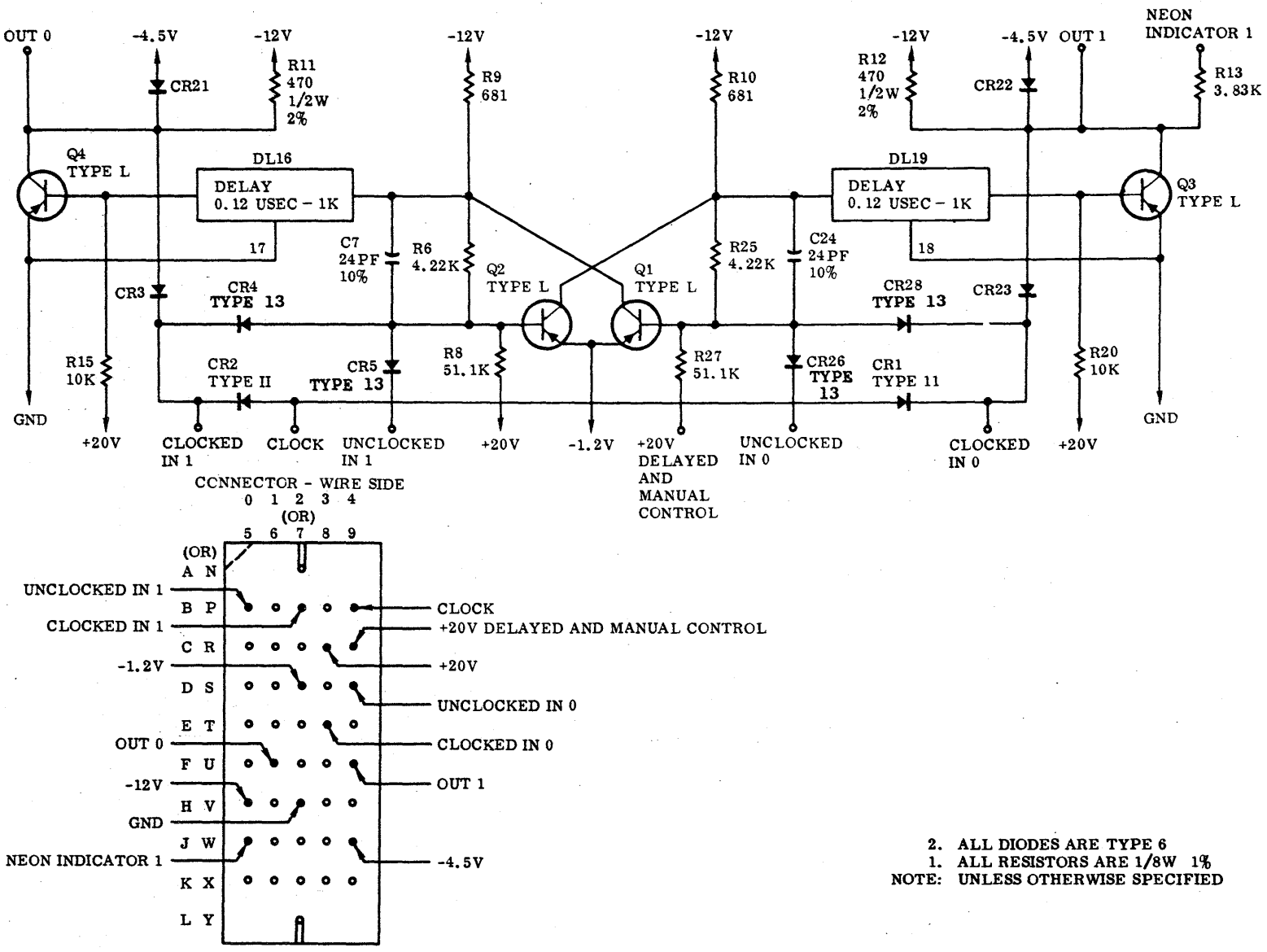
The +20V, and +20V Delayed provide the off bias for the transistors. The -1.2V is used to give an input voltage threshold. If the emitter of Q1 and Q2 were grounded, a false input level, $V_{IN}$, no more negative than -0.5V could trigger the flip-flop. This is unacceptable for logical operation since the false levels of the input gates may be as negative as -1.2V.

The -12V provides collector voltages and the base currents for the circuit.

The -4.5V prevents the true output levels from going excessively negative. This reduces voltage swings and the time required to charge and discharge stray capacitance. This also reduces the collector voltages on Q3 and Q4.

## PACKAGE SCHEMATIC

Refer to Figure 6.24-10 for the complete schematic of the flip-flop 20-70 parallel plate package.




2. ALL DIODES ARE TYPE 6
1. ALL RESISTORS ARE 1/8W 1%
NOTE: UNLESS OTHERWISE SPECIFIED

FIGURE 6.24-10. FLIP-FLOP 20-70 PACKAGE SCHEMATIC

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## 6.25 SWITCH I

### GENERAL DESCRIPTION

The standard Switch I is intended for use as an active element in current-steering diode-mode logical circuitry. The switch always inverts and amplifies the incoming signal. The logical is used as an inverter.

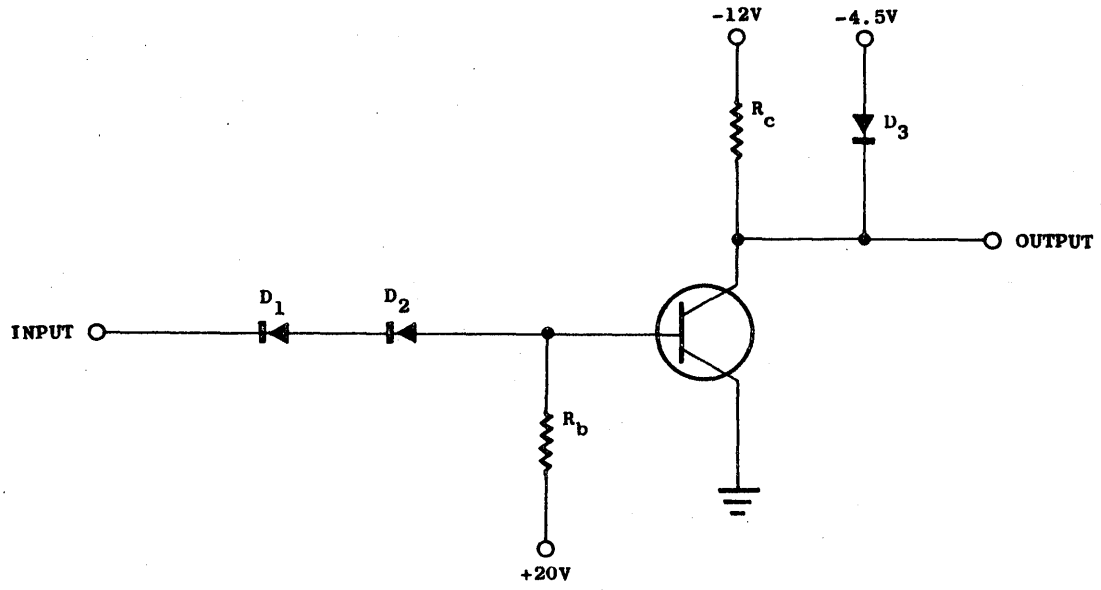



FIGURE 6.25-1. SWITCH I SCHEMATIC

### COMPONENTS

The circuit consists of one transistor stage with associated components. Diodes CR1 and CR2 are silicon diodes (stabistors) with a forward drop in the range of 0.5V.

The purpose is to hold the transistor base 1V positive with respect to the input. This guarantees that the switch will be back-biased even if the input goes to -1V.

The resistor $R_b$ is used as a pull-up resistor during the back-biasing of the transistor. It also supplies the ICBO protection and the current to remove base charge during the transistor turn-off. The transistor Q1 is the active element in the circuit. It is a PNP germanium transistor of the mesa design and provides the amplification and inversion of the signal. Diode CR3 is used to clamp the output voltage at -4.5V. This clamping action drastically reduces the switching dissipation of the transistor. Resistor $R_c$ is the collector supply return, the value of which is determined by expected loads.

### OPERATION

The following is a description of the basic operation of the circuit.

Assuming the transistor is OFF, the input signal will be more positive than -1.0V. The base of the transistor will then be positive through the action of CR1, CR2 and Rb. The transistor is back-biased and the collector voltage is damped through CR3 to -4.5V. When the input signal becomes more negative than -1.0V, the transistor becomes forward-biased and goes into the saturation region. During this state, there is an effective amplification of the input current to the collector current in the ratio of 20:1.

PACKAGE SCHEMATIC

Refer to Figure 6.25-2 for the complete schematic of the Switch I parallel plate package.

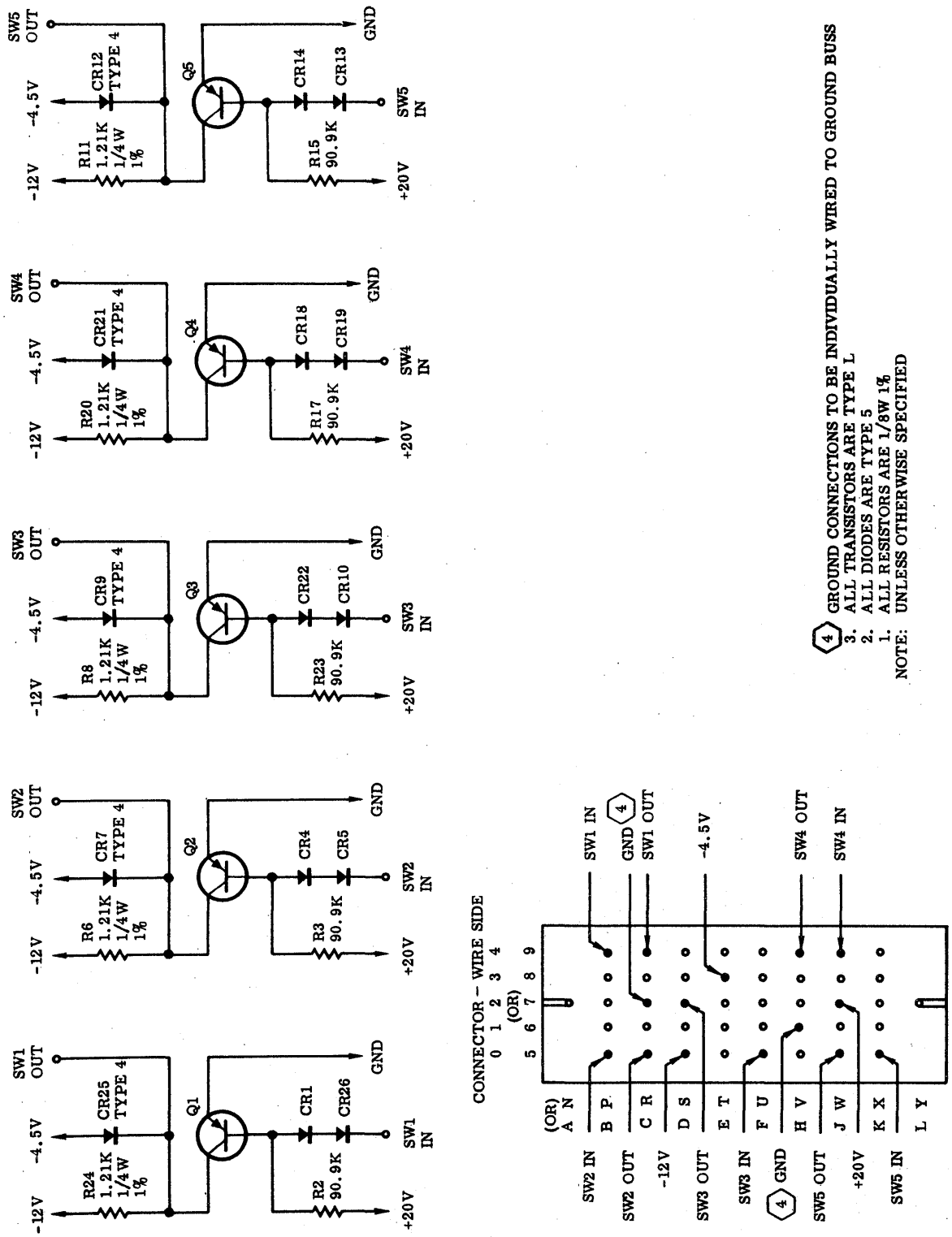



FIGURE 6.25-2. SWITCH I PACKAGE SCHEMATIC

## 6.26 DRIVER 50-90

### GENERAL DESCRIPTION

The Driver 50-90 is a non-inverting switch amplifier to be used in current mode diode logic circuitry and for driving cables and other loads requiring currents up to 90 ma. Depending on load conditions, it can operate at switching rates in excess of 5 megacycles. In current mode diode logic, the circuit restores the true and false levels as well as amplifying.

### BLOCK DIAGRAM DESCRIPTION

See Figure 6.26-1 for Driver 50-90 Block Diagram illustration.

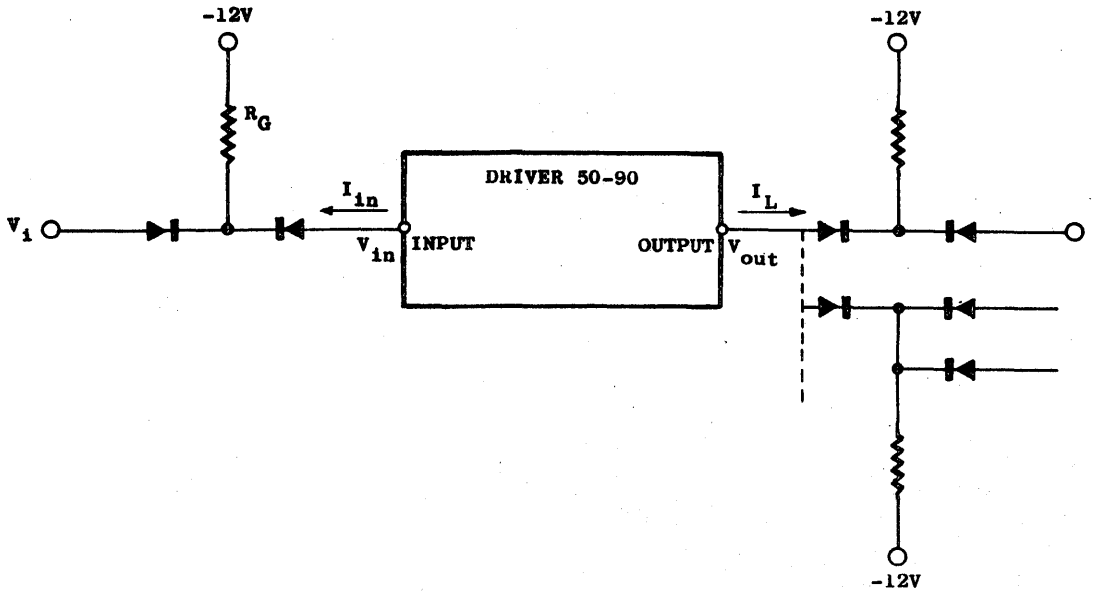



FIGURE 6.26-1. DRIVER 50-90 BLOCK DIAGRAM

A Driver has one input and one output. The output responds to input signals in one of two ways.

1. If the input signals are such as to hold the input between ground and -1.0V, then $V_0$ will be between ground and -0.3V and will be able to supply an $I_L$ of up to 90 ma.

2. If the input signals can produce an $I_{in}$ of 1 ma or more (occurring when $V_i$ is more negative than -1.8V), then $V_0$ will be more negative than -4.5V provided $I_L$ is no greater than -8.0 ma.

### CIRCUIT DESCRIPTION

Refer to Figure 6.26-2 for working schematic of Driver 50-90.

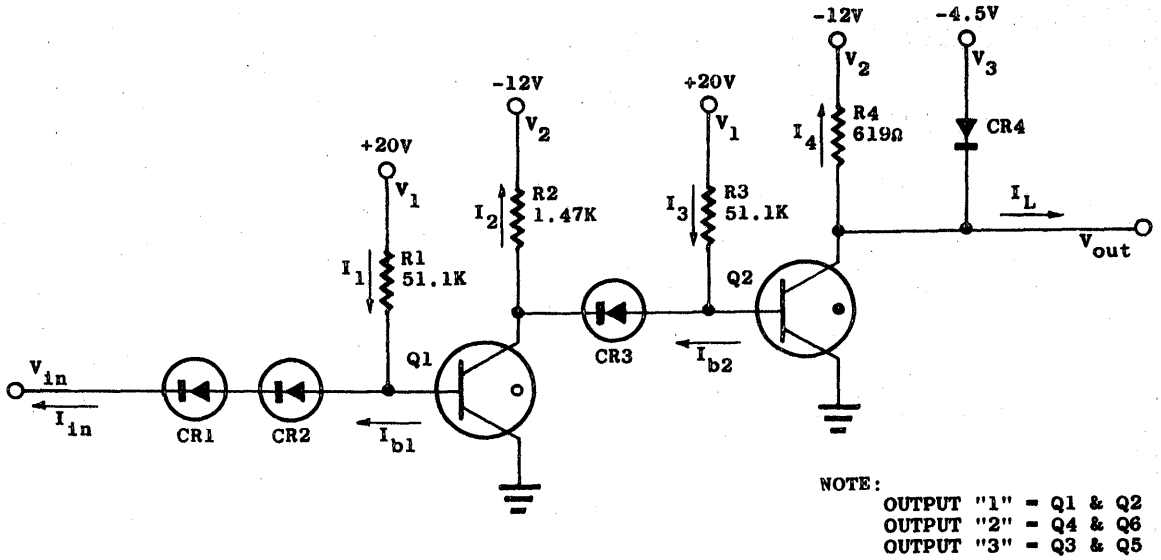



FIGURE 6.26-2. DRIVER 50-90 CIRCUIT SCHEMATIC

Driver 50-90 is basically two switches connected serially. The two states described under Block Diagram Description occur as follows:

1. When $V_{in}$ is -1.0V or more positive, $V_{b1}$ is at ground or above, due to the forward drop characteristics of silicon diodes CR1 and CR2. With $V_{b1}$ at ground, Q1 is necessarily cut off. With Q1 OFF, $I_2$ flows through CR3. This current is much greater than $I_3$ so that a large $I_{b2}$ results. $I_{b2}$ is sufficient to hold Q2 in saturation when $I_{c2}$ is as great as 119 ma. Since the maximum $I_4$ is 20 ma, $I_L$ can be as great as 90 ma.

2. When $I_{in}$ exceeds 1.0 ma, it also exceeds $I_1$ by several hundred microamps. Therefore, an $I_{b1}$ flows, which is sufficient to drive Q1 into saturation. This brings $V_{c1}$ to -0.3V. Thus, the base of Q2 is above ground so that Q2 is OFF. Thus, the base of Q2 is above ground so that Q2 is OFF. CR4 is forward-biased and supplies $I_4$ so that $V_0$ is slightly more negative than -4.5V.

SWITCHING

Refer to Figures 6.26-2 and 6.26-3.

When the input changes from the false conditions ($V_i$ more positive than -1.0V) to the true condition ($V_i$ more negative than -1.8V and $I_{in}$ > 1.0 ma), the following sequence of events occurs in the driver.

1. $I_{b1}$ starts from the cut off condition in which no forward current flows.

2. When $I_{in}$ exceeds $I_1$, $I_{b1}$ starts flowing.

3. Q1 turns on at a rate which depends on transistor speed and available $I_{b1}$.

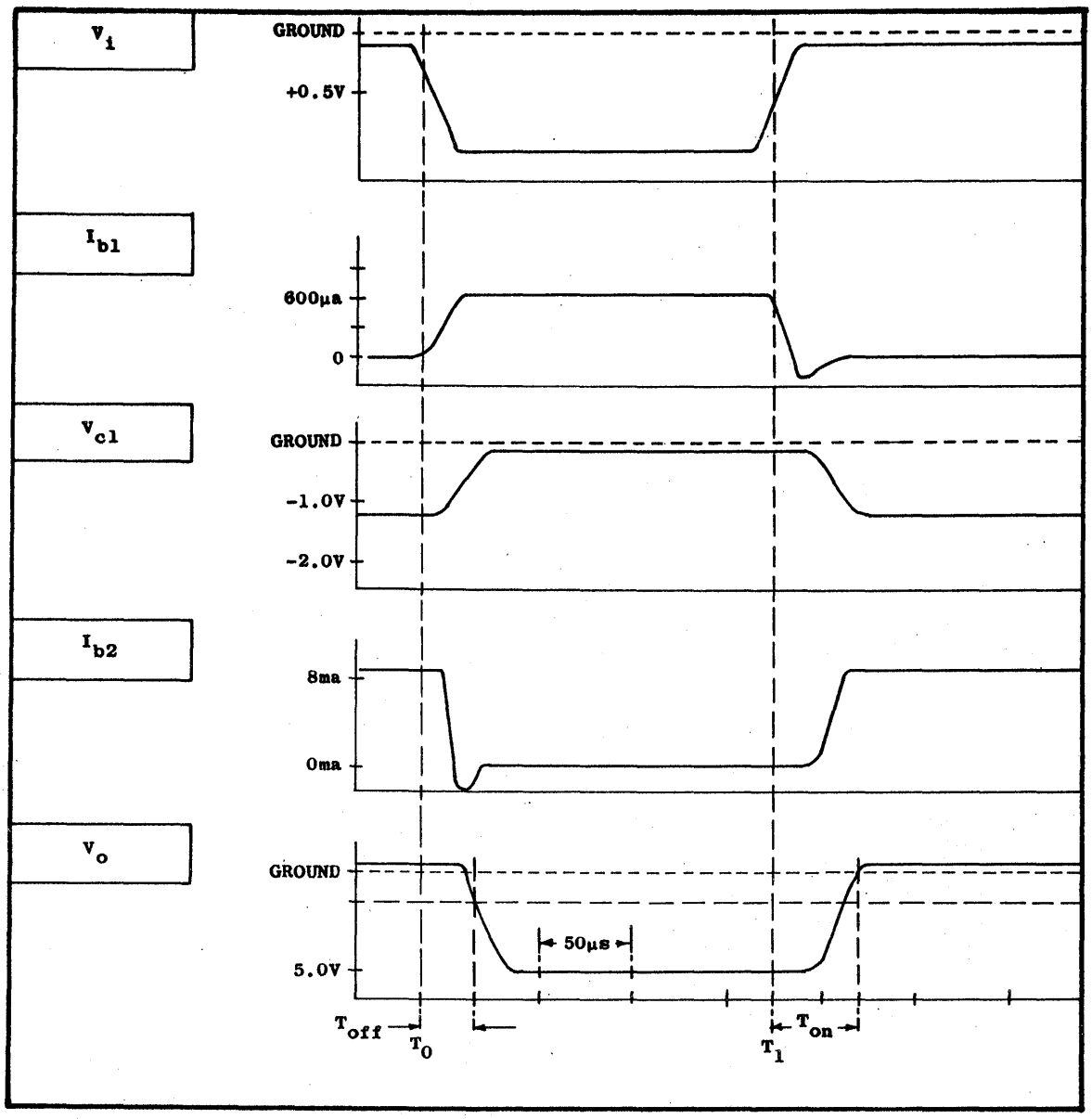



FIGURE 6.26-3. DRIVER 50-90 TYPICAL WAVEFORMS

4. $V_{c1}$ is about -1.3V when Q1 is OFF. It is clamped at this level by the sum of the forward drop of CR3 and the base emitter diode of Q2. It is driven to -0.3V as Q1 turns ON.

5. During turn on, Q2 starts supplying $I_2$ so that $I_{b2}$ is reduced. Also during this period, CR3 which is a stabistor, looks like a battery so that some reverse current may flow through it even though it is forward-biased. This reverse current and $I_3$ combine to sweep out the stored base charge of Q2 and turn Q2 OFF in the shortest possible time.

6. When Q2 turns OFF, $V_0$ falls. The rate at which $V_0$ falls will depend primarily on the output load conditions.

When the input goes from this true state to the false state, the reverse sequence occurs.

PACKAGE SCHEMATIC

Refer to Figure 6.26-4 for the complete schematic of the Driver 50-90 Parallel Plate Package.

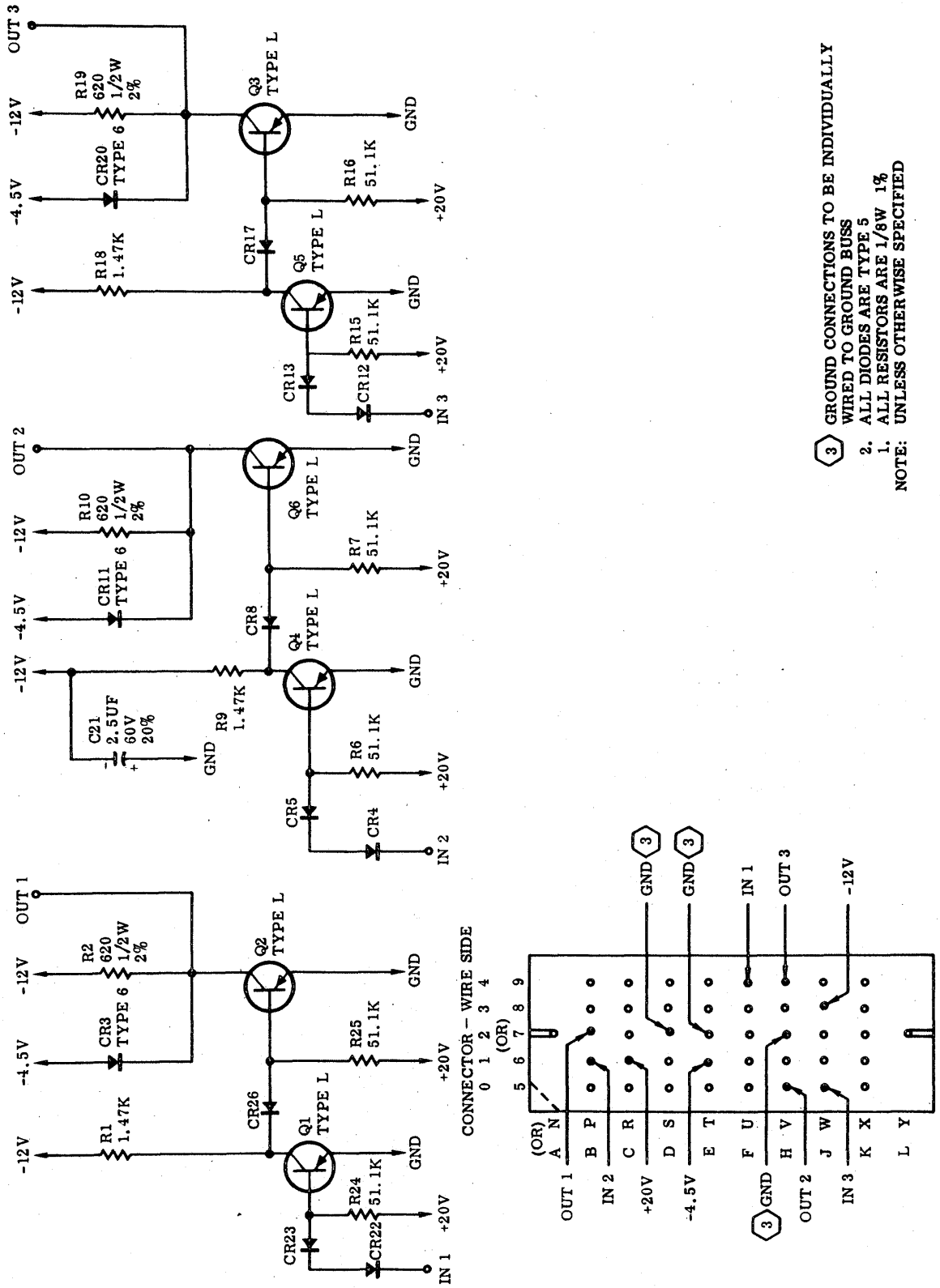



FIGURE 6.26-4. DRIVER 50-90 PACKAGE SCHEMATIC

## 6.27 DELAY "A"

### GENERAL DESCRIPTION

The Delay "A" is a delay circuit of the holdover type to be used in current steering diode logic. The output in the quiescent state is false. When a short negative pulse (0.10 to 0.20 μs) is received, the output becomes true. With this type input, the delay time is measured from the beginning of the input pulse.

If after at least 25 percent of the delay time, a second input pulse is received, the output will continue true and will now be timed from the beginning of the second pulse. The circuit may thus be kept in the true state for any desired length of time by the repeated application of short input pulses.

After the conclusion of the last input pulse, the circuit will time out the delay and then return to the false state.

The delay time is determined by the choice of two capacitors and by the adjustment of a potentiometer.

### CIRCUIT DESCRIPTION

Refer to Figure 6.27-1 for circuit schematic and to Figure 6.27-2 for Delay "A" Timing.

### INITIATE OUTPUT PULSE

In the quiescent condition, Q1 is cut OFF, Q2 is conducting, and Q3 and Q4 are saturated. At this time, the potential at the input terminal is -1.2V.

When a negative pulse of greater magnitude is applied to the input terminal so that the potential lies in the range of -1.4V to -2.2V, Q1 will begin to conduct. The input voltage cannot go more negative than this because the base emitter diode of Q1 will act as a clamp.

When Q1 begins to conduct, the collector which has been resting at -6.0V will start toward its saturation voltage of about -0.3V. The collector is restrained by capacitors C12 and C14 so that approximately 6 coulombs must be removed from these capacitors before saturation is reached. The time required for this is called $T_a$. In general, $T_a = T_{in}$. Therefore, it is necessary to supply current to hold Q1 ON until the end of $T_a$. The collector current of Q1 is derived between R9, C12 and C14. That portion which flows in C14 is applied to the base of Q3 to turn Q3 OFF. When Q3 begins to turn OFF, its collector which was resting near ground, starts toward -12V. CR20 will then begin to conduct, allowing R19 to supply current to the base of Q1, thus holding Q1 ON. As soon as Q1 has become saturated, C14 receives no more current from Q1.

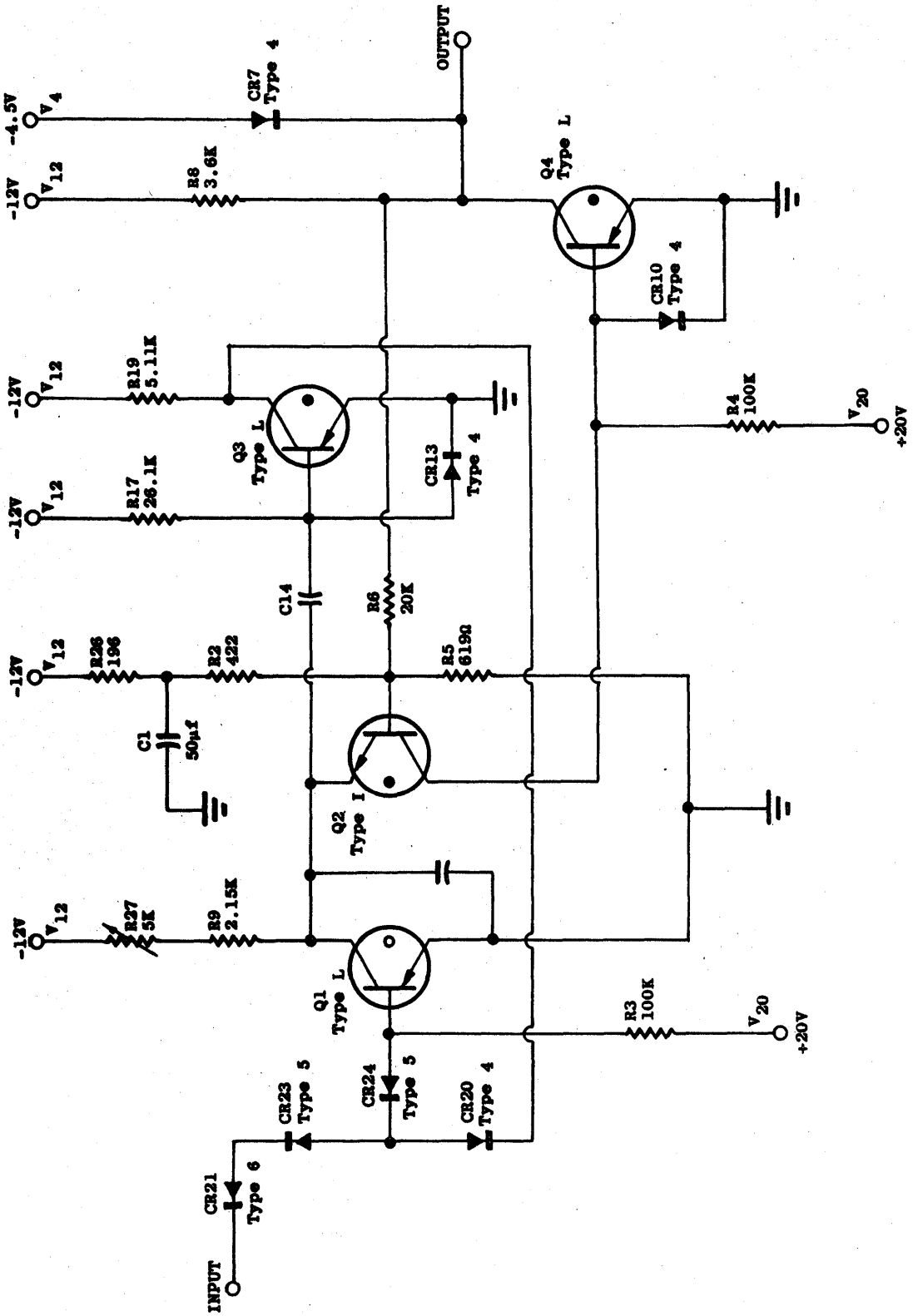



FIGURE 6.27-1. DELAY "A" CIRCUIT SCHEMATIC

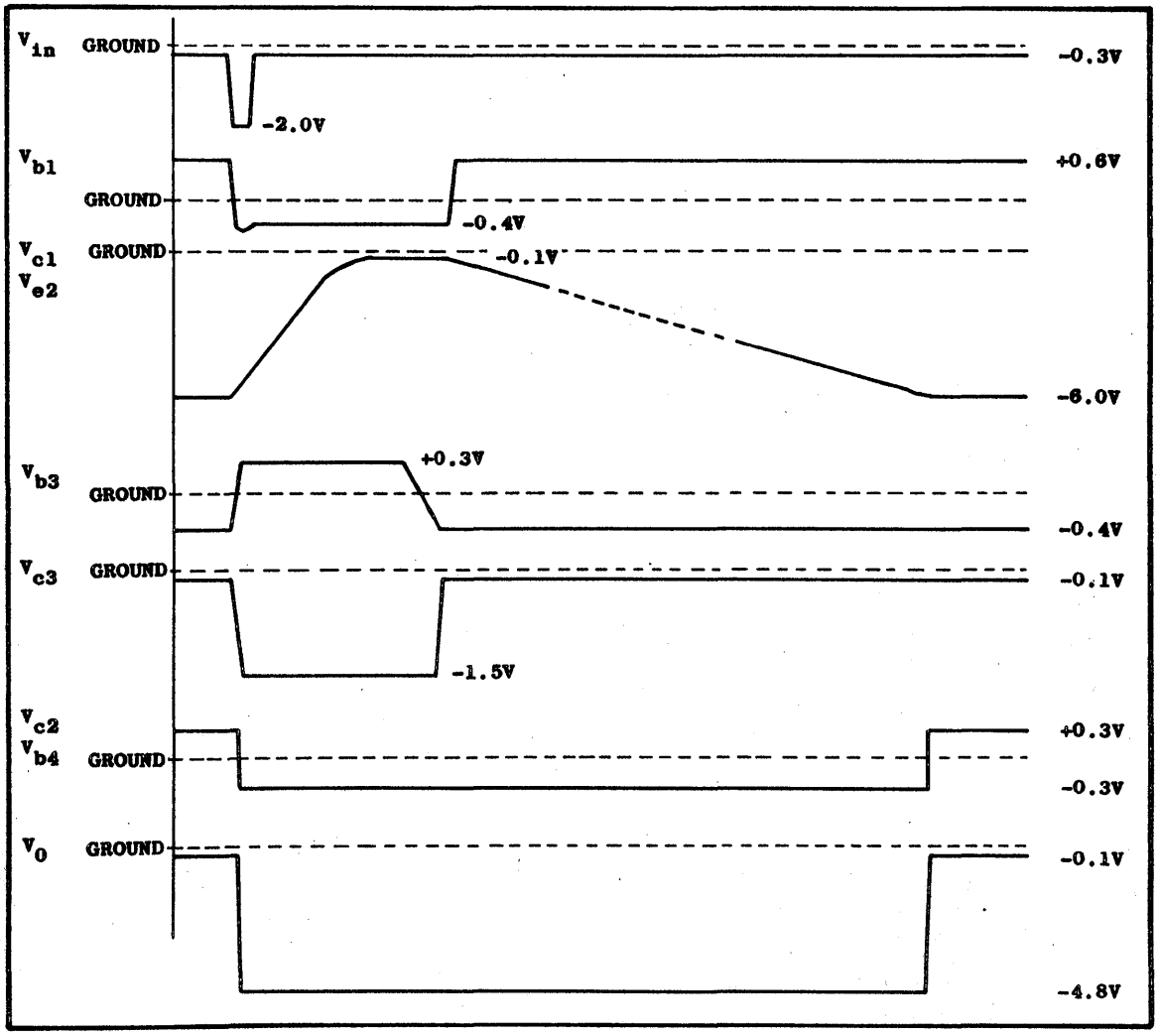



FIGURE 6.27-2. DELAY "A" TIMING

At this time, the base of Q3 will be at approximately +0.3V, being prevented from going more positive by CR13. When Q1 goes into saturation, the base of Q3 will be pulled toward -12V by R17, but will move slowly because C14 must be charged. When the base of Q3 becomes slightly negative, Q3 will begin to conduct. CR20 will then cease to conduct so that Q1 will be turned OFF. Meanwhile, as soon as the collector of Q1 has moved about 0.1V, Q2 has begun to turn OFF.

The turn OFF of Q2 removes the drive from Q4 so that it turns OFF, initiating a true output pulse

OUTPUT PULSE TERMINATION

After Q1 turns OFF, C12 and C14 begin to charge toward -12V thru R9. When the potential reaches approximately 6V, Q2 begins to turn ON. When Q2 turns ON, the collector current will begin to turn Q4 ON. When Q4 begins to turn ON, feedback through R6 will speed up the turn ON, thus terminating the output pulse.

After 20 percent of the delay time has passed, C14 will be reset and the collector of Q1 has moved far enough so that a new input pulse will re-trigger the circuit. The delay time may now be measured from the new pulse.

PACKAGE SCHEMATIC

Refer to Figure 6.27-3 for complete schematic of the Delay "A" Parallel Plate Package.

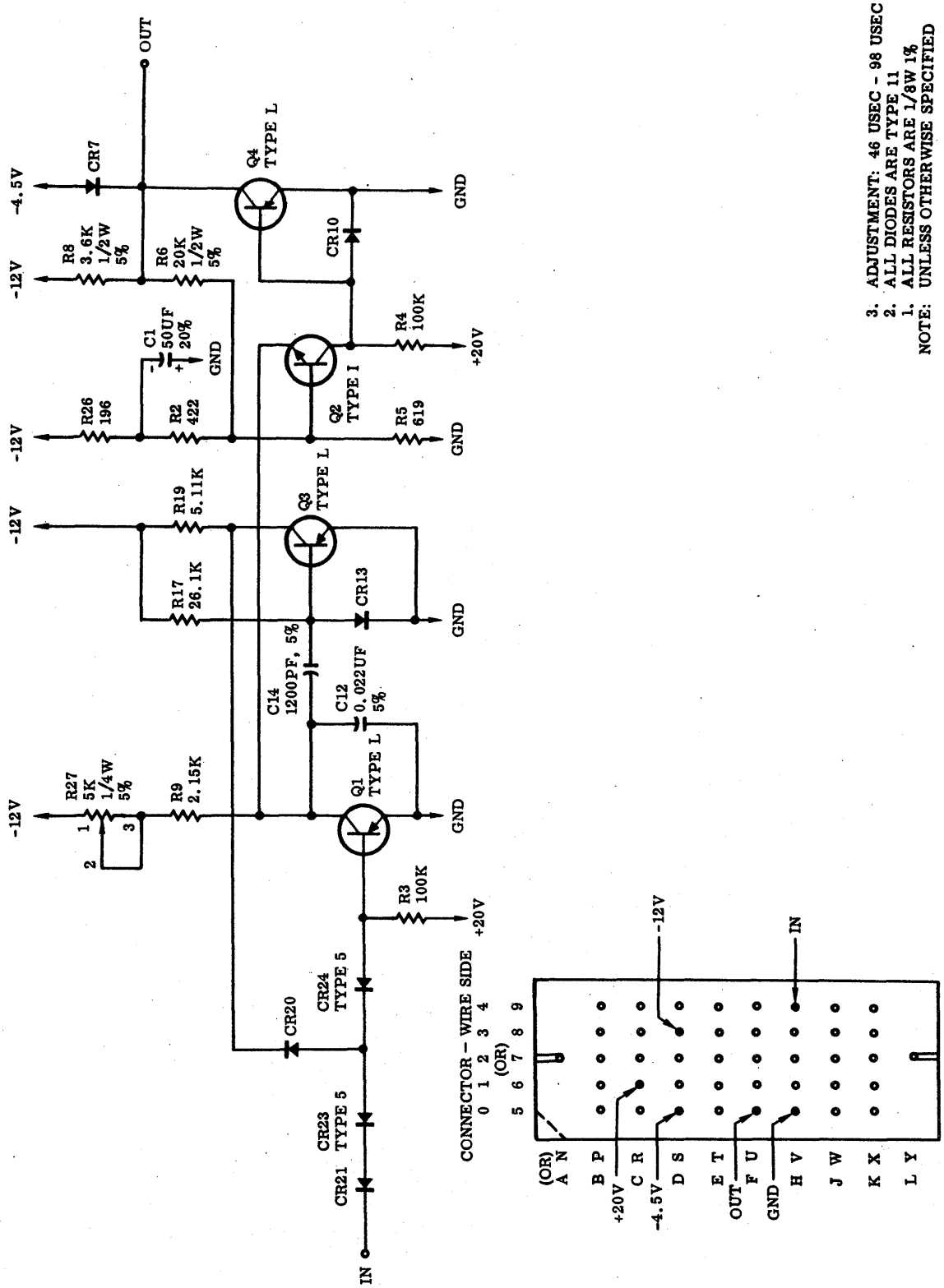



FIGURE 6.27-3. DELAY "A" PACKAGE SCHEMATIC

## 6.28 DELAY "C"

### GENERAL DESCRIPTION

The Delay "C" is a delay circuit of the holdover type. When a negative pulse of prescribed minimum width (0.11 μs) and magnitude is received at the input, the output is caused to go negative, and will remain negative until a specified delay time after the completion of the input pulse. If, before the output pulse is completed, a new input pulse of the proper length and magnitude is received, the output will continue negative until the delay time has elapsed after the completion of the last input pulse received. There is no maximum limit on length of input pulse which can be tolerated, but the delay time does not begin until the input is completed. Delay time is determined by the choice of a capacitor and by the adjustment of a potentiometer.

### CIRCUIT DESCRIPTION

Refer to Figure 6.28-1 for Delay "C" circuit schematic, and Figure 6.28-2 for Delay "C" Timing.

### INITIATION OF THE OUTPUT PULSE

In the quiescent condition, Q1 is cut OFF, Q2 is conducting, and Q3 is saturated. At this time, the potential at the input terminal is -1.0V. When a negative pulse is applied to the input terminal, the potential will become more negative and lie in the range of -1.2V to -2.2V, being prevented from going more negative by the base emitter diode of Q1. Q1 begins to conduct, causing its collector which has been resting at -6.0V, to start toward its saturation voltage of approximately -0.3V. The first change in the collector voltage will be a small step due to voltage drop across R14. Since the emitter of Q2 is connected to this point, Q2 will quickly be turned OFF. The collector of Q1 will now continue toward saturation at a rate determined by C17. The input time must be suffficient (0.11 μs) to allow this process to reach completion if accurate timing is to be obtained.

When Q2 is turned OFF, the drive is removed from Q3 so that Q3 is quickly turned OFF. When Q3 is turned OFF, the output pulse is initiated.

### CONCLUSION OF THE OUTPUT PULSE

At the conclusion of the input pulse, Q1 turns OFF and C17 begins to charge toward -12V through R21 and R27. When the potential reaches -6.0V, Q2 will begin to turn ON. When Q2 begins to turn ON, Q3 will also begin to conduct. As soon as the current at the collector of Q3 is sufficient to cause the collector voltage to charge, the base of Q2 will be made slightly more positive. This brings Q2 further into conduction and speeds the turn ON of Q3. When Q3 goes into conduction, the output pulse is terminated. If at any time during the above delay cycle, a new input pulse of sufficient length is received, C17 will again discharge, initiating a new delay.

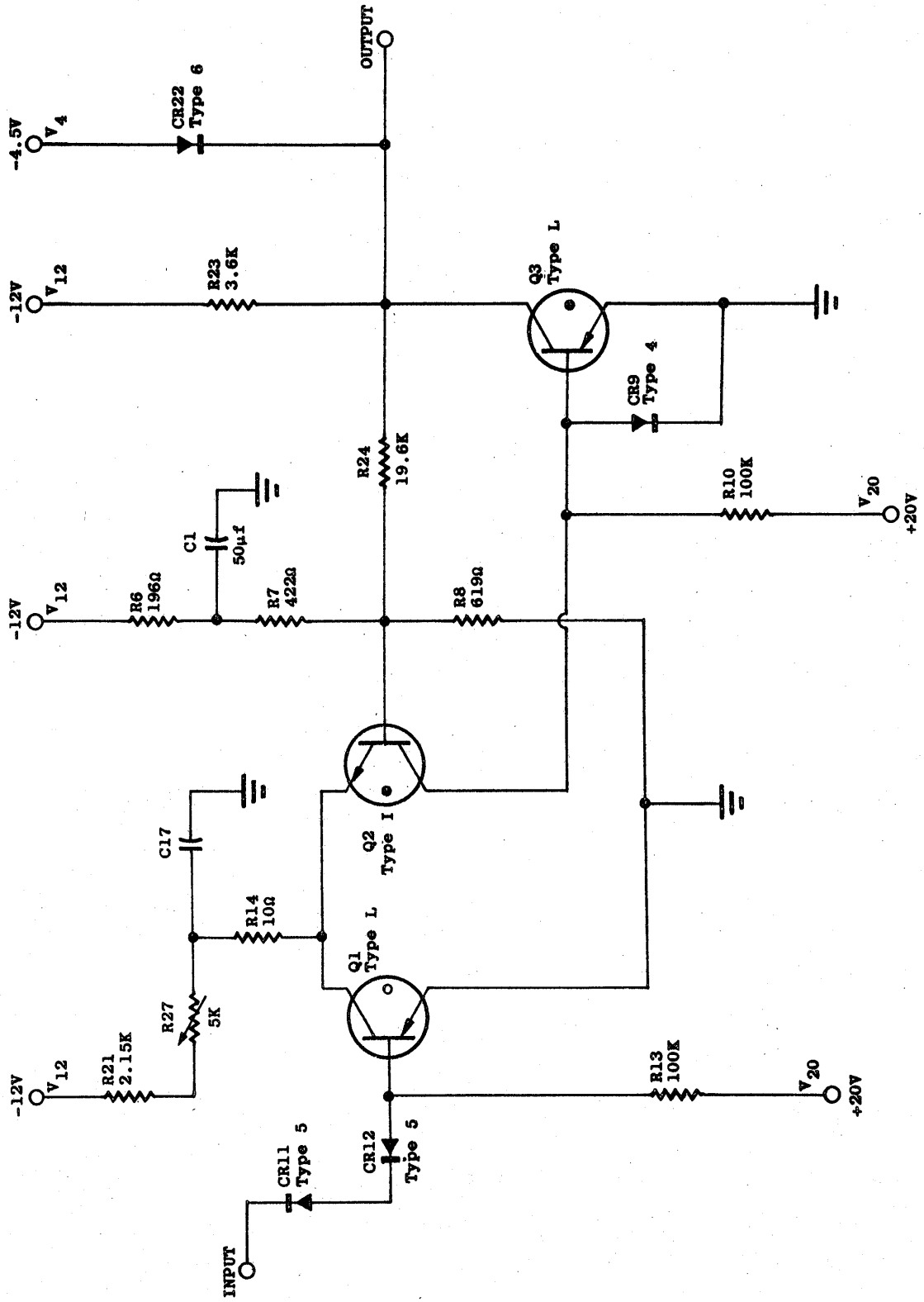



FIGURE 6.28-1. DELAY "C" CIRCUIT SCHEMATIC

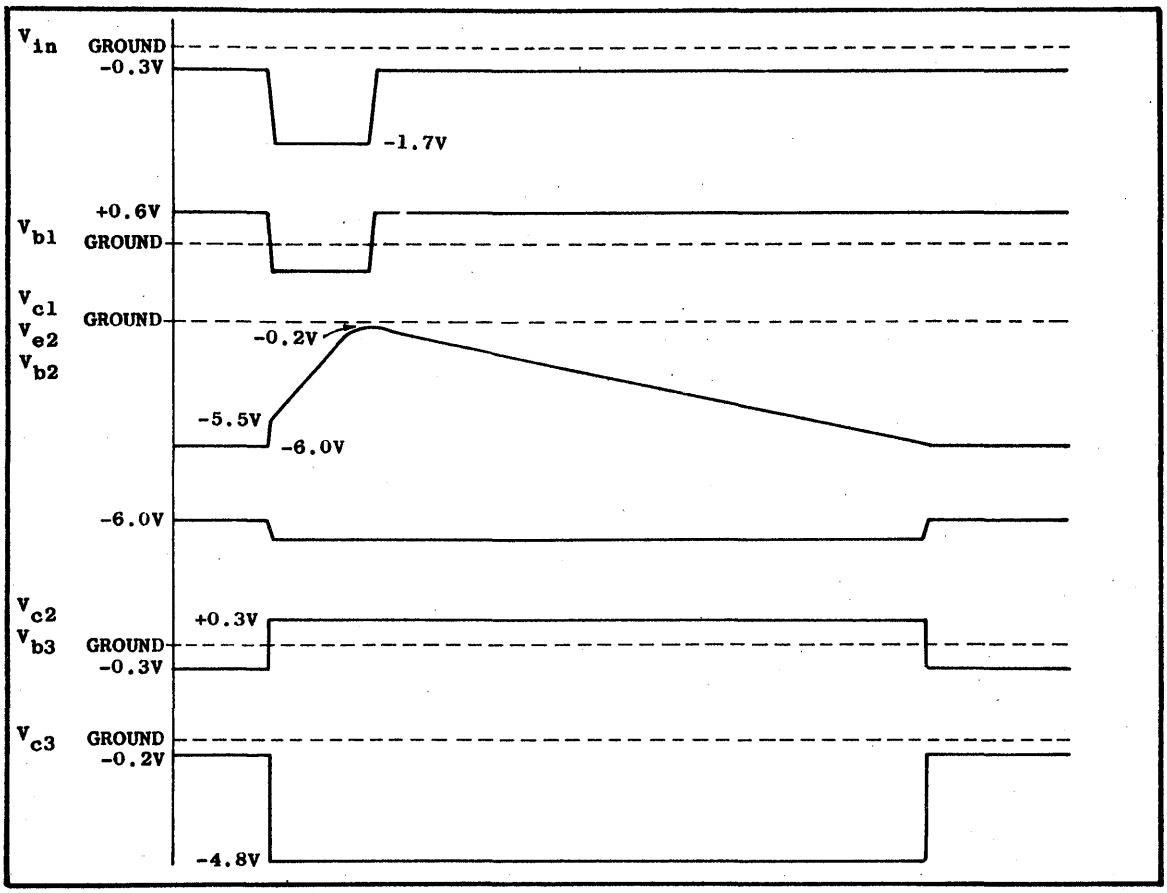
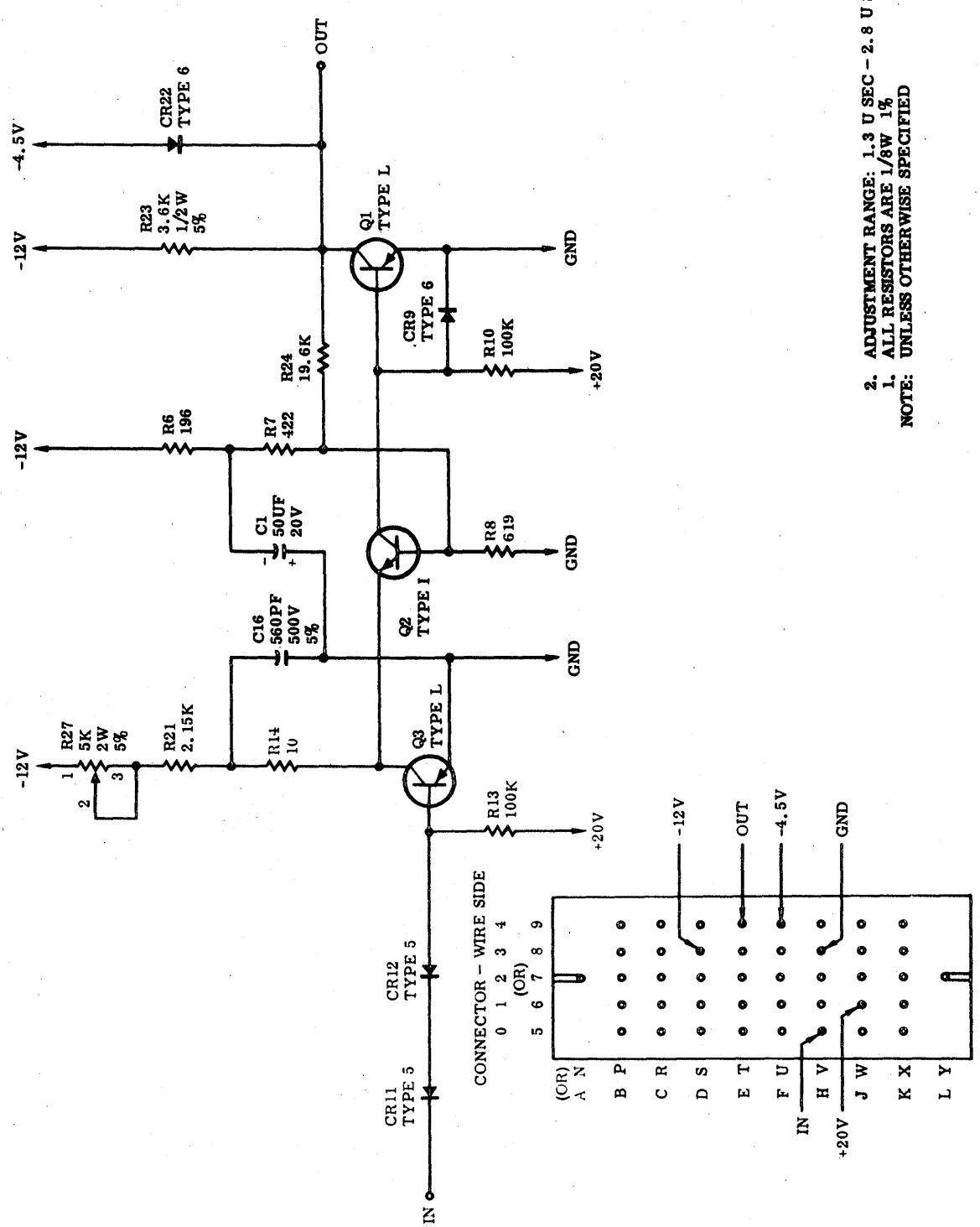



FIGURE 6.28-2. DELAY "C" TIMING

PACKAGE SCHEMATIC

Refer to Figure 6.28-3 for the complete schematic of the Delay "C" Parallel Plate Package.




2. ADJUSTMENT RANGE: 1.3 U SEC - 2.8 U SEC
1. ALL RESISTORS ARE 1/8W 1%
NOTE: UNLESS OTHERWISE SPECIFIED

FIGURE 6.28-3. DELAY "C" PACKAGE SCHEMATIC

# 6.29 MULTI

## GENERAL DESCRIPTION

The Multi is a delay circuit of the "Multi" type which differs from most Multis in that no allowance need be made for reset time because the reset time is included in the delay.

When a negative pulse of 0.1 μs or greater width, and at least 1100 μamp magnitude is received at the input, the output is caused to go negative and will remain negative until a specified delay time after the application of the input pulse.

If a new input pulse is received before the reset portion of the delay begins, the pulse will not be accepted; the delay time will be measured from the application of the first pulse.

If an input pulse is received during reset time, the pulse will be accepted but will result in an unpredictable delay time.

If the logic allows an input to arrive during reset time, provision is made for inhibiting the input during this time by means of an external switch circuit driven by the output of the delay circuit. The length of the input pulse is not to be longer than the delay time minus the reset time in the first case, or longer than the delay time in the second.

Delay time is determined by the choice of one capacitor and by the adjustment of a potentiometer.

## CIRCUIT DESCRIPTION

Refer to Figure 6.29-1 for Delay "B" Multi circuit schematic, and Figure 6.29-2 for Delay "B" Multi Timing.

## INITIATION OF THE OUTPUT PULSE

In the quiescent state, Q1 is cut OFF, Q2 is conducting, and Q3 and Q4 are in saturation. At this time, the potential at the input is 0 to -1.1V. When a negative pulse equal to or greater than 400 μamp is applied to the input terminal, the potential will become more negative and lie in the range of -1.7V to -2.5V. It is prevented from going more negative by the base emitter diode Q1.

Q1 begins to conduct, causing the collector which has been resting at -6.0V, to start toward its saturation voltage of -0.3V. As soon as the collector of Q1 has moved 0.3V in the positive direction, Q2 will turn OFF because its emitter is tied to the collector of Q1. As soon as Q2 begins to turn OFF, the base of Q4 will go positive, causing Q4 to turn OFF and thus initiating the output pulse.

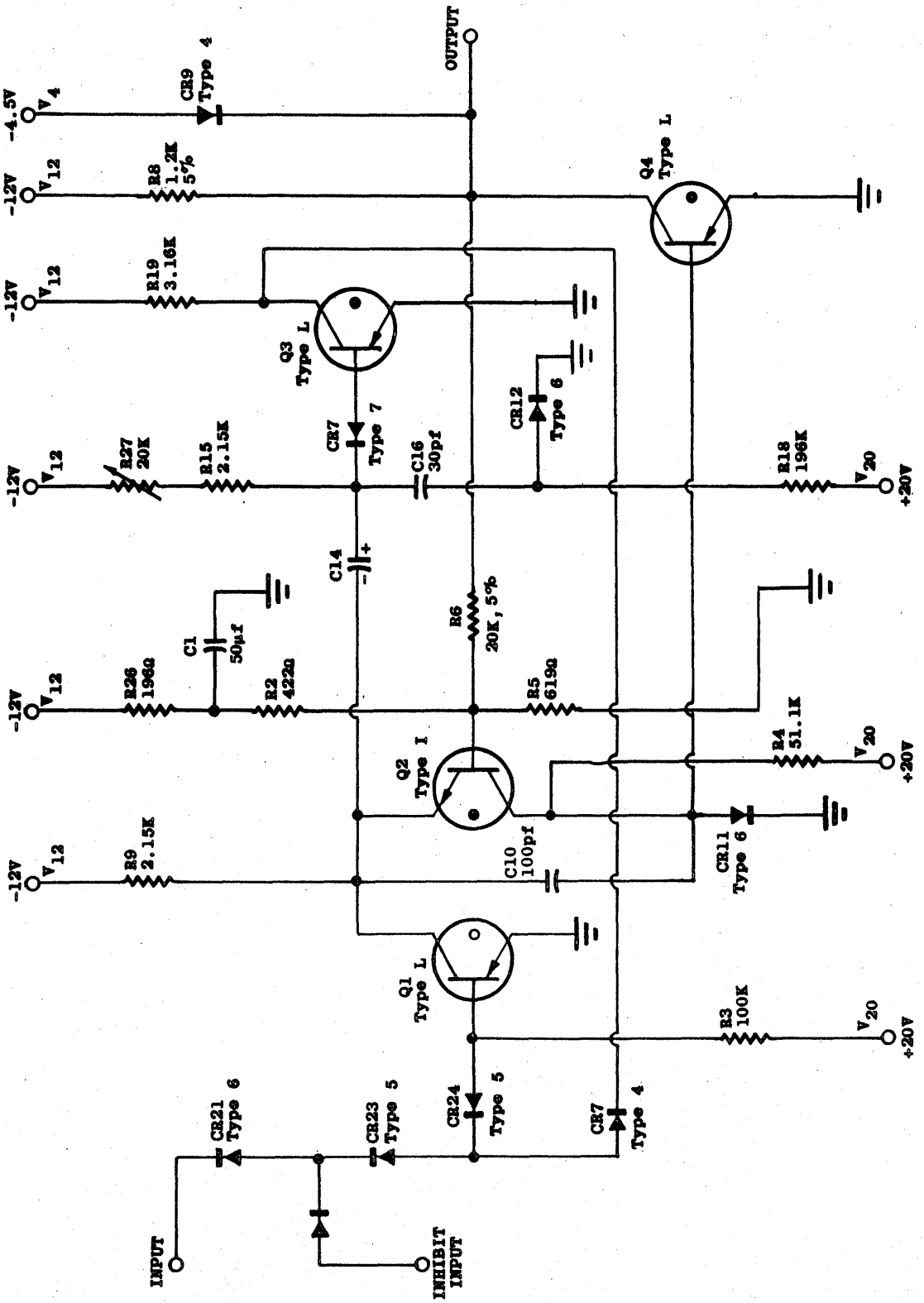



FIGURE 6.29-1. DELAY MULTI "B" CIRCUIT SCHEMATIC

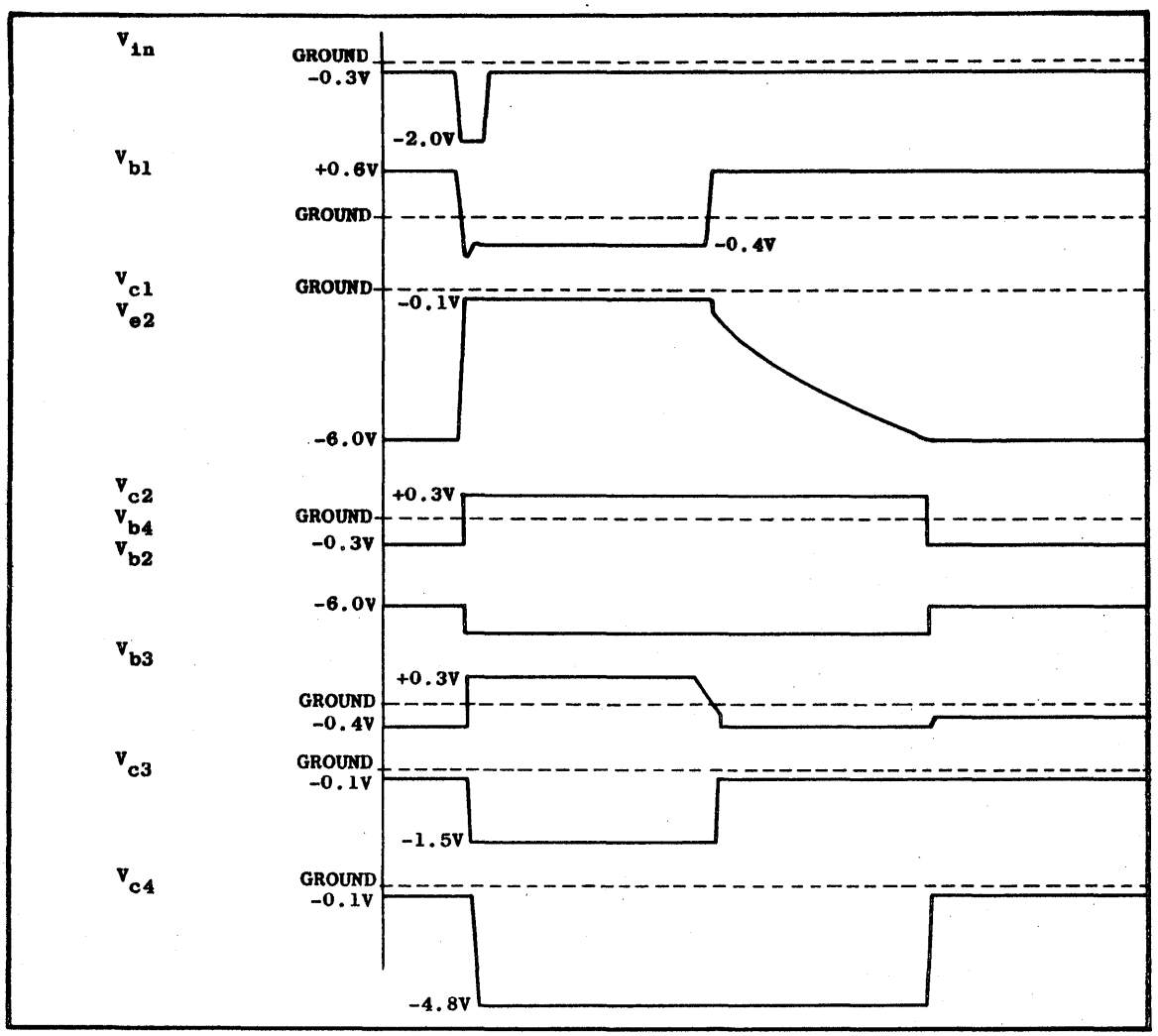



FIGURE 6.29-2. MULTI TIMING

THE DELAY HALF CYCLE

When the collector of Q1 goes toward ground, capacitor C14 cannot discharge instantaneously, so the base of Q3 is driven positive, resulting in the transistor being turned OFF.

When Q3 is turned OFF, the base of Q1 is held negative so that the collector of Q1 is brought to -0.3V and held there as long as Q3 is cut OFF.

The cathode of CR17 which is now at +6.0V, begins to move toward -12V as C14 is charged through R15 and R27. When this point begins to go negative, Q3 will begin to turn ON. When Q3 turns ON, Q1 will turn OFF (assuming that there is no input at this time).

THE RESET HALF CYCLE

When Q1 turns OFF, its collector starts toward -12V, being restrained by C14.

When the collector of Q1 reaches -6.0V, Q2 will begin to turn ON. When Q2 turns ON, Q4 will be turned ON, thus ending the output pulse.

The circuit is now ready to receive a new input and repeat the above cycle.

INHIBIT

The input is automatically inhibited during the time Q3 is OFF, but a separate inhibit input has been provided to prevent triggering during the reset time if this is desirable.

The complete inhibit circuit was not included in this package because in most cases, no pulses would be received during this time. The use of this inhibit input with an external switch is shown in Figure 6.29-3.

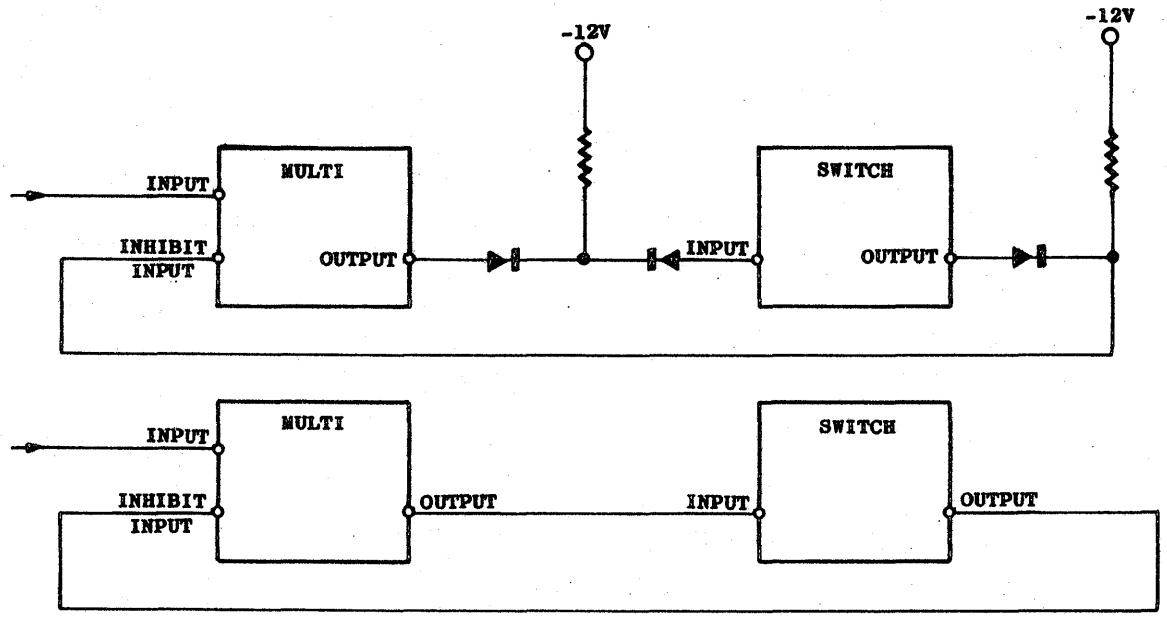



FIGURE 6.29-3. POSSIBLE CONNECTIONS FOR INHIBIT CIRCUIT

The true output from the multi circuit produces a false output from the switch, which when applied to the inhibit input (a shunt AND) prevents an input from reaching the base of Q1.

PACKAGE SCHEMATIC

Refer to Figure 6.29-4 for the complete schematic of a Multibrator Parallel Plate Package.

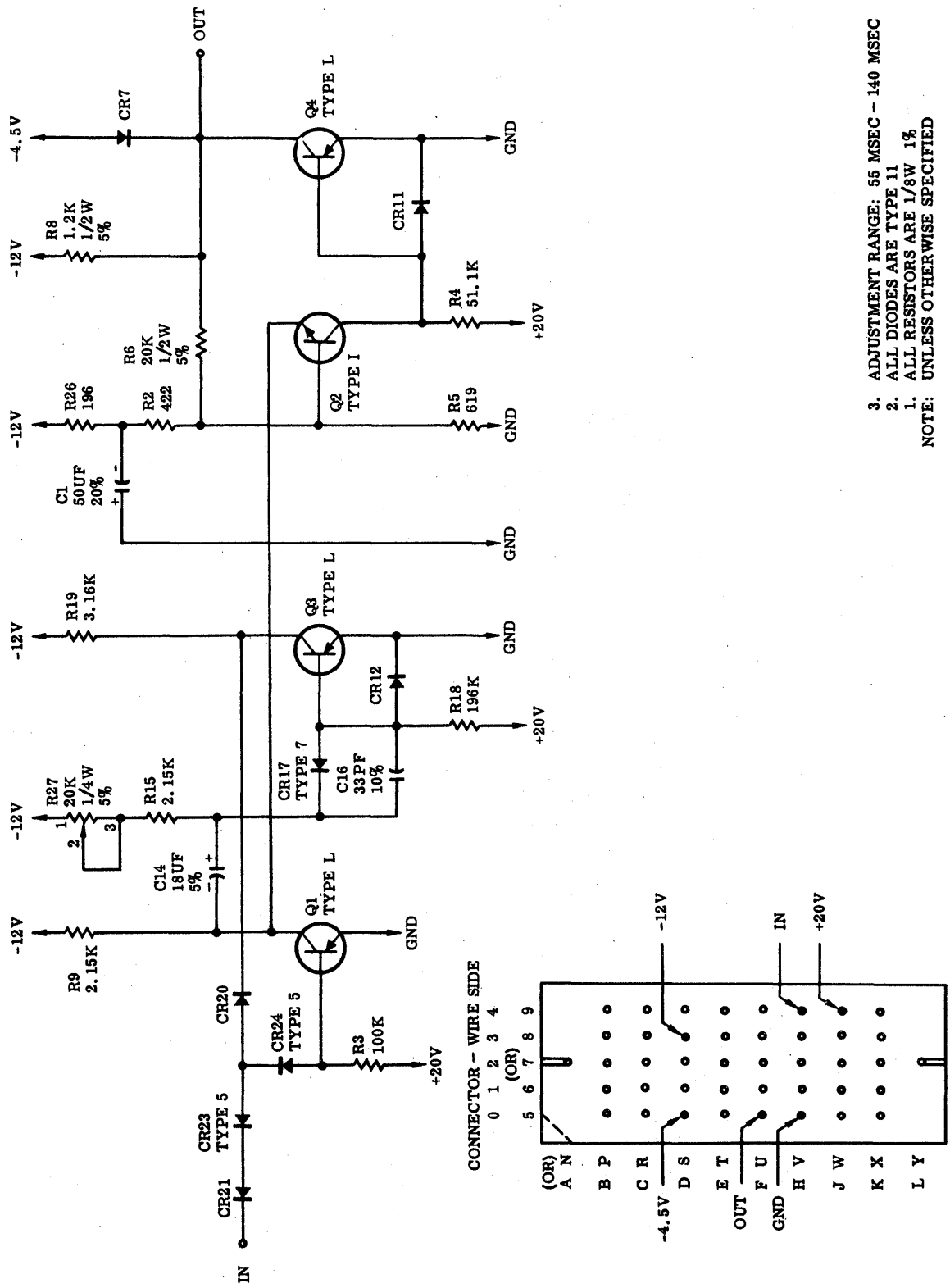



FIGURE 6.29-4. MULTIVIBRATOR PACKAGE SCHEMATIC

## 6.30 COMPRESSOR

### GENERAL DESCRIPTION

The Compressor is a circuit which produces an output pulse of about 0.400 μs when an input pulse longer than 1 μs is received.

The output of the circuit is primarily meant to trigger a flip-flop.

### BASIC CIRCUIT

Refer to Figure 6.30-1.

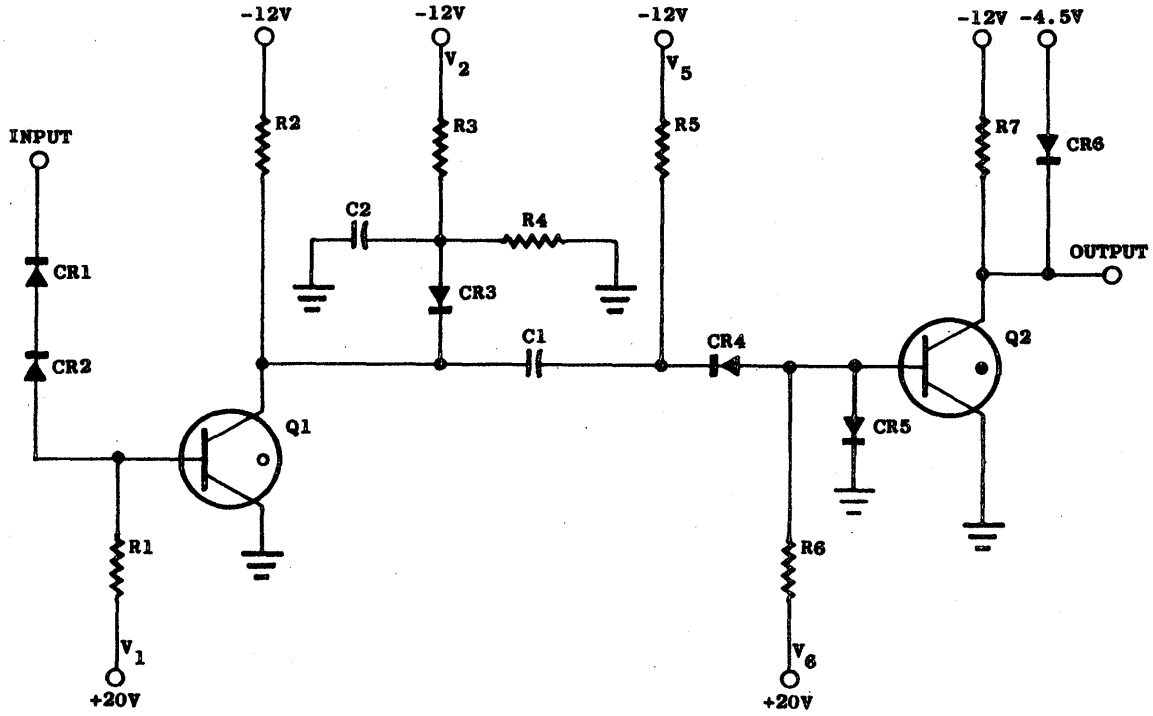



FIGURE 6.30-1. COMPRESSOR CIRCUIT SCHEMATIC

The circuit is basically a monostable multivibrator, except for the fact that no feedback is used since the input pulse is longer than the desired output pulse.

In its stable state, Q1 is OFF, and Q2 is ON. For a false input, the output is false. For a true input pulse of duration longer than 1 μs, there will be a true output pulse of approximately 0.400 μs. The input must be of a minimum length, and the output will never be longer than the input.

The width of the output pulse actually produces ranges from 0.340 μs to 0.450 μs. A reset time of 0.400 μs is required.

OPERATION

Refer to Figure 6.30-1 for Compressor circuit schematic, and to Figure 6.30-2 for Compressor waveforms.

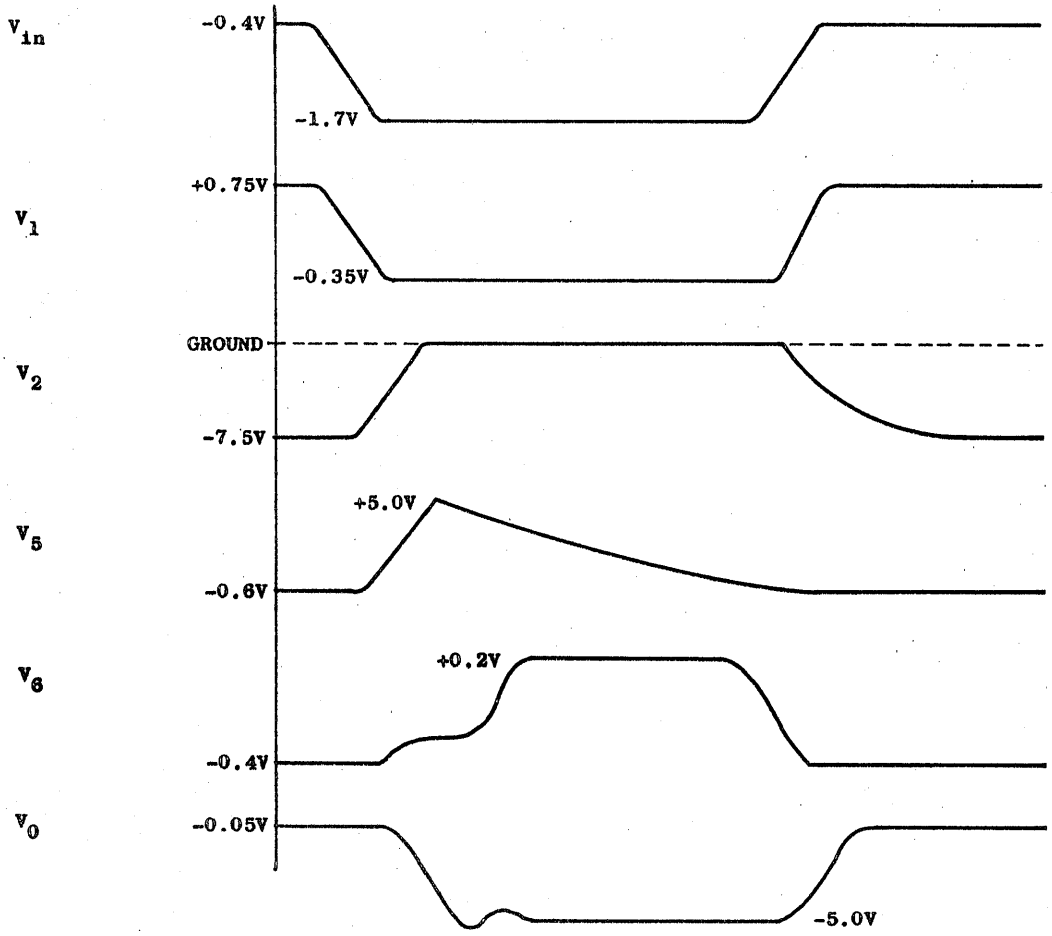



FIGURE 6.30-2. COMPRESSOR WAVEFORMS

BEGINNING OF CYCLE

In the quiescent state, Q1 is OFF and Q2 is ON. At this time, the input voltage is -0.2V to -1.0V. When a true input pulse is applied, transistor Q1 will turn ON. The potential at the input will be in the range of -1.3V to -2.0V. It will not be any more negative because of the clamping action of Q1, CR1 and CR2. As Q1 is turned ON, its collector will swing from a potential of about -7.0V to about -0.2V. $V_5$, normally at about -0.6V, now rises through capacitor C1 to a potential of about +5.0V.

DURATION OF OUTPUT

As soon as $V_5$ becomes more positive than -0.6V, Q2 starts turning OFF and the stored charges in CR4 and the base of Q2 just about cancel out. The time during which $V_5$ is greater than -0.6V is mainly determined by the RC combination of C1 and R5. The output of the circuit is true during this same time, minus the rise time, plus the fall time.

RESET

At the end of the input pulse when $V_{in}$ reaches -1.0V in the positive direction, Q1 is turned OFF, but $V_2$, the voltage at the collector of Q1, cannot change instantly from about -0.2V to about -7.0V. The reset time is determined by the RC combination of R2 and C1. The minimum duration of a complete cycle is equal to the length of the input pulse plus the reset time.

PACKAGE SCHEMATIC

Refer to Figure 6.30-3 for the complete schematic of the Compressor Parallel Plate Package.

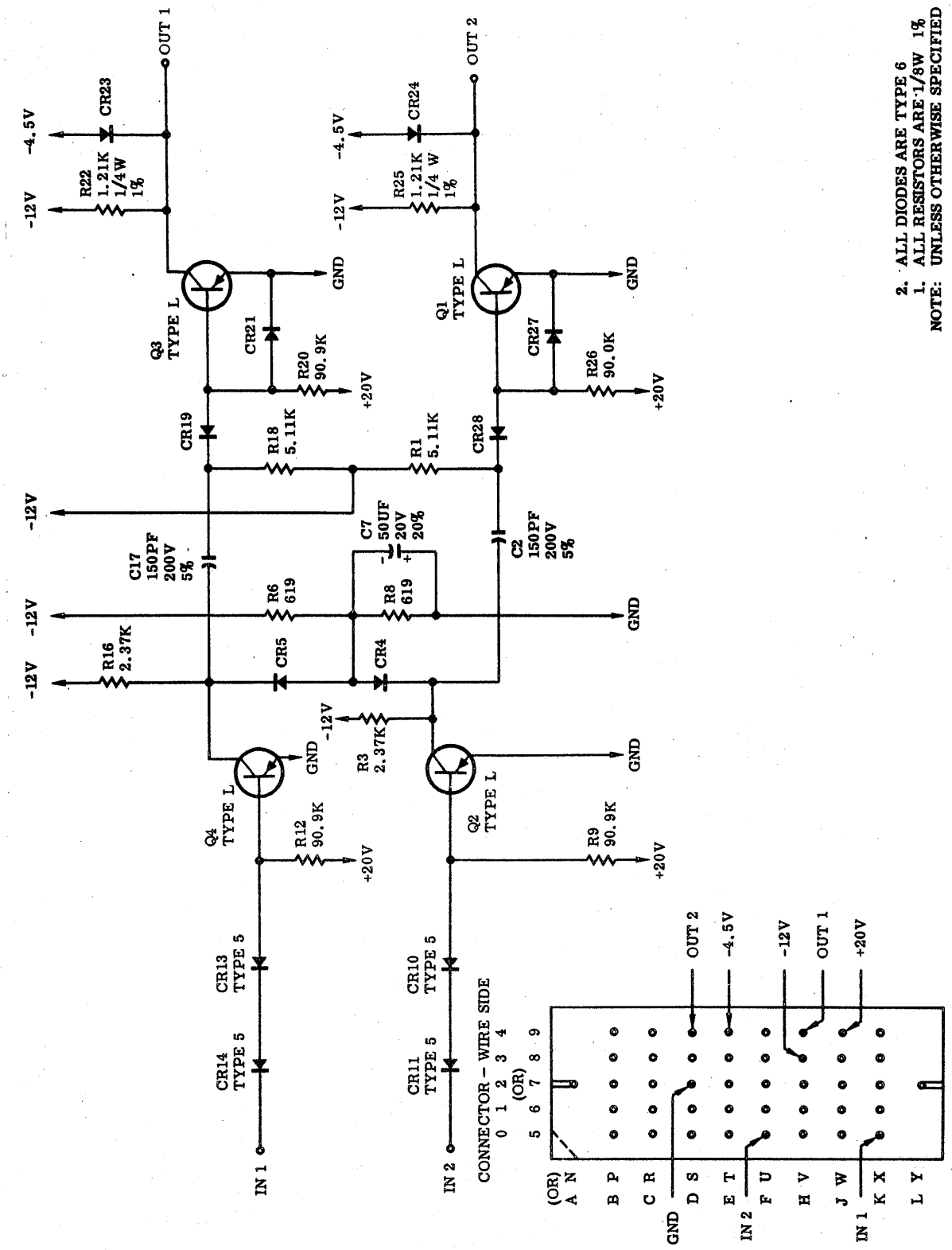



FIGURE 6.30-3. COMPRESSOR PACKAGE SCHEMATIC

## 6.31 PULSE SYNCHRONIZER

### GENERAL DESCRIPTION

The Pulse Synchronizer is a circuit which synchronizes a pulse with a level.

There are two inputs to the circuit. One input is a negative going clock pulse of a given width and frequency, and the other is a negative going logical level whose maximum width or frequency is not specified. However, the minimum duration of the logical level must be such that it overlaps at least two clock pulses. A certain minimum reset time must be allowed to elapse between two consecutive logical levels.

The output is true only when both inputs are true and there is only one negative going output pulse for every logical level input. The output pulse starts after the clock pulse has completed and it (output pulse) brackets one and only one input clock pulse. Refer to Figure 6.31-1.

### GENERAL OPERATION OF THE CIRCUIT

Since there must be only one input pulse for every time both inputs are true, the circuit consists of three stages.

1. To trigger the circuit with the trailing edge of the clock pulse when both inputs are true.

2. The second stage holds the circuit from triggering again with another clock pulse for the same logical level input.

3. There is a timing circuit which controls the width of the output followed by the third and final stage.

### CIRCUIT DESCRIPTION

Refer to Figure 6.31-1.

When both the level and clock are false, transistors Q1 and Q3 are in saturation, and Q2 is cut OFF.

When the clock pulse becomes true, Q1 may be driven harder. However, when the clock pulse terminates, Q1 will be cut OFF by the stored charge in C1. If the level input is false, Q2 will remain cut OFF. However, if the level input is true when Q1 is cut OFF, Q2 will be turned ON and the positive voltage at $P_1$ will be coupled to the base of Q3, turning it OFF. The output pulse width is dependent upon the RC time constant of C3 and R8. This time must be more than 1 μs, but less than 2 μs. Since point $P_1$ is fed back to the input, when $P_1$ goes positive (false) Q1 will be held off and Q1 is turned ON.

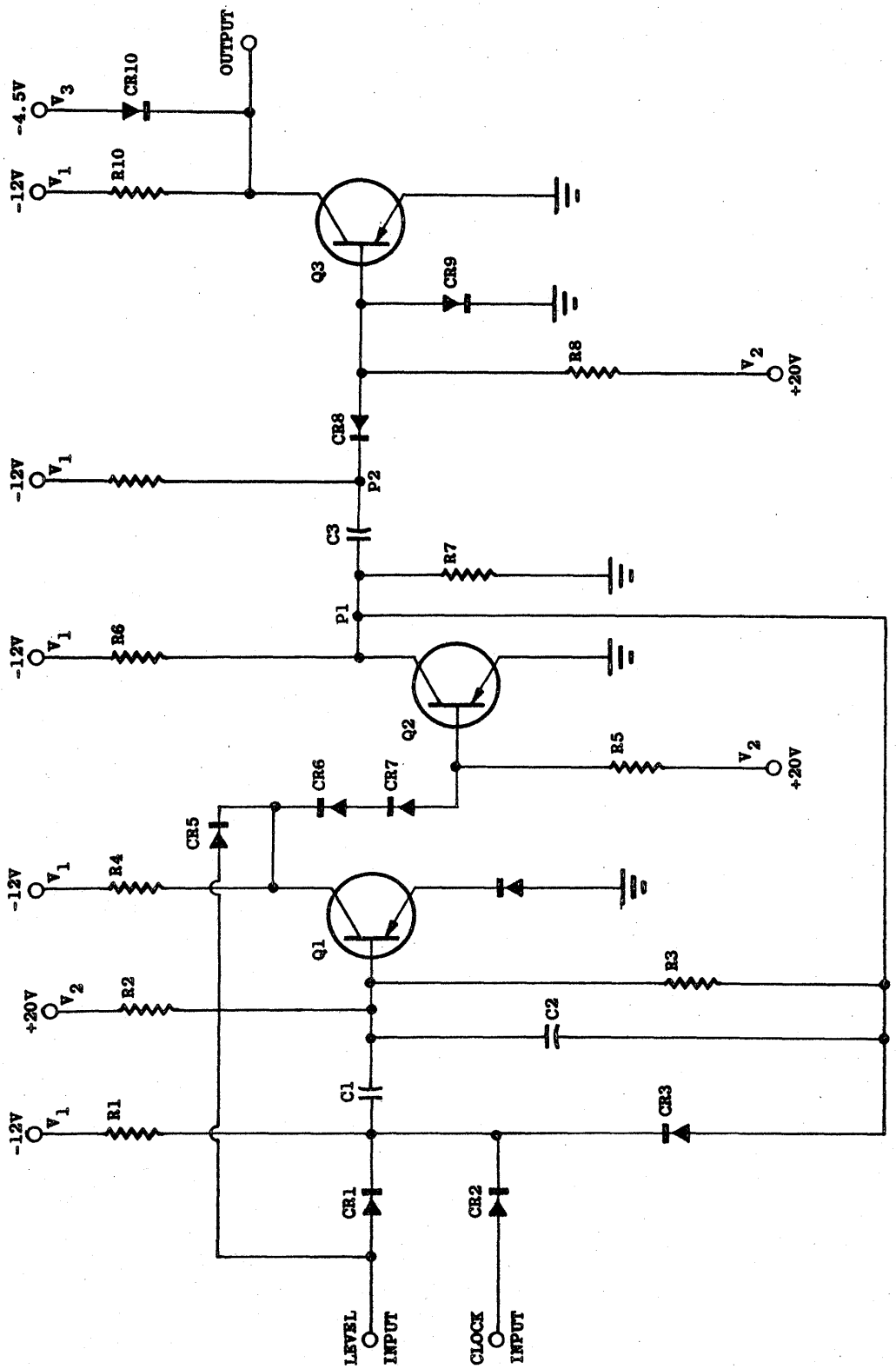



FIGURE 6.31-1. PULSE SYNCHRONIZER CIRCUIT SCHEMATIC

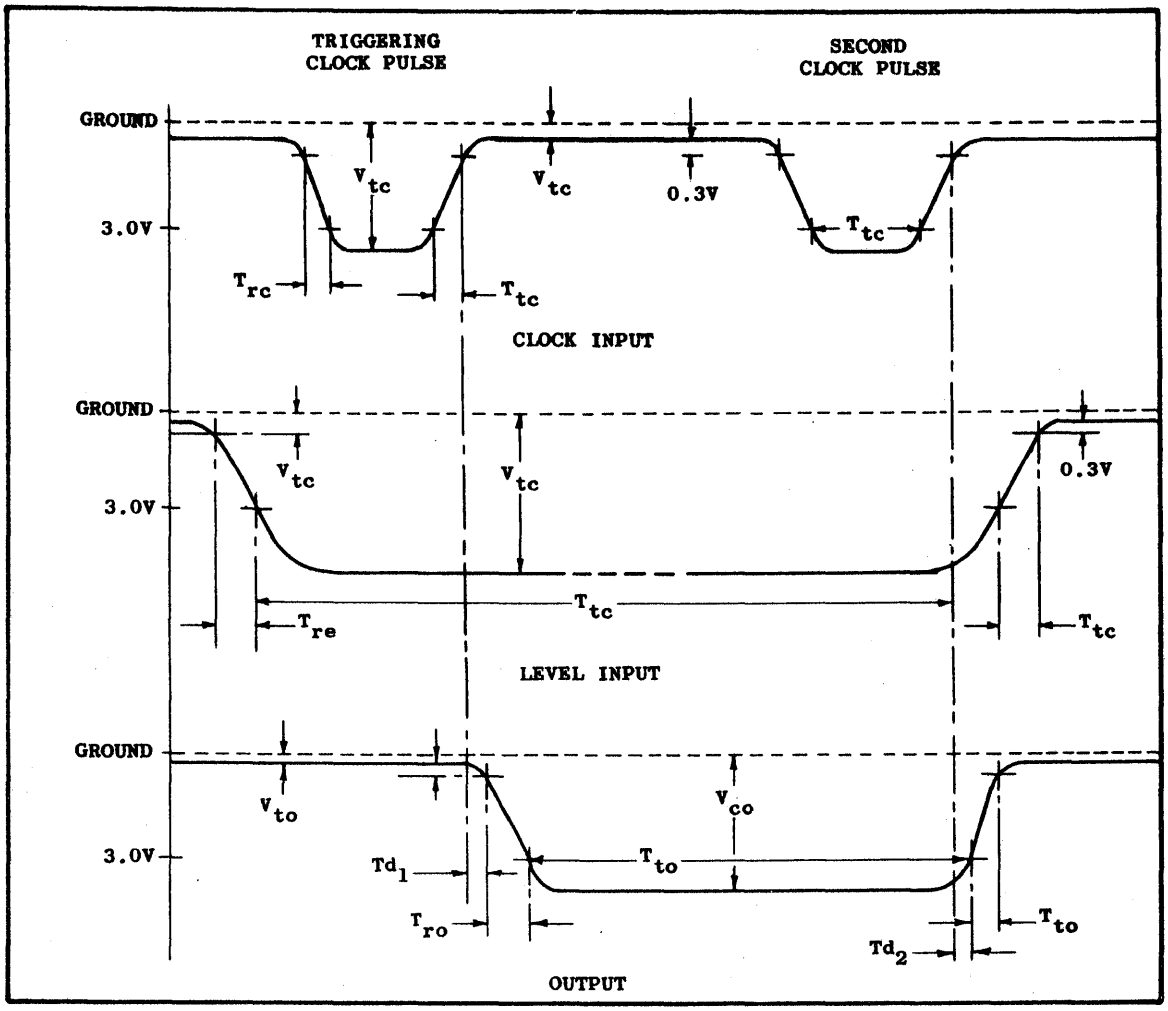



FIGURE 6.31-2. PULSE SYNCHRONIZER TIMING

PACKAGE SCHEMATIC

Refer to Figure 6.31-3 for the complete schematic fo the Synchronizer Parallel Plate Package.

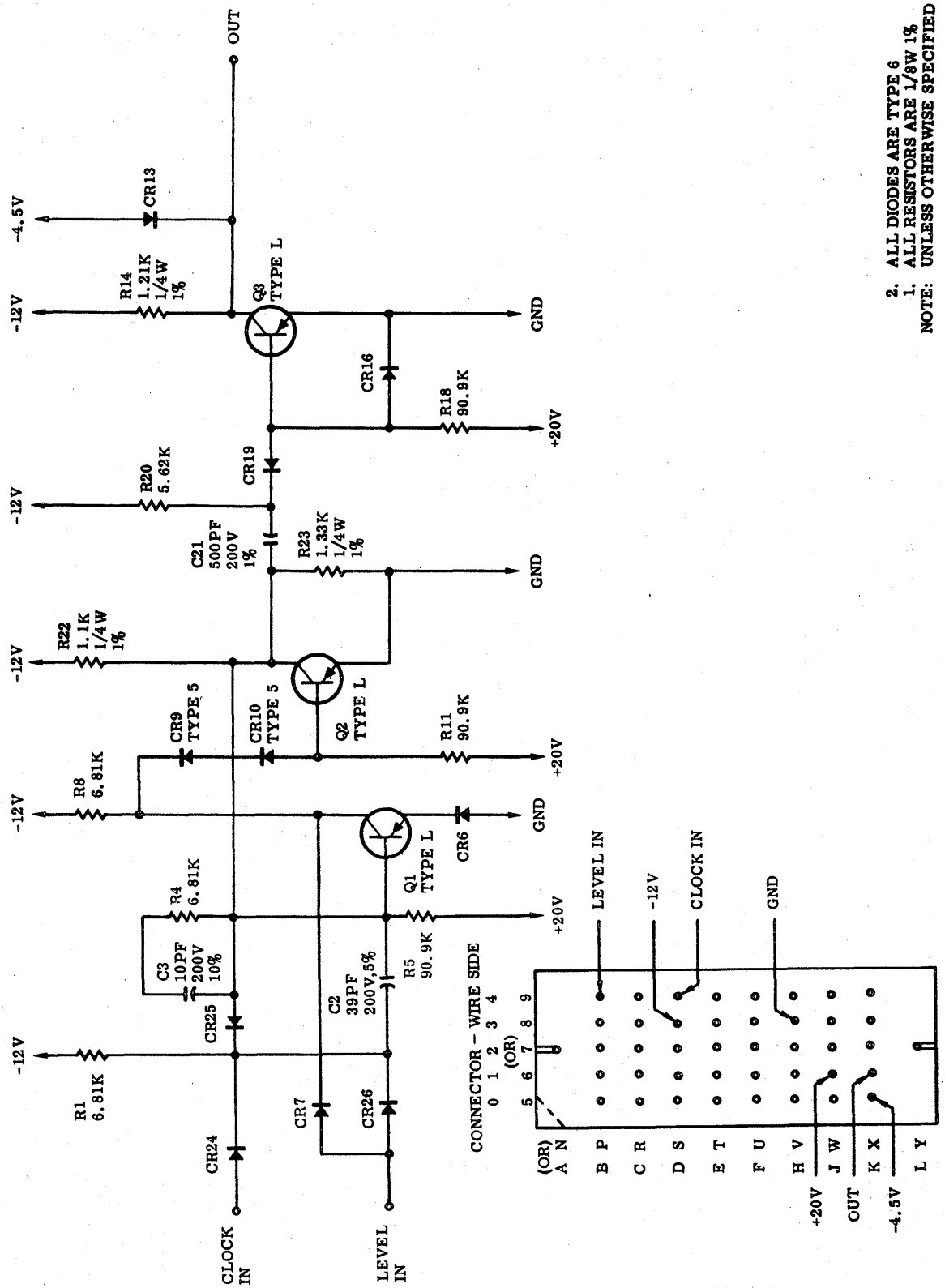



FIGURE 6.31-3. PULSE SYNCHRONIZER PACKAGE SCHEMATIC

## 6.32 CLOCK OSCILLATOR & SQUARING AMPLIFIER

### GENERAL DESCRIPTION

The Clock Oscillator and Squaring Amplifier consists of two circuits; one which generates the 1 megacycle Master Clock sine wave signal, and one which shapes the sine waves into square wave output pulses.

The oscillator circuit is a crystal controlled oscillator with a basic frequency of 1 megacycle. The circuit is so packaged that the crystal may be shorted out of the circuit thus converting the circuit to a Variable Frequency Oscillator for maintenance purposes.

The Squaring Amplifier circuit uses the positive peak to negative peak slope of the oscillator sine wave to produce a negative output pulse having a frequency of 1 megacycle with a width of 0.43 to 0.48 μs.

### CIRCUIT DESCRIPTION

Refer to Figure 6.32-1 for circuit schematic and to Figure 6.32-2 for Timing.

Transistor Q3 and Q4, crystal X37 and the tank circuit L36 and C4 make up the basic oscillator circuit. Q3 and Q4 are both biased into conduction. When power is applied to the circuit, the crystal X37 will be shocked into oscillation. The AC voltage developed across the crystal is coupled through C2 and R35 to the emitter of Q3. This voltage on the emitter results in a pulsating Q4 emitter current which develops an AC voltage across R23, which supplies positive feedback to the crystal to maintain oscillation.

Capacitor C20 and diodes CR18 and CR19 make up a gain limiter, limiting the voltage applied to the base of Q4, plus providing a more symetrical sine wave at the base of Q4.

Capacitor C2 provides DC isolation to the crystal X37.

R35 provides a means of adjusting the gain of the circuit.

Transistor Q5 and its associated circuit comprise the Squaring Amplifier circuit. Q5 is normally ON. The change from a positive to a negative peak of the sine wave applied to the base of Q4, causes Q4 to conduct more. Part of this greater collector current flows through C14, R13 and CR15, resulting in a positive potential on the base of Q5 cutting it OFF. Q5 remains cut OFF until the signal on the base of Q4 has nearly reached its peak in the negative direction, resulting in a negative pulse to be developed at the collector of Q5. This method of deriving a square wave pulse from a sine wave results in a constant width pulse of 0.43 to 0.48 μs, regardless of the amplitude of the sine wave.

The negative potential at the collector of Q5 when it is cut OFF, is applied to the bases of the two emitter followers Q2 and Q1. The emitters follow the bases providing a negative pulse of -4.5V at outputs 1 and 2.

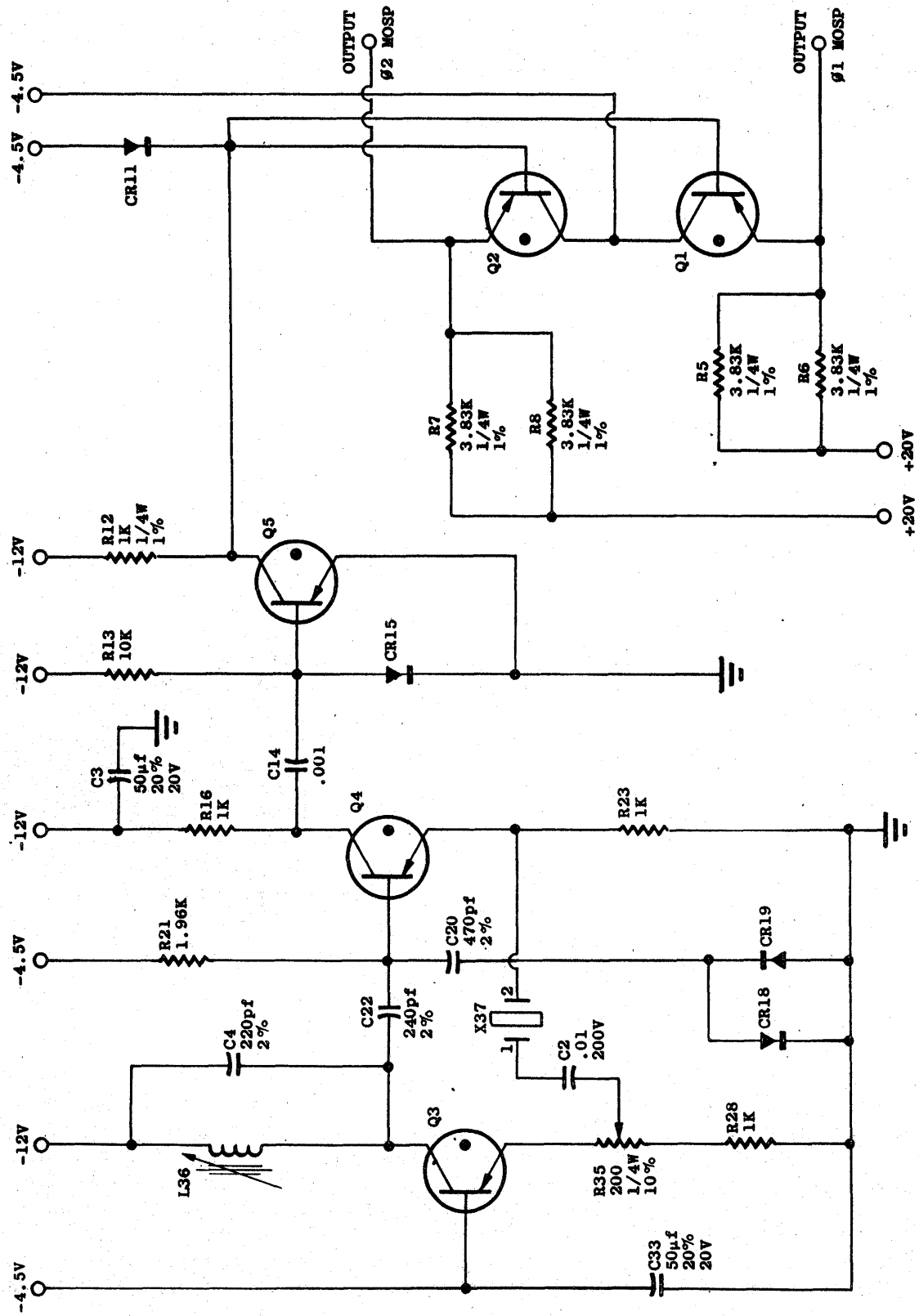



FIGURE 6.32-1. CLOCK OSCILLATORY SQUARING AMPLIFIER CIRCUIT SCHEMATIC

Output 1 is used to trigger the BO and Line Drivers and output 2 is used in the Clock Control circuitry of Central Control.

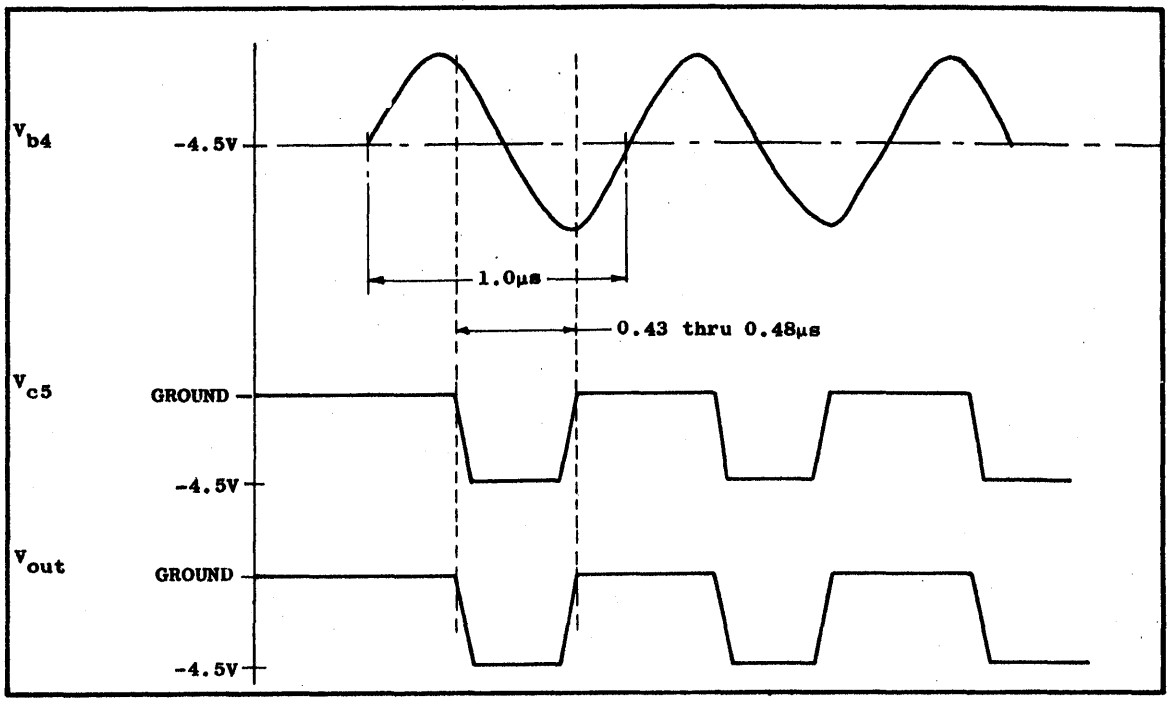



FIGURE 6.32-2. CLOCK OSCILLATOR AND SQUARING AMPLIFIER TIMING

VARIABLE FREQUENCY OSCILLATOR OPERATION

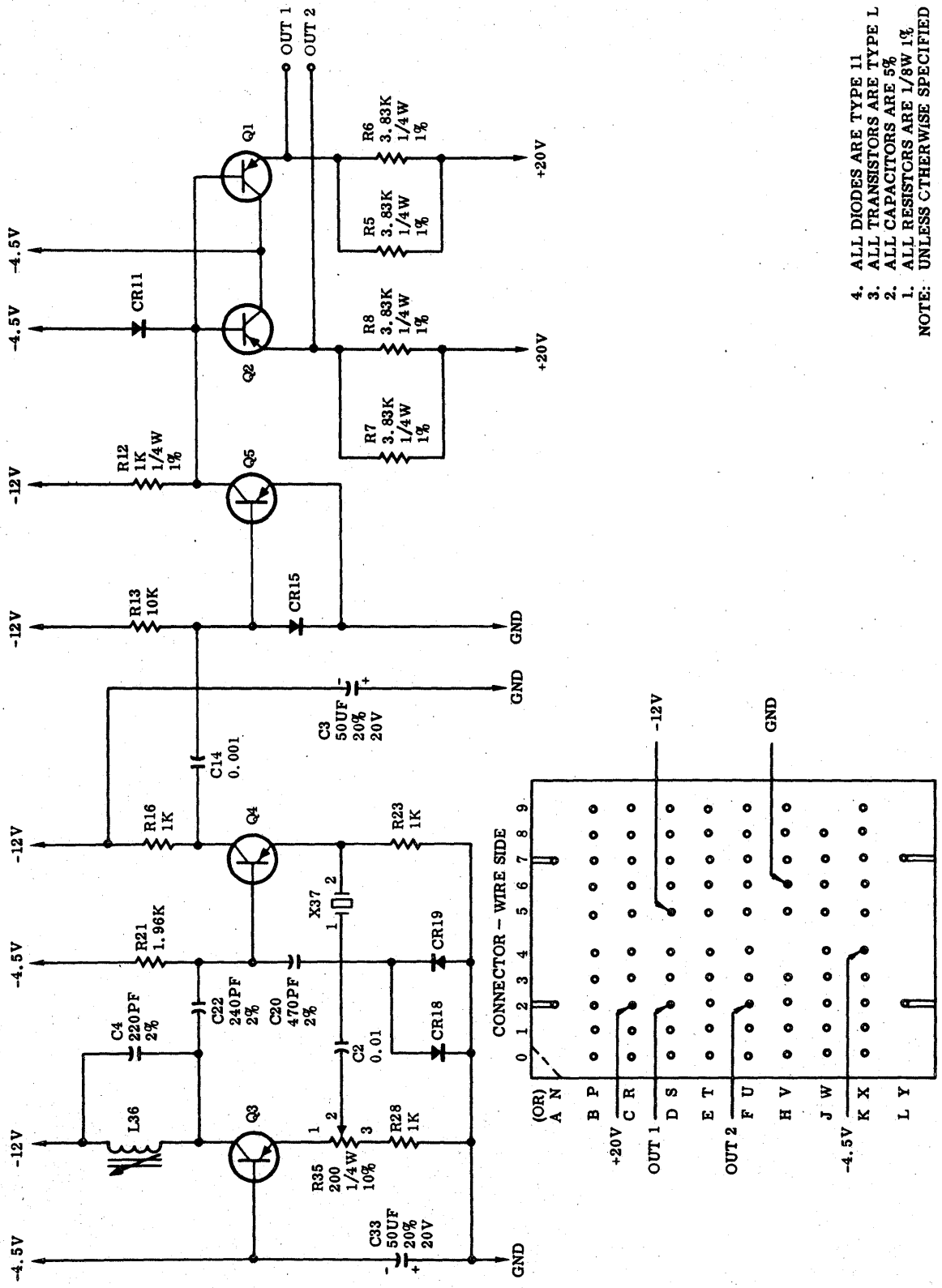
The oscillator circuit may be converted to a variable frequency oscillator for maintenance purposes by shorting out crystal X37. Without the crystal in the circuit, the oscillator is dependent upon the tuned tank circuit, L36 and C4, to determine the frequency of oscillation. Therefore, by varying the inductance L36, the circuit will oscillate over a frequency range of 400 kc from 800 kc to 1.2 megacycles.

Potentiometer R35 provides a means of adjusting the gain of the circuit. When using the circuit as a variable frequency oscillator, it may be necessary to increase the gain to obtain stable operation when tuned near the limits of the frequency range.

When returning the circuit to normal by removing the short from across X37, it is necessary to tune the tank circuit to 1 megacycle prior to removing the short.

PACKAGE SCHEMATIC

Refer to Figure 6.32-3 for the complete schematic of the Clock Oscillator and Squaring Amplifier Parallel Plate Package.




NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/8W 1%
2. ALL CAPACITORS ARE 5%
3. ALL TRANSISTORS ARE TYPE L
4. ALL DIODES ARE TYPE 11

FIGURE 6.32-3. CLOCK OSCILLATOR AND SQUARING AMPLIFIER PACKAGE SCHEMATIC

## 6.33 BLOCKING OSCILLATOR AND LINE DRIVER

### GENERAL DESCRIPTION

The Blocking Oscillator and Line Driver is a circuit used in conjunction with the Clock Oscillator and Squaring Amplifier to produce a 1 megacycle clock pulse having a width of 0.155 μs. The Line Drivers drive the clock lines going to all units requiring these pulses.

### CIRCUIT DESCRIPTION

Refer to Figures 6.33-1 and 6.33-2.

In the quiescent state, Q7, Q4 and Q1 are cut OFF. Q6, Q2, Q3, Q5 and Q8 are conducting.

The input to Q7 consists of a level (Inhibit IN) and a negative pulse from the Clock Oscillator and Squaring Amplifier (IN). The inhibit level is false until such time that the start, load or single pulse switch is depressed. When any of these three switches are depressed, a true level is applied at the Inhibit IN terminal. This level along with a negative clock pulse at the IN terminal will bias Q7 into conduction.

R23 limits the emitter current of Q7 when the input is true. The collector of Q7 in the quiescent state has a +10.0V bias applied to it due to the voltage divider R20 and R21 between ground and +20V. When A7 begins to conduct, the collector will start to go negative towards its saturation voltage, causing current to flow through C28, thus supplying base drive to Q4 to turn it ON. The turning ON of Q4 provides a current path for Q1 emitter current, resulting in turning ON Q1.

The base of Q1 is held at a constant -6.0V due to the voltage divider R1 and R34 between ground and -12V. This constant voltage on the base of Q1 results in a constant Q1 emitter current as long as Q4 and Q1 are held ON. When Q1 turns ON, a 6.0V potential is placed across the primary of the constant voltage switching transformer (T28).

Q1 collector current will begin to flow and to increase linearly through T38 inducing a voltage in the secondary and feedback windings of T38. The voltage induced in the secondary cuts OFF Q6. The voltage induced in the feedback winding continues to supply base drive to Q4 to hold it ON. When the collector current has increased to such a value that it equals the constant emitter current, the field across the primary of T38 collapses, removing base drive to Q4, cutting it OFF along with Q1, and turning Q6 ON again.

The circuit and T38 are so designed as to allow a pulse of 0.155 μs duration to be produced during the time Q4 and Q1 are ON. R37 provides a means of accurately adjusting the width of the pulse. CR2 and R3 provide a damping network across the primary of T38.

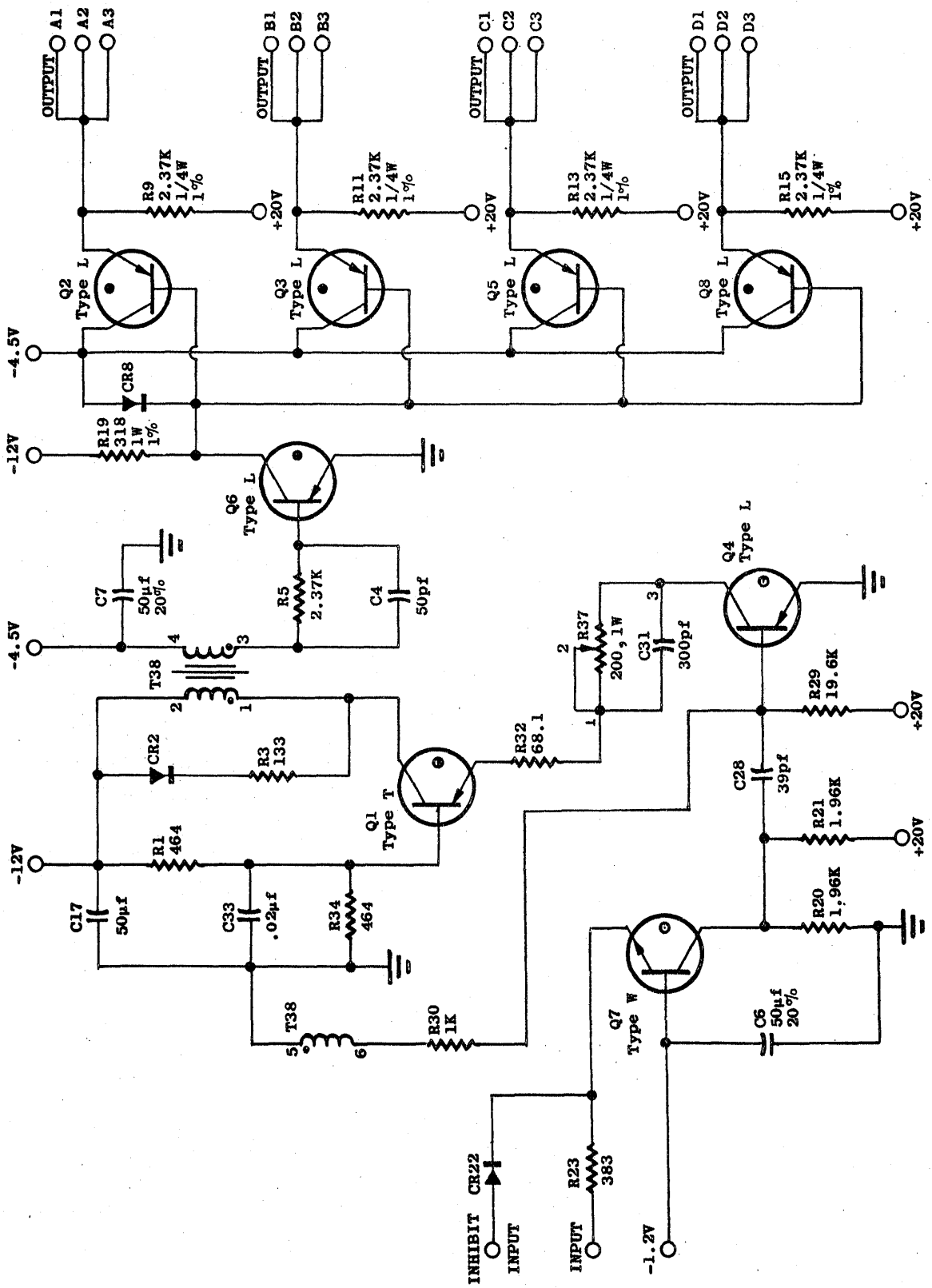



FIGURE 6.33-1. BLOCKING OSCILLATOR AND LINE DRIVER CIRCUIT

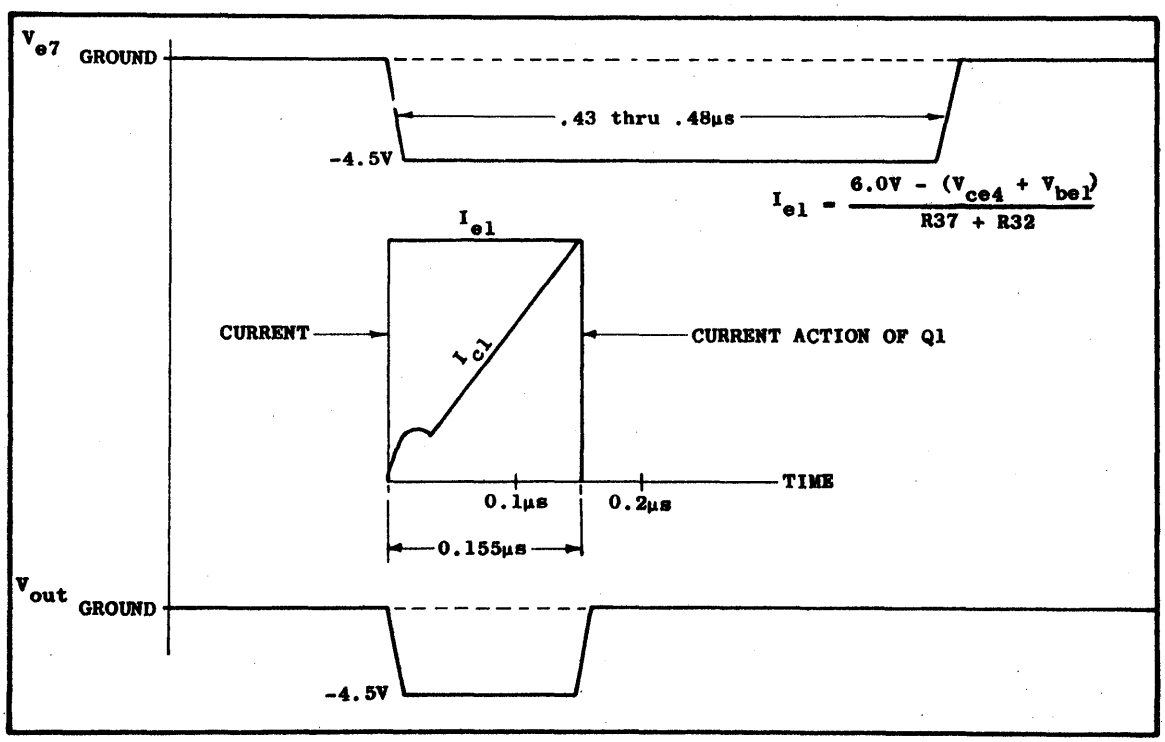



FIGURE 6.33-2. BLOCKING OSCILLATOR AND LINE DRIVER TIMING

When Q6 is cut OFF by the induced voltage in the secondary of T38, its collector starts toward its cut OFF potential of -12V. CR8, however, prevents it from reaching -12V by clamping it to -4.5V. The -4.5V potential is applied to the bases of the emitter followers Q2, Q3, Q5 and Q8. The emitters follow this potential resulting in a -4.5V pulse of 0.155 μs width to be sent out via cables to all units requiring the clock pulses from the output terminals A1 through D3.

PACKAGE SCHEMATIC

Refer to Figure 6.33-3 for the complete schematic of the Blocking Oscillator and Line Driver Parallel Plate Package.

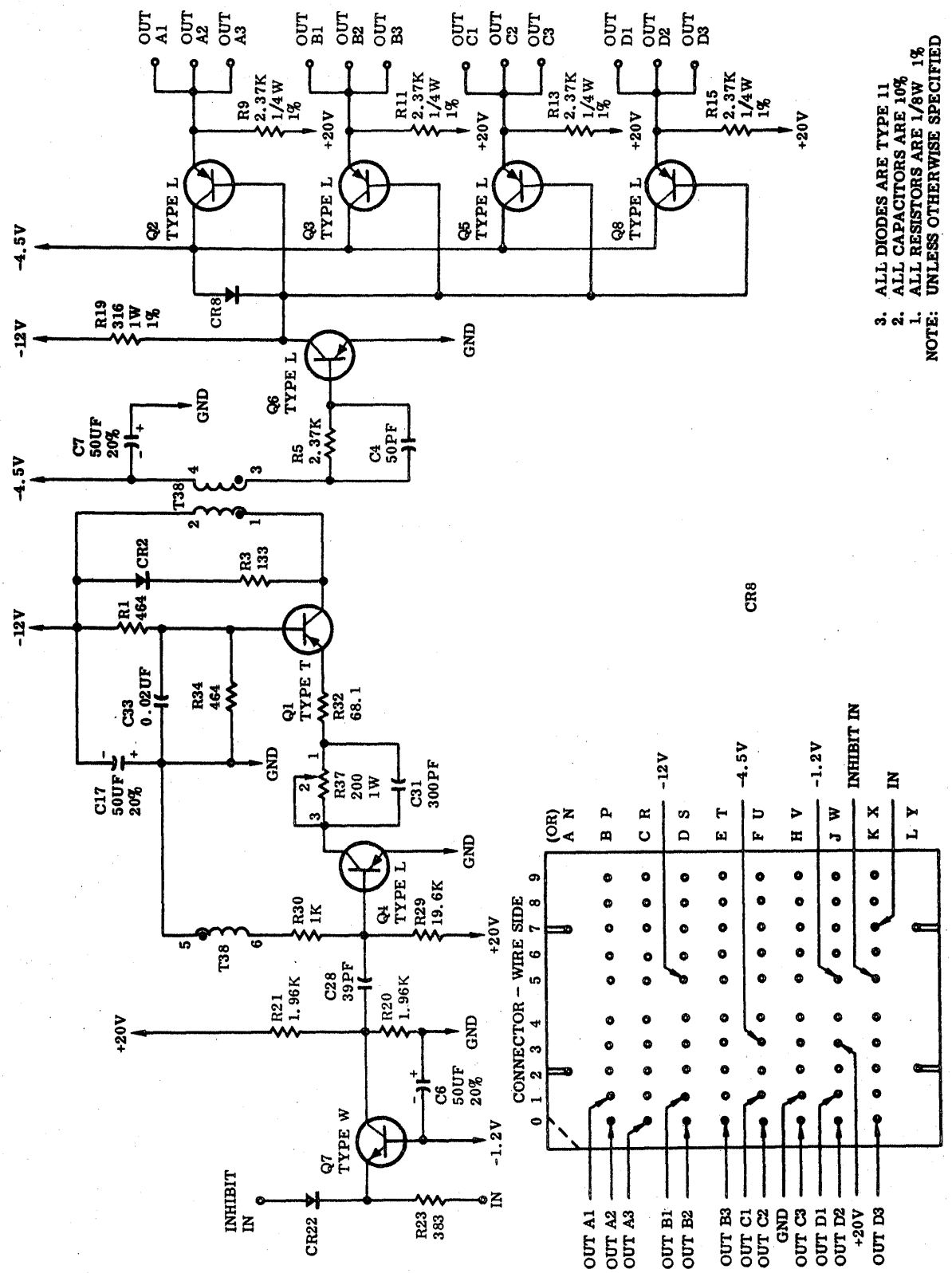



FIGURE 6.33-3. BLOCKING OSCILLATOR AND LINE DRIVER PACKAGE SCHEMATIC

## 6.34 DIRECT-COUPLED LOCAL CLOCK DRIVER AND VARIABLE BIAS

### GENERAL DESCRIPTION

The Direct-Coupled Local Clock Driver is a circuit centrally located in each panel of each gate of every unit requiring clock pulses. Its function is to distribute the clock pulses sent via cables from the BO and Line Driver package in Central Control to the individual circuits on a panel. It also isolates the loads of these circuits from the clock cables.

### CIRCUIT DESCRIPTION

Refer to Figure 6.34-1.

In the quiescent state, Q1 and Q2 are cut OFF. Q3, Q4 and Q5 are conducting.

When a negative clock pulse is applied to the input between T/P Input and T/P Ground Input, Q1 will be turned ON. R8 provides termination for this pulse.

The turn ON of Q1 results in its collector going negative towards its saturation potential, supplying base drive to Q2 turning it ON.

When Q2 turns ON, its collector starts toward its saturation potential, removing the base drive from Q3, Q4 and Q5, cutting them OFF. This action results in a -4.5V clock pulse at outputs 1 through 6 being made available to be used by the circuits within the unit.

Diodes CR35, CR30, CR39 and CR27, clamp the outputs at -4.5V.

### VARIABLE BIAS

In the flip-flop circuit, the clocked inputs see the gated circuits as a load if the diodes between the clock line and the gated levels are not back biased. This would normally be the case since the gated inputs will tend to be at a lower level than the clock lines due to the drop through the cascading of gating diodes. The leakage would load the clock driver to a greater extent than necessary. Therefore, the false level from the Local Clock Driver is adjusted sufficiently negative by the variable bias input, to back bias the flip-flop gating diodes, reducing the current and loading caused by it.

This variable bias is in the range of -0.5V to -0.8V and is applied to the two paralleled bias terminals from a variable bias package. There is a variable bias package associated with each Local Clock  package.

### PACKAGE SCHEMATIC

Refer to Figure 6.34-2 for the complet ect-Coupled Local Driver Parallel Plate Package.

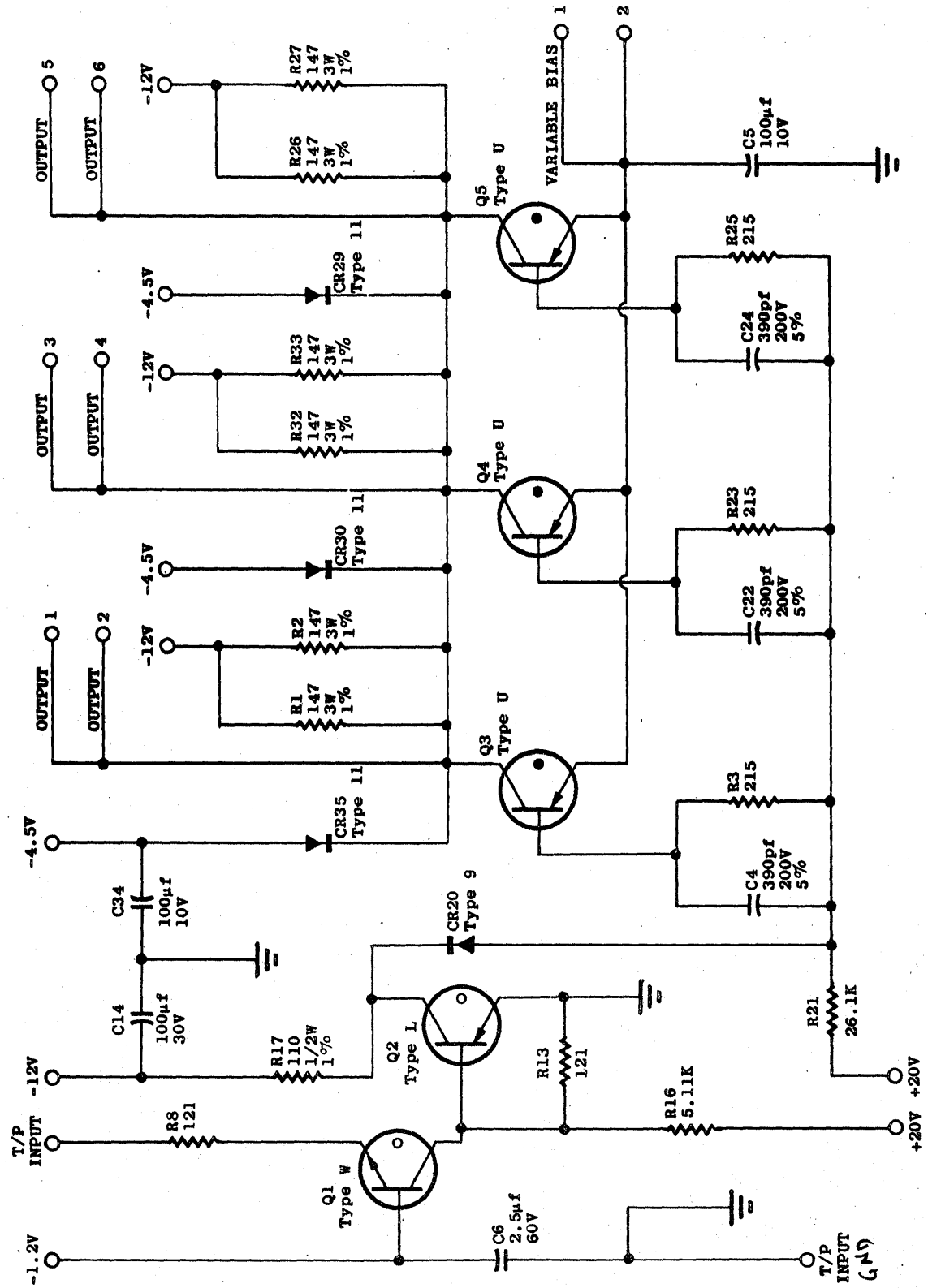



FIGURE 6.34-1. DIRECT COUPLED LOCAL CLOCK DRIVER

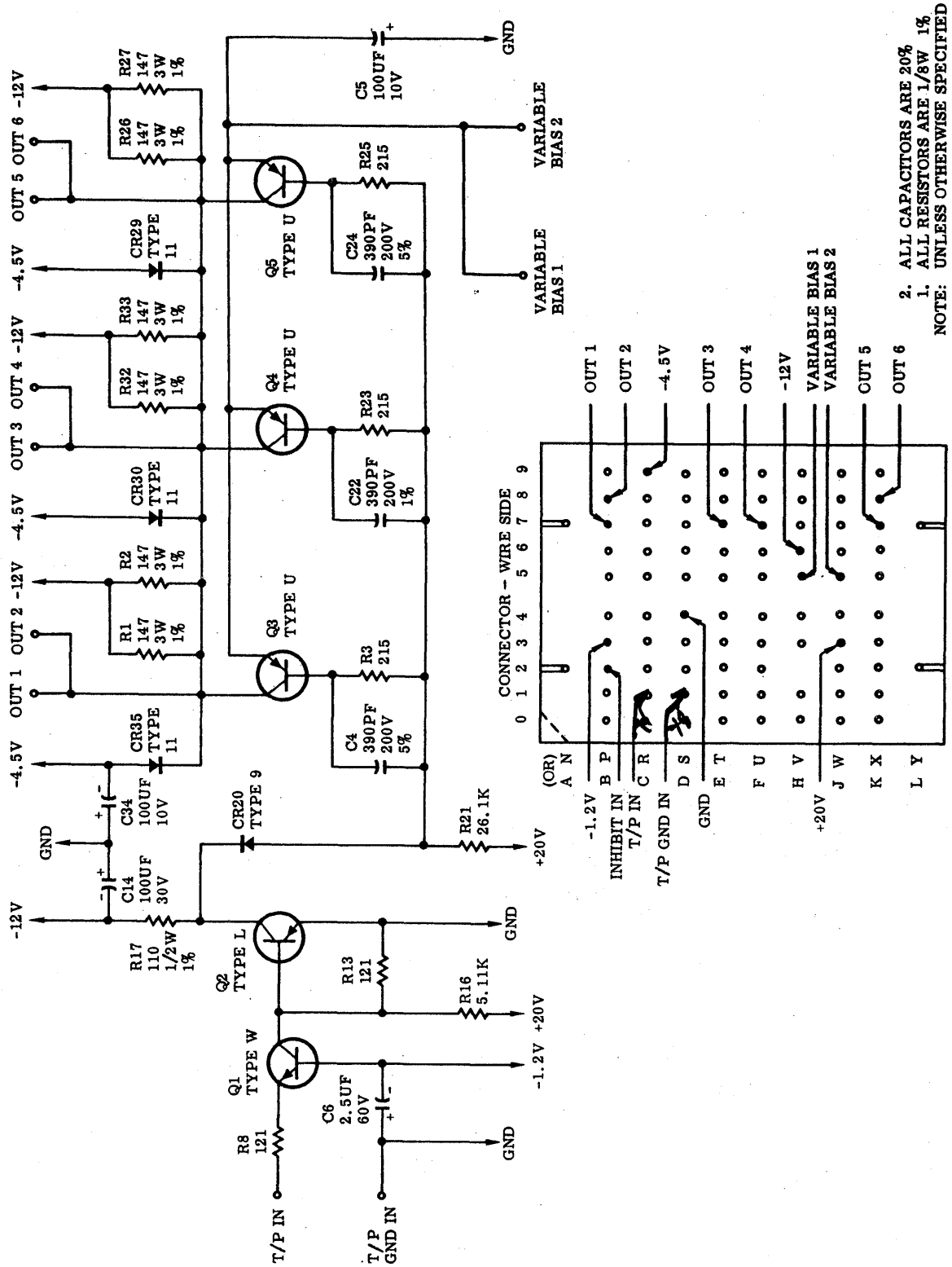



FIGURE 6.34-2. DIRECT COUPLED CLOCK DRIVER PACKAGE SCHEMATIC

## 6.35 DOUBLE DRIVER 90

### GENERAL DESCRIPTION

The Double Driver 90 is a package specifically designed to reduce the number of driver packages required by the system as well as to reduce the number of back-plane wires.

The package consists of two identical Double Driver 90 circuits. Each has one input and two outputs. The circuit is a non-inverting switch amplifier to be used to drive cables and load requiring currents up to 90 ma.

### CIRCUIT DESCRIPTION

Refer to Figures 6.35-1 and 6.35-2.

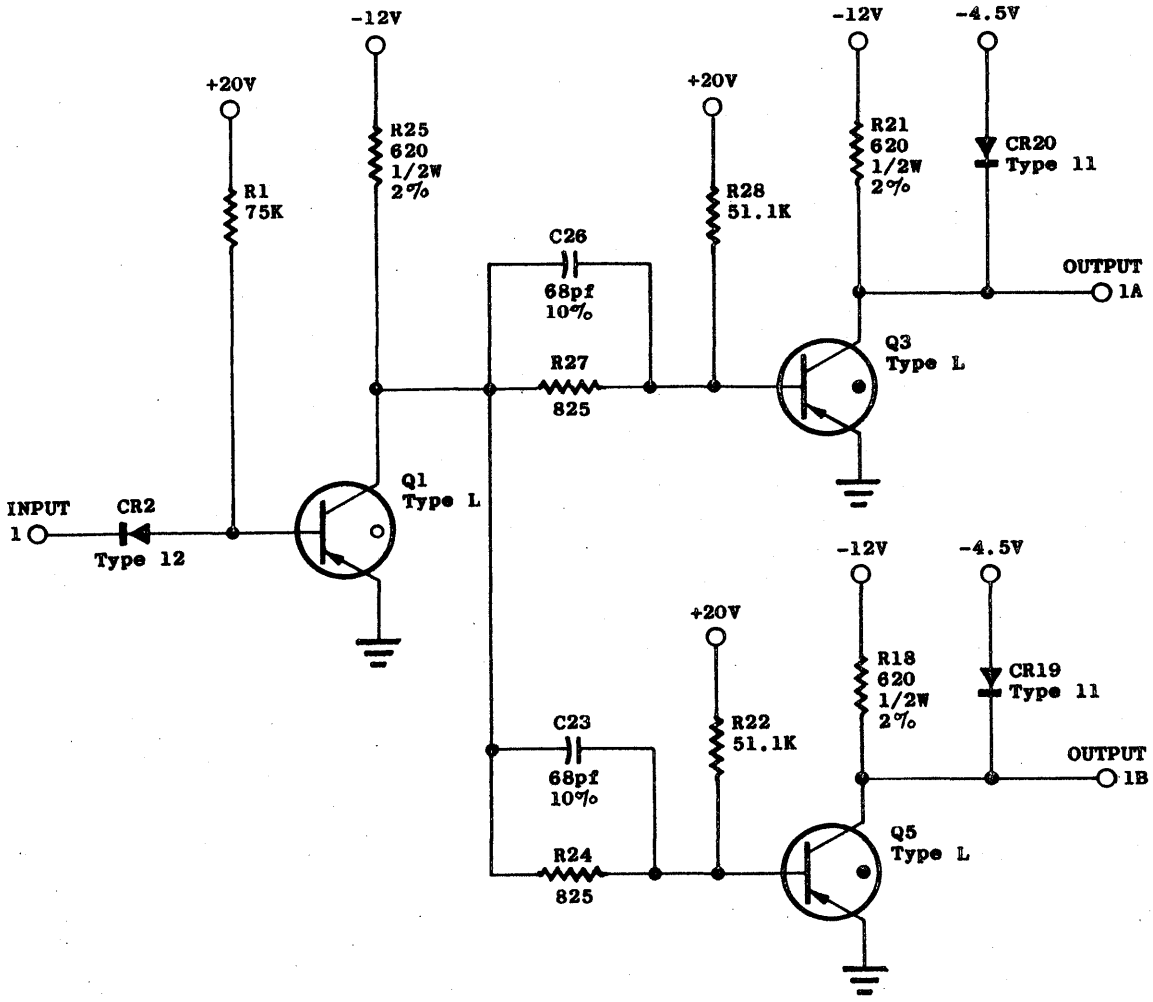



FIGURE 6.35-1. DOUBLE DRIVER 90 CIRCUIT SCHEMATIC

In the quiescent state, Q1 is cut OFF and Q3 and Q5 are in saturation.

When a negative input greater than -1.2V is applied at the input, base drive is supplied to Q1, turning it ON. When Q1 goes ON, its collector goes toward its saturation voltage, removing base drive to Q3 and Q5 cutting them OFF. The cut OFF of Q3 and Q5 results in their collectors rising toward -12V. However, the clamping diodes CR20 and CR19, clamp the rise to -4.5V resulting in an output of -4.5V at 1A and 1B.

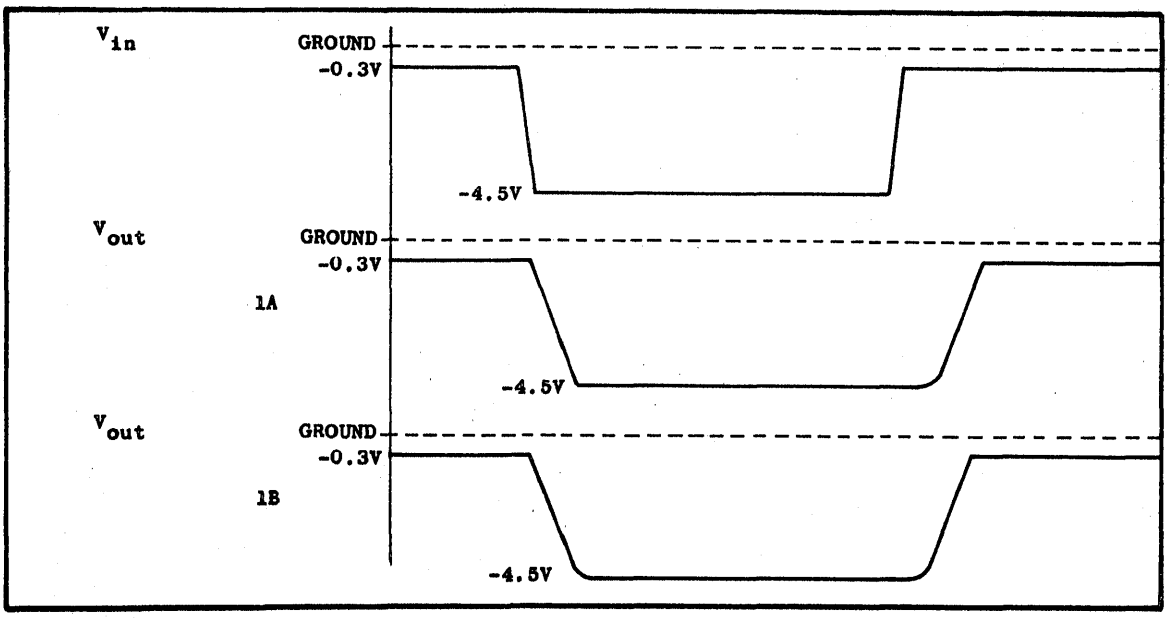



FIGURE 6.35-2. DOUBLE DRIVER 90 TIMING

SWITCHING

When the input goes from a true level to a false, the reverse action takes place.

Q1 will be turned OFF, Q3 and Q5 will be turned ON, resulting in a false level of -0.3V at output 1A and 1B.

Capacitors C26 and C23 speed up the switching time of Q3 and Q5.

Resistors R27 and R24 limit the base to emitter current of Q3 and Q5 when Q1 is cut OFF.

PACKAGE SCHEMATIC

Refer to Figure 6.35-3 for the complete schematic of the Double Driver 90 parallel Plate Package.

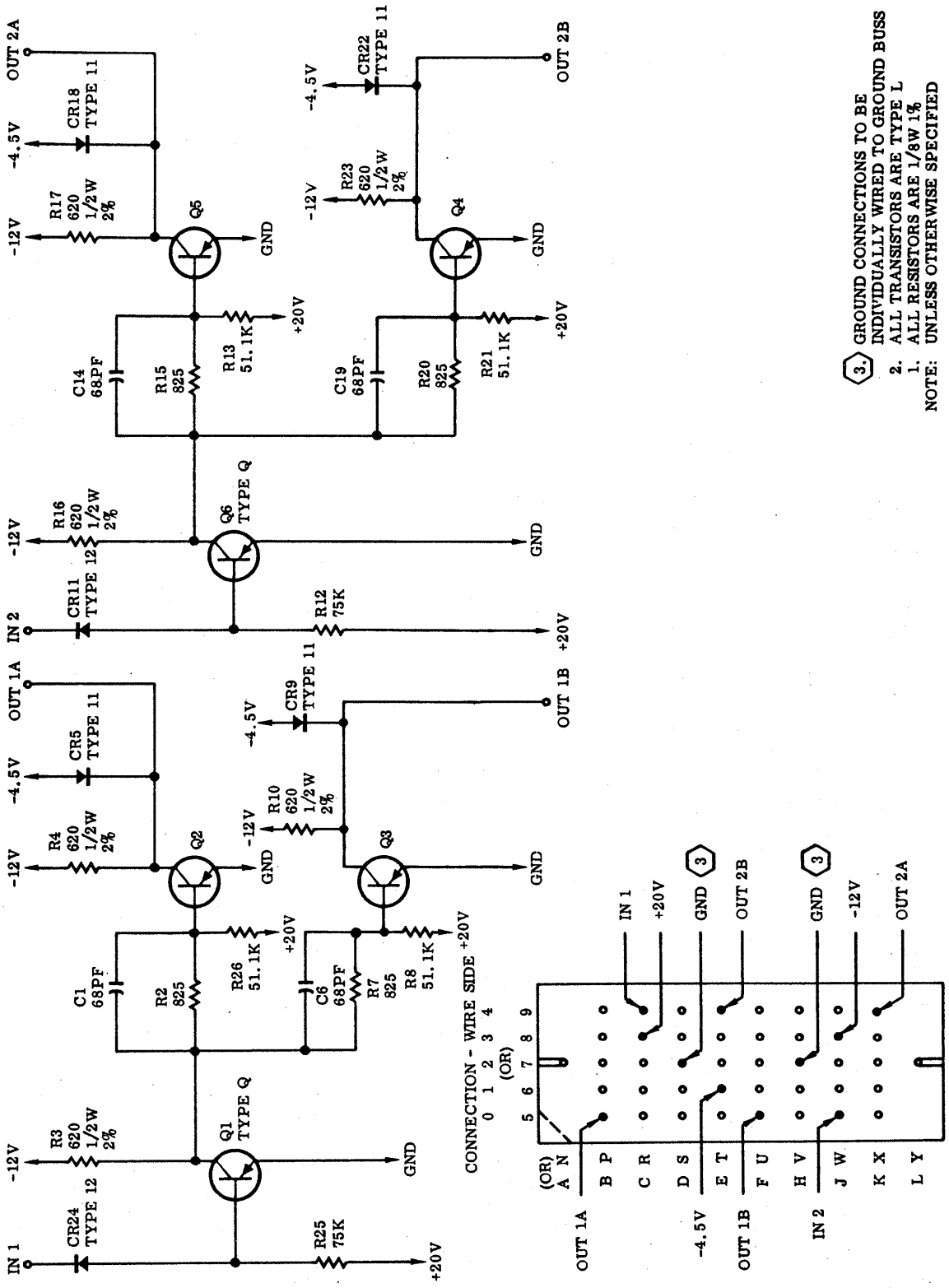



FIGURE 6.35-3. DOUBLE DRIVER 90 PACKAGE SCHEMATIC

## 6.36 INVERTER DRIVER 90

### GENERAL DESCRIPTION

The Inverter Driver 90 is a circuit which provides two driver outputs. One non-inverted and one inverted, for one input.

The package contains two identical circuits, each having one input and two outputs. The circuits are used to drive loads and cables requiring currents up to 90 ma.

### CIRCUIT DESCRIPTION

Refer to Figures 6.36-1 and 6.36-2.

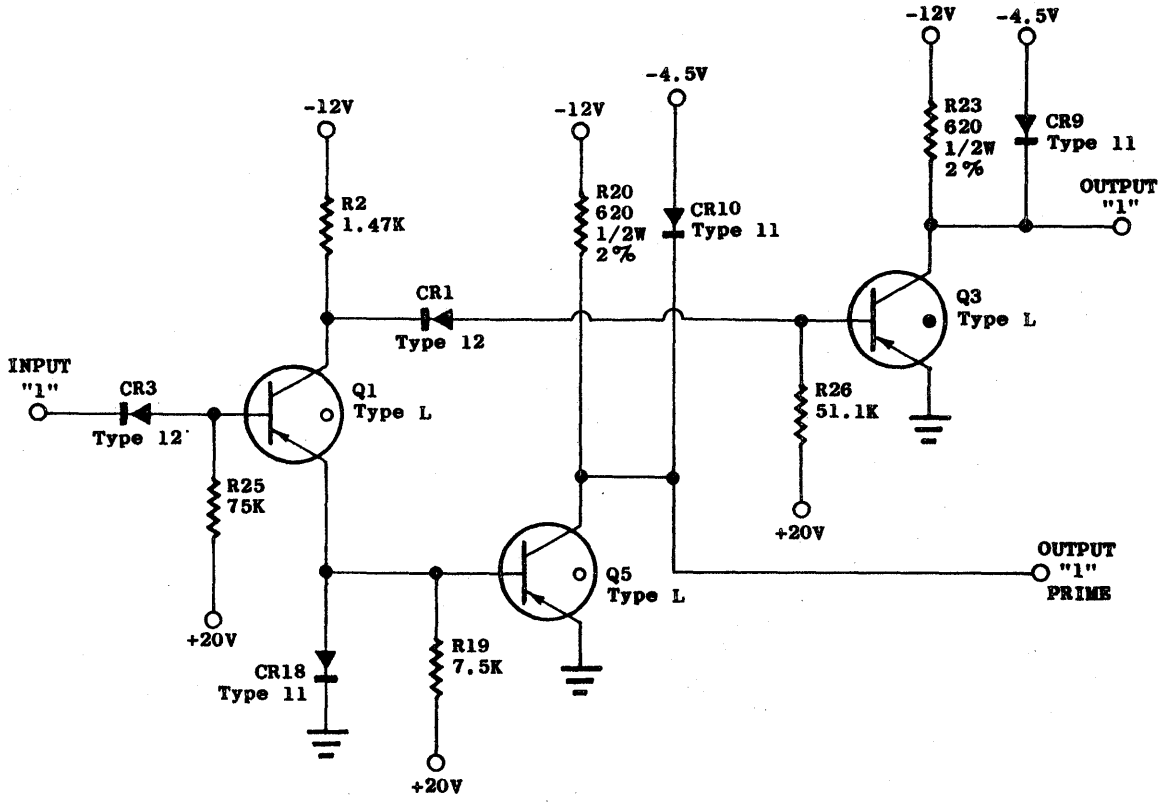



FIGURE 6.36-1. INVERTER DRIVER 90 CIRCUIT SCHEMATIC

In the quiescent state, Q1 and Q5 are cut OFF, and Q3 is in saturation.

When a true level is applied to the input, base drive will be supplied to Q1 turning it ON. When Q1 turns ON, its emitter follows the base supplying base to Q5, turning it ON.

The turn ON of Q5 results in its collector going toward its saturation potential, supplying an inverted (false in this case) output at Output 1 Prime.

The turn ON of Q1 also results in its collector going toward its saturation potential, removing base drive from Q3 turning it OFF. When Q3 goes OFF, its collector rises toward -12.0V, the clamp diode CR9 clamps the rise to -4.5V resulting in an output of -4.5V at Output 1.

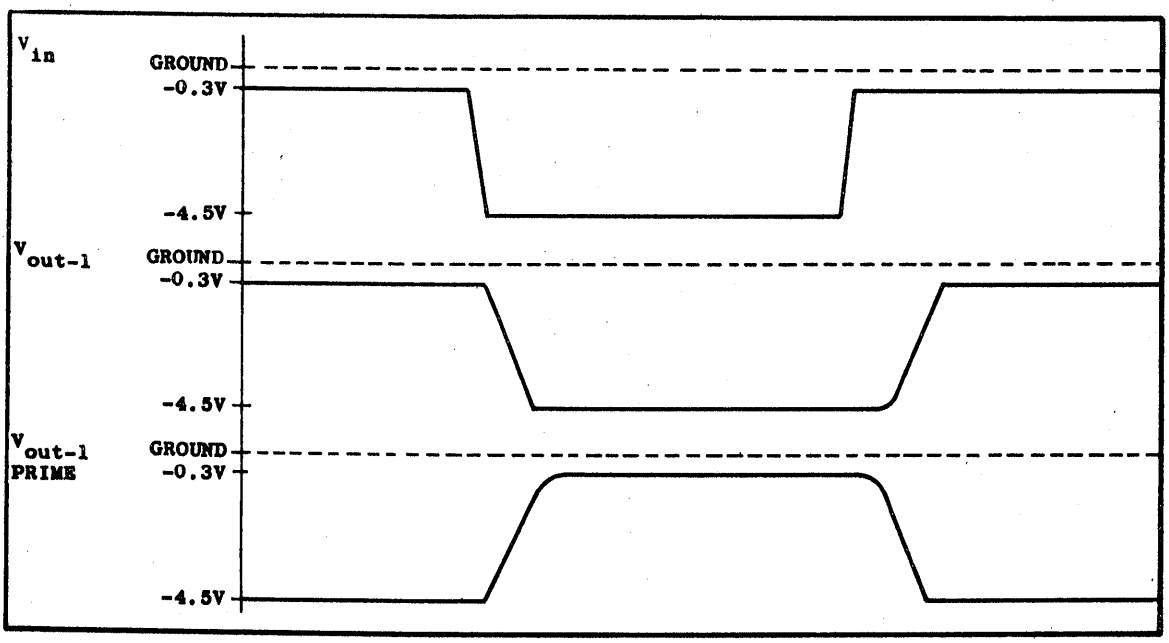



FIGURE 6.36-2. INVERTER DRIVER 90 TIMING

SWITCHING

When the input goes from a true level to a false, the reverse action takes place.

Q1 will be turned OFF, turning OFF Q5, which results in Ouput 1 Prime going true (-4.5V). The turn OFF of Q1 also results in Q3 turning ON, producing a false (-0.3V) output at Output 1.

PACKAGE SCHEMATIC

Refer to Figure 6.36-3 for the complete schematic of the Inverter Driver 90 Parallel Plate Package.

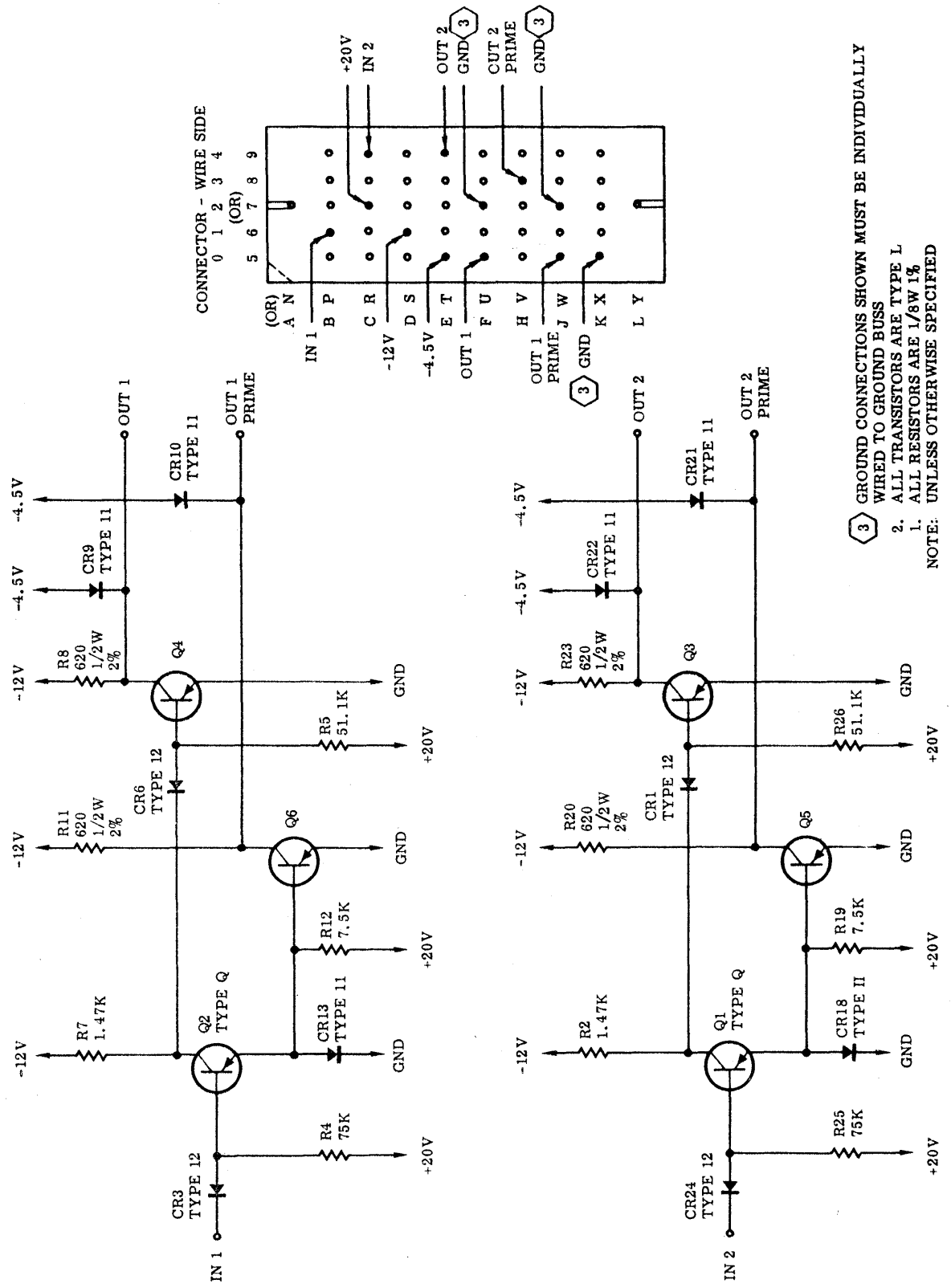



FIGURE 6.36-3. INVERTER DRIVER 90 PACKAGE SCHEMATIC

## 6.37 FLIP-FLOP AMPLIFIER

### GENERAL DESCRIPTION

The Flip-Flop Amplifier is a package containing three circuits. Two of these circuits are double switches, having two outputs for a single input, and the third is a single switch.

The circuits are used directly with the outputs of a flip-flop, providing drive to more loads, with no time delay than is possible with the conventional switch or driver circuit.

### CIRCUIT DESCRIPTION

Refer to Figures 6.37-1 and 6.37-2.

In the quiescent state, Q1 and Q3 are cut OFF.

When a negative level is applied to input 1, base drive is supplied to Q1 and Q3, turning both ON.

The collectors of Q1 and Q3 move toward their saturation potentials providing false (-0.3V) outputs at Output 1A and 1B.

Capacitors C27 and C24 speed up the switching time of Q1 and Q3.

Resistors R28 and R25 limit the base to emitter currents of Q1 and Q3 when the input is true.

The identical circuit consisting of Q4 and Q5 operates the same as the Q1 and Q3 circuit. However, normally, this circuit will have as its output the opposite state of the flip-flop. Therefore, if Input 1 is true, Input 2 will be false, and Output 2A and 2B will be true.

In the third circuit, Q2 is cut OFF in the quiescent state.

When a negative level is applied to Input 3, base drive is supplied to Q2, turning it ON. Its collector will then start toward its saturation potential, producing a false (-0.3V) output at Output 3.

### PACKAGE USAGE

When the Flip-Flop Amplifier is used with a flip-flop, its inputs tie directly to the output of the flip-flop, and is the only load tied to the flip-flop.

All loads requiring an input from the flip-flop are then tied to the outputs of the Flip-Flop Amplifier.

If a Flip-Flop Amplifier is used with the flip-flops "1" output, there will also be an amplifier on the "0" output. The maximum amplifiers used with one output of a flip-flop is 5. Inputs 1, 2 and 3 are connected in parallel to one of the outputs of the flip-flop.

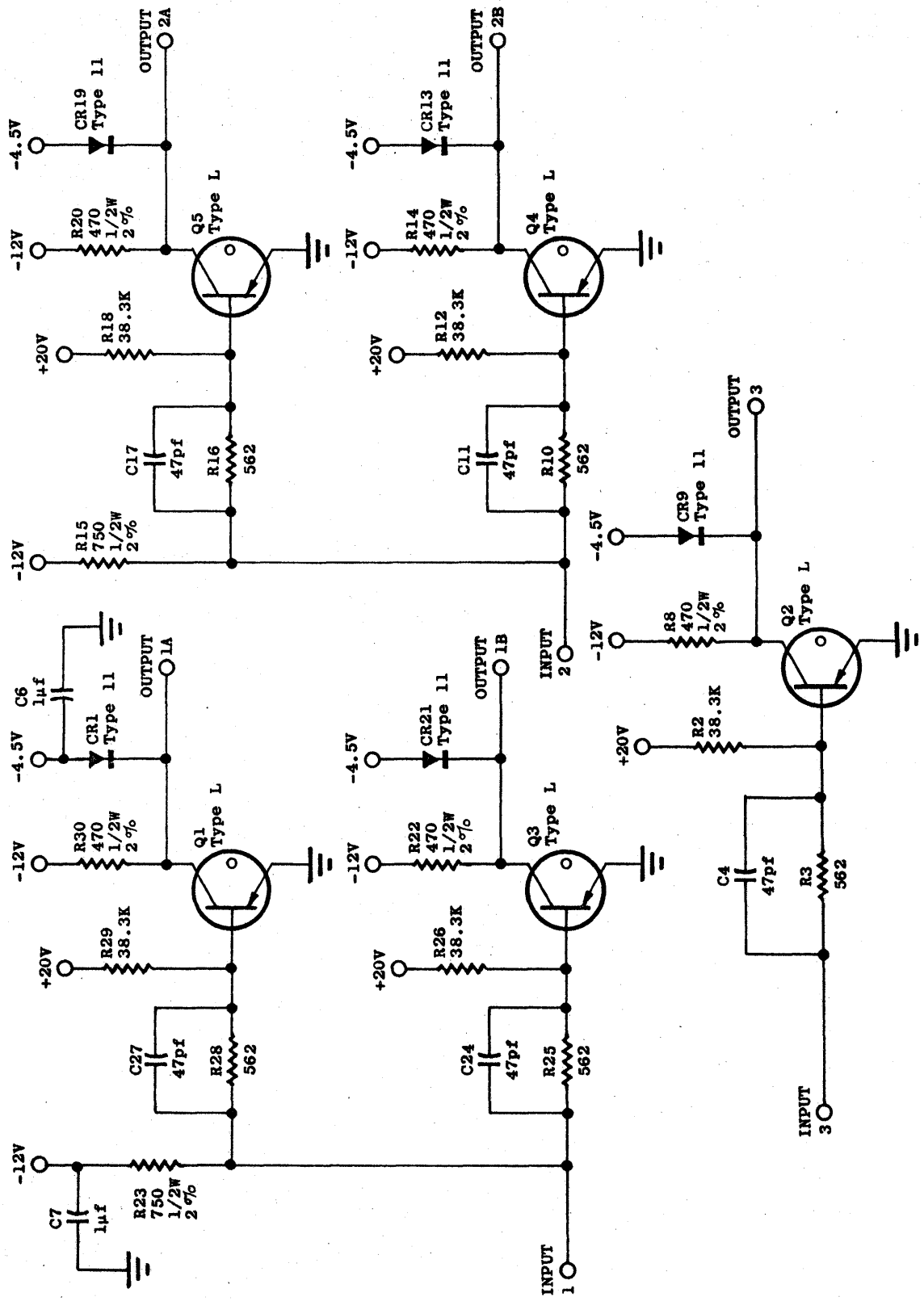



FIGURE 6.37-1. FLIP-FLOP AMPLIFIER CIRCUIT SCHEMATIC

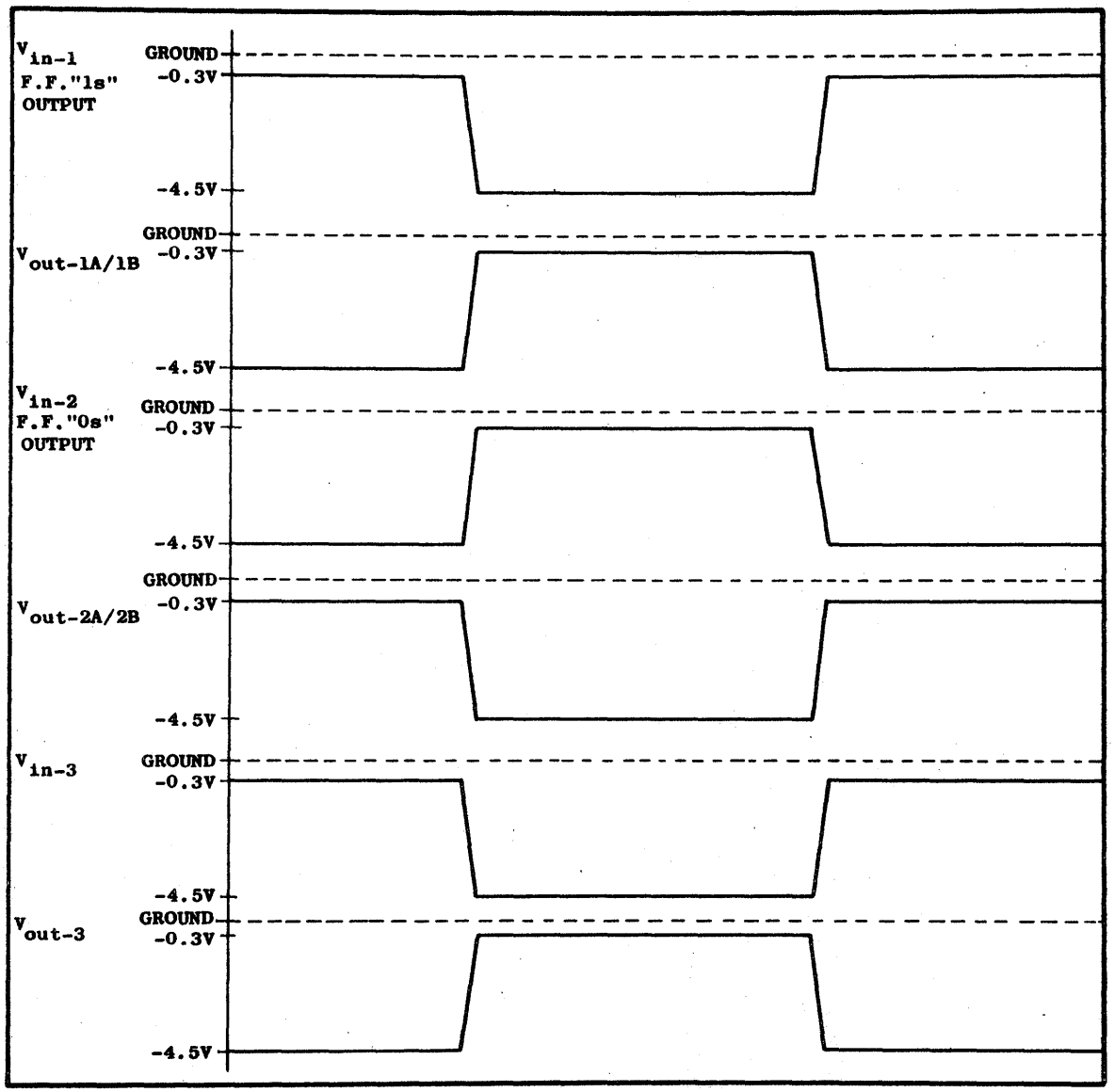



FIGURE 6.37-2. FLIP-FLOP AMPLIFIER WAVEFORMS

PACKAGE SCHEMATIC

Refer to Figure 6.37-3 for the complete schematic of the Flip-Flop Amplifier Parallel Plate Package.

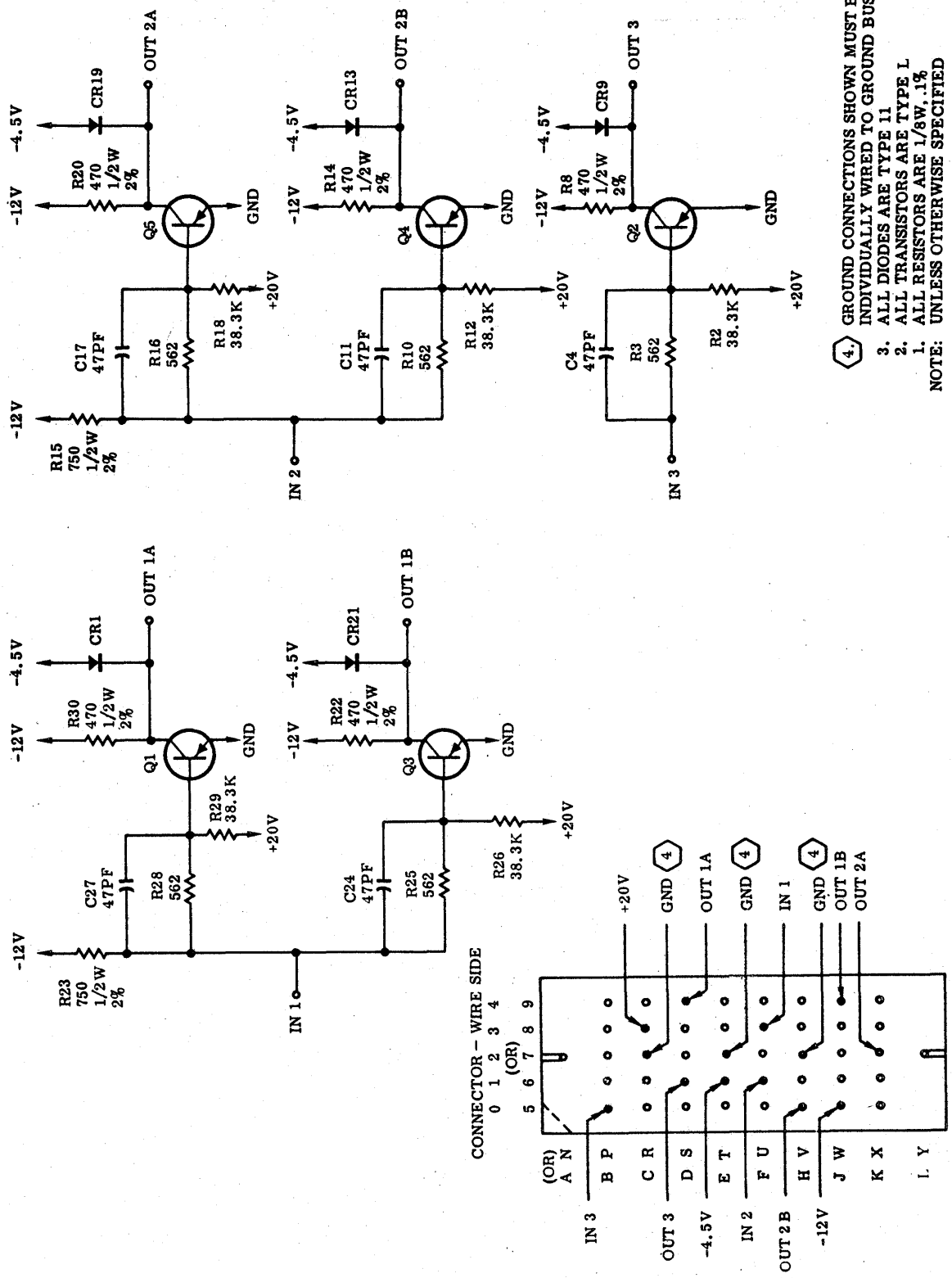



FIGURE 6.37-3. FLIP-FLOP AMPLIFIER PACKAGE SCHEMATIC