#1913 1747

Burroughs Corporation

SYSTEMS M&E GROUP
SANTA BARBARA PLANT

M-MEMORY PROCESSOR

PRODUCT SPECIFICATION

REVISIONS

REV LTR	REVISION ISSUE DATE	PAGES REVISED ADDED DELETED OR CHANGE OF CLASSIFICATION	PREPARED BY	APPROVED BY
A	8-10-70	Original Issue	WFK	
B	9- -70	Added figure 2, Minor corrections throughout. Added omitted Branch absolute micro-instruction.	WFK	
C	1- -71	Sec 1 Changed Halt Interrupt to Console Interrupt. Changed length of FL from 20 to 16 bits. Sec 2 Deleted Base-Limit Adapter 3.1 Specified CPL>24 as undefined 3.1.2 Corrected descritpion of SUM for CPU=01 3.1.7 Added missing relational symbols 3.2.3 & 3.3.4 Changed Halt Interrupt to Console Interrupt 3.3.5 Changed length of FL register 3.3.7 Added "equal to" as being within limits 3.4.1 Added Exceptions 4 and 5 3.4.7 Added MSM(A) as destination in MTR mode 3.4.10 Corrected CPU to CPL in 1st para 3.4.25 Corrected note to reverse branch conti-tions on M=0000 3.4.29 Corrected V=010 to Read	WFK	
D	2-13-71	Changed name to B1502 Processor Sec. 1 Table 1 FLB changed to FT. MC deleted. MBR, BUSD, BUSC added Table 2 (XNY) ≠ 0 changed to INT. CC added timer & bus interrupts Sec 3.1 Deleted 6-bit operands throughout Sec 3.1.8 Added INT conditions Sec 3.2 FLB changed to FT 3.2.3 & 3.2.16 Added timer and bus interrupt 3.3.10 Added MBR register and changed description of A register to reflect changes in M-string addressing. 3.4.1 Excluded CPU as a source Allowed MBR, BUSC and BUSD as source-destination. 3.4.11 Changed Base Relate FA to Scratchpad relate FA	WFK	

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D		3.4.14, 3.4.15 & 3.4.20 Deleted 6-bit operands 3.4.16 Changed normalize X and Y to Normalize X 3.4.19 Specified Branch Relative as 2 clocks if the resultant address is beyond M-Max. 3.4.32 Added Moniter		
E	3/17/71	1 Table 1, MF deleted. TOPM added 3.2 TOPM Register added 3.3.10 TOPM Register and description added 3.4.12 Corrected Rotate register T right to Rotate left 3.3.14 Deleted use of MMAX to detect end of M Memory 3.3.16 Added BUSD and BUSC descriptions 3.4.17 Branch Absolute deleted 3.4.18 Call Branch Address changed to relative 3.4.19 Branch Relative - OP code and address container size changed 3.4.25 Corrected V=4 to V=3	WFK	
F	8/3/71	Changed name from B1502 to M-Memory Processor Preface & Rel. Specs: Added I/O Bus interface and add't specs. 1 Deleted MD &ME registers, added console lamp flip-flop. Changed name BUSD & BUSC to DATA & CMND. 3.1 Deleted paragraph on delay imposed if requested SUM-DIFF differs from micro to micro. 3.1.2 Changed condition for borrow-out level. 3.3.10 Added TOPM cleared to 1000. Added paragraph on moves to TOPM. 3.3.11 Deleted MD & ME. 3.4.13 Added note 3 and 4. 3.4.14 & 3.4.15 Deleted S/R count control by CPU. 3.4.20 Changed V=4, V=6 & V=7. 3.4.27 Deleted Clear Registers 2. 3.4.33 Added detailed info for monitor. 3.5 Added description of concurrent operation. 3.6 Added detailed timing information.		WFK, 11-2-71 AO 11/3/71
	11/25/71	Sec 3.1 & 3.1.2 Changed CPU=11 to undefined Sec 3.1.2 Clarified negative result format Sec 3.2.3 & 3.2.4 Deleted description redundant with sec 3.3.16	WFK	

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G	11/25/71	3.3.2 Deleted use of L register a temporary storage during overlay 3.3.11, 3.4.1 Added exception to M-Register bit-or in tape mode 3.3.13 Added lower 16 bits of register are are always zero. 3.3.14 Added lower 14 bits of register are always zero. 3.3.15 Added operation of U-Reg in tape mode 3.3.16, 3.3.17 Specified only two micros can reference DATA & CMND 3.4.2 Deleted use of MSM in tape mode as well as RUN & STEP 3.4.3 Time decreased from 2 to 1 3.4.7 Time decreased when A is destination from 4 to 3. 3.4.9 Added definition for MFL=25 and 26 on write operations 3.4.10 Added value of FL after overflow is undefined. Added Lit value of 25 through 31 are treated as 24. 3.4.11 Increased time from 1 to 2 3.4.14 Defined S/R for count=0. 3.4.16 Added CPL=0 is undefined, added plus one clock. 3.4.20 Changed value CPU set to when FU=8 3.4.22 & 3.4.25 Removed exclusion of pseudo registers but restrict use. 3.4.28 Specified plus 4 clocks 3.4.30 Added processor halts for V=2 3.4.31 Added info on state of M & A Reg 3.4.33 Added time and pulse width info Example four-interchange WAIT & BASE LIMIT check clocks.		
H	12/31/71	Sec 3.3.5 & 3.4.10 Specified wrap around for FL on overflow 3.3.10 Changed exception to note 1 3.3.10 & 3.4.1 Prohibited moves to TOPM & MBR from slow sources. 3.3.15 Prohibited TOPM as destination		W.F.K. 1-3-72 REP 1/5/72 TOM 1/12/72 EPM 1/11/72

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SYSTEMS M & E GROUP
SANTA BARBARA PLANT

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I	3-10-72	Sec. 2 Added M & E # Sec. 3.3.2 Added BIND uses L-Reg. 3.3.3 Added BIND uses T-Reg. 3.3.4 Added condition on overflow-underflow 3.3.10 Added BIND affect A MBR & TOPM Reg. 3.4.1 & 3.4.2 Reg/Scratchpad move: Increased time when binary SUM, binary DIFF,XYCN, XYST,BICN & FLCN are addressed and when Scratchpad is used as destination swap/store of scratchpad word: 3.4.3 & 3.4.4 Increased time 1 clock 3.4.11 Added condition on overflow-underflow 3.4.20 Bias: Increased time 1 clock when Test Flag = 1 3.4.22 Manipulate: Increased time 1 clock when XYCN,XYST,BICN,FLCN are addressed, increased time 1 clock when V = 5 & 7 3.4.23 & 3.4.24 Increased time 1 clock when XYCN,XYST,BICN,FLCN are addressed. 3.4.27 BIND: added new operator 3.4.28 Increased time by 1 clock for each 16 bits moved. 3.4.29 Added 17 MSB of T are unaffected by Read & Clear dispatch. 3.5 Added 1 clock NOP inserted after each concurrent micro. Figures: Increased by 1 clock time when Read Data is received. 3.6 Adjusted times to reflect new times.	WFK	
J	5-1-72	Sec. 3.1.1 & 3.1.7 Specified bit position pointed to by CPL=0. 3.1.6 & 3.1.8 Changed CPU conditions for LSUY & LSUX to be true. 3.2 Added CPU as an acceptable input for 4-bit operations. 3.2.1 & 3.2.2 Changed to sections 3.1.9 & 3.1.10 3.3.7 Specified count not inhibited if memory write is inhibited 3.3.10, 3.3.12 & 3.3.15 Removed restrictions on source-destination conbinations. 3.3.13 Changed resolution of MAXS from 8K to 4K bytes.	WFK	

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SYSTEMS M & E GROUP
SANTA BARBARA PLANT

M-MEMORY PROCESSOR

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J	Cont'd.	3.3.14 Changed resolution of MAXM from bits to 16-bit words. 3.3.17 & 3.3.18 Removed restrictions on operators allowed. 3.3.19, 3.3.20 & 3.3.21 Added NULL, READ & WRIT register descriptions. 3.4 All times removed-covered in Sec. 3.6 3.4.1 & 3.4.2 Allowed CPU & READ as sources & NULL as a destination. Excluded WRIT as source & destination. 3.4.1, 3.4.2 & 3.4.13 Removed requirement of 20 leading zeros in source when TOPM is destination. 3.4.1 Removed restriction of U as source in RUN mode & MSM as destination in STEP & RUN mode. Allowed TOPM & MBR as destinations with slow sources. 3.4.2 Removed restriction of U & MSM as sources. Allowed MSM as destination. 3.4.6 & 3.4.7 Allowed MSM as destination 3.4.13 Deleted CPL as source of S/R when S/R in instruction=0. Excluded READ & WRIT as destinations. Allowed MSM, DATA & CMND as destinations. 3.4.15 Defined S/R count if 0 is valid. 3.4.17 Added Read/Write MSM operations. 3.4.22 Deleted CPU from exceptions & added when specified as operand to exception 1 3.4.25 Allowed CPU as operand. 3.4.29 Added Write High & Port Absent operations. 3.4.30 Changed V=2 to stop only if in tape mode. 3.4.31 Added Action of halt in tape mode. 3.5 Added scratchpad relate FA & monitor to set of operations permitted to be concurrent. Added NOP after branch. Deleted SWAP from timing examples. 3.6 Increased SWAP, dispatch lockout operations times.		

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SYSTEMS M & E GROUP
SANTA BARBARA PLANT

M-MEMORY PROCESSOR

PRODUCT SPECIFICATION

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REV LTR	REVISION ISSUE DATE	PAGES REVISED ADDED DELETED OR CHANGE OF CLASSIFICATION	PREPARED BY	APPROVED BY
K	6-19-72	WKF Sec 3.6 Times increased or decreased as follows: Register Move & Scratchpad Move: Minus 1 clock when XYCN, XYST, FLCN or BICN is source. Plus 1 clock when TOPM or MSM is destination Minus 1 clock when MBR is destination & A is not out-of-bounds. Plus 5 clock's when M is destination and A is out-of-bounds. Specified time when U is source. Increased times by 1 clock when MSM, SUM, DIFF, DATA or U is a source with TOPM, A, MSM, DATA, CMND, or MBR (out-of-bounds) as a destination Scratchpad Move: Corrected time when DATA is a source from 4 to 3. Plus 1 clock when MSM is a source Plus 1 clock when previous OP was a write into scratchpad Move 8-bit Literal: Plus 1 clock when MSM is destination Plus 5 clocks when M is destination & A is out-of-bounds Move 24-bit Literal: Plus 1 clock when MSM is destination Plus 5 clocks when MSM or TAS is destination and A is out-of-bounds. Plus 4 clocks when other register is destination and A is out-of-bounds. Specified time when in tape mode. Write Memory: Specified time when memory cycle is inhibited Dispatch Port Absent: Specified time Shift/Rotate Register T: Plus 1 clock when TOPM or MSM is destination. Plus 2 clocks when DATA or CMND is destination Minus 1 clock when MBR is destination and A is not out-of-bounds. Plus 5 clocks when M is destination and A is out-of-bounds Shift/Rotate Register X/Y L/R: Plus 1 clock Shift/Rotate Register XY L/R: Plus 1 clock Bias: Minus 1 clock when Test Flag=1 and skip not taken Minus 1 clock when skip is not taken 4-bit Manipulate: Minus 1 clock for V=5 or 7 except for XYCN, XYST, FLCN and BICN Bit Test Branch False & Bit Test Branch True: Minus 1 clock for XYCN, XYST, FLCN, BICN Skip When: Minus 1 clock except for XYCN, XYST, FLCN, BICN Overlay M-Memory: Minus 1 clock		6-19-72 7/3/72 7-5-72 6-4-73

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#1913 1747

Burroughs Corporation

BUSINESS MACHINES GROUP
SMALL SYSTEMS PLANT

M-MEMORY PROCESSOR

PRODUCT SPECIFICATION

REVISIONS

REV LTR	REVISION ISSUE DATE	PAGES REVISED ADDED DELETED OR CHANGE OF CLASSIFICATION	PREPARED BY	APPROVED BY
L	5-24-74	Rel Spec: Deleted B1700 I/O Subsystem reference. Table 3: BIAS variants V=4, 6, 7 changed to CPL. Tape variant X=Y added. Sec 3.4.7: Excluded M and MSM as destination registers. Sec 3.4.13: Added CPL value used if S/R count in micro is zero. Sec 3.4.28: Removed A=A (max) as a condition for terminating operation. Sec 3.4.30: Added V=6 stop tape if X=Y. Sec 1: Added 6K M-Memory.	WFK	WFK 5-24-74 CEW 5 June 74 7-9-74

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SYSTEMS M & E GROUP
SANTA BARBARA PLANT

M-MEMORY PROCESSOR

PRODUCT SPECIFICATION

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PREFACE

This specification defines the functional requirements of the M-Memory Processor which is intended for general purpose data processing. Environmental conditions, safety conditions, reliability parameters, power requirements, etc., are specified in P.S. #1913 1739 Central Systems.

The processor communicates with other major units of the system such as main memory via the Port Interchange and to the I/O subsystem via either the I/O Bus Interface or the Port Interchange. It is connected directly to the control panel.

RELATED SPECIFICATIONS

P.S. #	NAME
1904 5681	B1700 System Index
1913 1739	B1700 Central System
2204 8623	B1700 I/O Bus Subsystem
1913 1754	B1700 Memory Subsystem
1913 1778	Port Interchange

S.D.S. #	NAME
2200 2083	Port Adapter - Port Device Interface

1 GENERAL DESCRIPTION

The M-Memory Processor provides the combinatorial and arithmetic portion of the system along with other registers and hard storage that are appropriate for efficient operation.

The Processor provides hardware sensitivity to a set of low-level micro-functions which are used in a program string to perform the normal processor functions of instruction fetch and execution. This micro-program is contained in either a local high speed Read-Write M-Memory or in the Main Memory or in both. The local M-Memory is modular and consists of the following sizes:

0 bytes
2K bytes
4K bytes
6K bytes
8K bytes

Included in the Processor are registers and psuedo registers which are addressable by the individual micro-operators.

The registers are normally addressed by a 4-bit group (row) number and a 2-bit select (column) number as shown in Table 1.

Some of the registers listed such as the psuedo sum register can serve only as a source register while others are capable of serving both as a source and as a destination register. Also some of the registers listed are actually subregisters which, although part of a larger register, can be individually addressed and manipulated.

A summary of the various conditions which are available by addressing particular psuedo source registers and actual registers is listed in Table 2.

A listing of the micro-instructions and their variants is given in Table 3.

A diagram of the Processor's major registers is shown in Figure 1.

2 PRODUCT IDENTIFICATION

M&E #	Name
2204 8839	M-Memory Processor
2204 8847	M-Memory Adapters

1 (Con't.)

GROUP NUMBER	SELECT NUMBER 0	1	2	3
0	TA	FU	X	SUM
1	TB	FT	Y	CMPX
2	TC	FLC	T	CMPY
3	TD	FLD	L	XANY
4	TE	FLE	A	XEOY
5	TF	FLF	M	MSKX
6	CA	BICN	BR	MSKY
7	CB	FLCN	LR	XORY
8	LA	TOPM	FA	DIFF
9	LB	UNASSIGNED	FB	MAXS
10	LC	UNASSIGNED	FL	MAXM
11	LD	UNASSIGNED	TAS	U
12	LE	XYCN	CP	MBR
13	LF	XYST	MSM	DATA
14	CC	INCN	READ	CMND
15	CD	CPU	WRIT	NULL

TABLE 1

BICN:	LSUY	CYF	CYD	CYL
XYCN:	MSBX	X=Y	X<Y	X>Y
XYST:	LSUX	INT	Y≠0	X≠0
FLCN	FL=SFL	FL>SFL	FL<SFL	FL≠0
INCN:	PORT DEVICE MISSING	PORT HI PRIORITY	PORT INTERRUPT	PORT LOCKOUT
CC:	CONTROL PANEL STATE LAMP FLIP-FLOP	TIMER INTERRUPT	I/O BUS INTERRUPT	CONTROL PNL INTERRUPT
CD:	MEMORY READ DATA PARITY ERROR INTERRUPT	MEMORY WRITE/SWAP ADDR OUT OF BOUNDS OVERRIDE	MEMORY READ ADDR OUT OF BOUNDS INTERRUPT	MEMORY WRITE/SWAP ADDR OUT OF BOUNDS INTERRUPT

TABLE 2

	MICRO NAME	MC 15	14	13	12	MD 11	10	9	8	ME 7	6	5	4	MF 3	2	1	0
1C	REGISTER MOVE	0	0	0	1	REG 1 GROUP SOURCE REGISTER				REG 1 SELECT		REG 2 SELECT		REG 2 GROUP SINK REGISTER			
2C	SCRATCHPAD MOVE	0	0	1	0	REGISTER GROUP SOURCE OR SINK				REG SELECT		MOV DIR	DPW 1/2	DOUBLE PAD WORD ADDRESS			
3C	4 BIT MANIPULATE	0	0	1	1	REGISTER GROUP, 4 BIT SOR & SNK				REG SEL	MANIPULATE VARIANTS			4 BIT MANIP. LITERAL			
4C	BIT TEST REL BRANCH FALSE	0	1	0	0	REGISTER GROUP, 4 BIT SOURCE				REG SEL	TEST BIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG			
5C	BIT TEST REL BRANCH TRUE	0	1	0	1	REGISTER GROUP 4 BIT SOURCE				REG SEL	TEST BIT NUMBER		DSP SGN	RELATIVE BRANCH DISPLACEMENT MAG			
6C	SKIP WHEN	0	1	1	0	REGISTER GROUP 4 BIT SOR & SNK				REG SEL	SKIP TEST VARIANTS			4 BIT TEST MASK			
7C	READ/WRITE MEMORY	0	1	1	1	R/W VAR	COUNT FA/FL VARIANTS			DATA REG CODE		TW SGN		DATA TRANSFER WIDTH MAGNITUDE			
8C	MOVE 8 BIT LITERAL	1	0	0	0	REGISTER GROUP, REG SEL IS 2.				ENTIRE 8 BITS OF 8 BIT LITERAL							
9C	MOVE 24 BIT LITERAL	1	0	0	1	REGISTER GROUP, REL SEL IS 2.				8 MOST SIGNIFICANT BITS OF FULL 24 BIT LITERAL							
10C	SHIFT/ROTATE T REG	1	0	1	0	SINK REGISTER GROUP				SNK REG SELECT		S/R VAR		LEFT SHIFT/ROTATE COUNT			
11C	EXTRACT FROM T REG	1	0	1	1	RIGHT BIT POINTER FOR EXTRACTION FLD				SNK REG CODE				EXTRACTION FIELD WIDTH			
12C	BRANCH RELATIVE	1	1	0	DSP SGN	RELATIVE DISPLACEMENT MAGNITUDE											
13C	CALL RELATIVE	1	1	1	DSP SGN	RELATIVE CALLED ADDRESS MAGNITUDE											
2D	SWAP MEMORY	0	0	0	0	0	0	1	0	DATA REG CODE		TW SGN		DATA TRANSFER WIDTH MAGNITUDE			
3D	CLEAR REGISTERS	0	0	0	0	0	0	1	1	L REG	T REG	Y REG	X REG	FA REG	FL REG	FU REG	CP REG
4D	SHIFT/ROTATE X OR Y	0	0	0	0	0	1	0	0	S/R DIR VARIANT		X/Y VAR		LEFT OR RIGHT, X OR Y SHIFT/ROTATE COUNT			
5D	SHIFT/ROTATE X AND Y	0	0	0	0	0	1	0	1	S/R DIR VARIANT				LEFT OR RIGHT X AND Y SHIFT/ROTATE COUNT			
6D	COUNT FA/FL	0	0	0	0	0	1	1	0	COUNT FA/FL VARIANTS				COUNT SCALAR MAGNITUDE			
7D	EXCHANGE DPW	0	0	0	0	0	1	1	1	SINK DPW ADDRESS				SOURCE DPW ADDRESS			
8D	SCRATCHPAD RELATE FA	0	0	0	0	1	0	0	0				DSP SGN	LEFT HALF PAD WORD ADDRESS			
9D	MONITOR	0	0	0	0	1	0	0	1	LITERAL OCCURRENCE IDENTIFIER							
1E	DISPATCH	0	0	0	0	0	0	0	0	0	0	0	1	DISPATCH VARIANTS			SKP FLG
2E	CASSETTE CONTROL	0	0	0	0	0	0	0	0	0	0	1	0	CASSETTE MANIP VARIANTS			
3E	BIAS	0	0	0	0	0	0	0	0	0	0	1	1	BIAS VARIANTS			TST FLG
4E	STORE F INTO DPW	0	0	0	0	0	0	0	0	0	1	0	0	SINK DPW ADDRESS			
5E	LOAD F FROM DPW	0	0	0	0	0	0	0	0	0	1	0	1	SOURCE DPW ADDRESS			
6E	CARRY FF MANIPULATE	0	0	0	0	0	0	0	0	0	1	1	0	CYF → CYD	CYF → CYL	CYF → 1	CYF → 0
7E	EXERCISE MEM(L)	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	R/W VAR
1F	HALT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
2F	OVERLAY MASKING	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3F	NORMALIZE X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4F	BIND ALGORITHM MIR	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VARIANTS	0 00 000	1 01 001	10 010	11 011	100	101	110	111
MOV DIR: 1/2 DPW:	P←R LEFT	R←P RIGHT						
MANIP. VARIANTS:	SET	AND	OR	EOR	INC	INC TEST	DEC	DEC TEST
DSP SIGN:	+	−						
DSP SIGN:	+	−						
SKIP TEST VARIANTS:	ANY CLR/	ALL CLR/	EQL CLR/	ALL CLR	ANY/ CLR/	ALL/ CLR/	EQL/ CLR/	ALL/ CLR
R/W VAR: CNT VAR: REG SEL: TW SIGN:	READ NOP X +	WRT FA↑ Y −	FL↑ T	FA↑ FL↑ L	FA↑ FL↑	FA↑	FL↑	FA↑ FL↑
S/R VAR:	SHFT	ROT						
SINK REG CODE:	X	Y	T	L				
DSP SIGN:	+	−						
DSP SIGN:	+	−						
TW SIGN: REG CODE:	+ X	− Y	T	L				
X/Y VAR: S/R. DIR:	X . SFT←	Y SFT→	ROT←	ROT→				
S/R. DIR VARIANTS:	SFT←	SFT→	ROT←	ROT→				
COUNT FA/FL VAR:	NOP	FA↑	FL↑	FA↑ FL↑	FA↑ FL↑	FA↑	FL↑	FA↑ FL↑
DSP SIGN:	+	−						
SKP FLAG: DISP VAR:	FAIL LOCK	SUCC WRTLO	READ	R&C	WRTHI	ABSNT	UNDEF	UNDEF
CASSETTE MANIP:	START TAPE	STOP GAP	STOP @ X+Y	UNDEF	UNDEF	Undef	STOP @ X=Y	UNDEF
TEST FLG: BIAS VAR:	TST/ UNIT	TEST F	S	FS	CPL	FCP	CPL	CPL
R/W VAR	READ	WRIT						

Table 3

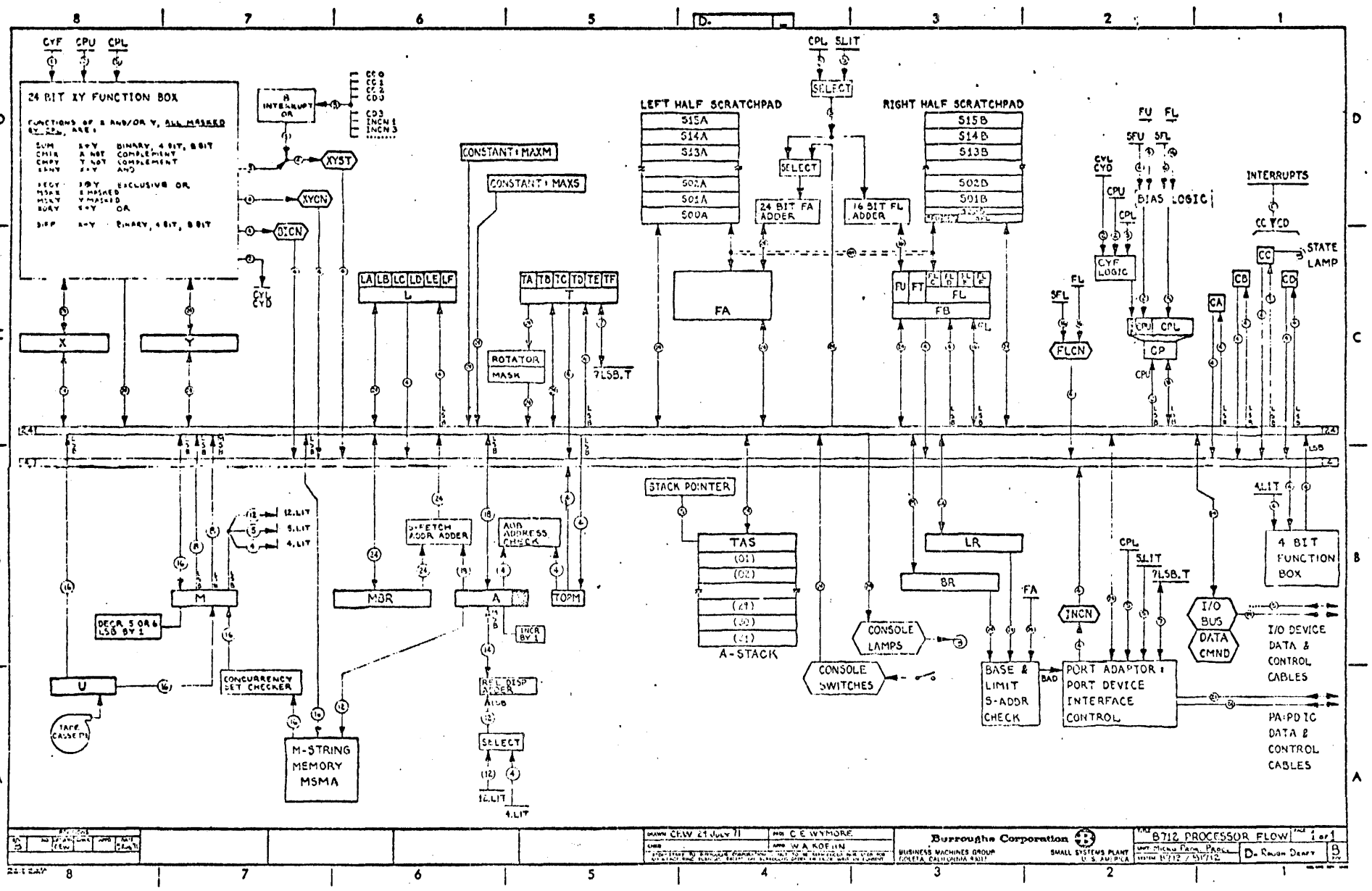

24 BIT XY FUNCTION BOX
CYF CPU CPL
CONSTANT: MAXM
CONSTANT: MAXS
LEFT HALF SCRATCHPAD
RIGHT HALF SCRATCHPAD
S15A
S14A
S13A
S02A
S01A
S00A
S15B
S14B
S13B
S02B
S01B
24 BIT FA ADDER
16 BIT FL ADDER
SELECT
FA
FL
FB
ROTATOR MASK
7LSB.T
INTERRUPTS
STATE LAMP
BIAS LOGIC
CYF LOGIC
FLCN
STACK POINTER
TAS
A-STACK
LR
BR
CONSOLE LAMPS
CONSOLE SWITCHES
BASE & LIMIT S-ADDR CHECK
PORT ADAPTOR: PORT DEVICE INTERFACE CONTROL
I/O BUS DATA CMND
4 BIT FUNCTION BOX
I/O DEVICE DATA & CONTROL CABLES
PA:PD IC DATA & CONTROL CABLES
M-STRING MEMORY MSMA
CONCURRENCY SET CHECKER
DECR 5 OR 6 LSB BY 1
TAPE CASSETTE
MBR
TOPM
Burroughs Corporation
B712 PROCESSOR FLOW
C E WYMORE
W A KOEHN
BUSINESS MACHINES GROUP
SMALL SYSTEMS PLANT
U.S. AMERICA

Figure 1

3. PRODUCT DESCRIPTION

3.1 TWENTY-FOUR BIT ARITHMETIC AND COMBINATORIAL SECTION

3.1.1 Sum

Sum is a psuedo Register equal to the sum of the X, Y and CYF registers (X+Y+CYF). Zero bits in the more significant bit positions of the 24-bit result are produced when the length as determined by CPL is less than 24. Results are not defined for CPL values 25 through 31. The carry out level is generated from the bit position of the output specified by CPL. If CPL = 0, the carry out level is equal to CYF. If CPL = 1, the carry out level is generated from the rightmost bit of X, Y and CYF.

If CPU=00, the binary sum is produced.

If CPU=01, the decimal sum is produced by considering the X and Y inputs to be comprised of six 4-bit units. Results are not defined for non-BCD units. CPL must be a multiple of four.

If CPU=10 or 11, the sum is undefined.

3.1.2 Difference

Difference is a psuedo Register equal to the difference of the X, Y and CYF registers (X-Y-CYF). Zero bits in the more significant bit positions of the 24-bit result are produced when the length as determined by CPL is less than 24. Results are not defined for CPL values 25 through 31. The borrow out level is generated from the static comparison of all 24-bits of X&Y and is true if X<Y or if X=Y and CYF is true.

If CPU=00, the binary difference is produced.

If CPU=01, the decimal difference is produced by considering the X&Y inputs to be comprised of six 4-bit units. Results are not defined for non-BCD units. CPL must be a multiple of four.

If CPU=10 or 11, the difference is undefined.

A negative result in the case of binary is in the 2's complement form while for decimal, a negative result is in the 10's complement form.

3.1.3 And/Or/Exclusive-Or

The result of the appropriate logical function and/or/exclusive-or of the "X" and "Y" registers is produced. Zero bits in the more significant bits positions of the 24-bit result are produced when the length as determined by "CPL" is less than 24. Results are not defined for CPL values 25 through 31.

3.1.4 Complement X/Complement Y

The 1's complement of the appropriate register "X" or "Y" is produced. Zero bits in the more significant bits positions of the 24-bit result are produced when the length as determined by "CPL" is less than 24. Results are not defined for CPL values 25 through 31.

3.1.5 Masked X/Masked Y

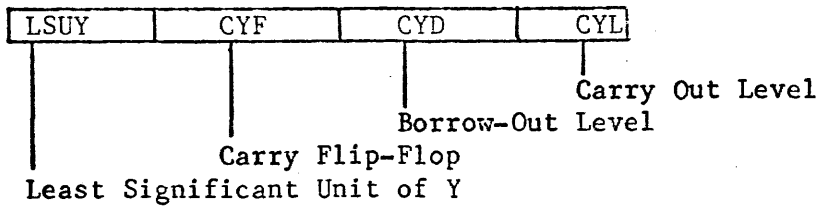
The contents of the appropriate register "X" or "Y" is produced. Zero bits in the more significant bit positions of the 24-bit result are produced when the length as determined by "CPL" is less than 24. Results are not defined for CPL values 25 through 31.

3.1.6 Binary Conditions (BICN)

The following binary conditions considered as a 4-bit group are produced and are addressable as a source only.

NOTE: "CYF" is also addressed by the Set CYF M-Instruction as well as being available in the (8-bit) group addressed as CP.

BICN:



The carry out is a function of "X", "Y", "CPL" and CPU. See Section 3.1.1. The borrow-out level is a function of "X", "Y" and "CYF". See Section 3.1.2.

"LSUY" is true if the least significant unit of "Y" is equal to "1" and CPU=00 or 10 or the least significant unit of "Y" is equal to 1001 and CPU=01 or 11.

3.1.7 XY Condition (XYCN)

The following relational conditions considered as a 4-bit group are produced and are addressable as a source only.

XYCN:

MSBX	X=Y	X<Y	X>Y

MSBX is true if the bit in "X" referenced by CPL is one. CPL=1 reference the rightmost bit while CPL=24 reference the leftmost bit of "X". MSBX=0 if CPL=0.

The relational results are based on the binary value of all 24-bits of X and Y.

3.1.8 XY States (XYST)

The following relational conditions considered as a 4-bit group are produced and are addressable as a source only.

XYST:

LSUX	INT	Y≠0	X≠0

"LSUX" is true when the least significant unit of "X" is equal to "1" and CPU=00 or 10 or when the least significant unit of "X" is equal to 1001 and CPU = 01 or 11.

The relational results are based on the binary value of all 24 bits of X or Y.

"INT" is true if any of the following conditions as reflected in INCN, CC and CD are true. (See section 3.1.10 and 3.3.16.)

1. Missing Port Device
2. Port Interrupt
3. Timer Interrupt
4. BUS I/O Interrupt
5. Control Panel Interrupt
6. Memory Parity Error Interrupt
7. Memory Write/Swap Address Out of Bounds Interrupt

3.1.9 FLCN (Field Length Conditions)

The result of a static comparison of the FL portion of the FB register and the corresponding portion of the first scratchpad word is addressable as FLCN. It carries the following information:

FLCN:

FL=SFL	FL > SFL	FL < SFL	FL ≠ 0

3.1.10 INCN (Interrupt Conditions)

The condition of particular interface lines beween the processor and the port interchange is addressable as INCN. It carries the following information:

INCN:

PORT MISSING DEVICE	PORT HI PRIORITY INTERRUPT	PORT INTERRUPT	PORT LOCKOUT

3.2 FOUR-BIT ARITHMETIC AND COMBINATORIAL SECTION

The 4-bit arithmetic and combinatorial section of the processor can accept as one of its inputs the contents of any of the following 4-bit registers and pseudo registers. The second input is obtained from the M-Instruction itself.

INPUTS

TA	TB	TC	TD	TE	TF
LA	LB	LC	LD	LE	LF
FU	FT	FLC	FLD	FLE	FLF
CA	CB	CC	CD	TOPM	CPU
BICN	XYCN	XYST	FLCN	INCN	

Its outputs include the result of most of the commonly used functions between two operands. These include the generation of the SET, AND, OR, EXCLUSIVE-OR, BINARY MODULO SIXTEEN SUM, and BINARY MODULO SIXTEEN DIFFERENCE functions. This output is directed back to the source register.

The sum and difference output can be tested for overflow and underflow respectively and a skip of one instruction based on the test can be made.

This section also provides for the selective testing of one of the bits of a four bit group and relative branching based on the result of the test. The skip of one instruction based on the result of a test on a combination of up to four bits in the group is also provided.

BICN, XYCN, XYST, FLCN and INCN are not actually registers but can be sourced as if they were. They can be changed only as a result of changing the condition which they reflect.

CPU is actually a 2-bit register but can be addressed as if it were a 4-bit register whose leftmost 2 bits are always equal to zero.

3.3 REGISTER SECTION

3.3.1 X and Y Registers

The X-Register and the Y-Register are 24-bit general purpose registers used primarily to hold and to act as a source for the two operands of the arithmetic and combinatorial unit. Each register is addressable as a source and as a sink.

Both registers along with the L-Register and the T-Register are capable of Read/Write operations with main memory.

Both registers are capable of the shift/rotate operation. The X-Register is capable of the normalize and the Read/Write MSM operations.

3.3.2 L-Register

The L-Register is a 24-bit general purpose register used typically to hold logical flags for the micro-program code. The L-Register, as well as each 4-bit group of L denoted as LA, LB, LC, LD, LE and LF is addressable as a source and as a sink.

Dispatch operations use the L-Register as the source or sink for a 24-bit message (usually an address) which is stored in/ fetched from S-Memory location zero.

Overlay operations use the L-Register as the source of the starting M-Memory address to be used in the M-Memory overlay operation.

The Bind operator uses the L-Register as the source of the 24-bit value to be moved to the MBR-Register.

Since the L-Register is addressable in 4-bit groups, its contents are available for analysis and alteration via the 4-bit function box. Manipulate, skip and bit test branch instructions can operate on L data.

The L-Register is one of 4 registers (X, Y, L, and T) capable of Read/Write operations with main memory.

The Read/Write MSM operator uses the L-Register as the source of the M-Memory address to be used in the operation.

3.3.3 T-Register

The T-Register is a 24-bit general purpose register used primarily for the interpretation of S-Language instructions. The T-Register, as well as each 4-bit group of T denoted as TA, TB, TC, TD, TE and TF, is addressable as a source and as a sink.

Dispatch operations use the least significant seven bits of T as the source or sink for the port and channel information associated with the dispatch operation.

The Bind operator uses the T-Register as the source of the 4-bit value to be moved to the TOPM-Register and as the source of the 14-bit value to be moved to the A-Register. The value to be moved to TOPM is contained in the rightmost (LSB) 4 bits of T while the value to be moved to A is contained in the leftmost (MSB) 20 positions of T. Note that data when moved to A will be truncated on the left.

Since the T-Register is addressable in 4-bit groups, its contents are available for analysis and alteration via the 4-bit function box. Manipulate, skip and bit test branch instructions can operate on T data.

The T-Register is one of 4 registers (X, Y, L, and T) capable of Read/Write operations with main memory.

The T-Register is also capable of the shift/rotate and extract operations.

3.3.4 FA-Register

The FA-Register (Field Address) is a 24-bit register used primarily to hold an absolute bit address for main memory. It has the capability of directly addressing any bit in the memory starting at any point.

The FA-Register is addressable as a source and as a sink.

The FA-Register is capable of being counted up or down by a literal in a micro-instruction or by the value contained in CPL in order to facilitate iteration through a memory field. It can be incremented or decremented by a value in a left scratchpad word. It also has the ability of being loaded, stored, or swapped along with FB into a double scratchpad word.

Neither overflow nor underflow of FA is detected. The value of FA may go through its maximum value or its minimum value and wrap around.

3.3.5 FB-Register

The FB-Register is a 24-bit register which can be functionally divided into three portions: a 4-bit FU (Field Unit) register, a 4-bit FT (Field Type) register, and a 16-bit FL (Field Length) register.

The FB-Register, as well as each 4-bit portion of FB denoted as FU, FT, FLC, FLD, FLE and FLF is addressable as a source and as a sink. In addition, the 16-bit portion comprised of FLC, FLD, FLE and FLF and denoted as FL is also addressable as a source and as a sink.

The FU-Register holds the length of the unit which makes up a field in memory. The FT-Register holds field type information while the FL-Register holds the total length of the field. FL is capable of describing fields up to 65,536 bits and can be adjusted up or down by a literal in a micro-instruction or by the value contained in CPL in order to facilitate iteration through a memory field.

Note: Overflow of FL is not detected. The value of FL will go through its maximum value and wrap around. Underflow of FL is detected and will not wrap around. The value of zero is left in FL.

Since the FB-Register is addressable in 4-bit groups, its contents are available for analysis and alteration via the 4-bit function box. Manipulate, skip and bit test branch instructions can operate on FB data.

FB has the ability of being loaded, stored, or swapped along with FA into a double scratchpad memory word.

FU and FL along with corresponding portions of the first cell of scratchpad are used to set the various conditions of FLCN (see section 3.1.9) and the various conditions of the CP register (see section 3.4.20 Bias).

3.3.6 Scratchpad Memory

A scratchpad of 16 words of 48 bits is provided to hold field descriptors during the iteration of operands. Some cells may be used to hold S-Language stack pointers and other processor registers which are under constant manipulation.

The FU and FL portion of the FB-Register and like portions of the first cell of the scratchpad are used to set the various conditions of FLCN (see section 3.1.9) and the various conditions of the CP register (see section 3.4.20 Bias).

3.3.7 Base and Limit Registers

The LR and BR Registers are both 24-bit registers and are used for memory protection and for base relative addressing. Memory protection is provided by checking the memory address in FA with the BR (Base Register) and the LR (Limit Register) for all memory cycles. Any address outside these bounds is flagged in the CD register. A memory read operation is always allowed whether inside or outside the boundary, but a write or swapcycle is allowed outside the boundary only if the override bit of the CD register is true. A memory address equal to the BR or LR is considered in bounds. Note: The memory protection is provided only on the initial pointer and does not provide protection on those memory bits accessed when the Field Length is greater than one. The count operation specified by the count variants will take place regardless of whether or not the memory cycle takes place.

Each register is addressable as a source and as a sink.

3.3.8 TAS Register

The TAS-Register is a 24-bit register which is the top of the A-Stack. The TAS-Register is addressable as a source and as a sink. References to TAS result in the stack being automatically pushed or popped.

3.3.9 A-Stack

The A-Stack is a 32 word deep 24 bit wide memory, without automatic hard overflow, which operates as a push-down stack with a last-in, first-out type of structure. Using this stack, the M-String routines operate in the normal software call-return type of programming. This allows for a highly shared M-String structure and reduces the M-String memory requirements. Although the A-Stack is not intended to be used as an operand stack, it has purposely been made 24 bits wide to allow limited capabilities for operand storage.

Wrap around of the TAS pointer is provided. That is, 32 consecutive pops or 32 consecutive pushes will cause the TAS pointer to contain its original contents.

3.3.10 A, MBR and TOPM Registers

The A-Register is a 14-bit micro-program address register capable of addressing 16,384 micro-operaters located in M-Memory and and/or Main Memory.

The A-Register is capable of having binary increments from 0 through 4095 added to or subtracted from it with a high speed carry adder to facilitate micro-program branching. The A-Register is automatically incremented during run mode. Wrap-around can occur and is permitted.

The A-Register can be addressed as a source and as a sink. When used as a source, the contents of the A-Register is multiplied by 16. When used as a destination, the rightmost 4-bits of the source are lost.

Associated with the A-Register is a 4-bit TOPM-Register. This register, multiplied by 512, is compared with the A-Register to determine which memory (M-String or Main) from which to access the micro-operator.

If the address in the A-Register is equal to or is greater than the address denoted by (512)X(TOPM), the micro-operator is obtained from main memory, otherwise, it is obtained from the M-Memory.

To obtain the micro-operator from main memory, the A address is multiplied by 16 and added to a 24-bit MBR-Register to yield a bit address pointing to the micro-operator.

Both the TOPM and the MBR registers are addressable as a source and as a sink.

The TOPM register is cleared to the binary value 1000 by the system clear signal.
The MBR, A, and TOPM registers are addressed as destination registers by the MICRO operator "Bind."

3.3.11 M-Register

The M-Register (micro-register) is a 16 bit register which is used to hold the active M-Operator. The state of this register is decoded to enable the different control signals within the processor to perform the operations called for by the M-Operator. The M-Register is broken into 4 fields for decoding that are structured such that 60 distinct micro-operations can be decoded.

The M-Register is addressable as a source and as a sink. When used as a sink register, the source is bit-or-ed with the up and coming M-Operator. Exception: In tape mode, the source is not bit-or-ed with the up and coming M-operator.

3.3.12 M-String Memory (MSM)

M-String Memory is a high speed memory which is used to hold the sequences of micro-instructions which perform the macro operations called for by S-language operators normally located in main memory. M-Memory is available in four sizes: Zero, 1024, 2048, and 4096 16-bit words. Any excess strings of micro-instructions which do not fit into the installed M-Memory are located in main memory.

Normal micro-programming should order the micro-instruction sequences of the speed important functions first so that the fastest execution speed possible is achieved regardless of the actual size of the installed M-Memory.

Significant improvements in throughput are achieved when more and more of the important sequences of M-Instructions are located in the M-Memory since the M-Memory is at least 5 times the speed of the main memory and the processor is capable of overlap operation with main memory.

The M-Memory is addressable as a source and as a sink. The location accessed is usually determined by the contents of the A-Register which is normally pointing to the next micro-operator. However, the micro-operator READ/WRITE MSM accesses the word determined by the contents of the L-Register as does the move SMEM to MMEM (overlay) micro-operator.

3.3.13 MAXS Register

The MAXS-Register is a 24-bit pseudo register which can be set by a field engineer to indicate the maximum size in bits of the installed S-memory. The MAXS-Register is addressable as a source register only. The lower 15 bits of the register are always zero. (Resolution: 4K bytes.)

3.3.14 MAXM Register

The MAXM-Register is a 24-bit pseudo register which can be set by a field engineer to indicate the maximum size in words of the installed M-Memory. The MAXM-Register is addressable as a source register only. The lower 10 bits of the register are always zero. (Resolution: 1K words.)

3.3.15 U-Register

The U-Register is a 16-bit register used primarily to accumulate the bit by bit input from the control panel's tape cassette. The U-Register is addressable as a source register only.

In run mode, if data is not yet available in the register, the micro-operator will be delayed.

In tape mode, the register's contents are automatically moved to the M-Register for execution except when executing micros which reference the U-Register as a source. In these cases the source data is moved directly from the U-Register to the destination and will not be treated as an instruction to be executed. The next instruction from the tape will follow this data. In the case of "Move 24-bit literal", the 8 bits of the literal in the M-Register are also moved to the destination.

In tape mode, the execution of a conditional branch may affect a change in the A register but will not cause the next micro-operator read from the tape to be skipped.

3.3.16 C-Registers

The C-Register is a 24-bit register which is not addressable as an entity but which is functionally divided into one 8-bit section and four 4-bit sections.

The 8-bit section addressed as CP is comprised of the arithmetic unit carry flip-flop (CYF), the 2-bit unit control for the arithmetic unit (CPU) and the 5-bit variable data length control (CPL). CPU is also addressable as a source and as a sink and when so addressed can be treated as if it were a 4-bit register whose leftmost 2 bits are always equal to zero.

CP:

CYF	CPU	CPL
0...1	0...3	0...31

↑ LSB

The remaining 16-bits of the C-Register are addressable in 4-bit groups as CA, CB, CC and CD. Their contents are available for analysis and alteration via the 4-bit function box. Manipulate, skip and bits test branch instructions are applicable.

The 4-bit groups designated as CA and CB have no special functional assignment and are available as general purpose 4-bit storage registers.

The 4-bit group designated as CC and CD are used for the storage of various processor states and conditions as shown below:

CC:

CONTROL PNL STATE LAMP FLIP-FLOP	TIMER INTERRUPT	I/O BUS INTERRUPT	CONTROL PNL INTERRUPT

↑ LSB

CD:

MEMORY READ DATA PAR ERROR INTERRUPT	MEMORY ADDRESS WRITE/SWAP OUT OF BOUNDS OVERRIDE CONTROL	MEMORY ADDRESS READ OUT OF BOUNDS INTERRUPT	MEMORY ADDRESS WRITE/SWAP OUT OF BOUNDS INTERRUPT

↑ LSB

The Control Panel State Lamp Flip-Flop when true will cause a lamp on the control panel to light.

The control panel's interrupt level is derived from the on position of the control panel's interrupt switch.

The BUS interrupt level is derived from the various I/O controls connected to the processor's I/O BUS. The signal is the result of a service request by one or more controls.

The timer interrupt signal is developed from the primary power frequency. A field engineer adjustment is required for either 50HZ or 60HZ. The interrupt signal is received and is used to set the appropriate CC-bit once every 100 milliseconds.

3.3.16 Cont'd

The memory address out of bounds signals are derived from logic which compares the contents of the FA register with the contents of the base (BR) and limit (LR) registers on all memory accesses. The state of the out of bounds override control bit does not affect the setting of out of bounds interrupt bits but does affect whether or not a memory write operation takes place. (See section 3.3.7)

The memory read parity error is received from the Processor's Interface to the port interchange.

No reaction occurs as a result of any interrupt until the microprogram tests the interrupt bit.

3.3.17 DATA-Register

DATA-Register is a 24-bit pseudo-register which can act as a source or as a destination. It is used to transfer data to and from the I/O BUS. When used as a source the processor generates the RC (Response Complete) signal to the interface and accepts the 24-bits of data from the BUS. When used as a destination, the processor generates the RC signal to the interface and the data from the designated source to the BUS.

3.3.18 CMND-Register

CMND-Register is a 24-bit pseudo-register which can act as a destination only. It is used to transfer command to devices on the I/O BUS. The processor generates the CA signal to the interface and the data (command) from the designated source to the BUS.

3.3.19 NULL-Register

NULL-Register is a 24-bit pseudo-register which can act as a source and as a destination.

When addressed as a source, all zeros are supplied to the destination.

When addressed as a destination the source data is not accepted. However NULL is useful as a destination in order to pop the TAS-Register without affecting other registers.

3.3.20 READ-Register

READ-Register is a 24-bit pseudo-register which can act as a source only.

When addressed as a source the position of the switches on the control panel is supplied to the destination.

3.3.21 WRIT

WRIT is not permitted to be addressed as a source or as a destination.

3.4 M-INSTRUCTIONS

3.4.1 Register Move

FORMAT:

OP CODE 0001	SOURCE REGISTER GROUP # 0 - 15	SOURCE REGISTER GROUP # 0...3	DESTINATION REGISTER SELECT # 0...3	DESTINATION REGISTER GROUP # 0...15

Move the contents of the source register to the destination register. If the move is between registers of unequal lengths, the data is right justified with left (most significant) zero bits supplied or with data truncated from the left whichever is appropriate.

The contents of the source register are unchanged unless it is also the destination register.

Exceptions:

1) When M is used as a destination register in run or step mode, the operation is changed to a bit-or which modifies the next micro-operation. It does not modify the instruction as stored in the memory. In tape mode, no bit-or takes place.
2) WRIT and CMND are excluded as source registers.
3) BICN, FLCN, XYCN, XYST, INCN, READ, WRIT, SUM, CMPX, CMPY, XANY, XEOY, MSKX, MSKY, XORY, DIFF, MAXS, MAXM and U are excluded as destination registers.
4) When DATA is designated as a source, CMND and DATA are excluded as destinations.
5) When U or DATA is designated as a source and when the next micro is to be obtained from S-Memory, M is excluded as a destination.

3.4.2 Scratchpad Move

FORMAT:

OP CODE 0010	REGISTER GROUP # 0...15	REGISTER SELECT # 0...3	DIRECTION 0-TO SCRATCHPAD 1-FROM SCRATCH-PAD	SCRATCHPAD WORD 0-LEFT WORD 1-RIGHT WORD	SCRATCHPAD WORD ADDRESS 0...15

Move the contents of the register (scratchpad) to the scratchpad (register). If the move is between registers of unequal lengths, the data is right justified with left (most significant) zero bits supplied or with data truncated from the left whichever is appropriate.

The contents of the source register are unchanged.

Exceptions:

1) When M is used as a destination register, the operation is changed to a bit-or which modifies the next micro-operation. It does not modify the instruction as stored in the memory.
2) WRIT and CMND are excluded as source registers.
3) BICN, FLCN, XYCN, XYST, INCN, READ, WRIT, SUM, CMPX, CMPY, XANY, XEOY, MSKY, MSFY, XORY, DIFF, MAXS, MAXM and U are excluded as destination registers.

3.4.3 Swap F with Doublepad Word

FORMAT:

OP CODE 0000 0111	DESTINATION 48-BIT SCRATCHPAD WORD 0...15	SOURCE 48-BIT SCRATCHPAD WORD 0...15

Move the contents of the FA and FB registers to a holding register. Move the contents of the left and right word of the source scratchpad word to the FA and FB register respectively. Move the contents of the holding register to the left and right word of the destination scratchpad word.

3.4.4 Store F into Doublepad Word

FORMAT:

OP CODE 0000 0000 0100	SCRATCHPAD WORD ADDRESS 0...15

Move the FA and FB register's contents to the left and right word respectively of the designated scratchpad word.

3.4.5 Load F From Doublepad Word

FORMAT:

OP CODE 0000 0000 0101	SCRATCHPAD WORD ADDRESS 0...15

Move the contents of the left and right word of the designated scratchpad word to the FA and FB register respectively.

3.4.6 Move 8-Bit Literal

FORMAT:

OP CODE 1000	DESTINATION REGISTER GROUP # 0...15	LITERAL 0...255

Move the 8-bit literal given in the instruction to the destination register. If the move is between registers of unequal lengths, the data is right justified with left (most significant) zero bits supplied. The register select number is assumed to be 2.
Exceptions:

Read and Writ are excluded as destination registers.

3.4.7 Move 24-Bit Literal

FORMAT:

OP CODE 1001	DESTINATION REGISTER GROUP # 0...15	24-BIT LITERAL 0...MAX

Move the 24-bit literal given in the instruction to the destination register. If the move is between registers of unequal lengths, the literal is truncated from the left. The register select number is assumed to be 2.
Exceptions:

Read, Writ, M and MSM (except in tape mode) are excluded as destination registers.

3.4.8 Swap Memory

FORMAT:

OP CODE 0000 0010	REGISTER # 00 = X 01 = Y 10 = T 11 = L	FIELD DIRECTION 0 - POSITIVE 1 - NEGATIVE	MEMORY FIELD LENGTH 0...24

Swap data from main memory with the data in the specified register. If the value of the memory field is less than 24, the data from memory is right justified with left (most significant) zero bits supplied while the data from the register is truncated from the left.

Register FA contains the bit address of the memory field while the field direction sign and field length is given in the instruction.

If the value of the memory field length as given in the instruction is zero, the value given in CPL is used.

3.4.9 Read/Write Memory

FORMAT:

OP CODE 0111	DIRECTION 0 TO REGISTER 1 TO MEMORY	COUNT VARIANTS 0...7	REGISTER # 00 = X 01 = Y 10 = T 11 = L	FIELD DIRECTION 0 - POSITIVE 1 - NEGATIVE	MEMORY FIELD LENGTH 0...26

Move the register's (memory's) contents to the memory (register). If the value of the memory field length is less than 24, the data from memory is right justified with left (most significant) zero bits supplied while the data from the register is truncated from the left.

The contents of the source is unchanged.

Register FA contains the bit address of the memory field while the memory field direction sign and memory field length is given in the instruction.

If the value of the memory field length as given in the instruction is zero, the value in CPL is used.

Memory field length values (or CPL values if MFL=0) of 25 and 26 are truncated to the value 24. When used on a write operation, the value 25 and 26 cause odd and even parity respectively to be written into memory regardless of the parity of the read data.

For a description of the count variants, see section 3.4.10.

3.4.10 Count FA/FL

FORMAT:

OP CODE 0000 0110	COUNT VARIANTS 0...7	LITERAL 0...31

Increment (decrement) binarily the designated register(s) by the value of the literal contained in the instruction or by the value of CPL if the value of the literal is zero.

Neither overflow nor underflow of FA is detected. The value of FA may go through its maximum value or its minimum value and wrap around.

Overflow of FL is not detected. The value of FL will go through its maximum value and wrap around. Underflow of FL is detected and will not wrap around. The value of zero is left in FL.

Literal values (or CPL values if LIT=0) of 25 through 31 are truncated to the value 24.

Count variants are as follows:

V = 000 No count
    001 Count FA Up
    010 Count FL Up
    011 Count FA Up and FL Down
    100 Count FA Down and FL Up
    101 Count FA Down
    110 Count FL Down
    111 Count FA Down and FL Down

3.4.11 Scratchpad Relate FA

FORMAT:

OP CODE 0000 1000	RESERVED 000	SIGN OF SPAD WORD 0-POSITIVE 1-NEGATIVE	LEFT SCRATCHPAD WORD ADDRESS 0...15

Replace the contents of the FA register by the binary sum of the FA register and the specified scratchpad register.

Neither overflow nor underflow of FA is detected. The value of FA may go through its maximum value or its minimum value and wrap around.

3.4.12 Extract From Register T

FORMAT:

OP CODE	ROTATE BIT COUNT	DESTINATION REGISTER	EXTRACT BIT COUNT
1011	0...24	00 - X 01 - Y 10 - T 11 - L	0...24

Rotate register T left by the number of bits specified and then extract from the right the number of bits specified. Move this result to the destination register supplying left most (most significant) zero bits if the extract count is less than 24.

The contents of the source register is unchanged unless it is also the destination register.

A rotate value of 24 is equivalent to 0.

3.4.13 Shift/Rotate Register T Left

FORMAT:

OP CODE	DESTINATION REGISTER GROUP #	DESTINATION REGISTER SELECT #	S/R VARIANT:	S/R BIT COUNT
1010	0...15	0...3	0 - SHIFT 1 - ROTATE	0...24

Shift (Rotate) register T left by the number of bits specified and then move the 24-bit result to the destination register. If the move is between registers of unequal lengths, the data is right justified with data truncated from the left.

The contents of the source register is unchanged unless it is also the destination register.

Zero fill on the right and truncation on the left occurs for the shift operation.

If the value of the shift/rotate count as given in the instruction is zero, the value given in CPL is used.

Exceptions:

1) When M is used as a destination register, the operation is changed to a bit-or which modifies the next micro-operation. It does not modify the instruction as stored in the memory.
2) BICN, FLCN, XYCN, XYST, INCN, READ, WRIT, SUM, CMPX, CMPY, XANY, XEOY, MSKX, MSKY, XORY, DIFF, MAXS, MAXM and U are excluded as destination registers.

3.4.14 Shift/Rotate Register X/Y Left/Right

FORMAT:

OP CODE 0000 0100	S/R VARIANT 0-SHIFT 1-ROTATE	L/R VARIANT 0-LEFT 1-RIGHT	X/Y VARIANT 0-X REG 1-Y REG	S/R BIT COUNT 0...24

Shift (rotate) register X(Y) left (right) by the number of bits specified.

Zero fill on the right and truncation on the left occurs for the left shift. Zero fill on the left and truncation on the right occurs for the right shift.

3.4.15 Shift/Rotate Registers XY Left/Right

FORMAT:

OP CODE 0000 0101	S/R VARIANT 0-SHIFT 1-ROTATE	L/R VARIANT 0-LEFT 1-RIGHT	S/R BIT COUNT 0...48

Shift (rotate) registers X and Y left (right) by the number of bits specified. The register X is the leftmost (more significant) half of the concatenated 48-bit XY register.

Zero fill on the right and truncation on the left occurs for the left shift. Zero fill on the left and truncation on the right occurs for the right shift.

3.4.16 Normalize X

FORMAT:

OP CODE 0000 0000 0000 0011

Shift the X register left while counting FL down, until FL=0 or until the bit in X referenced by CPL is a one. Zeros are shifted into the rightmost end of X.

CPL = 1 references the rightmost bit of X while CPL=24 references the leftmost bit of X. CPL=0 is undefined.

3.4.17 Read/Write MSM

FORMAT:

OP CODE	UNUSED	R/W VARIANT
0000 000 0111	000	0 TO X 1 FROM X

Move the contents of the X Register to the MSM word specified by the address contained in the L-Register if R/W variant bit = 1. The data is truncated from the left.

Move the contents of the MSM word specified by the address contained in the L-Register to the X-Register if R/W variant bit = 0. The data is right justified with left (most significant) zero bits supplied.

The lower 4 bits and the upper 8 bits of the address in L are ignored.

The operation of this instruction causes the A-register to be moved to the TAS-Register and the L- Register to be moved to the A-Register before reading or writing MSM. The TAS is restored to A after the Read/Write operation is completed.

3.4.18 Call

FORMAT:

OP CODE	DISPLACEMENT SIGN	DISPLACEMENT VALUE
111	0=POSITIVE 1=NEGATIVE	0...4095

Push the address of the next in-line micro-instruction into the A-Stack and then fetch the next micro-instruction from the location obtained by adding the signed displacement value given in the instruction to the address of the next in-line micro-instruction.

A displacement value indicates the number of 16-bit words.

Note: When the A address is stored in the A-stack, it is multiplied by 16 and stored as a bit address.

Note: Exit is accomplished by employing the Move Register instruction with the TAS as the source register and A as the destination register.

3.4.19 Branch

OP CODE	DISPLACEMENT SIGN	DISPLACEMENT VALUE
110	0=POSITIVE 1=NEGATIVE	0...4095

Fetch the next micro-instruction from the location obtained by adding the signed displacement value given in the instruction to the address of the next in-line micro-instruction.

A displacement value indicates the number of 16-bit words.

3.4.20 Bias

FORMAT:

OP CODE	VARIANTS	TEST CPL ≠ 0 FLAG
0000 0000 0011	0...7	0 - NO TEST 1 - TEST CPL RESULT

Set CPU to the value 1 if the value of FU is 4 or 8 and to 0 otherwise unless V=2, in which case, the value set into CPU is determined by SFU in lieu of FU.

Set the value of CPL to the value denoted or to the smallest of the values denoted in the following table.

V	VALUES
0	FU
1	24 and FL
2	24 and SFL
3	24 and FL and SFL
4	CPL
5	24 and CPL and FL
6	CPL
7	CPL

If test flag equals 1 and final value of CPL is not zero, the next 16-bit micro-instruction is skipped.

3.4.21 Set CYF

FORMATS:

OP CODE	VARIANTS
0000 0000 0110	1,2,4,8

Set the carry flip-flop as specified by the variants.

V = 1 Set CYF to 0
2 Set CYF to 1
4 Set CYF to CYL
8 Set CYF to CYD

Note CYD = (X<Y) + (X=Y)·CYF.

3.4.22 4-Bit Manipulate

FORMAT:

OP CODE	REGISTER GROUP #	REGISTER SELECT #	VARIANTS	LITERAL
0011	0...15	0...1	0...7	0...15

Perform the operation specified by the variants on the designated register.

V=0 SET THE REGISTER TO THE VALUE OF THE LITERAL.
1 SET THE REGISTER TO THE LOGICAL AND OF THE REGISTER AND LITERAL.
2 SET THE REGISTER TO THE LOGICAL OR OF THE REGISTER AND LITERAL.
3 SET THE REGISTER TO THE LOGICAL EXCLUSIVE OR OF THE REGISTER AND LITERAL.
4 SET THE REGISTER TO THE BINARY SUM MODULO 16 OF THE REGISTER AND LITERAL.
6 SET THE REGISTER TO THE BINARY DIFFERENCE MODULO 16 OF THE REGISTER AND LITERAL.
5 SET THE REGISTER TO THE BINARY SUM MODULO 16 OF THE REGISTER AND LITERAL AND SKIP THE NEXT M-INSTRUCTION IF A CARRY IS PRODUCED.
7 SET THE REGISTER TO THE BINARY DIFFERENCE MODULO 16 OF THE REGISTER AND LITERAL AND SKIP THE NEXT M-INSTRUCTION IF A BORROW IS PRODUCED.

Exceptions:

1) BICN, FLCN, XYCN, XYST and INCN when specified as an operand register are not changed as a result of this operation. However, the carry and borrow outputs are produced and a skip can result.

3.4.23 Bit Test Branch False

FORMAT:

OP CODE 0100	REGISTER GROUP # 0...15	REGISTER SELECT # 0...1	REGISTER BIT # 0...3	DISPLACEMENT SIGN 0-POSITIVE 1-NEGATIVE	DISPLACEMENT VALUE 0...15

Test the designed bit within the specified register and branch relative to the next instruction by the signed displacement value if the bit is zero. If the bit is one, a displacement value of zero is assumed and control passes to the next in-line M-instruction. A displacement value indicates the number of 16-bit words from the next in-line instruction.

3.4.24 Bit Test Branch True

FORMAT:

OP CODE 0101	REGISTER GROUP # 0...15	REGISTER SELECT # 0...1	REGISTER BIT # 0...3	DISPLACEMENT SIGN 0-POSITIVE 1-NEGATIVE	DISPLACEMENT VALUE 0...15

Test the designated bit within the specified register and branch relative to the next instruction by the signed displacement value if the bit is one. If the bit is zero, a displacement value of zero is assumed and control passes to the next in-line M-instruction. A displacement value indicates the number of 16-bit words from the next in-line instruction.

3.4.25 Skip When

FORMAT:

OP CODE 0110	REGISTER GROUP # 0...15	REGISTER SELECT # 0...1	VARIANTS 0...7	MASK 0...15

Test only the bits in the register that are referenced by the "1" bits in the mask ignoring all others unless V=2 or V=6, in which case, compare all bits for an equal condition. Then perform the action as specified below.

V=0 If any of the referenced bits is a "1", skip the next M-instruction.
V=1 If all of the referenced bits are "1", skip the next M-instruction.
V=2 If the register is equal to the mask, skip the next M-instruction.
V=3 Same as V=1, but also clear the referenced bits to zero without affecting the non-referenced bits.
V=4 If any of the referenced bits is a "1", do not skip the next M-instruction.
V=5 If all of the referenced bits are "1" do not skip the next M-instruction.
V=6 If the register is equal to the mask, do not skip the next instruction.
V=7 Same as V=4 but also clear the referenced bits to zero without affecting the non-referenced bits.

Note: If the mask equals 0000 the "ANY" result is false. The skip is not made for V=0 and is made for V=4. If the mask equals 0000, the "all" result is true. The skip is made for V=1 and V=3 and is not made for V=5 and V=7.

Exceptions:

1) BICN, FLCN, XYCN, XYST and INCN cannot be cleared with V=3 or 7. However, they can be tested.

3.4.26 Clear Registers

FORMAT:

OP CODE 0000 0011	REGISTER FLAGS 8-BITS							
	L	T	Y	X	FA	FL	FU	CP

Clear the specified register(s) to zero if the respective flag bit is a one.

3.4.27 Bind

FORMAT:

OP CODE
0000 0000 0000 0100

Move the 24-bit value from the L-Register to the MBR-Register. Move the least significant 4-bits from the T-Register to the TOPM-Register. Move the most significant 20 bits from the T-Register to the A-Register truncating the left most 6 bits of the source.

3.4.28 Overlay M-Memory

FORMAT:

OP CODE
0000 0000 0000 0010

Overlay M-Memory from Main Memory.

The starting M-Memory and starting Main Memory Addresses are taken from register L and register FA respectively. The length of the data overlay in bits is taken from register FL.

The execution of the instruction proceeds as follows:

1. A is moved to TAS, with a stack push.
2. L is moved to A.
3. The first 16 bits are read from main memory and stored in the M-memory. Register FL is decremented and FA and A are incremented.
4. Step three is repeated until FL=0 at which point the process terminates with a move of TAS to A.

3.4.29 Dispatch

FORMAT:

OP CODE	VARIANTS	SKIP VARIANT
0000 0000 0001	000-LOCKOUT 001-WRITE LOW 010-READ 011-READ & CLEAR 100-WRITE HIGH 101-PORT ABSENT	0-SKIP IF ALREADY LOCKED 1-SKIP IF NOT ALREADY LOCKED (Applies only to lockout variant)

The dispatch operation is used to initiate I/O operations and to receive interrupt information from other ports.

Since the interrupt system is shared by all ports, the processor must gain control of the interrupt system by successfully completing a lockout prior to a dispatch write.

The skip variant allows skipping of the next 16-bit instruction based upon success or failure of the lockout attempt.

The write dispatch operation sets the lockout and interrupt flip flops in the port interchange, It also stores the contents of the L register into memory locations 0 through 23 and the contents of the least significant 7 bits of the T register (designating the destination port # and channel # into the appropriate Port Interchange Register. In addition, it sets (write high) or resets (write low) the high interrupt flip flop in the Port Interchange.

The read dispatch operation stores the contents of memory locations 0 through 23 into the L Register and the contents of the Port Interchanges Port-channel register into the least significant 7 bits of the T register. The other 17 bits of the T-register are unaffected.

The read & clear dispatch operation in addition to performing the Read dispatch operation clears the lockout flip flop, the two interrupt flip-flops and the port device absent flip flop in the Port Interchange. It does not clear any memory locations.

The port absent operation is executed by the processor when necessary to return a port absent level signal to another port indicating the absence of the designated channel.

3.4.30 Cassette Control

FORMAT:

OP CODE 0000 0000 0010	VARIANTS 0...7	RESERVED FLAG BIT 0...1

Perform the indicated operation on the tape cassette.

V=0 Start Tape
1 Stop Tape (The processor also halts if it is in tape mode.)
2 Stop Tape if X≠Y (The processor also halts if it is in tape mode.)
3 Reserved
4 Reserved
5 Reserved
6 Stop tape if X=Y (The processor also halts if it is in tape mode.)
7 Reserved

All tape stops variants cause the tape to halt in the next available gap.

3.4.31 Halt

FORMAT:

OP CODE 0000 0000 0000 0001

Stop execution of the micro-instructions. In run mode the next micro to be executed is fetched and stored in the M-Register and the A Register points to the next following micro. In tape mode the next micro is not fetched and stored in the M-Register but the halt micro is left in the M-Reg.

3.4.32 No Operation

FORMAT:

OP CODE 0000 0000 0000 0000

Skip to the next sequential instruction.

3.4.33 Monitor

FORMAT:

OP CODE 0000 1001	VARIANTS 7 6 5 4 3 2 1 0

Skip to the next sequential instruction.

During the time this micro-operator is executing the operator and the last two bits (0 and 1) are decoded, and-ed with the system clock and are present in the backplane as follows:

3.4.33 Monitor (Cont'd.)

MONITOR	0	True for the OP code
MONITOR	00R0	True if last two bits are 00
MONITOR	01R0	True if last two bits are 01
MONITOR	02R0	True if last two bits are 10
MONITOR	03R0	Ture if last two bits are 11

The monitor at the backplane are ½ clock from leading edge of trailing edge.

3.5 CONCURRENT OPERATIONS

In order to achieve maximum utilization of the processor during processor memory cycles, the micro-instructions are classified into two classes -- a concurrent set and a non-concurrent set. The non-concurrent set is that set which must wait until the memory cycle is completed (data has been accepted or released) before proceding with its execution. The concurrent set is that set which can overlap its execution with the memory cycle. The overlap starts with the clock period following ADDRESS ACCEPT and can extend up to including and beyond the time data is ACCEPTED.

For a write operation, the processor presents data during the clock period immediately following address accept and is released for a non-concurrent operation during the very next clock period.

For a read operation, the processor accepts data during the first clock period data is presented and is released for a non-concurrent operation during the clock period immediately following this acceptance.

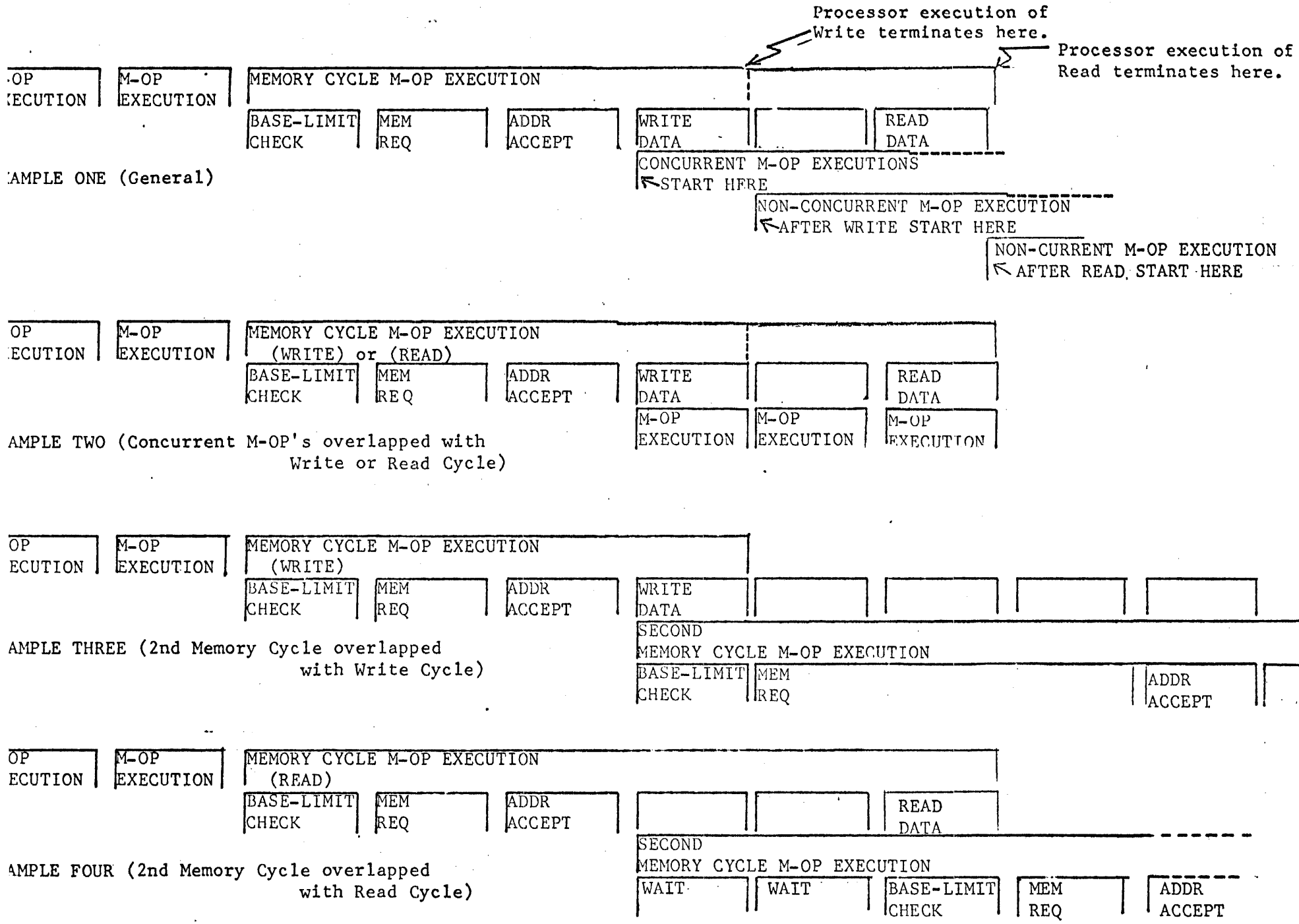
The m-instructions comprising the concurrent set are:

Read Memory*	Count FA/FL**	Scratchpad Relate FA
Write Memory*	BIAS**	Swap F with Doublepad Word*
Swap Memory*	Monitor**	Store F Into Doublepad Word
	Branch**	Store F From Doublepad Word

*A memory cycle operation overlaps with another only during that portion of the cycle comprising the base-limit checking. The actual memory request is made during the clock period following acceptance of data.

** A 1 clock concurrent micro operator and the 2 clock branch micro operator has a 1 clock NOP placed after it by the hardware.

Timing diagram showing execution times for consecutive processor m-instructions are shown below. The diagram assume that the instructions are obtained from M-Memory and that the processor receives the memory cycle immediately after requesting.


Processor execution of Write terminates here.
Processor execution of Read terminates here.
:OP :ECUTION
M-OP EXECUTION
MEMORY CYCLE M-OP EXECUTION
BASE-LIMIT CHECK
MEM REQ
ADDR ACCEPT
WRITE DATA
READ DATA
CONCURRENT M-OP EXECUTIONS START HERE
NON-CONCURRENT M-OP EXECUTION
AFTER WRITE START HERE
NON-CURRENT M-OP EXECUTION
AFTER READ START HERE
:AMPLE ONE (General)
OP ECUTION
M-OP EXECUTION
MEMORY CYCLE M-OP EXECUTION
(WRITE) or (READ)
BASE-LIMIT CHECK
MEM REQ
ADDR ACCEPT
WRITE DATA
READ DATA
M-OP EXECUTION
M-OP EXECUTION
M-OP EXECUTION
AMPLE TWO (Concurrent M-OP's overlapped with Write or Read Cycle)
OP ECUTION
M-OP EXECUTION
MEMORY CYCLE M-OP EXECUTION
(WRITE)
BASE-LIMIT CHECK
MEM REQ
ADDR ACCEPT
WRITE DATA
SECOND MEMORY CYCLE M-OP EXECUTION
BASE-LIMIT CHECK
MEM REQ
ADDR ACCEPT
AMPLE THREE (2nd Memory Cycle overlapped with Write Cycle)
OP ECUTION
M-OP EXECUTION
MEMORY CYCLE M-OP EXECUTION
(READ)
BASE-LIMIT CHECK
MEM REQ
ADDR ACCEPT
READ DATA
SECOND MEMORY CYCLE M-OP EXECUTION
WAIT
WAIT
BASE-LIMIT CHECK
MEM REQ
ADDR ACCEPT
AMPLE FOUR (2nd Memory Cycle overlapped with Read Cycle)

3.6 M-INSTRUCTION TIMING

The following instruction times are given for the case where the next m-instruction is contained in the M-Memory. In general, an additional five clocks are added to the basic time if the m-instruction is fetched from S-Memory.

Register Move

SINK→ / SOURCE↓	TOPM A	MSM	DATA CMND	MBR WITH A OUT OF BOUNDS	M WITH A OUT OF BOUNDS	OTHERS
MSM, SUM, DIFF	3	3	4	3	6	2
DATA	4	4	-	4	-	3
U	u+1	u+2	u+2	u+1	-	u
OTHERS	2	2	3	2	6	1

M-Instruction	Clocks
Scratchpad Move	1*
(MSM, SUM, DIFF as source)	2
(DATA as source)	3
(U as source)	u
(MSM, TOPM, A as destination)	2*
(DATA, CMND as destination)	3*
(MBR as destination and A out-of-bounds)	2*
(M as destination and A out-of-bounds)	6
*Add one additional clock if previous OP was write into scratchpad	
Swap F with Doublepad Word	1
Store F into Doublepad Word	1
Load F from Doublepad Word	1
Move 8-bit Literal	1
(A, MSM as destination)	2
(M as destination and A out-of-bounds)	6
Move 24-bit Literal	3
(MSM as destination)	4
(MSM, TAS as destination and A out-of bounds)	8
(OTHERS as destination and A out-of-bounds)	7
(TAPE MODE)	u+1
Swap Memory	
(Followed by Non-concurrent M-OP)	10
(Followed by Memory Cycle)	9
(Followed by 7 concurrent M-OP's)	3
Write Memory	
(Followed by non-concurrent M-OP)	4
(Followed by Memory cycle)	5
(Followed by 1 concurrent M-OP)	3
(If outside base-limit & inhibited)	1

3.6 Cont'd.

M-Instruction	Clocks
Read Memory	
(Followed by non-concurrent M-OP)	6
(Followed by Memory cycle)	5
(Followed by 3 concurrent M-OP's)	3
Dispatch Lockout	Same as Read Memory plus 1
(Skip taken)	Same as Read Memory plus 2
Dispatch Write	Same as Write Memory
Dispatch Read	Same as Read Memory plus 1
Dispatch Read & Clear	Same as Read Memory plus 1
Dispatch Port Absent	1
Count FA/FL	1
Scratchpad Relate FA	2
Extract from Register T	1
Shift/Rotate Register T Left	1
(A, TOPM, MSM as destinations)	2
(DATA, CMND as destinations)	3
(MBR and A out-of-bounds)	2
(M and A out-of-bounds)	6
Shift/Rotate Register X/Y L/R	1 plus S/R count
Shift/Rotate Register XY L/R	1 plus S/R cound
Normalize	1 plus # of bits shifted
Read/Write MSM	6
Call	2
Branch	2
Bias	1
(Skip taken)	2
Set CYF	1
4-bit Manipulate	1
(Skip taken)	2
(BICN, FLCN, XYNC, XYST)	2
(BICN, FLCN, XYCN, XYST & SKIP taken)	3
Bit Test Branch False	1
(Branch taken)	2
Bit Test Branch True	1
(Branch taken)	2
Skip When	1
(Skip taken)	2
(BICN, FLCN, XYCN, XYST)	2
(BICN, FLCN, XYCN, XYST & SKIP taken)	3
Clear Registers	1
Bind	3
Overlay M-Memory	4+(6)(# of words moved)
(FL=0 initially)	1
Cassette Control	1
Halt	1
No operation	1
Monitor	1