bcc	title	prefix/class-number.revision
	DATA COMMUNICATIONS COMPUTER	BCCDCC/S-32

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ABSTRACT and CONTENTS

Addressing conventions and control procedures are described for the Multiplexer section of the DCC.

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A. GENERAL

The Multiplexer section of the Data Communications Computer (DCC) is generally equivalent to the CHIO multiplexer (MPX) (see Document NCHIO/S-17). Control is provided for up to 128 high speed devices and up to 512 low speed data sets or local teletypes. Special devices are addressed as high speed devices and include the Scanner, a Real-Time Clock, a Time-Out Clock, and a Dialer Controller. The basic clock cycle in the DCC is 140 nanoseconds, with the Scanner running at half the basic clock rate. The Real-Time and Time-Out Clocks are eight-bit counters running from a local, asynchronous, 10-microsecond period oscillator. Addressing any device (or device group) results in a dump of data bits to the E2 bus. The data will remain on the E2-bus until the end of a POT or a PIN command. Data is output to an addressed device by an ALERT Command followed with a POT Command. Flags are cleared in a device by an ALERT followed by a PIN. The control and data assignments of the E2- and Z-bus bits are detailed below for each device.

B. ADDRESSING

Bits Z(8) thru Z(15) comprise the address word. This eight-bit group is divided into three fields (E, F, and G) of three, two, and three bits respectively. Address block assignments are shown in Table 1.

Table 1. Address Block Assignments.

Address	E	F	G	Device
000B - 177B	0-3	0-3	0-7	Bit Scanned (BS) Devices
200B - 377B	4-7	0-3	0-7	Character Assembled (CA) Devices
374B	7	3	4	Dialer Controller
375B	7	3	5	Time-Out Clock
376B	7	3	6	Real-Time Clock
377B	7	3	7	Scanner

C. DEVICE INTERMIX.

There are three strictures on device intermix flexibility: programming limitations, the card space available in the BCCDCCMPX card cage, and the intermix modulus of the modem racks. Allowed intermixes are shown in Table 2.

NOTE

The high speed modems to the M500 and to the neighboring DCC are controlled by one card in a group of five overhead cards.

Table 2. Device Intermix.

BS Devices *	224	192	160	128	96	64	32	0
CA Devices	0	8	16	24	32	40	48	56
Total Devices	224	200	176	152	128	104	80	56

* When the modem rack is implemented with Vadic Data Sets, the number of BS Modems is limited to 112 minus twice the number of CA Modems. BS devices in excess of this number must be hardwired local terminals.

D. DEVICE DETAILS

1. Bit Scanned Devices.

The prototypical BS device is the Bell 103A2 Data Set which provides full-duplex operation at a 300-baud rate. Substitution of equivalent modems is probable in which case access to the telephone lines by these 'foreign attachments' must be via the Bell F58118 Data Access Units, not now tariffed in California.

a. Addressing. BS devices are addressed as 32 groups of sixteen devices each. Within the group of sixteen devices, one of four functions is addressed by the E-field. Bit Z(8) must be zero for BS devices. Function assignments are shown in Table 3.

Table 3. Function Assignments.

E	Receiver Function/Transmitter Function
Ø	RD/TD; Received Data/Transmit Data
1	RI/BO; Ring Indicator/Busy Out
2	DSR/DTR; Data Set Ready/Data Terminal Ready
3	CTS/--; Clear to Send/ (unused)

NOTE

The Bell 103A2 does not accept a Busy Out command and as the Carrier Detector signal provided is redundant with Clear-to-Send, it is not used.

b. Answering a Call. BS device controllers set no flags so the status of the RI lines in each group must be cyclically sampled by addressing E1 in each group. When a call is coming in, the RI line will typically be ON for two seconds then OFF for four seconds. The response to RI for a device is DTR. In setting DTR for one device, the status of the other 15 DTR lines in that group must be copied again into the output latches to preserve the status of each device. After a delay during which the telephone equipment reacts to DTR (which appears as an OFF-HOOK signal on the phone lines), the local modem sets DSR and initiates a handshake procedure with the remote (calling) modem. This time interval ranges from 2.5 to 5 seconds. If the handshake is successful, the modems are ready for data exchange and the local modem sets CTS. An abort timer between DSR and CTS should be used to terminate unsuccessful calls (wrong numbers, calls disconnected by the exchange, calls discontinued by the originator) by dropping DTR for at least 50 milliseconds. A modem may be made unresponsive to incoming calls by setting BO which appears on the line as an OFF-HOOK or BUSY signal.

c. Originating a Call. At the end of the dialing sequence, detailed below, the Dialer puts the associated modem into the OFF-HOOK state and reconnects the telephone line (via the Data Access Unit, DAU) to the

modem. DTR must be ON at this time. The answering modem initiates the handshake procedure to which the calling modem responds with DSR followed approximately two seconds later by CTS. Abort timing between presentation of the End-of Number code to the Dialer and CTS from the modem should be adjusted to local conditions. A lapse of 30 seconds is not uncommon.

d. Terminating a Call. Calls may be terminated from either end by dropping DTR for 50 milliseconds or until DSR goes OFF. The other set should respond to the loss of CTS by dropping DTR. For a discussion of optional manual and LONG SPACE disconnect routines available with the 103A2 Data Set, refer to the Bell System Data Communications Technical Reference of February, 1967, titled DATA SET 103A INTERFACE SPECIFICATION.

2. Character Assembled Devices.

The basic scheme for CA devices is given in NCHIO/S-17. The instruction sequence for input is:

Device Address → Z, ALERT

TE2Y, Y → Internal Register, VCY, PIN

If the receiver flags are to be cleared when data is gated to the E2-bus, the instruction sequence is:

1B5 + Device Address → Z, ALERT

TE2Y, Y → internal register, VCY, PIN

The flags cleared by PIN·Z(Ø)=1 are Receiver Error, bit

E2(7), and Receiver Buffer Full, not output to E2. The 16 bits on the E2-bus are assigned as shown in Table 4.

Table 4. E2-bus Assignments.

E2(Ø)	PIN·Z(Ø)=1	Flags Cleared in Receiver
E2(1)	CD	Carrier Detector
E2(2)	CTS	Clear-to-Send
E2(3)	DSR	Data Set Ready
E2(4)	TRQ	Transmitter Request
E2(5)	TER	Transmitter Error
E2(6)	RRQ	Receiver Request
E2(7)	RER	Receiver Error
E2(8-15)	RD	Received Data Word

The instruction sequence for output is:

Device Address → Z,ALERT

Output Word → Z,POT

The 16 bits on the Z-bus are assigned as shown in Table 5.

Table 5. Z-bus Assignments.

Z(Ø)	--	Not used
Z(1)	--	Not used
Z(2)	RTS	Request-to-Send
Z(3)	--	Not used
Z(4)	LDL	Load Data Latch
Z(5)	TON	Transmitter On
Z(6)	RON	Receiver On
Z(7)	LCL	Load Control Latch
Z(8-15)	TD	Transmitted Data Word

Bit 4 must be set for the transmitter to accept a data word (Bits 8-15) for transmission. Bit 7 must be set to change the status of the control lines (bits 2, 5, and 6). It is legal to set both bit 4 and bit 7 for the same POT command.

3. Scanner.

The Scanner runs at half the basic rate of the DCC, searching for flags put up by CA modems indicating requests to transmit or receive (i.e. empty transmitter buffers or full receiver buffers). When the Scanner stops, it sets ATTENTION LATCH 2. If the Scanner has stopped on a high priority request (from a receiver with its buffer full and four or more bits of the next received word in the shift register) ATTENTION LATCH 3 is also set. Addressing the Scanner with the sequence:

Scanner Address (377B) → Z, ALERT

gates the bits to the E2-bus as shown in Table 6.

Table 6. Scanner Bits Gated to E2-bus.

E2(Ø)	TREQ	Transmitter Request
E2(1)	RREQ	Receiver Request
E2(2)	ERR	Transmitter or Receiver Error
E2(3)-(7)	--	Not used
E2(8)-(15)	SCPT	Stop Address

The Scanner is a seven-bit counter to address 128 CA devices (including itself and other non-modems). An

eighth bit, always set, is gated to E2(8) so that E2(8) thru E2(15) is the actual address of the device requesting service. The following instruction sequence restarts the Scanner.

```
1B5 + Scanner Address → Z, ALERT
VCY, PIN
```

This is the usual command sequence to the Scanner. If Z(Ø) is not set in the address word, the Scanner will not restart. A PIN must follow ALERT to clear the E2-bus whether or not Z(Ø) is set.

4. Real-Time Clock.

A local oscillator with a 10-microsecond period is counted by the eight-bit Real-Time Clock. The clock bits are gated to the lower half of the E2-bus by addressing the clock:

```
Real-Time Clock address (376B) → Z, ALERT
NOP
TE2Y, Y → internal register, VCY, PIN
```

Input pulses to the clock, synchronized to the K2 clock, are inhibited while the clock is addressed from ALERT until the end of the succeeding PIN or POT. The NOP allows the clock, a ripple counter, to stabilize before the data on E2 is swallowed by the Processor. The Real-Time Clock may be reset by addressing it, then doing POT. No data is accepted from the Z-bus.

5. Time-Out Clock.

Operating from the same oscillator as the Real-Time Clock is an eight-bit Time-Out Clock. The result of the sequence:

Time-Out Clock address (375B) → Z, ALERT

Output Word → Z, POT

is to load the clock with the complement of the output word from Z(8) - Z(15). The clock then counts to 377B and sets ATTENTION LATCH 3. The Time-Out Clock runs continually, setting ATTENTION LATCH 3 every 2.56 millisecond following the time interval set at the last POT. Addressing either clock inhibits the synchronized input pulses from the 10-microsecond oscillator to both the Time-Out Clock and the Real-Time Clock.

6. Dialer.

The Vadic dialer is generally similar to the Bell 801A4 Automatic Calling Unit with the following exceptions:

a. The dialer will accept a seven-bit line address.

b. There is no self-contained abort timer.

c. Dial-out is not blind but is only possible following receipt of dial tone on the selected line.

d. The control lines (PW1, Power Indication; DSS, Data Set Status; ACR, Abandon Call and Re-

try) available with the Bell unit, are not used in the Vadic System. The status of the Dialer is sampled by:

Dialer Address (374B) → Z, ALERT

TE2Y, Y → internal register, VCY, PIN

The Dialer is controlled by:

Dialer Address → Z, ALERT

Output Word → Z, POT

Bit assignments for the Z-bus and the E2-bus are shown in Table 7.

Table 7. Dialer Bit Assignments.

Bit	Z-bus	E2-bus	FUNCTION
Ø	LAØ		Line Address Bit Ø
1	LA1		Line Address Bit 1
2	LA2		Line Address Bit 2
3	LA3		Line Address Bit 3
4	LA4		Line Address Bit 4
5	LA5		Line Address Bit 5
6	LA6		Line Address Bit 6
7	---	---	Not used
8	APR	APR	Address Present
9	CRQ	CRQ	Call Request
10	NB8	---	BCD Digit, Weight 8/ not used
11	NB4	ARQ	BCD Digit, Weight 4/ Address Request
12	NB2	DLO	BCD Digit, Weight 2/ Data Line Occupied

Table 7. Dialer Bit Assignments. (cont'd)

Bit	Z-bus	E2-bus	FUNCTION
13	NB1	---	BCD Digit, Weight 1/ Not Used
14	DPR	DPR	Digit Present
15	---	PND	Not used/ Present Next Digit

APR (Z8) must be set to load the line address latch (ZØ-Z6). DPR (Z14) must be set to load the digit latch (Z1Ø-Z13). Any POT to the Dialer reloads the control latch (Z8, Z9, and Z14).

The dialing sequence is initiated by setting CRQ. APR and LAØ - LA6 may be set simultaneously with CRQ. The Dialer responds with ARQ and accepts the line address. The line is tested and if already occupied (OFF HOOK), DLO is set. If the line is not occupied, blind dialing begins after a five second delay, signified by setting PND. PND from the Dialer should be used to set DPR (conveniently via LCY1), along with the digit to be dialed (encoded on NB1 thru NB8). When the Dialer has dialed the last pulse of the digit, PND goes off. DPR is then cleared by hardware. After a wait of 600 milliseconds, PND again comes ON indicating that the Dialer is ready for the next digit. The response is to put up DPR and the next NB1 - NB8. This cycle continues until the complete number has been dialed.

When PND comes ON after the last digit has been dialed, NB1 - NB8 should be loaded with the End-of-Number code, 1100 (14B). No dial pulses are generated by the code but a control signal is sent to, and latched by, the data set to hold it in the OFF-HOOK state, and the telephone line is transferred from the Dialer back to the data set.

NOTE

DTR must be ON for the data set.

When PND goes OFF following acceptance of the EON code; CRQ and APR should be cleared to conclude the dial-out sequence.

Note that data gated to the E2-bus contains not only the ARQ, DLO, and PND signals from the Dialer, but also copies of signals APR, CRQ, and DPR to the Dialer.

If a line has been reserved by setting BO for the associated modem, dial out must begin by clearing BO, then waiting a few seconds for the exchange to respond before setting CRQ.