class - number revision	prefix	title	author(s)	remarks
M-4.4	MICPU	Model I CPU Reference Manual	Butler Lampson Charles Simonyi	
M-5	CMI	Central Memory Interface	Charles P. Thacker	Obsolete
M-6	ICSEM	IC & Semiconductor Manual	Uli Spannagel	Not in originals
M-7	MISPS	MCALLs on the Model I Sub-Process System	Jack Freeman	
M-8	MICRO	MICRO Reference and User Manual	Bo Lewendal	
M-9	ROMT	ROM TESTER Description and Operation	Larry Sweeney	
M-10	PREP	Phase One Preprocessor Interface	Rick Dove	
M-11	UPREP	Phase One Unpreprocessor Interface	Rick Dove	
M-12	CSED	MICS Phase One Language Editor	L. Peter Deutsch R. K. Dove	Missing from originals
M-13	PIG	Interactive Microprocessor Simulator	Paul Heckel	
M-14.1	CPUPG	CPU Programmers Guide	Charles Simonyi	
M-15	AKOCS	Character Sets	Paul Heckel	
M-16	PTES	Paper Tape Reading and Punching	Paul Heckel	
M-17	PCNR	CHIO Phase 1 Test Routines	Paul Heckel	

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M-18.1	M3OT	Model 30 Trivia	Henry Thompson	
M-19	PMS	Process Memory System	Jack Freeman	
M-20	DCODT	DCODT Reference Manual	Butler Lampson	
M-21	RPASS	Remote Processor Assembler	Paul Heckel	
M-22	WL	Wire Listing	Al Goodrich	
R-1	RIICTD	Methods for Reliability Improvement of Integrated Circuits, Transistors, and Diodes	L. Sweeny	
R-2	TRGEN	M1CS Phase One Tree Generator	L. Peter Deutsch R. K. Dove	
R-3	SPLGR	SPL Grammar and Precedence	Butler W. Lampson	
R-4	OPREC	Support Software for Operator Precedence Parsing	B. W. Lampson	
R-5	GELAI	GE Lexical Analyzer Implementation	R. K. Dove	
R-6	GEPARS	GE Parser Implementation	R. K. Dove	Missing from original
R-7	GESYMB	GE Symbol Implementation	R. K. Dove	Missing from original
R-8	GEFEQV	GE FORTRAN Equivalence Algorithm	R. K. Dove	
S-1	CHIOM	Phase 1 Character I/O Interface Specification	Charles P. Thacker	
S-2.1	FOO	CHIO/CPU Interface	P. Heckel	

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S-3.1	SCCP	System Control, Clocks and Power	S. Dinsmore	
S-4	PMAP	Physical Map Specifications	Charles P. Thacker	
S-4.1	PIPM	The Phase 1 Physical Map	Chuck Thacker	
S-5	empty	empty	empty	
S-6	----	Model I Layout & System Structures	B. Brinker	Lost and was never finished
S-7	M30	Communications with the IBM Model 30	Henry Thompson	
S-8.3	SR	System Registers	Stan Dinsmore	
S-9	PCPW	Workmanship Methods for PC Boards	R. Lawson	Obsolete
S-10	BCCPU1	Special and Branch Conditions in CPU1	Charles Simonyi	Obsolete
S-11	MEMS	Microprocessor Expanded Memory Specification	Chuck Thacker	
S-12	MPMBM	Description & Operation of the MPMBM & Protect Logic	Chuch Thacker	Missing from originals
S-13.1	SFBCM	Special Functions and Branch Conditions in the Standard Microprocessor	Don Dodge	
S-14	MPPC	Micro-Processor Parity Checking Logic	Chuck Thacker	
S-15.1	MSIOI	Micro-Scheduler Input/Output Interface	Chuck Thacker	

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S-16	MPPI	Microprocessor Pot/Pin Interface	Charles Thacker	
S-17.1	NCHIO	CHIO Multiplexer Specification	Chuck Thacker	
S-18	CMPC	Core Module Parity Checkout	S. Tulloh	Not in originals
S-19	M3ØIS	Model 3Ø Interface Specification	Max Marutani	
S-20	ROMBA	Read Only Memory Bit Assignment	Don Dodge	
S-21	PIF	Specification of Program Image Files	Larry Barnes L. Peter Deutsch	
S-22	COMCON	Command Writing Conventions	Larry Barnes	
S-23	RC	The Remote Concentrator Design	Paul Heckel	
S-24	CS	The Communications System - Phase II	Paul Heckel	
S- 25	INITT	System Initialization Tape	Henry Thompson	
S-26	DKBK	Disk Backup Subsystem	Bo Lewendal	
S-27	TEXTF	M1 Text File Standard	L. Peter Deutsch	
S-28	SFBCDC	Special Functions and Branch Conditions in the Data Communications Computer	Warren Powell	
S-29	DCCROM	Data Communications Computer ROM Bit Assignment	Warren Powell	
S-30	MULT	Phase 1.5 CPU Multiplier	Norm Cohler	

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S-31	SFBCPA	Special Functions, Branch Conditions and Pseudo Scratch-pad Address in Phase 1.5 CPU	Norm Cohler	
S-32	BCCDCC	Data Communications Computer	L. Sweeney	
S-33	RPU	Remote Processor Unit	P. Heckel	
S-34	P1.5PM	Phase L.5 Physical Map	A. Spannagel	
S-35	MMS	Memory Management System	Butler Lampson	
S-36	FSOD	Format of System Owner's DAEL	C. Wilford	
T-1.2	PCS	Procurement Standards for Printed Circuit Boards	Chuck Thacker Al Murdock	Not in originals
T-2	CCAS	Cable Card Assembly Method	Charles P. Thacker	
T-3	PCBW	Workmanship Methods for P.C. Boards	Dick Lawson	
T-4	unknown	unknown	unknown	
T-5	SSE	Standard for Syntax Equations	Larry Barnes	
T-6	TLB	Testing Large Boards	R. Saunders	Not in originals
T-7.1	TC	Transistor Circuits	Norm Cohler	
T-8.2	TPPSLC	Test Procedure Unit Power Supplies and Unit Local Control Boards	Stanley H. Dinsmore	
T-9	PCBWR	PC Board and Backboard Wiring Rules	Norman R. Cohler	

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T-10	TTP	Transistor Test Procedures	U. Spannagel	Missing from originals
T-11	DTP	Diode Test Procedures	U. Spannagel	Missing fron originals
T-12	IIP	Incoming Inspection Procedures	Jesse T. Quatse	
T-13.1	PCFI	PC Board Final Inspection Procedure	Jesse T. Quatse	
T-14	PTDP	Painting, Technical Data and Procedure	Thurman Philpot	
W-1	MM1	Memory Management	R. R. Van Tuyl	
W-2	PMTSPT	MCALLs for Manipulating PMT and SPT	Jack Freeman	
W-3.1	TPDDT	Test Processor DDT	R. R. Van Tuyl	
Special version of R-11, a document of Project GENIE at UC, Berkeley.				
W-4	FNS	System I File-Naming System	Larry L. Barnes	
W-5	CWS	The Core Working Set	Jack Freeman	
W-6	CMP	The Command Processor	Larry L. Barnes	
W-7.1	AUD	The Account and User Directories	Larry L. Barnes	
W-8	PRUN	Running a Process	Butler W. Lampson	
W-9	SCBFS	System Calls to the Basic File System	Rainer Schulz	
W-10	MIFS	Model I File System	Rainer Schulz	

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W-11.1	IWS	Interrupt and Wake-up System	Rainer Schulz	
W-12	CSED	Preliminary Description of Compiler System Editor	L. Peter Deutsch	
W-13	SPLDS	SPL Command Language and Debugging System	M. Greeberg	Obsolete
W-14	USI	Micro-Scheduler Implementation	Butler W. Lampson	
W-15.1	SYSP	System Parameters	Rainer Schulz	
W-16	SPLAL	Facilities for Allocation in SPL	Butler W. Lampson	
W-17	SPLDS	SPL Command Language and Debugging System	M. Greenberg Roger Sturgeon	
W-18.2	MPAP	Microprocessor Acceptance Procedure	J. Quatse	
W-19	SINIT	System Initialization and Error Recovery	Larry L. Barnes	
W-20	CPUINT	CPU Interruptability	Butler W. Lampson	
W-21	SPLEP	SPL Conventions for System - Defined Entry Points	Butler W. Lampson	
W-22	ITPEX	External Interfaces for the Integrated Test Processor	Butler W. Lampson	
W-23	ITPRM	Integral Test Processor Reference Manual	Butler W. Lampson	
W-24	DFMS	Brief Description of Fast Memory Simulator	Max Marutani	

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W-25	SPLAPF	Allocation and Program Format in SPL	Butler W. Lampson	
W-26	UTENT	The Utility Enter Dialog	Larry Barnes	
W-27	BSRA	Basic System Resource Allocation	Butler W. Lampson	
W-28	MCHIO	CHIO Functions in Basic System	Rainer Schulz	
W-29	SSIN	Software System Initialization	Rainer Schulz	
W-30	MPREC	Microprocessor Crash Procedures Initialization and Breakpoints	Butler W. Lampson	
W-31	CIOSUC	Control Input/Output Streams	Larry Barnes	
W-32	SPLEX	SPL Executive Commands	L. Peter Deutsch	
W-33	SPCAP	Sub-process Capabilities	Larry Barnes	
W-34	MNODT	MNODT	Charles Thacker	
W-35.1	PTPP	Procedures for TP Programs	R. R. Van Tuyl	
W-36	PROC	Processes	Rainer Schulz	
W-37	ATONFIC	An Efficient Multiplexing Algorithm	Raul Heckel	
W-38	IHTWD	CHIO Implementation Phase 1	Paul Heckel	
W-39	DITP	ITP Diagnostic Program	Butler W. Lampson	
W-40	FAROUT	An Error-Free Communications Line	Paul Heckel	

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W-41	OHWOW	Local Echoing in the Communications System	Paul Heckel	
W-43	DBAMC	Microprocessor Debugger for the AMC	R. R. Van Tuyl	
W-44	MPT	Microprocessor Test Program	Dieter A. Susset	
W-45	TSTX	CPU Test Programs	Charles Simonyi	
W-46	SDDTCOM	SYSDDT Commands	Peter Deutsch	
W-47	APUD	APU Diagnostic Program	B. Lampson	
W-48	PM	Profile Maintenance	J. Ford	
W-49	P2CSS	Software for the Phase 2 Communication System	P. Heckel	
W-50	TM	Terminal Management	J. Ford	