IFIP CONGRESS 65

Title   IPL-VC, AN IPL-V HARDWARE COMPUTER

Author   Donald Hodges
Applied Mathematics Division
Argonne National Laboratory
9700 South Cass Avenue
Argonne, Illinois   60440

Language of Summary   English

Statement of Work   An IPL-V hardware processor, Engine No. 2, has been
added to the CDC-3600, thereby converting the system
into the IPL-VC, an IPL-V hardware computer. This
paper presents a discussion of the completed system.

IPL-VC, AN IPL-V HARDWARE COMPUTER*

There exists a List Processing Language IPL-V (Ref. 1) which up to the present time has always been "interpreted" on other computers rather than hardware-implemented. A second Processor (called Engine No. 2) for the Laboratory CDC-3600 computer has been built to convert the CDC-3600 into an IPL-VC system.

"Shaw, et al." have described a possible hardware computer called IPL-VI which shows the important features such a machine should have for its IPL-V instructions, but the input/output and arithmetic instructions are not considered (Ref. 2). However, with the arrival of the present-day module concept of arithmetic computer organization, a new possibility arises for the construction of an IPL-V hardware machine. An arithmetical computer can be converted into an IPL-V system by providing it with a second processor which operates with certain basic IPL-V "J" processes as its instruction set. This second processor has direct access to memory for its data and instructions in order to operate as fast as the memory allows. The instruction set of this second processor consists of all the basic list operations. The remaining list operations are built up as routines from these basic operations. All of the arithmetic and input/output processes are performed in the original arithmetic processor, with the list processor taking care of any necessary list "book-keeping." The necessary data and addresses are communicated between the two processors by prelegislation of memory locations where the processors will find the relevant information when requested to perform a particular operation. Thus, there has to be some means of transferring control back and forth between the two processors, namely the interrupt system. IPL-V instructions are executed in one of three ways, each comprising approximately one-third of the

---

total IPL-V instruction set. One-third are directly executed in Engine No. 2, a second one-third are executed as subroutines in terms of the instructions executed in Engine No. 2, and the last one-third are those executed in the CDC-3600 Processor.

The advantages of such an approach to an IPL-V hardware system over building a completely new system are as follows:

1. The existence of a large fast memory as provided with present day large arithmetic computer systems.

2. The arithmetic and input/output facilities are both immediately available and as fast as possible. Also, the wealth of input/output devices on a modern large arithmetic computer installation is much greater than could ever be justified for an IPL-V computer itself.

3. The availability of an IPL-V simulator program on the original computer. The actual IPL-VC system will presumably not contain all the excellent tracing, dumping, and snapshot procedures which are available in the simulator and which are so useful for program debugging.

4. The tremendous economical advantage of only having to build a fairly simple list processor instead of a complete computer.

In order for the IPL-VC system to have universal use, it should use as its input the program cards identical to those used for input to present-day IPL-V simulators as specified in the IPL-V reference manual (Ref. 1). This has required the writing of a new assembler to set up the program in storage in a suitable manner for the IPL-VC system to be able to execute it.

The construction of Engine No. 2 utilizes the same printed circuit boards that are used to construct the CDC-3600. The total printed circuit board count is slightly over 800, and it is interesting to note that it takes about this

same amount of logic to control a 100-cpm card punch on the CDC-3600. An increase in operating speed and the ability of Engine No. 2 to directly address all the 64K of memory are the main advantages of the IPL-VC system. While the actual speed advantage over the CDC-3600 interpretive program has not yet been measured, it is known to be greater than ten. References 3 and 4 describe the original proposals for Engine No. 2.

References

1. Information Processing Language-V Manual, editor A. Newell (et al.), Prentice Hall, Inc.

2. A Command Structure for Complex Information Processing, J. Shaw, A. Newell, H. A. Simon, and T. O. Ellis, Proc. Western Joint Computer Conference, 1958.

3. IPL-VC, A Proposal for a Computer System Having the IPL-V Instruction Set, Argonne National Laboratory AMD Technical Memorandum No. 66, January 1964, Donald Hodges.

4. IPL-VC, A Computer System Having the IPL-V Instruction Set, Argonne National Laboratory Report No. 6888, June 1964, Donald Hodges.