MAINTENANCE MANUAL LSI SIDEWINDER®

ARCHIVE
CORPORATION

SIDEWINDER®

(LSI VERSION)

1/4" Streaming Cartridge Tape Drive

MAINTENANCE MANUAL

Part Number 20288-001

September 1984

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual contains maintenance information for the LSI Sidewinder Intelligent Streaming Cartridge Tape Drive (Figure 1-1). This manual applies to the models identified in table 1-1. Included in this manual are physical descriptions, specifications, theory of operation, maintenance procedures and parts list.

Table 1-1 Equipment Model Identification

MODEL	PART NUMBER	TAPE FORMAT
3020L-1	20240-XXX	QIC-11
3020L-2	20523-XXX	QIC-11/QIC-24
9020L-1	20241-XXX	QIC-11
9020L-2	20524-XXX	QIC-11/QIC-24
9045L-1	20242-XXX	QIC-11
9045L-2	20525-XXX	QIC-11/QIC-24

1.2 RELATED DOCUMENTS

- LSI Sidewinder Product Description, Part Number 20442-001.
- Procedures for Incoming Inspection, Part Number 20414-001A.

1.3 PHYSICAL DESCRIPTION

The LSI Sidewinder Intelligent Drive is designed to be easily installed in the eight inch floppy disk mounting space. It consists of two major assemblies; main frame assembly and electronics PCB assembly, which are attached to a mounting frame. The LSI Sidewinder utilizes a 1/4-inch cartridge tape to record data supplied by the host system.

1.3.1 Main Frame Assembly

The main frame assembly consists of the magnetic recording head assembly, capstain drive motor, tape hole sensors, and the cartridge in place and safe sensing switches. The basic drive may be equipped with an optional front panel.

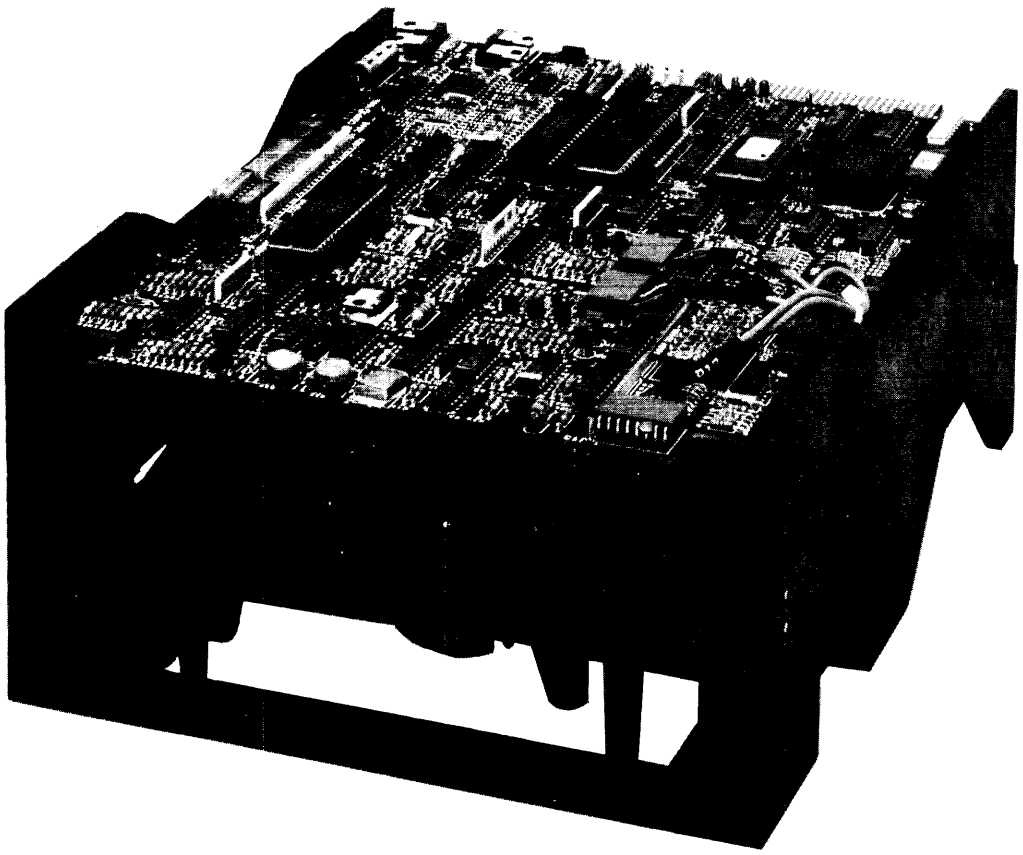


Figure 1-1 Sidewinder 1/4-Inch Cartridge Streaming Tape Drive

1.3.2 Electronic PCB Assembly

The electronic PCB assembly contains independent read and write channels, buffer memories, QIC-02 host interface, drive interface and two microcomputers. Large scale integration (LSI) is employed extensively in the electronics PCB assembly. The microcomputers make tape formatting, tape error processing, tape positioning, and tape motion control invisible to the host system. In addition, statistical error data to monitor progressive deterioration of the tape system, caused by bad tape and/or marginal components is provided by the microcomputers. Data, commands and status information between the host and the electronics PCB are transmitted via the industry standard QIC-02 interface.

1.3.3 Tape Cartridge

A 1/4-inch wide tape, contained in a cartridge, is used as the storage media. The cartridge is described mechanically by ANSI Standard X 3.55 — 1982. The Sidewinder uses the DC300XL (450 feet long) or the DC600A (600 feet long) 1/4-inch tape cartridge.

Different write currents are required for the two cartridges, due to the difference in oxide coating thickness and coercivity. The drive automatically determines the cartridge type by measuring the distance between the BOT and load point holes (3 feet for DC300XL and 4 feet for DC600A) and selects the appropriate write current for the type of cartridge inserted.

1.4 EQUIPMENT SPECIFICATIONS

The performance, environmental, power and physical specifications of the equipment are listed in tables 1-2 through 1-5.

Table 1-2 Performance Specification Summary

Model	3020L	9020L	9045L
No. of Tracks	4	4	9
No. of Channels*	2	2	2
Capacity DC300XL	20 MB	20 MB	45 MB
Capacity DC600A	26.7 MB	26.7 MB	60 MB
Backup Time DC300XL	12 MIN.	4 MIN.	9 MIN.
Backup Time DC600A	16 MIN.	5.2 MIN.	12 MIN.
Recording Mode	NRZI	NRZI	NRZI
Encoding Method	4 to 5 RLL	4 to 5 RLL	4 to 5 RLL
Recording Density	8000 BPI	8000 BPI	8000 BPI
Flux Density	10,000 FCI	10,000 FCI	10,000 FCI
Track Capacity DC300XL	5.0 MB	5.0 MB	5.0 MB
Track Capacity DC600A	6.6 MB	6.6 MB	6.6 MB
Data Transfer Rate	28.9 K Bytes/sec	86.7 Bytes/sec	86.7 Bytes/sec
Tape Speed	30 IPS	90 IPS	90 IPS
Start/Stop Time	100 MS (max.)	300 MS (max.)	300 MS (max.)

*Channel is defined as one write head gap followed by one read head gap

Table 1-3 Environmental Requirements

Characteristic	Operational	Non-Operational
Temperature	+5 to +45°C (+41 to +113°F)	−30 to +60°C (−22 to +140°F)
Relative Humidity	20 to 80% (non-condensing)	0 to 99% (non-condensing)
Thermal Gradient	1 C/min (33.8°F/HR)	
Altitude	−1,000 ft to 15,000 ft	−1,000 ft to 50,000 ft
Shock	2.5g max (1/2 sine wave 11 msec duration on any axis)	50g max (1/2 sine wave 11 msec duration on any axis)
Vibration	0.005 inch max peak to peak displacement 0 to 63 Hz, 1g peak max. acceleration 63 to 500 Hz	0.1 inch max peak to peak displacement, 0 to 17 Hz, 1.5g peak max. acceleration 17 to 500 Hz
ESD	4KV max	

Table 1-4 Power Specifications

DC Voltage	Tolerance	Current	Max Ripple (P-P)
+24 VDC	±10% (including ripple)	1.7A Maximum (operational) 0.8A Nominal (Operational) 2.5A Surge*	500 Millivolts
+5 VDC	±5% (including ripple)	2.7A Maximum	100 Millivolts

*Up to 300 Milliseconds

Note: The surge time may be longer if the cartridge is defective.

Table 1-5 Physical Specifications

Characteristic	English System	Metric System
Depth Width Height Weight	10 ± 0.01 inches 8.55 ± 0.01 inches 4.5 +0, −0.2 inches 4.0 ± 0.2 pounds	254.0 ± 0.25 mm 217.2 ± 0.25 mm 114.3 +0, −5.1 mm 1.81 ± 0.09 kg

1.5 REQUIRED TOOLS AND TEST EQUIPMENT

A complete list of tools and test equipment necessary to perform testing and maintenance as outlined in chapters 6 and 7 follows. These items are also mentioned where used in a procedure.

1. A host system that will provide:

   a. Power of +24VDC and +5VDC to the tape drive.

   b. Diagnostic capability that includes: RESET, ERASE, RETENSION, WRITE, READ AND READ STATUS operations. The write operation must be able to alter the data pattern to those specified in testing.

2. A shop quality oscilloscope which must include 60MHZ minimum response, two channels, dual trace and accompanying ×10 probes in its complement of functions and accessories.

3. One digital multimeter.

4. Model 09C Tape Cartridge. Archive P/N 20121-00X

5. Azimuth alignment cartridge. Archive P/N 20072-00X

6. Track zero alignment tape.

   Nine track drives - Archive P/N 20180-00X

   Four track drives - Archive P/N 20071-00X

7. Zenith Alignment Inspection Plate and Indicator Block. Archive P/N 90003-00X

8. Shop tools must include:

   a. Numbers zero and one Phillips screw drivers.

   b. 3/16 inch long shaft and 1/4 inch nut drivers.

9. Jumper clips for connecting adjacent pins on PCB jumper blocks.

10. 14 or 16 pin IC test clip.

CHAPTER 2
INSTALLATION AND OPERATION

2.1 PRELIMINARY CONSIDERATIONS

2.1.1 Power Requirements

The power requirements of the tape drive are listed in Table 1-4. The DC power connector (J2) is an AMP type 641737-1. The mating connector for the cable is an AMP type 1-480424-0 and uses AMP type 60619-1 female contact pins. The power connector pin assignments are listed in table 2-1 and shown in figure 2-1.

2.1.2 Space Requirements

The LSI Sidewinder is designed to be installed in the mounting space of an eight inch floppy disk. The physical specifications of the Intelligent Drive are listed in table 1-5 and shown in figure 2-2. Figure 2-3 is the optional front panel outline drawing. Free air flow is required to prevent the unit's ambient temperature from rising above 45 degrees C (113 degrees F) under operating conditions. Otherwise forced air cooling should be supplied to achieve the operating temperature requirements.

2.1.3 System Connections

The host QIC-02 interface has been designed to minimize the number of interconnects between the drive and the host. The host connector (J1) pin assignments are listed in table 2-2, and shown in figure 2-4. Data and commands are transferred to and from the intelligent LSI Sidewinder tape drive on an 8-bit bidirectional data bus using asynchronous hand-shaking techniques to eliminate rigorous timing constraints. The host interface connector is designated J1. The connection is through a 50 pin PCB edge connector. The pins are numbered 1 through 50 with the even numbered pins located on the component side of the PCB. There is a key slot located between pins 4 and 6 to ensure the cable is mounted in the correct position. The recommended mating connector is a 3M type 3415-0001 fifty pin connector.

Table 2-1 Power Connector J2 Pin Assignments

Pin	Function
J2-1	+24 VDC
J2-2	+24 V RET
J2-3	+ 5 V RET
J2-4	+ 5 VDC

Note: Pins J2-2 and J2-3 are tied together on the PCB.

Table 2-2 QIC-02 Interface Host Connector Pin Assignments

Pin#	To	Mnemonic	Name
02	R	SPR–	Reserved
04	R	SPR–	Reserved
06	R	SPR–	Reserved
08	R	SPR–	Reserved
10	R	HBP–	Reserved*
12	B	HB7–	Host Bus Bit 7
14	B	HB6–	Host Bus Bit 6
16	B	HB5–	Host Bus Bit 5
18	B	HB4–	Host Bus Bit 4
20	B	HB3–	Host Bus Bit 3
22	B	HB2–	Host Bus Bit 2
24	B	HB1–	Host Bus Bit 1
26	B	HB0–	Host Bus Bit 0
28	D	ONL–	Online
30	D	REQ–	Request
32	D	RST–	Reset
34	D	XFR–	Transfer
36	H	ACK–	Acknowledge
38	H	RDY–	Ready
40	H	EXC–	Exception
42	H	DIR–	Direction
44	R	SPR–	Reserved
46	R	SPR–	Reserved
48	R	SPR–	Reserved
50	R	SPR–	Reserved

Note: All odd numbered pins are signal returns. They are connected to signal GND at the Host.

*Reserved for host odd parity.

R = Reserved
B = Bi-directional
D = Drive
H = Host

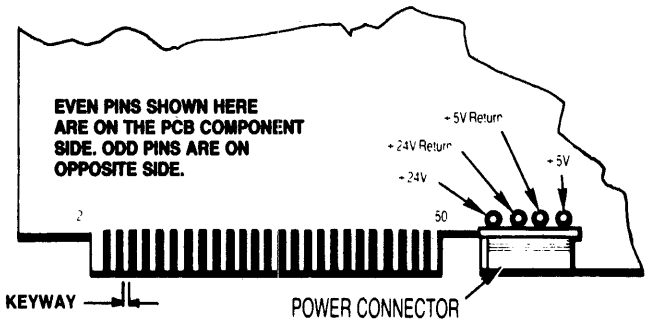


Figure 2-1 Drive Power Connector J2

2.1.4 Host and Tape Drive Termination Requirements.

Signal terminations at the host are 220 ohms to +5 VDC and 330 ohms to ground. The host shall terminate the bi-directional data bus and the four control signal lines from the tape drive.

Signal terminations at the tape drive are 220 ohms to +5 VDC and 330 ohms to ground. These resistances are provided by a 16 pin resistor dual inline package (DIP) located at socket 1J on the tape drive electronics PCB. The resistor DIP terminates the bi-directional data bus and 4 control signal lines from the host.

Signals from the host to the tape drive are loaded by no more than 2 milliamps and one terminator. The host shall not load the signals from the tape drive with more than 2 milliamps and one terminator.

2.1.5 Jumper Configuration

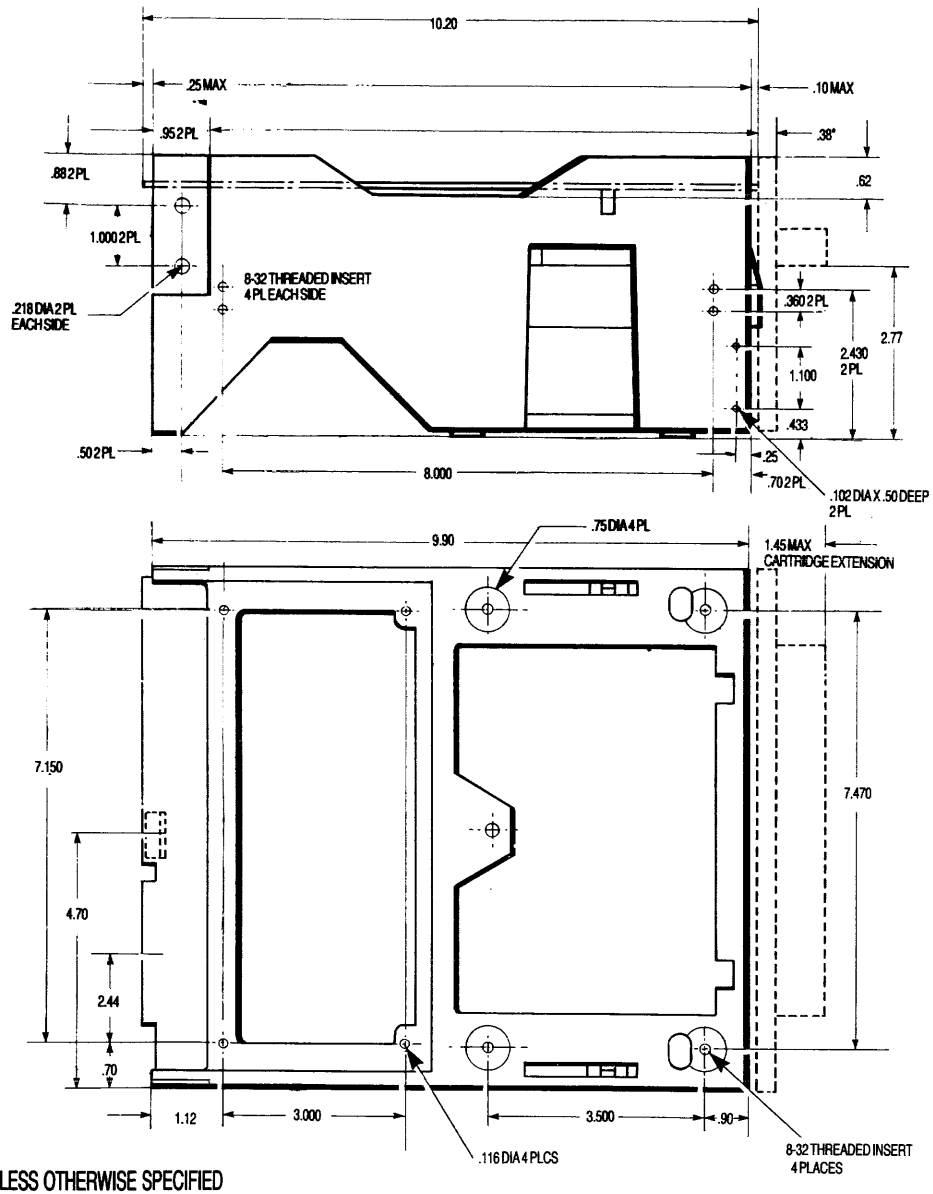
The jumper block, located on the electronics PCB, provides the means for selection of various options available with the tape drive. The jumper configuration is established at the time of manufacture and must not be changed. The only exceptions are deliberate changes by qualified service personel or during maintenance as described in this manual. The locations of the jumpers are shown in figure 2-5. Jumper configuration is listed in the table 2-3.

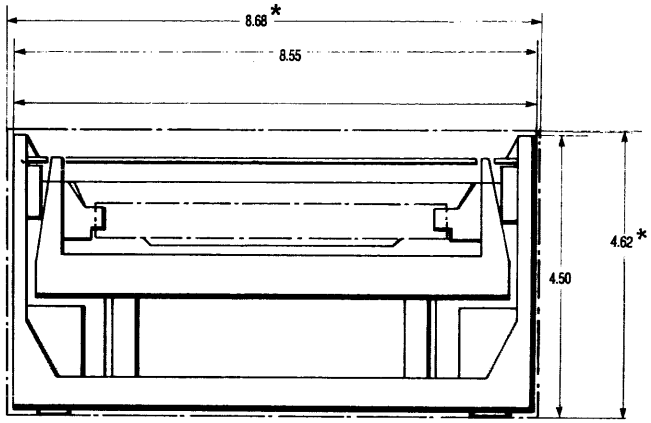
Table 2-3 Jumper Configuration For LSI Sidewinder Models (Table 1-1)

Jumper	Description
AA/BB	Always open
CC	Power-On Default Format Select • Jumper Present = QIC-24 Format • Jumper Removed = QIC-11 Format
DD	Speed Definition for Microprocessor • Jumper Present = 30 IPS • Jumper Removed = 90 IPS
EE	Interface Parity • Jumper Present = Parity Enabled • Jumper Removed = Parity Disabled (Not supported at this time)
FF	Loop on Error Used by Archive Engineering for troubleshooting.
HH	Test Configuration Used by Archive Manufacturing only
KK	Power on Confidence Test • Jumper Present = Test run at power on or on reset pulse • Jumper Removed = Test Disabled
ZZ	Defines to the Microprocessor application program that there is an external memory. • Jumper always present

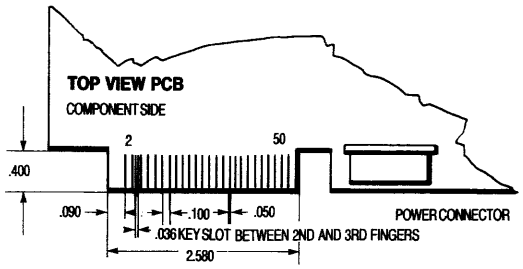
Table 2-3 Jumper Configuration For LSI Sidewinder Models (Table 1-1) (Continued)

Jumper	Description
A or B to Common	PLL Feedback for Speed Selection • A to Common Jumper = 30 IPS • B to Common Jumper = 90 IPS
A1, A2 and A3	Always A1 to A2
B1, B2 and A3	Always B1 to B2
C	Test Jumper for PLL Gain Adjustment • Removed for Operation
K	Gain Setting of Read Circuit • Jumper Present = 30 IPS • Jumper Removed = 90 IPS
R	Read Data Pulse One Shot Timing • Jumper Present = 90 IPS • Jumper Removed = 30 IPS
T	Run in Phase Clip • Used by Manufacturing Only Removed for Operation
U	Always Present
Y	Track Number Selection • Jumper Present = 9 Track • Jumper Removed = 4 Track
Location between 7B and 8B	Phase for Stepper Motor Set by Archive Manufacturing Do not change from factory setting





* OPTIONAL FRONT PLATE DIMENSION



TOP COMPONENT SIDE: EVEN NUMBERED FINGERS

BOTTOM SOLDER SIDE: ODD NUMBERED FINGERS

INPUT/OUTPUT CONNECTOR DETAIL

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 2-2 Outline Dimensions

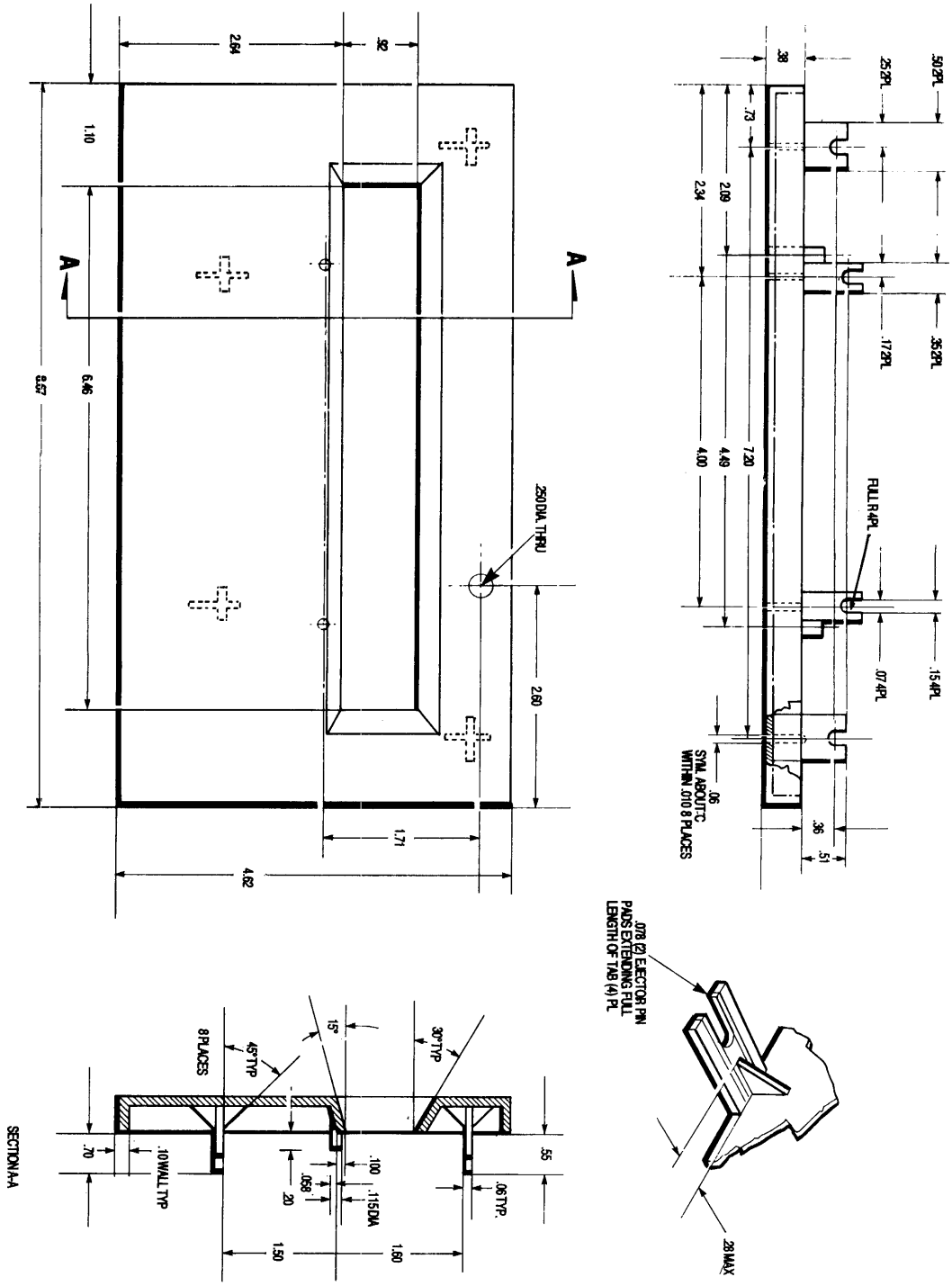


Figure 2-3 Optional Front Panel Outline Drawing

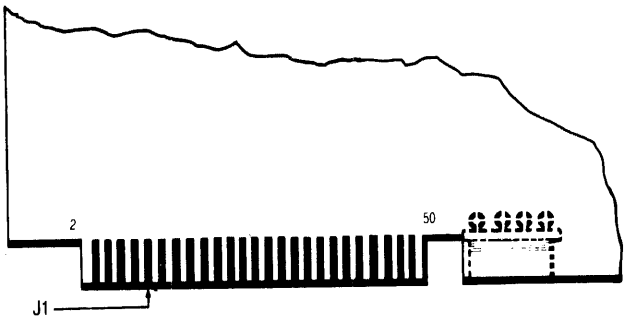


Figure 2-4 Host Interface Connector J1

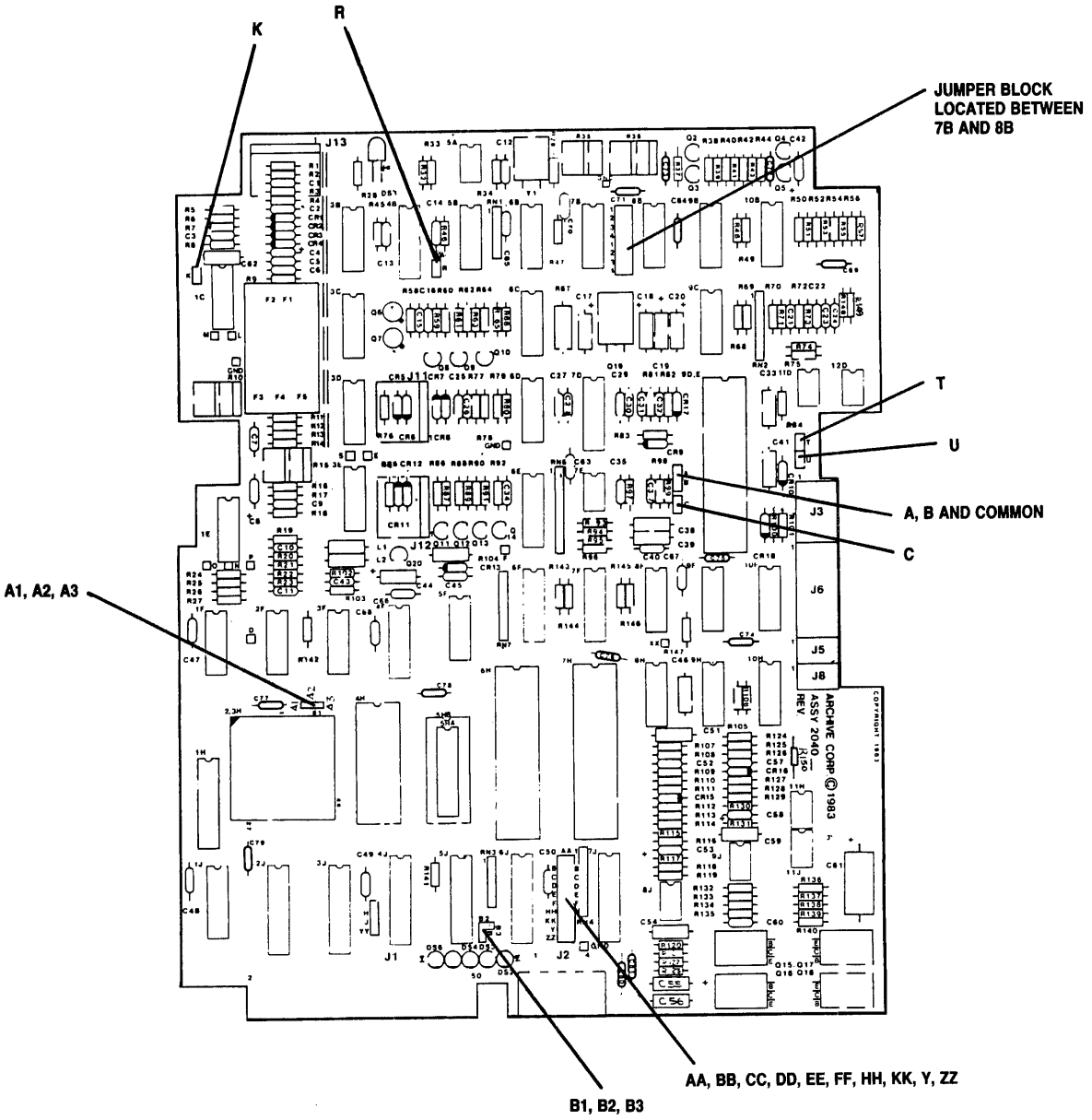


Figure 2-5 Electronics PCB Jumper Location

2.2 RECEIVING AND INSPECTION

2.2.1 Unpacking

To unpack the Intelligent Tape Drive, place the container on a flat stable surface. Remove the tape drive from the container. If practical, save the containers and packing materials for future re-shipment.

2.2.2 Inspection

Perform a complete visual inspection to assure that there is no physical damage caused during shipment.

2.2.3 Handling

It is often necessary to transport and handle the tape drive after it is unpacked and prior to installation. Industry standard procedures for the handling of electronic equipment are sufficient to ensure the equipment is not subjected to physical shock or damage. Since the unit contains exposed components and assemblies, proper care should be taken to ensure their protection from physical damage and damage caused by electrostatic discharge (ESD) introduced through handling. To prevent damage to the drive from ESD avoid handling the drive at electronic assemblies or employ ESD dissipation devices, e.g. wrist strap and mats.

2.3 INSTALLATION

When the tape drive is to be mounted in an enclosure, a number of precautions must be taken to ensure proper operation. Mounting instructions are explained in paragraphs 2.3.1 thru 2.3.2.

2.3.1 Horizontal Mounting

Mount the tape drive unit flat on the user supplied frame with the tape cartridge slot facing forward and the PCB at the top. Secure the drive using any four of the eight threaded holes on the sides of the unit.

2.3.2 Vertical Mounting

Mount the tape drive unit on its right side with the tape cartridge slot facing forward (J1 connector down). Both the top and bottom mounting holes (figure 2-2) should be used. Mounting the tape drive on its left side is not recommended. In the vertical position the drive is tested for alignment only on its right side.

It is not recommended that the tape drive unit be mounted such that the tape cartridge slot is facing up. This would allow dirt and other foreign materials to fall into the tape head area.

No special shock mounting is required when the Archive supplied frame is used. If a customer supplied frame is used, it is extremely important to maintain the three-point flexible mounting arrangement for the unit.

2.3.3 Electrostatic Discharge (ESD) Protection.

Two braided wires which are part of the ESD protection network are fastened to the sides of the tape drive chassis during drive shipment. Remove the two screws which fasten the wires to the tape drive chassis. Connect the wires to a good earth ground using the ring tongue terminals. The terminals accept 6-32 screws. Refer to Figure A2-1 for location of ESD protection wires.

2.4 OPERATION

The only operator intervention required to operate the Intelligent Tape Drive is to load the tape cartridge. All other functions are performed under software control from the tape drive electronics PCB and the host CPU.

2.4.3 Cartridge Loading/Unloading

The cartridge is loaded by pushing it to a hard stop through the loading aperture. The aperture in the optional front panel and the receiving hardware will allow the cartridge to be installed in only the proper orientation. Any customer supplied front panel must limit the aperture dimensions as specified in figure 2-3. Before inserting the tape cartridge, position the write protect plug as shown in figure 2-6, to enable or inhibit writing on the tape.

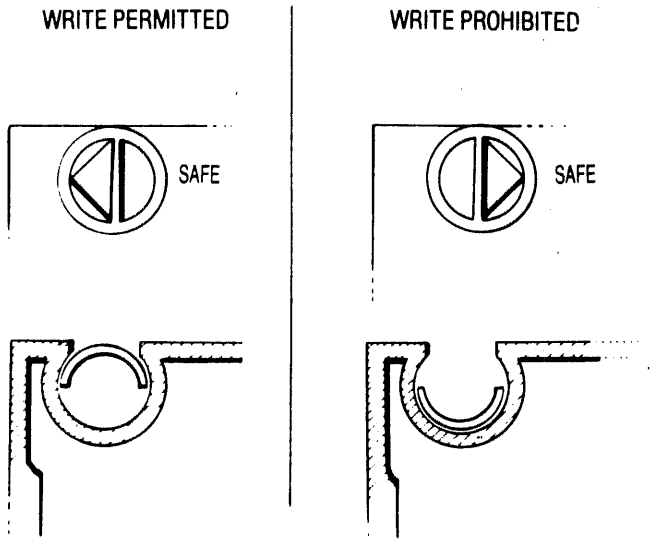


Figure 2-6 Write Protect Plug Positioning

2.5 INITIAL TESTS

There are no field adjustments for the Archive Intelligent Tape Cartridge Drive. The adjustments listed in Chapter 7 are shop adjustments requiring special equipment. There are two field checks that are overall performance tests. These are the read test and the write test.

2.5.1 Equipment Required

1. A known good tape with known data preferrably written on a Master Drive. The number of read errors when this tape is read on the Master Drive should be known. This tape is used only for read testing.
2. A known good tape to be used for write testing.

2.5.2 Read Test

1. Using the known good tape, read a file from tape.
2. Check the soft error count. If the tape was read with a comparable number of errors as were found on the Master Drive, the read channel is acceptable.

2.5.3 Write Test

1. Using a good test tape, write one track in the forward direction and one track in the reverse direction of known data pattern.
2. Check the soft error count. If the data was written with a comparable number of rewrites as occurred with the Master Drive, then the write channel is acceptable.

2.6 PREVENTIVE MAINTENANCE

Preventive Maintenance consists of cleaning the read/write/erase head and checking the soft error statistics to determine tape deterioration.

2.6.1 Cleaning

Clean the read/write/erase head assembly and the tape hole sensor openings with a clean, lintless cotton swab dampened with IBM head cleaning solution or 95% isopropyl alcohol using the following schedule:

1. After an initial pass with a new tape cartridge or, if using all new tape cartridges, after every 2 hours of actual use.
2. After every 8 hours of normal use.

2.6.2 Soft Error Statistics

Read and write error statistics are available to the host through the Read Status command. Typically, the Read Status command should be executed after completion of each cartridge used and the statistics reported at least on an exception basis. An increase in the soft write error rate normally indicates a deterioration of the recording media. If initializing the cartridge does not reduce the soft errors dramatically, a known good tape should be substituted. If the soft error rate is high on a known good tape, the tape drive is in need of servicing. If the soft write error rate is low on a known good tape, the cartridge with the high soft write error rate should be replaced with a new cartridge.

CHAPTER 3
SYSTEM INTERFACE

3.1 GENERAL

This chapter contains system interface information. The following paragraphs provide an explanation of the signals that pass between the LSI Intelligent drive and the host. Read/write commands, data and status information are transmitted to and from the LSI intelligent drive and host via the industry standard QIC-02 interface (figure 3-1). The QIC-02 interface contains the following control and data lines.

a. Four control lines from the host.

b. Four control lines from the LSI drive.

c. An 8-bit bi-directional data/command bus.

The bus and control signals between LSI drive and host are all standard TTL levels (low true).

FALSE: Logic 0 (high) = 2.4 to 5.25VDC

TRUE: Logic 1 (low) = 0 to 0.55VDC

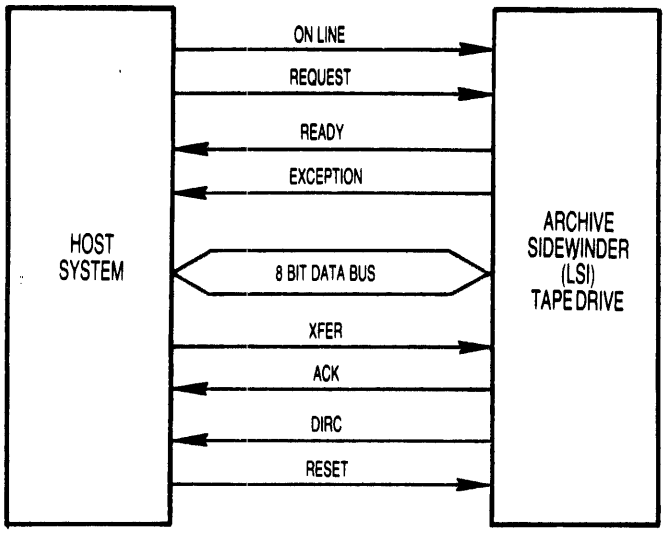


Figure 3-1 QIC-02 Interface

3.2 HOST GENERATED SIGNALS

3.2.1 REQUEST

REQUEST is driven by the host to signal to the controller that a command is present on the 8 bit bi-directional bus and to handshake the command across the bus.

REQUEST is also used to handshake the six status bytes from the drive to the host.

3.2.2 ON-LINE

ON-LINE must be true prior to beginning a read or write operation. When ON-LINE becomes false, the operation is terminated and the cartridge is rewound to BOT. If the drive is in the Write mode when ON-LINE is dropped a File Mark will also be written prior to rewinding to BOT.

3.2.3 TRANSFER

TRANSFER is the data handshake signal from the Host. It is used with ACKNOWLEDGE from the drive to transfer data across the bi-directional bus.

3.2.4 RESET

The RESET line is used to initialize the tape drive. A RESET causes the drive to recalibrate the heads to track zero and to initialize the firmware. If Jumper KK is present on the PWB a power on confidence test will be run as described in Chapter 7 of this manual.

3.3 DRIVE GENERATED SIGNALS

3.3.1 READY

READY is driven by the tape drive. It signals that the drive can accept a command and is used to handshake the command across the interface. During a read status operation it is used to handshake status information across the interface to the host. In the write mode READY indicates that a buffer in the drive is ready to be filled by the host. In the read mode READY indicates that a drive buffer is ready to be emptied by the host.

3.3.2 EXCEPTION

EXCEPTION is used to alert the host to a condition which has terminated the execution of a command. The drive sets EXCEPTION to signal the termination of an operation. The termination referred to may be a normal completion or an interruption due to an encountered fault (hard errors, write protected cartridges, etc.). The only acceptable response by the host to an EXCEPTION condition is to command READ STATUS. The cause of the EXCEPTION condition will be revealed in the drive status. (see paragraph 3.4.10.1)

3.3.3 ACKNOWLEDGE

ACKNOWLEDGE is the data handshake signal from the drive. It is used with TRANSFER to transfer data across the interface.

3.3.4 DIRECTION

The state of the DIRECTION signal establishes the direction of signal flow before commands, data or status are placed on the bus. The intelligent Sidewinder (LSI) drive controls the direction of the bus. DIRECTION is available to the host only to enable/disable the host's bus drivers.

3.4 DATA BUS

The Bi-directional bus lines are used to transfer commands, status, and data between the host system and the intelligent Sidewinder (LSI) tape drive.

3.4.1 The Command Set

The Sidewinder command set is shown in Table 3-1. All Sidewinder commands are single byte commands and are QIC-02 compatible.

Table 3-1 Command Summary

Bit 7654	Bit 3210	DESCRIPTION
0000	0001	Select, Soft Lock OFF
0001	0001	Select, Soft Lock ON
0010	0001	BOT
0010	0010	Erase
0010	0100	Retension
0010	0110	Select QIC-11 Format (Note 1)
0010	0111	Select QIC-24 Format (Note 1)
0100	0000	Write
0110	0000	Write File Mark
1000	0000	Read
1010	0000	Read File Mark
1100	0000	Read Status

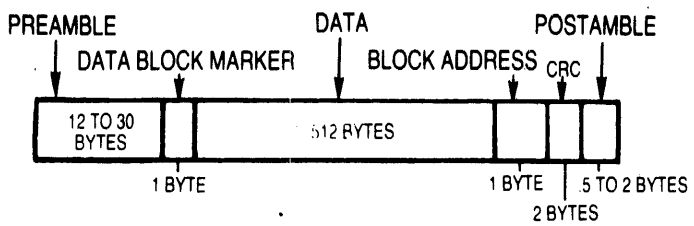
Note 1: LSI Sidewinder-2 models only.
See Table 1-1.

3.4.2 SELECT Command

The Soft Lock feature assists the operator in preventing inadvertent cartridge removal by controlling the drive select light. The SELECT, Soft Lock Off command will cause the select light to be on only when the tape is positioned away from BOT. The SELECT, Soft Lock On command will cause the select light to remain on regardless of tape position. In addition, EXCEPTION will be asserted when the cartridge is removed while the select light is on.

3.4.3 SELECT QIC-11 FORMAT Command (LSI Sidewinder-2 Models — see Table 1-1)

The SELECT QIC-11 FORMAT command sets the controller format to QIC-11 format. This command is legal only at BOT (i.e., it shall not be possible to append in a different format).

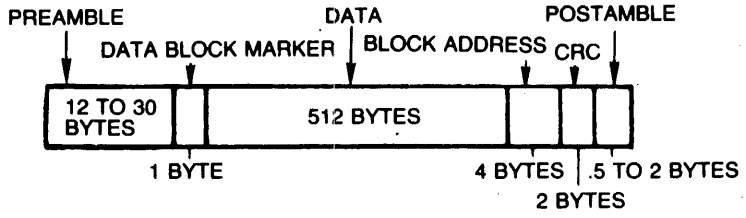


12 to 30	Bytes	Preamble	1	Byte	Block Address
1	Byte	Data Block Marker	2	Bytes	CRC
512	Bytes	Data	0.5 to 2	Bytes	Postamble

Figure 3-2 QIC-11 1/4-Inch Streaming Tape Format

3.4.4 SELECT QIC-24 FORMAT Command (LSI Sidewinder-2 Models — see Table 1-1)

The SELECT QIC-24 FORMAT command sets the controller format to QIC-24 format. This command is legal only at BOT (i.e., it shall not be possible to append in a different format).



12 to 30	Bytes	Preamble	4	Byte	Block Address
1	Byte	Data Block Marker	2	Bytes	CRC
512	Bytes	Data	0.5 to 2	Bytes	Postamble

Figure 3-3 QIC-24 1/4-Inch Streaming Tape Format

3.4.5 Motion Commands

Within the motion command type, there are three operations that can be performed.

1. Rewind the tape cartridge to BOT.
2. Completely ERASE a tape cartridge.
3. Manually intialize a cartridge.

The command to accomplish the first operation is called the BOT command. It will rewind the tape at high speed to BOT.

An ERASE command will accomplish the second operation. The entire tape is erased with an an erase bar the width of the tape.

To accomplish the third operation a RETENSION command is issued. This will rewind the tape first to BOT at high speed, then to EOT and back to BOT.

3.4.6 WRITE Command

The WRITE command instructs the drive to write data on the tape. While writing, data formatting and error correction are automatically performed. The host asserts

ONLINE and issues the WRITE command. The READY line is activated when the controller is ready for a data block transfer. When the READY line is active, the host terminates transfer of write data by issuing a WRITE-FILE-MARK command. When the READY line is active, the host alternatively terminates transfer of write data by deactivating ONLINE. Deactivating ONLINE causes a File Mark to be written (if not preceded by a WRITE-FILE-MARK command) and the tape rewound to BOT. Note: A WRITE command following cartridge insertion or RESET shall commence recording at BOT otherwise, recording shall commence at the current tape position. Note: if the host starts transfer between blocks before READY is asserted, READY may not be asserted. When the early warning hole of the last track is detected by the controller, the controller ceases to transfer additional data blocks from the host. The controller terminates the WRITE command and reports END OF MEDIA by means of an EXCEPTION and READ STATUS.

3.4.7 WRITE FILE MARK Command

A WRITE FILE MARK command causes the LSI Sidewinder to write a file mark on the tape. A file mark may be used to identify the end of recorded data or a division between groups of data. The command may be given to conclude writing or to create a division between the data being written.

3.4.8 READ Command

The READ command instructs the drive to read data from the tape. During a read operation, error recovery will be automatically performed by the drive. The host asserts ONLINE and issues the READ command. If the READ command is issued at BOT, the drive will start tape motion in search of data. When the first block has been read successfully, READY is asserted and data transfers to the host begin. The drive will continue reading and transmitting data to the host until a File Mark is encountered. When the drive reads a file mark, the read mode is exited and EXCEPTION is asserted with "File Mark Detected" in the status bytes.

If no data is present on the cartridge, the drive will assert "EXCEPTION" and "No Data Detected" will be set in the status bytes. When READY is asserted, the host may terminate the READ command by deactivating ONLINE. Deactivating ONLINE during READ also causes the tape to be rewound to BOT. When READY is true, the host may alternatively terminate the READ command by issuing a READ-FILE-MARK command. If a READ command is issued, the command is accepted and the drive continues reading. Note: A READ command following cartridge insertion or RESET shall commence at BOT, otherwise the read command commences from the current tape position. Note: If the host starts transfer between blocks before READY is asserted, READY may not be asserted.

3.4.9 READ FILE MARK Command

The READ FILE MARK command allows the user to seek to the end of a file. During a read file mark operation, the controller will read the tape, searching for a file mark, but the data will not be transferred to the host. When a file mark

is detected, tape motion is stopped, EXCEPTION is asserted, and the host learns that a file mark was found by commanding READ STATUS.

3.4.10 READ STATUS Command

The READ STATUS command is used to transfer status information from the drive to the host. Six status bytes are used to communicate such things as "end of media", "file mark detected", "write protected cartridge", etc.

A READ STATUS operation may be initiated by the host at the completion of a command. The host must issue the READ STATUS command whenever EXCEPTION is asserted by the drive.

3.4.10.1 Status Information

The LSI Sidewinder maintains six bytes of status information that are available to the host. The status bytes are requested by a READ STATUS command. When an exception condition occurs, the host must perform a read status operation. An exception condition is defined as any condition which prevents the performance or continuation of a command.

The host, however, is not limited to using the READ STATUS command only in response to an exception condition. Within the limits of the interface protocol, the host may request status at any time.

The status bytes contain the following information:

STATUS BYTE 0

BIT 0: FIL — File Mark Detected bit is set when a File Mark is detected during a Read Data or Read File Mark Sequence. The bit is reset by a Read Status Sequence.

BIT 1: BNL — Block in error Not Located bit is set when an unrecoverable read error occurs and the controller can not confirm that the last block transmitted was the block in error. The bit is reset by a Read Status Sequence.

BIT 2: UDE — Unrecoverable Data bit is set when the controller experiences a hard error during read or write operations. The bit is reset by a Read Status Sequence.

BIT 3: EOM — End of Media bit is set when the logical early warning hole of the last track is detected during a write operation. This bit will remain set as long as the drive is at logical end of media. The EOM bit will not be reset by a Read Status Sequence.

BIT 4: WRP — Write Protected bit is set if the cartridge write protect plug is set in the file protect "safe" position. Operator must change the write protect plug position before the status bit will reset.

BIT 5: USL — Drive Unselected bit is set if the selected drive is not physically connected or is not receiving power. Operator must correct the condition before the status bit will reset.

BIT 6: CNI — Cartridge not in Place bit is set if a cartridge is not fully inserted into the drive. Operator must correct the condition before the status bit will reset.

BIT 7: STO — Status Byte 0 bit is set if any other bit in Status Byte 0 is set.

STATUS BYTE 1

BIT 0: POR — The Power-on Reset bit is set after the host asserts RESET or when the controller is powered up. The bit is reset by a Read Status Sequence.

BIT 1: RES — Reserved

BIT 2: RES — Reserved

BIT 3: BOM — Beginning of Media bit is set whenever the cartridge is logically at beginning of tape, track 0. The bit is reset when the tape moves away from beginning of tape. This bit does not set EXCEPTION when it goes true, nor is it reset by the Read Status Sequence.

BIT 4: MBD — Marginal Block Detected bit is set when the controller determines that a data block is marginal. This bit is provided to indicate that eight or more retries were necessary. This bit does not set EXCEPTION when it goes true. This bit is reset by a Read Status Sequence.

BIT 5: NDT — No Data Detected bit is set when an unrecoverable data error occurs due to lack of recorded data. Absence of recorded data is the failure to detect a data block within a controller timeout. This bit is reset by a Read Status Sequence.

BIT 6: ILL — Illegal Command bit is set if any of the following occurs. The bit is reset by a Read Status Sequence.

a. ONLINE not asserted when a WRITE, WRITE FILE MARK, READ or READ FILE MARK command is issued.

b. A command other than WRITE or WRITE FILE MARK is issued during the execution of a Write Data Sequence.

c. A command other than READ or READ FILE MARK is issued during the execution of a Read Data Sequence.

d. A SELECT command is issued when the cartridge in the drive is not at beginning of tape, track 0.

e. Any unimplemented command is issued.

f. A SELECT FORMAT command is issued when the cartridge in the drive is not at the beginning of tape, track 0.

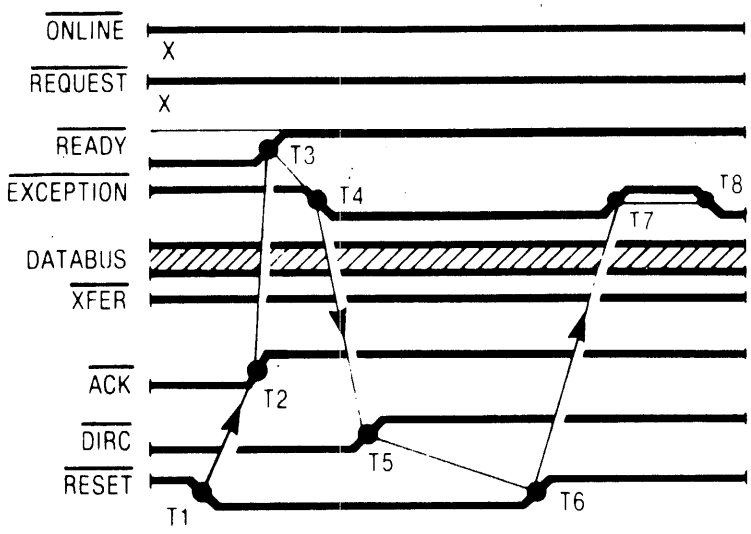
BIT 7: ST1 — Status byte 1 bit is set if any other bit in Status byte 1 is set.

Bytes 2 and 3 contain the data error counter (DEC) which accumulates the number of blocks rewritten for WRITE operations and the number of soft read errors during READ operations. These bytes shall be cleared by a Read Status Sequence. Byte 2 contains the MSB and Byte 3 contains the LSB.

Bytes 4 and 5 contain the underrun counter (URC) which accumulates the number of times that streaming was interrupted because the host failed to maintain the minimum through-put rate. These bytes shall be cleared by a Read Status Sequence. Byte 4 contains the MSB and Byte 5 contains the LSB.

3.5 INTERFACE SIGNAL TIMING

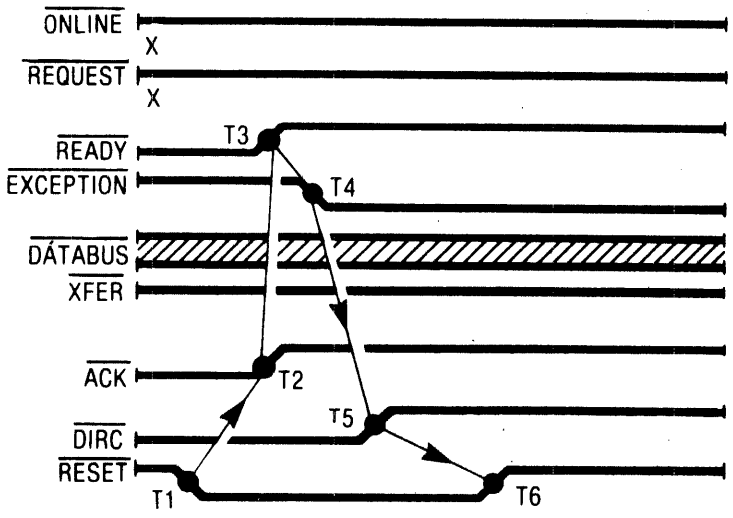
Timing diagrams (figures 3-4 thru 3-12) are included on the following pages for the reset control signal (with and without POC) and the QIC-02 REV D compatible command set.



ACTIVITY	CRITICAL TIMING
T1-HOST ASSERTS RESET	N/A
T2-CONTROLLER DISABLES ACK	T1—T2<1 U Sec.
T3-CONTROLLER DISABLES READY	T1—T3<1 U Sec.
T4-CONTROLLER ASSERTS EXCEPTION	T1—T4<3 U Sec.
T5-CONTROLLER DISABLES DIRC	T1—T5<3 U Sec.
T6-HOST DISABLES RESET	T1—T6>25 U Sec.
T7-CONTROLLER DISABLES EXCEPTION	T6—T7>0
T8-CONTROLLER ASSERTS EXCEPTION	T7—T8<5 Sec. For POC Pass

X-DON'T CARE

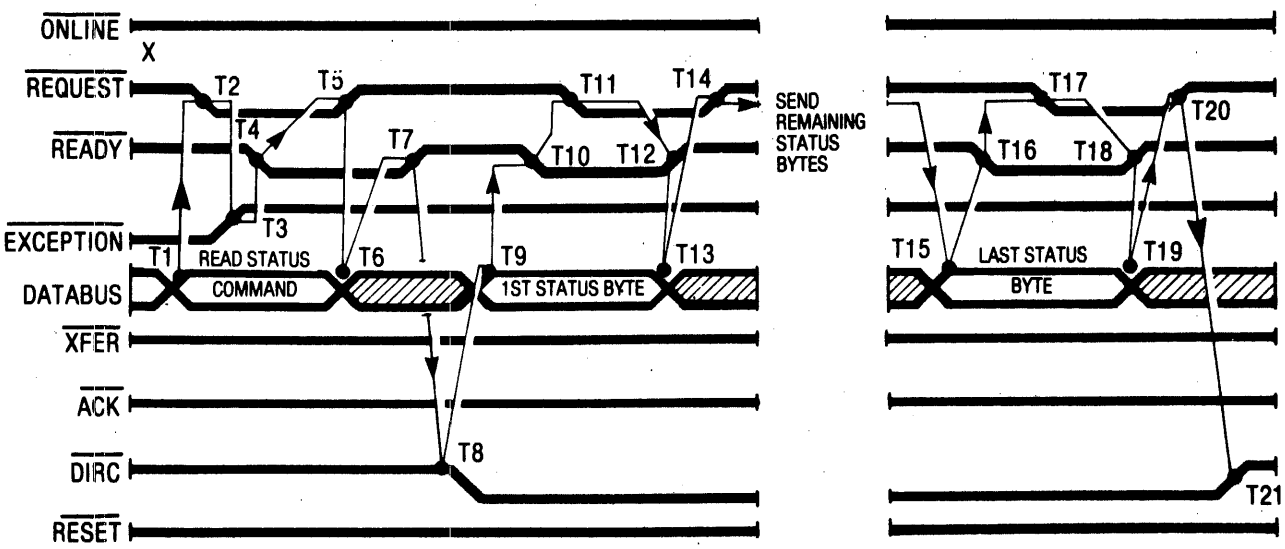
Figure 3-4 Reset Timing With POC Enabled



ACTIVITY	CRITICAL TIMING
T1-HOST ASSERTS RESET	N/A
T2-CONTROLLER DISABLES ACK	T1—T2<1 U Sec.
T3-CONTROLLER DISABLES READY	T1—T3<1 U Sec.
T4-CONTROLLER ASSERTS EXCEPTION	T1—T4<3 U Sec.
T5-CONTROLLER DISABLES DIRC	T1—T5<3 U Sec.
T6-HOST DISABLES RESET	T1—T6>25 U Sec.

X-DON'T CARE

Figure 3-5 Reset Timing Without POC Enabled

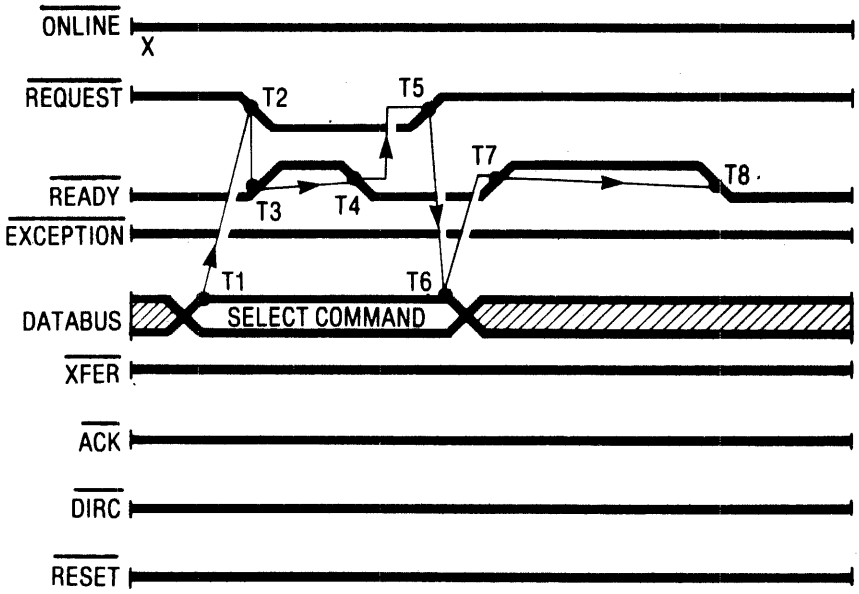


ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A
T2-HOST SETS REQUEST	T1—T2>0 U Sec.
T3-CONTROLLER RESETS EXCEPTION	T3—T4>10 U Sec.
T4-CONTROLLER SETS READY	20<T2—T4<500 U Sec.*
T5-HOST RESETS REQUEST	T4—T5>0 U Sec.
T6-BUS DATA INVALID	T4—T6>0 U Sec.
T7-CONTROLLER RESETS READY	20<T5—T7<100 U Sec.
T8-CONTROLLER CHANGES BUS DIRECTION	N/A
T9-1ST STATUS BYTE TO BUS	N/A
T10-CONTROLLER SETS READY	T7—T10>20 U Sec.
T11-HOST SETS REQUEST	N/A
T12-CONTROLLER RESETS READY	T11—T12<1 U Sec.
T13-BUS DATA INVALID	T11—T13>0 U Sec.
T14-HOST RESETS REQUEST	T11—T14>20 U Sec.
T15-LAST STATUS BYTE TO BUS	N/A
T16-SAME AS T10	SAME AS T10
T17-SAME AS T11	SAME AS T11
T18-SAME AS T12	SAME AS T12
T19-SAME AS T13	SAME AS T13
T20-SAME AS T14	SAME AS T14
T21-CONTROLLER CHANGES BUS DIRECTION	N/A
T22-CONTROLLER SETS READY	T20—T21>0 U Sec.
X-DON'T CARE	T21—T22>0 U Sec.

*NOTE: This time may be>500 M Sec. if the following occurs:

a. The online signal is deasserted
b. Retry sequence and no data detected
c. At end of the track and turn around or start up.

Figure 3-6 Read Status Command Timing Diagram

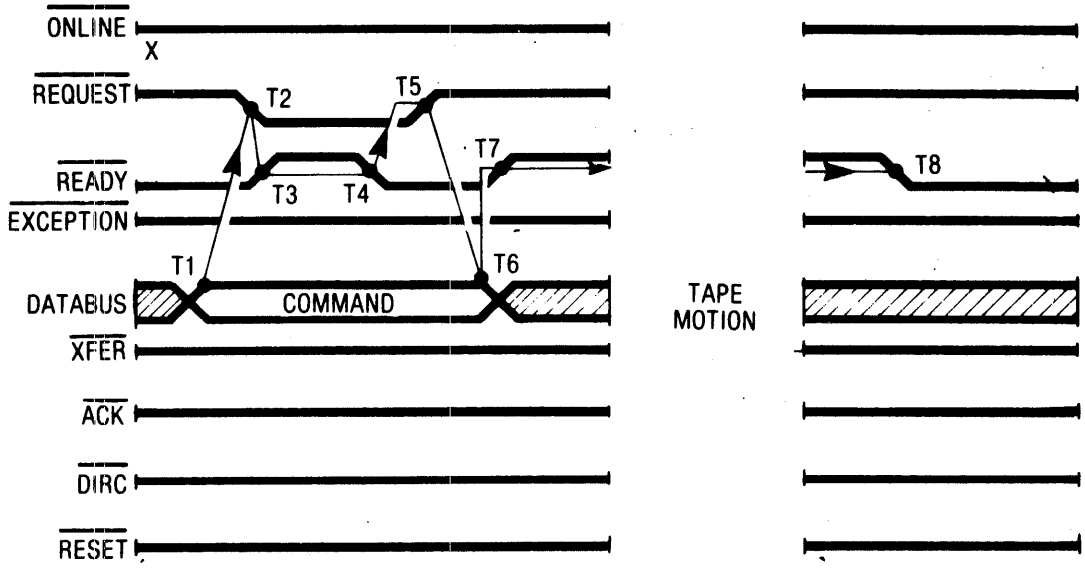


ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A
T2-HOST SETS REQUEST	T1—T2>0 U Sec.
T3-CONTROLLER RESETS READY	T2—T3<1 U Sec.
T4-CONTROLLER SETS READY	50<T3—T4<500 U Sec.*
T5-HOST RESETS REQUEST	T4—T5>0 U Sec.
T6-BUS DATA INVALID	T4—T6>0 U Sec.
T7-CONTROLLER RESETS READY	20<T5—T7<100 U Sec.
T8-CONTROLLER SETS READY	T7—T8>20 U Sec.
X-DON'T CARE	

*NOTE: This time may be>500 M Sec. if the following occurs:

a. The online signal is deasserted.
b. Retry sequence and no data detected.
c. At end of the track and turn around or start up.

Figure 3-7 Select Command Timing Diagram



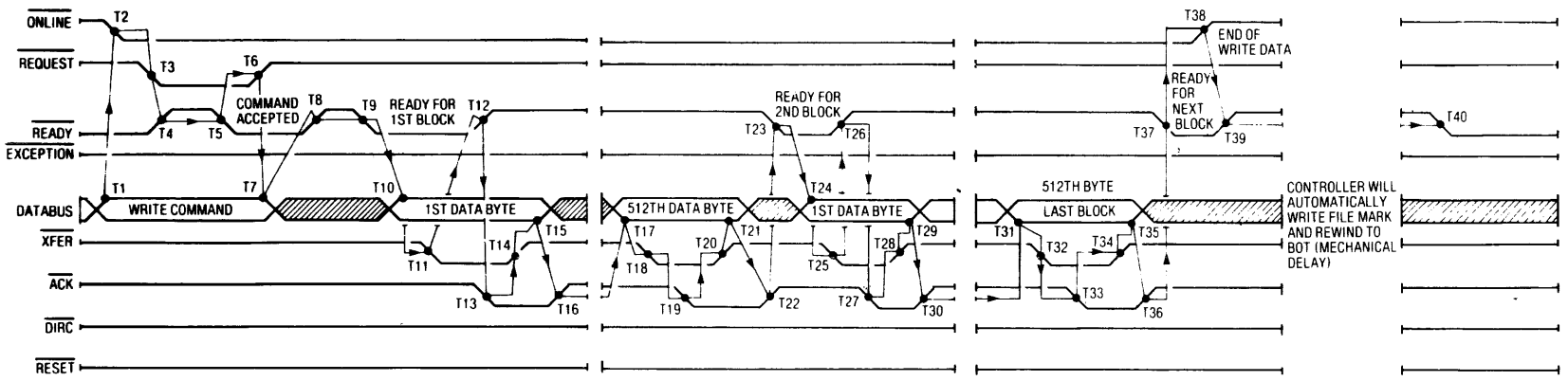
ACTIVITY	CRITICAL TIMING
T1-HOST BUS DATA VALID	N/A
T2-HOST SETS REQUEST	T1—T2>0 U Sec.
T3-CONTROLLER RESETS READY	T2—T3<1 U Sec.
T4-CONTROLLER SETS READY	20<T3—T4<500 U Sec.*
T5-HOST RESETS REQUEST	T4—T5>0 U Sec.
T6-BUS DATA INVALID	T3—T6>0 U Sec.
T7-CONTROLLER RESETS READY	20<T5—T7<100 U Sec.
T8-CONTROLLER SETS READY	T7—T8>20 U Sec.

X-DON'T CARE

*NOTE: This time may be>500 M Sec. if the following occurs:

a. The online signal is deasserted
b. Retry sequence and no data detected
c. At end of the track and turn around or start up

Figure 3-8 BOT, Retension or Erase Command Timing Diagram

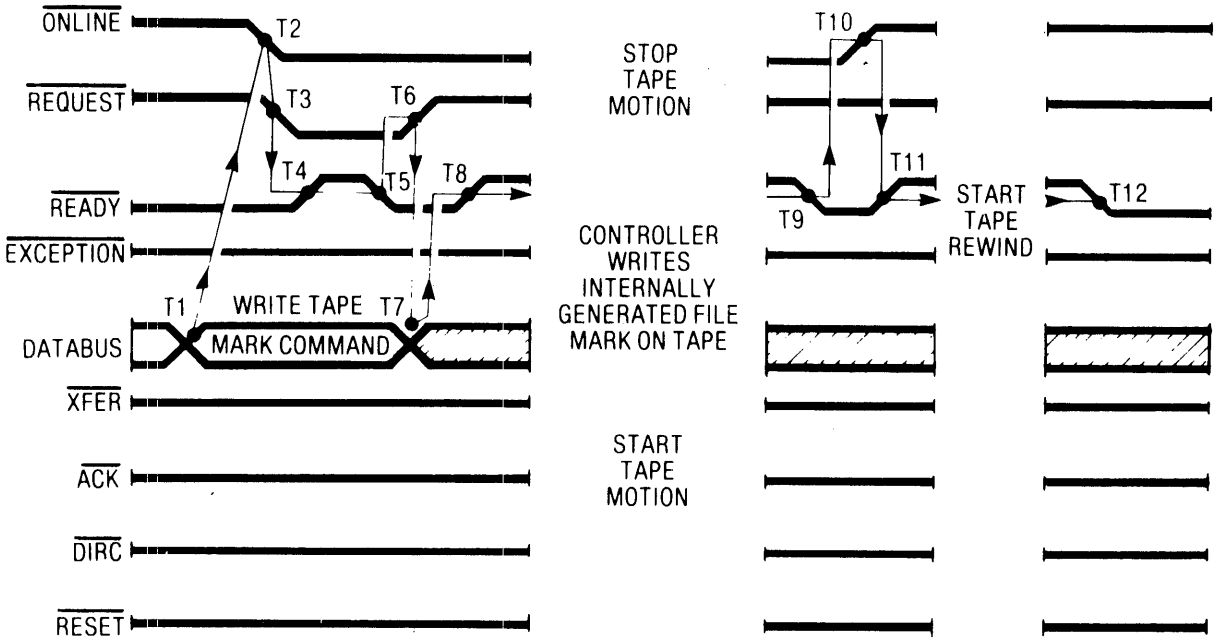


ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING	ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A	T15-BUS DATA INVALID	T13—T15>0 U Sec.	T28-HOST RESETS XFER	SAME AS T14
T2-HOST SETS ONLINE	N/A	T16-CONTROLLER RESETS ACK	0<T14—T16<3 U Sec.	T29-BUS DATA INVALID	SAME AS T15
T3-HOST SETS REQUEST	T2—T3>0 U Sec.	T17-HOST DATA TO BUS	N/A	T30-CONTROLLER RESETS ACK	SAME AS T16
T4-CONTROLLER RESETS READY	T3—T4<1 U Sec.	T18-SAME AS T11	SAME AS T11	T31-HOST DATA TO BUS	N/A
T5-CONTROLLER SETS READY	20<T4—T5<500 U Sec.*	T19-SAME AS T13	SAME AS T13	T32-HOST SETS XFER	SAME AS T18
T6-HOST RESETS REQUEST	T5—T6>0 U Sec.	T20-SAME AS T14	SAME AS T14	T33-CONTROLLER SETS ACK	SAME AS T19
T7-BUS DATA INVALID	T5—T7>0 U Sec.	T21-SAME AS T15	SAME AS T15	T34-HOST RESETS XFER	SAME AS T20
T8-CONTROLLER RESETS READY	20<T6—T8<100 U Sec.	T22-SAME AS T16	SAME AS T16	T35-BUS DATA INVALID	N/A
T9-CONTROLLER SETS READY	T8—T9>20 U Sec.	T23-CONTROLLER SETS READY	T22—T23>100 U Sec.	T36-CONTROLLER RESETS ACK	SAME AS T22
T10-HOST DATA TO BUS	N/A	T24-HOST DATA TO BUS	N/A	T37-CONTROLLER SETS READY	SAME AS T23
T11-HOST SETS XFER	T10—T11>-40 NANO Sec.	T25-HOST SETS XFER	SAME AS T11	T38-HOST RESETS ONLINE	N/A
T12-CONTROLLER RESETS READY	T11—T12<1 U Sec.	T26-CONTROLLER RESETS READY	SAME AS T12	T39-CONTROLLER RESETS READY	N/A
T13-CONTROLLER SETS ACK	0.5<T11—T13<100 U Sec	T27-CONTROLLER SETS ACK	SAME AS T13	T40-CONTROLLER SETS READY	N/A
T14-HOST RESETS XFER	T13—T14>0 U Sec.				

*NOTE: This time may be>500 M Sec. if the following occurs:

a. The online signal is deasserted
b. Retry sequence and no data detected
c. At end of the track and turn around or start up.

Figure 3-9 Write Data Command Timing Diagram

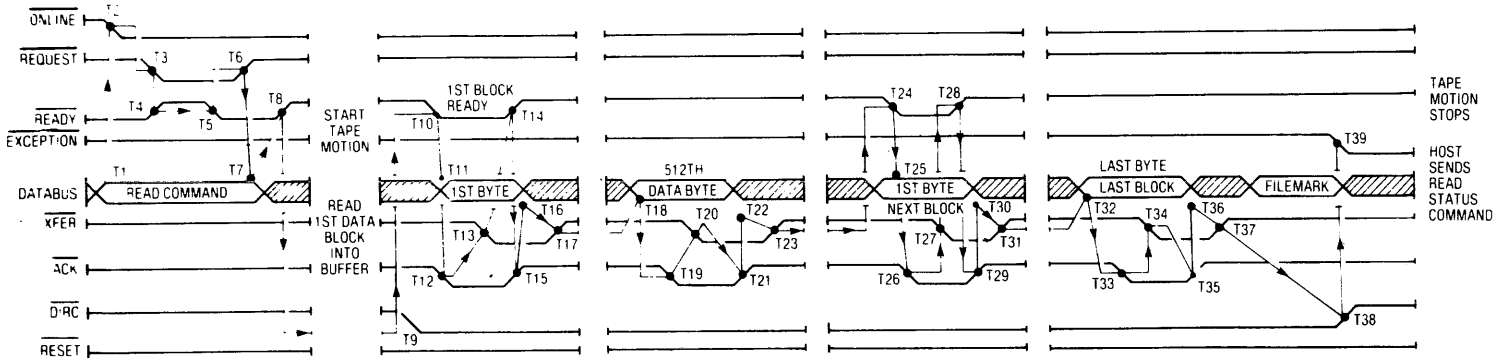


ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A
T2-HOST SETS ONLINE	T1—T2 >0 U Sec.
T3-HOST SETS REQUEST	T2—T3 >0 U Sec.
T4-CONTROLLER RESETS READY	T3—T4 <1 U Sec.
T5-CONTROLLER SETS READY	20< T4—T5< 500 U Sec.*
T6-HOST RESETS REQUEST	T5—T6 >0 U Sec.
T7-BUS DATA INVALID	T5—T7 >0 U Sec.
T8-CONTROLLER RESETS READY	20< T6—T8< 100 U Sec.
T9-CONTROLLER SETS READY	N/A
T10-HOST RESETS ONLINE	T9—T10 >0 U Sec.
T11-CONTROLLER RESETS READY	N/A
T12-CONTROLLER SETS READY (AT B.O.T.)	N/A

*NOTE: This time may be >500 M Sec. if the following occurs:

a. The online signal is deasserted
b. Retry sequence and no data detected
c. At end of the track and turn around or start up

Figure 3-10 Write File Mark Command Timing Diagram



ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N/A
T2-HOST SETS ONLINE	N/A
T3-HOST SETS REQUEST	T2—T3>0 U Sec.
T4-CONTROLLER RESETS READY	T3—T4<1 U Sec.
T5-CONTROLLER SETS READY	20<T4—T5<500 U Sec.*
T6-HOST RESETS REQUEST	T5—T6>0 U Sec.
T7-BUS DATA INVALID	T5—T7>0 U Sec.
T8-CONTROLLER RESETS READY	20<T6—T8<100 U Sec.
T9-CONTROLLER CHANGES DIRC	N/A
T10-1ST DATA BYTE TO BUS	N/A
T11-CONTROLLER SETS READY	N/A
T12-CONTROLLER SETS ACK	T11—T12>70 NANO Sec.
T13-HOST SETS XFER	T12—T13>0 U Sec.

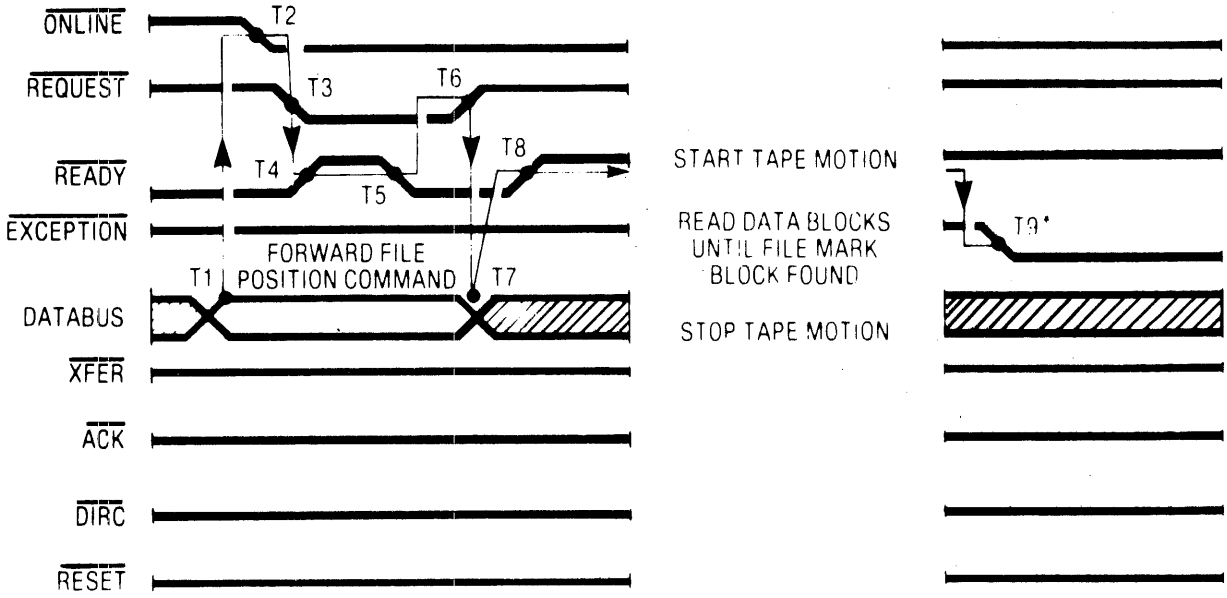
ACTIVITY	CRITICAL TIMING
T14-CONTROLLER RESETS READY	T13—T14<1 U Sec.
T15-CONTROLLER RESETS ACK	0.5<T13—T15<3 U Sec.
T16-BUS DATA INVALID	T13—T16>0 U Sec.
T17-HOST RESETS XFER	T15—T17>0 U Sec.
T18-BUS DATA VALID	
N/A	
T19-CONTROLLER SETS ACK	SAME AS T12
T20-HOST SETS XFER	SAME AS T13
T21-CONTROLLER RESETS ACK	SAME AS T15
T22-BUS DATA INVALID	SAME AS T16
T23-HOST RESETS XFER	SAME AS T17
T24-CONTROLLER SETS READY	N/A
T25-1ST BYTE TO BUS	N/A
T26-CONTROLLER SETS ACK	SAME AS T12

ACTIVITY	CRITICAL TIMING
T27-HOST SETS XFER	SAME AS T18
T28-CONTROLLER RESETS READY	SAME AS T14
T29-CONTROLLER RESETS ACK	SAME AS T15
T30-BUS DATA INVALID	SAME AS T16
T31-HOST RESETS XFER	SAME AS T17
T32-LAST BYTE TO BUS	N/A
T33-CONTROLLER SETS ACK	SAME AS T12
T34-HOST SETS XFER	SAME AS T13
T35-CONTROLLER RESETS ACK	SAME AS T15
T36-BUS DATA INVALID	SAME AS T16
T37-HOST RESETS XFER	SAME AS T17
T38-CONTROLLER SETS EXCEPTION	N/A
T39-CHANGE BUS DIRECTION	N/A

*NOTE: This time may be>500 M Sec. if the following occurs:

a. The online signal is deasserted
b. Retry sequence and no data detected
c. At end of the track or turn around or start up

Figure 3-11 Read Data Command Timing Diagram



ACTIVITY	CRITICAL TIMING
T1-HOST COMMAND TO BUS	N A
T2-HOST SETS ONLINE	T1—T3 > 0 U Sec.
T3-HOST SETS REQUEST	T2—T3 > 0 U Sec.
T4-CONTROLLER RESETS READY	T3—T4 < 1 U Sec.
T5-CONTROLLER SETS READY	20 < T4—T5 < 500 U Sec.**
T6-HOST RESETS REQUEST	T5—T6 > 0 U Sec.
T7-BUS DATA INVALID	T4—T7 > 0 U Sec.
T8-CONTROLLER RESETS READY	20 < T6—T8 < 100 U Sec.
T9-CONTROLLER SETS EXCEPTION	N A

*System must issue read status commmand

**NOTE: This time may be > 500 M Sec. if the following occurs:

a. The online signal is deasserted
b. Retry sequence and no data detected
c. At end of the track and turn around or start up

Figure 3-12 Read File Mark Command Timing Diagram

CHAPTER 4
THEORY OF OPERATION

4.1 OVERVIEW

The Sidewinder is an intelligent Tape Drive. The Tape Drive must be supplied with +24vdc and +5vdc from the host. When power is applied, and/or in response to RESET, the head positioning stepper motor is driven to its calibration point and then back to track 0 position.

The Intelligent Controller in the Sidewinder is microcomputer-based which relieves the host of the overhead functions of tape positioning, tape formatting, and error processing. The intelligent controller also permits eight-bit parallel bi-directional transfer of data. Commands or write data can be transferred from the host to the intelligent controller on the bi-directional data bus. Tape drive status or read data can also be transferred to the host on the bi-directional data bus. In addition to the bi-directional eight-bit data bus, there are four control signals sent to the host and four control signals required from the host. The host supplies on line (ONL-), transfer (XFER-), request (REQ-), and reset (RESET-) to the intelligent controller. The intelligent controller supplies ready (READY-), acknowledge (ACK-), direction (DIRC-), and exception (EXCPT-) to the host. See System Interface, Chapter 3, for command and control signal explanation. The logic diagrams for the Intelligent Tape Drive are provided in figure A3-1.

4.2 DRIVE CONTROL

Drive selection is accomplished with the SELECT, Soft Lock Off or the SELECT, Soft Lock On command. One unit is selected. Drive 0 is automatically selected in the SOFT LOCK OFF state following a power on sequence or a RESET to the drive. Soft Lock enables the operator to avoid inadvertent cartridge removal by controlling the drive select light. In the SELECT, Soft Lock Off state, the drive is selected and the select light will be on only when the tape cartridge is positioned away from BOT. SELECT, Soft Lock On will select the drive and provide a soft cartridge lock. Soft cartridge lock means the front panel LED will remain on regardless of tape position. In either soft lock state, cartridge removal while the select light is on will cause (EXCPT-) to be asserted. In addition, EXCEPTION (EXCPT-) will be asserted when a locked cartridge is removed. Execution of the SELECT command or reset (RESET-) will unlock the cartridge.

Once a drive has been selected, control circuits will cause the capstan motor to move the tape in the direction specified by the command being executed. A processed tachometer signal from the capstan is used by the microcomputer to maintain a constant capstan motor rotation at the selected speed. As the capstan motor rotates, the tape is moved past the read/write head, the capstan, and the tape hole sensors (figure 4-4).

The tape in the tape cartridge is normally opaque because of the oxide coating. However, there are a number of precisely located holes near each end of the tape (figure 4-3). These holes permit light from an LED (light emitting diode) to strike one or both of the light-activated transistors which generate a hole detected signal. These hole detected signals are used by circuits in the LSI Sidewinder to control tape motion, writing on the tape, and reading from the tape. Near the beginning of the tape are three pairs of holes. Each pair consists of an upper and lower tape hole located at 18-inch intervals. The circuits recognize this hole configuration as beginning of tape (BOT). A single upper tape hole between track 0 and track 1 placed 36 inches (DC300XL tapes) or 48 inches (DC600A tapes) beyond BOT marks the tape load point. Writing starts at this point. Near the other end of the tape are four holes. As the tape moves in the forward direction, the next upper tape hole (between track 0 and 1) is the early warning hole. Writing and reading may continue beyond this hole but will stop before the tape reaches the three End Of Tape (EOT) holes that are 48 inches beyond the early warning hole.

Track selection is automatically performed by the drive in such a way as to appear to the host as one long track. Physical track 0 and all even numbered tracks are recorded by the drive in the forward direction. Odd numbered tracks are recorded by the drive in the reverse direction. Read and write operations start at the beginning of the tape on track 0 (logical BOT) after cartridge insertion, reset, power on and following off-line sequence. Under all other circumstances, the read and write operations begin where the previous operation finished.

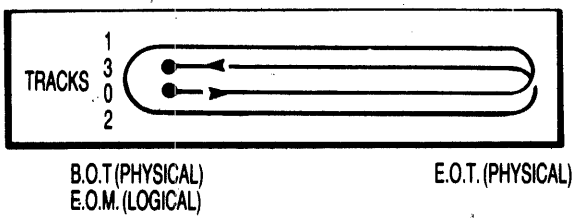
The serpentine recording pattern (figure 4-1) is created by writing track 0 with the lower pair of heads enabled while moving from BOT to EOT. An erase bar which precedes these heads will do a full tape width erase on the first pass, erasing all previously recorded data. When the end of tape holes are reached, the lower pair of heads and the erase bar are disabled and the upper pair of heads is enabled. The capstan motor is reversed and as the tape moves from EOT to BOT, track 1 is written. When the beginning of tape is reached, tape motion is stopped, the head assembly is stepped to the next track pair location and the process is repeated until either four or nine tracks are written, depending on the drive type. The track layout of the Sidewinder allows the nine track, 45/60 MB drive, to read tapes written on a four track, 20/26.7MB drive (figure 4-2).

Commands which will generate a tape positioning operation are BOT, RETENSION, and ERASE. A BOT command will rewind the tape to the BOT holes (figure 4-3) at the beginning of the tape. A RETENSION command will wind the tape to BOT then EOT and back to BOT. The ERASE command is used to erase the entire tape. This command will cause the drive to rewind the tape to BOT, erase from BOT to EOT and then rewind the tape to BOT.

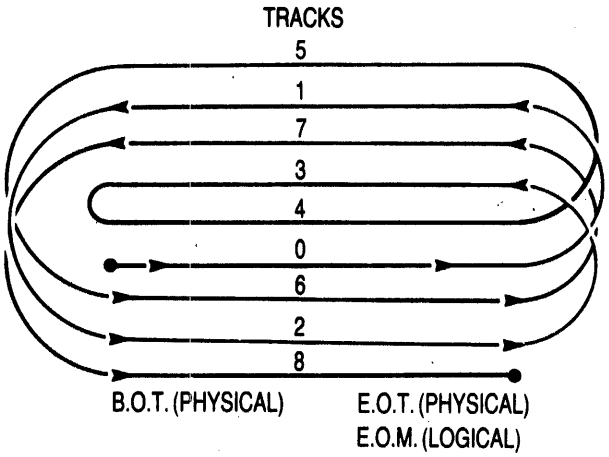
The power circuits provide the +5 vdc, +12 vdc, and +24 vdc for the intelligent Tape Drive.

The clock circuits provide the clock timing for the Intelligent Tape Drive control circuits.

The stepper circuits control the stepper motor that positions the head assembly to a number of positions on the tape. This allows four-track serial recording and nine-track serial recording.



A. Four track recording



B. Nine track recording

Figure 4-1 Serpentine Recording

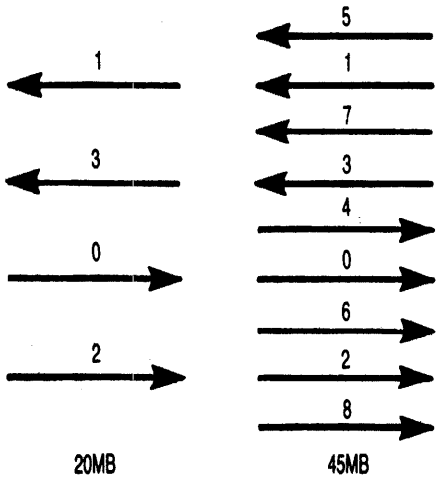
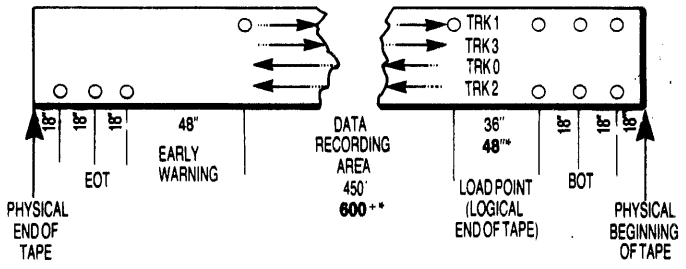


Figure 4-2 Comparative Track Layout



*DC 600A Tape Cartridge

Figure 4-3 Tape Position Holes

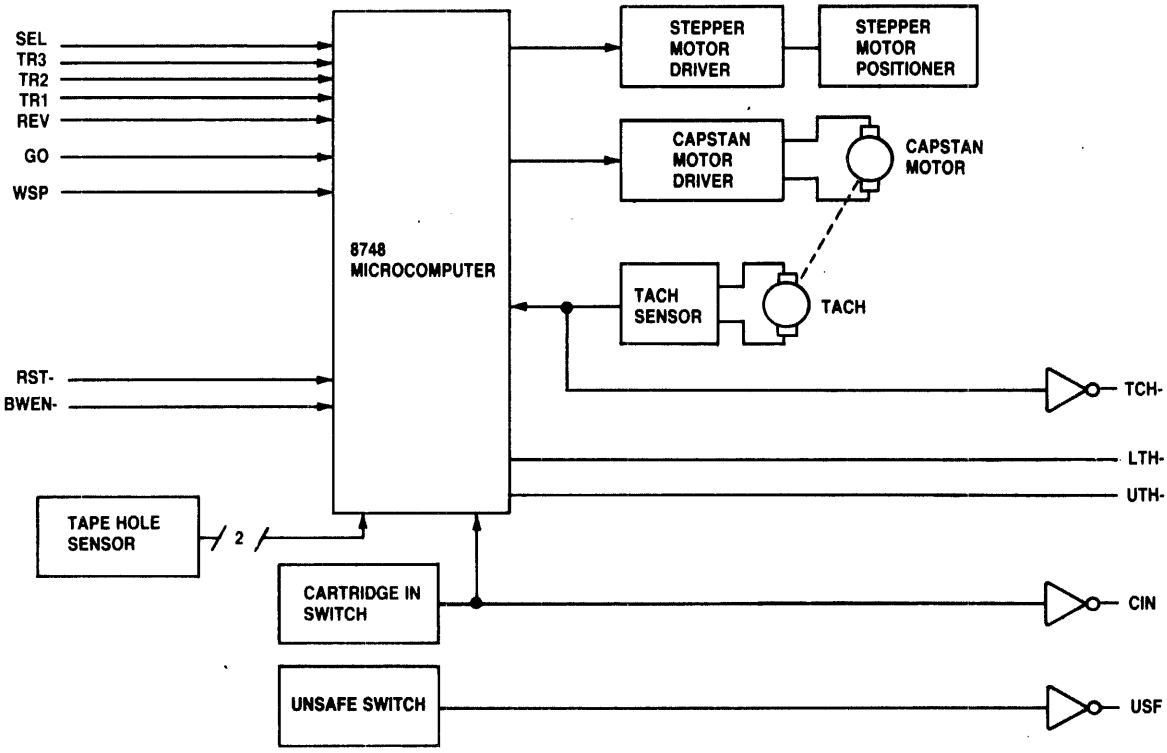


Figure 4-4 Tape Drive Control And Motor Circuits Block Diagram

Under microcomputer control, the capstan motor circuits provide regulation of the capstan speed during all forward and reverse operations of the drive.

The motor driver circuits power the drive motor in the forward direction or the reverse direction.

4.3 DATA TRANSFER CONTROL

Data transfer to and from the tape drive are in 512 byte blocks. The intelligent drive automatically formats each block as it is written on the tape. The 512 byte data blocks are extracted from the formatted data as it is read from tape and sent to the host. Also, the drive automatically performs all error recovery operations

4.3.1 Data Transfer Formats

Each formatted block of data is written after the preceding block. A short preamble (12 to 30 bytes) is written at the beginning of each formatted block. The preamble is an all ones pattern used for read data timing synchronization.

A long preamble (2300 bytes minimum) is written preceding the data block recorded immediately after the load point marker and before the first data block for interchange on all even numbered tracks.

A long preamble (4000 bytes minimum) is recorded before the early warning marker on all odd numbered tracks. A long preamble of 300 bytes is recorded after the early warning mark and before the first data block for interchange on odd tracks.

A long preamble (209 to 722 bytes) will be written when streaming resumes after an underrun or file mark sequence. The preamble will overlap the tail end of a long postamble and then continue until the first data block is dispensed to tape.

The data block marker is one byte, which consists of gap and sync., and is recorded after the preamble to identify the start of the data block.

The block address is one byte in the QIC-11 tape format or four bytes in the QIC-24 format. The block address uniquely identifies each block in a group of 256 blocks in the Archive QIC-11 format. The block address uniquely identifies each block in a group of 1,048,576 blocks in the QIC-24 format. It is used in error correction and tape positioning. The first block on the tape is block 1. Subsequent blocks are numbered sequentially.

The cyclic redundancy check (CRC) is calculated over the 512 bytes of data and the block address. A typical postamble is 0.5 to 2 bytes in length. It is recorded after the CRC and is used as a guard band.

A long postamble (364 to 508 bytes) is written after the last block when streaming is terminated by an underrun, a file mark, or an end of track sequence.

Long postambles and preambles are placed on the tape to compensate for mechanical and electrical properties of the tape or drive, and are invisible to the host.

4.3.2 Write Data Description

Each formatted block of data is written immediately after the preceding block.

A file mark is a unique data block created by the drive. The command may be given in one of two ways.

If the user wishes to write a file mark, a WRITE FILE MARK command is issued. The drive will write a file mark, stop tape motion, and exit write mode. The drive will not rewind the cartridge to BOT.

When the drive is in the write mode the user can also write a file mark by simply de-asserting ON-LINE when READY- is true. The drive will automatically write the file mark, exit write mode, and rewind to BOT.

Assuming the proper control signal protocol is in progress, write may be commanded by the host only under certain conditions. In any case, the drive will verify if the cartridge is in place and not write protected. If the host has not issued SELECT, Soft Lock On or position commands, the drive will default to SELECT, Soft Lock OFF and BOT before writing can begin. One of the conditions under which WRITE can be commanded then, is a write from BOT. Writing after a BOT operation will always record on track zero. Anytime the drive is recording on track zero, the write data will be preceded by a full tape width erase.

WRITE can also be commanded after writing a file to tape and terminating the file with a file mark. The drive will wait at the file mark vicinity until WRITE is commanded and the first block of new data is supplied.

It will begin writing the preamble of the new formatted data before the end of the last file mark postamble.

Writing may also begin following a read operation (Read Data or Read File Mark). In this case the last file written to tape must be located, because the drive is not designed to overwrite previously recorded data. The drive will wait in the vicinity of the last data read, when write is commanded and data blocks supplied writing will commence.

When the end of each track is detected, the blocks of write data remaining in the buffers are written to tape and the next blocks of data are written by the other write head on the next track in the sequence.

To write in the streaming mode, the tape must be in constant motion. For tape motion to be constant, the flow of data from the host must be sufficient to keep the tape drive's buffers full of data. If data transfers from the host are interrupted, an underrun will occur. If the transfer of data from the host are under 90K bytes per second, tape will not stop but the drive may, at intervals, write a duplicate of the preceding data block. The duplicate block is transparent to the host. The purpose of this operation is to keep the tape in motion and to give the host time to supply additional data.

If data from the host falls below 45K bytes per second the drive will respond by writing a second copy of the last block, and then writing an elongated postamble, stopping tape motion, changing direction and positioning back over the already written data. When the data transfers resume, the drive will search for the end of the last block and begin writing.

Underruns should be avoided since the second copy of the last block and the elongated preamble both consume tape. The reposition routine also takes some time, increasing the total backup time.

When a write operation is in process and the early warning hole for the last track is sensed, the drive will stop accepting data from the host at the next block boundary. The drive will finish writing all data blocks contained in the buffers and then raise EXCPT- to the host. In response, the host will read the drive status which will inform the host that the end of media bit has been set.

At this point the host may command the writing of one additional block of data or a file mark before the drive reports that the tape is at the end of media again, after which it may again issue the writing of another data block. This block or blocks of data may be used to describe the file as incomplete.

4.3.3 Read Data Description

When a READ command is given at the beginning of tape, the drive will start tape motion in search of data. If this is the first READ command in the operation, the drive will move the tape to BOT track 0. If no SELECT, Soft Lock On command was issued prior to the read command, the drive will default to SELECT, Soft Lock Off. When the first block has been successfully read, READY- is asserted and data transfers to the host begin. The drive will continue reading and transmitting data to the host until a file mark is encountered. When the drive reads a file mark, the read mode is exited and EXCPT- is asserted. If no data is present on the cartridge, the drive will assert EXCPT- and "No Data Detected" will be set in the status bytes.

When a file has been read from the tape, the host may continue reading by issuing another Read Command. The drive will search for data after the file mark. When the first block has been found, READY- will be asserted and data transfers to the host will begin.

If no data is present beyond the file mark, the drive will assert EXCPT- and "No Data Detected" is reported in the status bytes.

To the tape drive, a READ FILE MARK command is the same as a READ DATA command except that no data is transferred to the host.

The drive reads the tape in search of a file mark. When a file mark is found, EXCPT- is asserted with "file mark found" in the status bytes.

As long as the host can maintain the required data transfer rate, the drive will keep the tape in motion. If something should happen to interrupt the data transfer, the drive will stop tape motion, reverse tape direction, and position over previously read data. This is called a "read underrun". When the host is able to begin transferring data, the drive will start tape motion and continue reading. The repositioning routine generated by the read underruns slow the average throughput.

4.3.4 Error Detection Description

As data is written on the tape, a read-after-write check is performed. Error detection is accomplished by a sixteen-bit CRC character which is appended to the data block and written on tape. If a block is found to have an error, it is rewritten without stopping tape motion. Because the read head follows the write head by 0.3", writing of the block following the block-in-error has already been started. When this block is completed, the block-in-error is rewritten, along with a second iteration of the block following the block-in-error. If this effort is successful, writing continues. The drive will make 16 attempts to write the block-in-error before declaring a hard error. When a hard error occurs, the cartridge is rewound to BOT and EXCPT- is asserted with "Unrecoverable Data Error" in the status bytes.

During a Read operation, the drive verifies each block using the 16-bit CRC character. If either a CRC or block sequence error occurs, the drive will read the next two blocks to see if the block-in-error was rewritten without error. If not, the drive stops the tape, backs up, and tries to read the block-in-error a second time.

The drive will make 16 attempts to re-read a block before declaring a hard error. When a hard error occurs, the drive will stop tape motion, assert EXCPT- with "Unrecoverable Data Error" in the status bytes. After a hard error, the host may continue reading the balance of the tape by issuing a READ command.

Multiple read-retries will cause the controller to set bit 4 of status byte 1 if eight or more retries are required before an error is recovered from a block of data.

4.3.5 Intelligent Data Control

Intelligent data control refers to intelligent control of the data stream as it is processed by the LSI controller during write and read operations. See circuit description in paragraph 5.10 in Chapter 5.

CHAPTER 5
CIRCUIT DESCRIPTIONS

5.1 POWER CIRCUITS

The power circuits are shown in figure A3-1 sheet 3. The capacitors connected between +5 vdc and ground are distributed on the PCB as transient suppressors. Capacitors and a diode are connected between +24 vdc and ground for spike suppression. The +24 vdc supplies regulator, Q20, which provides regulated +12 vdc. Refer to figure A3-1 for distribution and filtering of power circuits.

5.2 POWER UP AND RESET CIRCUITS

The reset circuits are shown in figure A3-1 sheet 1. Reset from the host initializes:

1. The 8031 micro-computer.
2. The 8155 I/O circuit.
3. The LSI Controller.

After about a one-second delay, the 8031 produces a reset pulse to the 8748 microcomputer.

Application of power will produce a reset pulse from the reset circuits. The pulse is ORed through Q2 to the same path taken by host reset, but it also produces an immediate reset to the 8748. If jumper KK is in place, a reset will cause the 8031 to conduct the short Power On Confidence diagnostic test described in Chapter 7.

The reset circuits will also produce a constant reset signal if +24 or +5 volts become unacceptably low, disabling all drive operation.

To the left of the reset input to the microprocessor is the power-up reset pulse generator. In response to the reset pulse, the 8748 microcomputer generates the stepper controls to drive the stepper motor to its calibration stop and back to track zero.

5.3 CLOCK CIRCUITS

The 10.74 megahertz clock generator (top left, figure A-3, sheet 1) consists of crystal, Y1,and one inverter, followed by a buffer. The output is applied to the 8031 microcomputer and a divide by three circuit 3B and 5B. The circuit produces 3.58 MHZ symmetrical outputs. The outputs, CLK and CLK− are sent to the 8748 microcomputer, the erase circuits, and the LSI Controller. The clock signals generate the erase signal when gated to the erase drivers by erase enable. Clock also goes to the LSI controller to control all clocking required by the sequencers and controlling circuits.

5.4 STEPPER CIRCUITS

The stepper circuits are shown in figure A3-1 sheet 3. The stepper phase signals, P15 and P16, are inverted twice to provide four phase signals. In order for these signals to actually agree with the calibration point, they are routed through a sixteen pin jumper block between ICs 7B and 8B. Two shunt clips are inserted onto the pins of the jumper block to select the proper phase signals. The two selected signals are again inverted to generate the four signals required by the stepper motor. The four signals are gated to the stepper motor by STPEN from the microcomputer.

5.5 DRIVE AND TRACK SELECTION CIRCUITS

The drive and track selection circuits are shown in figure A3-1 sheets 3, 4, and 5. Only one drive can be selected. The drive is selected when the SELECT, SOFT LOCK ON or OFF command comes in on the bi-directional bus (A3-1 sheet 2). The command is processed by the 8031 microcomputer. If the drive is powered up and no select command is issued, the drive will default to the SELECT, SOFT LOCK OFF state. This means that the drive is still selected and ready for operation.

In either case the LSI Controller will enable (UNITEN) the output control signals (DIRC-, EXCPT-, ACK-, READY-) through 4J to the host interface. The LSI Controller will also allow the internal processing of input signals from the host bus (HBO thru HB7) and control signals (REQ-, XFER-, ONL-). The PARITY- signal is not used in -1 and -2 models (refer to Table 1-1) of the Sidewinder.

Track selection is controlled by the binary value of internal signals TR0 thru TR3 (9trk) and TR0 thru TR1 (4 trk). These ouputs are determined by the 8031 microcomputer and latched at the 8155 output. The microcomputer takes into consideration such things as RESET, the state of cartridge in switch (CIN-), tape position (logical EOT), and place within the track select sequence. Track selection involves both head positioning and head selection.

Table 5-1 Code Combinations For Track Selection

Track Select Bit	Binary Input Code								
	Track 0	Track 1	Track 2	Track 3	Track 4	Track 5	Track 6	Track 7	Track 8
(LSB) TR0-	0	1	0	1	0	1	0	1	0
TR1-	0	0	1	1	0	0	1	1	0
TR2-	0	0	0	0	1	1	1	1	0
(MSB) TR3-	0	0	0	0	0	0	0	0	1

5.6 CAPSTAN MOTOR CONTROL

The capstan motor control circuits are shown in figure A3-1 sheet 3. These circuits include the REV- and GO- signals, the tachometer circuits, the hole detector circuits, and circuits associated with the write protect switch, and cartridge-in-place switch. These circuits include the divide-by-three counter, 7B. REV- (reverse) and GO- (move tape) are routed to the microcomputer. When REV- is high the tape moves forward; when GO- is high, tape stops. REV- determines which output, P21 (forward) or P20 (reverse), of the microcomputer will be a pulse train. The pulse width in the pulse train determines the energy delivered to the capstan motor. As the pulse train becomes wider, more energy is applied to the motor and it accelerates. As the motor approaches the correct speed, the width of the pulse becomes narrower until both the motor speed and pulse width stabilize at the correct speed. As the capstan motor turns, a tachometer signal is generated by the motor.

Pulse width control is based on the frequency of tachometer pulses sent to the 8748 microcomputer. As the capstan motor turns, a tachometer signal is generated from the motor. After the pulse enters the PCB at J5, RC filtering and differentiator networks in conjunction with inverter 9C shape the pulse for input to the 8031 and 8748 microcomputers.

The ALE output of the 8748 microcomputer is divided by three by the latches at 7B. The 7B output is returned to the 8748 at T1.

The input at T1 is used to count the time between tach pulses and this information is used to determine if the pulse width of P20 or P21 must be altered to control motor speed.

The upper hole and lower hole transistors shown in figure A3-1 sheet 3, generate signals that are used by the microcomputer to identify which portion of the tape is passing the read/write heads. The signals from these photo-transistors are shaped by the operational amplifiers 1OB, to set the latch 8B. After the presence of the hole is recognized by the microcomputer, it generates a signal to reset the latches. When either hole signal is still present at NOR gate 6C, after the latches are reset, the microcomputer presumes that the tape has run off the supply reel and stops the capstan motor. The CIN switch is closed when the cartridge is correctly seated. Inverter 9C produces a low output CIN when the CIN switch is open which inhibits the microcomputer from energizing the capstan motor.

5.7 MOTOR DRIVE CIRCUITS

Figure A3-1, sheet 5 shows the motor driver circuits and their connection to the capstan motor. The motor driver circuit translates a low-frequency pulse train into a higher frequency pulse-modulated motor drive signal. The duty cycle of the higher frequency drive signal is proportional to the input pulse width. The signals SREV and SFWD control the direction and speed of the capstan motor. Only one of these two signals is active at a time. The motor drive circuits also monitor motor current for over-load conditions. Since the logic is the same for both directions, only forward tape motion is described.

The signal SFWD – is output by the 8748 microcomputer. The signal is a constant period square ware of varying negative pulse width. The power applied to the capstan motor is proportional to the negative pulse width. A wider pulse applies more power to the motor and it turns faster. The signal SFWD is applied to 10H, a cross coupled latch. The latch senses which of the two control signals is active (SFWD or SREV) and in this case enables the forward signal path. The 10H cross-coupled latch also disables the reverse signal path. The modulated and translated logic signal which will control the application of power to the capstan motor is channeled into the forward signal path from 10H pin 6. The pulse train flows consecutively through the enabled 11J gate (output pin 3), Q18, motor winding (J8 pin 2), the enabled Q15 transistor, and back to ground through R140. The signal SFWD also goes to 9H. The output is fed through a filter which converts SFWD to a DC voltage that is proportional to the width of SFWD. This voltage is monitored by the comparator 9J. The output is applied to the control input of the timer 8H. This timer performs a frequency translation function. A 5000-Hz square wave is applied to the trigger input of 8H. The output of the timer is a 5K-Hz signal whose duty cycle is proportional to the control voltage applied to 8H. The result of this circuit is a digital signal with a duty cycle that is directly proportional to the width of SFWD (or SREV) but which has a frequency that is about eight times greater (at 90 i.p.s.). The output of 8H is fed through 9H. This digital signal of varying duty cycle is used to switch Q18, applying +24 V to the capstan motor. The output of 9H is also filtered as was SFWD. The resulting DC voltage is fed back to the inverting input of the comparator. This voltage is directly proportional to the duty cycle of the signal at 9H. This allows the higher frequency modulated control signal to be compared to the original modulated control signal, SFWD. If the OUTPUT voltage of comparator 9J is not of sufficient amplitude, then the resulting output voltage of 9H-11 is increased. This resulting voltage is sensed at 9J-6, which then compares it to the positive input, pin 5 of 9J and makes an adjustment to give a correct OUTPUT amplitude at 9J-7. This circuit is a closed loop servo that ensures that the duty cycle of the translated modulated control signal equals the width of SFWD. This circuit is frequency sensitive (tape speed of 30 or 90 i.p.s.). To allow for either speed, the proper resistance value is selectable. The state of HSPD causes current to cease flowing through R105 providing the proper resistance for the filter of the frequency translated signal.

The two remaining circuits are overcurrent circuits. Current is monitored by sensing the voltage across R140. The first comparator, 8J, is a fast reacting circuit. It reacts quickly at a higher current value than the other overcurrent circuit. It is primarily used to prevent too-rapid acceleration of the tape. If this circuit is triggered, its output disables SFWD (or SREV) until current drops to an acceptable limit.

The other overcurrent circuit 9J reacts more slowly and triggers at a lower current value. When triggered, this circuit produces the signal OL-, which goes to the microcomputer. The microcomputer responds by stopping tape motion.

5.8 CONTROL CIRCUITS

5.8.1 Write Circuits

The write circuits are shown in figure A3-1 sheet 4. Before anything can be written to the tape, a number of conditions must be satisfied: the Tape Drive must be selected, the stepper motor must not be enabled, the cartridge write protect cam must be positioned to close the USF switch (figure A3-1 sheet 3), and the appropriate write head must be selected by one of the TRO signals. Transistor Q12 and Q13 form a write current switch. Q14 functions as an AND gate since the USF switch must be closed to provide a ground for its emitter, and T1 must be low to drive the base of Q14 to control base drive to Q13. Q13 controls the +24 volt input to the write head select transistor switches Q12 and Q11. The inverted TRO or TRO- signals will saturate one of the two transistors Q12, Q11 connected to a write head. When TRO- is high, current flows through the write 0 head. When TRO is high, current flows through the write 1 head.

Write enable (BWEN-) from the Intelligent Controller portion of the board enables the complementary write (WDA- and WDA+) signals, when high, to drive transistors Q8 or Q9 through the AND gates at 6C. This signal, when false, also enables the NAND gates at 3D used for read-after-write verify. Diodes CR5 and 6 and CR11 and 12 provide head isolation and protect Q8 and Q9 from switching transients.

The write head zero and the erase head centertaps are wired together. Any time write head zero is selected, a current path is provided for erase current from the erase signal drive circuits. The erase circuits are identical to the write circuits except for input signals. Erase enable (EEN-) replaces write enable, and the complementary clock signals replace the complementary write signals. There is a current control input, high current (HICUR-), that when low, turns on Q10 which causes the current sources Q8 and Q9 to go into a high mode. When HICUR- is high, the current source supplies a lower applied current. This enables the use of two types of tapes which are the DC300XL (lower current), and DC600A (high current).

5.8.2 Read Circuits

The read circuits are shown in figure A3-1 sheet 4. The flow is from the read heads in the upper left corner to amplifiers, 3E, on the right, through the one-shot multivibrators 4B and flip-flops 3C. The read heads are selected, as were the write heads, by TRO and TRO-. The inverted signal at 6D applies a bias voltage to the center-tap of the selected head which forward biases CR3 and CR4 for the read 1 head or CR1 and CR2 for the read 0 head. This action gates the signal read from the selected head to read amplifier 1C. The outputs of 1C, observed at TPL and TPM as a 200 to 600 millivolt pulse, represents a flux reversal which indicates a logical one. The pulses from 1C saturate amplifier 1E in such a manner that it switches with each logical one. The lower comparator, 3E, is a zero threshold comparator that switches on any transition of the input signal. The upper comparator is a 35 percent comparator and so requires a quality signal

to switch. During a read operation the output of the lower comparator creates the read signals. During a write operation the 35 percent comparator must detect the signal for the read-after-write signal to be generated.

The read signal from the zero threshold comparator triggers the top one-shot multivibrator, 4B. At the time out of one-shot 4B, the state of the read signal at 3D is latched by flip-flop 3C. Lower one-shot 4B is triggered by the output of flip-flop 3C and generates the read pulse (RDP). Lower flip-flop, 3C, conditions the exclusive OR gate to trigger the one-shot on the next opposite going transition.

5.9 HOST DATA BUS CIRCUITS

The controller allows eight-bit parallel byte transfer of data from and to the host via the HB0 thru HB7 bi-directional data bus. In addition to the data bus, there are four control signals sent to the host and four control signals required from the host. The host supplies online (ONL-), transfer (XFER-), request (REQ-), and reset (RESET-). The controller supplies ready (READY-), acknowledge (ACK−), direction (DIRC-), and exception (EXCPT-) to the host. The data bus and input and output control interface signals are shown and described in Chapter 3.

All commands from the host, write data from the host, read data to the host, and tape drive status to the host are transferred by the data bus circuits. The data bus circuits are shown in figure A3-1 sheet 2. The eight data bits for each byte pass through the input data buffer 2J to the data bus in the LSI controller when DIRC− is high, enabling 2J. When DIRC− is low, the input data buffer is disconnected from the data bus. When the incoming byte is a command, it is sent to the microcomputer through the LSI controller internal data bus.

5.10 LSI CONTROLLER

The block diagram of the LSI Controller is shown in Figure 5-1. The uP Interface control block controls the interface signals between the microcomputer and the LSI controller chip. The status and control block controls internal functions and stores status regarding those functions. When the data bus input to the LSI Controller is write data, it is sent to the host sequencer. Data flows from the host sequencer to the RAM buffer control in serial form. Under direction of the RAM buffer control, this serial data proceeds out of the LSI Controller as RAMIN data.

The RAMIN data is then stored in the 16K RAM Buffer. From the RAM Buffer, data goes back to the LSI Controller as RAMOUT data where it is processed by the write sequencer. From the write sequencer (WDA, WDA-) it is sent to be written on tape.

During the read mode, read data is taken from the tape and sent to the read sequencer in the LSI controller where it is retrieved from the formatted data stream and stored in the 16K RAM buffer in blocks of 512 bytes of data. From the 16K RAM buffer, the data RAMOUT goes to the host sequencer where it is converted from serial to parallel bytes of data and placed on the 8-bit bi-directional host bus HB0-HB7.

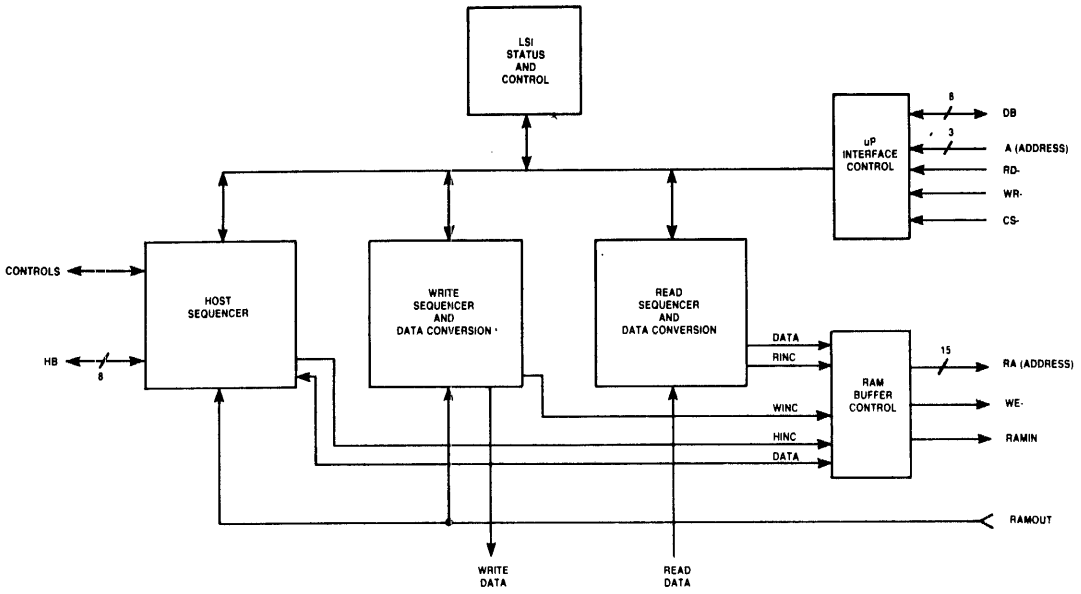


Figure 5-1 LSI Controller Block Diagram

5.10.1 Host Sequencer Circuits

The host sequencer, figure A3-1, sheet 2, controls the flow of read or write data to and from the host. The direction of data flow in the sequencer is dictated by control signal DIR. DIR is false when the sequencer is processing write data and true when the sequencer is processing read data. In the write data mode the sequencer converts parallel bytes of write data into a bit serial stream which it sends to the RAM Buffer Control. In the read data mode the sequencer converts a bit serial stream of data from the 16K RAM buffer to parallel bytes of data. This data is placed on the host bus as read data to the host computer. The sequencer is started by a control byte in the LSI Controller that comes from the microcomputer on the data bus DB0-DB7. Once directed to start by the computer, the host sequencer will independently process a 512 byte block of data. During a read or write transfer, the host sequencer cycles through logic states until all 512 bytes have transferred.

5.10.2 Read Sequencer Circuits

Key circuits which contribute to the operation of the read sequencer are gap detect and no data detected circuits in the LSI Controller and the phase lock loop circuits outside the LSI Controller (see paragraph 5.12).

The gap detect and no data detected circuits monitor all read data entering the LSI controller for an all-ones data pattern (gap), or no data. When a gap is detected, a logic signal is generated and sent to the read sequencer which starts the sequencer. If 12 bit-cell times occur with no data transition, the no-data-detected circuit returns the read sequencer to an idle state.

The read sequencer controls the read data from the tape. The clock supplied to the LSI controller sequencer follows the actual frequency of data as it is read from the tape. The source of this clock is the phase lock loop. The read sequencer remains in the idle state until a gap is detected. When the read sequencer is at idle, the phase lock loop will be synchronized in phase and frequency to the write clock. The write clock is the normal frequency at which the read logic expects to see the data. By synchronizing to this frequency, the phase lock loop will be close to the correct frequency when the actual data enters the circuit. When gap is detected, the sequencer goes to read lock state, causing the phase lock loop to synchronize to the all-ones gap signal off tape for frequency and phase. Now that the read sequencer has detected gap, and the VCO has locked to the read data, the read sequencer looks for a data block marker (sync byte). Once the data block marker has been found, the read sequencer will count the 512 byte record. Once 512 bytes have been counted, the read sequencer allows the block address to be checked by the microcomputer. During the processing of data by the read sequencer, the data is converted from 5-bit run length limited (RLL) code to 4-bit Hex code. The decoded data then will be loaded into the shift register, converted to bit serial form, and sent to the RAM buffers through the RAM Buffer Control. A cyclic redundancy check (CRC) is performed by a CRC checker on all data being read to determine if any errors are in the data.

5.10.3 Write Sequencer Circuits

The write sequencer is controlled by the microcomputer and takes data out of the RAM buffers 1H. The write sequencer data is handled in a bit serial stream and the write sequencer converts 4-bit nibbles to 5-bit GCR encoded data. The controller uses a 4-to-5 RLL (Run Length Limited) code to limit the number of consecutive zeroes in a data stream. In the encoded form, bytes are 10 bits long and nibbles are 5 bits long. Both forms of data must be handled in synchronization with each other. When gap write is enabled by the microcomputer, gap is written from BOT to the load point. The write sequencer is also in the gap write state when write is not enabled. The write sequencer is started by a command from the microcomputer. When the tape comes up to speed, the microcomputer begins looking for the load point. When the load point is detected, the write sequencer goes to the sync write state. Data then begins to flow from the buffers. The write sequencer will stay in the data write state or file mark write state until 512 bytes of data are moved out of the buffers. The block address is then supplied by the microcomputer and placed after the 512 bytes of data. A CRC character is also calculated as the data leaves the buffers and includes the block address. The data is converted from four-bit code to a five-bit code by the data conversion (shift register) circuit before it is written to tape. Also, gap is written between blocks of data and between the early warning hole and EOT.

5.10.4 RAM Buffer Control

Each buffer stores 512 bytes (4096 bits) of data which can become a block of data on the tape or a block of data sent to the host. At the beginning of each block transfer, either into or out of a buffer, the buffer address counter is zeroed. The counter is incremented during loading of data from the host, on a write operation, and to the host on a read operation.

During the write operation, the serial write data is shifted out by the host sequencer, and routed to the RAM buffer control. The RAM buffer control for the block of data being loaded is enabled by the microcomputer. The data is strobed into the selected RAM, advances the address counter, and each bit is loaded sequentially. When one buffer is full, the next buffer is enabled and loaded. After a buffer memory is filled, it is ready to be written to tape. The buffer is unloaded by resetting its address counter and enabling the appropriate RAM buffer control. As the counter counts up from zero, the output bit from each memory location is transferred out as write data into the write sequencer.

During the read operations, the serial read data is routed from the read sequencer to the appropriate buffer. The buffer memory address counters are advanced after each bit is input to the RAM. Each block on the tape fills a buffer. After a buffer is filled, the CRC check is made and the filling of the next buffer is started. A successful CRC check permits transferring the buffer contents to the host. The next buffer is enabled and that buffer's address counter is reset allowing the next block of data to be incrementally transferred.

5.11 BUFFER MEMORY CIRCUITS

The 16K RAM 1H is divided into four buffer memories that are used in both read and write operations. The input (RAMIN) and output (RAMOUT) data used during these operations is controlled by RA00 through RA13 and WE- from the RAM buffer control in the LSI chip.

5.12 PHASE LOCK LOOP AND DATA SEPARATOR

When data is read from magnetic tape moving across a read head, even a signal which was written at constant frequency will vary in frequency as it is read. This is due primarily to tape motor speed instantaneous velocity changes. When NRZ data is read from tape, it is necessary to identify where data bits should be. To do this, a bit cell window is needed. This window must be able to shift to some degree to follow the variation in tape speed and data frequency. The circuit which will produce a clock to define a bit cell window is the phase lock loop. The phase lock loop (PLL) will track the frequency of data as it is read from the tape and identify where the next bit should be. In the PLL, two different comparison circuits are used.

The first comparison circuit is for synchronizing to the write clock so that the read clock will be near the frequency of gap data when the drive is switched to the read mode. When synchronizing to the write clock, a phase and frequency comparison is made. The REF- signal (write clock), figure A3-1, sheet 6, is compared (phase and frequency) at 10F to the phase and frequency of the RD clock signal that the PLL produces. If the PLL signal is faster than the input data (REF-), a signal from 10F, controlled by phase and frequency of the data, will go into filter 7E (sheet 2), through the ladder circuit. The output of filter 7E will cause the control voltage FRQ CONT of the the voltage controlled oscillator (VCO) 7D to be lowered. The VCO produces a VCO1- or VCO2- signal whose frequency can be increased or decreased by increasing or decreasing the FREQ CONT voltage. The VCO1- signal is used with a 30 i.p.s. drive and the VCO2- signal is used with a 90 i.p.s. drive.

The VCO signal is divided by 4F (sheet 6) and becomes the RD Clock produced by the PLL. The clock is constantly compared to the write clock and is adjusted to match it. If the PLL is slower than the input REF- (write check), a signal is generated to speed up the VCO.

The second comparison circuit synchronizes to the read data stream with a circuit that is used to track where the ones are in relation to where they should be. If they are early, the VCO speeds up, if they are late, the VCO slows down. The REF- line to 10F consists of write clock until gap is detected. Once gap is detected, the LSI controller switches the read data stream onto the REF- line. After the VCO has been adjusted to the correct frequency during gap, the read sequencer in the LSI controller causes LOCK (sheet 6) to turn off the output of the first comparison circuit and turn on the output of the second comparison circuit. The second comparison circuit (sheet 6), generates a digital signal (using counter 4F and latch 6F) which is converted to a voltage across ladder circuit LAD0-LAD4 and applied to filter 7E (sheet 2).

The data separator (sheet 6) consists of 2F, 3F, 5F, and 1F. The data separator separates ones and zeroes from the data stream and sends them to the LSI controller. The pulses from the output of 9F-9 are gated through 5F-6 where they preset the first 1F latch. Each data-one pulse will set the latch for one bit-cell time. The bit-cell time is defined by the read clock pulse. The clock is delayed by 2F and input to the first 1F latch. If a data pulse does not occur during a bit-cell time (data zero), the low input at the 1F latch is shifted to the second 1F latch on the next RD CLOCK. When MARGIN, the set input to 3F-4 is high, inputs from the counter circuit are allowed to control the output of 3F producing an input to 5F which limits the bit-cell window to the center 75 percent.

CHAPTER 6
REPAIR PROCEDURES

6.1 SCOPE

The repair procedures in this section include general precautions, removal/ replacement procedures, and retest requirements.

6.2 GENERAL PRECAUTIONS

Before any procedure is performed, ensure power is removed from the drive. Within the drive mechanism, dirt, particulary oxide dust from the tape, degrades the operation of the drive. In all cases, when a drive has been removed from service for repair, the read/write head should be thoroughly cleaned using a lintless cotton swab saturated with 95% isopropyl alcohol. The holes in the hole sensor block should be carefully cleaned. All foreign material in the drive should be removed using a vacuum and a soft bristle brush.

6.3 TOOLS REQUIRED

Required hand tools are listed in Chapter 1, paragraph 1.5. These tools are also called out where used.

6.4 REMOVAL AND REPLACEMENT

It is recommended that the Electronic PCB be removed prior to removing any mechanical assembly from the Drive. Refer to figure A2-1 while performing the following applicable procedures.

6.4.1 Electronic PCB Removal

1. Disconnect all cables that connect the board to the drive mechanism.
2. Remove the two screws with a 3/16-inch nut driver.
3. Carefully remove board by slightly spreading the molded frame and sliding the PCB out of the molded clips near the drive front. Place it in a protective bag or box.

6.4.2 Electronic PCB Replacement

1. Gently lay the Electronic PCB on frame. Slide one side of the PCB into the clip which is part of the frame at the front of the drive. Press the PCB into the clip on the opposite side of the drive by slightly spreading the molded frame.
2. Ensure that cables are routed for easy reconnection.
3. Attach board with two screws using the 3/16-nut driver.
4. Reconnect cables to board.
5. Place stepper motor phase shunts on replacement board in locations identical to the phase shunts on the removed board.
6. See retest chart table 6-1.

Table 6-1 Retest Chart

Replaced Part Description	Retest Procedure
Electronic PCB	All performance tests paragraphs 7.2.1 to 7.2.4
Drive Motor	Read Test paragraph 7.2.3
Sensor Assembly	Basic Operations Paragraph 7.2.2
Carriage Assembly	Read Test Paragraph 7.2.3 Write Test Paragraph 7.2.4

6.4.3. Drive Motor Removal

1. Remove electronic PCB (paragraph 6.4.1).
2. Remove any tie wraps used for drive motor wire routing.
3. Remove tension spring from the post between the motor brackets.
4. If a tie wrap has been placed around the brackets, cut through, remove, and discard the tie wrap at this time. Carefully remove motor by separating the frame just enough to unsnap the motor at its axis on which it is supported.
5. Remove the tension spring from the motor and save for installation with replacement motor.

6.4.4 Drive Motor Replacement

1. Install tension spring saved in paragraph 6.4.3, step 5 on replacement motor.

   CAUTION: Ensure that the white plastic washers are in place on the motor axis supports. Carefully insert motor and bracket by snapping the motor into the frame at the motor axis supports.

2. Reattach the tension spring to the post between the motor brackets.
3. Replace electronics PCB (paragraph 6.4.2).
4. If a tie wrap was removed from around the brackets per paragraph 6.4.3, step 4, snugly install a new tie wrap in the same location.

   CAUTION: Do not distort the brackets by drawing the tie wrap too tight. Ensure the motor pivots freely on its axis after the tie wrap is installed.

5. Install the tie wrap needed for wire routing removed in paragraph 6.4.3, step 2.
6. See retest chart Table 6-1.

6.4.5 Sensor Assembly Removal

1. Remove electronic PCB (paragraph 6.4.1).
2. Remove push-ons securing wires to photo diodes and LED. Note placement and orientation of push-ons for proper replacement.
3. With the use of a 3/16" nut driver*, remove the two screws which secure the sensor assembly to the molded chassis.
4. Carefully remove the assembly.

*This is a special tool. This tool can be made from a common nut driver by having the shaft end ground down so the outside diameter does not exceed 0.28 inches for at least one inch from the shaft end.

6.4.6 Sensor Assembly Replacement (Figure 6-3).

1. Replace by carefully seating assembly in drive.
2. Attach assembly with two screws, but do not tighten them.
3. Reconnect push-ons to diodes and LED.
4. Insert a tape cartridge.
5. Position assembly so the sensor does not touch the cartridge, but clearance is 0.025-in. or less and tighten screws.
6. Replace electronic PCB (paragraph 6.4.2).
7. See retest chart this chapter.

6.4.7 Carriage Assembly Removal

WARNING: This manual does not contain a Carriage Assembly alignment procedure. Removal of this assembly for replacement will require alignment of the replacement assembly by Archive trained service persons. The alignment check in this manual is strictly for checking the existing carriage alignment.

1. Remove electronic PCB (paragraph 6.4.1).
2. Using a 1/4-inch nut driver, remove the three locking screws securing the carriage assembly to frame.
3. Carefully remove carriage assembly from drive.

6.4.8 Carriage Assembly Replacement (Figure 6-4).

1. Carefully place carriage assembly in drive and align mounting holes.
2. Replace the three locking screws (do not tighten), and secure assembly to frame.
3. Replace electronic PCB (paragraph 6.4.2).
4. Alignment of unit is required.
5. See retest chart this chapter.

CHAPTER 7
PERFORMANCE TESTING, CHECKS, AND ADJUSTMENTS

7.1 PERFORMANCE TESTING

Performance testing is of two types: performance testing of suspected tape drives, and performance testing of repaired tape drives. In either type of performance testing, the tape drive should be tested with a known good tape cartridge.

7.2 TESTING SUSPECTED OR REPAIRED DRIVES

Always clean the read/write heads and verify that the sensor block is secure and UTH and LTH holes are not obstructed before testing the tape drive.

It is useful to establish a data pattern for writing to and reading from tape that can be used for the remainder of this chapter, except where otherwise noted. The following data patterns result in a specific number of flux transitions per inch (FTPI), A5, 29, and CF. The optimum write data buffer would be 170 bytes of A5, 170 bytes of 29, and 172 bytes of CF (512 bytes total). A5 represents a one-half frequency (5000 FTPI) whose amplitude, when divided into the full-frequency amplitude of the all ones (at 10000 FTPI) written by the drive during GAP time, provides a resolution ratio. A 29 represents a one-third frequency (3300 FTPI) whose amplitude divided in the full-frequency amplitude of all ones (at 10000 FTPI) also provides a resolution ratio. CF is a worst case data pattern that, combined with a 29 pattern, exercises the unit's ability to accommodate peak shift.

7.2.1 Power On Confidence Test (POC)

The POC test runs diagnostic checks in the controller/formatter portion of the electronics PCB. POC is executed upon power-on or RESET if jumper KK is installed. The following tests are performed:

1. 8031 internal RAM and basic microcomputer instructions.
2. LSI controller chip.
3. 16K RAM chip.
4. Data separator logic.
5. 8155 PIA chip.

Failures detected by POC are reported via diagnostic LEDS (DS2 through DS6). Failures detected by POC are reported to the host by the absence of EXC- for more than 5 seconds.

A successful completion of all POC tests is reported via the diagnostic LEDS by a single blink of all five LEDS following the off period during which the POC tests are performed. Successful completion of all POC tests is reported to the host by the assertion of EXC- within 5 seconds.

Each non-8031 test shall have an associated diagnostic LED as follows:

DS2 LSI controller chip error.
DS3 16K RAM buffer chip error.
DS4 Data separator logic error.
DS5 8155 PIA error.
DS6 not used.

Each time a test fails, the associated diagnostic LED shall be blinked and the test repeated. Continued failure of a given test shall be indicated by a continued blinking of its associated LED. Failure of the 8031 is indicated by unpredictable results.

Refer to the trouble-shooting chart under POC test failure at the end of this chapter if a failure of POC test is indicated.

7.2.2 Basic Operational Checks

These tests address the basic operations criteria of the drive. They require that the drive responds to and executes computer issued commands.

1. Execute a Read Status command without a tape cartridge installed. The unit should respond with No Cartridge and Write Protected.
2. Install an Archive Model 09C Tape Cartridge with Safe indicator positioned to inhibit writing (Safe).
3. Execute a Read Status command. The unit should respond with Cartridge In and Write Protected.
4. Remove the Archive Model 09C Tape Cartridge and rotate the Safe indicator to enable writing.
5. Execute a Read Status command. The unit should respond with Cartridge In and Write Enabled.
6. Execute a Rewind command to position the tape at BOT (Beginning of Tape).
7. Execute an Initialize Cartridge command. The unit will respond by moving tape from BOT to EOT (End of Tape) and a Rewind from EOT to BOT (approximately two minutes).

If the drive will not operate as indicated in steps 1 through 5, refer to problems with Cartridge Not In Place (CNI) or Write Protect (WRP) in the trouble-shooting chart in this chapter. For tape positioning problems encountered in steps 6 and 7, see tape unloads, etc. in the trouble-shooting chart.

7.2.3 Read Test

The read test can be used to detect read problems in suspected drives or to evaluate the read performance of repaired drives.

Using a known good tape generated by a Master Drive (Appendix I), read at least one pass of the entire tape and compare the soft error status to the following limits:

For 1 error in 1 x 10^8 bits, the tables are as follows:

20 MB DRIVE	CUMULATIVE NUMBER OF ERRORS					
Number of Passes	0	1	2	3	4	5
1	A	A	T	T	F	F
2			A	A	T	F
3					A	F

45 MB DRIVE	CUMULATIVE NUMBER OF ERRORS					
Number of Passes	0	2	4	6	8	10
1	A	A	A	T	F	F
2				A	T	F
3					A	A

A = Accept, T = Test, F = Fail

If the tape can be read but has an unacceptable number of retries, then perform the alignment check in this chapter. If the tape cannot be read, refer to Read problems in the trouble-shooting chart in this chapter.

7.2.4 Write Test

The write test can be used to detect write problems in suspected drives or evaluate the write performance of repaired drives. The rate of rewrites should be within those noted next.

NOTE

Due to imperfections in the tape oxide coating, it is not uncommon to encounter soft errors during writing of data to tape. With a known good qualified cartridge, this soft error could approach 400 rewrites for a 20M byte transfer and 900 rewrites for a 45M byte transfer.

Using a tape that is known to be physically a good tape, attempt to write to the tape.

NOTE

Ensure that the write protect cam on the cartridge is in the write position before inserting the cartridge in the tape drive.

If the tape is written on but has an unacceptable number of rewrites, then perform the alignment check in this chapter. If the tape drive cannot write on the tape, recheck the position of the write protect cam and the condition of the tape. If the problem is not with the tape cartridge, refer to the trouble-shooting chart under Write Problems.

7.3 TAPE DRIVE CHECKS

Particular checks of the tape drive are recommended in the course of drive performance testing, referenced by the trouble-shooting chart, or may simply be used as an aid in determining the cause of a problem.

Tape drive checks require the use of test equipment listed in Chapter 1, paragraph 1.5. The test equipment is also called out where used in this chapter.

7.3.1 Checks

There are three mechanical checks: zenith, vertical track position, and azimuth. Zenith is checked with a tool. Vertical track position and azimuth alignment checks each require a special reference tape cartridge.

Proper care of the alignment tapes is an important factor in ensuring reliable alignment checks. The following precautions are essential:

1. Alignment tapes are precision tools and must be handled carefully. Insure proper personnel training and control procedures prior to use.
2. Always keep the alignment tape in a clean container in an area free from magnetic fields (electric motors, transformers, tools, etc.) when not in use.
3. Always cycle alignment tapes from BOT to EOT without stops.
4. Use alignment tapes under controlled temperature conditions (25° ± 3° C)
5. Return alignment tapes to Archive every 6 months or every 200 passes for calibration check.

7.3.1.1 Zenith

The zenith alignment check verifies that the forward (front) face of the read/write head is parallel to the vertical tape path. In other words, zenith is the slope or lean of the read/write head as it addresses the tape. Positive zenith would indicate that the head is sloped backwards from the vertical tape, while negative zenith would indicate that the head is leaning forward into the vertical tape.

1. Insert the Zenith inspection plate and zenith tool (Archive P/N 90003-00X).
2. Place the face of the tool between the two read/write heads.
3. Apply a light pressure to maintain the face of the tool on the face of the head.
4. Verify that the zenith of the read/write head is within ± 15 minutes. (± 1 graduation from center division on the zenith check tool).

CAUTION

Both of the reference tape cartridges required for the following procedures are manufactured by Archive under stringently controlled conditions and are intended for use by Archive trained and qualified personnel under the auspices of a constant calibration and correlation program. The program assures that the integrity of the reference tapes are maintained, since indiscriminate use of these tapes may result in erroneous conclusions regarding the integrity of the alignment checks.

7.3.1.2 Vertical Track Position Check (Figure 7-1).

The objective of the vertical track position check is to verify that the read/write head is properly positioned during the read/write operations.

A Vertical Track Position Reference Tape Cartridge is required. This tape has been written full width with an erase head at 5000 FRPI. The Track Zero position on the tape, with the exception of the first 75 feet, has been erased with a read head. The result is a Track Zero null.

1. Oscilloscope Settings:

   SYNC: INT POS 500NS CH 1

   CHAN 1: AC 100-500MV

   MODE: Channel One Only

   CHAN 1 PROBE: TPO. (Signal is DIFFOUT) GND. TPN

NOTE

Set ground on center graticule. The voltage base is selectable as it will be necessary to adjust the playback observed to full scale.

2. Execute a Reset and Retension command.

NOTE

Model 9045 with firmware -005 and above must have a jumper attached to jumper pin T before a vertical track position check can be accomplished.

3. Set amplitude of playback observed for the first 75 feet (10 seconds for 90 ips, 30 seconds for 30 ips) to eight divisions (maximum vertical deflection).
4. Verify that the output for reading the erased Track Zero is less than 1.2 division (peak to peak) for both the forward and reverse directions in both horizontal and vertical drive mounting positions.

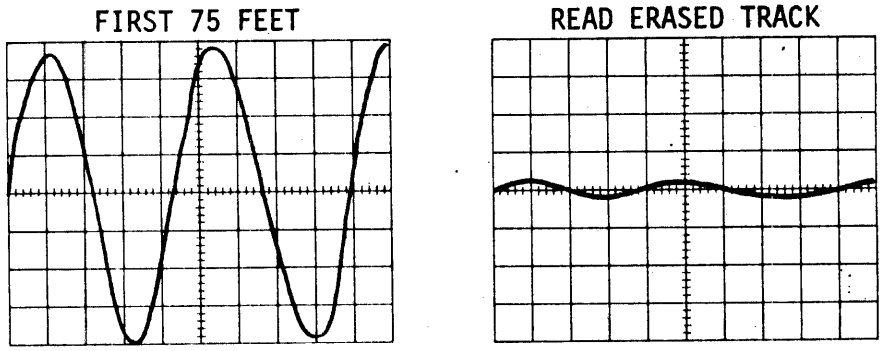


Figure 7-1 Vertical Track Position

7.3.1.3 Azimuth Alignment Check (Figure 7-2)

The azimuth check verifies that the read/write head is perpendicular to the tape path.

An Azimuth Reference Tape is required. This tape has a 15000 FRPI signal recorded on Track Zero only. The rest of the tape has been erased.

The objective of this check is to verify that the read/write head does not have excessive azimuth arc. This is done by verifying that the read head playback amplitude is at, or near, its peak (maximum) and that any movement of the head will result in a decrease in amplitude while reading the azimuth reference tape.

1. Oscilloscope Settings:

   SYNC: INT POS 500NS

   CHAN 1: AC 100-200MV

   MODE: Channel One Only

   CHAN 1 PROBE: TP0 (Signal is DIFFOUT)

   NOTE

   Set ground on control graticule. The voltage base is selectable as it will be required to adjust the observed playback for six divisions peak to peak.

2. Execute a Reset and Retension Command.

NOTE

Model 9045 with firmware -005 and above must have a jumper attached to jumper pin T before a vertical track position can be accomplished.

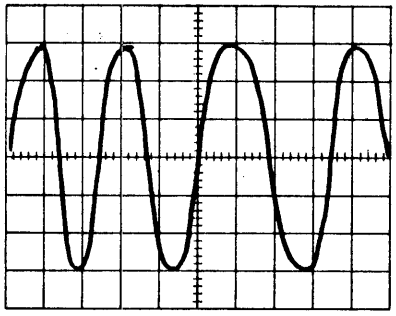


Figure 7-2 Azimuth Alignment Check

3. Apply finger point pressure to the base of the stepper motor at two points, one on each side.
4. Verify that the playback amplitude decreases in all cases.
5. Should the amplitude increase, note and record the point at which pressure on the stepper motor base resulted in the increase, i.e., inside or outside and how much the signal increased.
6. Verify that the increase in amplitude was less than 2-1/2 minor division, zero to peak.

7.3.2 Read Playback Verification Check (Figure 7-3)

Read playback confirms that both read heads (one head for forward tracks and one head for reverse tracks) and the first stage of the read channel respond within specified limits to a particular test signal off tape. The all ones pattern is the highest frequency signal placed on tape as part of a normal format between blocks of data.

This test is performed while monitoring the playback amplitude of the all one's frequency that occurs during the lock time (GAP) between the actual blocks of user data. The frequency of this all one's area is 10000 frpi. Its amplitude is, therefore, the lowest peak-to-peak value of all the possible data patterns/ frequencies.

1. Oscilloscope Settings:

   SYNC: INT POS 50uS CH 1

   CHAN 1: DC 5V

   CHAN 2: AC 500MV

   MODE: Alternate
   CHAN 1 PROBE: TPE. (Signal is LOCK)

   CHAN 2 PROBE: TPL. (Signal is RDAMP)

2. Execute a Read command. Read an adequate number of blocks/bytes to take readings/measurements of the playback amplitude in both directions, i.e, read from both the forward head and the reverse head.

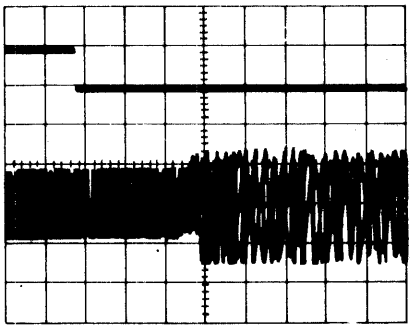


Figure 7-3 Read Playback Verification Signal

3. Verify that the read playback during LOCK is within the following tolerances:

   MODEL 9020L/9045L: 400 to 1100 millivolts in both directions.

   MODEL 3020L: 160 to 440 millivolts in both directions.

4. Note and record the values of the playback amplitudes in both directions.
5. Verify that the amplitudes of each head are within 20 percent of each other, i.e, divide the differences between them by the lesser of the two values and multiply by 100.

If the drive fails to meet these requirements, see Read Problems in the trouble-shooting chart at the end of this chapter. Electrical adjustments cannot be used to correct this problem.

7.3.3 Read Data Pulse Check (Figure 7-4)

The Read data pulse check can be used to verify that the read circuits approximately 1/3 through the read process are producing properly formed read pulses. RDP proceeds from this point to Pin 27 on the LSI Controller on the Electronics PCB.

1. Oscilloscope Settings:

TAPE SPEED:	90 ips	(30 ips)	
SYNC: INT POS	100NS	(200NS)	CH 1
CHAN 1:	AC	1V	
MODE: Channel One Only			
CHAN 1 PROBE: TPS. (Signal is RDP)			

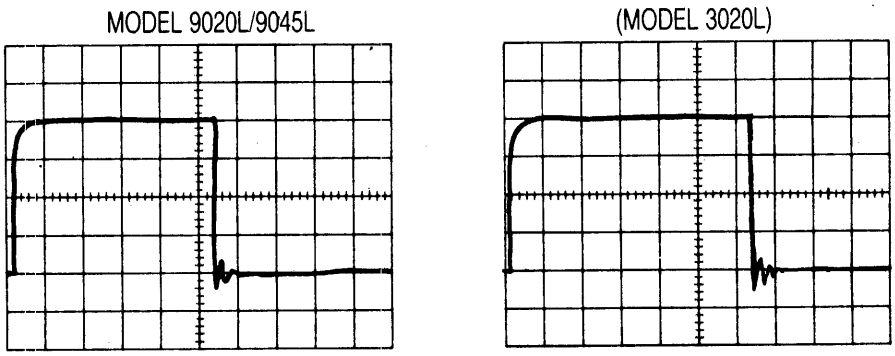


Figure 7-4 Read Data Pulse Check

2. Verify that the timing of the pulse is within the following tolerances:

   MODEL 9020L/9045L: 550 ± 55 nanoseconds.

   MODEL 3020L: 1300 ± 130 nanoseconds.

7.3.4 Peak Shift Check (Figure 7-5)

This procedure verifies that the PLL accommodates peak shift. In order to perform properly, the PLL must receive a good quality read signal and be properly adjusted. The test is performed by monitoring the output of the PLL's DAC. The objective is to verify that the error signals from the DAC do not exceed the requirements while reading a worst case peak shift pattern.

1. Oscilloscope Settings:

   SYNC: INT POS 500uS CH 1

   CHAN 1: DC 5V

   CHAN 2: AC 500MV

   MODE: Alternate:

   CHAN 1 PROBE: TPE. (Signal is LOCK)

   CHAN 2 PROBE: TPF. (Signal is DAC)

   NOTE

   Uncalibrate the time base. Vary the time base to display a LOCK pulse at each end of the screen. The Channel 2 display will then depict one entire 528.5 byte block.

2. If required, execute a Write command with the write buffer data pattern set to the combination of 29 and CF, i.e., 50 bytes of 29, 50 bytes of CF, etc. throughout the buffer. Figure 7-5 is based on A5, 29, CF buffer of approximately 170 bytes each.
3. Execute a Read command of adequate block/byte length to facilitate a reading in both directions.

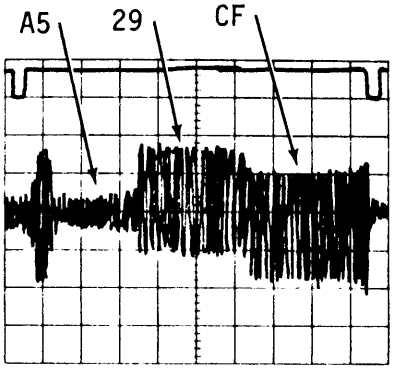


Figure 7-5 Peak Shift Check

4. Verify that the maximum peak-to-peak amplitude achieved by the combination of 29 and CF does not exceed 1700 millivolts (1.7V) in both directions. The measurement is taken from the top of the 29 pattern to the bottom of the CF pattern and excludes or discounts the minute spikes exceeding the body of the waveform.

If the required parameter cannot be met, see Read Problems in the troubleshooting chart at the end of this chapter.

7.3.5 Resolution Check (Figure 7-6)

This procedure verifies the resolution of the read/write heads and is provided as a troubleshooting aid, not a specification check.

The resolution check verifies the ability of the read heads to respond to basic rates of data read from tape. Failure of this test may indicate a worn or faulty head assembly. See Read Problems in the Troubleshooting chart at the end of this chapter to eliminate any other read problems that may interfere with a proper resolution check.

The objective is to measure the playback amplitudes of three frequencies, i.e., 10,000 FRPI, 5,000 FRPI, and 3,300 FRPI.

The 10,000 FRPI is always available under LOCK. The 5,000 FRPI is created by writing a data pattern of A5. The 3,300 FRPI is created by writing a data pattern of 29.

1. Oscilloscope Settings:

   SYNC: INT POS 50uS CH 1

   CHAN 1: DC 5V

   CHAN 2: AC 200MV

   MODE: Alternate

   CHAN 1 PROBE: TPE. (Signal is LOCK)

   CHAN 2 PROBE: TPL. (Signal is RDAMP)

2. If required, execute a Write command writing blocks of data consisting of A5.
3. Execute a Read command. Read and record the amplitude of the gap pattern under LOCK and the amplitude of the first new pattern to the right of the trailing (falling) edge of LOCK.
4. Perform the measurement in both directions.
5. Repeat steps 2, 3, and 4 with a data pattern of 29.
6. Develop the resolution by taking the ratio of each of the lower frequency, higher amplitude signals and dividing them into the high frequency, low amplitude signal. Then multiply by 100 to convert to percentages.

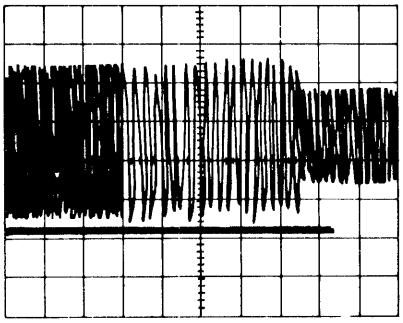


Figure 7-6 Resolution Check

7. Verify that the difference between the heads is less then 20 percent. A typical example is shown as follows:

Amplitude	GAP	A5	29	GAP/A5	GAP/29
Forward	800MV	1300MV	1400MV	61%	57%
Reverse	750MV	1200MV	1300MV	63%	58%
Delta	50/750 =7%	100/1200 =8%	100/1300 =8%		

8. Verify that the amplitude measured and resolutions developed are within the following tolerances:

	MODEL 9020/9045L	MODEL 3020L
AMPLITUDES:		
GAP	400-1100MV	160-440MV
A5	725-1570MV	290-625MV
29	850-1690MV	340-675MV
RESOLUTIONS:		
GAP/A5	53 to 85%	
GAP/29	47 to 65%	

7.3.6 Capstan Motor Noise Check (Figure 7-7)

This procedure verifies that the tape is being erased and that the capstan motor does not create excessive noise. The test is performed by reading an erased tape and monitoring the output of the differentiator for excessive noise spikes.

1. Execute an Erase command. The unit will move tape from BOT to EOT while it performs a full tape width erase. The unit will then move tape back to EOT (about two minutes).

2. Oscilloscope Settings:

TAPE SPEED:	90 ips	(30 ips)	
SYNC: INT NEG	1MS	(500uS)	CH 1
CHAN 1:	DC	2V	
CHAN 2:	AC	200MV	

MODE: Alternate

CHAN 1 PROBE: 9C pin 6. (Signal is TACH)

CHAN 2 PROBE: TP0. (Signal is DIFFOUT)

NOTE

The MODEL 9020/9045L will display 7 pulses at intervals of 1.62 ms
The MODEL 3020L will display 5 pulses at intervals of 500 ms.

3. Execute a RETENSION command. The unit will move tape from BOT to EOT and back to BOT (approximately two minutes).
4. Uncalibrate the time base. Vary the time base to display eight pulses across the screen, i.e., one revolution of the capstan motor.

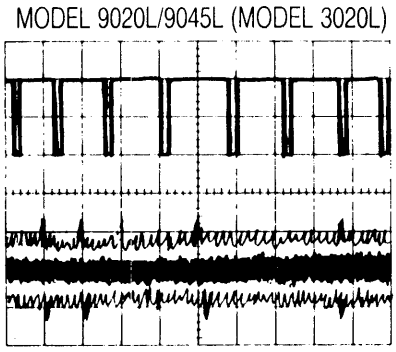


Figure 7-7 Capstan Motor Noise Check

5. Verify that the noise spikes do not exceed ± 250 millivolts peak (500mv peak-to-peak). The noise spikes will be asynchronous with the tachometer pulses.
6. Failure of this test may indicate a faulty erase circuit on the electronics PCB or a noisy capstan motor.

7.3.7 Capstan Motor Speed Variation Check (Figure 7-8)

This procedure verifies that the capstan motor is under the control of the microcomputer and does not exhibit excessive speed variation. This test is performed by monitoring the tachometer pulses to the microcomputer during the execution of a Motion command.

1. Oscilloscope Settings:

TAPE SPEED:	90 ips	(30 ips)	
SYNC: INT NEG	100uS	(200NS)	CH 1
CHAN 1:	DC	2V	

MODE: Channel One Only

CHAN 1 PROBE: 9C pin 6. (Signal is TACH)

2. Execute a Write command. Write from Beginning of Media (BOM) to End of Media (EOM). At the conclusion of the Write, ensure that a File Mark is written.
3. Horizontally position the second negative pulse on the center vertical graticule and magnify the display times ten (10X).

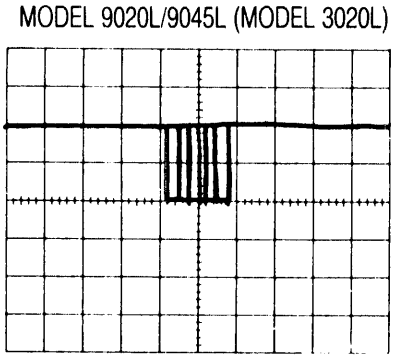


Figure 7-8 Capstan Motor Speed Variation

4. Verify the total "jitter" does not exceed six vertical graticules (± 3 Major Divisions) for the entire length of the tape in both directions.
5. At the conclusion of the Write sequence, note and record the following:

   Total number of Blocks/Bytes Written

   Total number of Blocks/Bytes Rewritten

NOTE

The number of blocks rewritten is provided via the read status data. The number of blocks rewritten divided by two equals the actual number of rewrites that occurr. Verify that the number of rewrites does not exceed 100.

CAUTION

If a motor speed problem is indicated, it could be due to using a faulty tape cartridge. If the tape cartridge is good, failure of this check may indicate faulty motor control and drive circuits on the Electronics PCB or a faulty capstan motor.

7.4 ELECTRICAL ADJUSTMENTS

The electrical adjustments ensure the proper setup of the read system on the Electronic PCB. Head alignment check is not necessary before performing these procedures. Because these adjustments are interactive, all adjustments in the procedure must be checked and in the order given. The first adjustment requires that power is applied to the drive, a good tape cartridge is installed, and that the drive respond to a WRITE command from the host computer. All other adjustments require only that power be applied to the drive.

The following adjustment procedures verify four potentiometer settings.

7.4.1 Read Amplifier Gain Adjust (R10) (Figure 7-9)

This procedure is a verification of the write and read operation of the tape drive. This test is performed by monitoring the waveform output at TP0. This test may require adjusting potentiometer R10 to bring the signal within tolerance.

1. Oscilloscope Settings:

   SWEEP TIME: 2 uSEC

   MODE: Channel One

   CHAN 1: 1 VOLT/DIV.

   CHAN 1 PROBE: TP0 and GND.

2. Input a pattern of Hex 29 to the tape drive from the host and write forward on Track 0.
3. Verify that the waveform is −9V below centerline as shown in figure 7-9.

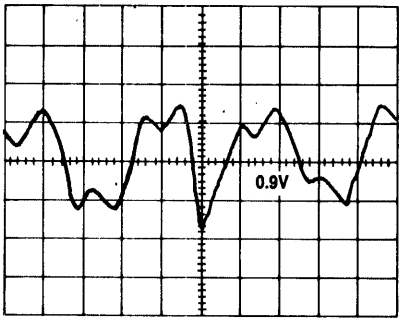


Figure 7-9 Read Amplifier Gain Adjustment

NOTE

All adjustments should be done on a read only for the lowest of the 2 head outputs.

4. Adjust potentiometer R10 as required. Verify waveform adjusts to 0.9V for the second overshoot on the signal.
5. Select Track 1 and Write Reverse.
6. Observe waveform and adjust R10 as required for 0.9V above and below centerline on scope.

7.4.2 Differentiator Symmetry/Balance (R15) (Figure 7-10)

This check is a verification of the symmetrical balance of the differentiator. The test is performed by monitoring the Read Data Pulse (RDP) at TP S on the circuit board. This test requires turning potentiometer R15 in both directions to verify the adjustment.

1. Oscilloscope Settings:

TAPE SPEED:	90 ips	(30 ips)	
SYNC: INT POS	200NS	(500NS)	CH 1
CHAN 1:	AC	1V	

MODE: Channel One Only

CHAN 1 PROBE: TPS. (Signal is RDP)

NOTE

Set ground on the center horizontal graticule.

2. Adjust the R15 potentiometer in both directions and verify that the signal waveform is at its maximum negative position/level.

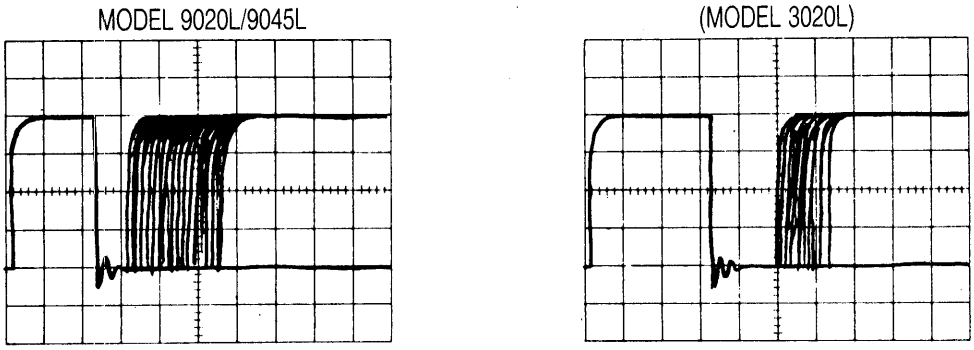


Figure 7-10 Differentiator Symmetry/Balance

7.4.3 Phase Lock Loop Gain (R36) (Figure 7-11)

This procedure verifies the gain setting of the Phase Lock Loop (PLL). The test is performed by monitoring the Read Clock at TP8 and injecting a calibration signal into the PLL. The adjustment is made via the R36 potentiometer located on the front of the controller.

1. Select the Drive.
2. Jumper the pins on the C jumper block. The C jumper block is located on the left side of the PCB about 1/3 of the distance to the rear of the board.
3. Oscilloscope Settings:

TAPE SPEED:	90 ips	(30 ips)	
SYNC: INT POS	100NS	(200NS)	CH 1
CHAN 1:	DC	1V	

MODE: Channel One Only

CHAN 1 PROBE: TPD. (Signal is RDCLK)

NOTE

Uncalibrate the time base. Vary the time base to display one entire cycle, including all the "jitter," over 9 major divisions on the screen (Figure 7-11).

4. Horizontally position the leading edge on the first left hand graticule and verify that the entire signal with all of its "jitter" is displayed (Figure 7-11).

5. Verify that the leading edge of the second pulse is within the following tolerances:

   MODEL 9020L/9045: 1.3 ± .1 major divisions.
   MODEL 3020L: .94 ± .1 major divisions.

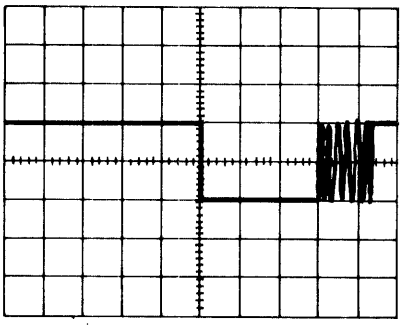


Figure 7-11 Phase Lock Loop Gain

NOTE

Vary the hold-off of the scope for assurance of a correct reading.

6. Adjust R36 as required. Adjust by turning the potentiometer one turn at a time. The entire signal is displayed by manipulating the horizontal position to locate the leading edge and the time base for the last of the second set of leading (rising) edges.
7. Remove the jumper clip from the C jumper block after the check/adjustment is completed.

7.4.4 Phase Lock Loop Balance (R35) (Figure 7-12)

This check is a verification of the Phase Lock Loop (PLL) Balance. The check is performed by monitoring the output of the digital to analog converter (DAC) at TPF while the drive is either reading or writing. TPF is located near the center of the Electronics PCB.

The adjustment is made via the R35 potentiometer. R35 is the second potentiometer mounted to the right of R36, which is located at the front of the PCB.

1. Oscilloscope Settings:

   SYNC: INT POS 50uS CH 1

   CHAN 1: DC 5V

   CHAN 2: AC 100MV

   MODE: Alternate

   CHAN 1 PROBE: TPE. (Signal is LOCK)

   CHAN 2 PROBE: TPF. (Signal is DAC)

2. Execute a Read command. Read an adequate number of blocks to ensure readings/measurements in both directions, i.e., read from both the forward head and reverse head.

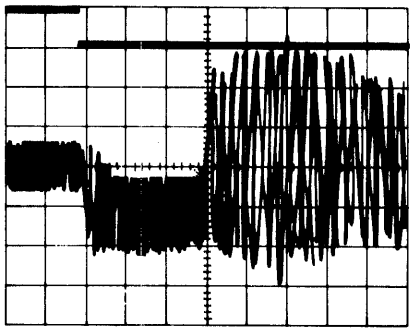


Figure 7-12 Phase Lock Loop Balance

3. Verify that the second level is negative with respect to the first level and that the difference between them is 100 millivolts (0.1V) as measured through the center of the "fuzz."

4. Adjust R35 to set the difference between the two levels at 100 millivolts (0.1V).

7.5 TROUBLE-SHOOTING CHART

The trouble-shooting chart is based upon discrepancies in performance and probable causes limited to identifying possible difficulties at the major subassembly level. All internal connections should be checked for security. The drive should also be checked for any visible damage and the R/W head cleaned.

Trouble-Shooting Chart

Symptom	Check	Probable Cause
Drive will not respond	+5 and +24 vdc on Electronics PCB at J2.	1. No power from host 2. Power to J2 disconnected. 3. Short in Electronics PCB
POC Test failure	POC TEST paragraph 7.2.1	1. Electronics PCB
Basic Operations Problems	Basic Operations test paragraph 7.2.2, steps 1 to 5.	
1. Problems with Cartridge Not In Place (CIN) or Write Protected (WRP)	Check by substituting a known good electronics PCB	
	a. Drive tests pass b. Drive test fails	1. Electronics PCB 2. Defective switch
2. Tape Positioning Problems	Basic Operations test paragraph 7.2.2	
a. No tape motion	With power applied, short test point T and push the cartridge-in switch.	
	1. Capstan motor turns 2. Motor does not turn	1. Replace Electronics PCB 2. Go to next check
	Disconnect the existing motor and externally connect a good motor. Short test point T and push the cartridge-in switch.	
	1. Motor drives 2. Motor does not drive (remove short from test point T after check)	1. Replace capstan motor 2. Replace Electronics PCB
b. Tape winds off the reel or tape sheers	Check for obstructed tape holes	Dirty tape holes
	Check by substituting a known good Electronics PCB. Perform steps 6 & 7 of the test in paragraph 7.2.2.	
	1. Test above passes 2. Test above fails	1. Replace Electronics PCB 2. Replace LED Sensor Assembly

Trouble-Shooting Chart (Continued)

Symptom	Check	Probable Cause
Read problems	Read Test, paragraph 7.2.3	
1. Will not read	Check by substituting a known good Electronics PCB	
	1. Drive tests pass	1. Replace Electronics PCB
	2. Drive tests fail	2. See other read checks
2. Will not read due to improper head position	Remove cartridge and watch head calibration movement on reset or power up.	
	1. Head does not move	1. Carriage Assembly or Stepper Assembly 2. Loose phase clip
3. Will read, but with an unacceptable number of retries	Double check the quality of the tape in use	Faulty tape cartridge
	Check head alignment Paragraph 7.3.1	Head alignment
	Check read system adjustments	Read system adjustment Paragraph 7.4
	If all other read checks fail to identify the problem, perform Resolution Check, paragraph 7.3.5	
	1. Check fails	1. Replace carriage assembly
Write problems	Write Test, Paragraph 7.2.4	
1. Does not write or has an unacceptable number of rewrites.	Substitute a good Electronics PCB	
	1. Drive test passes	1. Replace Electronics PCB.
	2. Drive test fails	2. See other write checks
	Verify that track and azimuth alignment is correct	Track and azimuth alignment checks Paragraphs 7.3.1.2 and 7.3.1.3
	Double check the quality of the tape cartridge used for the write test	Faulty Cartridge
	Failure of the above checks to identify the problem indicates a possible Carriage Assembly problem (Write head failure)	Carriage Assembly

NOTE

When replacement of Electronics PCB is necessary, electrical adjustments must be performed.

APPENDIX I
MASTER DRIVE

A1.1 PURPOSE

A Master Drive is frequently maintained by users and distributors as a secondary standard. This Master Drive is used to check the quality of tapes written by drives which are in daily use in the field. Specifically, this drive may be used to create software distribution tapes or to create test tape used for product verification. This appendix contains information to be used by a trained maintenance person and is intended to ensure the viability of the Master Drive as a standard.

A1.2 MASTER DRIVE CLEANING

Perform the following cleaning procedures on the Master Drive after every 10 hours of use. Clean the drive after each new tape is used or, if all new tapes are being used, clean after every two hours.

CAUTION

Do not use hard chemicals or soaps to clean the head.

1. Clean the read/write head using a clean, lintless cotton swab saturated with 95% isopropyl alcohol. Be sure to remove all visible oxide.
2. Using alcohol dampened swab, clean the tape hole detector opening.
3. Using alcohol dampened swab, wipe all dust and debris out of the tape cartridge cavity.

A1.3 MASTER DRIVE VERIFICATION

On a scheduled basis, perform the alignment and adjustment procedure in Chapter 7 using the special tools listed to verify the quality of the Master Drive. Archive Corp. will train personnel to effectively use these procedures.

CAUTION

Extreme caution should be exercised when performing the procedures in Chapter 7 on the Master Drive. Insure all personnel are properly trained and that adequate controls are in place prior to using the alignment and adjustment procedures.

APPENDIX II
PARTS LISTS

A2.1 SCOPE

This Appendix contains the parts lists and parts location diagrams for the LSI Sidewinder Intelligent Drive.

Table A2-1 LSI Sidewinder Parts List

Item (Fig. A2-1 & A2-2)	Part Number	Description	Qty	Usage Code (1)
1	20406-XXX	Electronic PCB 3020L-1	1	A
1	20406-XXX	Electronic PCB 3020L-2	1	B
1	20407-XXX	Electronic PCB 9020L-1	1	C
1	20407-XXX	Electronic PCB 9020L-2	1	D
1	20408-XXX	Electronic PCB 9045L-1	1	E
1	20408-XXX	Electronic PCB 9045L-2	1	F
2	20405-001	Filter PCB	1	C, D, E, F (3)
2	20405-002	Filter PCB	1	A, B (3)
3	80174-XXX	EPROM QIC-11	1	A, C, E (2)
3	80182-XXX	EPROM QIC-24/11	1	B, D, F (2)
4	20017-006	Carriage Assy	1	A, B, C, D
4	80169-001	Carriage Assy	1	E, F
5	20026-002	Sensor Assy	1	
6	20137-002	Drive Motor Assy	1	

Notes:

1. The Usage Code column contains codes which indicate that a part or assembly is used with a particular model of tape drive. See list below:
   A—Model 3020L-1
   B—Model 3020L-2
   C—Model 9020L-1
   D—Model 9020L-2
   E—Model 9045L-1
   F—Model 9045L-2
2. The EPROM is a separately ordered part and is required to complete an Electronic PCB assembly.
3. The Filter PCB is a separately ordered part and is required to complete an Electronic PCB assembly.

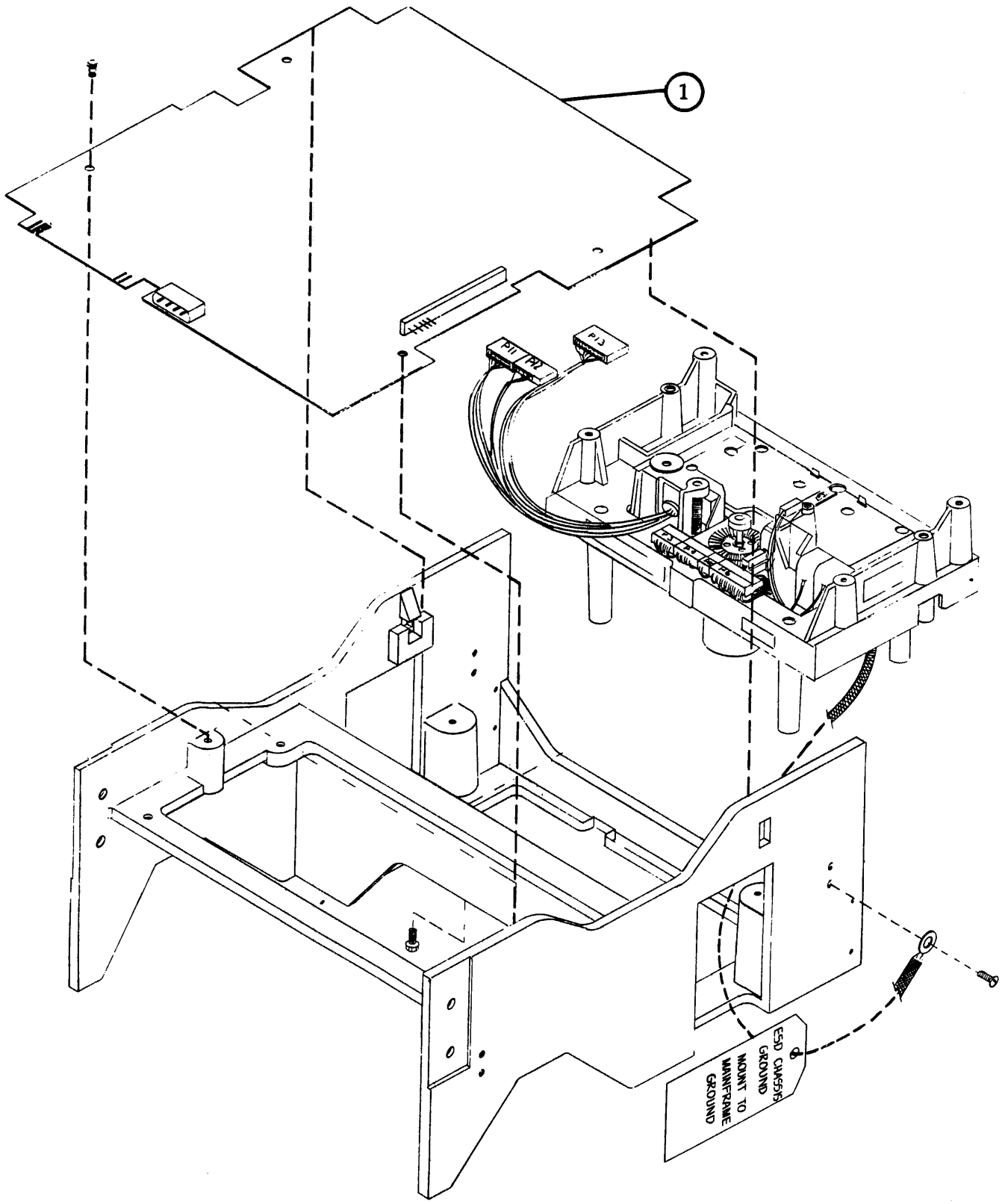


Figure A2-1 LSI Sidewinder Parts Location (Sheet 1 of 2)

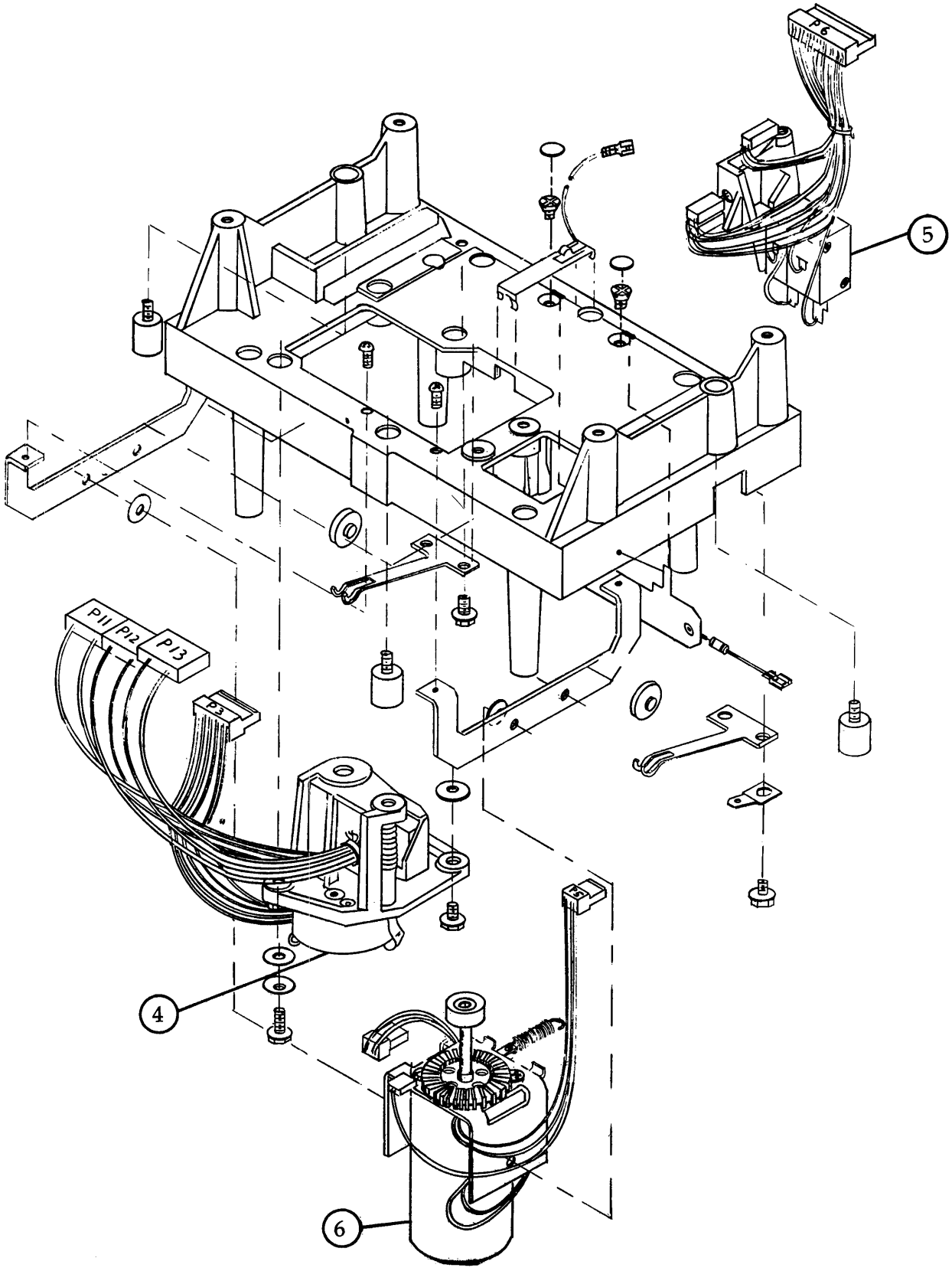


Figure A2-1 LSI Sidewinder Parts Location (Sheet 2 of 2)

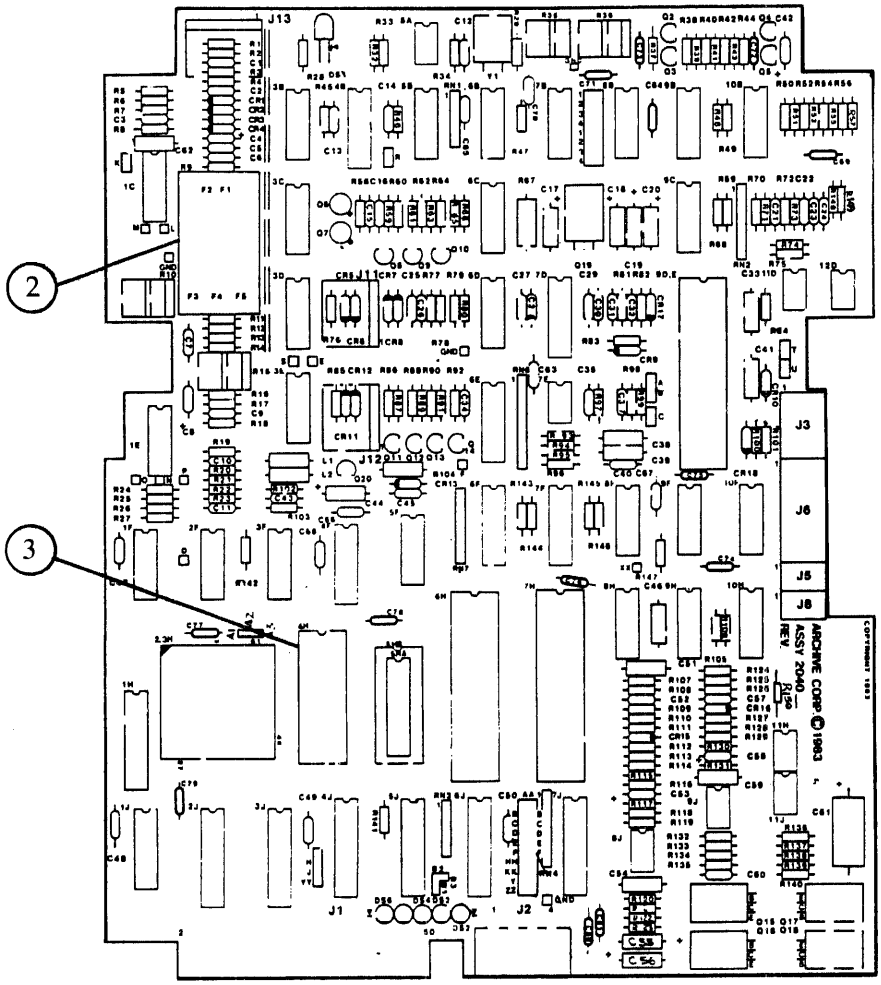


Figure A2-2 Electronic PCB Parts Location

Table A2-2 Electronic PCB Parts List

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR	USAGE CODE
20406-006	ASSY PCB 3020L-1	1 EA	(1)	A
20406-007	ASSY PCB 3020L-2	1 EA	(1)	B
20407-006	ASSY PCB 9020L-1	1 EA	(1)	C
20407-007	ASSY PCB 9020L-2	1 EA	(1)	D
20408-006	ASSY PCB 9045L-1	1 EA	(1)	E
20408-007	ASSY PCB 9045L-2	1 EA	(1)	F
15816-001	CLIP, JUMPER #DC25-100-2-T	6 EA		
17308-001	MICROCOMPUTER, 8031	1 EA	6F	
20183-003	MICROCOMPUTER, 8048	1 EA	90,9E	
20200-102	LSI, CONTROLLER	1 EA	2-3H	A, C, E
20461-002	LSI Q24 CONTROLLER	1 EA	2-3H	B, D, F
20220-009	ASSY S/W PCB W/DISCRETE PLL	1 EA		
14400-001	TAPE, DBL COATED POLORETHANE	1 FT	(1)Y1 Q15-19	
15500-068	CAP., CER. 5% 50V 6.8PF	2 EA	(1)C12,C28	
15500-101	CAP., CER. NPO 5% 50V 100PF	4 EA	(1)C71-74	
15500-152	CAP. CER.5% 50V 1500PF	1 EA	C38	
15500-200	CAP., CER. NPO 5% 50V 20PF	1 EA	(1)C25	
15500-221	CAP., CER. NPO 5% 50V 220PF	2 EA	(1)C13,C14	
15500-240	CAP., CER. 5% 50V 24PF	2 EA	(1)C29,C70	
15500-272	CAP., CER. 5% 50V 2700PF	1 EA	(1)C62	
15500-301	CAP., CER. NPO 5% 50V 300PF	2 EA	(1)C40,C3	
15500-330	CAP., CER. NPO 5% 50V 33PF	1 EA	(1)C10	
15500-472	CAP., CER. 5% 50V 4700PF	2 EA	C46,51	
15500-822	CAP., CER. 5% 50V 8200PF	1 EA	(1)C39	
15501-106	CAP., TANT. 20% 10V 10UF	2 EA	(1)C53,C58	
15501-225	CAP., TANT. 20% 10V 2.2UF	1 EA	(1)C42	
15501-226	CAP., TANT. 20% 10V 22UF	3 EA	(1)C19,C20 C55	
15501-475	CAP., TANT. 20% 10V 4.7UF	1 EA	(1)C17	
15502-685	CAP., TANT. 20% 4V 6.8UF	2 EA	(1)C4,C8	
15503-475	CAP., TANT. 20% 35V 4.7UF	2 EA	(1)C18,C56	
15504-225	CAP., TANT. 20% 20V 2.2UF	1 EA	(1)C44	
15505-104	CAP., CER. Z50 50V .1UF	31 EA	(1)C1,C2 C5-7,C9 C11,C15 C16,C32 C34,C35 C43,C45 C47-50 C52-C60 C64-68 C75-81	
15506-102	CAP., CER. X7R 10% 50V 0.001UF	4 EA	(1)C21-24	
15506-103	CAP, CER X7R 10% 50V .01UF	5 EA	(1)C27,C30 C31,C63 C69	

Table A2-2 Electronic PCB Parts List (Continued)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR
15506-104	CAP., CER. X7R 10% 50V 0.1UF	2 EA	(3)C33,C41
15506-183	CAP., CER. X7R 10% 50V .018UF	2 EA	(3)C54,C57
15506-473	CAP., CER. X7R 10% 50V 0.047UF	1 EA	(1)C59
15507-107	CAP., ELECTROLYTIC 100UF	1 EA	(1)C61
15809-024	HEADER, #640099-4	1 EA	(1)J3,J5 J6,J8
15810-006	PIN, .025 SQUARE TIN	36 EA	(1)A(2) A1,A2,A3 B,B1,B2 B3,C(2),D, E,F,H,J K(2),L,M, N,O,P, K(2),S, T(2),U(2), XX,YY, GND(4)
15810-007	PIN, .025 SQUARE SEL GOLD	5 EA	(1)F1-5
15815-016	SOCKET, I.C. 16 PIN DIP	1 EA	(1)1J
15815-020	SOCKET, 20 PIN	1 EA	(1)1H
15815-028	SOCKET, I.C., 28 PIN	1 EA	(1)4H
15815-040	SOCKET, I.C. 40 PIN DIP	3 EA	(1)6H,7H, 9D-E
15817-007	WAFER, RGT ANG #22-12-2071	2 EA	(1)J11,J12
15817-008	WAFER, RFT ANG #22-12-2081	1 EA	(1)J13
15818-016	HEADER, DOUBLE ROW, STRAIGHT	1 EA	(1)7B,8B
15818-020	HEADER, DOUBLE ROW, STRAIGHT	1 EA	(1)
15833-001	CONNECTOR, AMP 641737-1	1 EA	(1)J2 (POWER)
15842-001	I.C.SOCKET, 68 PIN	1 EA	2,3H
15846-024	SOCKET, 24 PIN	1 EA	
16000-004	CRYSTAL, 10.7386 MHZ	1 EA	(1)Y1
16100-001	DIODE, IN4150	16 EA	(1)CR1-12 CR15-18
16103-001	DIODE, IN4001	1 EA	(1)CR13
16401-106	INDUCTOR, MOLDED 10% 10UH	2 EA	(1)L1,L2
16500-001	I.C., 74S240	3 EA	(1)3J 4J, 6J
16502-001	I.C., 74LSO4	1 EA	(1)9B
16503-001	I.C., 7406	1 EA	(1)6D
16508-001	I.C., 74LSO2	1 EA	(1)8B
16509-001	I.C., 74LS74	2 EA	(1)3C,7B

Table A2-2 Electronic PCB Parts List (Continued)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR
16510-001	I.C., LM339	1 EA	(1)10B
16511-001	I.C., UA78L12 AWC	1 EA	(1)Q20
16512-001	I.C., 75451B	1 EA	(1)5A
16513-001	I.C., 9602	1 EA	(1)4B
16515-001	I.C., LM319	1 EA	(1)3E
16516-001	I.C., NE592A	2 EA	(1)1C,1E
16517-001	I.C., 74LS00	2 EA	(1)3D,10H
16521-001	I.C., 74LS14	1 EA	(1)2F
16539-001	I.C., 4044	1 EA	(1)10F
16548-001	I.C., 74LS240	2 EA	(1)2J,5J
16551-001	I.C., 74LS373	1 EA	(1)5H
16555-001	I.C., 74S74	4 EA	(1)1F 3F,5B,9F
16556-001	I.C., 74S00	1 EA	(1)5F
16557-001	I.C., 74S04	1 EA	8F
16558-001	I.C., 74S163	1 EA	(1)4F
16559-001	I.C., 74S174	1 EA	(1)6F
16560-001	I.C., 74S124	1 EA	(1)7D
16561-001	I.C., LF353	1 EA	(1)7E
16562-001	I.C., CD4502	2 EA	(1)6E,7F
16564-001	I.C., LM2904	2 EA	(1)8J,9J
16565-001	I.C., 74LS136	1 EA	(1)9H
16569-001	I.C., NE556	1 EA	(1)8H
16570-001	I.C., 75477	2 EA	(1)11D,12D
16571-001	I.C., 74HC14	1 EA	(1)9C
16572-001	I.C., 2167-3	1 EA	(1)1H
16573-001	I.C., TL78005	1 EA	(1)Q19
16575-001	I.C., 75478	2 EA	(1)11H,11J
16577-001	I.C., 74HC04	1 EA	6B
16579-001	I.C.,74S86	1 EA	(1)3B
16580-001	I.C., 74LS33	1 EA	(1)6C
16594-001	I.C., 8155	1 EA	(1)7H
17201-001	LED (RED)	1 EA	(1)DS1
17202-001	INDICATOR, LED (RED) T1	5 EA	(1)DS2-6
17801-104	POT, TRIMMER 10% 100K	1 EA	(1)R15
17801-502	POT, TRIMMER 10% 5K	2 EA	(1)R10,R36
17801-503	POT, TRIMMER 10% 50K	1 EA	(1)R35
18200-100	RESIS, CAR. 1/4W 5% 10	2 EA	(1)R9,R18
18200-101	RESIS, CAR. 1/4W 5% 100	1 EA	(1)R81
18200-102	RESIS, CAR. 1/4W 5% 1K	13 EA	(1)R25,R27 R44,R82 R84,R90

Table A2-2 Electronic PCB Parts List (Continued)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR
18200-102	RESIS, CAR. 1/4W 5% 1K	13 EA	R91,R92 R100,R101 R112,R142 R147
18200-103	RESIS, CAR. 1/4W 5% 10K	14 EA	(1)R29,R33 R37,R40 R43,R70 R72,R96 R138,R139 R145,R146 R148,150
18200-104	RESIS, CAR. 1/4W 5% 100K	3 EA	(1)R74,R75 R95
18200-105	RESIS, CAR. 1/4W 5% 1 MEG	1 EA	R34
18200-121	RESIS, CAR. 1/4W 5% 120	2 EA	(1)R58,R59
18200-122	RESIS, CAR. 1/4W 5% 1.2K	2 EA	(1)R49 R107
18200-151	RES., CAR, 1/4W 5% 150	1 EA	(1)R42
18200-152	RESIS, CAR. 1/4W 5% 1.5K	4 EA	(1)R8,R68 R133,R134
18200-153	RES, CARBON 1/4W 5% 15K	1 EA	(1)R53
18200-161	RESIS, CAR. 1/4W 5% 160	1 EA	(1)R106
18200-182	RES, CARBON 1/4W 5% 1.8K	1 EA	(1)R54
18200-202	RESIS, CAR. 1/4W 5% 2K	1 EA	(1)R132
18200-203	RESIS, CAR. 1/4W 5% 20K	6 EA	(1)R19,R56 R71,R73 R116,R123
18200-221	RESIS, CAR. 1/4W 5% 220	1 EA	(1)R69
18200-272	RESIS, CAR. 1/4W 5% 2.7K	3 EA	(1)R64,R65 R141
18200-302	RESIS, CAR. 1/4W 5% 3K	2 EA	(1)R7,R55
18200-330	RESIS, CAR. 1/4W 5% 33	1 EA	(1)R103
18200-332	RESIS, CAR. 1/4W 5% 3.3K	1 EA	(1)R149
18200-333	RESIS, CAR. 1/4W 5% 33K	4 EA	(1)R16,R17 R143,R144
18200-362	RESIS, CAR. 1/4W 5% 3.6K	1 EA	(1)R97
18200-392	RESIS, CAR. 1/4W 5% 3.9K	1 EA	(1)R41
18200-470	RESIS, CAR. 1/4W 5% 47	1 EA	(1)R80
18200-471	RESIS, CAR. 1/4W 5% 470	1 EA	(1)R28
18200-472	RESIS, CAR. 1/4W 5% 4.7K	5 EA	(1)R48,R57 R85,R99 R47

Table A2-2 Electronic PCB Parts List (Continued)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR
18200-473	RESIS, CAR. 1/R2 5% 47K	3 EA	(1)R38,R39 R50
18200-511	RESIS, CAR. 1/4W 5% 510	6 EA	(1)R1,R2 R21,R76 R83,R102
18200-622	RESIS, CAR. 1/4W 5% 6.2K	1 EA	(1)R45
18200-681	RESIS, CAR. 1/4W 5% 680	2 EA	(1)R60,R61
18200-682	RESIS, CAR. 1/4W 5% 6.8K	7 EA	(1)R78 R86-89 R136,R137
18200-752	RESIS, CAR. 1/4W 5% 7.5K	1 EA	(3)R135
18201-121	RESIS, CAR. 1/2W 5% 120	1 EA	(1)R104
18203-181	RESIS, MET.FLM. 1/4W 1% 75	1 EA	(1)R77
18203-210	RESIS, MET.FLM. 1/4W 1% 150	1 EA	(1)R66
18203-232	RESIS, MET.FLM. 1/4W 1% 255	1 EA	(1)R79
18203-254	RESIS, MET.FLM. 1/4W 1% 432	2 EA	(1)R62,R63
18203-288	RES, MET FILM 1/4W 1% 976	1 EA	(1)R105
18203-289	RESIS, MET.FLM. 1/4W 1% 1.00K	5 EA	(1)R11,R12 R52,R125 R127
18203-298	RES, MET FILM 1/4W 1% 1.24K	1 EA	(1)R51
18203-314	RESIS, MET.FLM. 1/4W 1% 1.82K	1 EA	(1)R109
18203-318	RESIS, MET.FLM. 1/4W 1% 2.00K	2 EA	(3) R110,R120
18203-327	RES MTL FILM 1/4W 1% 2.49K	2 EA	(1)R24,26
18203-335	RESIS, MET.FLM. 1/4W 1% 3.01K	1 EA	(1)R94
18203-347	RESIS, MET.FLM. 1/4W 1% 4.02K	2 EA	(1)R124, R128
18203-351	RESIS, MET.FLM. 1/4W 1% 4.42K	2 EA	(1)R3,R4
18203-361	RESIS, MET.FLM. 1/4W 1% 5.62K	2 EA	(1)R93,R98
18203-381	RES, MET FILM 1/4W 1% 9.09K	1 EA	(1)R32
18203-385	RESIS, MET.FLM. 1/4W 1% 10.0K	8 EA	(1)R5,R6 R13,R14 R20,R117 R119,R130
18203-413	RESIS, MET.FLM. 1/4W 1% 19.6K	1 EA	(1)R46
18203-415	RESIS, MET.FLM. 1/4W 1% 20.5K	2 EA	(1)R22,R23
18203-444	RESIS, MET.FLM. 1/4W 1% 41.2K	1 EA	(1)R113
18203-452	RESIS, MET.FLM. 1/4W 1% 49.9K	2 EA	(1)R121 R129
18203-460	RESIS, MET.FLM. 1/4W 1% 60.4K	1 EA	(1)R108
18203-477	RESIS, MET.FLM. 1/4W 1% 90.9K	1 EA	(1)R126

Table A2-2 Electronic PCB Parts List (Continued)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR
18203-481	RESIS, MET.FLM. 1/4W 1% 100K	4 EA	(1)R115 R118,R131 R111
18203-548	RESIS, MET.FLM. 1/4W 1% 499K	2 EA	(1)R114 R122
18205-001	TERMINATOR, 16 PIN DIP	1 EA	(1)1J
18207-101	RESIS, CAR. 1W 5% 100	1 EA	(1)R67
18208-002	RESISTOR, 1W, 1%, 0.2 OHM	1 EA	(1)R140
18211-102	RESISTOR NETWORK, 1K 6 PIN	1 EA	(1)RN1
18211-471	NETWORK, RES 470 6 PIN	1 EA	(1)RN3
18212-103	NETWORK, RES 10K 8 PIN	3 EA	(1)RN2,RM4 RN7
19100-001	TRANSISTOR, PWR, TIP 120	2 EA	(1)Q15,Q16
19101-001	TRANSISTOR, PWR, TIP 125	2 EA	(3)Q17,Q18
19107-001	TRANSISTOR, NPN 2N3904	8 EA	(1)Q2-5 Q8-10,Q14
19110-001	TRANSISTOR, PNP, 2N3906	3 EA	(1)Q11-13
19111-001	TRANSISTOR, NPN, 2N6717	2 EA	(1)Q6,Q7
19500-002	BAR, BUS	1 EA	(1)FENCE
20215-001	NETWORK, RESISTOR	1 EA	(1)RN6
20467-001	IC PAL10H8 PROGRAMMED	1 EA	(1)7J

Table A2-3 Filter PCB Parts List (Models 9020L & 9045L)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR
20405-001	ASSY, FILTER PCB, 90 IPS	1 EA	(1)
15500-101	CAP., CER. NPO 5% 50V 100PF	1 EA	(1)C3
15500-200	CAP., CER. NPO 5% 50V 20PF	1 EA	(1)C4
15500-391	CAP., CER. NPO 5% 50V 390PF	2 EA	(1)C1,2
15838-001	RECEPTACLE CONTACT	5 EA	(1)AMP
16401-127	INDUCTOR, MOLDED 5% 120UH	2 EA	(1)L3,4
16401-277	INDUCTOR, MOLDED 5% 270UH	2 EA	(1)L1,2
50104-001	BOARD, PN-FILTER (LSI)	1 EA	

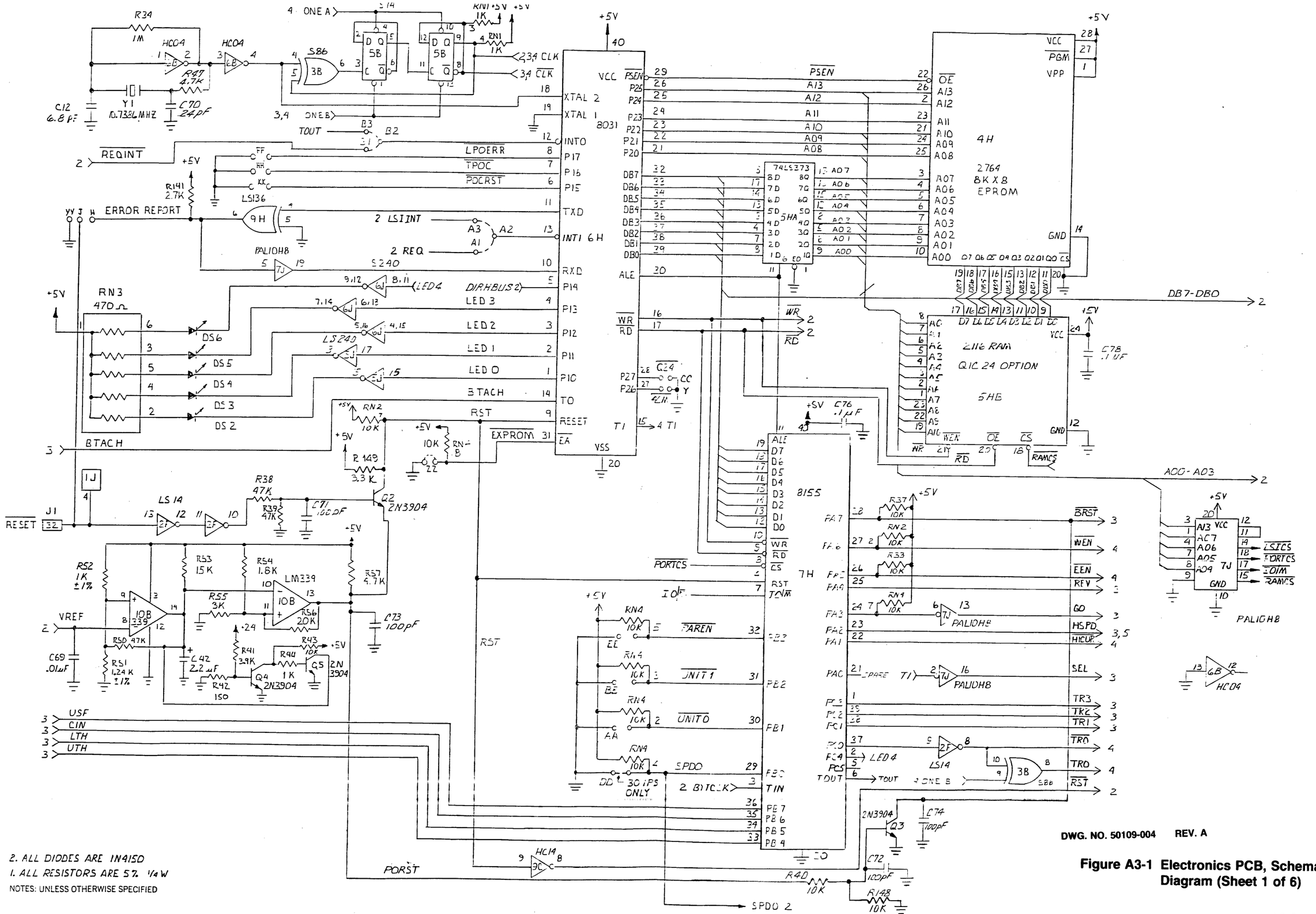
Table A2-4 Filter PCB Parts List (Model 3020L)

PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY UM	REFERENCE DESIGNATOR
20405-002	ASSY, FILTER PCB	1 EA	(1)
15500-122	CAP., CER. 5% 50V 1200PF	2 EA	(1)C1,2
15500-301	CAP., CER. NPO 5% 50V 300PF	1 EA	(1)C3
15500-620	CAP., CER. 5% 50V 62PF	1 EA	(1)C4
15838-001	RECEPTACLE CONTACT	5 EA	(1)AMP
16401-367	INDUCTOR, MOLDED 5% 360UH	2 EA	(1)L3,4
16401-827	INDUCTOR, MOLDED 5% 8200UH	2 EA	(1)L1,2
50104-001	BOARD, PN-FILTER (LS1)	1 EA	

APPENDIX III
SCHEMATIC DIAGRAMS

A3.1 SCOPE

This Appendix contains the schematic diagrams for the LSI Sidewinder Intelligent Drive.



2. ALL DIODES ARE IN4150
1. ALL RESISTORS ARE 5% 1/4 W
NOTES: UNLESS OTHERWISE SPECIFIED

DWG. NO. 50109-004 REV. A

Figure A3-1 Electronics PCB, Schematic Diagram (Sheet 1 of 6)

SPDO
RST
CLK
+5V
1J TERMINATOR
J1
LS240
REQ
XFER
ONL
PARITY
HB7
HB6
HB5
HB4
HB3
HB2
HB1
HB0
DIRC
EXCPT
ACK
READY
LAST PIN = 50;
ALL ODD PIN
NUMBERS ARE GND.
S240
3 J
2 J
4J
5J
6J
DIRHBUS
RDYHBUS
UNITEN
DIR
EXCEPT
ACK
RDY
1 REQ
REQINT
HCCA
+5 REG
C27 .01μF
C29 24pF
C28 6.8pF
C30 .01μF
C31 .01μF
R81 100
VCC
2CEXT
1CEXT
FRQ CONT
RNG
2G
1G
GND
VCO 7D 5124
VCO1
VCO2
3 LTH
3 UTH
2,3 H
LSI
CONTROLLER
C77 .1μF
RST
CLK
LOCK
REF
MARGIN
RDAT
WCLK/D
RCLK
D
C
BYTCLK 1
LOCK
REF
MARGIN
RD DATA
RD CLOCK
REQ 51
XFER 57
ONL 58
PARITY 1
HB7 67
HB6 66
HB5 65
HB4 64
HB3 63
HB2 62
HB1 61
HB0 59
DIR 54
EXCEPT 53
ACK 2
RDY 52
UNITEN 55
RDYHBUS 56
VSS INT CS
34, 9
60
48 LSICS
LSIINT
AD3
RDP
WDA
WDA
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
WR
RD
AD2
AD1
AD0
WD
WD
WE
RA14
RA13
RA12
RA11
RA10
RA09
RA08
RA07
RA06
RA05
RA04
RA03
RA02
RA01
RA00
NE
RAMIN
RAMOUT
LADO
LAD1
LAD2
LAD3
LAD4
LADDER
LADDOUT
VREF
RN6
LAD. OUT
R94 3.01K ±1%
C39 8200pF
301PS ONLY
R93 5.62K ±1%
C38 1500pF
901PS ONLY
R36 5K
R99 4.7K
LF353
R97 3.6K
+12
C35 .1μF
R93 510
CR9
VREF
C63 .01μF
R96 10K
R35 50K
+24
R95 100K
C40 300pF
R98 5.62K ±1%
C37 OPEN
R67 100 1W
C18 4.7μF ±20% 35V
TL7800S Q19
C17 4.7μF ±20% 10V
+5 REG 6
+5V
C79 .1μF
20
CS
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
WE
DIN
DOUT
GND
10
1 M 2167 16K X 1 RAM

Figure A3-1 Electronics PCB, Schematic Diagram (Sheet 2 of 6)

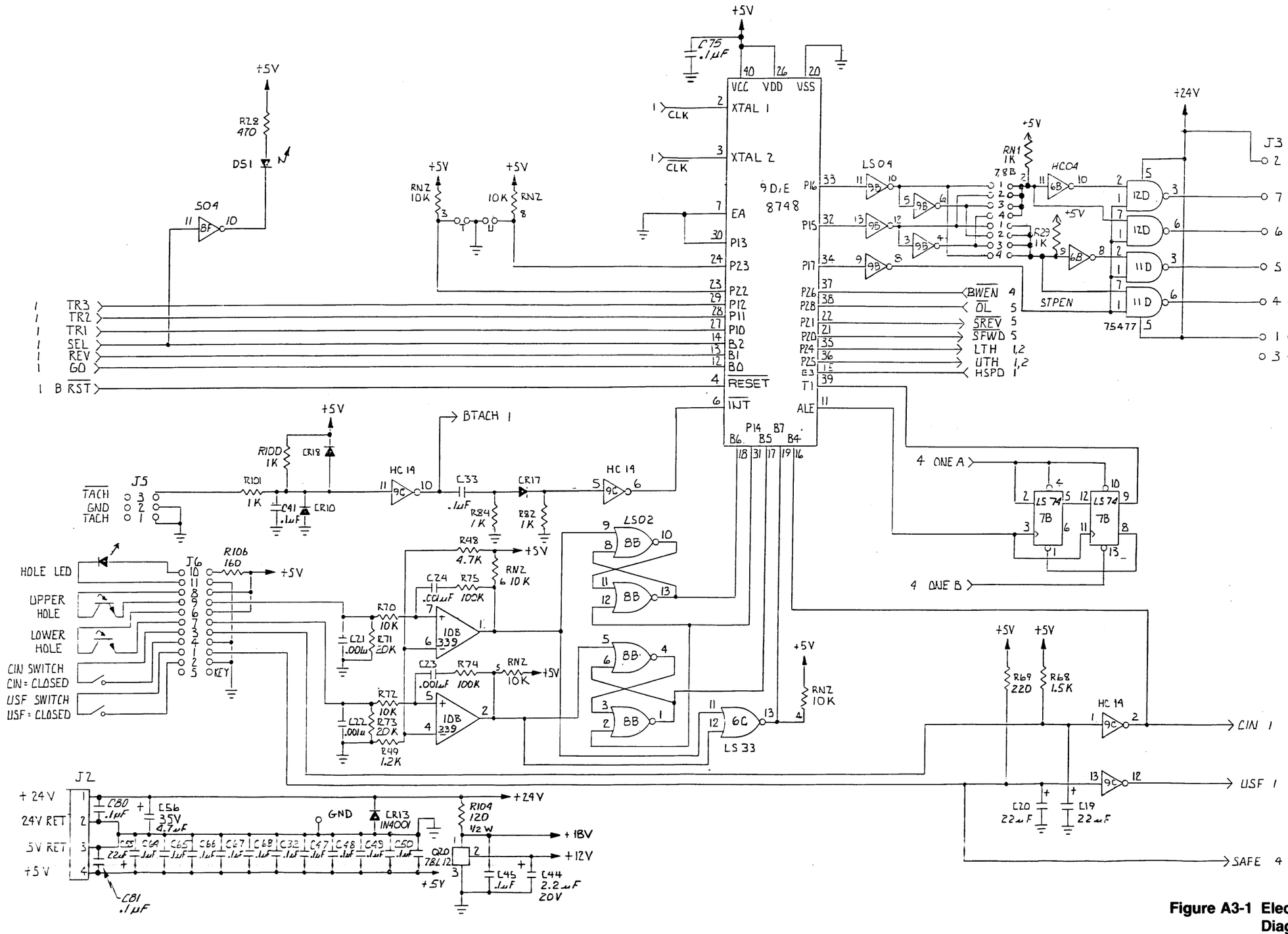


Figure A3-1 Electronics PCB, Schematic Diagram (Sheet 3 of 6)

READ 0
READ 1
J13
CR1
CR2
CR3
CR4
R6 10K ±1%
R7 3K
C3 220pF
R5 10K ±1%
R4 4.42K ±1%
R1 510
C2 .1μF
R3 4.42K ±1%
R2 510
C1 .1μF
7406
1 TRD
1 TRD
R8 4.5K
C62 2700pF
1K
30 IPS ONLY
IC 592
C4 6.8μF 4V
C5 .1μF
C6 .1μF
R9 10
L
M
F1 C1
F2 C2
L2
L3
L1
L4
C3
C4
F3
F4
ASSY # 20405-XXX
R18 10
C9 .1μF
R10 5K
R14 10K ±1%
R12 1K ±1%
R11 1K ±1%
R13 10K ±1%
IE 592
C8 6.8μF 4V
C7 .1μF
P
N
R17 33K
R16 33K
R15 100K
L2 10μH
+12V
R20 10K ±1%
R103 33
+18V
C11 .1μF
R24 2.49K ±1%
R27 1K
R26 2.49K ±1%
R25 1K
3E 3/8
R21 510
+5V
R19 20K
C10 33pF
R102 510
C43 .1μF
L1 10μH
R23 20.5K ±1%
R22 20.5K ±1%
LS00 3D
LS00 3D
LS04 9B
1 WEN
B WEN 3
WRITE 0
ERASE
J11
J12
WRITE 1
CR7
C75 20pF
CR8
CR5
CR6
R85 4.7K
CR11
CR12
+24V
R92 1K
L34 1μF
Q13 3906
R78 6.8K
+5V
R79 255 ±1%
7406
T1 1
Q14 2N3904
R80 47
3 SAFE
R90 1K
R91 1K
Q12
Q11
R89 6.8K 2N3906
R87 6.8K 2N3906
R88 6.8K
R86 6.8K
7406
1 TRD
7406
1 TRD
LS33
2 WDA
6C
R60 680
Q8 2N3904
+5V
R65 2.7K
LS33
R62 432 ±1%
6C
2N3904
1 HICUR
7406
R64 2.7K
Q10
R63 932 ±1%
2N3904
Q9
LS33
2 WDA
6C
R61 680
R66 150 ±1%
R58 120
HC 14
75451
2 EEN
5A
Q7 2N6717
Q6
1 CLK
1 CLK
5A
R59 120
+5V
C16 OPEN
R77 75 ±1%
C14 .1μF
C15 .1μF
+5V
RN1 1K
R32 9.09K ±1%
R46 19.6K ±1%
30 IPS ONLY
C14 220pF
R76 510
SB6
3B
4B 3602
LS 74 3C
ONE A 1,3
+5V
RN1 1K
R45 6.2K
C13 220pF
SB6
3B
4B 3602
LS 74 3C
RDP 2
ONE B 1,3

Figure A3-1 Electronics PCB, Schematic Diagram (Sheet 4 of 6)

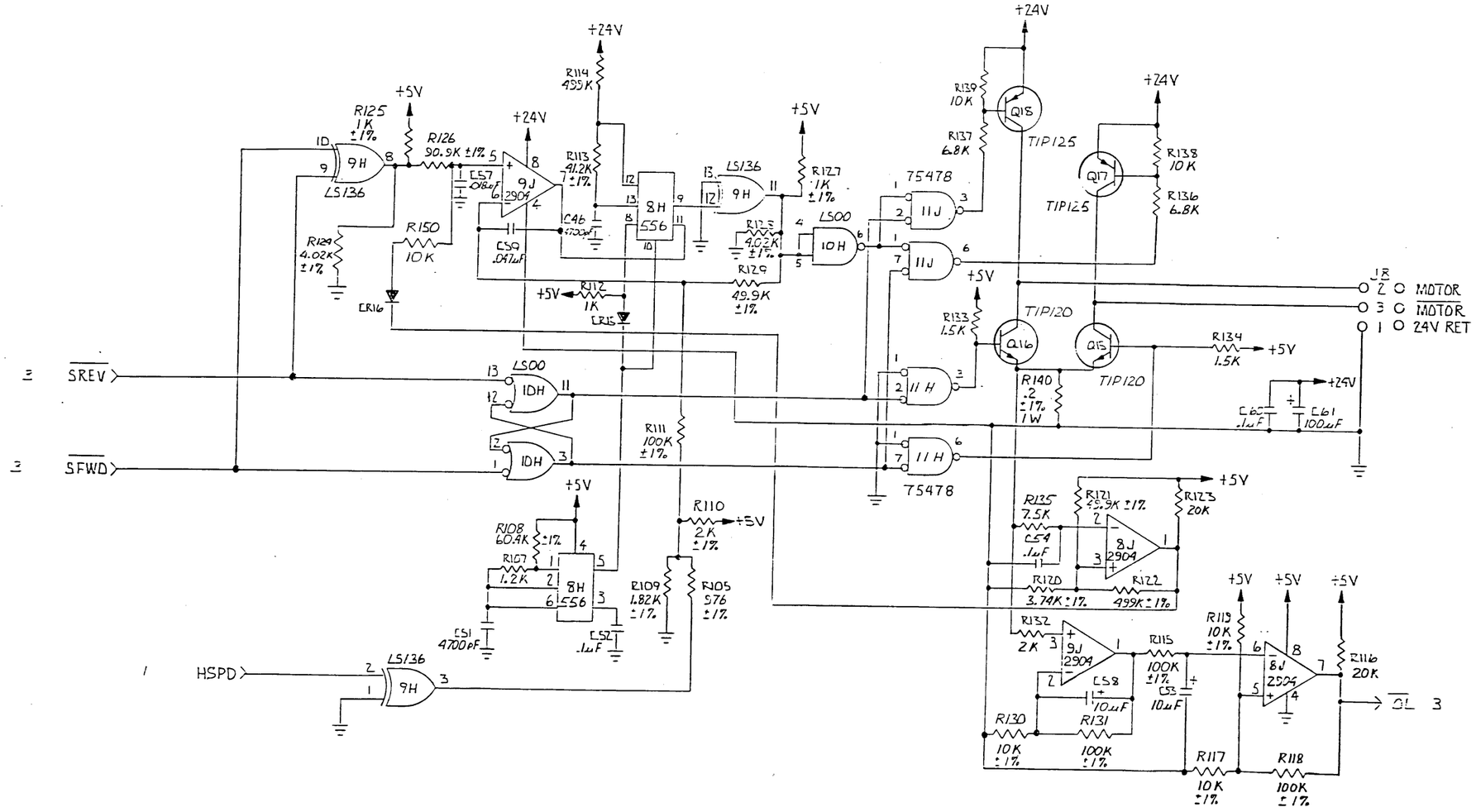


Figure A3-1 Electronics PCB, Schematic Diagram (Sheet 5 of 6)

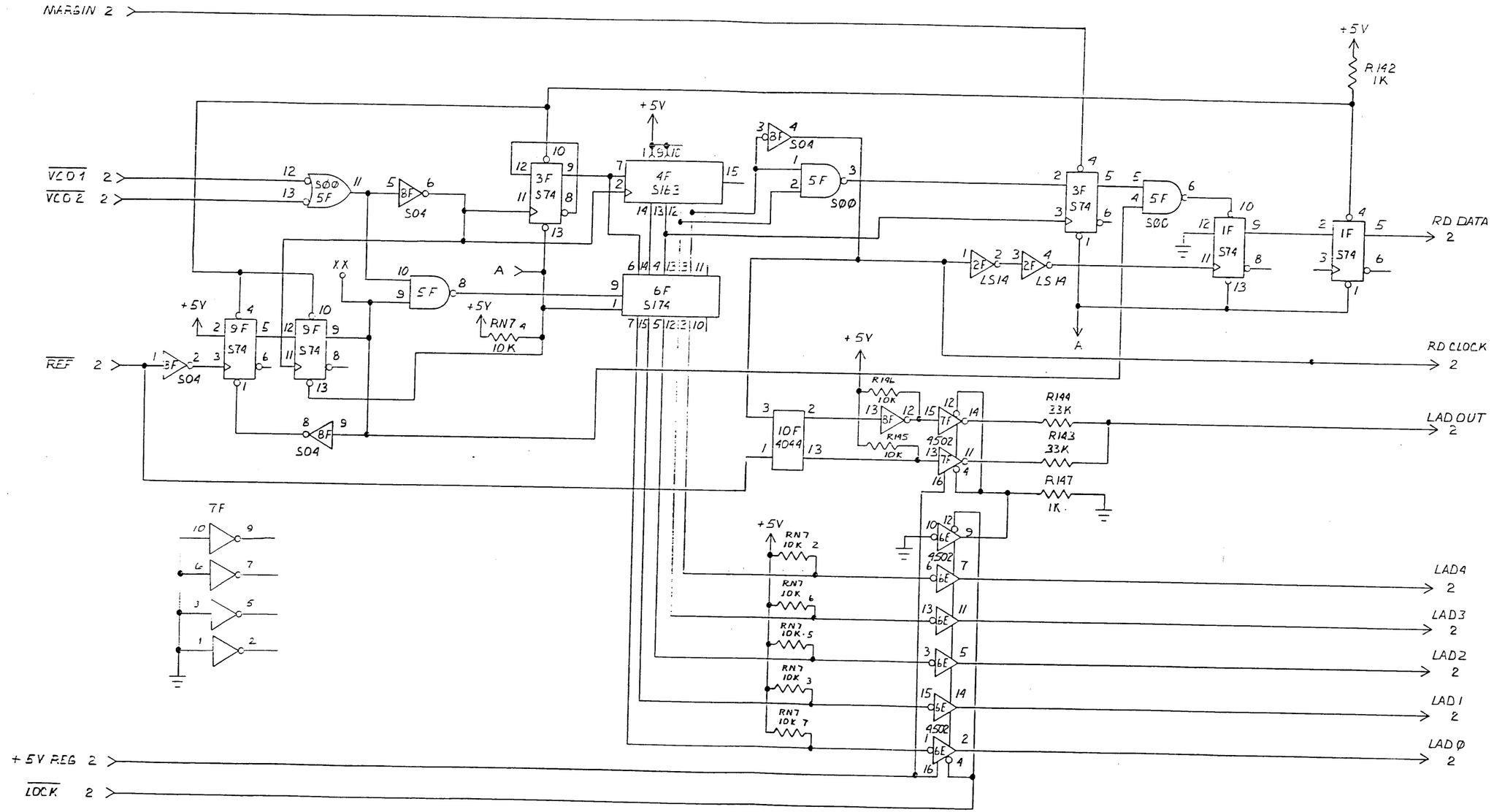


Figure A3-1 Electronics PCB, Schematic Diagram (Sheet 6 of 6)

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