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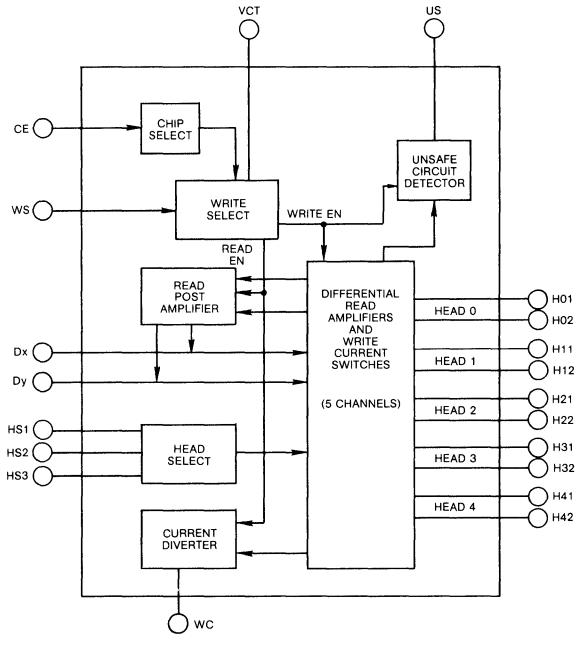
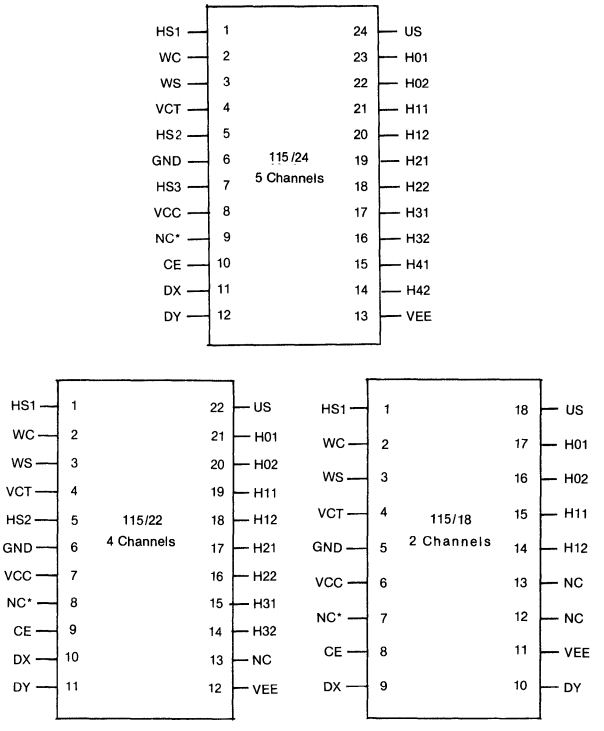
SSI 115
Winchester Read/Write Circuit

Data Sheet



SSI 115 Block Diagram



SSI 115 Pin Out
(Top View)

*Do not connect to any etch or any part of any circuit

FEATURES

- **Electrically compatible with 8 inch and 5-1/4 inch Winchester disk drive magnetic recording heads.**
- **Supports up to five recording heads per circuit.**
- **Detects and indicates unsafe write conditions.**
- **On-chip current diverter eliminates the need for external write current switching.**
- **Control signals are TTL compatible.**
- **Operates on standard +5 volt and −5 volt (or −5.2 volt) power sources.**

DESCRIPTION

The SSI 115 is a monolithic bipolar integrated circuit designed for use with 8 inch and 5-1/4 inch Winchester disk drive magnetic recording heads. The circuit interfaces with up to five magnetic recording heads providing the required read/write electronic functions as well as various control and data protect functions. The circuit operates on +5 volt and −5 volt (or −5.2 volt) power and is available in a variety of packages. The 115/24 is a 5 channel circuit available in both flatpack and dip packages. The 115/22 is a 4 channel circuit packaged in a 22 pin dip and the 115/18 is a 2 channel circuit offered in a 18 pin dip package.

SSI 115
Winchester
Read/Write Circuit

CIRCUIT OPERATION

WRITE MODE

With both the chip enable and write select signals activated, the SSI 115 is switched to the write mode and the circuit operates as a differential current switch. The center tap head voltage (VCT) is turned on, the unsafe circuit detector is activated, and the current diverter is disabled. The head select signals (HS1, HS2, HS3) select one of five differential current switches. The selected current switch senses the polarity of the data input signal (Dx−Dy) and gates write current to the corresponding side of the head (HN1 or HN2). Head overshoot voltages that occur during normal write operation are sensed to determine safe or unsafe head circuit conditions. The detector senses the following unsafe conditions—no data transitions, head open, or no write current.

READ MODE

With chip enable active and write select disabled, the SSI 115 is switched to the read mode and the circuit operates as a differential amplifier. The center tap head voltage is turned off, the unsafe circuit detector is deactivated, and the write current diverter is enabled. The differential head input signal (HN1−HN2), selected by the head select signals, is amplified by a differential read amplifier and appears as a differential output signal on the data lines (Dx, Dy).

During the read and idle modes, the on-chip current diverter circuit prevents write current from flowing in the head circuits. Therefore, external gating of the write current source is not required.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage, VCC 6V
Negative Supply Voltage, VEE..... −6V
Write Current (IWC) ..... 70 mA
Operating Junction Temperature ..... 25°C to 135°C
Storage Temperature..... −65°C to 150°C
Lead Temperature (Soldering, 10 SEC)..... 260°C

Input Voltages

Head Select (HS) .. .. −0.4V to VCC +0.3V
Unsafe (US) (IHUS ≤ 15mA)... −0.3V to VCC +0 3V
Write Current (WC) Voltage in read idle modes. (Write mode must be current limited to −70mA) .... VEE −0.3V to 0.3V
Data (Dx, Dy) ..... VEE to 0.3V
Chip Enable ($\overline{CE}$) .. .. −0.4V to VCC +0.3V
Write Select ($\overline{WS}$) ..... −0.4V to VCC +0.3V

RECOMMENDED OPERATING CONDITIONS

VCC ..... 5V IWC . ..... −45mA
VEE..... −5V (−5.2)V LH..... 10μh

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $4.75 \leq VCC \leq 5.25V$, $-5.5V \leq VEE \leq -4.75V$
$25°C \leq T$ (Junction) $\leq 135°C$

POWER SUPPLY

Parameter	Test Conditions	Min.	Max.	Units
Total Power Dissipation (PD)	Write Mode, IWC≤45mA, TJ≥125°C		700	mW
Positive Supply Current (ICC)	Read/Write Mode		35 + IWC	mA
Positive Supply Current (ICC)	Idle Mode		10	mA
Negative Supply Current (IEE)	Read/Write Mode	-65		mA
Negative Supply Current (IEE)	Idle Mode	−10		mA

LOGIC SIGNALS

Parameter	Test Conditions	Min.	Max.	Units
Chip Enable Low Voltage (VLCE)	Read or Write Mode	−0.3	0.8	V
Chip Enable Low Current (ILCE)	VLCE = 0V	−2.4		mA
Chip Enable High Current (IHCE)	Idle Mode	−250		μA
Write Select Low Voltage (VLWS)	Write or Idle Mode	−0.3	0.8	V
Write Select Low Current (ILWS)	VLWS = 0V	−3 2		mA

LOGIC SIGNALS (Cont.)

Parameter	Test Conditions	Min.	Max.	Units
Write Select High Current (IHWS)	Read or Idle Mode	−250		μA
Head Select High Level Voltage (VHHS)		2.0	VCC	V
Head Select High Level Current (IHHS)	VHHS = VCC		100	μA
Head Select Low Level Voltage (VLHS)		−0.3	0.8	V
Head Select Low Level Current (ILHS)	VLHS = 0V	−0 6		mA
Unsafe Low Level Voltage (VLUS)*	ILUS = 8mA (Denotes Unsafe Condition)		0.5	V
Unsafe High Level Current (IHUS) *	VHUS = 5.0V (Denotes Safe Condition)		100	μA

*Note: Unsafe is an open collector output

READ MODE: Tests performed with 50 load resistors from Dx and Dy to ground.

Parameter	Test Conditions	Min.	Max.	Units
Input Common Mode Range		−0.6	0.1	V
Total Input Bias Current	$-0.6V \leq Vin \leq 0.1V$		60	μA
Differential Voltage Gain	Vin = 1mVpp, f = 300kHz	26	52	V/V
Voltage Bandwidth (−3dB)	$Zs \leq 10\Omega$, Vin = 1mVpp, $f_{midband}$ = 300kHz	30		MHz
Input Noise Voltage	Zs = 0, Vin = 0V, Power Bandwidth = 15MHz		7	μV_{rms}
Differential Input Capacitance	Vin = 0, f = 5MHz		20	pF
Differential Input Resistance (Internal Damping Resistor)	Vin = 0, f = 300kHz	560	1070	Ω
Output Offset Voltage			120	mV
Differential Head Current	IWC = 45mA, LH = 10μH, f = 2MHz		2	mAp
Output Common Mode Voltage		−0 4	− 125	V
Single Ended Output Resistance	f = 300kHz	10		kΩ
Single Ended Output Capacitance			10	pF
Dynamic Range	DC input voltage where the AC gain falls to 90% of its 0VDC input value (Measured with 0.5mVpp AC input voltage)	2		mVp
Common Mode Rejection Ratio	Vin = 100mVpp, 0VDC, f = 5MHz	50		dB
Power Supply Rejection Ratio	ΔVCC or ΔVEE, 100 mVpp, f=5MHz	45		dB
Channel Separation	The 4 unselected channels are driven with Vin = 100mVpp, f = 5MHz	45		dB
Write Current Voltage	IWC = 45mA	−2.7	−0.5	V
Total Head Input Current	IWC = 0		200	μA

WRITE MODE

Parameter	Test Conditions	Min.	Max.	Units
Current Gain (IH/IWC)	IWC = 45mA, IH ≙ Head Current	0.95	1.0	
Write Current Pin Voltage	IWC = 45mA	−3.7	−1.5	V
Center Tap Head Voltage (VCT)	IWC = 45mA	3.0	VCC-0.5	V
Differential Head Voltage Swing	3.0 ≤ VCT ≤ VCC −0.5V IWC = 45mA, LH = 10μH	5.7	7.7	V
Differential Data Voltage (Dx-Dy)		.175		V
Single Ended Data Input Voltage (Dx, Dy)		−0.9	0.1	V
Data Input Current	−0.9 ≤ VDx, VDy ≤ 0.1	−10	100	μA
Data Input Differential Resistance	f = 300kHz	5		kΩ
Data Input Capacitance			10	pF
Unselected Diff Head Current	IWC = 45mA, LH = 10μH, f = 2MHz		2	mA_p
Write Current Range		30	50	mA
Total Head Input Current	IWC = 0		500	μA

IDLE MODE

Parameter	Test Conditions	Min.	Max.	Units
Write Current Pin Voltage	IWC = 45mA	VEE		V
Differential Head Current	IWC = 45mA, LH = 10μH, f = 2MHz		2	mA_p
Total Head Input Current	IWC = 0		500	μA

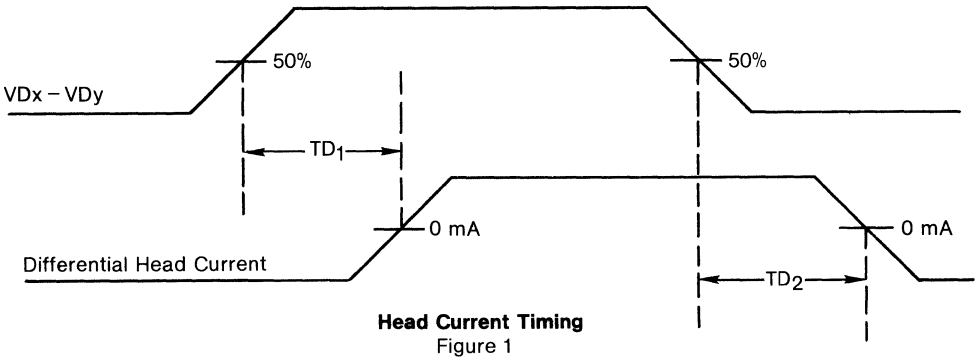
SWITCHING CHARACTERISTICS

Parameter	Test Conditions	Min.	Max.	Units
Idle to Read/Write Transition Time			0.6	μS
Read/Write to Idle Transition Time			0.6	μS
Read to Write Transition Time	0 ≤ VLCE ≤ 0.8V (Circuit Enabled)		0.6	μS
Write to Read Transition Time	0 ≤ VLCE ≤ 0.8V (Circuit Enabled)		0.6	μS
Head Select Switching Delay Time			0.25	μS
Head Current Transition Time	(10% to 90% points) IWC = 45mA, LH = 0H, RH = 0 Ω		15	nS
Head Current Switching Delay Time (TD_1, TD_2)	IWC = 45mA, LH = 0H, RH = 0 Ω f = 5MHz (see figure 1)		19	nS
Head Current Switching Hysteresis TH = (TD_1-TD_2)	IWC = 45mA, LH = 0H, RH = 0 Ω f = 5MHz (VDx-VDy) Rise Time = 2nS (see figure 1)		3	nS
Unsafe to Safe Delay After Write Data Begins (TD_3)	IWC = 30mA, LH = 10μH f = 2MHz (see figure 2A)		1.0	μS
Safe to Unsafe Delay (TD_4)	LH' = 10μH, f = 2MHz IWC = 45mA (see figure 2B)	1.6	8.0	μS

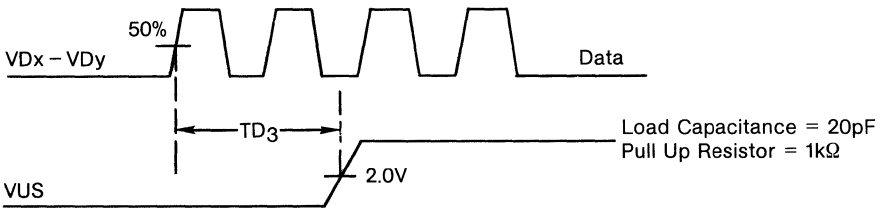
HEAD SELECT TABLE

Head Selected	HS1	HS2	HS3
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

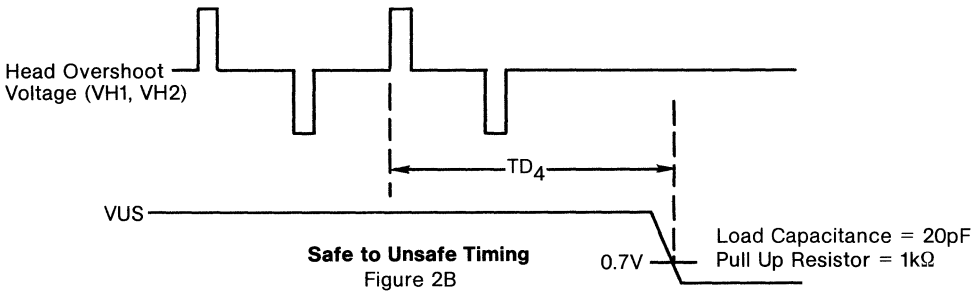
Note: Invalid Head Select input codes (5, 6 and 7) have the effect of not selecting any heads.



Head Current Timing
Figure 1



Unsafe to Safe Timing
Figure 2A



Safe to Unsafe Timing
Figure 2B