Rev 9/77

Amdahl 470V/6

MANAGEMENT SUMMARY

Aimed directly at the IBM System/370 Model 168, the Amdahl 470V/6 computer represents the first campaign on the part of a company to market what is essentially a plug-compatible replacement for an IBM central processing unit. In contrast to previous products offered by other mainframe vendors in attempts to nibble away at portions of the lucrative IBM customer base, the Amdahl 470/V6 offers a singular advantage: complete functional compatibility with IBM System/360 and System/370 software products and with the wide variety of IBM-manufactured and plug-compatible peripheral devices supplied for the System/360 and System/370 computers.

Purchase prices for the Amdahl central processor and main memory are slightly below those of the 370/168, beginning at $3,750,000 for a central processor with 16 I/O channels, system console, power distribution unit, and one million bytes of main memory. But the Amdahl system is rated at approximately twice the internal speed of the 370/168, and it executes IBM system software and program products without the necessity for software or file conversions. In addition, the Amdahl 470V/6 is estimated to occupy only about one-third of the space required by its IBM competitor and operates in an ordinary air-conditioned environment, with no additional requirements for liquid cooling facilities as are necessary for the very large IBM systems. ▷

The large-scale Amdahl 470V/6 computer features IBM System/370 architecture implemented in "fourth-generation" high-speed LSI circuitry. Rated at twice the internal speed of the IBM 370/168 and priced just below it, the 470V/6 can execute any System/360 and System/370 software and interface to any System/360 and System/370-compatible peripheral device.

CHARACTERISTICS

MANUFACTURER: Amdahl Corporation, 1250 East Arques Avenue, Sunnyvale, California 94086. Telephone (408) 735-4011.

MODEL: Amdahl 470V/6.

DATA FORMATS

All data formats, instruction formats, and other architectural features completely follow. IBM System/370 architecture.

BASIC UNIT: 8-bit byte. Each byte can represent 1 alphanumeric character, 2 BCD digits, or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word."

FIXED-POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode. ▶
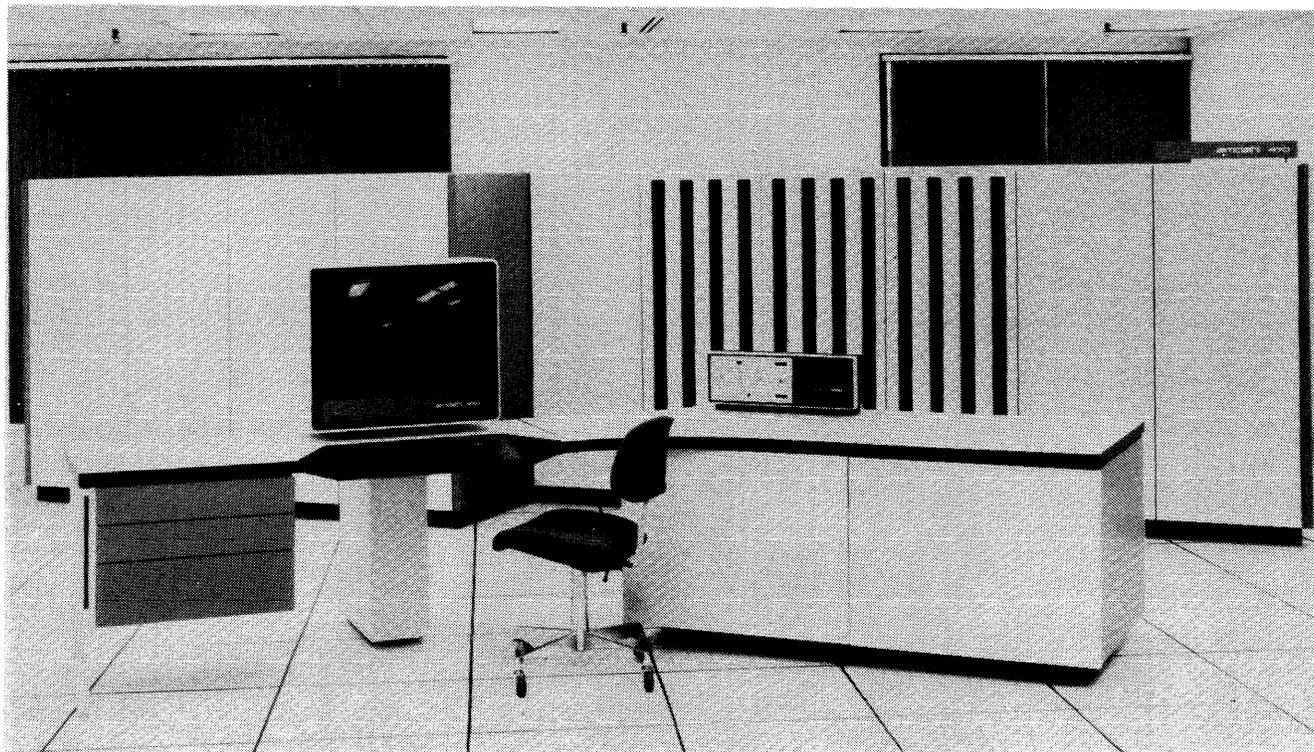
The 470V/6 System Console (foreground) features a Data General Nova 1200 minicomputer that acts as a console processor, as well as a CRT display, keyboard, and control panel. Though its rated internal speed is twice that of the IBM 370/168, the 470V/6 requires two-thirds less floor space and needs no plumbing for cooling purposes because of its "fourth-generation" LSI circuitry.

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The Amdahl 470V/6 design is based on System/370 architecture. It achieves its superior performance through the use of the latest in super-fast integrated circuit technology and, to a lesser extent, from central processor architectural optimization that provides for more efficient operation of the High-Speed Buffer memory and the virtual storage address translation hardware and permits extensive overlapping of input/output operations and instruction execution in the central processor.

Large-scale integration (LSI) semiconductor circuits are used throughout the system, resulting in substantially increased processing speeds, higher reliability, and reduced space and cooling requirements. The central processor uses an LSI version of bipolar emitter-coupled logic (ECL) with chip speeds in the area of 600 picoseconds (trillionths of a second), and has a CPU cycle time of approximately 32 nanoseconds.

Main memory uses metal oxide semiconductor (MOS) LSI circuits and has a cycle time of 300 nanoseconds, while ultra-high-speed bipolar components are used in the cache-like buffer memory. Buffer loading from main memory is performed in 32-byte blocks. Using the maximum (four-way) main storage interleaving capabilities, a maximum data transfer rate of one 32-byte "line" per 163 nanoseconds can be achieved between the High-Speed Buffer and main memory.

The LSI chips used in the Amdahl 470V/6 measure 154 thousandths of an inch square, are 10 mils thick, and have a maximum capacity of about 100 circuits. The LSI chips are mounted on a multi-chip carrier, which is the field-replaceable unit of the system. Each carrier has a maximum capacity of about 4200 circuits. Thus, all 150,000 circuits comprising the 470V/6 system can be housed on 51 multi-chip carriers, resulting in a system requiring an estimated one-third of the floor space occupied by an IBM System/360 Model 168 with its associated channels.

The Amdahl circuits also require only a fraction of the power consumed by standard ECL circuitry, resulting in significantly reduced cooling requirements for the system. The entire 470V/6 system is air-cooled, and a cooling stub is bonded to the surface of each LSI chip carrier to conduct heat into the air flow.

At the time when development began on the Amdahl system, economically practical LSI technologies were not available to produce circuit chips with the density and speed required to implement the Amdahl concepts. As a result, all of the circuitry, plus the manufacturing techniques, test equipment, and chip interconnection methods, have been specially designed by Amdahl engineers.

The Amdahl 470V/6 configuration consists of a central processor unit with 16 integrated input/output channels, a minicomputer-based system console with CRT display, from one to eight million bytes of main memory, and a ▷

FLOATING-POINT OPERANDS: 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short" format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; or 4 words in "extended precision" format.

INSTRUCTIONS: 2, 4, or 6 bytes in length, which usually specify 0, 1, or 2 memory addresses respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: Metal oxide semiconductor (MOS) LSI circuitry.

CAPACITY: From one to eight million bytes, in one-million-byte increments, housed in a maximum of four main storage units. Each main storage unit is equipped with an independent power supply and can contain one million or two million bytes of memory. Four-way interleaving of memory accesses can be performed in main storage units containing two million bytes, and two-way interleaving is performed in storage units containing one million bytes.

CYCLE TIME: 300 nanoseconds per 32-byte "line." One 32-byte line every five CPU cycles (163 nanoseconds) with four-way interleaving.

CHECKING: Error checking and correction (ECC) circuitry in main memory performs automatic correction of all single-bit errors and detection of all double-bit and most other multiple-bit memory errors.

A Configuration Control Register, associated with each one- or two-million-byte storage unit, maintains a map of the assignment of main storage address space for that storage unit. In the event of an unrecoverable memory error, the one-million-byte memory module can be removed from operation and the remaining memory reconfigured for continuous system operation.

In addition, a parity check is performed on all data transferred between main memory and the High-Speed Buffer. A separate parity check is also made on storage keys, which are used to implement storage protection and to record references and modifications to main storage.

STORAGE PROTECTION: Storage protection facilities are comparable to those implemented in the IBM System/370.

STORAGE CONTROL UNIT (S-UNIT): The Storage Control Unit, or S-Unit, handles all requests for data from main storage made by the CPU and the channels. An internal priority structure is used to resolve conflicts resulting from multiple concurrent requests for access to main memory. The internal priority structure of the S-Unit has the following five priority levels, in descending order: Internal High (including ECC handling), Channel Unit High, Central Processing Unit, Channel Unit Low, and Internal Unit Low (such as instruction prefetch). Normally, the central processor unit is given higher priority than a channel except when a channel issues a high-priority request. The Storage Control Unit locates the requested data either in the High-Speed Buffer or in main memory and includes a dynamic address translation facility for translating program-specified virtual addresses into real-memory addresses.

The High-Speed Buffer has a cycle time of 32 nanoseconds and a total capacity of 16,384 bytes. It is organized as a set associative memory composed of primary and alternate halves, each containing 256 32-byte lines that can be addressed on a single-word or double-word basis. Data is transferred between the buffer and the central processing ▶

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power distribution unit. Central processor functions are performed by four independent functional units: a Storage Unit which controls accesses to main memory and includes both virtual address translation hardware and a 16K-byte cache memory; an Instruction Unit for controlling instruction interpretation and execution; an Execution Unit which performs the arithmetic, logic, and data manipulation functions of instruction execution; and a Channel Unit that interprets and executes input/output instructions and interfaces with the standard control unit interface that can communicate with any System/360- or System/370-compatible peripheral equipment. Operation of all functional units can be overlapped, and four-way interleaving can be performed on accesses to main memory.

Although the basic concept underlying the 470V/6 system design is to produce an extremely fast but architecturally simple computer system, sophisticated modifications have been made to several key functional components to achieve more efficient operation. The high-speed buffer, for example, uses a "non-store-through" technique, permitting data to be modified in the buffer without updating main storage. Main storage is updated only when the data is written back to main storage to provide space for new data. The Amdahl system also provides user access to the hardware algorithms that control instruction prefetching and the location and replacement of data in the High-Speed Buffer to enable users to "tune" the system. In addition, Amdahl has engineered a number of probe points into the hardware to facilitate the use of hardware monitors.

Instruction execution is performed in a "pipeline" structure which allows the execution of up to six instructions to occur concurrently. In addition, although the Amdahl Dynamic Address Translation (DAT) feature provides virtual storage operations comparable to those of the System/370, Amdahl has extended its design for more efficient operation. The Amdahl DAT feature maintains a segment table origin (STO) stack that allows up to 31 different virtual storage environments to maintain translation information in the Translation Lookaside Buffer, reducing the amount of updating activity in the buffer. When the capacity of the STO stack is exceeded, the oldest entry in the stack and its associated Translation Lookaside Buffer entries are purged during spare machine cycles. The Translation Lookaside Buffer portion of the Amdahl address translation hardware has also been expanded to 256 entries, compared to the System/370's 128.

The total aggregate input/output data rate of the Amdahl 470V/6 is some 14 million bytes per second, which is comparable to that of the IBM 370/168. The Amdahl central processor, however, includes 16 integrated input/output channels, each of which has a maximum data transfer rate of about two million bytes per second (or four million bytes per second using the optional two-byte interface). Any channel can be configured at installation time as a selector channel or a block or byte
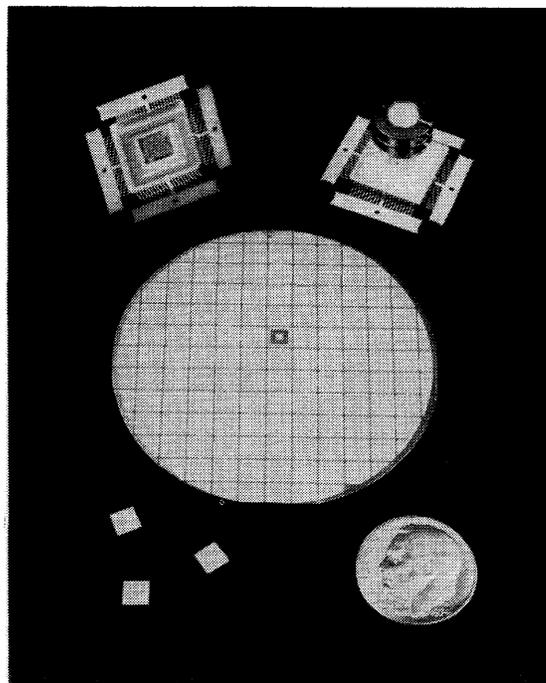
The 470V/6's high performance and compact size are largely due to its "fourth-generation" LSI chips. Each of the three chips shown at bottom left is 0.154 inch square and contains up to 100 circuits. Top and bottom views of a chip mounted in a carrier are shown at the upper right and left, respectively; the top view shows the cooling fins which project into the air stream and cool the chip. At center is a multi-chip LSI wafer prior to the dicing operation. The different-looking chip in the middle is a test circuit used for a quick measure of the quality of the wafer.

unit in groups of 4 bytes per cycle and is brought into the buffer from main memory in lines of 32 bytes, each requiring 4 buffer cycles. In contrast to the System/370, Amdahl I/O channels as well as the CPU access the High-Speed Buffer. A tag field associated with each 32-byte line in the buffer includes a block identifier containing the high-order real address bits of the buffer data, plus parity and check fields, modification indicators, and reference bits to specify whether a central processor or channel access brought the data into the buffer and whether the CPU was in the supervisor or problem state of operation. The 470V/6 allows the user to control the location of data in the High-Speed Buffer according to the CPU state and whether it originates from a central processor channel access.

When a request is made for data by the central processor Instruction Unit or by the Channel Unit, the Storage Control Unit forms a pointer into the buffer and reads four 32-byte lines of data from the primary and alternate halves of the buffer. The S-Unit then uses the real line address calculated by the address translation hardware to select one of the four lines, and a tag comparison on the real address bits is used to select the data from the primary or alternate half of the buffer. Location of the data in the buffer can be performed in two machine cycles, although overlapped buffer operations allow it to accept a request for data during each cycle. If the data is not in the buffer, a main storage request is generated and the requested data is made available to the program and is also placed in the High-Speed Buffer.

Operation of the 470V/6 High-Speed Buffer is based on a non-store-through technique, in which data that is modified

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▷ multiplexer channel. A dynamic priority allocation scheme based on the availability of space in each channel buffer is used to allocate cycles between central processor operations and input/output data transfers. Normally, the central processor has the highest priority in the 470V/6 system, but channels performing high-speed data transfers are allowed to take precedence over the central processor by the Amdahl internal priority scheme. This allows high-speed devices to be attached to any channel without performance degradation and provides additional flexibility in the configuration of peripheral subsystems.

In addition to the 470V/6's impressive speed, Amdahl Corporation states that users can expect significant improvements in hardware reliability and ease of maintenance as a result of the system's sophisticated circuitry. The miniaturization of the circuitry substantially reduces the number of wiring interconnections required in the system, resulting in potentially fewer system failures. Additional circuitry on each LSI chip also allows some 16,000 key logic points in the system to be examined and exercised by diagnostic programs under control of the system console. Remote diagnostic services are also available through a modem supplied with the system console. Other reliability features incorporated in the 470V/6 design include instruction retry, error checking and correction (ECC) circuitry in main memory, and the ability to recover from high-speed buffer and main memory failures by configuring out the malfunctioning portions of the buffer and main memory.

The Amdahl 470V/6 was originally targeted at large multiple-computer installations with substantial investments in IBM-oriented software and staffs with a high level of technical expertise, where the Amdahl system could coexist with other IBM systems and supply superior performance while protecting the users' investment in software and personnel. As it turned out, in the first four installations, the Amdahl systems have completely displaced (or will eventually displace) an IBM central processor as the major computer system at each site. Amdahl Corporation provides maintenance service for its equipment and intends to support users of current IBM system software by providing new releases of the software, including the minor modifications to account for the differences in the way the Amdahl system handles machine check conditions, and by supplying software support services for its customers.

Detailed pricing for separate components of the Amdahl 470V/6 are not available. The basic system, including the central processing unit, one million bytes of main memory, 16 I/O channels, system console, and power distribution unit, has a purchase price of $3,750,000 and a maintenance charge of $6,700 per month. The largest available configuration, which includes the same components but is equipped with 8 million bytes of main memory, has a purchase price of $6,000,000 and a maintenance charge of $9,400 per month. Amdahl estimates that the price of the 470V/6 is approximately 5 percent less than that of a comparable IBM 370/168, but ▷

▶ in the buffer is not written to main storage until the line is removed from the buffer to make room for new data. As a result, frequently referenced data can be accessed and modified in the buffer without incurring a large number of main memory accesses. An instruction prefetch function can be enabled for accesses to the buffer from input/output channels, the operand stream, or the instruction stream. A combination of three bits in the Storage Unit controls the order of prefetch operations, although that order can be modified through the use of an additional register bit provided for that purpose. Six operating state register bits are used to control the operation of the buffer replacement algorithm. The algorithm can be modified by each installation by resetting the values of bits through the System Console. Four additional bits of the S-Unit operating state register, which also can be set through the System Console, can be used to partition the buffer to configure out a portion of the buffer with a hardware failure.

DYNAMIC ADDRESS TRANSLATION: The dynamic address translation facility is located in the S-Unit and controls the translation of program-specified virtual addresses into real-memory addresses. Virtual memory implementation in the 470V/6 is similar to that of the IBM System/370. Virtual storage is divided logically into segments of 64K bytes or 1024K bytes, which are in turn divided into pages of either 2048 or 4096 bytes. Segment and page tables are maintained in main storage to perform address mapping. A high-speed Translation Lookaside Buffer (TLB) is used to store the most recently referenced addresses, and a Segment Table Origin (STO) stack stores information on the size and main memory location of the segment table associated with TLB entries. The TLB consists of 128 virtual and real address pairs in each of the primary and alternate halves. Translation of virtual to real addresses for data located in the TLB is overlapped with the High-Speed Buffer search, and data for both real and virtual operation can be accessed in two S-Unit cycles. If the data is not located in the TLB, an address translation is performed and two additional storage references are required to locate the data either in the High-Speed Buffer or in main memory. The new translated address is placed in the TLB according to an algorithm similar to that used by the High-Speed Buffer.

The STO stack can contain up to 32 virtual storage identification fields associated with TLB entries. The identification fields correspond with address translation information such as segment table size and location, contained in Control Register 0 and Control Register 1. When the contents of these registers are modified, subsequent TLB entries are assigned a new STO ID by the S-Unit, but earlier TLB entries are not invalidated up to a total of 32. If Control Registers 0 and 1 are restored to a previous value, any previous TLB entries remaining are thus still available. The S-Unit controls selective purging (when an STO entry is automatically removed from the stack and its associated TLB entries invalidated) of the TLB and STO stack during spare cycles.

CENTRAL PROCESSOR

Central processor functions such as instruction fetching and decoding and instruction execution are performed by two separate units, the Instruction Unit (I-Unit) and the Execution Unit (E-Unit).

The I-Unit controls instruction execution through a pipeline structure and can have up to six instructions concurrently in some phase of execution. The instruction execution process is divided into the fetch phase plus six additional decoding and execution phases. The instruction fetching operation requires three cycles, while Phases A, B, ▶

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price differences will vary depending on the number of I/O channels configured on the 370/168.

The maintenance agreement offers 24-hour on-call service. In addition, for customers who wish to lease rather than purchase, Amdahl Corporation has negotiated agreements with DPF, Incorporated, an independent computer leasing company, and First Municipal Leasing Corporation. These agreements provide $180 million worth of financing for structuring leases for 470V/6 customers.

It took nearly five years for the Amdahl computer to progress from the drawing board to the first customer's computer room. The Amdahl Corporation was founded by computer wizard Gene M. Amdahl, principal designer of the IBM System/360 and subsequently a director of IBM's advanced systems laboratory and an IBM Fellow, the company's highest scientific position. Equipped with $27 million in funds, supplied primarily by Nixdorf Computer AG, Fujitsu Limited, and Heizer Corporation, the company planned to deliver its first computer system by the end of 1973.

The original Amdahl 470 was a real-memory system targeted at the IBM System/370 Model 165. The target moved, however, with IBM's announcement of the virtual memory 370/168 in August 1972, and Amdahl in turn elected to modify its own system design to incorporate virtual memory hardware that would enable the system to compete with IBM's latest technology. An additional $18 million of financing was required before the first Amadhl 470V/6 system was delivered in May 1975. Fujitsu Limited currently owns 23 percent of the company and manufactures some system subassemblies for Amdahl, although all design, procurement, unit and system testing, and the complete assembly of some system modules is performed by Amdahl.

The first Amdahl 470V/6 system was installed in the National Aeronautics and Space Administration's Institute for Space Studies, replacing an IBM 370/165. A second system replaced an IBM 370/168 at the University of Michigan in August 1975. A third system was installed at Texas A and M University on October 1, 1975, while the fourth (and the first commercial Amdahl 470V/6 site) was installed at Computer Usage Corporation early in November. The company expects to ship two additional systems before the end of 1975.

USER REACTION

At the time of the writing of this report, four Amdahl 470V/6 systems had been installed, and they had aroused more interest and excitement in the data processing community than any recently announced computer mainframe. Datapro conducted telephone interviews with the users of three of these systems. The Amdahl systems in these three installations replaced an IBM System/370 Model 158, a System/370 Model 168, and a combination of a System/360 Model 65 and a System/370 Model 145 that would otherwise have been replaced with a 370/168.

and C, which perform instruction decoding, operand address generation, and operand retrieval, each require a minimum of two central processor cycles. Phases D, E, and F each require a minimum of one cycle, and perform execution plus checking and writing of the results of the instruction execution. The overlapped instruction execution in the pipeline can result in the completion of an instruction execution every two machine cycles, except in the case of long instructions requiring additional cycles for execution.

Extensive parity checking is performed throughout the I-Unit. All incoming instructions are checked for parity, and the results are checked again after completion of execution. All control registers and the program status word are checked each time they are used. In addition, parity is checked for the timer and the address generation function, and parity is also maintained for all program-referable data.

The Execution Unit (E-Unit) executes arithmetic and logical instructions received from the I-Unit; it consists of a logical unit and checker (LUCK), a group of functional units (multiplier, adder, shifter, and byte mover), a table lookup unit to generate an inverse in the I-register (for divide operations), registers for storage of intermediate results, and a result register for output of the result of instruction execution to the I-Unit. Instruction operation codes plus control information are sent from the I-Unit to the E-Unit, and instruction operands are received either from the I-Unit or directly from main storage. The LUCK checks the validity of incoming operands, performs logical operations and comparisons on incoming operands, validates decimal digit formats, sets condition codes, and counts leading zeroes for use in shifting and normalization. LUCK operations require one CPU cycle. Additional arithmetic functions are performed by the multiplier, adder, shifter, and byte mover units, each of which also completes its function in one machine cycle.

When instructions require processing by multiple E-Unit functions, the I-Unit synchronizes the operation of its pipeline by delaying the progress of other instructions in the pipeline until the final cycle of the instruction that is currently in the E-Unit. The E-Unit performs parity checks on all incoming data and on logical and shift operations, and uses a check summation technique to verify the results of addition and multiply functions. The E-Unit also generates parity for final instruction execution results, and the parity is checked by the I-Unit before storing the final results.

Failure to complete the execution of an instruction because of a hardware malfunction results in a machine check condition. Most instructions in the Amdahl 470V/6 repertoire can be automatically retried by the E-Unit. The instruction retry feature attempts to re-execute the failed instruction (in contrast to returning the machine state to a hardware checkpoint). Instructions that cannot be retried or recovered result in a hard machine check, which is handled according to standard System/370 procedures.

INDEX REGISTERS: Sixteen 32-bit general registers are used for indexing, base addressing, and as accumulators.

INSTRUCTION REPERTOIRE: The Amdahl 470V/6 instruction set consists of the complete System/370 Universal Instruction Set, including the five System/370 instructions for Dynamic Address Translation. Two exceptions are the Store CPU ID (STIDP) and Store Channel ID (STIDC) instructions, which differ in their operations because of architectural differences between the System/370 and the Amdahl 470V/6. In the Amdahl 470V/6, a machine check extended logout (MCEL) is performed by the Console Processor in its own memory,

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▷ In each of the three cases, the Amdahl equipment replaced the IBM system as the sole central processing equipment in the installation.

One of these Amdahl customers was executing under a specially designed operating system, while the other two were in the process of transferring standard IBM system software to the 470V/6. The IBM system software products already running on or planned for the Amdahl equipment included OS/VS2, IMS, OS/MVT, and VM/370.

All three respondents affirmed that except for minor modifications for handling machine check error recovery conditions (which Amdahl supplies for standard IBM operating systems), the Amdahl system required absolutely no changes in any system software or user programs. All three installations also reported that they had encountered no problems in running their communications applications. The two users who were executing under IBM system software planned to receive future releases of the IBM software through Amdahl and to rely on Amdahl and their own in-house technical personnel for technical support of the software.

According to these three users, the Amdahl 470V/6 was extraordinarily easy to install; in the words of one, "We just slapped it right in." That system was delivered on Monday and began handling the site workload on Friday morning. The 470V/6 itself was operational in less than a day, but the installation was also replacing IBM peripheral gear with plug-compatible disk drives and magnetic tape units. A spokesman for another Amdahl 470/V6 installation stated that there were "very, very few problems" in installing the equipment. After the power distribution unit and the cabling were installed, only about 12 hours were required to install the hardware and to complete running the diagnostics. One installation reported some initial problems with bugs in the early console diagnostic routines, but added that Amdahl has already replaced the console programs with new versions.

One respondent observed that hardware maintenance people must have had a say in the design of the system because of the many aids incorporated in the hardware to facilitate diagnostic and maintenance procedures.

Only one of the three Amdahl 470V/6 installations interview by Datapro had had time to begin to compare the performance of Amdahl computer with the replaced IBM system in its own environment, and this installation's initial measurements indicated that the Amdahl processor is, at the very least, clearly faster than an IBM 370/168.

Even though these Amdahl customers were still in the early phases of implementation, all three described themselves as extremely pleased with the equipment. To quote one satisfied user, "It's the best thing in the world on the market right now."□

▶ whereas in the System/370 the address in main memory and size of the machine check extended logout are dependent on the central processor model and control

register information. Since the MCEL on the 470V/6 is made to the Console Processor, the MCEL length field stored by the STIDP instruction is all zeroes. The model number is 0470. The STIDC instruction stores zeroes for a channel model number because all Amdahl channel types are implicit in CPU type. According to Amdahl, no system or application program is likely to be affected by these model dependencies.

INSTRUCTION TIMES: Average execution times, in microseconds, for some representative instructions are as follows:

Add (32-bit binary):	0.065
Multiply (32-bit binary):	0.228
Divide (32-bit binary):	1.625
Load (32-bit binary):	0.065
Store (32-bit binary):	0.065
Add (5-digit packed decimal):	0.423
Compare (5-digit packed decimal):	0.488
Add (short floating-point):	0.195
Multiply (short floating-point):	0.260
Divide (short floating-point):	0.878
Add (long floating-point):	0.260
Multiply (long floating-point):	0.650
Divide (long floating-point):	2.080

OPERATIONAL MODES: Like the System/370, the Amdahl 470V/6 can operate in either the Basic Control (BC) or Extended Control (EC) mode. The BC mode maintains general upward compatibility with the System/360 architecture and programming. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other new system control functions; therefore, the virtual-storage-oriented operating systems must be used.

PROCESSOR FEATURES: The standard timing features of the System/370 architecture are included in the Amdahl 470V/6 Central Processor. These include a CPU timer and a Clock Comparator; the latter provides a means for causing an interrupt when the standard Time-of-Day Clock reaches a program-specified value. Additional instructions are provided to set and store the Time-of-Day Clock, Clock Comparator, and CPU Timer.

The optional Direct Control Feature, as on the System/370, provides six external interrupt lines which operate independently of the normal data channels, plus the Read Direct and Write Direct instructions which provide for single-byte data transfers between an external device and main storage.

The optional Channel-To-Channel Adapter permits direct communication between an Amdahl 470V/6 Processor and a System/370 via a standard I/O channel. It can be attached to either a selector channel or a block multiplexer channel and uses one control unit position on either channel. In an interconnection between an Amdahl 470V/6 and a System/360 or System/370, either system can be equipped with the Channel-To-Channel Adapter, and it is required on only one of the interconnected channels.

The Two-Byte Interface, available as an option for all selector and multiplexer channels, doubles the bandwidth of the data path between the channel and the control units which support this option.

CONSOLE INPUT/OUTPUT

The System Console includes a Data General Nova 1200 minicomputer that acts as a Console Processor, an operator

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▶ control panel, and a CRT display and keyboard. The Console Processor is also equipped with a magnetic disk cartridge that is used by the console operating system and for logout and other functions, a magnetic tape cassette unit for loading diagnostic programs, and a modem to provide for remote diagnostic services.

The console has a direct interface to the central processing unit to allow access to the status of approximately 16,000 system key logic points and setting of control and data registers. The computer-to-console interface allows diagnostic tests to be performed on the central processor modules under control of the Console Processor without regard to the operating condition of the central processor, the I/O channels, or other components of the main system. The System Console is also equipped with a channel interface to a selector or multiplexer channel for operation as a standard console device.

The System Console operates in three modes: the maintenance mode, the hardware command mode, and the device support mode. In the device support mode, the console emulates either an IBM 3066 System Console or an IBM 3215 Console Printer-Keyboard (using the CRT display for output in place of the 3210 matrix printers), and can be connected to either a selector or block multiplexer channel. Functions that can be performed in the hardware command mode include IPL, reset operations, display and modification of the contents of registers and main storage locations, and setting of operating conditions for the system.

INPUT/OUTPUT CONTROL

Each central processor includes 16 standard input/output channels, each of which can be configured as a byte multiplexer, block multiplexer, or selector channel. Each channel can support a maximum data rate of approximately two million bytes per second using the standard one-byte interface or four million bytes per second with the optional two-byte interface. The maximum aggregate data rate for the entire channel unit is approximately 14 million bytes per second.

Each selector-type channel can address up to 256 input/output devices and contains a single implicit channel for addressing one device at a time at burst-mode speeds. An additional 1024 subchannels are available for allocation to byte multiplexer and block multiplexer operations in groups of 64, 128, or 256 subchannels. Channels with either 64 or 128 assigned subchannels can be configured for shared-channel operation. In channels with 64 subchannels, 4 can be shared, while those with 128 subchannels can have 8 shared subchannels. The maximum data rate for single-byte block multiplexer operation is two million bytes per second (or four million bytes per second with the two-byte interface), while channels operating in the byte-multiplexer mode have a maximum data transfer rate of 110,000 bytes per second.

Input/output operations are performed under control of the Channel Unit (C-Unit), which operates independently of central processor operations. The C-Unit consists of three major functional units called the Central Interface Control Logic (CICL), the Direct Access Control Logic (DACL), and the Operation Control Logic (OCL), plus buffers and communications areas and the Remote

Interface Logic which interfaces to control units for any System/360 or System/370-compatible peripheral devices.

The CICL controls the transfer and buffering of data between the Channel Buffer Store and the peripheral devices. It polls the channels every eight cycles for data transfer requests, and transfers data from the Channel Buffer Store to the Remote Interface Logic one or two bytes at a time.

The DACL controls the movement of data between the Storage Unit and the Channel Buffer Store and has a data transfer rate of one word every eight cycles. The DACL is organized as a pipeline to allow overlapping of the functions. It polls each channel every 16 cycles for service requests, concurrently transfers data in both directions between the Storage Unit and the Channel Buffer Store, and reads or stores the results of each transfer operation.

The OCL translates channel commands and coordinates channel program execution for the C-Unit.

A dynamic priority scheme controls the allocation of service to I/O channels. Channels can issue high-priority and low-priority requests for service. Each channel is assigned a 32-byte buffer area in the Channel Buffer Store. Channels with less than half a buffer area remaining are assigned high priority while those with more than half a buffer space available are assigned low priority. The S-Unit resolves conflicts for access to the High-Speed Buffer according to its own internal priority structure, permitting high-priority channel requests to take precedence over central processor requests for access to the High-Speed Buffer. An I/O operation is always executed at a higher priority than buffer prefetch operations.

The C-Unit performs parity checks on all input and output data transfers and on data transfers to the Storage Unit. Other functions include channel indirect data addressing comparable to that implemented on the System/370, and extended channel logout.

PERIPHERAL EQUIPMENT

The Amdahl 470/V6 can utilize all IBM System/360 and System/370 input/output and mass storage devices, as well as their plug-compatible counterparts from independent vendors.

SOFTWARE

The Amdahl 470V/6 offers complete functional compatibility with IBM System/360 and System/370 software. Amdahl Corporation intends to support users of current IBM system software by providing new releases of the software, including minor modifications to account for differences in the way the 470V/6 handles machine check conditions, and by supplying software support services for its customers.

PRICING

The 470V/6 is offered for outright purchase or on a third-party lease. Detailed component prices were not available at this writing. See the Management Summary for prices and configurations of the minimum and maximum 470V/6 central systems.■