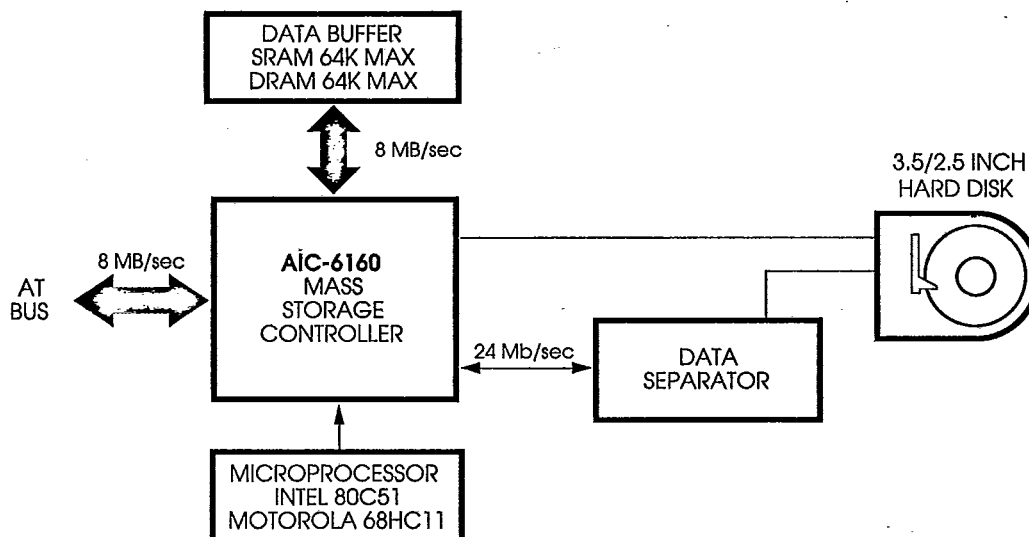*adaptec*

T-52-33-63

AIC-6160

Single-Chip PC/AT Mass Storage Controller

AIC-6160 Typical Application

FEATURES

Host AT Interface

- Up to 8 MBytes/sec data transfer
- Supports PIO and DMA modes
- On-chip 24 mA bus drivers
- Emulates PC/AT disk control for full IBM BIOS compatibility
- Permits two embedded controller drives in a master–slave configuration per system
- 16-byte FIFO for speed matching

Peripheral Interface

- NRZ transfer rate up to 24 Mbits/sec and MFM or (2,7) RLL data rates up to 18 Mbits/sec
- Built-in MFM and 2,7 RLL ENDEC with programmable write precompensation
- User-programmable 32-bit and 48-bit ECC and 16-bit CRC
- Fully programmable 31 X 4-byte sequencer RAM

Buffer Interface

- Supports DRAMs and SRAMs; up to 64K
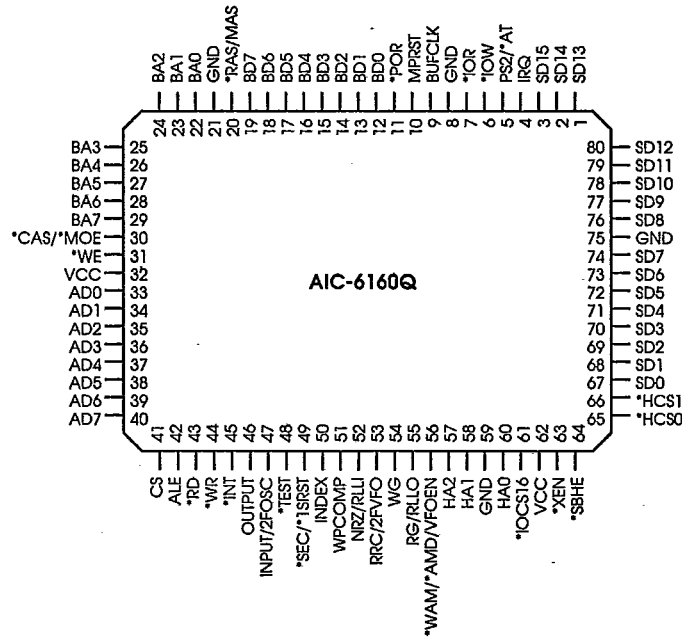- Buffer bandwidth independent of disk rate
- Auto DRAM refresh

Microprocessor Interface

- High-speed multiplexed microprocessor interface
- Fully maskable interrupts
- Direct access to FIFO or buffer memory

Technologies

- High-speed CMOS
- Software compatible to the Adaptec AIC-010/AIC-300 family
- 84-pin PLCC and 80-pin QFP packages
- Software compatible to the Adaptec AIC-6110 Single-Chip Synchronous SCSI Storage Controller

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AIC-6160

AIC-6160 80-Pin QFP Package

Overview

AIC-6160 is a software programmable VLSI chip that provides host bus control, buffer management, encode/decode, and data format control function for a PC AT or PS/2 Micro Channel compatible hard disk, floppy, optical disk or tape controller. With the high integration of the AIC-6160, all the disk control function can be embedded on a disk drive, eliminating the need of a separate disk controller board and offers cost and space reduction in hard disk applications. The AIC-6160 is programmable to allow two hard disk cards or two embedded disk drives to be connected to the host bus.

The AIC-6160 directly connects to the PC AT bus and allows the emulation of the AT disk control register set, ensuring both DOS and BIOS compatibility. It interfaces directly to a microcontroller with a multiplexed address/data bus such as those offered by the Intel microprocessor family.

The AIC-6160 is fabricated in CMOS technology that allows for operation with NRZ data rates up to 24 Mbits/second and Host data rate up to 8 MBytes/second. The CMOS design significantly reduces power consumption requirements and offers improved reliability in addition to permitting embedded controllers to be used in small form factor drives.

The serializer/deserializer and sequencer in AIC-6160 is based on the AIC-010 programmable storage controller architecture. This allows software compatibility with firmware being developed in today's products using the Adaptec architecture. The fully programmable RAM-based sequencer controls various disk control operations such as formatting, reading and writing. The controller section also allows a 32-bit or 48-bit user programmable ECC polynomial for error detection and correction and a fixed 16-bit CRC-CCITT polynomial for error detection only.