SYSTEM REFERENCE MANUAL

ADAGE GRAPHICS TERMINAL

MODEL 5

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System Reference Manual

Adage Graphics Terminal

Model 5

July 1969

TABLE OF CONTENTS

● System Description

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Product Specification

GENERAL

The Adage Graphics Terminal provides the user with a high performance graphics facility. The AGT/5 has a high precision, high speed vector generator and CRT, and a coordinate transformation array for positioning images. The DPR3 processor holds the displayed images, services operator requests, and coordinates communications. A large, easy-to-use console is human engineered to accommodate books, papers, and many options such as joystick and alpha-numeric keyboard. Included at the console are function switches, foot pedals, and a light pen.

TO REMOTE PROCESSOR

COMMUNICATIONS INTERFACE

PERIPHERALS

DIGITAL PROCESSOR

GRAPHICS COORDINATATE TRANSFORMATION ARRAY

VECTOR GENERATOR

CHARACTER GENERATOR

GRAPHICS CONSOLE AND DISPLAY

ASR-33 TELETYPE

LIGHT PEN
ANALOG DATA TABLET *
JOYSTICK *
KEYBOARD *
FUNCTION SWITCHES
VARIABLE CONTROL DIALS *

UP TO FOUR CONSOLES
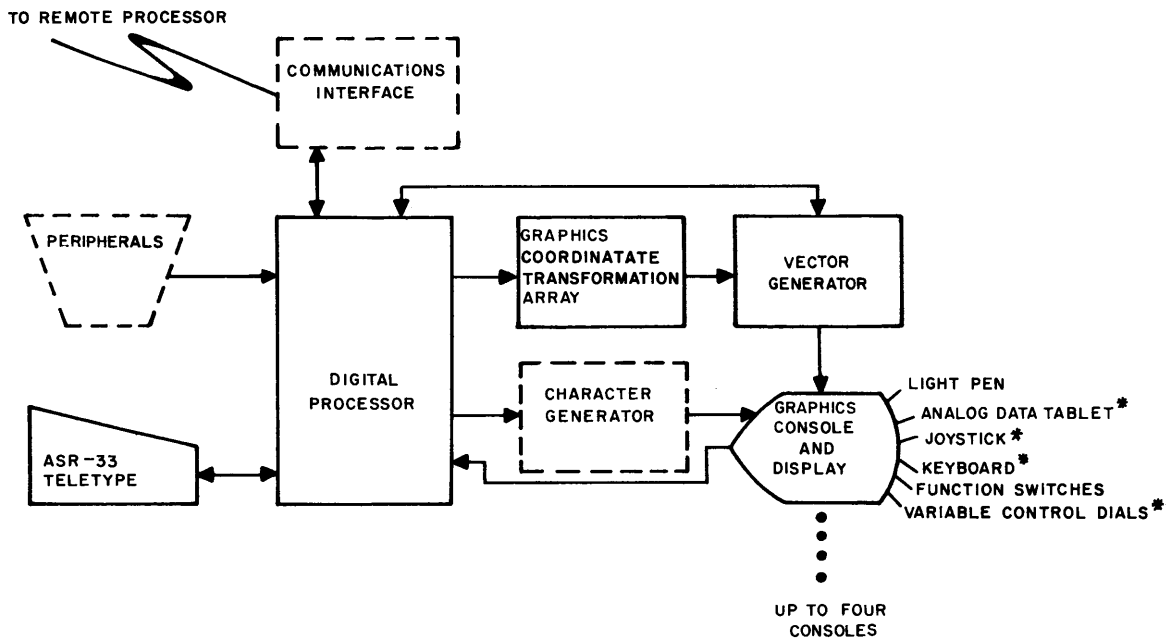
* OPTIONAL

AGT/5 SYSTEM CONFIGURATION

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SPECIFICATIONS

The CRT display, coordinate transformation array and vector generator are described in the following Product Specifications: GDS1, GHA4, and AVG1. The CRT display has a large screen containing a 12" x 12" display area and a 10" x 10" high quality area in which the resolution is greater than 50 lines per inch and the vector endmatching is better than 32 mils. The coordinate transformation array implements the following transformation:

$$X' = X\emptyset + X$$

$$Y' = Y\emptyset + Y$$

The SCF1 option adds hardware scaling capability to the coordinate transformation array (GHA1 replaces the GMA4).

The PIC1-P1 option permits programmed setting of the display line intensity. The vector generator accepts absolute end points of vectors to be drawn; thus, images are specified in transformable form. The vectors are drawn point-to-point, saving memory and providing smooth straight lines. In the AGT/5 the vector drawing rate varies from $5.5\mu s$ for 1/2" x 1/2" lines to $38\mu s$ for 10" x 10" lines. These times include $5.5\mu s$ of required processor time. The remainder of the time the DPR3 is free to continue servicing other devices and programs, since it services the vector generator on an interrupt basis.

The DPR3 processor is described in the DPR3 Product Specification. The DPR3-P1 is included in the AGT/5. Additional memory is available with the M10 options. The DPR3-P1 is a 4K, 30-bit word digital processor with 5 channels of priority interrupt. The memory cycle time is $2.0\mu s$. The 30-bit word provides a flexible 15-bit operation field and a 15-bit address or operand field, permitting direct addressing of up to 32K words.

The DPR3 has 8 word sources to its transfer buss and 16 word destinations from the transfer buss. The source/destination assignments are shown below:

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Table 1.
AGT/5 Source/Destination Assigments

	Source Assignment	Destination Assignment
∅	Memory Data Register	Memory Data Register
1	Accumulator	Accumulator
2	Interface Control Register	Interface Control Register
3	Buffer Register	Buffer Register
4	Sense Lines	Instruction Register
5	Function Switches, ADC	X, Y Data Registers
6	-	Command, Z Data Registers
7	High Speed I/O	X∅, Y∅ Data Registers
1∅	-	Control
11	-	Multiplexer Control
12	-	Line Printer
13	-	-
14	-	High Speed I/O
15	-	Half Word Add
16	-	Full Word Add
17	-	Exclusive OR

The standard systems software package furnished with the AGT/5, called DSS, supports its display function. DSS includes a display file processor, a debugging routine, a text editor, and an assembler. Communications and formatting routines, specific to the host machine, are added to this set of programs. The user has complete access to the capabilities of the AGT terminal via programs written on the host machine. Image files are transmitted to the AGT for processing and display. Control files are used to activate the keyboard and the light pen, and to sample the function switches and any other interactive controls. The editor, assembler, and debugger are provided for support and maintenance of the communications and formatting routines.

The console includes an adjustable scope mount, work space, a light pen, 16 function switches, 2 foot pedals, and a manual interrupt button (PULSE 1).

● Hardware

INTRODUCTION

The DPR3 is a general purpose digital processor having the following features: a 30-bit word length, two-microsecond memory cycle time and a five-channel priority interrupt system expandable to 25 channels. It has an ADD time of 4μs including all memory references. As an option, the DPR3 offers hardware multiply and divide. The DPR3 is used as the terminal processor for the Model 5 Adage Graphics Terminal. In this configuration, the DPR3 is designed to coordinate and control the graphics terminal operation. Many digital peripherals are available with the DPR3 including high-speed paper tape reader/punch, card reader, and line printer.

VERSIONS

The DPR3 is available in the following versions:

Version	Memory
DPR3-P1	4K
DPR3-P2	8K
DPR3-P3	16K
DPR3-P4	32K

The following options are available:

Option	Description
EAU1-P4	Hardware multiply/divide
PRI1-P1	5 additional PRI channels
PRI1-P2	10 additional PRI channels
TTY1-P2	ASR35 in lieu of ASR33

FUNCTIONAL DESCRIPTION

The functional block diagram of Figure 1 illustrates the layout of the DPR3 digital processor. There is the Core Memory Unit, Transfer Buss, Control Unit, Priority Interrupt subsystem, Arithmetic Unit, Buffer Register, Interface Control Register, and the Sense Lines. These subsystems are interconnected by the Transfer Buss as shown in Figure 1.
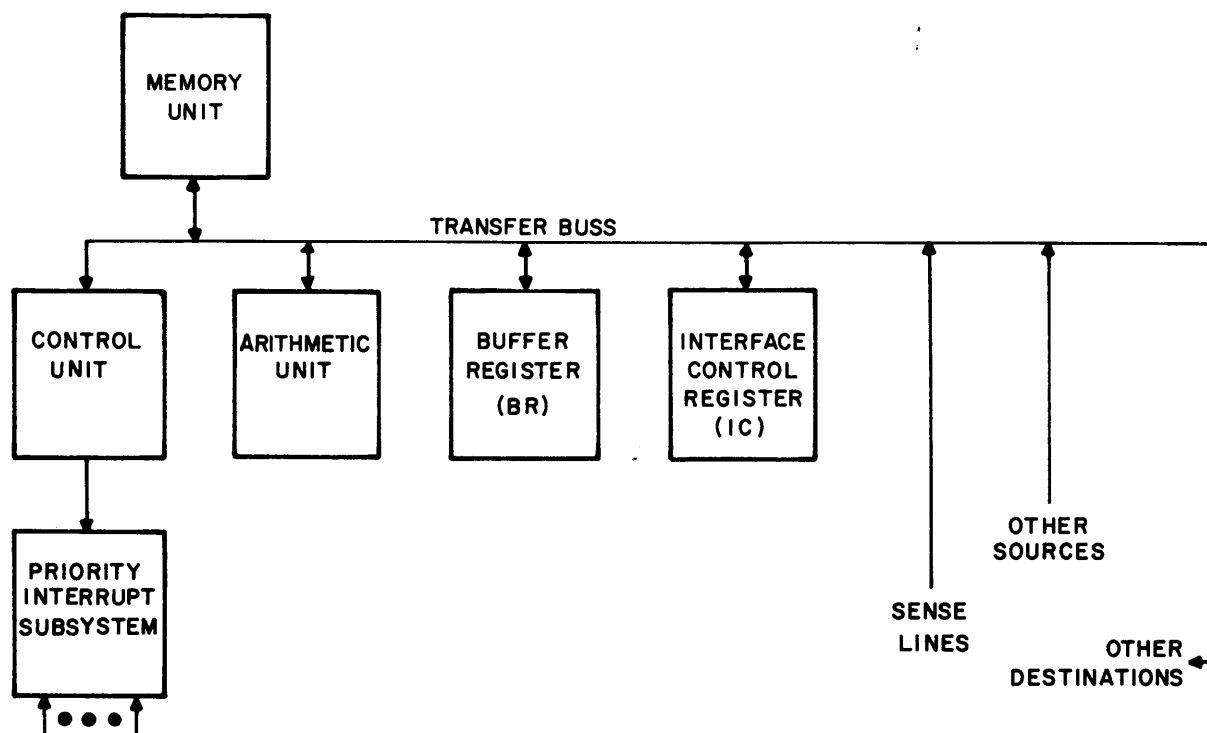
Figure 1. DPR3 Functional Block Diagram

Transfer Buss

The Transfer Buss is a 30-bit path for the interconnection of the system elements. The Transfer Buss accommodates up to eight source registers and up to 16 destination registers. The logical operations AND, OR, and Complement may be done by the Transfer Buss. Also, during a transfer, left rotation of 1, 6, or 15 bits may be performed.

Memory Unit

The Memory unit contains a core memory of 30-bit words with a two-microsecond full cycle time. It can have 4, 8, 16, or 32K words. The Memory Unit contains three registers. The memory data register (MD) is used for holding data going in or out of memory. The memory address register holds the address of the current memory location. The location counter (LC) contains the address of the next instruction to be executed from memory.

Arithmetic Unit

The Arithmetic Unit performs addition, subtraction and Exclusive OR. The Arithmetic Unit may be extended with the EAU1-P4 option to include 15-bit by 15-bit multiply, 30-bit by 15-bit divide, Normalize, left shift, and right shift.

Control Unit

The Control Unit fetches instructions to be executed. It contains the instruction register (IR) and the cycle counters and sequencing logic which drive the processor.

Priority Interrupt Subsystem

The Priority Interrupt Subsystem provides, as standard, five channels of priority interrupt in an absolute hierarchy. The number may be expanded to 25 channels by including the appropriate options. Each priority interrupt channel has an associated 30-bit word input. This word input is executed as an instruction in response to the priority interrupt request.

BR and IC Registers

The Buffer Register (BR) and Interface Control (IC) register are used for buffering and controlling I/O devices such as the paper tape reader/punch, card reader, and communication interfaces.

Sense Lines

The Sense Line inputs provide 30 status bits. Some of these bits are committed for intrinsic system functions, such as testing for arithmetic overflow.

Other Sources and Destinations

The sources and destinations which have not been committed provide 30-bit input paths and output paths which are directly under program control. With the appropriate interrupt control, these paths may be used as high-speed data ports.

INSTRUCTION SET

The DPR3 has a microcoded instruction format which permits great flexibility and efficiency. The general instruction format has 13 bits for the operation code, two bits for indirect addressing and incrementing and 15 bits for address or immediate operand. The indirect bit permits multi-level indirect addressing. The index bit increments the lower 15 bits of the location to be read. This feature allows easy access to data vectors, arrays, parameter tables, and calling sequence arguments.

The instruction set description is divided into arithmetic instructions, control instructions, I/O instructions, and the general microcoded set.

Arithmetic

Arithmetic is performed in ONE's complement by the arithmetic unit. Logical and rotation operations are performed by the transfer buss under control of the control unit.

Two add operations are available, a sign and 29 bit add (extended precision) and sign and 14 bit add (single precision) to the lower half of AR. The operands are the contents of AR and the value from the transfer buss.

The following instruction implement arithmetic and logic operations.

OP Code	Modifiers	Address Field	Description	Time
MDAR		A	Load accumulator register AR from address A	4us
ARMD		A	Store AR at A	4µs
MDAE		A	Add the contents of A to AR in extended precision	4us
MDAS		A	Add the contents of A to AR in single precision	4µs
MDAE	N	A	Subtract extended precision	4µs
MDAS	N	A	Subtract single precision	4us
MDXO		A	Exclusive OR the contents of A with AR	4us
MDAR	A	A	Mask AR with the contents of A	4µs
MDAR	O	A	OR the contents of A into AR	4µs

OP Code	Modifiers	Address Field	Description	Time
MDAR	N	A	Load negative of the contents of A into AR	4μs
ARXO	F		Clear AR	3μs
MDAS	F		Add A field single precision	3μs
MDAS	F, N	A	Subtract A field	3μs

The EAU1-P4 Option provides the additional instructions:

OP Code	Address Field	Description	Time
MPYU	A	Multiply AR[15-29] by (A[0-14])	4-10μs
DIVU	A	Divide AR[0-29] by (A[0-14])	4-10μs
MPYL	A	Multiply AR[15-29] by (A[15-29])	4-10μs
DIVL	A	Divide AR[0-29] by (A[15-29])	4-10μs
MPYI	A	Multiply AR[15-29] by A	3-9μs
DIVI	A	Divide AR[0-29] by A	3-9μs
ARRS	A	Shift AR right A bits	3-9μs
ARLS	A	Shift AR left A bits	3-9μs
NORM	A	Left justify AR[0-29]	3-9μs
ERAR	A	Transfer (ER) to AR	3 μs

Control Instructions

The instructions which implement change of control, subroutine calls, and conditional tests are in the table below:

OP CODE	Address Field	Description	Time
JUMP	A	Transfer control to location A	3μs
JPAN	A	If (AR) < 0, JUMP to A	3μs
JPLS	A	If (AR [15-29]) ≠ 0, JUMP to A	3μs
JPSR	A	Store Location Counter at A, then transfer control to A+1	5μs
JSLS	A	If (AR[15-29]) ≠ 0, JPSR to A	5μs
JSAN	A	If (AR) < 0, JPSR to A	5μs
SKUA	A	If A ⊙ (S4[0-15]) ≠ 0, SKIP	3μs
SKLA	A	If A ⊙ (S4[15-29]) ≠ 0, SKIP	3μs

I/O Instruction

The OPIO instruction is used to control most digital peripherals. The address field of the OPIO has a six bit device code and a nine bit command for the device.

Some devices such as the console Teletype are turned on and off with an Interface Control (IC) register bit.

In order to enable and to disable interrupts, Freeze PRI and Unfreeze PRI instructions are provided.

General Transfer Instruction

There is a class of instructions which perform logic operations on a destination register with an operand from a source register.

The instruction format contains fields which specify memory addressing mode, source register, destination register, transfer logic, left rotation, indirect addressing and indexing. The DPR3 Subsystem Programming Specifications details the specification and use of the general instruction set. The previously defined instruction classes may be considered subsets of the general definition.

PRIORITY INTERRUPT SUBSYSTEM

The priority interrupts provide the capability for executing an externally supplied instruction upon the occurrence of an external event. This procedure is useful for many real time operations, such as input/output and light pen hit response.

There is a unique instruction associated with each interrupt. This instruction may be dynamically specified depending upon conditions in the interrupting device. Multi-instruction services normally cause a subroutine jump (JPSR) to the service routine. Single instruction services may be used for reading and writing memory locations at 3.0μs per word.

When a subroutine jump (JPSR) is the service instruction for a priority interrupt channel, all lower channels are locked out until the subroutine executes an indirect jump to return to the interrupted routine.

The five channels included in the standard AGT/5 are assigned as follows:

Channel	Interrupt Source
0	Light Pen, Pulse 1 Manual Interrupt
1	Teletype
2	Communications
3	Frame Clock
4	Vector Generator

INPUT/OUTPUT TRANSFER BUSS OPERATION

Digital data transfers over the transfer buss proceed from any of the 8 sources to any of the 16 destination registers under direction of Control Unit. The memory data, accumulator, buffer and interface control necessarily serve as both sources and destinations for program instructions.

Sources and destinations may also be shared among the optional subsystems by one of three methods:

1. Source Multiplexing

2. Assignment of Priority Interrupt Level

3. Use of Discrete OPIO instructions.

In any case, hardware in individual subsystem interfaces prevents presentation of conflicting demands on the DPR3.

The Buffer Register (Source 2 and Destination 2) is a 30-bit parallel register whose function is to provide temporary storage of data for use either internal to the DPR2, or by external subsystems.   Data is strobed into the BR register by a transfer to destination 2.   In this manner, BR can be loaded from any source with the desired Transfer Buss logical operations being performed.   The Interface Control register (Source 3 and Destination 3) is also a 30-bit parallel register whose function is to provide individual interface control bits to the various peripheral units.   In operations, it is identical to BR except that it is not directly displayed on the Operator's Control Panel.

I/O Use of Priority Interrupts

The function of a PRI channel is to cause the execution of a "PRI instruction" in response to a "request" by the device using the channel. A user request causes the PRI instruction to be fetched and placed in the IR (Instruction Register) exactly as if it had come from memory. A user request for service is called an "interrupt" because the main program sequence being run is interrupted for execution of the PRI instruction. If the PRI instruction does not affect the LC (Location Counter), control returns to the main program where it left off after the PRI instruction is

executed. PRI instructions are supplied to the IR from an external instruction buss, called S8 (Source 8). The instructions are usually "stored" in diode matrix cards (CRM1 cards) or hardware registers that are gated into S8 at the appropriate time.

A special Fetch cycle, called FPI or Fetch Priority Instruction, is used when a PRI instruction is fetched. This FPI cycle is only 1 microsecond in duration. The first Execute cycle of a PRI instruction will be extended from 1 to 2 microseconds if that Execute cycle is an immediate Execute cycle (normally 1 microsecond). Thus, the execution time for a PRI instruction is 3 microseconds.

There may be up to 25 PRI channels in a fully expanded system and each channel has a "priority" with respect to the other channels. The channels are num numbered from 0 to 24 and priority is inversely proportional to channel number. If several channels request service at the same time, the highest priority channel is serviced first; when its service is done the next highest is serviced, and so on. It is possible for any one channel to repeatedly ask for service and thus delay all lower channels until it is through.

If a channel's PRI instruction is any machine instruction except any Jump Subroutine, the channel's service consists simply of the execution of that instruction. If the PRI instruction is a Jump Subroutine, the service is considered to consist of execution of the whole subroutine involved. (The end of the subroutine is defined to be the execution of the first Jump Indirect instruction or successful conditional jump after the Jump Subroutine). A higher priority channel may interrupt a subroutine on a lower channel immediately. Because of the subroutine linkage provided by a combination of Jump Subroutine and Jump Indirect instructions, it is possible for the PRI to keep track of any number of "simultaneoisly in process" subroutines if lower channel subroutines are successively interrupted by higher channel subroutines.

Two special instructions affect the PRI subsystem. Execution of FPRI (Freeze PRI) special instruction causes execution of PRI instructions to be locked out. Any requests pending before the execution of FPRI are stored and serviced only when the PRI is unlocked by a UPRI (Unfreeze PRI) special instruction. UPRI causes the PRI to be unlocked and service proceeds in the normal way.

OPIO Special Instructions in I/O Operations

The OPIO Special Instruction is used for both controlling and sensing peripheral devices and interfaces. The instruction is normally 6 microseconds long (without indexing and indirect cycles), the extra two microseconds being obtained by blocking completion of the first execute cycle. When OPIO is fetched and executed, a 1.5 microsecond peripheral strobe pulse is generated during the first execute cycle. Peripheral devices use the pulse as a signal to decode the input from the Transfer Buss as the address field of the OPIO instruction (modified by the T field). This address field contains a 6-bit device code and a 9-bit command code which tells the selected device what operation to perform.

If the selected device raises its event line, a second execute cycle will be a sequential memory cycle which increments the LC by 1 and thus skips an instruction. If the event line is not raised, no memory cycle takes place.

OPERATOR CONTROLS

In addition to the graphics I/O devices available at the display console, operator control of Digital Processor is available at the console teletypewriter, operator's control panel and the maintenance panel of the memory unit.

Teletypewriter(TTY)

The Teletypewriter is the principal operator I/O device for communication with the DPR3. The TTY1 (Model 33-ASR shown in Figure 2) is the 10 cps teletypewriter and paper tape reader/punch included with the AGT processor. The TTY1-P1 (Model 35-ASR shown in Figure 3) substitutes heavy duty typewriter for standard ASR-33.
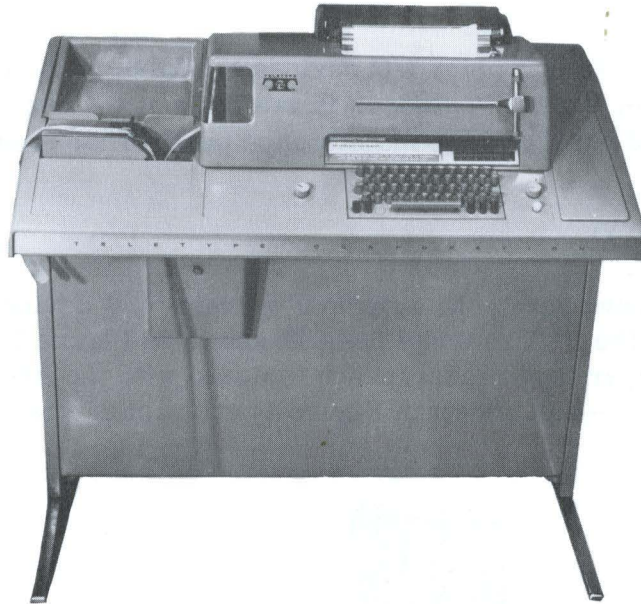
Figure 2. TTY1 (Model ASR-33) Teletypewriter

Figure 3.   TTY1-P2 (Model ASR-35) Teletypewriter

Operator's Control Panel (OCP)

The Operator's Control Panel contains switches, indicators, and controls for a programmer or operator to control and communicate with the Digital Processor, see Figure 4.   The functions provided are described below.   "I" denotes a lighted indicator and "S" denotes a switch.
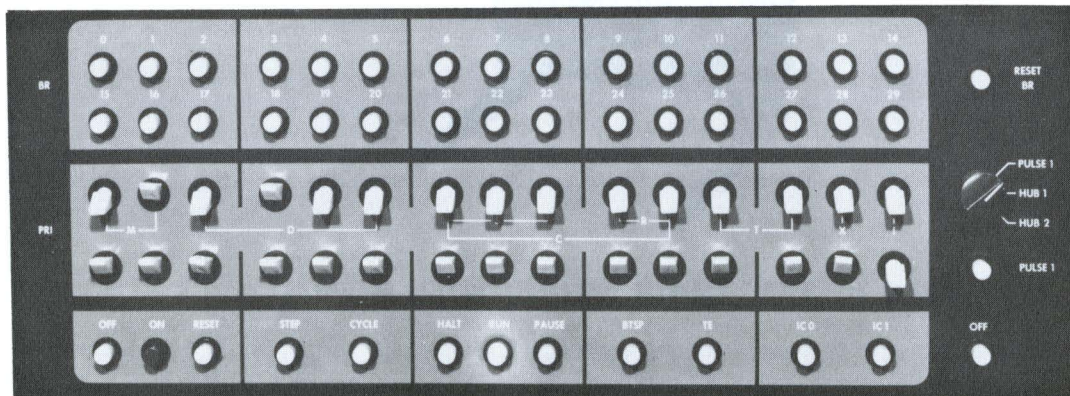

Figure 4.   OCP Operator's Control Panel

1.   BR Display (I/S)

This is a 30-bit display using push button lights.   The lights indicate a static display of the Buffer Register.   Depressing a push button will cause the corresponding bit of BR to be set.   In conjunction with the PRI Instruction Register, this register may be used to display any machine source and to load words to any destination.

2.   RESET BR (S)

Depressing this push button causes all bits of BR to be reset to ZERO.

3.   PRI Instruction Register (S)

This is a 30-bit toggle switch register which may be used as a PRI instruction source.   The request for this source is generated by PULSE 1 (see item 5) or by an external device through HUB1 or HUB2.

4.   Request Selector (S)

A three-position rotary switch selects PULSE 1, HUB1 or HUB2 as a request source on the PRI channel using the PRI Register as a source.   HUB1 and HUB2 can be used to receive request signals from external devices.

5.   PULSE 1 (I/S)

Depressing this push button causes the generation of a PRI request on a channel which uses the PRI Instruction Register as its source.   The indicator is lit while the request awaits service.   Depressing the switch when the indicator is lit turns off the request and the indicator.   PULSE 1 is only active when it is selected by the Request Selector.

6.   OFF (S)

Two OFF push buttons are provided.   Both of these must be depressed simultaneously in order to disconnect a-c power.

7.   IC Control Bits 0, 1 (I/S)

Bits [0] and [1] of the IC register are displayed on the panel.   These bits may be set by pushing the switch associated with the display; resetting must be programmatic or by RESET.

8.   TE (Teletype Error) (I/S)

This indicator lights when the teletype generates an interrupt before its previous interrupt is serviced.   The indicator is reset by the switch, programmatically, or by RESET.

9.   BTSP (Bootstrap) (I/S)

Depressing the BTSP push button causes the machine to alternately enter or leave the Bootstrap input mode, i.e., to complement the Bootstrap state.   Upon entering the Bootstrap mode, the PAUSE mode is established and IC bit [28] is set (teletype read in with printing inhibited).   Entering Bootstrap also establishes the appropriate interrupt requests for reading Bootstrap paper tapes.   Depressing RESET will turn off the BTSP indicator and establish the non-Bootstrap mode.

10.   PAUSE (I/S)

This is a push button which causes entry to the PAUSE mode.   PAUSE enables the fetching of PRI external instructions only.   If a PRI request is present in the PAUSE mode, the external instruction will be the first instruction to be fetched.

11.   RUN (I/S)

RUN initiates continuous operation, starting with the fetch of an instruction from memory.   If a PRI request is present, the external instruction will be the second instruction to be fetched.

12.   HALT (I/S)

HALT establishes the HALT mode by stopping the machine cycle counter at the end of the current program step.

13.   CYCLE (S)

Depressing the CYCLE while in the HALT mode causes one machine cycle to take place.

14.   STEP (S)

Depressing the STEP button while in HALT mode causes one instruction to be fetched and executed.

15.   RESET (S)

This is a push button which establishes a safe and reproducible starting point for system operation and causes entry to the HALT mode.

16.   ON (I/S)

Depressing the ON push button activates the Power Sequencer which brings up Main Frame power, turns on the DME Digital Core Memory, and removes the SMR System Reset.   The Digital Processor is then activated in the HALT mode.

GENERAL

The AVG1 Vector Generator takes analog signals which specify the desired end points of vectors and converts them to properly shaped signals for driving the horizontal, vertical, and intensity inputs to the display scope used. The AVG1 usually receives its analog input signals from one of the Adage hybrid arrays. Digital control signals may be received directly from the DPR2, as in the Models 10 and 30 Graphics Terminals, or from a specialized controller such as the Extended Image Processing Unit in the Model 50.

The AVG1 accepts analog input signals corresponding to a 20-inch display space; however, the longest component that may be displayed in one stroke is 10". Vectors cannot be displayed outside of a 12" x 12" square on the standard GDS1 viewing scope. (For vectors which would extend beyond this boundary, the drive signals are automatically clamped.) The average spot position over any six-second interval must be within the 10" square.

The vector generator has many modes so as to maximize the data rate to the scope; these modes are set by the DPR2 or Extended Image Processor. Some of the typical measures of performance follow.

1. Up to 4550, 2D, short vectors (less than 0.5 inches in X and Y components) can be displayed (both draw and move vectors are counted) at a flicker-free rate of 40 frames per second.

2. In the normal modes (not short), the drawing time is automatically selected to maintain nearly the same spot velocity for X, Y and Z components between 0.5 and 10 inches. The drawing time varies from 5 microseconds to 39 microseconds, including the minimum of three microseconds between the end of one displayed vector and the beginning of the next vector.

3. When a vector is used to position, (move) X, Y, Z components between 0.5 and 3.0 inches require the same time per vector as when the beam is intensified. A "move" with any X, Y or Z components which are greater than 3 inches up to 10 inches requires a total of 15 microseconds including three microseconds from the end of the move to the beginning of the next vector.

4. In the normal 2D mode where vector lengths may vary and where draw/move and end of list flag bits are imbedded in the data list, up to 2,940 vectors with one-inch components, 1,660 vectors with three-inch components, or 800 vectors with seven-inch components, may be drawn at 40 frames per second.

5. In the normal 3D mode where vector lengths may vary and where draw/move and end of list command words are included in the data list, up to 1,660 vectors

AVG1-P2

The standard vector generator with an additional Z channel. X, Y, and Z coordinates
are accepted at the inputs. The Z input is used to produce a variation of intensity
with Z as the vector is drawn, thus providing depth cueing. Drives the GDS1 display
scope and one AVS auxiliary scope.

OPTIONS

MSD1-P1

A module which may be added to either the AVG1-P1 or the AVG1-P2 to provide
outputs to the 3rd and 4th auxiliary scopes.

<u>NOTE</u>

For the Product Specification for the AVG2, see
EIP1/PRS.

GENERAL

The GHA4 Graphics Coordinate Transformation Array provides hardware for positioning two-dimensional vector image descriptions. Position values (DX, DY) are loaded into the array registers directly from the DPR3 processor. Each X, Y pair of vector coordinates (end-points) passed through the array are transformed into new coordinates X' and Y' which are the end points of the vector to be drawn. Parameters in the array registers can be quickly changed by loading new values into the array registers. See Figure 1.

The transform equations are:

$$X' = DX + X$$
$$Y' = DY + Y$$

When any of the joystick (JSB1), Adage Data Tablet (ADT1), or function dials (VCD1) options are chosen, an eight-channel multiplexer card and a comparator module are included. The output of the multiplexer is summed with the negative of the X' coordinate transformation array output, and the sum enters the comparator.

The output of the comparator is connected to a sense line of the DPR3 processor. Thus, analog-to-digital conversion is programmed to sample the optional analog devices. An AGT/5 user may implement his own analog devices and may purchase the modules necessary for analog-to-digital conversion.

OPTIONS

1. Programmable Intensity Control   PIC1-P1
2. Eight channels of multiplexer   AMC1-P1
3. Seven additional multiplexer channels   AMC1-P2

SPECIFICATIONS

Digital Input: 15-bit binary values (1's complement for negative numbers).

Settling Time: 2μs to reach .01% of final value.

Analog Outputs: X' & Y'; Z' optional.

Sense Bit: $S = 1$ if $[E_{mx} + X'] < 0$

DPR3

GTI
D5[0:14]
D5[15:29]
ETRD5
D6[15:29]
ETRD6
D7[0:14]
D7[15:29]
ETRD7
DIIs[15:29]
ETRDIIs
SMR

S4[24]

SCU

X
Y
Z
XD
YD
MX

GHA4

X
Y
Z

AVG

ANALOG
INPUTS TO
MULTIPLEXER
CHANNELS

CHO

CHI4
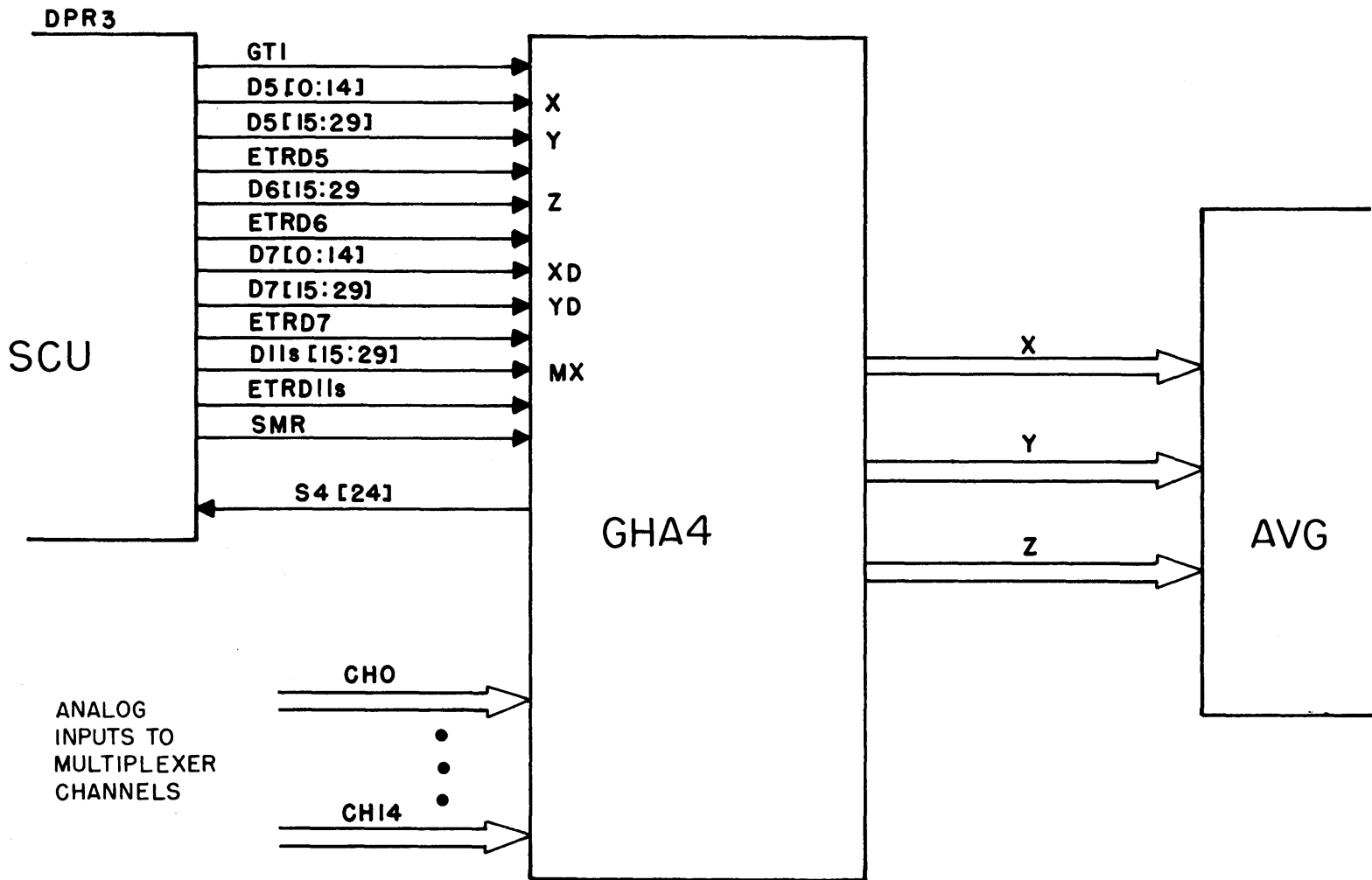
Figure 1. GHA4 Graphics Coordinate Transformation Array,
Subsystem Block Diagram

GENERAL

The BGC2-P1 Basic Graphics Console is the standard operating station supplied with the AGT/5 Adage Graphics Terminal. It consists of the following items:

1. A GDS1 Graphics Display Scope mounted in a low, adjustable scope frame.

2. A LPN1 Light Pen.

3. A Function Switch subsystem assembly, FNS1-P1, which includes 16 digital function switches and two foot pedals.

4. Console providing space for options and work materials.

5. Operator's chair.

A second version, the BGC2-P2, is available for use as an auxiliary console. It contains all the features of the BGC2-P1 except the FNS1-P1 Function Switch subsystem.

GENERAL

The GDS1 is a 21" rectangular display scope which may be driven by any of the Adage vector generators or character generators. The scope has a quality viewing area of 100 square inches (10" x 10") and a larger usable area of 12" x 12". All necessary adjustment controls are located behind a panel and are within easy reach of the operator.

Typical spot size is .020" and resolution is in excess of 50 lines per inch. The display has adequate brightness for viewing under even adverse ambient lighting conditions. The brightness of a 10" x 10" raster is at least 2 foot-lamberts at the specified spot size as measured by an SEI Photometer. The resolution is measured by the closest allowable line spacing permitting one to distinguish separate lines without magnification at a distance of one foot from the face of the screen.

Six controls are provided for initial adjustment of the GDS1 display scope. These controls are for horizontal and vertical gain and position, focusing and intensity.

When driven by an AVG1 P1 or AVG1 P2 vector generator subsystem, all end points of lines will be within 20 mils of their correct values. The linearity will be 1% of full scale along a major axis in the 10" precision square.

Blanking circuitry is provided as part of the GDS1 subsystem. The circuitry is physically located in the AVG1-A unit. The blanking is controlled by the following bits:

Scope A — Destination 10, bit 6
Scope B — Destination 10, bit 7
Scope C — Destination 10, bit 8
Scope D — Destination 10, bit 9

The GDS1 display scope requires 115 v ±10% 50-60 a-c power at 500 watts. For the power requirement of the control circuitry, see the AVG1 specification.

GENERAL

The FNS1 Function Switches provide several very flexible means of communicating with the computer. A small box easily positioned anywhere on the operator's work area contains 16 function keys and a PULSE1 pushbutton. Two foot pedals are also provided; the input function of these pedals is identical to that of the function keys. The function keys and foot pedals may be read by the program at any time. The PULSE1 switch is wired in parallel with the PULSE1 switch on the DPR operator's control panel. Associated with each function key is a label on an easily prepared, easily changeable overlay.

A second version of the function switch box has a light associated with each function key. These lights are connected as DPR destination bits and are controlled by the program rather than by the associated switch.

VERSIONS

FNS-P1: 16 function keys with labels,
2 foot pedals, 1 PULSE1 switch

FNS-P2: 16 function keys with labels and lights,
2 foot pedals, 1 PULSE1 switch

GENERAL

The LPN1 Light Pen subsystem is an input device which is used in conjunction with a display oscilloscope. Up to four light pens may be used in an AGT system. Each pen has associated with it an enable bit, a hit bit, and a fingertip switch on the light pen barrel. When the fingertip switch is depressed and the enable bit is set programmatically, the light pen will set its hit bit if it detects a light pulse. The setting of any one of the four hit bits causes a machine interrupt on PRI Channel 5; the instruction is JPSR'I 77760. Hit bits must be reset programmatically.

MACHINE ASSIGNMENTS

Light Pen	Enable Bit	Hit Bit
#1	$D10_8$ [10]	IC [15]
#2	$D10_8$ [11]	IC [16]
#3	$D10_8$ [12]	IC [17]
#4	$D10_8$ [13]	IC [18]

● **Software**

INTRODUCTION

The AGT/5 Adage Graphics Terminal is designed for operation in an environment in which the user software is developed for and resides in a central computing facility.

The central facility provides mass storage and interfaces with the terminal over a communications link.

The user software written for the central computer will assemble tables with messages or pictorial information, command the terminal to receive or return new table areas or to input or output from existing areas, and respond to inputs or conditions activated at the terminal.

The system software for such an application falls into four categories:

1. Central System Programs (written by the user)

2. Terminal Resident Programs (supplied by Adage with each AGT/5)

3. Support Programs (supplied by Adage with each AGT/5)

4. Maintenance Programs (supplied by Adage with each AGT/5)

Central System Programs

Adage supplies a Central Table Builder (in FORTRAN) for building display tables appropriate for display in the display terminal. In addition, user-supplied programs, resident in the central computer, are required to perform the following tasks:

1. Interrupt and activate user programs to service attention conditions or requests arising at the terminal.

2. Accept user program calles to process messages or picture data into formatted tables for transmission to the terminal.

3. Transmit or receive selected tables to or from the terminal as commanded.

4. Process user program commands to control the terminal I/O processing or the transmission of data.

5. Operate the central computer end of the communication link as needed to accomplish items 1 and 3 above.

Resident Terminal Programs

The terminal is operated online with the following three programs resident. The remainder of terminal core is allocated by central user programs into tables for processing.

1. <u>Display Processor - DSIMG</u>

This routine processes specified tables containing control and pictorial data and drives the necessary terminal hardware.

2. <u>Executive - DSRES</u>

This routine performs all I/O and system control. It responds to central commands received over the communication link and generates central attention requests when necessary.

3. <u>Communication Routine - DSCOM</u>

This program operates the terminal-end of the communication link as needed.

Terminal Support Programs

These programs provide a terminal programmer with tools for developing, modifying, or extending the terminal resident software.

1. <u>Console Display Debugger - DSDBG</u>

This routine is designed for use during the debugging of user-written terminal programs. Its facilities include reading and punching programs on paper tape, displaying selected portions of core memory on the CRT, listing portions of core on the TTY, changing the contents of core, and monitoring the execution of all or part of programs in core.

2. <u>Display Editor - DSEDT</u>

This routine is a general purpose display text editor. It permits online interactive development or modification of assembler source program texts but can be used to enter or edit any textual material.

3. <u>Assembler - DSASM</u>

This terminal program is a two pass assembler providing symbolic address locations, parameter assignments, and packing of ASCII character strings.

Terminal Maintenance Routines

Terminal system and subsystem maintenance routines are provided to accomplish the following functions:

1. Calibration and Preventative Maintenance

2. Diagnostic Testing

USER PROGRAMMING

All terminal facilities are used and controlled by central computer user programs which issue commands, respond to attentions, or build tables.

1. Commands

The available commands are:

CALL RESERVE (Size, Terminal Table)

CALL READ (Size, Terminal Table Address, Central Buffer)

CALL WRITE (Size, Terminal Table Address, Central Buffer)

CALL TYPE (Terminal Table)

CALL SHOW (Terminal Table, Frame Rate)

where messages, pictures, or terminal I/O control have been built or received in central buffers for transmission to or from reserved table areas in the terminal.

2. Attentions

An "Attention" request activates user programs to read and process unexpected or exceptional conditions arising at the terminal.

Attention may be activated for triggering on the following conditions:

a. Operator Interrupt (Manual pushbutton "Pulse 1")

b. TTY input character

c. Picture "ATTN" item

d. Pen Interrupt

e. Command Error

f. Show Error

3. Table Building

Four calls are implemented to permit User programs to enter, change, or replace data in central Buffers for transmittal to the terminal. These calls provide for the following types of information:

a. Vector coordinate data

b. Text character strings

c. Picture items (see following)

PICTURE DESCRIPTIONS

All display presented at the Graphics Terminal are generated from "Picture Descriptions" resident in Tables at the terminal.

These are entered, replaced, changed, or modified via WRITE commands in the user program. A given Picture Description is selected for display via the SHOW command.

Picture Descriptions are assembled as a header word followed by a list of picture describing "Items". Each item has an Operation and an Address.

Picture item operations may:

1. Generate visual elements for display (lines, characters, text)

2. Control display generation modes (*multi-scope, dash, short)

3. Effect geometric transformations on display portions (*scale, displacement)

4. Control Picture description processing (jumps, calls, tests)

5. Control Terminal (I/O, variables, attentions)

Picture item addresses may be given as:

1. Immediate (address fied is value)

2. Direct (address is table and location of value)

3. Indirect (address is Table-address of Table-address of value)

4. Relative (address is ± distance to location of value)

* Hardware Subsystem Option

SOFTWARE ITEMS AND REQUIREMENTS

Standard Resident Software/Core Requirements

DSRES	Display Resident Executive	700 words
DSIMG	Display Image Processor	900 words
CSIOT	Central Table Builder	~ 40 Fortran Statements

Standard Support Software

DSDBG	Display Console Debugger
	Version 1: 4K AGT/5
	Version 2: 4K AGT/5 and PRP1
DSASM	Display Assembler
	Version 1: 4K AGT/5 and PRP1
DSEDT	Display Text Editor
	Version 1: 4K AGT/5
	Version 2: 4K AGT/5 and LCG1 Character Generator

Standard Maintenance Routines

DSCPM	Display Calibration and Preventive Maintenance
DSDTP	Display Diagnostic Test Program

User-Supplied Software

DSCOM	Display Communication I/O
CSCOM	Central Communication I/O
CSCMD	Central Command Processor
CSATN	Central Attention Processor
CSDIO	Central Data I/O Handler
CSTFM	Central Table Formatter

GENERAL

This Display Software System program is resident in the Adage Graphics Terminal to interpret the tabular image data structures sent from the central computer as data blocks for displaying two-dimensional pictures on the CRT and controlling Terminal Operation. DSIMG requires approximately 900 words of core DPR3 core memory.

All displays presented at the Graphics Terminal are generated from "Image Descriptions" resident in the terminal core storage. These are entered, replaced, changed, or modified via WRITE commands in the user program on the central computer. A given Image description is selected for display via the SHOW command. Image Descriptions are assembled as a header word followed by a list of picture-describing "Items." Each item has an Operation and an Address.

Image Item operations may:

1.   Generate visual elements for display (lines, characters, text)

2.   Control display generation modes (multi-scope, dash, short)

3.   Effect geometric transformations on portions of the display (scale, displacement)

4.   Control Image description processing (jumps, calls, tests)

5.   Control Terminal I/O (variables, Attentions)

Picture item addresses may be given as:

1.   Immediate (address field is value)

2.   Direct (address is Table and location of value)

3.   Indirect (address is T-address of T-address of value)

4.   Relative (address is ± distance to location of value).

DSIMG operates via the framing clock in the AVG1 at the specified frame rate. Each table image item processed by the program is displayed at the maximum rate specified when performed by the hardware directly. Each item not performed directly by the hardware incurs some overhead in addition to the time necessary to perform the required functions in software.

GENERAL

DSASM is a Display Software System support program used to convert symbolic source programs written in the DSASM assembly language into object programs. The DSASM translator accepts a string of input characters, then outputs machine language instructions and data in machine readable format. The DSASM also outputs error diagnostics. Two passes of the source language input paper tape are made to permit unlimited forward referencing of symbolic addresses.

DESCRIPTION

Symbolic input to DSASM may contain instruction codes, memory addresses, translator operators, text, and expressions in octal, symbolic, or mixed representation. Other features are:

1. Automatic definition of location symbols.

2. Parameter assignment statements.

3. Text conversion and packing.

HARDWARE REQUIREMENTS

AGT/5 subsystem required by the one version of DSASM are as follows:

AGT/5 with PRP1 High Speed Paper Tape Reader/Punch

INTRODUCTION

DSDBG is a Display Software System support program primarily used for debugging user-written programs. Its features include reading and writing programs on paper tape, displaying selected portions of core memory on the CRT, listing portions of core on the TTY, changing the contents of core memory locations, and executing all or part of user programs in core memory.

Entry to this debugging routine causes the saving of the computer's active registers e.g., Accumulator (AR), Buffer (BR), Interface Control (IC), and Location Counter (LC). This register list, known as the "panel," may be displayed and modified by the console operator and is re-instated when the operator requests return to program execution or execution of another program segment.

REQUIREMENTS

Version 1 - AGT/5

Version 2 - AGT/5 with PRP1 High Speed Paper Tape Reader/Punch

GENERAL

DSEDT is a Display Software System support program used in editing alpha-numeric information available in punched paper tape. With this routine, the console operator can, under typewriter control, perform many desired editing functions. DSEDT holds one page of text at a time in its buffer, allowing insertion, deletion, and appending of new text. DSEDT simplifies the preparation of error-free alphanumeric text, such as symbolic programs, from either typewriter input or previously prepared punched paper tape.

HARDWARE REQUIREMENTS

Version 1 - 4K AGT/5

Version 2 - 4K AGT/5 with LCG1 Character Generator

● **Options**

GENERAL

The Adage Data Tablet is a device for entering two-dimensional information into the computer. The working surface of the tablet is transparent glass; thus curves and graphs may be traced into the machine. The pickup stylus has the look and feel of an ordinary pen. The tablet may be used for drawings or graphic inputs and it may also be used with appropriate overlays to implement control switches.

The accuracy and linearity of the tablet over the working area of 10 in. x 10 in. is 5%. The tablet requires one multiplexer channel to an analog-to-digital converter. The linearity can be made better than 1% by best-fit techniques.

VERSIONS

ADT1-P1   For use with the Models 5 and 10 Adage Graphics Terminals. Includes necessary additional multiplexer and analog-to-digital hardware.

ADT1-P2   For use with the Models 30 and 50 Adage Graphics Terminals.

GENERAL

The ANK2 Alphanumeric Keyboard is a small, portable keyboard unit which is easily moved about* on any operating surface. Its functions and key layout are essentially the same as that of the DPR2-TTY1.

The dimensions of the keyboard are approximately $14\frac{1}{2}$" wide by 10" long by 6" high. The maximum input rate is 100 words per minute with automatically locked-out double striking of keys and key repeat function.

The ANK2 permits at least four keyboards to be operated simultaneously with the TTY1 and the display subsystems. Priority Interrupt channel 2, IC[15], and Source 5 bits [0-9] are required for interfacing with the DPR2.

VERSIONS

ANK2-P1:	First Keyboard
ANK2-P2:	Second Keyboard
ANK2-P3:	Third Keyboard
ANK2-P4:	Fourth Keyboard

* The standard cable length between Adage peripheral units and Main Frame interfaces is 35 feet; other lengths are available on special order.

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GENERAL

The AVS1 Auxiliary Viewing Scope consists of a GDS1 Display Scope mounted in an LSF Low Scope Frame (AVS1-P1). Up to three auxiliary scopes may be added to a standard Adage Graphics Terminal. Each such auxiliary viewing scope has associated with it an independent blanking bit which allows the program to determine which scopes shall be on or off at any time.

VERSIONS

AVS1-P1   GDS1 Display Scope in LSF Low Scope Frame

See the GDS1 and AGC1 Product Specifications for a more complete description of these components.

GENERAL

The AVS2 Auxiliary Viewing Scope consists of a GDS1 Display Scope mounted in an HSM High Scope Frame (AVS2-P1). Up to three auxiliary scopes may be added to a standard Adage Graphics Terminal. Each such auxiliary viewing scope has associated with it an independent blanking bit which allows the program to determine which scopes shall be on or off at any time.

VERSIONS

AVS2-P1   GDS1 Display Scope in HSM High Scope Frame

See the GDS1 and AGC1 Product Specifications for a more complete description of these components.

GENERAL

The CDR1 is an AGT peripheral subsystem consisiting of an Interface Unit and a 200-card-per-minute photoelectric Card Reader, with binary and BCD read capabilities. In the binary read mode, columns are transferred, six bits at a time; first the upper six bits, then the lower six bits. In the BCD mode, the standard IBM Hollerith card code is translated into a 6-bit common language code, which is compatible with the standard IBM magnetic tape code, without parity bit.

There are four pivot locations: character, end of card with error, end of card without error, and reader start button.

VERSIONS

The CDR1 has only the P1 version.

READER OPERATION

When the Reader is in the ready condition and the computer issues a read command (sets $IC[6]$), a card is fed to the read station. In the BCD mode, a character request is generated for each column. After the interrupt is acknowledged, the character is loaded into the register ($BR[9\text{-}14]$) by a special instruction ($C10_8$).

In the binary mode, each column is two characters. The top six holes in the column are the first character, and the bottom six holes are the second character. The character interrupt for the second character occurs immediately after the special instruction for the first character service.

Following the last character of a card, in either mode, an end of card interrupt occurs. This end of card interrupt occurs no sooner than 600 microseconds after the last character interrupt.

A read error or a validity error will cause $S4[7]$ to be set.

A skipped character will cause $S4[7]$ to be set.

I/O COMMUNICATION

The CDR1 interfaces directly with the DPR1 System Control Unit through $BR[9\text{-}14]$,

and occupies one PRI channel. PRI pivot addresses (and JPSR'I instruction) are generated within the interface for character, end of card, and start interrupts. IC[6] is used to start a card read operation, and IC[7] to select the mode, binary, or BCD. Two S4 bits are used: S4[7] for a read error, validity error, or for an unanswered PRI request, and S4[6] to indicate that the card reader is in the ready state.

The maximum cable length between the Reader and the interface is 25 feet.

Card Translucency: "Standard Translucency" of punch cards is defined for use in this Specification as the translucency of standard beige cards with row numbers 0-9 and column number 1-80 printed on one face.

The Card Readers covered by this specification can be set by a field engineer at any translucency value from 0 to 150% that of standard. Once set, the reader can read cards in a translucency range of +15% about the set value. Cards in this range can be intermixed.

Note: The Tabco blue cards and the standard are not within the +15% range and cannot be read on this reader when mixed.

Scored Cards: A card scored in any pattern across or on any edge is not to be used on the 200 CPM Card Reader.

Power Samas 80-column cards can be read if all cards are either verified or unverified, not both. A Field Engineer is required to readjust the unit to handle verified after unverified cards, or vice-versa.

GENERAL

The DCM1 Display Comparator performs a programmed picking function. A box approximately 1/2" x 1/2" is defined to exist in X and Y around any chosen position on the display scope. If the beam passes through this area with any Z coordinate while the beam is intensified, an interrupt is generated in the same manner as those from the light pens. Like the light pens, the DCM1 may be disabled programmatically. Coupled with the analog-to-digital conversion capability of the AGT, the DCM1 allows the position of the picking box to be positioned by any input device such as the JSB1 Joystick, the ADT1 Data Tablet, and the VCD1 Variable Control Dials.

OPERATION

The DCM1 is controlled by the OPIO Special Instruction C30 with device code 02_8. The available commands are:

C30 (02, 001) – Load new center position of the picking
box from the BR register.

C30 (02, 002) – Enable interrupt (position is retained)

C30 (02, 004) – Disable interrupt (position is retained)

The center position of the box is strobed out of the BR register by Special Instruction C30 (02, 001). The position data must be present in the BR when this instruction is executed. This position is defined by two eight-bit numbers for X and Y which correspond to the full output range of the AVG1 Vector Generator. The position numbers are in ONE's complement form and occupy bits 0-7 (X) and 15-21 (Y).

The DCM1 interrupts on PRI channel 10 and its interrupt instruction is JPSR'I 77760, the same channel and pivot as used for the four possible light pens in the system. (Any one of the five devices can produce the interrupt.)

The picking box is approximately 1/2" x 1/2", centered at the position last loaded from BR. The size of the box is adjustable by maintenance personnel from approximately a 1/8" square to a 3/4" square.

TIMING CONSIDERATION

From the end of the C30 instruction that enables the interrupt until a hit may actually be detected, there is a delay of approximately 30 microseconds to allow the comparator circuitry to set up. Hits during this time will be missed.

For each entrance of the beam into the hit box there will be one interrupt. Keeping the beam within the box will not cause repeated interrupts.

MECHANICAL

The DCM1 occupies one 5-1/4" assembly in the B2 rack of the AGT and is available on the AGT/10, AGT/30, and AGT/50. All environmental requirements are compatible with other units in the AGT.

GENERAL

The DPI1 is capable of full-duplex transmission/reception of eight-bit characters in conjunction with a communications modem equipped with an Electronic Industry Association (EIA) interface. Data is sent and received in bit serial format between the DPI1 and the modem. The DPI1 is designed to permit operation over a voice grade channel.

The AGT utilizes an I/O control/test instruction (OPIO) to operate DPI1 modes. DPI1 hardware is wired to receive and detect the specific synchronous idle pattern used on the interface between the DPI1 and the remote computer. All other control character recognition and error checking calculations, except vertical parity, must be performed by DPI1 software in the AGT.

VERSIONS

The DPI1 is available in two versions. It assumes a clocked modem such as the Bell 201A or 201B.

Version	Sync. Code	Characteristics
DPI1-P1	026_8	USASCII
DPI1-P2	062_8	EBCDIC

CONFIGURATION

1. Two AGT rack locations.

2. One Priority Interrupt channel.

3. Two memory pivot locations:

   a. Output character (to DPI1).

   b. Input character (from DPI1).

4. OPIO peripheral control instruction.

GENERAL

The GDR1 Graphics Display Recorder allows the operator to quickly make a hard copy recording of the information being displayed on the system display scope. Total cycle time for a finished print is less than 15 seconds; copy area is 8" x 8" on an 8-1/2" x 11" page. A dry development process is used so that the operator need only load paper into the device.

A cycle is initiated by depressing a PRINT switch located on the front of the unit. In less than 25 seconds a finished print is available at an exit chute on the front of the unit. It is possible to expose the paper without developing so that several images may be superposed on a single print.

SPECIFICATIONS

1. Print Characteristics

Print Size:	8.5 x 11 inches
Paper Roll Size:	approximately 545 prints/roll
Copy Area:	8 x 8 inches maximum
Paper Thickness:	.003 inches
Shelf Life:	6 months
Cycle Time:	less than 25 seconds

2. Controls
   ON/OFF
   Out of Paper Indicator
   Exposure Timer
   Ready Pilot Light
   Expose Switch
   Expose & Develop Switch

3. Size
   Unit is free standing and requires approximately 36 x 30 inches of floor space.

GENERAL

The GHA1 Graphics Coordinate Transformation Array provides hardware for scaling and positioning two-dimensional vector image descriptions. A scale factor, SC, and position (DX, DY), are loaded into the array registers directly from the DPR2 processor. Each pair of vector coordinates (end-points) passed through the array are transformed into new coordinates X' and Y' which are the end points of the vector to be drawn. Parameters in the array registers can be quickly changed by loading new values into the array registers, see Figure 1.

The transform equations are:

$$X' = DX + SC * X$$
$$Y' = DY + SC * Y$$
$$Z' = Z$$

When any of the joystick (JSB1), Adage Data Tablet (ADT1), or function dials (VCD1) options are chosen an 8 channel multiplexer card and a comparator module are included. The output of the multiplexer is summed with the negative of the X' coordinate transformation array output, and the sum enters the comparator.

The output of the comparator is connected to a sense line of the DPR3 processor; thus, analog-to-digital conversion is programmed to sample the optional analog devices. An AGT/5 user may implement his own analog devices and may purchase the required modules.

OPTIONS:

1.	Z' output	PIC1-P1
2.	8 channels of multiplexer	AMC1-P1
3.	7 additional multiplexer channels	AMC1-P2

SPECIFICATIONS:

Digital Input:	15-bit binary values (1's complement for negative numbers)
Settling Time:	2 usec to reach .01% of final value
Analog Outputs:	X' & Y'; Z' optional
Sense Bit:	$S = 1$ if $[E_{mx}tX'] < 0$

DPR2

SCU

GT1
D5[0:14]
D5[15:29]
ETRD5
D6[15:29]
ETRD6
D7[0:14]
D7[15:29]
ETRD7
D11s[15:29]
ETRD11s
SMR

S4[24]

X
Y

Z

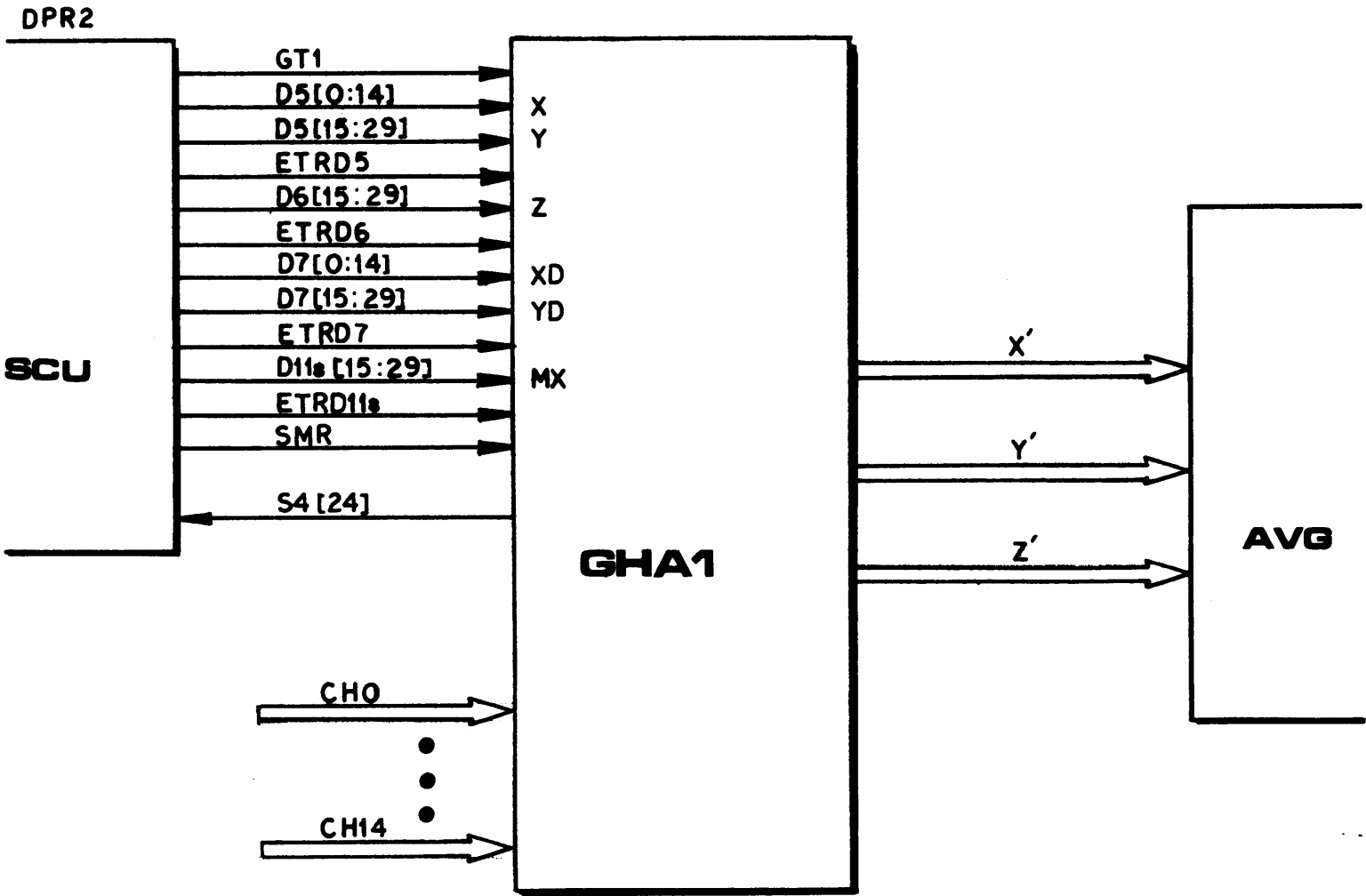XD
YD

MX

GHA1

X'

Y'

Z'

AVG

CH0

CH14

FIGURE 1.   GHA1 GRAPHICS COORDINATE TRANSFORMATION ARRAY
SUBSYSTEM BLOCK DIAGRAM

GENERAL

The HWD1 Windowing Operator accepts six limits in the coordinate system of the Display Scope — upper and lower bounds on X, Y, and Z. The six limits define a rectangular solid. The HWD1 blanks the display whenever the beam is driven outside any of these limits, a special register bit is set. The status of any of these six register bits can be interrogated by the program, and they each can be reset under program control.

GENERAL

The JSB1 is a device for manually entering three-dimensional information into the computer. This is done by moving a handle which protrudes from a small box. There are two handle versions available—one with a small straight stick and one with a 6-inch-diameter hemisphere. Two dimensions are obtained by moving the handle back and forth or left and right. The third dimension corresponds to twisting the handle.

The JSB1 uses 3 multiplexer channels to an analog-to-digital converter.

VERSIONS

JSB1-P1   For use with the Model 10 Adage Graphics Terminal. Includes necessary additional multiplexer and analog-to-digital hardware.

JSB1-P2   For use with the Models 30 and 50 Adage Graphics Terminals.

GENERAL

The LCG1 Character Generator is a high-speed, versatile stroke writer capable of converting digital information into alphanumeric or special symbols, through CRT output.

In the basic LCG1-P1, the Character Generator is set up to produce 64 characters (ASCII code subset). The average display speed (defined as equal to the summation of the display time of all 64 characters divided by 64) is 12.8 microseconds per character in a line format, including spacing and positioning time. Over 2,600 characters can be written flicker-free on the display scope (30 frames per second). At customer option, the LCG1 can be modified to incorporate 32 additional symbols (extended ASCII code or as specified for the particular application).

Twelve control characters (coded compatible with ASCII code) can be used to position the beam, select the character size, shape and brightness, and format the text (line feed, carriage return, superscripts or subscripts). Unless otherwise specified by control characters, successive characters are written to the right of the previous one just as on a typewriter.

The LCG1 takes 5.5 microseconds of processor time to read a 30-bit memory word containing four 7-bit characters and automatically writes these characters on the display scope (or uses them for control) before requesting the next word of data. Once the LCG1 is initiated, word transfers are made automatically from consecutive core memory locations. The return of the control of LCG1 to the program can be made in two distinct ways selected by the setting of the Interrupt bits in the End of List word.

The upper left corner of a list can be positioned either by an initial setting of the horizontal and/or vertical coordinates explicitly specified in the program or in addition by relating it to the last position to which the vector generator brought the beam. The choice is made according to the status of a special control bit.

The interface provides direct communication with the DPR2. The LCG1 requires one Priority Interrupt (PRI) channel.

CONFIGURATION

The LCG1 interfaces directly with the DPR2 using Destination DD, IC register bits X and Y, and one PRI channel. The LCG1 drives up to 4 display scopes, Models GDS1, AVS1, or AVS2.

OPERATIONAL AND ENVIRONMENTAL SPECIFICATIONS

CHARACTERS

Type:	36 gothic alphanumerics plus 28 punctuation and special symbols (ASCII) basic; expandable to a total of 96 characters at option
Writing Technique:	Stroke (function generation)
Writing Speed:	15 microseconds (average over the 64 characters set) to write and space
Aspect Ratio (Height/Width):	3/2
Italics:	Selected by one control character
Character Size:	Three sizes selected by control characters, as follows:

Size 1 — 8 characters/inch horizontally
   3 lines/inch vertically

Size 2 — 6 characters/inch horizontally
   2 lines/inch vertically

Size 3 — 3.4 characters/inch horizontally
   1.13 lines/inch vertically

Character Brightness:	Three levels selected by control characters.

POSITION

Character Position:	On a grid compatible with the current character size when positioning with control characters only. The grid can be moved anywhere on the screen with the vector generator.
Character Spacing:	Automatic, compatible with the character size
Special Formatting Features:	Line feed, carriage return, raise line for superscripts, lower line for subscripts

ENVIRONMENTAL

Compatible with the AGT system

GENERAL

The LPR2 is a 136-column, buffered line printer and interface. Printing is performed one line at a time.   The vertical spacing is 6 lines per inch, and the horizontal spacing is 10 characters per inch.   The buffer/controller contains vertical format control.   The interface provides direct communication with either the DPR1 or DPR2 Digital Processor.   The LPR2 requires one priority interrupt (PRI) channel, two control bits, and two sense bits.

VERSIONS

There are five versions of the LPR2.   The printing speed determines the version.

Version	Printing Speed (64-Character Set)
LPR2-P1	1000 lpm
LPR2-P2	600 lpm
LPR2-P3	300 lpm
LPR2-P4	120 lpm
LPR2-P5	60 lpm

OPERATOR CONTROLS AND INDICATORS

The following operator controls and indicators are located on the front panel of the printer:

ON	–	Power-on switch/indicator.
OFF	–	Power-off switch/indicator.
ON LINE	–	Start switch/indicator. Lights when depressed to place printer on-line.
OFF LINE	–	Stop switch/indicator. Lights when depressed to drop printer off-line. Printer remains on-line until after the buffer is clear and the print cycle complete.

NO PAPER   -   Lights to indicate when paper supply is exhausted or paper is torn.

TOP OF FORM   -   Top of form switch/indicator lights in power-on condition. When pushed, moves paper to top of next form.

INPUT/OUTPUT COMMUNICATION

The LPR2 Line Printer interfaces directly with either the DPR1 or DPR2 Digital Processor, occupying one 30-bit data destination, one PRI service channel, two control bits, and two sense bits. Five separate PRI service instructions are generated within the printer interface for word data transfers, buffer full notification, and error conditions. Parity is checked on the transfer from the interface to the printer.

CHARACTER SET

The LPR2 Printer characters are shown below. These include the ASA Standard FORTRAN Character Set (Communications of the ACM, October 1965).

Printer Character

[(left bracket)	SPACE
% (percent)	A
] (right bracket)	B
! (exclamation)	C
& (ampersand)	D
* (asterisk)	E
: (colon)	F
\ (back slash)	G
+ (plus)	H
< (less than)	I
? (question)	J
" (double quote)	K
' (single quote)	L
> (greater than)	M

Printer Character (cont.)

(	(left parenthesis)	N
)	(right parenthesis)	O
Ø		P
1		Q
2		R
3		S
4		T
5		U
6		V
7		W
8		X
9		Y
;	(semicolon)	Z
=	(equals)	$ (dollar)
,	(comma)	# (number)
–	(minus)	@ (at)
.	(period)	∧ (circumflex)
/	(slash)	_ (underscore)

PHYSICAL DIMENSIONS

Printer

Width: 48 in.
Height: 54 in.
Depth: 41 in.

Interface

The interface requires 5-1/4 in. of cabinet space.
The maximum cable length between the interface and the printer is 75 ft.

POWER REQUIREMENTS

Printer

115V ± 10%
60 Hz ± 1 Hz, single phase
30A service

Interface

The interface uses DPR1 or DPR2 digital voltages

OPERATING ENVIRONMENT

Temperature: 60°F to 85°F
Relative Humidity: 40% to 60%

GENERAL

The PRP1 subsystem is comprised of a high speed paper tape interface, paper tape reader, a paper tape punch or both depending on version.

VERSIONS

There are nine versions of the PRP1. The version determines the paper tape equipment included.

Version	Equipment
PRP1-P1	Paper Tape Reader
PRP1-P2	Paper Tape Reader with Tape Spooler
PRP1-P3	Paper Tape Reader with Fan Fold Bins
PRP1-P4	Paper Tape Punch
PRP1-P5	Paper Tape Punch with Tape Spooler
PRP1-P6	Paper Tape Punch with Fan Fold Bins
PRP1-P7	Paper Tape Reader and Punch
PRP1-P8	Paper Tape Reader and Punch with Tape Spooler
PRP1-P9	Paper Tape Reader and Punch with Fan Fold Bins

Paper Tape Reader

This photoelectric reader may be operated at a reading speed up to 300 characters per second.

Paper Tape Punch

This solenoid operated device may be operated at any speed up to 60 characters per second.

INPUT/OUTPUT COMMUNICATION

The PRP1 interfaces with the DPR2 Digital Processor, occupying eight bits of the buffer register on a shared basis and one priority interrupt (PRI) channel. It is selected and controlled by decoding the address and command portions of the I/O special instruction (C30).

GENERAL

The TCI1 Telephone Communication Interface controls full duplex data transfers between an Adage Graphics Terminal and a remote CDC 6674 Data Set Controller and is designed to operate with common carrier broad band equipment.

The Data transfer occurs upon receipt of an external clock at up to 50 kilobaud in bit serial format. Interrupts and status conditions are used by the TCI1 to inform programs of incoming/outgoing characters and busy/error conditions. Receiving or transmitting modes are defined to the TCI1 by dedicated Interface Control (IC) register bits.

VERSIONS

TCI1-P1 operates at any broad band serial rate to 50 kilobaud.

CONFIGURATION

The TCI1 interfaces to the DPR2 as follows:

1. One interrupt channel is shared among four pivots to indicate:

   a. start of incoming message (SOM)
   b. incoming character available (ICH)
   c. outgoing character needed (OCH)
   d. check of status conditions needed (CST)

2. One sense line (S4). Status conditions available are:

   a. Busy
   b. Access Error
   c. Transmission Error (valid following Redeive Mode only)
   d. Transmission acknowledged (valid following Transmit Mode only)
   e. Action requested (valid in Inactive Mode only)

   The BUSY status condition appears on S4 (15). The remaining status conditions are loaded into BR with a CST interrupt and special instruction.

3. Buffer Register BR [18-29]

adage

WIDEBAND TELEPHONE LINE INTERFACE, TLI1

Product Specification

GENERAL

The TLI1 Wideband Telephone Line Interface is designed for full-duplex use with synchronous communication modems at speeds from 2 Kilobaud to 50 Kilobaud. Versions are available for use with a basic eight-bit character size (including seven-bit ASCII plus parity bit) or a basic six-bit character size.

Hardware provides accumulation under software control of the message block check character (BCC) as either a Longitudinal Redundancy Character (LRC) or as a specific cyclic check character. Also, hardware scan of up to 15 defined control characters allows receive software to identify these characters rapidly. Each received character produces an interrupt. Should transmit software not respond to a Transmit Interrupt, the hardware transmits a synchronous idle pattern.

TLI1 VERSION TABLE

Communication Interfaces:	Bell 301/303	MIL STD 188B	RS 232B (Bell 201)
USASCII with BSC* Conventions	P1	P6	P11
EBCDIC with BSC* Cinventions	P2	P7	P12
TRANSCODE with BSC* Conventions	P3	P8	P13
CDC 6673, 6674	P4	P9	P14
Univac 1108	P5	P10	P15

HARDWARE REQUIREMENTS

1. One Prioity Interrupt Channel
2. Three Memory Pivot Locations
   a. Transmit – Next Operation
   b. Receive – Control Character
   c. Receive – Data Character
3. OPIO Peripheral Control Instruction
4. AGT BR Bits [22-29] or [24-29]

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*Binary Synchronous Communications (IBM Systems Reference Library A27-3004-0)

GENERAL

The TRB1 is a device for manually entering three-dimensional information into the computer. This is done by moving a ball which protrudes from a small box. Two dimensions are obtained by rotating the Track Ball around orthogonal horizontal axes, and the third dimension by rotating about the vertical axis.

The TRB1 uses three multiplexer channels to an analog-to-digital converter and may be substituted for the JSB1 Joystick and Bowling Ball.

VERSIONS

TRB1-P1   For use with the Model 10 Adage Graphics Terminal. Includes necessary additional multiplexer and analog-to-digital hardware.

TRB1-P2   For use with the Models 30 and 50 Adage Graphics Terminals.

GENERAL

The VCD1 computer input device consists of a control box which serves as a mounting for six potentiometers. Each potentiometer is connected to a multiplexer channel and may thus be sampled by the computer. Such potentiometers are useful for continuously changing almost any program variable. Combined with function switches, variable rates or coarse and fine adjustments may easily be programmed. The control potentiometers require six multiplexer channels to an analog-to-digital converter.

VERSIONS

VCD1-P1   For use with the Model 10 Adage Graphics Terminal. Includes necessary additional multiplexer and analog-to-digital hardware.

VCD1-P2   For use with the Models 30 and 50 Adage Graphics Terminals.