YM3613B

Digital Audio Interface Transmitter (DIT)

■ OUTLINE

The YM3613B is an LSI device used for signal processing in order to output Voice Digital signals of a CD player to the external world. Digital signal output to the external world enables Digital Audio Interface Format signals to be output without requiring a special externally-mounted circuit. This YM3613B has a built-in PLL (Phase-Locked Loop) circuit, which synchronizes the sampling frequency that is input to this LSI device to 44.1KHz.

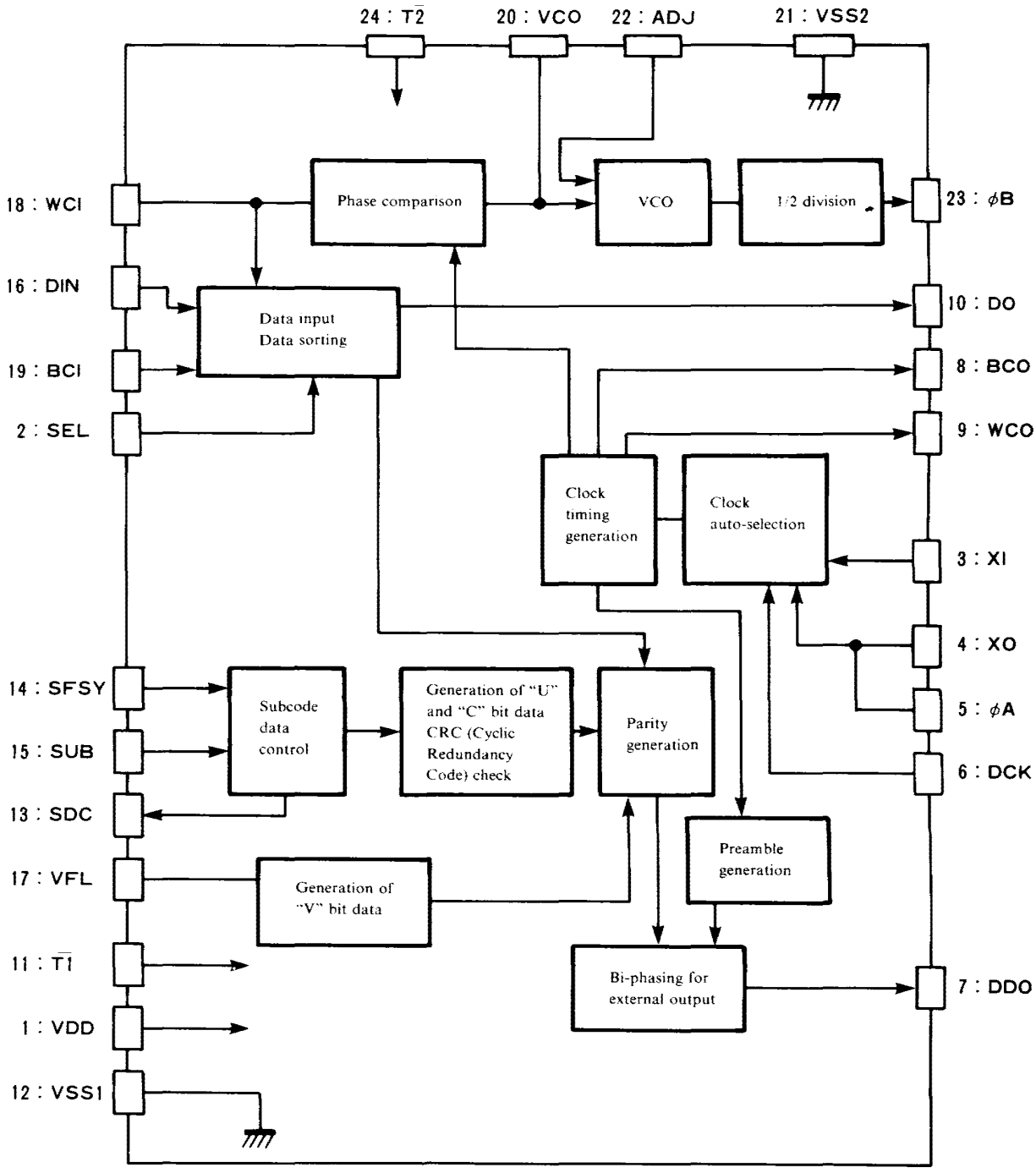
■ FUNCTIONS AND FEATURES

1) Reference clock output and internally required Timing signals can all be generated by merely connecting a liquid crystal.
2) The YM3613B has a function for switching the format of the 16-bit serial Voice signal input, so that the data can be output using the Digital Audio Interface format regardless of whether it was input started from the MSB or LSB.
3) Its built-in PLL circuit outputs clocks of a central 8.6436MHz frequency in accordance with the input frequency of the WCI pin.
4) The YM3613B outputs the External Digital signals of the Digital Audio Interface format.
5) The Subcode input terminal permits Subcode data to be read automatically.
6) Since the "Q" bit of Subcode data is subjected to a CRC (Cyclic Redundancy Code) check, the Channel status of the Digital Audio Interface is affected only when the CRC check on the "Q" bit tests positive.
7) Silicon gate CMOS construction (low power consumption)
8) 24-pin Dual-Inline Package (DIP)
9) +5V power supply

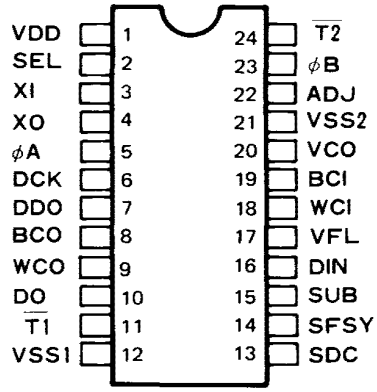
NIPPON GAKKI CO., LTD.

V6366カタログ
CATALOG No. : LSI-2136131
1987.4

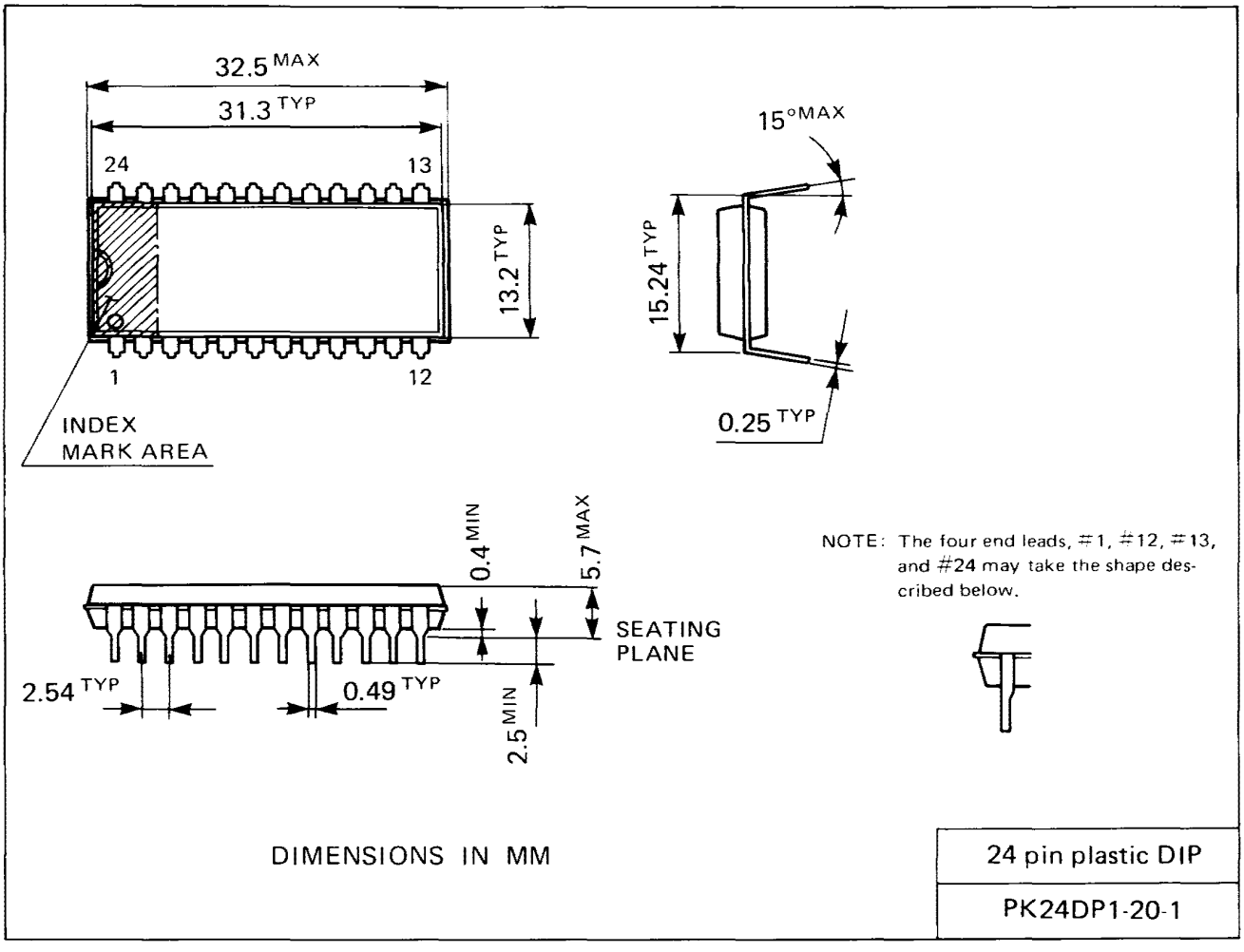
■ BLOCK DIAGRAM



■ PIN ASSIGNMENT DIAGRAM



■ EXTERNAL DIMENSIONS



■ TABLE OF PIN FUNCTIONS

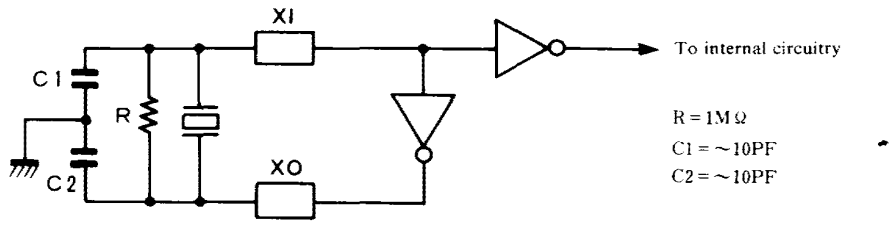
The asterisk in the I/O column indicates that the terminal is pulled-up internally.

Pin No.	Pin Name	I/O	Function
1	VDD		System power supply (+5V)
2	SEL	*I	Switches the data input to the DIN pin to MSB-first or LSB-first format. "H": MSB first "L": LSB first
3	XI	I	Connection (input) pin for the crystal oscillating element (16.9344MHz)
4	XO	O	Connection (output) pin for the crystal oscillating element.
5	øA	O	Output for crystal oscillation (16.9344MHz).
6	DCK	*I	External clock input. Switching from the crystal clock is automatically performed.
7	DDO	O	Outputs Bi-Phase signals for external digital output.
8	BCO	O	Timing clocks for the DO pin. DO output data changes at the rise or fall of BCO. (2.8224MHz)
9	WCO	O	Indicates the L or R channel and is synchronized to DO output. "H": L channel. "L": R channel.
10	DO	O	Serially outputs 16-bit Voice data starting from the MSB.
11	$\overline{T1}$	*I	Used for checking the internal circuitry and is not to be connected.
12	VSS1		System GND.
13	SDC	O	Timing clock for reading the Subcode data. Eight clocks are output after SFSY goes "L".
14	SFSY	*I	Indicates the presence of Subcode data at the SUB pin. When SFSY = "L", it indicates the leading bit of the Subcode data.
15	SUB	*I	Subcode data input. Serially inputs Subcode data in a "P"-"W" sequence.
16	DIN	I	16-bit Serial data input.
17	VFL	I	Indicates the presence/absence of errors in Voice data that was input from the DIN pin.
18	WCI	I	Indicates the L or R channel synchronized to the input Voice data of the DIN pin. "H": L channel. "L": R channel.
19	BCI	I	Input Voice Data Timing clocks of the DIN pin. The Voice data is input at the rising edge of BCI when SEL = "H" or at the falling edge of BCI when SEL = "L".
20	VCO	I/O	Externally-mounting capacitor pin for the internal VCO circuit.
21	VSS2		GND for the VCO circuit. To be connected in common with VSS1, since it is not commonly connected in the LSI.
22	ADJ	I	Used for adjusting the VCO oscillating frequency. Not to be connected.
23	øB	O	Clocks for VCO output. (8.643MHz)
24	$\overline{T2}$	*I	Used for checking the internal circuitry, and is not to be connected.

■ DESCRIPTION OF PINS

1) Clock Oscillation

If a crystal oscillator element (16.9344MHz) is connected between the X1 and X0 pins, it will oscillate.



If clocks (5.6448MHz) are input to the DCK pin, the switching from the oscillating frequency of the crystal clock will be automatically performed and the clock will operate on the clock frequency of the DCK pin.

In case the DCK pin will not be used, leave it disconnected or fix it to "H". Leave the crystal oscillating element connected, even while the clock of the DCK pin will be operating.

2) SEL Pin Functions

The SEL pin will go "H" or "L" according to the Serial Voice Data Format of the data that is input to the DIN pin. If SEL is not connected, SEL will be set to "H" by an internal pull-up resistor. The only pins that will be affected by the SEL pin are the DIN, SDC, and BCI pins. Other pins will give no appearance of changing.

- When SEL = "H"
  Figs. 5 and 6-1 show the case where the SEL pin is "H".
  The input data of the DIN pin is input at the rising edge of BCI, the DIN pin will assume a negative logic state, and the DO pin will assume a positive logic state.
- When SEL = "L"
  Figs. 5 and 6-2 show the case where the SEL pin is "L".
  The input data of the DIN pin is input at the falling edge of BCI, and both the DIN and DO pins will assume a positive logic state.
  WCI will change at the rise of BCI.
  The output timing of SDC is constant irrespective of "H" or "L" of SEL. But its polarity will be inverted.

3) Data Input Pins: BCI, DIN, and WCI

The operating clock for the data output of the DO, BCO, DDO, and WCO pins is different from that of data input of the BCI, DIN, and WCI pins.

The BCI clock can be freely set if WCI and WCO are properly synchronized and 16 bits of L/R channel data is available.

4) VCO-Related Pins

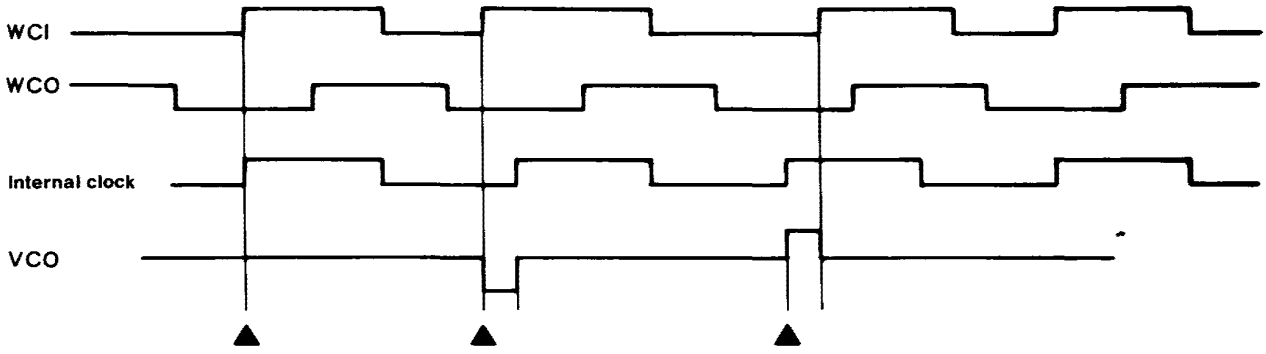


Fig. 1

In case of 50% duty, the phase difference between WCO and the internal clock is about 180° off when SEL is "H", or about 90° off when SEL is "L".
The VCO oscillating frequency will change so that a phase comparison of WCI and ▲ will produce equivalent phases. The oscillating frequency will rise when the WCI phase is delayed, and will fall when the WCI phase is advanced. When their phases are equal, the VCO oscillating frequency of the øB pin will become 8.6436MHz.
Be sure not to connect the ADJ pin (it is not particularly required for adjustment).

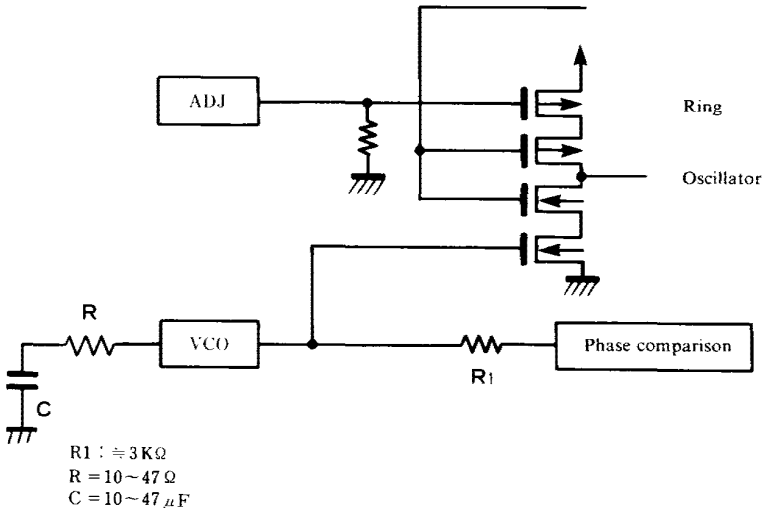


Fig. 2

■ TIMING CHARTS

(1) Output

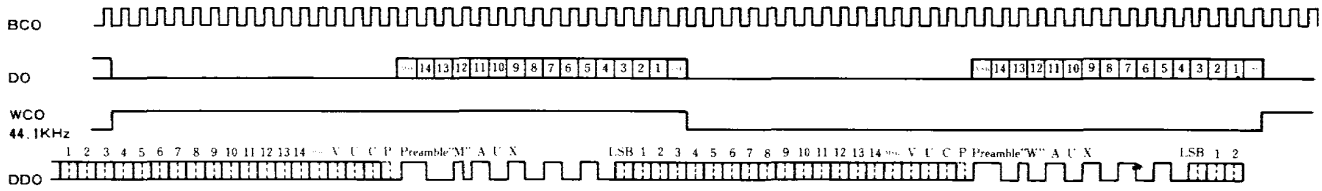
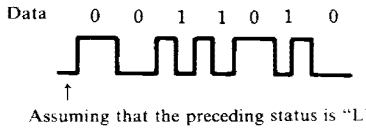


Fig. 3

NOTE 1: DDO is the bi-phase output. Thus, if the data of one data bit is "0", the DDO status will not change; if it is "1", its status will change. This situation is represented in Fig. 3 by a broken line. The solid line indicates the points where the status will always change.



NOTE 2: Preamble "M" indicates that the data is for the L channel, whereas Preamble "W" indicates it is for the R channel. "M" and "W" will appear alternately; once every 192 times, however, "B" will appear instead of "M" to indicate the beginning of a block.

NOTE 3: The "V" bit is called the Validity flag, and reflects the value input from the VFL pin.

NOTE 4: The "U" bit is called User data. Among the Subcode data "P" to "W" which is input from the SUB pin, only "P" is compulsorily set to "1" so that serial output of "1, Q, R, S, T, U, V, and W is performed (see Fig. 4).

	1	2	3	4	5	6	7	8	9	10	11	12
13	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0
37	1	Q_1	R_1	S_1	T_1	U_1	V_1	W_1	0	0	0	0
49	1	Q_2	R_2	S_2	T_2	U_2	V_2	W_2	0	0	0	0
—												
—												
—												
1165	1	Q_{96}	R_{96}	S_{96}	T_{96}	U_{96}	V_{96}	W_{96}	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0
37	1	Q_1	R_1	S_1	T_1	U_1	V_1	W_1	0	0	0	0

Sub code sync word

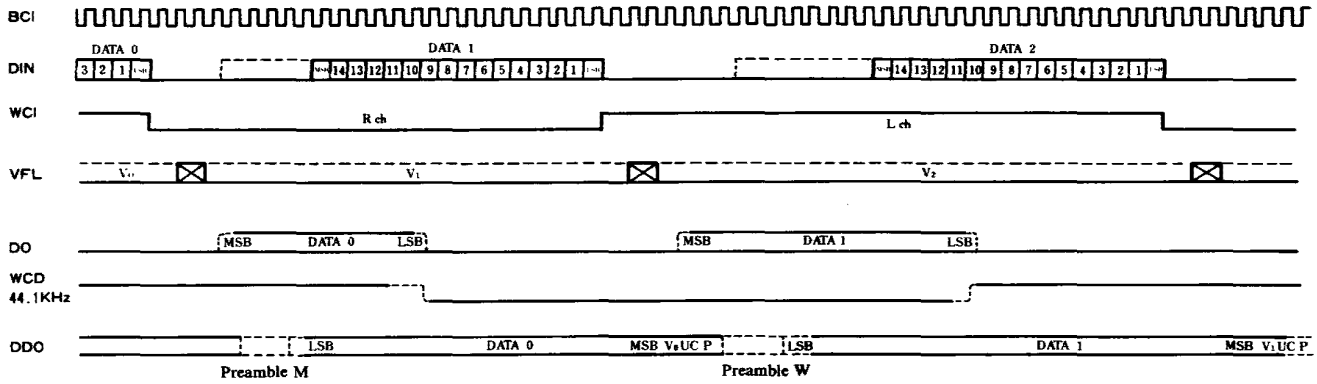
Fig. 4

NOTE 5: The "C" bit is called Channel Status and comprises 192 bits. Only when the Control bit of the Channel Status tests positive for a CRC check, the four Control bits ("Q" bits) within the Subcode will be copied. (From Preamble "B", sequentially from the 0th to the 3rd) the 8th "C" bit will be compulsorily set to "1" to indicate that the Category Code is CD. All other bits will be set to "0".

NOTE 6: The "P" bit is the Parity bit and employs even parity. The "P" bit will thus change so that the quantity of "1's" in the data will total an even number.

(2) Input

*** When SEL = "H"**



*** When SEL = "L"**

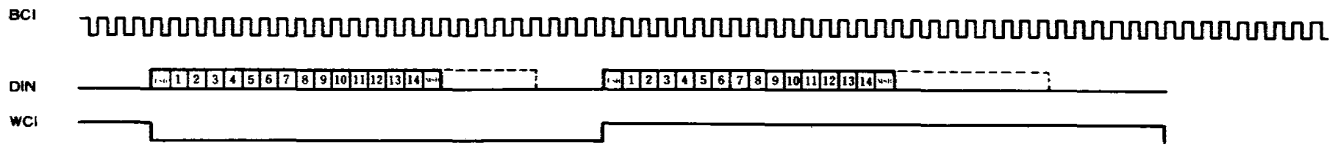


Fig. 5

NOTE 1: The above timing charts are standard examples. The broken line within the figure indicate the sections in which the changing point of the data cannot be clearly shown. BCI, DIN, WCI, and VFL operate on a different clock than DO, WCO, DDO, and BCO.

NOTE 2: Within the broken-line section, if the VFL pin is set "H" for an interval longer than one BCI1 clock, the Validity flag of DDO will become "H".

* When SEL = "H"

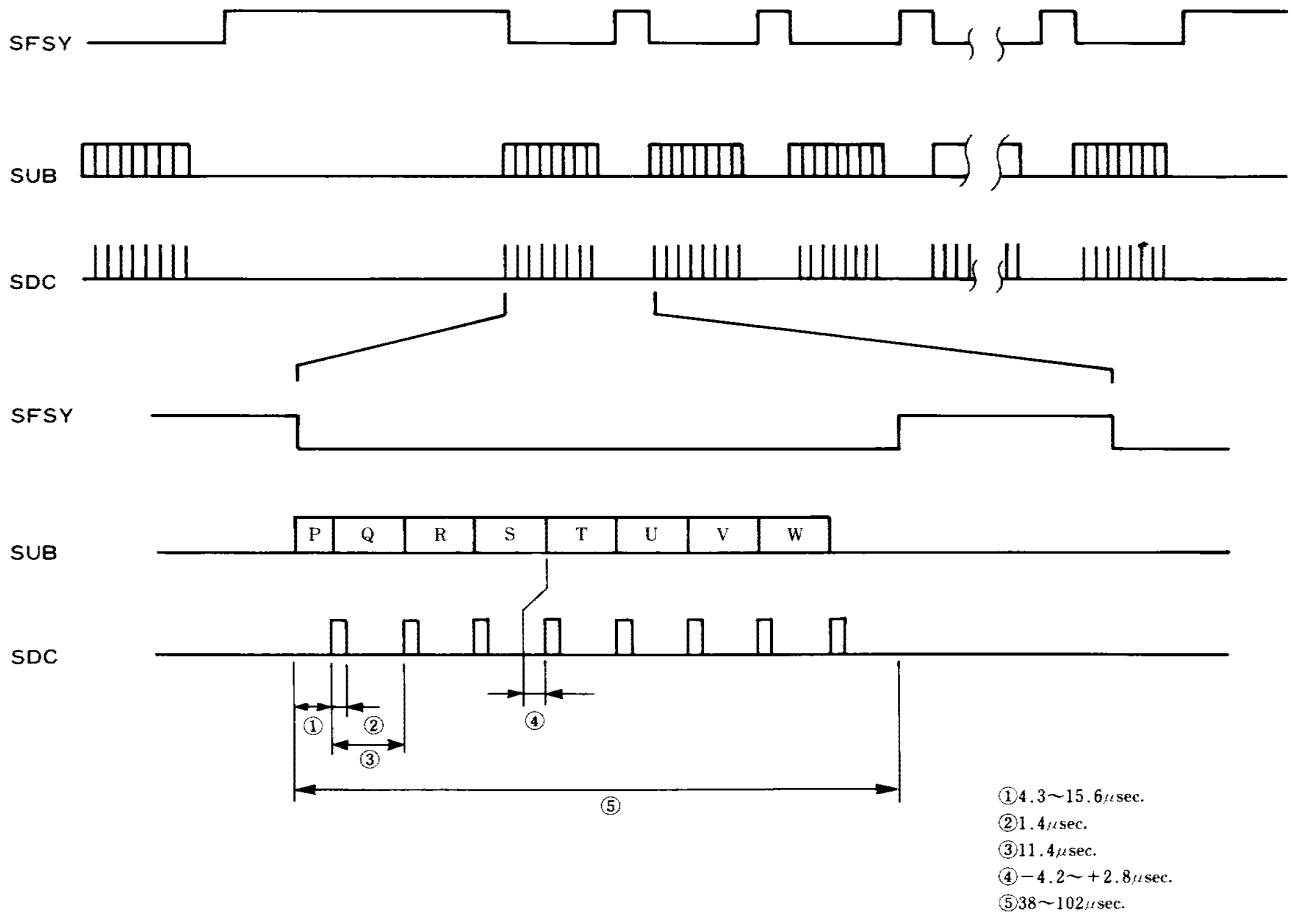
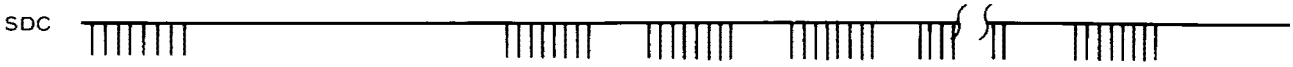


Fig. 6-1

* When SEL = "L"



Inversion of polarity only

Fig. 6-2

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Rating	Units
Supply voltage	V_{DD}—V_{SS}	−0.3 ~ +7.0	V
Input voltage	V_I	V_{SS} − 0.3 ~ V_{DD} + 0.5	V
Operating temperature	T_{OP}	−20 ~ +75	°C
Storage temperature	Tstg	−50 ~ +125	°C

2. Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
Supply voltage	V_{DD}—V_{SS}	4.5	5.00	5.5	V

3. Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating current	I_{DD}	V_{DD} = 5V fc = 16.9344MHz		10	18	mA
High-level output voltage	V_{OH}	I_{OH} = 0.4mA	4.0			V
Low-level output voltage	V_{OL}	I_{OL} = 2mA			0.4	V
High-level input voltage	V_{IH}	X_I pin excluded X_I pin	2.0 3.0			V
Low-level input voltage	V_{IL}				0.8	V
Input leakage current	I_{LK}	V_I = 5V			10	μA

NOTE: The analog VCO pin and the ADJ pin are excluded.

The specifications of this product are subject to improvement changes without prior notice.

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