PARADISE™
A WESTERN DIGITAL COMPANY

Features

- 100% IBM* CGA and MDA compatibility
- 720 x 348 pixel Hercules* compatibility
- AT&T* Model 6300 compatibility
- Plantronics* Colorplus compatibility
- Functionally compatible with 6845 CRTC
- Bus interface and decoding logic included
- Flicker-free operation in all video modes
- Composite Video and Composite Sync outputs
- Support for color simulation on monochrome monitors using Paradise Color Simulation chip (PSC)
- Internal multiplexer to select three video clock sources
- Printer port enable logic included with three selectable I/O address ranges
- Configuration Registers Auto-Load 16 parameters upon power-up or reset
- Supports up to four 256-character fonts with external character generator ROM
- Logic to support light pen included
- Available in 100-pin Shenko plastic flat package
- Minimum circuit board space requirements

Description

The Paradise PVC4 is a 2 micron, 6700 gate CMOS LSI device that implements virtually a "video card on a chip." With the addition of only RAM, a ROM character generator, an oscillator and two buffer devices, the PVC4 provides the functionality of the CGA, MDA, Hercules Graphics Card, Plantronics Colorplus Mode and AT&T video adapters.

* IBM is a registered trademark of International Business Machines Corporation.
* Hercules Graphics is a registered trademark of Hercules Computer Technology.
* AT&T is a registered trademark of American Telephone and Telegraph Corporation.
* Plantronics and ColorPlus are registered trademarks of Plantronics Inc.

Paradise Video Controller
PVC4

ORDER INFORMATION:

PACKAGE TYPE	WESTERN DIGITAL PART NO.
100 PIN SHENKO PFP	PVC4ANK00

Description of Operation

The PVC4 includes several features to maximize flexibility and minimize the required external hardware. This flexibility is implemented with two internal 8-bit registers which sense and retain configuration information.

At power-up, or after any hardware reset to the PVC4, the 8 video data and 8 video address lines are tested by the PVC4 to determine whether pull-up or pull-down resistors are connected. This selection allows the PVC4 to automatically configure itself according to the resistor connection.

The 8 address lines are sensed and stored in the Paradise Register and the 8 data lines are sensed and stored in the Configuration Register.

The Paradise Register is available as a write-only I/O register at address 3XB, after performing an unlocking operation. This unlocking operation consists of reading I/O port 3X8 twice in succession and then doing a write with the Paradise Register data to port 3XB. (NOTE: "X" = B (hex) in monochrome MDA modes, and D (hex) in color CGA modes.)

The Configuration Register can be written at address 3XA after it is unlocked. Unlocking the Configuration Register consists of reading I/O port 3X8 twice in succession and then doing a write with the Configuration Register data to port 3XA.

Configuration Selection

The primary configuration selection determined by the resistor programming is between the standard PC video adapters (including MDA, Hercules and CGA) and AT&T modes of operation. The AT&T configuration allows 400 lines to be displayed as either unique lines (M24 mode) or as double scanned CGA compatible 400 line display. When AT&T mode is selected, the CRTC timing is automatically set to conform to the AT&T display timing requirements.

Another configuration selection is the number of RAM banks used by the PVC4. Either one bank of 120 ns RAM, or two banks of 120 ns RAM are possible, depending on the memory bandwidth requirements. One bank of 120 ns RAM will support pixel clock rates up to 16.7 MHz, while two banks of 120 ns RAM will allow a 25 MHz pixel clock.

The operation of the Configuration and Paradise registers is detailed on the following pages.

Unlocking Locked Registers

To write to a locked register, the CPU must read the register at 3X8 twice, then write to the target register.

Note that these three I/O operations must be consecutive. Any intervening I/O access will cause the target register to remain locked.

To prevent the interrupt code from interfering with the unlocking operation, interrupts must be disabled for the duration of the unlocking sequence. For example:

```
                            ;Save dx, al first
mov     dx,03X8             ;Unlock address
cli                         ;Disable interrupts
in      al,dx               ;Read once
in      al,dx               ;Read again
mov     dx,<target reg>     ;Register address
mov     al,<reg-val>        ;Register value
out     dx,al               ;Output to unlocked register
sti                         ;Enable interrupts
```

Pixel Clock Selection

The PVC4 includes three input pins and an internal three-way multiplexer to allow for a choice of pixel clocks. The control of the clock select multiplexer is implemented with a combination of hardware and software, allowing for maximum flexibility.

Composite Video Support

Two output signals from the PVC4 are used to provide support for composite input monitors. Use of these two signals, along with a minimum of external circuitry, will allow driving NTSC-compatible RS-170 compatible composite monitors (or standard television, when used with an external RF modulator) in CGA 200 line modes.

The first signal, CSYNCN (Composite SYNC, active-LOW), includes both horizontal and vertical sync information mixed together via an internal EXCLUSIVE-OR gate. The result is a TTL-level signal, suitable for driving an external analog composite signal generator.

Using the XOR function for generating CSYNCN ensures that horizontal sync remains active even during the vertical retrace time. Although many monitors do not require this "serration" operation, it is specified in the NTSC standard.

The second composite support signal, CMPVD (CoMPosite ViDeo), contains the color pixel information needed for the display. The CMPVD signal also includes the video Color Burst signal specified by the NTSC. The purpose of the Color Burst (6 cycles of 3.5795 MHz) is to allow an analog monitor to correctly decode the color phase information for each of the 6 colors possible (using RED, GREEN and BLUE signals).

A third composite signal, CINTEN (Composite INTENsity), can be made available on pin 59 of the PVC4 (MONO signal pin), by setting the Configuration Register bit 3 high (1).

A functional diagram of PVC4 is shown on the following page.

VDD (+5 VDC)
14 41 87 89

HSYNC
VSYNC
MONO
IT
RD
GR
BL

CRT MONITOR

CMPVD
CSYNCN

VIDEO COMBINER

COMPOSITE MONITOR

RESET → RESET

CLOCK 0
CLOCK 1
CLOCK 2

CLK
CLOCK SELECT

LPNSTN
LPNSWN

SYSTEM CONTROL BUS
AEN
MEMRDN
MEMWRN
IORDN
IOWRN

SA (19)
SA (18)
SA (17)
SA (16)
SA (15)
SA (14)
SYSTEM ADDRESS BUS
SA (13)
SA (12)
SA (11)
SA (10)
SA (9)
SA (8)
SA (7)
SA (6)
SA (5)
SA (4)
SA (3)
SA (2)
SA (1)
SA (0)

VIDEO CONTROL

SYNC
VIDEO
COMPOSITE VIDEO/SYNC
CHAR DATA
FONT SEL
VID DATA

CD (7)
CD (6)
CD (5)
CD (4)
CD (3)
CD (2)
CD (1)
CD (0)

TIMING

CRT CONTROL

COLUMN ADDR
ROW ADDR
VID ADDR

CA (13)
CA (7)
CA (6)
CA (5)
CA (4)
CA (3)
CA (2)
CA (1)
CA (0)
RA (3)
RA (2)
RA (1)
RA (0)

CHAR ADDR

CHAR GEN EPROM

CHAR DATA

SYSTEM BUS INTERFACE

SYS DATA & CTL

DECODED PRINTER PORT ENB

TIMING

MD (7)
MD (6)
MD (5)
MD (4)
MD (3)
MD (2)
MD (1)
MD (0)

VIDEO DATA

SEQUENCER

RAM CTLS
READY

MA (7)
MA (6)
MA (5)
MA (4)
MA (3)
MA (2)
MA (1)
MA (0)

DRAM

VIDEO ADDR

DRAM

RAS10N
CASON
CAS1N
WE01N
SPP1N

PPC CONTROLLER (OUTPUT PORT)

ENB

IORDN, IOWRN (D0–D7)

LS245
SD (0)—A1 B1—D (7)
SD (1)—A2 B2—D (6)
SD (2)—A3 B3—D (5)
SYSTEM DATA BUS SD (3)—A4 B4—D (4)
SD (4)—A5 B5—D (3)
SD (5)—A6 B6—D (2)
SD (6)—A7 B7—D (1)
SD (7)—A8 B8—D (0)
EN AB

CENTRONICS PRINTER PORT

DIR
READY

CENTRONICS PRINTER

15 40 66 90
VSS GROUND

PVC4 FUNCTIONAL DIAGRAM

6

PVC4

Pin Assignments for 100-Pin Shenko Flat Pack

NAME	PIN#	DIR	LEVEL	DRIVE	DESCRIPTION
SPP1N	1	out	LOW	2 ma	Parallel Port ENable
CLOCK2	2	in			Video Clock Input (24.000 MHz)
CLOCK1	3	in			Video Clock Input (16.257 MHz)
CLOCK0	4	in			Video Clock Input (14.318 MHz)
A0	5	in			System Address Bus
A1	6	in			
A2	7	in			
A3	8	in			
A4	9	in			
A5	10	in			
A6	11	in			
A7	26	in			
A8	27	in			
A9	28	in			
A10	29	in			
A11	30	in			
A12	31	in			
A13	32	in			
A14	33	in			
A15	39	in			
A16	37	in			
A17	38	in			
A18	49	in			
A19	50	in			
MA0	18	out		4 ma	Video Memory Address Bus
MA1	19	out			
MA2	20	out			
MA3	21	out			
MA4	22	out			
MA5	23	out			
MA6	24	out			
MA7	25	out			
D0	34	in/out			Buffered Data Bus
D1	35	in/out			
D2	36	in/out			
D3	42	in/out			
D4	43	in/out			
D5	44	in/out			
D6	45	in/out			
D7	46	in/out			
DIR	47	out	LOW⇒Bus	4 ma	Bus Buffer Direction Control

Pin Assignments for 100-Pin Shenko Flat Pack cont'd

NAME	PIN#	DIR	LEVEL	DRIVE	DESCRIPTION
READY	48	out	HIGH	12 ma	Memory Access Complete
RESET	52	in	HIGH		System Reset
AEN	51	in	LOW		System Address Enable
MEMRDN	53	in	LOW		Memory Read
MEMWRN	54	in	LOW		Memory Write
IORDN	55	in	LOW		I/O Read
IOWRN	56	in	LOW		I/O Write
CMPVD	57	out	HIGH	4 ma	Composite Video
CSYNCN	58	out	LOW		Composite Sync
MONO	59	out			Monochrome Video
IT	70	out			Monochrome Video Intensity
BL	60	out			Blue Output
GR	61	out			Green Output
RD	62	out			Red Output
HSYNC	69	out			Horizontal Sync
VSYNC	68	out		4 ma	Vertical Sync
LPNSWN	64	in	LOW		Light Pen SWitch
LPNSTN	63	in	LOW		Light Pen STrobe
CD0	65	in			Character Generator Data
CD1	71	in			
CD2	72	in			
CD3	73	in			
CD4	74	in			
CD5	75	in			
CD6	76	in			
CD7	77	in			
RA0	78	out		2 ma	Character Gen. Row Address
RA1	79	out			
RA2	80	out			
RA3	81	out			
CA0	82	out			Character Gen. Character Address
CA1	83	out			
CA2	84	out			
CA3	85	out			
CA4	86	out			
CA5	87	out			
CA6	88	out			
CA7	91	out			
CA13	12	out		2 ma	

Pin Assignments for 100-Pin Shenko Flat Pack cont'd

NAME	PIN#	DIR	LEVEL	DRIVE	DESCRIPTION
MD0	92	in/out		4 ma	Video Memory Data
MD1	93	in/out			
MD2	94	in/out			
MD3	95	in/out			
MD4	96	in/out			
MD5	97	in/out			
MD6	98	in/out			
MD7	99	in/out			
CAS0N	16	out	LOW		Column Address Strobe - RAM Bank 0
CAS1N	17	out	LOW		Column Address Strobe - RAM Bank 1
WE01N	13	out	LOW	4 ma	Write Enable: RAM Banks 0 and 1
RAS01N	100	out	LOW	8 ma	Row Address Strobe Banks 0 and 1
VDD	14, 41, 67, 89				+5 VDC
VSS	15, 40, 66, 90				0 VDC (Ground)

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias   0° C TO 70° C
Storage temperature   -40° C to 100° C
Voltage on all inputs and
outputs with respect to VSS   -0.5 to 7 Volts
Power dissipation   1.0 Watt

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

STANDARD TEST CONDITIONS

The characteristics below apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to VSS (0V Ground). Positive current flows into the referenced pin.

Operating temperature range   0° to 70° C
Power supply voltage VDD   4.75 to 5.25 Volts

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
VIL	Input Low Voltage	VSS	0.8	Volts	VDD = 5V
VIH	Input High Voltage	2.0	VDD	Volts	VDD = 5V
IIL	Input Low Current	-0.5	-20	uA	VIN = 0.0V
IIH	Input High Current	-----	20	uA	VIN = VCC
VOL	Output Low Voltage	-----	0.4	Volts	IOL = 4.0MA
VOH	Output HighVoltage	2.4	-----	Volts	IOL = 4.0MA
VOL	Output Low Voltage	-----	0.4	Volts	IOL = 2.0MA
VOH	Output High Voltage	2.4	-----	Volts	IOL = 2.0 MA
IOZ	High Z Leakage Current	-10.0	10.0	uA	OV<VOUT<VDD
IDD	Supply current	-----	60.0	mA	For VDD = +5V

AC CHARACTERISTICS

DYNAMIC RAM READ/WRITE TIMING DIAGRAMS

SYMBOL	PARAMETER	MODE	MIN	MAX	UNITS
1	Clock Period				
	(1 RAM Bank)		60	-----	ns
	(2 RAM Banks)		40	-----	ns
2	RAS Set Up Time		0	-----	ns
2a	Row Address Hold Time		0.5 T	-----	ns
3	CAS Set Up Time		0	-----	ns
3a	Column Address Hold Time		0.5 T	-----	ns
4	RAS Precharge		2.5 T	-----	ns
4a	RAS Low to CAS Low		1 T	2 T + 10ns	ns
5	CAS Low Pulse Duration		1.5 T - 10ns	-----	ns
6	CAS Precharge				
	(1 RAM Bank)		3.5 T	-----	ns
7	RAS Low To Memory Data Valid				
	(1 RAM Bank)		-----	2.5 T	ns
8	CAS Low To Memory Data Valid				
	(1 RAM Bank)		-----	1.5 T - 10ns	ns
9	RAS Low Pulse Duration				
	(1 RAM Bank)	(Color)	3 T	142 T	ns
		(MDA)	3 T	166 T	ns

NOTE: For all timing diagrams, T = 40ns in Olivetti* mode (High Speed), T = 60ns in CGA or Plantronics mode (Low Speed), and T = 70ns in MDA or Hercules mode (Low Speed).

* Olivetti is a registered trademark of Ing. C. Olivetti & C., S.p.A.
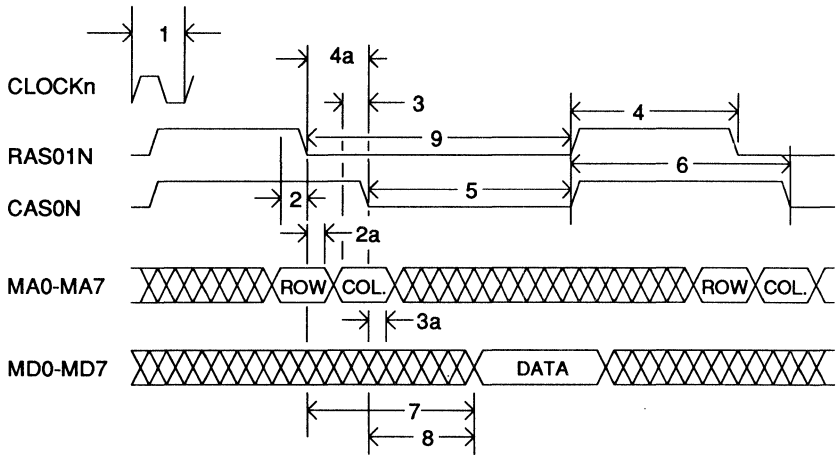
AC CHARACTERISTICS (Cont'd)

DYNAMIC RAM READ/WRITE AND REFRESH TIMING DIAGRAMS

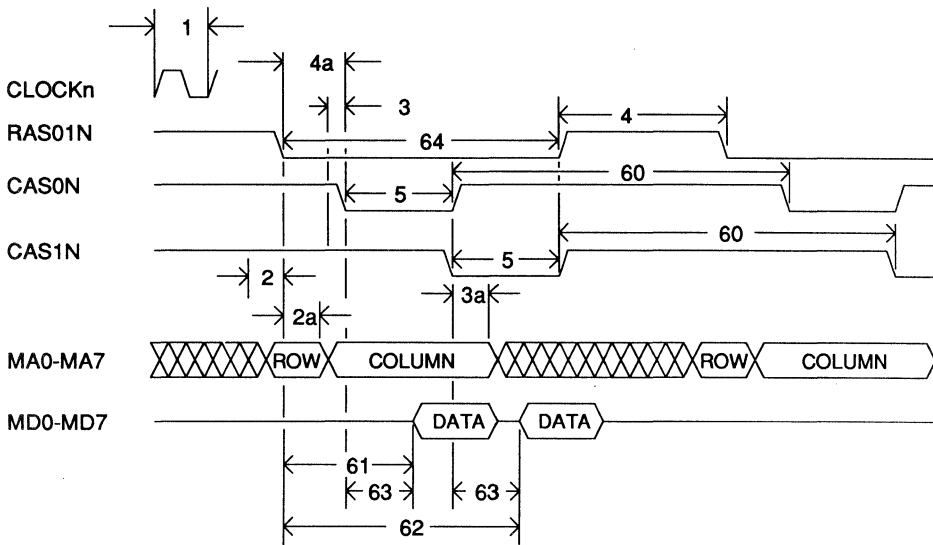| SYMBOL	PARAMETER	MODE	MIN	MAX	UNITS
10	Data Hold From CAS0N		T	-----	ns
11	Data Setup Before CAS0N		0	-----	ns
12	Write Enable Low Pulse Duration		3 T	-----	ns
60	CAS Precharge (2 RAM Banks)	(Olivetti)	7 T	-----	ns
		(Color Or MDA)	6 T	-----	ns
61	RAS Low To First Memory Data Valid (2 RAM Banks)	(Olivetti)	-----	4 T	ns
		(Color Or MDA)	-----	3 T	ns
62	RAS Low To Second Memory Data Valid (2 RAM Banks)	(Olivetti)	-----	6 T	ns
		(Color Or MDA)	-----	5 T	ns
63	CAS Low To Memory Data Valid (2 RAM Banks)		-----	2 T - 10ns	ns
64	RAS Low Pulse Duration (2 RAM Banks)	(Olivetti)	4 T	250 T	ns
		(Color)	4 T	166 T	ns
		(MDA)	4 T	142 T	ns
102	RAS Low (Refresh)		2.5 T	-----	ns
103	RAS Precharge (Refresh)	(Olivetti)	2.5 T	-----	ns
		(Color or MDA)	2 T	-----	ns

NOTE: For all timing diagrams, T = 40ns in Olivetti mode (High Speed), T = 60ns in CGA or Plantronics mode (Low Speed), and T = 70ns in MDA or Hercules mode (Low Speed).

DYNAMIC RAM 1 BANK READ CYCLE
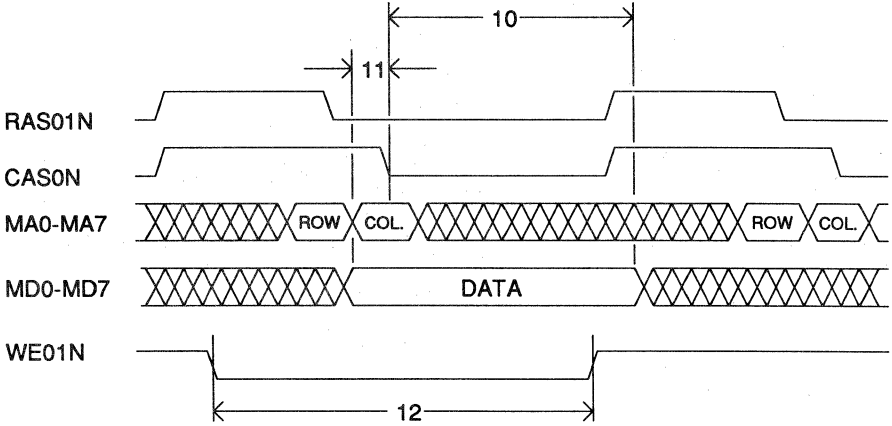

DYNAMIC RAM 2 BANK READ CYCLE
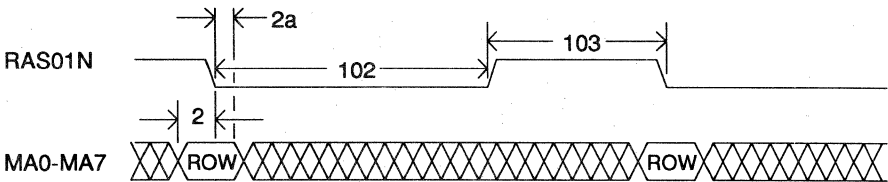
DYNAMIC RAM WRITE CYCLE

REFRESH CYCLE

AC CHARACTERISTICS (Cont'd.)

MEMORY READ/WRITE TIMING DIAGRAMS

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS
14	Memory Write Data Valid After Memory Write Low	-----	-----	4 T	ns
15	Memory Write Data Hold After Ready High	0	-----	-----	ns
16	Address Hold After Memory Write High	0	-----	-----	ns
17	READY Low (Memory Write Cycle)	-----	-----	2000	ns
18	Memory Write Low To READY Low	-----	-----	30	ns
19	Memory Write High to READY High Impedance	-----	-----	27	ns
20	Address Set Up To Memory Write Low	0	-----	-----	ns
21	Memory Read Data Set Up To READY High	0	-----	-----	ns
22	Memory Read Data Hold After Memory Read High	15	-----	-----	ns
23	Address Set Up To Memory Read Low	0	-----	-----	ns
24	Memory Read Low to DIR Control Low	-----	-----	40	ns
25	Memory Read Low To READY Low	-----	-----	30	ns
26	READY Low (Memory Read Cycle)	-----	-----	2000	ns
27	Memory Read High to DIR Control High	-----	-----	30	ns
28	Memory Read High to READY High Impedance	-----	-----	27	ns
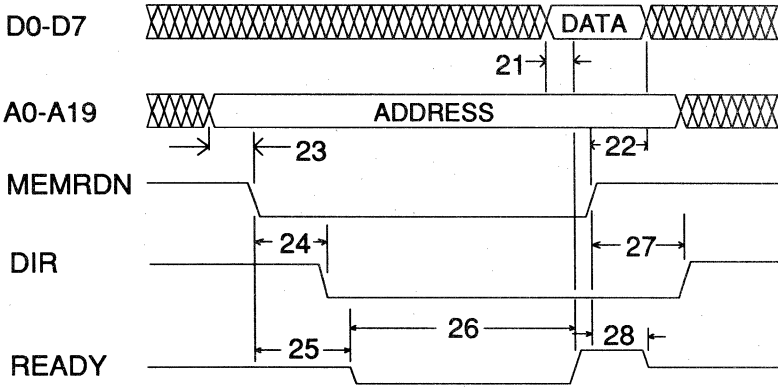
D0-D7 · · · · · DATA · · · · ·

21→ ←

A0-A19 · · · ADDRESS · · · ←22→

←23

MEMRDN

←24→ ←27→

DIR

←26→ 28 ←

←25→

READY

MEMORY READ BUS CYCLE

DO-D7 · · · · · DATA · · · · ·

←——14——→ → 15 ←

A0-A19 · · · ADDRESS · · ·

→|20|← ←16→

MEMWRN

DIR
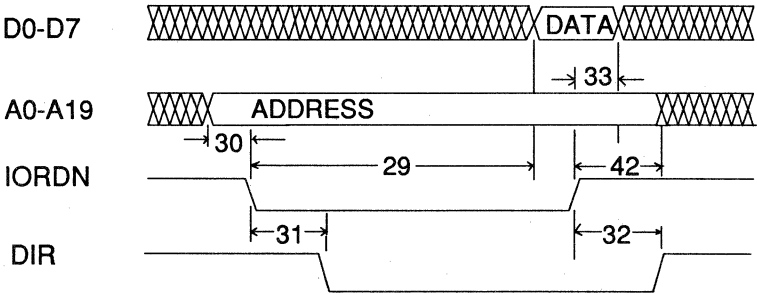
←17→ ←19→

←18→

READY
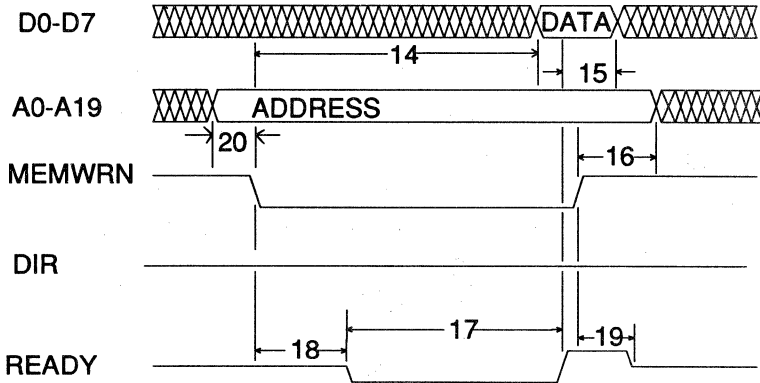
MEMORY WRITE BUS CYCLE

AC CHARACTERISTICS (Cont'd.)

I/O READ/WRITE AND PRINTER PORT ENABLE TIMING DIAGRAMS

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS
29	I/O Read Low To Data Valid	-----	-----	80	ns
30	Address Set Up To I/O Read Low	0	-----	-----	ns
31	I/O Read Low to DIR Control Low	-----	-----	55	ns
32	I/O Read High to DIR Control High	-----	-----	40	ns
33	Data Hold After I/O Read High	10	-----	-----	ns
42	Address Hold After I/O Read High	10	-----	-----	ns
34	Data Hold After I/O Write High	1 / 2 T	-----	-----	ns
35	Data Set Up To I/O Write High	T	-----	-----	ns
36	Address Hold After I/O Write High	30	-----	-----	ns
37	Address Set Up to I/O Write Low	30	-----	-----	ns
38	AEN Active to PPEN Low	-----	-----	50	ns
39	AEN Inactive to PPEN High	-----	-----	30	ns
40	Character ROM Read Period	8 T	-----	-----	ns
41	Character ROM Address Valid to Data Valid	-----	-----	200	ns

D0-D7

A0-A19

IORDN

DIR

I/O READ BUS CYCLE

D0-D7

A0-A19

IOWRN

DIR

I/O WRITE BUS CYCLE

A0-A19

AEN

PPEN
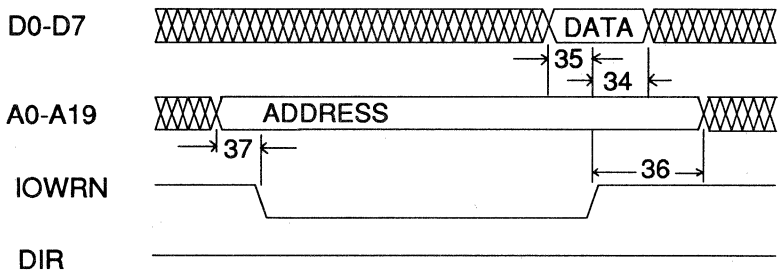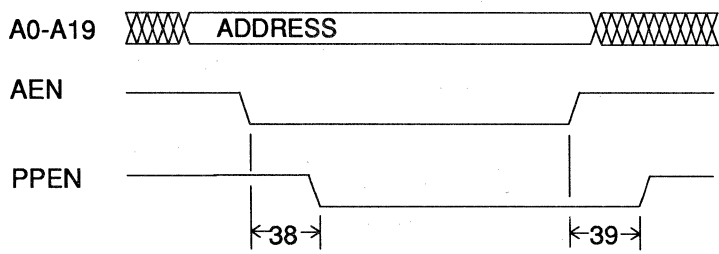
I/O PRINTER PORT ENABLE

18

RA/CAnn

$\leftarrow$ 40 $\rightarrow$

CHAR GEN ADDRn

CHAR GEN ADDRn+1

$\leftarrow$ 41 $\rightarrow$

CD0-CD7

CHAR GEN DATA

CHAR GEN DATA
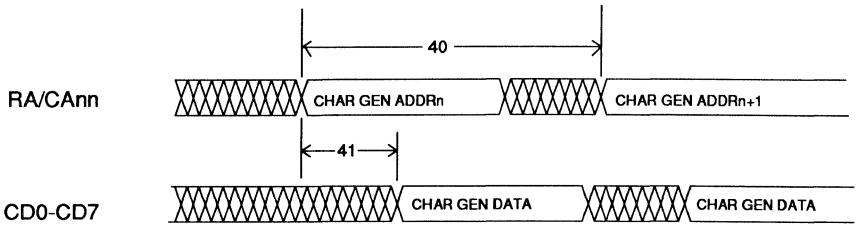
CHARACTER GENERATOR ROM READ TIMING

AC CHARACTERISTICS (Cont'd)

PAGE MODE READ TIMING DIAGRAMS

SYMBOL	PARAMETER	MODE	MIN	MAX	UNITS
70	RAS Set Up Time		0	-----	ns
71	CAS Set Up Time		0	-----	ns
72	RAS Precharge		2 . 5 T	-----	ns
73	CAS Low Pulse Duration		1 . 5 - 10ns	-----	ns
74	CAS Precharge (1 RAM Bank)		1 T	-----	ns
75	RAS Low To Memory Data Valid (1 RAM Bank)		-----	3 T - 10ns	ns
76	CAS Low To Memory Data Valid		-----	1 . 5 T - 10ns	ns
77	RAS Low Pulse Duration (1 RAM Bank)	(Olivetti)	3 T	250 T	ns
		(Color)	3 T	166 T	ns
		(MDA)	3 T	142 T	ns
78	CAS Precharge (2 RAM Banks)		2 T	-----	ns
79	RAS Low To Memory Data Valid (2 RAM Banks)	(Olivetti)	-----	4 T	ns
		(Color Or MDA)	-----	3 T	ns
80	RAS Low Pulse Duration (2 RAM Banks)	(Olivetti)	6 T	250 T	ns
		(Color)	5 T	166 T	ns
		(MDA)	5 T	142 T	ns

NOTE: For all timing diagrams, T = 40ns in Olivetti mode (High Speed), T = 60ns in CGA or Plantronics mode (Low Speed), and T = 70ns in MDA or Hercules mode (Low Speed).
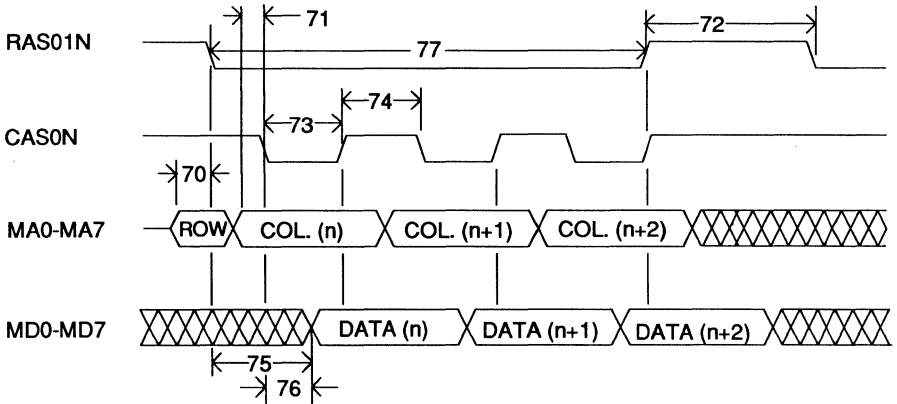
PAGE MODE 1 BANK READ CYCLE
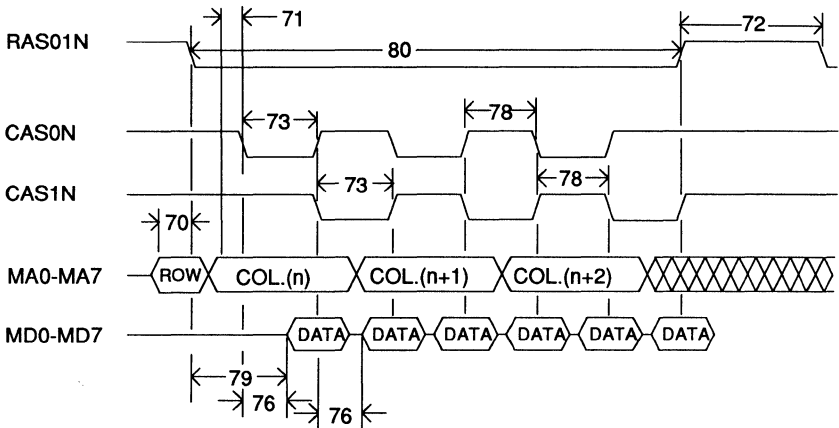
PAGE MODE 2 BANK READ CYCLE

SEQUENCE DIAGRAMS

RAS01N

CAS0N

VMA(7:0)   ROW   COL   ROW   COL   COL+1   COL+2   COL+3

VMD(7:0) - READ   DATA   D0   D1   D2   D3

VMD(7:0) - WRITE   DATA

CPU READ/WRITE   DISPLAY REFRESH PAGE MODE READ
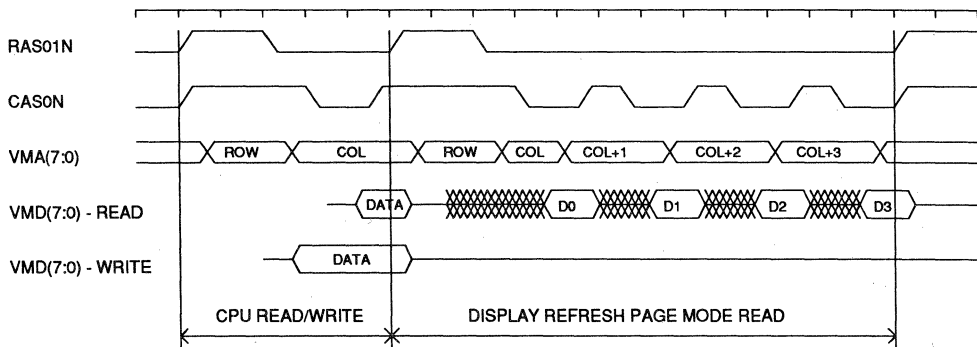
LOW SPEED, ONE RAM BANK MEMORY SEQUENCE
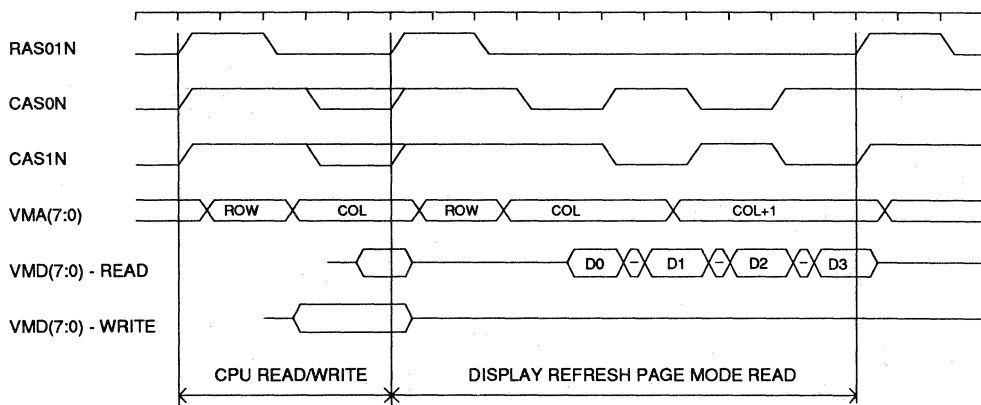
RAS01N

CAS0N

CAS1N

VMA(7:0)   ROW   COL   ROW   COL   COL+1

VMD(7:0) - READ   D0   D1   D2   D3

VMD(7:0) - WRITE

CPU READ/WRITE   DISPLAY REFRESH PAGE MODE READ

LOW SPEED, TWO RAM BANK MEMORY SEQUENCE

NOTE: During the CPU Read/Write sequence, either CAS0N or CAS1N will go low (active). Both CAS0N and CAS1N will never go low (active) at the same time.

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SEQUENCE DIAGRAMS (Cont'd.)

| RAS01N |
| CAS0N |
| CAS1N |
| VMA(7:0) | ROW | COL | ROW | COL | COL+1 |
| VMD(7:0) - READ | D0 | D1 | D2 | D3 |
| VMD(7:0) - WRITE |

CPU READ/WRITE   DISPLAY REFRESH PAGE MODE READ

HIGH SPEED, TWO RAM BANK MEMORY SEQUENCE

NOTE: During the CPU Read/Write sequence, either CAS0N or CAS1N will go low (active). Both CAS0N and CAS1N will never go low (active) at the same time.

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PVC4

PARADISE REGISTER

PARADISE REGISTER - WRITE-ONLY PORT = 3XB

7	6	5	4	3	2	1	0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

I/O Mapping
1=Monochrome I/O Mapping(3BB)
0=Color I/O Mapping(3DB)

Monitor Type (Olivetti Only)
1=Monochrome Olivetti Monitor Type
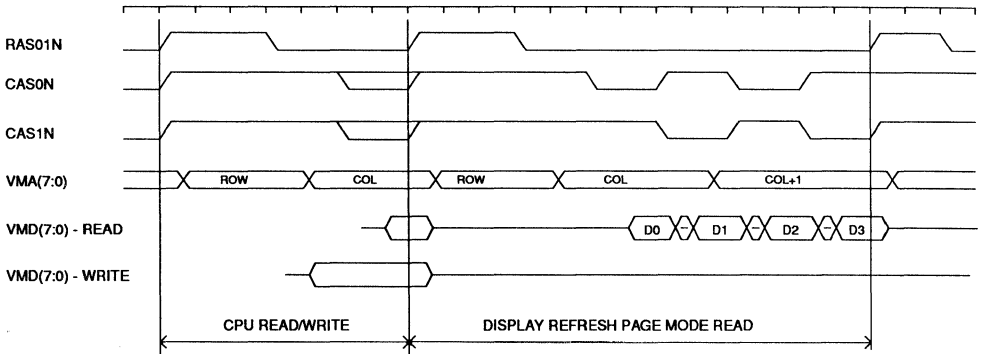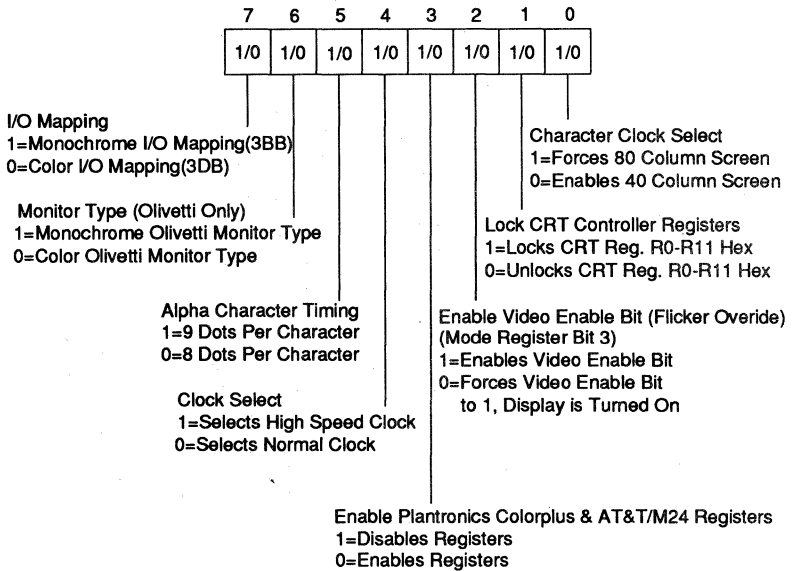0=Color Olivetti Monitor Type

Alpha Character Timing
1=9 Dots Per Character
0=8 Dots Per Character

Clock Select
1=Selects High Speed Clock
0=Selects Normal Clock

Character Clock Select
1=Forces 80 Column Screen
0=Enables 40 Column Screen

Lock CRT Controller Registers
1=Locks CRT Reg. R0-R11 Hex
0=Unlocks CRT Reg. R0-R11 Hex

Enable Video Enable Bit (Flicker Overide)
(Mode Register Bit 3)
1=Enables Video Enable Bit
0=Forces Video Enable Bit
   to 1, Display is Turned On

Enable Plantronics Colorplus & AT&T/M24 Registers
1=Disables Registers
0=Enables Registers

The Paradise Register is a write protected register located at I/O port address 3XB. The register is loaded upon power-up or reset with the pull-up (=1) or pull-down (=0) values either hard-wired or programed with switches on the PVC4's MA(0:7) DRAM address lines. This register is then write protected or locked out, but may be unlocked by performing two consecutive reads from location 3X8 followed by a write to location 3XB with the data value. After the write to 3XB the register will be relocked. This register occupies the same port as the Clear Light Pen Latch in CGA so any read or write to this port when locked resets the Light Pen Latch (3XB).

Bit 7   1 = Selects monochrome I/O mapping at location 3BB.
             0 = Selects color I/O mapping at location 3DB.

NOTE: For all registers, "X" = B (hex) in monochrome MDA modes, and D (hex) in color CGA modes.

PARADISE REGISTER CONT'D

Bit 6   1 = Selects M24 monochrome Olivetti monitor type as an output device.
               0 = Selects M24 color Olivetti monitor type.

Bit 5   1 = Selects 9 dot alpha character timing.
               0 = Selects 8 dot alpha character timing.

Bit 4   1 = Selects the high speed clock, which is at input pin CLOCK2 (24 MHz) for
                   AT&T / M24 mode. This clock is the source for the pixel clock and internal state
                   machine of the video controller.
               0 = Selects the normal clock, which is CLOCK1 (16 MHz) for MDA mode; or
                   or CLOCK0 (14 MHz) for CGA or Plantronics mode. An 80 Column screen is
                   produced.

Bit 3   1 = Disables the Plantronics Colorplus Register and the AT&T / M24 Register.
               0 = Enables the Plantronics Colorplus Register and the AT&T / M24 Register.

Bit 2   Flicker Overide
               1 = Enables the video enable bit (bit 3 of the Mode Register).
               0 = Forces the video enable bit to "1" (Mode Register(3)=1). The display is turned on.

Bit 1   1 = Write protects the CRT Controller Registers R0 thru R12 Hex, which are located
                   at address 3X5.
               0 = Allows the CRT Controller Registers R0 thru R12 Hex to be written to at address
                   3X5 by using 3X4 as the index pointer.

Bit 0   1 = This produces an 80 column screen.
               0 = Allows bit 0 of the mode register (3 x 8 hex) to select 40 column mode
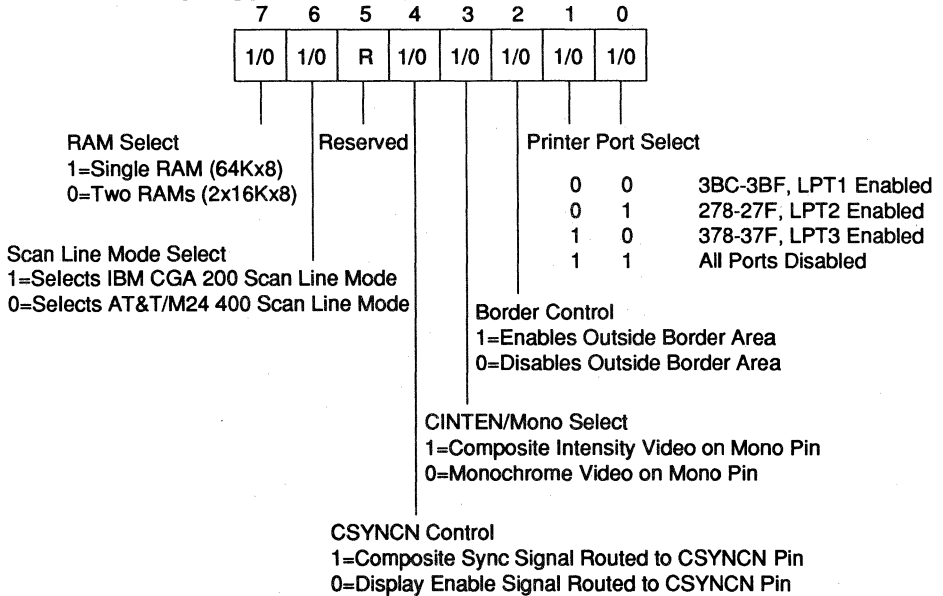   (NOTE: The clock input pin selection is not affected by this bit.)

NOTES: 1. For further information on PVC4 clock selection, refer to the Clock Selection Table on page 32.

CONFIGURATION REGISTER

CONFIGURATION REGISTER - WRITE PORT = 3XA

7	6	5	4	3	2	1	0
1/0	1/0	R	1/0	1/0	1/0	1/0	1/0

RAM Select
1=Single RAM (64Kx8)
0=Two RAMs (2x16Kx8)

Reserved

Printer Port Select

0	0	3BC-3BF, LPT1 Enabled
0	1	278-27F, LPT2 Enabled
1	0	378-37F, LPT3 Enabled
1	1	All Ports Disabled

Scan Line Mode Select
1=Selects IBM CGA 200 Scan Line Mode
0=Selects AT&T/M24 400 Scan Line Mode

Border Control
1=Enables Outside Border Area
0=Disables Outside Border Area

CINTEN/Mono Select
1=Composite Intensity Video on Mono Pin
0=Monochrome Video on Mono Pin

CSYNCN Control
1=Composite Sync Signal Routed to CSYNCN Pin
0=Display Enable Signal Routed to CSYNCN Pin

The Configuration Register is a write protected register located at I/O port address 3XA. This register is loaded at power-up or reset with the pull-up (=1) or pull-down (=0) values on the MD(0:7) data lines of the PVC4 chip. The register is then write protected or locked out, but may be unlocked by performing two consecutive reads from location 3X8 followed by a write to location 3XA with the data value. After the write to 3XA, the register will be relocked.

Bit 7   1 = Selects one memory bank (64K x 8) for the video display buffer.
               0 = Selects two memory banks (2 x 16K x 8) for the video display buffer.

Bit 6   1 = Selects IBM CGA 200 scan line mode.
               0 = Selects M24 (AT&T and Olivetti) 400 scan line mode.

CONFIGURATION REGISTER CONT'D

Bit 5   Not used.

Bit 4   1 = The Composite Sync signal (HSYNC + VSYNC) is routed to the
PVC4 output pin CSYNCN. (NOTE: "+" = Logical OR)
0 = The Display Enable signal DE (which is functionally equivalent to
Motorola's 6845 CRT Controller output signal DE) is routed to PVC4
output pin CSYNCN. Display Enable DE is high when the controller is

Bit 3   1 = Selects Composite Intensity Video from PVC4 mono pin.
(Y = I + R + G + B). (NOTE: "+" = Logical OR)
0 = Selects Monochrome Video from PVC4 mono pin.

Bit 2   1 = Enables the border area outside of the normal character display area.
0 = Disables outside border area.

Bit 1	Bit 0	
0	0	Port address decode = 3BC-3BF, LPT1 enabled
0	1	Port address decode = 278-27F, LPT2 enabled
1	0	Port address decode = 378-37F, LPT3 enabled
1	1	Port address decode = Disables all ports

These two bits select the range of the line printer port addresses that are
decoded by the PVC4 chip, in addition to a setting that disables this
decoding function. When enabled, and the range of addresses are decoded,
the PVC4 control SPPIN is driven low. This provides a chip select
function that enables an attached Paradise Parallel Printer Port Chip
(PPC1/ PPC2) connected to the System Address Bus Lines (SA0-SA1)
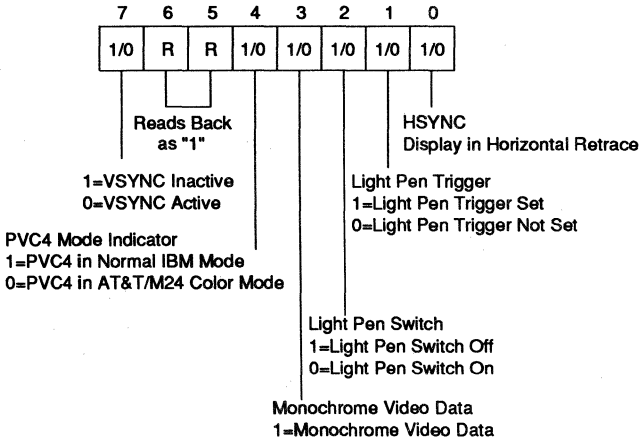and the System Data Bus Lines D(0:7).

NOTES: 1. Port 3XA is also used for status readback. See the Status Register description.
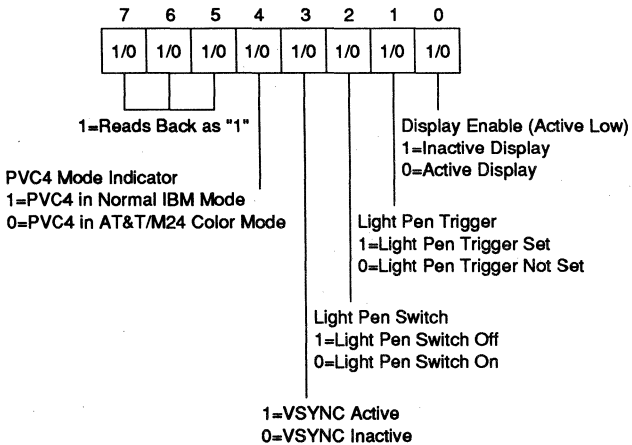2. For further information on PVC4 clock selection, refer to the Clock Selection Table on page 32.

STATUS REGISTER

STATUS REGISTER MONOCHROME OPERATION -READ-ONLY PORT = 3BA

```
    7    6    5    4    3    2    1    0
  +----+----+----+----+----+----+----+----+
  |1/0 | R  | R  |1/0 |1/0 |1/0 |1/0 |1/0 |
  +----+----+----+----+----+----+----+----+
```

Reads Back
as "1"

HSYNC
Display in Horizontal Retrace

1=VSYNC Inactive
0=VSYNC Active

Light Pen Trigger
1=Light Pen Trigger Set
0=Light Pen Trigger Not Set

PVC4 Mode Indicator
1=PVC4 in Normal IBM Mode
0=PVC4 in AT&T/M24 Color Mode

Light Pen Switch
1=Light Pen Switch Off
0=Light Pen Switch On

Monochrome Video Data
1=Monochrome Video Data

STATUS REGISTER COLOR OPERATION - READ-ONLY PORT = 3DA

```
    7    6    5    4    3    2    1    0
  +----+----+----+----+----+----+----+----+
  |1/0 |1/0 |1/0 |1/0 |1/0 |1/0 |1/0 |1/0 |
  +----+----+----+----+----+----+----+----+
```

1=Reads Back as "1"

Display Enable (Active Low)
1=Inactive Display
0=Active Display

PVC4 Mode Indicator
1=PVC4 in Normal IBM Mode
0=PVC4 in AT&T/M24 Color Mode

Light Pen Trigger
1=Light Pen Trigger Set
0=Light Pen Trigger Not Set

Light Pen Switch
1=Light Pen Switch Off
0=Light Pen Switch On

1=VSYNC Active
0=VSYNC Inactive

STATUS REGISTER CONT'D

The Status Register is a read only register located at I/O port address 3XA. (See the Configuration Register description).
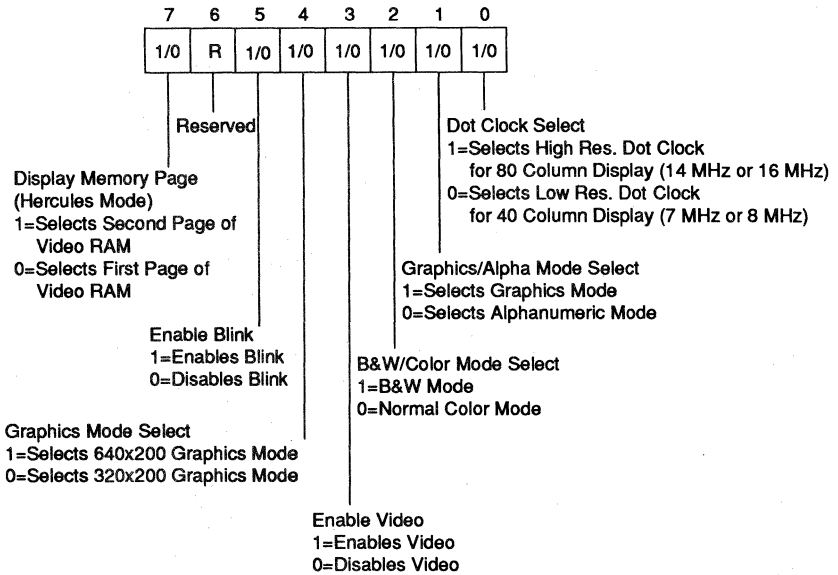
Bit 7   **Monochrome modes**
1 = Indicates vertical retrace is inactive.
0 = Indicates the raster is in vertical retrace mode.
Color modes
Always Reads back as "1".

Bit 6, Bit 5   Always Read back as "1".

Bit 4   1 = Indicates PVC4 is in normal IBM mode.
0 = Indicates PVC4 is in AT & T / M24 color mode.

Bit 3   **Monochrome modes**
1 = Monochrome video data.
Color modes
1 = Indicates the raster is in vertical retrace mode.
0 = Indicates vertical retrace is inactive.

Bit 2   1 = Indicates the Light Pen Switch is off (open).
0 = Indicates the Light Pen Switch is on (closed).

Bit 1   1 = Indicates the Light Pen Trigger is set. This trigger is reset at power-up
and may be cleared by any read or write to location 3XB.
0 = Indicates the Light Pen Trigger is not set.

Bit 0   **Monochrome modes**
Display is always in horizontal retrace.
Color modes
1 = Indicates the screen border or blanking is active; display enable is
inactive
0 = Indicates display enable is active.

MODE REGISTER

MODE REGISTER - READ/WRITE PORT = 3X8

7	6	5	4	3	2	1	0
1/0	R	1/0	1/0	1/0	1/0	1/0	1/0

Reserved

Display Memory Page
(Hercules Mode)
1=Selects Second Page of
  Video RAM
0=Selects First Page of
  Video RAM

Enable Blink
1=Enables Blink
0=Disables Blink

Graphics Mode Select
1=Selects 640x200 Graphics Mode
0=Selects 320x200 Graphics Mode

Dot Clock Select
1=Selects High Res. Dot Clock
  for 80 Column Display (14 MHz or 16 MHz)
0=Selects Low Res. Dot Clock
  for 40 Column Display (7 MHz or 8 MHz)

Graphics/Alpha Mode Select
1=Selects Graphics Mode
0=Selects Alphanumeric Mode

B&W/Color Mode Select
1=B&W Mode
0=Normal Color Mode

Enable Video
1=Enables Video
0=Disables Video

The Mode Register is a read/write register located at I/O port address 3X8. It is cleared at reset. This register is used to unlock any locked register by reading from port 3X8 twice in succession. (Note: any unlocked register is relocked after it has been written to, or if any other PVC4 video port is accessed).

Bit 7   Display Memory Page (Hercules mode)
               1 = Selects the second page of video RAM mapped to address B8000.
               0 = Selects the first page of video RAM mapped to address B0000.

Bit 6   Not used.

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MODE REGISTER CONT'D

Bit 5   1 = Enables the blinking function. The character background intensity will change to the blinking attribute function for alphanumeric modes. When the high order attribute is not selected, 16 background colors or intensified colors are available.
0 = Disables the blinking function.

Bit 4   1 = Selects the high resolution 640 x 200 graphics mode. One of 16 colors, determined by the CGA Border Control Register at port 3D9H, can be selected on direct drive monitors in this mode.
0 = Selects 320 x 200 graphics mode (medium resolution).

Bit 3   1 = Enables the Video Signal. (The Video Signal is disabled when changing modes).
0 = Disables the Video Signal.

Bit 2   1 = Selects black-and-white mode from composite color mode.
0 = Selects normal color mode.

Bit 1   1 = Selects graphics mode.
0 = selects alphanumeric mode.

Bit 0   1 = Selects high resolution dot clock (14 or 16 MHz); 80 column mode.
0 = Selects low resolution dot clock (7 or 8 MHz); 40 column mode.

NOTES: 1. For further information on PVC4 clock selection, refer to the Clock Selection Table on page 32.

CLOCK SELECTION TABLE

PARADISE REGISTER BIT 4	MODE REGISTER BIT 1	PARADISE REGISTER BIT 5	CONFIG. REGISTER BIT 6	PARADISE REGISTER BIT 7	CLOCK SELECTION
PAR(4) = 1	X	X	X	X	CLOCK 2
X	MR(1) = 0	PAR(5) = 1	CNF(6) = 0	X	CLOCK 2
PAR(4) = 0	MR(1) = 1	X	X	PAR(7) = 1	CLOCK 1
PAR(4) = 0	X	PAR(5) = 0	X	PAR(7) = 1	CLOCK 1
PAR(4) = 0	X	X	CNF(6) = 1	PAR(7) = 1	CLOCK 1
PAR(4) = 0	MR(1) = 1	X	CNF(6) = 0	X	CLOCK 1
PAR(4) = 0	X	PAR(5) = 0	CNF(6) = 0	X	CLOCK 1
PAR(4) = 0	X	X	CNF(6) = 1	PAR(7) = 0	CLOCK 0

Internally, two other bits affect how the clock is used:

Paradise Register Bit 0 = 1 : Disable Mode Register Bit 0.
Paradise Register Bit 0 = 0 : Enable Mode Register Bit 0.

Mode Register Bit 0 = 1 : Normal (80 column display).
Mode Register Bit 0 = 0 : Divide selected video clock by 2 if enabled (40 column display).

(PAR(0) = 0) * (MR(0) = 0) = 40 Column mode.

For switch settings:
The Paradise Register, PAR(7:0), is set by the pull-up and pull-down resistors on the Video Memory Address Bus, MA(7:0).
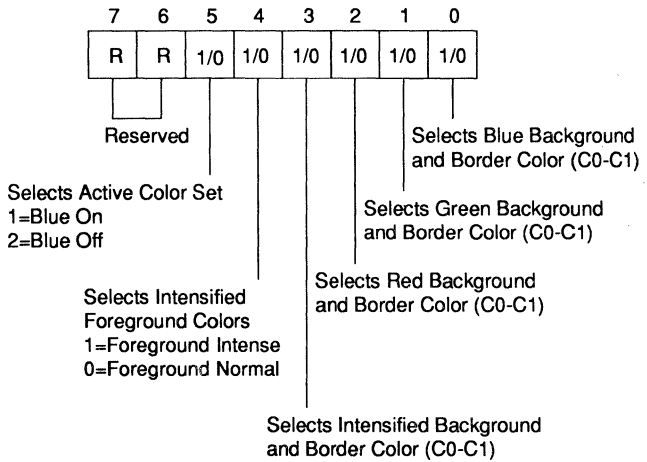The Configuration Register, CNF(7:0), is set by the pull-up and pull-down resistors on the Video Data Bus, MD(7:0).
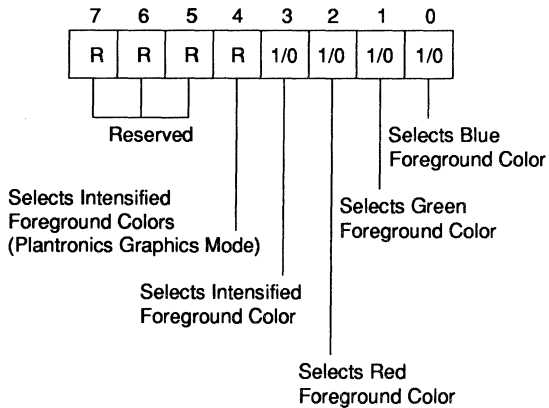
CGA BORDER CONTROL REGISTER

CGA BORDER CONTROL REGISTER 320 X 200 GRAPHICS MODE
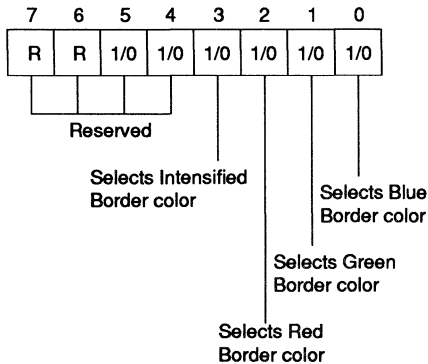### (MEDIUM RESOLUTION) - WRITE-ONLY PORT = 3D9

```
  7   6   5   4   3   2   1   0
+---+---+---+---+---+---+---+---+
| R | R |1/0|1/0|1/0|1/0|1/0|1/0|
+---+---+---+---+---+---+---+---+
```

Reserved

Selects Blue Background
and Border Color (C0-C1)

Selects Active Color Set
1=Blue On
2=Blue Off

Selects Green Background
and Border Color (C0-C1)

Selects Red Background
and Border Color (C0-C1)

Selects Intensified
Foreground Colors
1=Foreground Intense
0=Foreground Normal

Selects Intensified Background
and Border Color (C0-C1)

CGA BORDER CONTROL REGISTER 640 X 200 GRAPHICS MODE
(HIGH RESOLUTION) - WRITE-ONLY PORT = 3D9

```
  7   6   5   4   3   2   1   0
+---+---+---+---+---+---+---+---+
| R | R | R | R |1/0|1/0|1/0|1/0|
+---+---+---+---+---+---+---+---+
```

Reserved

Selects Blue
Foreground Color

Selects Intensified
Foreground Colors
(Plantronics Graphics Mode)

Selects Green
Foreground Color

Selects Intensified
Foreground Color

Selects Red
Foreground Color

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CGA BORDER CONTROL REGISTER ALPHANUMERIC MODE
WRITE-ONLY PORT = 3D9

```
  7    6    5    4    3    2    1    0
┌────┬────┬────┬────┬────┬────┬────┬────┐
│ R  │ R  │1/0 │1/0 │1/0 │1/0 │1/0 │1/0 │
└────┴────┴────┴────┴────┴────┴────┴────┘
```

Reserved

Selects Intensified
Border color

Selects Blue
Border color

Selects Green
Border color

Selects Red
Border color

The CGA Border Control Register is a write-only register located at I/O port address 3D9. This register is cleared at reset.

Bit 7, Bit 6   Not used.

Bit 5   **Alphnumeric Mode**
Reserved.
320 x 200 Graphics Mode
Selects active color set in 320 X 200 graphics mode (medium resolution)
1 = Blue on.
0 = Blue off.
640 x 200 Graphics Mode
Reserved.

Bit 4   **Alphnumeric Mode**
Reserved.
320 x 200 Graphics Mode
Selects intensified foreground colors in 320 x 200 graphics mode
(medium resolution).
1 = Foreground intense.
0 = Foreground normal.
640 X 200 Graphics Mode
Selects intensified foreground colors in 640 X 200 Plantronics graphics mode
(high resolution).
1 = Foreground intense.
0 = Foreground normal.

CGA BORDER CONTROL REGISTER CONT'D

Bit 3   **Alphanumeric Mode**
1 = Selects intensified border color.
320 x 200 Graphics Mode
1 = Selects intensified background and border color (C0-C1).
640 x 200 Graphics Mode
1 = Selects intensified foreground color.

Bit 2   **Alphanumeric Mode**
1 = Selects red border color.
320 x 200 Graphics Mode
1 = Selects red background and border color (C0-C1).
640 x 200 Graphics Mode
1 = Selects red foreground color.

Bit 1   **Alphanumeric Mode**
1 = Selects green border color.
320 x 200 Graphics Mode
1 = Selects green background and border color (C0-C1).
640 x 200 Graphics Mode
1 = Selects green foreground color.

Bit 0   **Alphnumeric Mode**
1 = Selects blue border color.
320 x 200 Graphics Mode
1 = Selects blue background and border color (C0-C1).
640 x 200 Graphics Mode
1 = Selects blue foreground color.

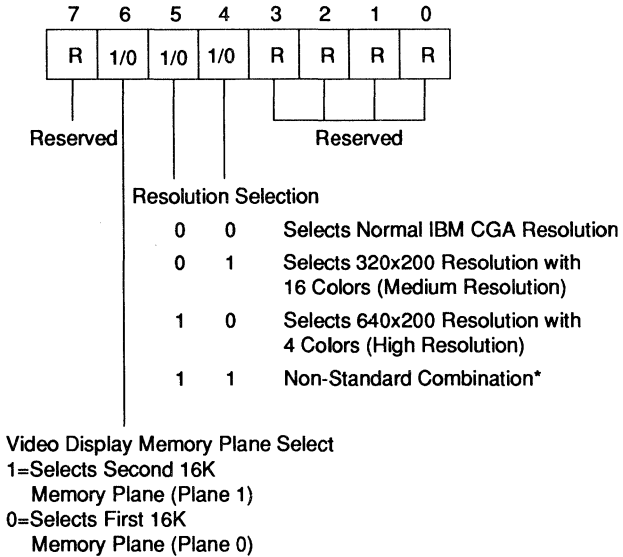**NOTE:** Any read or write to port 3B9 in mono mode sets the Light Pen Latch.

PORT 3DC

Any read or write to port 3DC in color mode sets the Light Pen Latch. (Port 3DC is the Preset Light
Pen Latch Register port in CGA).

PLANTRONICS COLORPLUS REGISTER

PLANTRONICS COLORPLUS REGISTER - WRITE-ONLY PORT = 3DD

```
  7   6   5   4   3   2   1   0
┌───┬───┬───┬───┬───┬───┬───┬───┐
│ R │1/0│1/0│1/0│ R │ R │ R │ R │
└───┴───┴───┴───┴───┴───┴───┴───┘
```

Reserved   Reserved

Resolution Selection

0	0	Selects Normal IBM CGA Resolution
0	1	Selects 320x200 Resolution with 16 Colors (Medium Resolution)
1	0	Selects 640x200 Resolution with 4 Colors (High Resolution)
1	1	Non-Standard Combination*

Video Display Memory Plane Select
1=Selects Second 16K
   Memory Plane (Plane 1)
0=Selects First 16K
   Memory Plane (Plane 0)

* NOTE: Bit 4 and bit 5 should not be set to one at the same time, since this is non-standard. If both bits are set to one, bit 4 overides bit 5.

The Plantronics Colorplus Mode Register is a write-only register located at I/O port address 3DD. This register controls the emulation of the Plantronics Colorplus features, allowing the display of 4 colors with a resolution of 640 x 200 pixels, or 16 colors with a resolution of 320 x 200 pixels. This register is cleared by alpha mode (Mode Register(1)=0), mono mode, or Plantronics disable (PAR(3)=1). The Plantronics Colorplus Register contains 3 active bits.

**PLANTRONICS COLORPLUS REGISTER CONT'D**

Bit 7   Not used

Bit 6   This bit is used to control the location where the CPU accesses the two
               individual 16K planes of video display memory. The video controller
               access to these planes is always contiguous, from B8000 hex to BFFFF
               hex. This bit is effective only if one of the two modes available in bits
               4 or 5 are selected, and the second video memory bank is needed.
               1 = Selects the second 16K plane of memory (Plane 1). Plane 1 is located
                   at B8000 hex and Plane 0 is at BC000 hex.
               0 = Selects the first 16K plane of memory (Plane 0). Plane 0 is now
                   located at B8000 hex and Plane 1 is at BC000.

Bit 5   1 = Selects 640 x 200 resolution with four colors (high resolution).
               0 = Selects normal IBM CGA resolution only if bit 4 is also set to "0".

Bit 4   1 = Selects 320 x 200 resolution with sixteen colors (medium resolution).
               0 = Selects normal IBM CGA resolution only if bit 5 is also set to "0".

Bit 3 - Bit 0 Not used.

HERCULES REGISTER

HERCULES REGISTER - WRITE-ONLY PORT = 3BF

7	6	5	4	3	2	1	0
R	R	R	R	R	R	1/0	1/0

Reserved
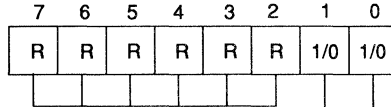
Enable Mode Reg. Bit 1
1=Graphics Mode Can Be Selected
   (Bit 1 of Mode Reg. Can Be Set)
0=Alpha Mode Forced
   (Bit 1 of Mode Reg. Cannot Be Set)

Enable Mode Reg. Bit 7
1=Second Page of Video Memory Can Be Accessed
   (Bit 7 of Mode Reg. Can Be Set)
0=Second Page of Video Memory Cannot Be Accessed
   First Page of Video Memory is Displayed
   (Bit 7 of Mode Reg. Cannot Be Set)

The Hercules Register is an 8-bit write-only register located at I/O port address 3BF hex and is used to control the Hercules Mode graphics with a monochrome display resolution of 720 x 348 pixels. Only bits 1 and 0 are used. Bits 7 thru 2 are reserved. Both bit 1 and bit 0 are reset to low(0), upon power-up or resetting the PVC4, or by selecting a color operating mode.

Bit 7 thru Bit 2   Reserved. (Do not use).

Bit 1   Enables Mode Register bit 7 (Address 3X8). Bit 7 of the Mode Register
                   is used by the Hercules Graphics Card to select the displayed memory page
                   in graphics mode. Mode Register(7)=1 selects the second page of the video
                   RAM, which is mapped to address B8000 hex. Mode Register(7)=0 selects
                   the first page of video RAM, which is mapped to address B0000 hex. This bit
                   also maps the PVC4 video memory into B8000-BFFFF, regardless of the state
                   of Mode Register Bit 7.
                   1 = Bit 7 of the Mode Register may be set and the second page of video
                       RAM may be accessed and displayed.
                   0 = Bit 7 of the Mode Register cannot be set, preventing the second page
                       of video RAM from being accessed or displayed. The first page of video
                       RAM is displayed.

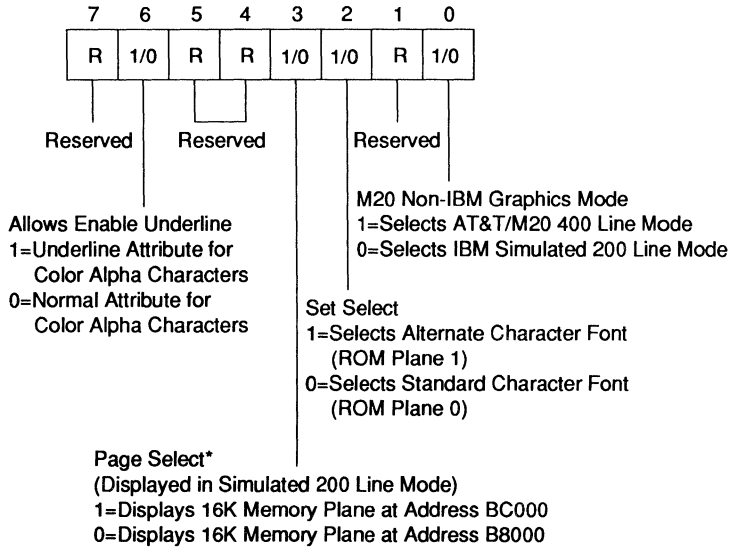**HERCULES REGISTER CONT'D**

Bit 0   Enables Mode Register bit 1 (Address 3X8). Mode Register(1)=1 selects
               graphics mode. Mode Register(1)=0 selects alpha mode.
               1 = Allows Bit 1 of the Mode Register to be set and alpha or graphics mode
                   may be selected.
               0 = Bit 1 of the Mode Register cannot be set, forcing alpha mode.

AT&T / M24 REGISTER

AT&T / M24 REGISTER - WRITE-ONLY PORT = 3DE

7	6	5	4	3	2	1	0
R	1/0	R	R	1/0	1/0	R	1/0

Reserved   Reserved   Reserved

M20 Non-IBM Graphics Mode
1=Selects AT&T/M20 400 Line Mode
0=Selects IBM Simulated 200 Line Mode

Allows Enable Underline
1=Underline Attribute for
   Color Alpha Characters
0=Normal Attribute for
   Color Alpha Characters

Set Select
1=Selects Alternate Character Font
   (ROM Plane 1)
0=Selects Standard Character Font
   (ROM Plane 0)

Page Select*
(Displayed in Simulated 200 Line Mode)
1=Displays 16K Memory Plane at Address BC000
0=Displays 16K Memory Plane at Address B8000

*NOTE: This bit has no effect if bit 0 of the AT&T / M24 Register is set to 1.

The AT&T / M24 Register is a write-only register located at I/O port address 3DE hex. It is used to produce a display resolution of 640 x 400 pixels. In AT&T nomenclature, this mode is referred to as "Mode Select 2". In order for this register to be enabled, bit 3 of the Paradise Register must equal 0. (NOTE: Reset disables the AT&T / M24 Register and sets all its bits to 0).

Bit 7   Reserved.

Bit 6   Enable Underline
                    1 = Causes an attribute of "blue foreground, black background" to produce
                        a white, underlined character.
                    0 = Normal attribute for color alpha characters.

AT&T / M24 REGISTER CONT'D

Bit 5, Bit 4   Reserved.

Bit 3   Page Select. This bit is used to toggle between 16K pages of display
                memory when operating in the simulated 200 line mode, after bit 0 of the
                AT&T / M24 Register has been set to 0. (NOTE: This bit has no effect
                if bit 0 of the AT&T / M24 Register is set to 1).
                1 = Causes the video controller in PVC4 to display the 16K plane of
                    memory at address BC000 hex, in simulated 200 line mode.
                0 = The 16K plane of memory at address B8000 hex is displayed, in
                    simulated 200 line mode.

Bit 2   Set Select. This bit selects between two character fonts.
                1 = Selects the alternate the character font (ROM Plane 1).
                0 = Selects the standard character font (ROM Plane 0).

Bit 1   Reserved.

Bit 0   M24, Non-IBM Graphics Mode.
                1 = Selects AT&T / M24 400 line mode (two color).
                0 = Selects simulated IBM 200 line mode, i.e. double-scanned lines.
                (Note: If the AT&T / M24 Register is disabled, IBM standard 200 line
                mode is displayed).

PVC4

6845 CRT CONTROLLER REGISTERS

Register name	Port (hex)	Index (3 x 4 hex)	R/W
Horizontal Total	3X5	00	W
Horizontal Displayed	3X5	01	W
H. Sync. Character Position	3X5	02	W
H. Sync. Character Width	3X5	03	W
Vertical Total	3X5	04	W
Vertical Adjust	3X5	05	W
Vertical Displayed	3X5	06	W
V.Sync. Char. Row Position	3X5	07	W
*Not Used		08	
Maximum Scan Line Address	3X5	09	W
Cursor Start	3X5	0A	W
*Cursor End	3X5	0B	W
RAM Start Address High	3X5	0C	W
RAM Start Address Low	3X5	0D	W
Cursor RAM Address High	3X5	0E	R/W
Cursor RAM Address Low	3X5	0F	R/W
Light Pen High	3X5	10	R
Light Pen Low	3X5	11	R
*Reserved	3X5	1C	N/A
*Reserved	3X5	1D	N/A
*Reserved	3X5	1E	N/A
*Reserved	3X5	1F	N/A

Notes: 1. CRT Controller Registers must be unlocked before they can be accessed, by writing the register index to address 3X4, and then writing the data to, or reading the data from, address 3X5.

2. "X" = B (hex) in monochrome MDA modes, and D (hex) in color CGA modes.

3. * = This register is not identical to the 6845 definition.

PVC4

6845 CRT Controller Registers (CRTC)

Index (Hex)	Register Name	Register Field Details	Register Bit Definitions 7	6	5	4	3	2	1	0
00	Horizontal Total	Horizontal Total Character Count Less 1 - Bits (7-0)	-	-	-	-	-	-	-	-
01	Horizontal Displayed	Horizontal Displayed Character Count - Bits (7-0)	-	-	-	-	-	-	-	-
02	H. Sync Character Position	Horizontal Sync Character Position - Bits (7-0)	-	-	-	-	-	-	-	-
03	H. Sync Character Width	Horizontal Sync Character Width - Bits (3-0)	R	R	R	R	-	-	-	-
04	Vertical Total	Vertical Total Character Row Count Less 1 - Bits (6-0)	R	-	-	-	-	-	-	-
05	Vertical Adjust	Vertical Adjust Scan Lines Bits (4-0)	R	R	R	-	-	-	-	-
06	Vertical Displayed	Vertical Displayed Character Row Count - Bits (6-0)	R	-	-	-	-	-	-	-
07	V. Sync Character Row Position	Vertical Sync Character Row Position - Bits (6-0)	R	-	-	-	-	-	-	-
*08	Not Used	The PVC4 Supports only the Non-Interlace Mode								
09	Max. Scan Line Address	Maximum Scan Line Address (per character) Less 1 - Bits (4-0)	R	R	R	-	-	-	-	-

Notes: 1. R = Reserved Bits.

2. Bit 0 = LSB.

3. * = This register is not identical to the 6845 definition.

PVC4

6845 CRT Controller Registers (CRTC) (Cont'd)

Index (Hex)	Register Name	Register Field Details	7	6	5	4	3	2	1	0
					Register Bit Definitions					
0A	Cursor StartOn/Off	Cursor On/Off Bit (Q5), and Cursor Start Scan Line Bits (4-0)	R	R	Q5	CS4	CS3	CS2	CS1	CS0
*0B	Cursor End	Unlocked: Cursor End Scan Line. Locked: Underline Scan Line Bits (4-0)	R	R	R	-	-	-	-	-
0C	RAM Start Address High	RAM Starting Address High Bits (5-0)	R	R	-	-	-	-	-	-
0D	RAM Start Address Low	RAM Starting Address Low Bits (7-0)	-	-	-	-	-	-	-	-
0E	Cursor RAM Address High	Cursor RAM Address High Bits (5-0)	R	R	-	-	-	-	-	-
0F	Cursor RAM Address Low	Cursor RAM Address Low Bits (7-0)	-	-	-	-	-	-	-	-
10	Light Pen High	Light Pen Address High Bits (5-0)	R	R	-	-	-	-	-	-
11	Light Pen Low	Light Pen Address Low Bits (7-0)	-	-	-	-	-	-	-	-

Notes: 1. R = Reserved bits.
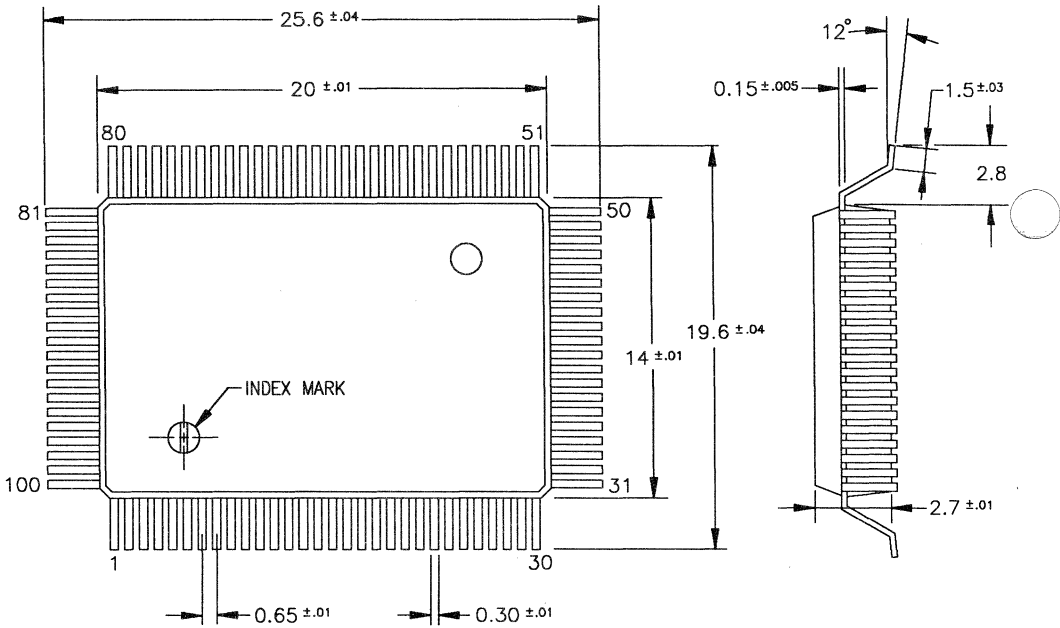
2. Bit 0 = LSB.

3. * = This register is not identical to the 6845 definition.

100-PIN SHENKO FLAT PACKAGE

NOTE: ALL DIMENSIONS ARE IN MILLIMETERS

Paradise Video Controller

PVC4

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