System Programming Manual

VX855 / VX875 Series

Preliminary Revision 1.21
October 4, 2011

VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	10/22/09	Initial public release	LW
1.1	1/21/10	Modify copyright page Modify description of D17F0_Rx97	LW
1.2	8/4/11	Modify D17F0 Rx95[0] and PMIO Rx20[14]	DA
1.21	10/4/11	Updated Taiwan office address in legal page Updated D20F0 Rx3D description	JW

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

REGISTERS OVERVIEW

Register Document Introduction

This document includes the registers for VIA VX855 and VX875. Please refer to Table 1 for the specification differences of VX855 and VX875 series products.

This chip integrates functional modules of the traditional North Bridge and South Bridge chips, plus 3D/2D and Video Processors, Video Decoding Accelerator and controller for external display interface. The register set is partitioned into three blocks: North Module, South Module and Graphics and Video Module; of which, North Module and South Module registers are described in this **System Programming Manual** while graphics and video registers are described in the **Graphics Programming Guide**.

Table 1. VX855 and VX875 Feature Comparison Table

Product Model	VX855	VX875
FSB Speed (MHz)	400-800	400-533
Memory Type	DDR2-800 1.5V / 1.8V	DDR2-667 1.5V / 1.8V
Snapshot Memory	Yes	Yes
Core Voltage	1.2V	1.03V
Ball Pitch	27x27	21x21

Module and Register Scope Definitions

Module Name Abbreviations

NM: North Module. It contains functional modules of the traditional North Bridge chip.
SM: South Module. It contains functional modules of the traditional South Bridge chip.
NSMIC: North-South Module Interface Control
SNMIC: South-North Module Interface Control
PM: Power Management
HDAC: High Definition Audio Controller

Register Scope Map within Modules

To specifically identify every function, the following abbreviations will be applied in subsequent sections.

Abbreviation of Register Space / Module Name	Register Space	Function
	North Module	
D0F0	PCI Device 0, Function 0	Host Controller
D0F1	PCI Device 0, Function 1	Error Reporting
D0F2	PCI Device 0, Function 2	Host Bus Control
D0F3	PCI Device 0, Function 3	DRAM Bus Control
D0F4	PCI Device 0, Function 4	Power Management and Chip Testing Control
D0F5	PCI Device 0, Function 5	APIC and Central Traffic Control
D0F6	PCI Device 0, Function 6	Scratch Registers
D0F7	PCI Device 0, Function 7	North-South Module Interface Control **<NSMIC>**

Abbreviation of Register Space / Module Name	Register Space	Function
South Module		
D11F0	PCI Device 11, Function 0	USB Mass Storage Device
USBD-MMIO	Memory Space	USB Device Memory Mapped I/O Space Registers
D12F0	PCI Device 12, Function 0	SDIO Host Controller
SDIO-MMIO	Memory Space	SDIO Memory Mapped I/O Space Registers
D13F0	PCI Device 13, Function 0	Card Reader Controller
xDC-MMIO	Memory Space	Extreme Digital-Picture Controller Memory Mapped I/O Space
SDC-MMIO	Memory Space	Security Digital Controller Memory Mapped I/O Space Registers
Data DMA-MMIO	Memory Space	Data DMA Memory Mapped I/O Space Registers
CICH DMA-MMIO	Memory Space	CICH DMA Memory Mapped I/O Space Registers
PCI Control-MMIO	Memory Space	PCI Control Memory Mapped I/O Space Registers
D15F0	PCI Device 15, Function 0	Serial ATA and EIDE Controller
IDE-IO	IO Space	Bus Master IDE I/O Space Registers
D16F0	PCI Device 16, Function 0	USB 1.1 UHCI Ports 0-1
D16F1	PCI Device 16, Function 1	USB 1.1 UHCI Ports 2-3
D16F2	PCI Device 16, Function 2	USB 1.1 UHCI Ports 4-5
USB 1.1-IO	IO Space	USB 1.1 I/O Space Registers
D16F4	PCI Device 16, Function 4	USB 2.0 EHCI Controller, Ports 0-5
USB 2.0-MMIO	Memory Space	EHCI USB 2.0 Memory Mapped I/O Space Registers
D17F0	PCI Device 17, Function 0	Bus and Power Management Control
PMIO	IO Space	ACPI I/O Registers
PM-MMIO	Memory Space	Power Management Memory Mapped I/O Space Registers
SMIO	IO Space	System Management Bus I/O Space Registers
HPET	Memory Space	HPET Memory Mapped I/O Space Registers
SPI-MMIO	Memory Space	Special Peripheral Interface Memory Mapped I/O Space Registers
SPI0-MMIO	Memory Space	SPI Bus 0 Memory Mapped I/O Space Registers
SPI1-MMIO	Memory Space	SPI Bus 1 Memory Mapped I/O Space Registers
UART-IO	IO Space	UART Host Controller I/O Space Registers
UART DMA-IO	IO Space	UART DMA Controller I/O Space Registers
D17F7	PCI Device 17, Function 7	South-North Module Interface Control **<SNMIC>**
D19F0	PCI Device 19, Function 0	PCI-to-PCI Bridge
D20F0 / HDAC	PCI Device 20, Function 0	High Definition Audio Controller
HDAC-MMIO	Memory Space	HDAC Memory Mapped I/O Space Registers

Register Table Format

Basic Attribute Definitions:

RO: Read Only.
WO: Write Only (register value can not be read by the software).
RW: Read / Write.
RW1: Write Once then Read Only after that.
RW1C: Read / Write of "1" clears bit to zero.

Sticky Attributes: adding a "S" in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.

ROS: Sticky-Read-Only.
WOS: Sticky-Write-Only.
RWS: Sticky-Read/Write.
RW1S: Sticky-Write-Once.
RW1CS: Sticky-Write-1-to-Clear.

Special Default Value Definitions

Dip: Means the default value is set by dip switch or strapping.
HwInit: Hardware initialized; bit default value is set by hardware to reflect related status.
ROMSIP: The default value with ROMSIP attribute is loaded from preset ROM when chipset resets.

PCI Arbiter Control

I/O Port Address: 22h
PCI Arbiter Disable **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**PCI2 Arbiter Control** 0: Enable PCI2 Bus Arbiter 1: Disable PCI2 Bus Arbiter
0	RW	0	**PCI1 Arbiter Control** 0: Enable PCI1 Bus Arbiter (arbiter will respond to REQ# assertion) 1: Disable PCI1 Bus Arbiter (arbiter will not respond to PCI-1 REQ# and PREQ# assertion)

PCI Configuration Space I/O

This chip's PCI space registers are addressed via the following configuration mechanism:
Mechanism #1
These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

I/O Port Address: CFB-CF8h
PCI Configuration Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Configuration Space Enable** 0: Disable 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	**Reserved** Always reads 0
23:16	RW	0	**PCI Bus Number** Used to choose a specific PCI bus in the system
15:11	RW	0	**Device Number** Used to choose a specific device in the system
10:8	RW	0	**Function Number** Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	**Register Number (also called the "Offset")** Used to select a specific DWORD in the configuration space
1:0	RW	0	**Fixed** Always reads 0

I/O Port Address: CFF-CFCh
PCI Configuration Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI Configuration Data**

Note: Refer to PCI Bus Specification Version 2.3 for further details on operation of the above configuration registers.

Device 0 Function 0 (D0F0): Host Control

PCI Configuration Space

All registers in D0F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F0)
Device ID **Default Value: 0409h**

Bit	Attribute	Default	Description
15:0	RO	0409h	**Device ID Code**

Offset Address: 05-04h (D0F0)
PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0. (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0. (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	1b	**Support New Capability List** 0: No new capability 1: Support new capability
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Chip Revision Code**

Offset Address: 0B-09h (D0F0)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D0F0)

PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice for CPU as A Master (In Unit of PCI Clocks)**
2:0	RO	0	**Reserved** Bits [2:1] is programmable; however, it's read as 0.

Offset Address: 0Eh (D0F0)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Default value is 80h when Rx4F[0] = 1

Offset Address: 0Fh (D0F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F0) – Reserved

Offset Address: 2D-2Ch (D0F0)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F0)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F0) – Reserved

Offset Address: 34h (D0F0)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space 0 indicates the end of the list.

Offset Address: 35-3Fh (D0F0) – Reserved

Offset Address: 40-4Eh (D0F0) – Reserved

Multiple Function and Legacy Space Access Control (4F-C6h)

Offset Address: 4Fh (D0F0)

Multiple Function Control **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	1b	**Multi-Function Support** 0: Disable. Registers of functions 1-7 cannot be accessed, and the value returned will be 0FFFFFFFFh when accessed. 1: Enable. The status will be reflected on Rx0E[7].

Offset Address: 50-BFh (D0F0) – Reserved

Offset Address: C0h (D0F0)

Graphics Shadow Memory and IO Space Access Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	1	**Memory Space Access** Two memory spaces of GFX are used: SL, MMIO. 0: Does not respond to memory space access 1: Responds to memory space access
0	RO	1	**I/O Space Access** The IO address ranges are 3B0h~3B7h, 3B8h~3BBh and 3C0h~3DFh. 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: C1-C5h (D0F0) – Reserved

Offset Address: C6h (D0F0)

Legacy Space Access Control **Default Value: nnh**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4:2	RO	x	**Reserved**
1	RW	0	**MDA Resource Location** 0: PCI2. Forward MDA access cycles to PCI2. 1: PCI1. Forward MDA access cycles to PCI1. The setting of this bit overwrites the settings on the IO / Memory's Base and Limit of other devices. MDA Resources include Memory: B0000h-B7FFFFh and I/O Ports 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh.
0	RO	x	**Reserved**

Control Registers for Integrated Graphics / Video Processor (C7-FFh)

Offset Address: C7h (D0F0) – Reserved

Offset Address: CB-C8h (D0F0)

GFX Shadow Memory Base 0 - S.L. **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:16	RO	FFF0h	**GFX's Memory Base 0 Address[31:16] for S.L.**
15:0	RO	0000h	**GFX's Memory Base 0 Address[15:0] for S.L.**

Offset Address: CF-CCh (D0F0)

GFX Shadow Memory Base 1 - MMIO — **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:20	RO	FFFh	**GFX's Memory Base 1 Address [31:20] for MMIO**
19:0	RO	00000h	**GFX's Memory Base 1 Address[19:0] for MMIO**

Offset Address: D0-D3h (D0F0) – Reserved

Offset Address: D4h (D0F0)

GFX Memory Control — **Default Value: 03h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	1	**GFX's Memory Base 1 Address for MMIO Enable** 0: Disable 1: Enable
0	RW	1	**GFX's Memory Base 0 Address for S.L. Enable** 0: Disable 1: Enable

Offset Address: D5-DFh (D0F0) – Reserved

Offset Address: E0h (D0F0)

Graphics Shadow Power State — **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RO	00b	**GFX Device Power State** 00: D0 state 01: D1 state 10: D2 state 11: D3 state Central Traffic Controller will forward downstream cycle to GFX only when bits [1:0] = 00. Otherwise, Central Traffic Controller will forward it to P1.

Offset Address: E1-FDh (D0F0) – Reserved

Offset Address: FEh (D0F0)

Legacy VGA Cycle Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:5	RW	0	**Reserved**
4	RW	0	**Enable Base VGA 16 Bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3:0	RW	0	**Reserved**

Offset Address: FFh (D0F0) − Reserved

DEVICE 0 FUNCTION 1 (D0F1): ERROR REPORTING

PCI Configuration Space

All registers in D0F1 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 1.

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F1)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F1)
Device ID — **Default Value: 1409h**

Bit	Attribute	Default	Description
15:0	RO	1409h	**Device ID**

Offset Address: 05-04h (D0F1)
PCI Command — **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RO	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F1)

PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target Abort Assertion** This chip does not assert Target Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed ; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F1)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F1)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F1)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D0F1)

PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master (In Unit of PCI Clock)**
2:0	RO	0	**Reserved** Bits [2:1] are programmable; however, it’s read as 0.

Offset Address: 0Eh (D0F1)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F1)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F1) – Reserved

Offset Address: 2D-2Ch (D0F1)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F1)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F1) – Reserved

Offset Address: 34h (D0F1)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-3Fh (D0F1) – Reserved

Offset Address: 40-5Fh (D0F1) – Reserved

Host Bus Error Report (60-6Fh)

Offset Address: 60h (D0F1)

Host Parity Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Host Address Parity Error Detected** 0: Not detected 1: Detected
6	RW1C	0	**Host Data Parity Error Detected** 0: Not detected 1: Detected
5	RW1C	0	**AGP Access Above 4G Detected** 0: No above 4GB AGP cycles being detected 1: AGP Access Above 4GB detected
4	RW1C	0	**Host LOCK Cycle to PCI Detected** 0: Not detected 1: Detected
3:0	RO	0	**Reserved**

Offset Address: 61-67h (D0F1) – Reserved

Offset Address: 68h (D0F1)

Host Parity Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved** Do not program the register. Keep it as 0.
6	RW	0	**Reserved** Do not program the register. Keep it as 0.
5	RW	0	**Reserved** Do not program the register. Keep it as 0.
4	RW	0	**Reserved** Do not program the register. Keep it as 0.
3	RW	0	**Parity Test Mode** 0: Disable (normal mode) 1: Enable (invert the parity bit) Do not program register. Keep it as 0.
2:0	RW	0	**Reserved**

Offset Address: 69-6Fh (D0F1) – Reserved

Offset Address: 70-FFh (D0F1) – Reserved

DEVICE 0 FUNCTION 2 (D0F2): HOST BUS CONTROL

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F2)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F2)
Device ID **Default Value: 2409h**

Bit	Attribute	Default	Description
15:0	RO	2409h	**Device ID Code**

Offset Address: 05-04h (D0F2)
PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (N/A)
8	RO	0	**SERR# Enable** Hardwired to 0 (N/A)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (N/A)
6	RO	0	**Parity Error Response** Hardwired to 0 (N/A)
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (N/A)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (N/A)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (N/A)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F2)
PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** Hardwired to 0 (N/A)
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master-Abort (Except Special Cycle)** Hardwired to 0 (N/A)
12	RO	0	**Received Target-Abort** Hardwired to 0 (N/A)
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** Hardwired to 0 (N/A)
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F2)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F2)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F2) – Reserved

Offset Address: 0Dh (D0F2)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PCI Bus Time Slice for CPU as a Master (in Unit of PCI clocks)**

Offset Address: 0Eh (D0F2)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h indicates this is a multi-function device.

Offset Address: 0Fh (D0F2)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F2) – Reserved

Offset Address: 2D-2Ch (D0F2)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F2)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F2) – Reserved

Offset Address: 34h (D0F2)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** This function does not have capability lists.

Offset Address: 35-4Fh (D0F2) – Reserved

Host CPU Control (50-5Fh)

Offset Address: 50h (D0F2)
Request Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	dip	**IOQ (In-Order Queue) Depth** 0: 1 level 1: 12 levels Default sets from the PDA0 signal during system initialization. For strap pin information, check the Strap Pin table for details.
6	RO	dip	**PLLOK Source Select** 0: PLLOK from NBPLL 1: PLLOK from SB logic
5	RW	0	**Reserved**
4:0	RW	0	**Dynamic Defer Snoop Stall Count** Count for the Defer Snoop Stall timer. The timer starts counting at the beginning of the snoop phase of a cycle which is not directed to DRAM; it increases one for every 2 host clocks. Before the timer expires, the controller will use Snoop Stall protocol to extend the snoop phase. When the timer expires, if that cycle is not finished and the IOQ of the host controller has been queued more cycles (could be from CPU before the snoop phase of the current request or from upstream masters), a Defer/Retry response will be replied to the CPU bus for that cycle. How the controller will do on the response phase will depend on the register setting on Rx51[4,1,0]. Please refer to Table 3 (Rx51[1]). 00h: timer count is 0 host clocks, i.e., the host controller goes to the response phase immediately. 01h: timer count is 2 host clocks. …. 0Fh: timer count is 30 host clocks. 10h: timer count is 32 host clocks. …. 1Fh: timer count is 62 host clocks. Note: Please refer to Table 2 (Rx50[1]) below for the response of the host controller upon different situations.

Table 2. RX50[1] Dynamic Defer Snoop Stall Table

Timer Expire	IOQ has more requests followed the current downstream cycles	The current downstream cycles - Completion	The action of the host controller of this chip does on the host bus upon the conditions on the left column:
No	-	No	Snoop Stall to extend the snoop phase.
No	-	Yes	Go to response phase and do Normal Data Response.
Yes	No	No	Snoop Stall to extend the snoop phase.
Yes	No	Yes	Go to response phase and do Normal Data Response
Yes	Yes	No	Go to response phase and do Defer/Retry Response
Yes	Yes	Yes	Go to response phase and do Normal Data Response

Offset Address: 51h (D0F2)

CPU Interface Control – Basic Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Fast Cycle Control for CPU to DRAM Read Cycle** Host controller finishes the CPU to DRAM read cycle earlier. 0: Disabled, the host controller will wait for all data (e.g. 8QW) coming back from the DRAM controller to finish its CPU to DRAM read cycle. i.e. the host controller won't enter the data phase on the GTL bus until all the data has returned from the DRAM controller. 1: Enabled, the host controller will finish its CPU to DRAM read cycle before all read data returned from the DRAM controller. This is for better CPU to DRAM read performance.
6	RW	0	**Read Around Write** The CPU read command can bypass the queued CPU write command to let DRAM controller process the read first. 0: Disable 1: Enable Note: When this bit is enabled, the policy of CPU to DRAM write retire become critical for the entire system performance. Please refer to Table 4 (Rx52[1]) & Table 6 (Rx5E[1]) for more details.
5	RW	0	**CPU to Memory Request Queue Control** Request pipelining for host controller to DRAM controller 0: Disable 1: Enable
4	RW	0	**Defer Response Control** This bit works for CPU memory Read cycles targeted to non-DRAM agents, some other memory cycles and CPU IOR cycles. 0: Disable, for the cycles listed above, host controller will do retry on the CPU bus until the cycle is complete. 1: Enable, for the cycles listed above, host controller will do defer on the CPU bus. Note: please refer to Table 3 (Rx51[1]) for more details.
3	RW	0	**Defer / Retry Queue Entries** This bit specified the number of defer/retry queue entries for CPU memory read cycles targeted to non-DRAM agents and CPU IOR cycles. 0: 1 entry 1: 2 entries
2	RW	0	**2-Entry Defer / Retry Queue Sharing Policy** 0: One entry for each host processor 1: Each entry is shared by the two host processors
1	RW	0	**Special Cycle Handling** 0: Host controller will treat the special cycle as a posted write cycle. A "Normal response" will be returned to CPU bus. 1: Host controller will treat the special cycle as a non-posted write cycle. A "Defer response" will be returned to CPU bus. Note: please refer to Table 3 (Rx51[1]) for more details.
0	RW	0	**Defer Response Control for I/O Write and Some Memory Write Cycles** 0: Host controller will do defer response on the CPU bus for some cycles. 1: Host controller will always do retry on the CPU bus for the some cycles until those cycle are complete. Note: please refer to Table 3 (Rx51[1]) for more details.

Note: For different downstream cycles on the CPU side, with different registers setting at Rx51[4,1,0], the host controller's responses are shown in Table 3 (Rx51[1]) below.

Table 3. Rx51[1] The host controller's response for different cycles at different register settings.

	Rx51[4]	0	0	0	0	1	1	1	1
	Rx51[1]	0	0	1	1	0	0	1	1
	Rx51[0]	0	1	0	1	0	1	0	1
Cycles	**Target**	**Response Phase Action**							
CPU Memory *Read*	DRAM	N	N	N	N	N	N	N	N
CPU Lock *Read*	Extended Configuration, Others (GFX, or SB devices)	R	R	R	R	D	D	D	D
CPU I/O *Read*	Internal Configuration Space, Others (GFX, or SB devices)	R	R	R	R	D	D	D	D
CPU Memory *Write*	DRAM	N	N	N	N	N	N	N	N
	Extended Configuration	R	R	R	R	R	D	R	D
	Others (GFX, or SB devices)	N	N	N	N	N	N	N	N
CPU Lock *Write*	DRAM	N	N	N	N	N	N	N	N
	Others (GFX, or SB devices)	R	R	R	R	R	D	R	D
CPU I/O *Write*	Internal Configuration Space, Others (GFX, or SB devices)	R	R	R	R	R	D	R	D
Special Cycle	SB Devices								

Notes:
N: Normal; **D**: Defer; **R**: Retry

Table 4. Rx52[1] DRAM Write Retire Policy

Rx51[6]	**Rx52[3]**	**Rx55[2]**	**Rx56[7:4]**	**Rx5D[7:4]**	**Rx5D[3:0]**	Write Policy* for write requests which might come from CPU or upstream masters.
0	-	-	----	----	----	Host controller will issues read or write cycles to the DRAM controller in the order of their coming in sequence. These include upstream cycles.
1	0	-	----	----	----	If the DRAM bus is idle (i.e. all the DRAM read cycles are finished), the host controller will of course start to flush all DRAM write requests out. However, if the DRAM bus is busy (i.e. DRAM read cycles are on going), the host controller will start to flush those write requests only when the write queue is full. It will stop flushing when the write queue is not full.
1	1	0	----	x	y	If the DRAM bus is idle (i.e. all the DRAM read cycles are finished), the host controller will of course start to flush all DRAM write requests out. However, if the DRAM bus is busy (i.e. DRAM read cycles are on going), host controller will start to flush the write requests out to the DRAM controller when the request count in the write queue accumulates to x, and it will stop flushing those write requests when the request count in the write queue lowers to y. where x= 0000b means count is 1, x=1111b means count is 16; y= 0000b means count is 1, y=1111b means count is 16; and since the write queue in this chip is only 12 levels, so: (a) x must be in between 0000b and 1011b (b) y must be in between 0000b and 1011b (c) x must be >= y.
1	1	1	z	x	y	If the DRAM bus is idle (i.e. all the DRAM read cycles are finished), the host controller will of course start to flush all DRAM write requests out. However, if the DRAM bus is busy (i.e. DRAM read cycles are on going), host controller will start to flush the write requests out to the DRAM controller when the request count in the write queue accumulates to z, and it will stop flushing those write requests when the request count in the write queue lowers to y. where z= 0000b means count is 1, z=1111b means count is 16; y= 0000b means count is 1, y=1111b means count is 16; and since the write queue in this chip is only 12 levels, so: (a) z must be in between 0000b and 1011b (b) y must be in between 0000b and 1011b (c) z must be >= y. (d) z must be <= x.

Note: In addition to what being listed in this table, there are extra adjustments in Table 6 (Rx5E[1]). Please also refer to register Rx5E, Rx5F[2], Rx5F[1] for more information.

Offset Address: 52h (D0F2)
CPU Interface Control – Advanced Option **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**RS Response Phase Pipeline Control** The interval in between two response phases of CPU write and CPU read (including upstream read cycles) is 0: 1T 1: 0T, the pins HRS[2:0]# can be continuously asserted.
6	RW	0	**High Priority Request to DRAM Controller** Priority request to DRAM controller for efficient DRAM usage. 0: Disable. All the cycles to DRAM controller will be treated as normal priority. 1: Enable. Requests to DRAM controller will have high priority when a) the CPU write request queue is full, or b) the upstream cycles which targeted to DRAM controller have high priority entity (this can be done by programming corresponding register bits on the register space of different devices connected to the system).
5	RO	0	**Reserved**
4	RW	0	**Reserved**
3	RW	0	**DRAM Write Retire Policy - I** DRAM write retire policy with high and low threshold on the request counts in the write queues for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 4 (Rx52[1]) for detailed operations. 0: Disable 1: Enable
2	RW	1b	**Reserved**
1:0	RW	00b	**Speculative Read Policy** Speculative read refers to the case that the host controller issues read request to the DRAM controller prior to knowing the result of the snoop of a read request which originated from the CPU or an upstream device. However, if the read cycle does hit the cache inside another CPU (for multi-CPU's case) or inside the single CPU (i.e. for upstream read cycle's case), the speculative read which had just been executed will need to be discarded. -0: Speculative read is disabled, i.e., host controller only issues read to DRAM controller after it gets to know the snoop result of that read cycle. 01: Speculative read applied only when the read request queue in the host controller before this in coming read request is empty, i.e., the speculative read only happened for the first read in a bunch of consecutive reads. 11: Speculative read applied to every read requests.

Offset Address: 53h (D0F2)
Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Host Occupancy Timer** In arbitration for the read/write requests to DRAM controller from the CPU or the upstream master devices, this timer guarantees a period of time counted by the number of host clocks (in unit of 4 host clocks) that the requests from the CPU can be serviced as long as there are continuous requests from the CPU. 0000: Infinite. 0001: 1 x 4 host clocks. 0010: 2 x 4 host clocks. … 1111: 15 x 4 host clocks.
3:0	RW	0000b	**Master Occupancy Timer** In arbitration for the read/write requests to DRAM controller from the CPU or the upstream master devices, this timer guarantees a period of time counted by the number of host clocks (in unit of 4 host clocks) that the requests from the upstream masters can be serviced as long as there are continuous requests from the upstream master devices. 0000: Infinite. 0001: 1 x 4 host clocks. 0010: 2 x 4 host clocks. … 1111: 15 x 4 host clocks.

Note: The host controller arbitrates the requests from the CPU and upstream masters guarded by these two occupancy timers. When two requests coming in from CPU and the upstream master at the same time, the controller will serve the one which had been serviced last time.

Offset Address: 54h (D0F2)
Miscellaneous Control 1 **Default Value: 60h**

Bit	Attribute	Default	Description
7:5	RO	000b dip	**CPU FSB Frequency** This register setting must be consistent with the HCLK frequency setting. When this bit is set to Auto Mode, the chip can detect the frequency itself. However, HCLK must be running at one of the following frequencies: 000: 100MHz 001: 133MHz 010: 200MHz 111: Auto mode Others: Reserved Default value comes from the GPIO[12:10] signals during system initialization. For strap pin information, check the Strap Pin table for details.
4	RW	0	**8QW Burst Memory Access** Host controller takes 8QW read/write cycles from either CPU or upstream masters and sends them to DRAM controller. 0: Disabled, host controller splits the 8QW r/w requests into two 4QW cycles. 1: Enabled, host controller will forward the 8QW r/w requests to DRAM controller. Noted: Not being implemented completely, this bit must be programmed to 1.
3	RW	0	**Host Controller to DRAM Read Cycle Control - I** The read cycle control for requests from either CPU or upstream masters to DRAM controller. 0: Normal mode. 1: Special mode. This bit works with other registers (Rx55[1]; Rx90[1:0]) in different conditions for the DRAM read cycle.
2	RW	0	**Merge 4QW to 8QW Burst Memory Access for Upstream Cycles.** The bit is the option for host controller to merge two 4QW upstream master read or write cycles into one 8QW cycle and to send it to DRAM controller. 0: Disable 1: Enable
1	RW	0	**Memory to Host Controller Conversion Mode** 0: Transparent mode 1: Synchronous mode (some control signals will be synchronized 1T in certain clock phases) Note: Transparent mode (default operating mode) is faster than Sync mode. This register option affects the timing of host controller to DRAM controller accessing.
0	RO	0	**Reserved**

Offset Address: 55h (D0F2)
Miscellaneous Control 2 **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RO	1b	**Reserved (Do Not Program)**
4:3	RW	0	**Reserved**
2	RW	0	**DRAM Write Retire Policy – II** In addition to write queue threshold registers in Rx5D[7:4] and Rx5D[3:0], this register is an extra option for write retire policy with medium threshold on the request counts in the write queues for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 4 (Rx52[1]) for detail operation. 0: Disable 1: Enable
1	RW	0	**Host Controller to DRAM Read Cycle Control - II** The read cycle control for requests from either CPU or upstream masters to DRAM controller. 0: Several T faster 1: 2T slower This bit works with other registers (Rx54[3] and Rx90[1:0]) in different conditions for the DRAM read cycle.
0	RO	0	**Reserved**

Offset Address: 56h (D0F2)

Write Policy 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0h	**Medium Threshold for Write Retire Policy** These registers indicate the request count in the write queue as the medium threshold for flushing write. They work with Rx55[2] for extra write retire policy for CPU or upstream memory write cycles to DRAM controller. Please refer to Rx52[1] for details. 0000: 1 write request 0001: 2 write requests … 1011: 12 write requests Others: Reserved
3	RW	0	**Reserved**
2	RW	0	**Upstream Request 3T Rate** Request queuing rate for host controller to accept upstream requests from PCIe devices or other master devices (i.e. SATA, USB ..) 0: Disabled, 2T request rate. 1: Enabled, 3T request rate.
1	RW	0	**Flushing Write Requests when GFX's Requests Hit Any of the Requests in the Write Queue** 0: Disable 1: Enable
0	RW	0	**High Priority Upstream Requests** Enabling of this bit gives higher priority to the upstream cycles when host controller arbitrates in between CPU and upstream cycles for obtaining the CPU bus. The priority of the requests also depends on the priority setting of each master devices. i.e. Even with this bit being enabled, if the corresponding priority bit of the master device had not been set, the priority of the request won't be raised. 0: Disable 1: Enable Note: The high priority attribute comes with the request from the traffic controller module. Please refer to RCRB register sets Rx200~Rx255, Rx234[7] is an example of setting the priority to high for requests from conventional master devices in the SB.

Offset Address: 57h (D0F2)

Calibration Function **Default Value: 07h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0 ROMSIP	**CPU bus HREQ5 Support** Unlike Intel's P4, VIA's C7 series CPUs only have three HREQ pins, HREQ[2:0]#. By using 4X sampling, we have information on beat 1 of HREQ[2:0]# for HREQa[3]#, HREQa[4]# (which P4 had as pins) and HREQa[5]#. VIA's C7 source-2 CPU introduced to use the extra information – HREQa[5]# which indicates the processor may assert DBSY# for adding wait states at the data phase of the current write cycle. In this case, the fast TRDY feature (chipset accept the write data earlier, please refer to Rx96[3]) cannot work. Thus, the chipset must dynamically turn the fast TRDY function off when it detects HREQa[5]# is asserted. 0: Host controller will never activate the fast TRDY feature. 1: Host controller will detect the de-assertion of HREQa[5]# to activate the fast TRDY feature for the current downstream write cycles. Note: 1. This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the secondary QW, byte 5, bit[0] in the initialization ROM. 2. Fast TRDY feature is an enhanced protocol introduced since VIA's C7 source-1 CPU. This feature is also controlled by register Rx96[3]. For details on this feature, please refer to Table 5 (Rx57[1]) below.

Table 5. Rx57[1] Enabling of fast TRDY feature

VIA C7 CPU	Rx57[0]	Rx96[3]	Fast TRDY Feature	Comment
Source-1	0	-	off	
	1	0	off	
	1	1	n/a	Invalid setting, system cannot work normally.
Source-2	0	-	off	
	1	0	off	
	1	1	on	Host controller will detect the status of HREQa[5]# to enable the fast TRDY feature

Offset Address: 58h (D0F2) – Reserved

Offset Address: 59h (D0F2)

CPU Miscellaneous Control 1 **Default Value: 08h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	0	**Warm CPU Reset (CPURST#) Duration Control** These two bits define the active duration of the CPURST# when Rx59[3] is programmed to 1. 00: 475ns 01: 1050ns 10: 1425ns 11: 1905ns
3	RW	1b	**Warm CPU Reset (CPURST#) Trigger** A 0 to 1 transition of this bit will trigger warm reset, i.e. CPURST# will be driven low for a certain period of time defined in Rx59[5:4]. Firmware will have to write this bit to “0” before write “1” to trigger another CPURST#.
2	RW	0	**CPU to DRAM Access control** Host controller will delay 1T for CPU to DRAM access. 0: Disable 1: Enable
1	RO	0	**Reserved**
0	RW	0	**MSI Cycle IPI (Inter-Processor Interrupt) Flat Model Support** While working with multiple CPUs, the host controller can take the Message Interrupt cycle (downstream from one CPU) and re-direct that Message Interrupt cycle to the local APIC controller in CPU cores with least task priority. The address bit AHa[3:2]# of this coming in MSI cycle equals to 11b. 0: Disable 1: Enable

Offset Address: 5A-5Bh (D0F2) – Reserved

Offset Address: 5Ch (D0F2)

CPU Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Data Bit 11 Mask for Redirected MSI Cycle** Used for the IPI (Inter-Processor Interrupt) support, the chipset takes the MSI cycle (downstream cycle from one CPU) whose redirection hint bit (address bit Aha[3]#) is set to 1 and redirect that MSI cycle to proper CPU cores. Rx59[0] is the enable bit for the IPI support. However, for proper operation, this bit should always be set to 1. 0: Data bit[11] of the redirected MSI cycle uses the data bit[11] from CPU. 1: Data bit[11] of the redirected MSI cycle is 1.
3:0	RW	0	**Reserved**

Offset Address: 5Dh (D0F2)

Write Policy 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**High Threshold for Write Retire Policy** These registers indicate the request count in the write queue as the high threshold for flushing write. They work with Rx52[3] for write retire policy for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 4 (Rx52[1]) for details. 0000: 1 write request 0001: 2 write requests … 1011: 12 write requests Others: Reserved
3:0	RW	0	**Low Threshold for Write Retire Policy** These registers indicate the request count in the write queue as the low threshold for flushing write. They work with Rx52[3] for write retire policy for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 4 (Rx52[1]) for details. 0000: 1 write request 0001: 2 write requests … 1011: 12 write requests Others: Reserved

Offset Address: 5Eh (D0F2)

Bandwidth Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0h	**Preset Value For Host Bandwidth Counter** The Host Bandwidth Counter is used to direct this chip to a period called HOSTBW period when Rx5F[2]) is 1. In this HOSTBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 6 (Rx5E[1]) for details. The counter is loaded with the programmed value after the reset or when the chip is going to enter the DRAMBW period (please refer to Rx5E[3:0]). The counter decreases by one whenever a non-DRAM cycle is issued by the CPU. Before the counter counts down to zero, if there is a cycle targeted to DRAM coming in, the counter will also be reloaded. Working with DRAM Bandwidth counter (Rx5E[3:0]), when the counter counts down to zero, it gives an indication that the past several cycles are not targeted to DRAM. The chip enters the HOSTBW period to handle the write cycles to DRAM in an appropriate way. Basically, under normal operation, the chip should be running in between HOSTBW and DRAMBW period. Thus, the write policy to DRAM is changing dynamically. 0000: immediately. It means the chip is always running at HOSTBW period. 0001: If 1 CPU cycle not targeted to DRAM comes, the chip goes into HOSTBW period. 0010: If 2 consecutive CPU cycles not targeted to DRAM come, the chip goes into HOSTBW period. … 1111: If 15 consecutive CPU cycles not targeted to DRAM come, the chip goes into HOSTBW period.
3:0	RW	0	**Preset Value For DRAM Bandwidth Counter** The DRAM Bandwidth Counter is used to direct this chip to a period called DRAMBW period when Rx5F[1] is 1. In this DRAMBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 6 (Rx5E[1]) for details. The counter is loaded with the programmed value after the reset or when the chip is going to enter the HOSTBW period (please refer to Rx5E[7:4]). The counter decreases by one whenever a DRAM cycle is issued by CPU or other masters (upstream cycles go through CPU bus too). Before the counter is counted down to zero, if there is cycle not targeted to DRAM coming in, the counter will also be reloaded. Working with HOST Bandwidth counter (Rx5E[7:4]), when the counter counts down to zero, it gives an indication that the past several cycles are all targeted to DRAM. The chip enters the DRAMBW period to handle the write cycles to DRAM in an appropriate way. Basically, under normal operation, the chip should be running in between HOSTBW and DRAMBW period. Thus, the write policy to DRAM is changing dynamically. 0000: immediately. It means the chip is always running at DRAMBW period. 0001: If 1 CPU cycle targeted to DRAM comes, the chip goes into DRAMBW period. 0010: If 2 consecutive CPU cycles targeted to DRAM come, the chip goes into DRAMBW period. … 1111: If 15 consecutive CPU cycles targeted to DRAM come, the chip goes into DRAMBW period.

Table 6. Rx5E[1] DRAM Write Retire Policy Adjustments in HOSTBW Period and DRAMBW Period.

HOSTBW Period	DRAMBW Period	DRAM write policy adjustments* besides those shown in Table 4 (Rx52[1])
0	0	When the chip is in neither HOSTBW period nor DRAMBW period (Rx5F[2] =0 and Rx5F[1] =0), the write to DRAM policy followed what Table 4 (Rx52[1]) described.
1	0	This case happened when Host Bandwidth Period (Rx5F[2]) is 1 and Host Bandwidth counter (Rx5E[7:4]) counted down to zero; The DRAM write policy described in table Rx52[1] will be adjusted to: a. When the DRAM bus is idle, as long as there is write request queued, as described in Table 4 (Rx52[1]), the host controller should flush the write right away. However, in this case, the host controller won't start the DRAM write unless there is no DRAM read from the CPU or upstream masters in the coming up consecutive 8T. i.e. the host controller will delay 8T to make decision of flushing the writes out. Within this 8T, if there is any DRAM read cycle comes in, the host controller won't flush the write. b. When the DRAM bus is not idle, and when the write requests in the write queue accumulated over the high (or medium, when Rx55[2] = 1) threshold, as described in Table 4 (Rx52[1]), the host controller should flush the write. However, in this case, if there is DRAM read coming in from the CPU or upstream masters, it won't start the DRAM write unless the write queue is currently full.
0	1	This case happened when DRAM Bandwidth period (Rx5F[1]) is 1 and DRAM Bandwidth counter (Rx5E[3:0]) counted down to zero; The DRAM write policy described in table Rx52[1] will be adjusted to: a. When the DRAM bus is idle, as long as there is write request queued, as described in Table 4 (Rx52[1]), the host controller should flush the write right away. However, in this case, the host controller won't start the DRAM write unless there is no DRAM read from the CPU or upstream masters at the current moment. i.e. the host controller will start to flush the write as long as there is no DRAM read request coming in. b. When the DRAM bus is not idle, and when the write requests in the write queue accumulated over the high (or medium, when RX55[2], ROPTWEN = 1) threshold, as described in table RX52.1, the host controller should flush the write. However, in this case, if there is DRAM read coming in from the CPU or upstream masters, it won't start the DRAM write unless the write queue is currently full. (This b operating condition is the same as that described in last row, case b of HOSTBW period =1.)
1	1	This case only happened when 1. Both Host Bandwidth period (RX5F[2]) and DRAM Bandwidth period (RX5F[1]) are enabled and 2. The Host bandwidth counter (RX5E[7:4]) and the DRAM bandwidth counter (RX5E[3:0]) are both programmed to 00h. In a normal operation, such programming (2. above) is abnormal. Even so, the DRAM write policy described in table RX52.1 will be adjusted to: a. As described in table RX52.1, no matter whether there is DRAM read coming in or not, the host controller won't issue write until the write requests accumulated over the high (or medium) threshold. In this case, if there is no DRAM read request coming in, host controller will flush the write requests as long as it accumulated the write requests to two. b. As described in table RX52.1, the host controller won't issue write until the write requests accumulated over the high (or medium) threshold. In this case, if any one of the writes in the write queue has the same memory page as the one on processing to DRAM controller, the host controller will start flush the write out to DRAM controller even that the write request number in the write queue is only larger than the low threshold.

Note: These adjustments only apply to the third and fourth rows in
Table 4 (Rx52[1]), where the Rx51[6] and Rx52[3] are both 1.

A typical HOSTBW and DRAMBW operating behavior is as shown in figure Rx5E[1] below. During HOSTBW period and DRAMBW period, the DRAM write retire policy will be a slight different. Please refer to the case a on the second row (HOSTBW=1) and third row (DRAMBW =1) in

Table 6 (Rx5E[1]) above. Summarily, when DRAM bus is idle, during HOSTBW period, we do give host side a little bit more time (8T) to see if there is DRAM read needed to be serviced before we serve the DRAM write. i.e. During HOSTBW period, the chip gives DRAM read cycle more priority. When DRAM bus is not idle, during these two periods, the chip gives DRAM read cycle the highest priority, those DRAM write cycles only can be flushed out when the write queue is full.

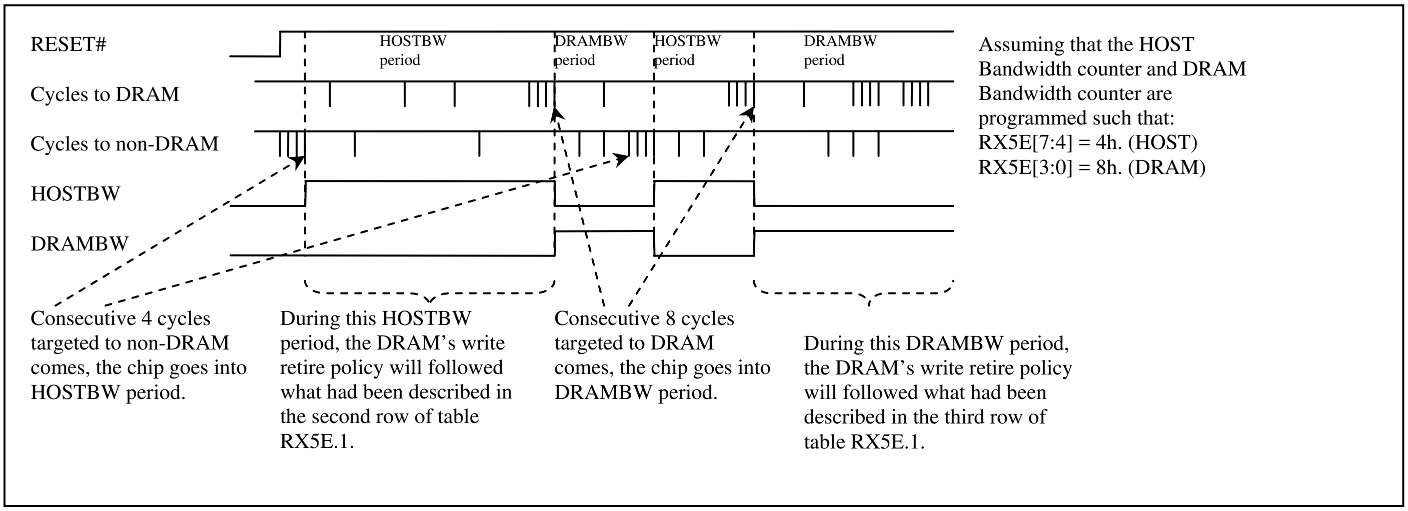


Figure 1. Rx5E[1] An Typical Behavior of HOSTBW and DRAMBW When Rx5F[2:1] are both programmed to 1

Offset Address: 5Fh (D0F2)

CPU Miscellaneous Control 3 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RO	1b	**Reserved (Do Not Program)**
6	RW	0	**Enable Reorder Retry Queue** For CPU downstream cycles, this chip handled the retried cycles in a different fashion. 0: Retried CPU transactions always complete in order. 1: Allow the second retried transaction to complete before the previous retried transaction. Note that this chip has only two levels of retry queue for the transactions on the CPU bus.
5:3	RO	0	**Reserved**
2	RW	0	**Host Bandwidth Period** This bit works with Host Bandwidth Counter, Rx5E[7:4]. In the HOSTBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 6 (Rx5E[1]). 0: Disabled, the chip will never go to HOSTBW period. 1: Enabled, the chip will go to HOSTBW period when Host Bandwidth Counter is counted down to zero.
1	RW	0	**DRAM Bandwidth Period** This bit works with DRAM Bandwidth Counter, Rx5E[3:0]. In the DRAMBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 6 (Rx5E[1]). 0: Disabled, the chip will never go to DRAMBW period. 1: Enabled, the chip will go to DRAMBW period when the DRAM Bandwidth Counter is counted down to zero.
0	RO	0	**Reserved**

Host Controller to DRAMC Read Cycle Interface (DRDY) Timing Control (60-6Fh)

Offset Address: 60h (D0F2)
DRDY Timing Control 1 for Read Line Access **Default Value: 00h**

These bits must be programmed to certain value at different cases.

Bit	Attribute	Default	Description
7:6	RW	0	**DRDY Timing Control of the first data cycle in a line access - 4**
5:4	RW	0	**DRDY Timing Control of the first data cycle in a line access - 3**
3:2	RW	0	**DRDY Timing Control of the first data cycle in a line access - 2**
1:0	RW	0	**DRDY Timing Control of the first data cycle in a line access - 1**

Offset Address: 61h (D0F2)
DRDY Timing Control 2 for Read Line Access **Default Value: 00h**

These bits must be programmed to certain value at different cases.

Bit	Attribute	Default	Description
7:6	RW	0	**DRDY Timing Control of the first data cycle in a line access - 8**
5:4	RW	0	**DRDY Timing Control of the first data cycle in a line access - 7**
3:2	RW	0	**DRDY Timing Control of the first data cycle in a line access - 6**
1:0	RW	0	**DRDY Timing Control of the first data cycle in a line access - 5**

Offset Address: 62h (D0F2) - Reserved

Offset Address: 63h (D0F2)
DRDY Timing Control 1 for Read Quad-Word (QW) Access **Default Value: 00h**

These bits must be programmed to certain value at different cases.

Bit	Attribute	Default	Description
7:6	RW	0	**DRDY Timing Control of Single QW Cycle - 4**
5:4	RW	0	**DRDY Timing Control of Single QW Cycle - 3**
3:2	RW	0	**DRDY Timing Control of Single QW Cycle - 2**
1:0	RW	0	**DRDY Timing Control of Single QW Cycle - 1**

Offset Address: 64h (D0F2)
DRDY Timing Control 2 for Read QW Access **Default Value: 00h**

These bits must be programmed to certain value at different cases.

Bit	Attribute	Default	Description
7:6	RW	0	**DRDY Timing Control of Single QW Cycle - 8**
5:4	RW	0	**DRDY Timing Control of Single QW Cycle - 7**
3:2	RW	0	**DRDY Timing Control of Single QW Cycle - 6**
1:0	RW	0	**DRDY Timing Control of Single QW Cycle - 5**

Offset Address: 65h (D0F2) - Reserved

Offset Address: 66h (D0F2)
Burst DRDY Timing Control of the Second Data Cycle in a Line Access 1 **Default Value: 00h**

These bits must be programmed to certain value at different cases.

Bit	Attribute	Default	Description
7	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 8**
6	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 7**
5	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 6**
4	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 5**
3	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 4**
2	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 3**
1	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 2**
0	RW	0	**DRDY Timing Control of the Second Data Cycle in a Line Access - 1**

Offset Address: 67h (D0F2) - Reserved

Offset Address: 68h (D0F2)

Logical APIC ID of local APIC #0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 00h.** The value is updated when the host controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_0qq0h. This register will be updated with qqh.

Note: HAa#, HAb#, HREQa# and HREQb# refer to the different packages (a and b) of HA# and HREQ# pins.

Offset Address: 69h (D0F2)

Logical APIC ID of local APIC #1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 01h.** Same as Rx68, with exception to HAa# = FEE0_1qq0h.

Offset Address: 6Ah (D0F2)

Logical APIC ID of local APIC #2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 02h.** Same as Rx68, with exception to HAa# = FEE0_2qq0h.

Offset Address: 6Bh (D0F2)

Logical APIC ID of local APIC #3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 03h.** Same as Rx68, with exception to HAa# = FEE0_3qq0h.

Offset Address: 6Ch (D0F2)

Logical APIC ID of local APIC #4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 04h.** Same as Rx68, with exception to HAa# = FEE0_4qq0h.

Offset Address: 6Dh (D0F2)

Logical APIC ID of local APIC #5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 05h.** Same as Rx68, with exception to HAa# = FEE0_5qq0h.

Offset Address: 6Eh (D0F2)

Logical APIC ID of local APIC #6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 06h.** Same as Rx68, with exception to HAa# = FEE0_6qq0h.

Offset Address: 6Fh (D0F2)

Logical APIC ID of local APIC #7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Logical APIC ID of APIC which has physical local APIC ID = 07h.** Same as Rx68, with exception to HAa# = FEE0_7qq0h.

Host AGTL+ I/O Circuit (70–8Fh)

Offset Address: 70h (D0F2)

Host Address Pad Pull-up Resistance Control – Manual Mode **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Manual setting on compensating output impedance (PMOS part) of output driver for strobe signals of address/request group (HADSTB0P#, HADSTB0N#)**
3:0	RW	1000b ROMSIP	**Manual setting on compensating output impedance (PMOS part)of output driver for HAHI[0], HA [16:3] #, HREQ [2:0] #, HABI# of address/request group**

Offset Address: 71h (D0F2)

Host Address Pad Pull-down Resistance Control – Manual Mode **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Manual setting on compensating output impedance (NMOS part) of output driver for strobe signals of address/request group (HADSTB0P#, HADSTB0N#)**
3:0	RW	1000b ROMSIP	**Manual setting on compensating output impedance (NMOS part) of output driver for HAHI[0], HA[16:3] #, HREQ[2:0] #, HABI# of address/request group**

Offset Address: 72h (D0F2)

Host Data Pad Pull-up Resistance Control – Manual Mode **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Manual Setting on Compensating Output Impedance (PMOS part) of Output Driver for Strobe Signals of Data Group (HDSTB[3:0]P#, HDSTB [3:0] N#)**
3:0	RW	1000b ROMSIP	**Manual Setting on Compensating Output Impedance (PMOS part) of Output Driver for HD[63:0] #, HDBI[3:0]# of Data Group**

Offset Address: 73h (D0F2)

Host Data Pad Pull-down Resistance Control – Manual Mode **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Manual Setting on Compensating Output Impedance (NMOS part) of Output Driver for Strobe Signals of Data Group (HDSTB[3:0]P#, HDSTB [3:0]N#)**
3:0	RW	1000b ROMSIP	**Manual Setting on Compensating Output Impedance (NMOS part) of Output Driver for HD[63:0]#, HDBI[3:0]# of Data Group**

Offset Address: 74-75h (D0F2) - Reserved

Offset Address: 76h (D0F2)
AGTL+ I/O Configuration **Default Value: 0nh**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Power Down Input Comparators of AGTL+ IO Buffers When Entering S3 State (Suspend to DRAM State)** 0: Disable 1: Enable
2	RO	1b	**Reserved (Do Not Program)**
1	RW	0 ROMSIP	**DBI Function on the Host Bus** HDBI[3:0]# are valid only when the HD[63:0]# are valid. When HDBI[3:0]# are low, it indicates the data bits of the corresponding data group are inverted. The HDBI[3:0]# and the data bus group are related as: HDBI3# goes with HD[63:48]# ; HDBI2# goes with HD[47:32]#; HDBI1# goes with HD[31:16]#; HDBI0# goes with HD[15:0]# 0: Enabled, when this chip is in output mode, HDBI[3:0]# will be driven low to indicate that the data bits are inverted on the corresponding data bus group. 1: Disabled, when this chip is in output mode, HDBI[3:0]# will always stay at high. Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the first QW, byte3, bit[7] in the initialization ROM.
0	RW	0 ROMSIP	**DBI Functional Mode** This register bit defined the generation method of HDBI[3:0]#. 0: DBI signals HDBI[3:0]# are generated to minimize the number of changes on the data bits. i.e. The HDBI[3:0]# are asserted if the number of data bits changed (0->1 or 1-> 0) on its corresponding data group from the previous clock cycle to the current clock cycle are equal to or greater than 8. 1: DBI signals HDBI[3:0]# are generated to minimize the AGTL+ pull down count. i.e. The HDBI[3:0]# are asserted if the number of “low” on the data bits on its corresponding data group for the current clock cycle are equal to or greater than 8. Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the first QW, byte3, bit[6] in the initialization ROM.

Offset Address: 77-79h (D0F2) – Reserved

Offset Address: 7Ah (D0F2)
AGTL Compensation Status **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Auto-Compensation Mode** Auto compensation mode for those pull up and pull down setting for high speed AGTL+ I/O control. These I/O are HADSTB0N#, HADSTB0#, HADSTB1#, HA[32:3]#, HREQ[2:0]#, HDSTB[3:0]N#, HDSTB[3:0]P#, HD[63:0]#, and HDBI[3:0]#. 0: Disable auto mode 1: Enable auto mode Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#.
6:0	RO	0	**Reserved**

Offset Address: 7B-8Fh (D0F2) – Reserved

Miscellaneous Control (90–9Eh)

Offset Address: 90h (D0F2)
Miscellaneous Control 1 **Default Value: 08h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RO	1b	**Reserved (Do Not Program)**
2	RW	0	**Reserved**
1:0	RW	00b	**Host Controller to DRAM Read Cycle Control - III** 00: 2T faster 01: 3T faster 10: 4T faster 11: 5T faster Note: These bits work with Rx54[3] and Rx55[1] for different CPU to DRAM read cycle timing.

Offset Address: 91Fh (D0F2) – Reserved

Offset Address: 92h (D0F2)
ACPI IO Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**C2,C3,C4,C5 Command Address Decoding** If the request address [15:5] equals to RPMIOBA[15:5] **Byte-enable bit** / **Value** / **Power level** 4 / 1b / LVL2 5 / 1b / LVL3 6 / 1b / LVL4 7 / 1b / LVL5 0 / 1b / LVL6

Offset Address: 93h (D0F2)
ACPI IO Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**C2,C3,C4,C5 Command Address Decoding** If the request address [15:5] equals to RPMIOBA[15:5] **Byte-enable bit** / **Value** / **Power level** 4 / 1b / LVL2 5 / 1b / LVL3 6 / 1b / LVL4 7 / 1b / LVL5 0 / 1b / LVL6

Offset Address: 94-95h (D0F2) - Reserved

Offset Address: 96h (D0F2)
Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**V4 Bus Fast TRDY** VIA's C7/Nano series CPUs have a fast TRDY feature which has higher throughput for CPU downstream write cycles. This enhanced protocol basically allowed chipset to assert TRDY at a faster rate. Besides this register bit, Rx57[0] must also be set to let the feature work. Please refer to table Table 5 (Rx57[1]) for details. 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	0	**HDPWR# Assertion Enable** HDPWR# is connected to VIA's C7/Nano series CPU. When it is asserted, the chipset tells the CPU to provide power to the HD (host data) bus. When it is de-asserted, the CPU can shut down the power of the HD bus. 0: HDPWR# is always asserted by this chip. 1: HDPWR# is dynamically asserted by this chip. With this feature, VIA's C7/Nano series CPU can dynamically shut off the power of HD I/O when there is no data transfer. It gives better CPU power saving.
0	RW	0	**HDPWR# Assertion Policy** This bit only works when Rx96[1] is 1. 0: The chip asserts HDPWR# at the data phase for a.) CPU downstream read cycles, b.) Upstream APIC write cycles, and c.) CPU downstream write cycles (including snoop write back data phase of upstream DRAM read and write cycles). 1: The chip asserts HDPWR# at the data phase for a.) CPU downstream read cycles, and b.) Upstream APIC write cycles. This one gives more power saving.

Offset Address: 97h (D0F2)
APIC Related Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Redirect Lowest Priority MSI Requests to APIC with Physical ID = 00h** For supporting the IPI cycle (Inter-Processor Interrupt), the chip is able to redirect the coming in MSI cycle to the CPU with least task priority. Please refer to Rx59[0] for details. This register always redirects the IPI cycle to the CPU with APIC physical ID = 00h (i.e. CPU0 is treated as the lowest priority processor). 0: Disable 1: Enable.

Offset Address: 98h (D0F2)
Miscellaneous Control 3 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Control if DEFRQ accept a new C2P read request if there exists a C2P read request with "RETRY" flag in it** 0: DEFRQ can accept a new C2P read request if there exists a C2P read request with "RETRY" flag in it 1: DEFRQ will not accept a new C2P read request if there exists a C2P read request with "RETRY" flag in it.
6	RW	0	**Snoop Disable Selection** C5 state trigger condition 0: CPU send special cycle enable/disable C5 state 1: CPU read level 5 and then the STPGNT for lvl5 read request send to NM Suggestion: always set to 1b.
5	RO	0	**Reserved**
4:1	RW	0	**Reserved**
0	RW	0	**Enable Host Do P2C Cycle Redirection When C5 State** 0: Disable 1: Enable Suggestion: always set to 1b.

Offset Address: 99h (D0F2)
Miscellaneous Control 4 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**MSI Redirect** 0: Discard MSI cycle in C5 state if SM can not hold the MSI cycle in this state 1: Send MSI cycle to CPU in C5 state if SM can not hold the MSI cycle in this state
2	RW	0	**Snoop Sync Selection** 0: Finish redirect after 3T GCLK of SLP # de-asserted 1: Finish redirect after 6T GCLK of SLP# de-asserted.
1	RW	0	**Dynamic Fast TRDY** 0: Not implement dynamic fast TRDY by observing if there is pipeline ADS outstanding 1: Implement dynamic fast TRDY by observing if there is pipeline ADS outstanding
0	RW	0	**Reserved**

Offset Address: 9A-9Eh (D0F2) – Reserved

GTLPHY Control (A0–FFh)

Offset Address: A0h (D0F2)

GTLPHY Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0 ROMSIP	**Enable Faster Slew Rate Control of N-driver** 0: Disable 1: Enable
0	RW	0 ROMSIP	**Enable Faster Slew Rate Control of P-driver** 0: Disable 1: Enable

Offset Address: A1h (D0F2)

GTLPHY Control 2 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Manual Setting on Compensating Output Impedance (NMOS Part) of Output Driver for Source-synchronous 1X Signals in V4 Bus**
3:0	RW	1000b ROMSIP	**Manual Setting on Compensating Output Impedance (PMOS Part) of Output Driver for Source-synchronous 1X Signals in V4 Bus**

Offset Address: A2h (D0F2)

GTLPHY Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto Setting on Compensating Output Impedance (NMOS part) of HA/HASTB/HD/HDSTB/bdgtl1xd All Use this Value**
3:0	RO	0	**Auto Setting on Compensating Output Impedance (PMOS part) of HA/HASTB/HD/HDSTB/bdgtl1xd All Use this Value**

Offset Address: A3h (D0F2)

GTLPHY Control (HADSTB0P#/HADSTB0N#) **Default Value: 70h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Setting of Adjusting Output Delay of HADSTB0P#/HADSTB0N#** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:2	RW	0	**Reserved**
1	RW	0 ROMSIP	**Hot Conversion Circuits Mode Control** Select Pseudo Synchronous Mode or Asynchronous Mode 0: Pseudo Synchronous Mode 1: Asynchronous Mode
0	RW	0 ROMSIP	**Enable Schmitt Trigger at Input Comparator** In case there is a voltage dip below VREF 0: Disable 1: Enable

Offset Address: A4h (D0F2)

GTLPHY Control (HAHI[0], HA[16:3]#, HREQ[2:0]#, HABI#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 1** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 0** Same as bits[7:4].

Offset Address: A5h (D0F2)

GTLPHY Control (HAHI[0], HA[16:3]#, HREQ[2:0]#, HABI#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 3** Same as RxA4[7:4].
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 2** Same as RxA4[7:4].

Offset Address: A6h (D0F2)
GTLPHY Control (HADSTB0P#/HADSTB0N#) **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0111b ROMSIP	**Manual Setting on Adjusting Input Delay of HADSTB0P#/HADSTB0N#** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)

Offset Address: A7h (D0F2)
GTLPHY Control (HAHI[0], HA[16:3]#, HREQ[2:0]#, HABI#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 1** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 0** Same as bits[7:4].

Offset Address: A8h (D0F2)
GTLPHY Control (HAHI[0], HA[16:3]#, HREQ[2:0]#, HABI#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 3** Same as RxA7[7:4].
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 2** Same as RxA7[7:4].

Offset Address: A9h (D0F2)
GTLPHY Control 3 **Default Value: 07h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Enable IO Loopback Test** (Signal transmitted through output buffer circuit will be directly looped back to input driver of IO buffer) 0: Disable 1: Enable
3:2	RW	01b ROMSIP	**Threshold Setting of Digital Low Pass Filter for Jitter Reduction in DLL Process** 00: 3 steps 01: 4 steps 10: 5 steps 11: 6 steps
1	RW	1b ROMSIP	**The result obtained from auto de-skewing circuit can be used in transmit path**. Otherwise, manual setting will be: 0: Use manual setting 1: Use the result obtained from auto de-skewing circuit
0	RW	1b ROMSIP	**The result obtained from auto de-skewing circuit can be used in receive path**. Otherwise, manual setting will be: 0: Use manual setting 1: Use the result obtained from auto de-skewing circuit

Offset Address: AAh (D0F2)
GTLPHY Control (HDSTB[1:0]P#/HDSTB[1:0]N#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Setting on Adjusting Output Delay of HDSTB1P#/HDSTB1N#** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Manual Setting on Adjusting Output Delay of HDSTB0P#/HDSTB0N#** Same as bits[7:4].

Offset Address: ABh (D0F2)
GTLPHY Control (HDSTB[3:2]P#/HDSTB[3:2]N#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Setting on Adjusting Output Delay of HDSTB3P#/HDSTB3N#** Same as RxAB[7:4].
3:0	RW	0111b ROMSIP	**Manual Setting on Adjusting Output Delay of HDSTB2P#/HDSTB2N#** Same as RxAB[7:4].

Offset Address: ACh (D0F2)

GTLPHY Control (HD[15:0]#, HDBI[0]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 1** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 0** Same as bits[7:4].

Offset Address: ADh (D0F2)

GTLPHY Control (HD[15:0]#, HDBI[0]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 3** Same as RxAC[7:4].
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 2** Same as RxAC[7:4].

Offset Address: AEh (D0F2)

GTLPHY Control (HD[31:16]#, HDBI[1]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 1** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 0** Same as bits[7:4].

Offset Address: AFh (D0F2)

GTLPHY Control (HD[31:16]#, HDBI[1]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 3** Same as RxAE[7:4].
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 2** Same as RxAE[7:4].

Offset Address: B0h (D0F2)

GTLPHY Control (HD[47:32]#, HDBI[2]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 1** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 0** Same as bits[7:4].

Offset Address: B1h (D0F2)

GTLPHY Control (HD[47:32]#, HDBI[2]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 3** Same as RxB0[7:4].
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 2** Same as RxB0[7:4].

Offset Address: B2h (D0F2)
GTLPHY Control (HD[63:48]#, HDBI[3]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 1** Driven through IO buffer to the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 0** Same as bits[7:4].

Offset Address: B3h (D0F2)
GTLPHY Control (HD[63:48]#, HDBI[3]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Output Delay of Group 3** Same as RxB2[7:4].
3:0	RW	0111b ROMSIP	**Adjust Output Delay of Group 2** Same as RxB2[7:4].

Offset Address: B4h (D0F2)
GTLPHY Control (HDSTB[1:0]P#/HDSTB[1:0]N#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Setting on Adjusting Input Delay of HDSTB1P#/HDSTB1N#** Driven through IO buffer from the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Manual Setting on Adjusting Input Delay of HDSTB0P#/HDSTB0N#** Same as bits[7:4].

Offset Address: B5h (D0F2)
GTLPHY Control (HDSTB[3:2]P#/HDSTB[3:2]N#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Setting on Adjusting Input Delay of HDSTB3P#/HDSTB3N#** Same as RxB4[7:4].
3:0	RW	0111b ROMSIP	**Manual Setting on Adjusting Input Delay of HDSTB2P#/HDSTB2N#** Same as RxB4[7:4].

Offset Address: B6h (D0F2)
GTLPHY Control (HD[15:0]#, HDBI[0]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 1** Driven through IO buffer from the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 0** Same as bits[7:4].

Offset Address: B7h (D0F2)
GTLPHY Control (HD[15:0]#, HDBI[0]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 3** Same as RxB6[7:4].
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 2** Same as RxB6[7:4].

Offset Address: B8h (D0F2)

GTLPHY Control (HD[31:16]#, HDBI[1]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 1** Driven through IO buffer from the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 0** Same as bits[7:4].

Offset Address: B9h (D0F2)

GTLPHY Control (HD[31:16]#, HDBI[1]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 3** Same as RxB8[7:4].
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 2** Same as RxB8[7:4].

Offset Address: BAh (D0F2)

GTLPHY Control (HD[47:32]#, HDBI[2]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 1** Driven through IO buffer from the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 0** Same as bits[7:4].

Offset Address: BBh (D0F2)

GTLPHY Control (HD[47:32]#, HDBI[2]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 3** Same as RxBA[7:4].
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 2** Same as RxBA[7:4].

Offset Address: BCh (D0F2)

GTLPHY Control (HD[63:48]#, HDBI[3]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 1** Driven through IO buffer from the host bus (25ps per step, 16 steps as total, reaching maximum latency of 400ps)
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 0** Same as bits[7:4].

Offset Address: BDh (D0F2)

GTLPHY Control (HD[63:48]#, HDBI[3]#) **Default Value: 77h**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Adjust Input Delay of Group 3** Same as RxBC[7:4].
3:0	RW	0111b ROMSIP	**Adjust Input Delay of Group 2** Same as RxBC[7:4].

Offset Address: BEh (D0F2)

GTLPHY Control 29 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0 ROMSIP	**PVT (Process, voltage, temperature) compensation scheme on output impedance of output driver of AGTL+ IO buffers is operated either in** 0: Single-shot mode 1: Continuous-updated mode
3:2	RW	11b ROMSIP	**Medium threshold of digital low pass filter to update the counter values only when the identical number of consecutive sample values reaches this medium threshold** 00: 1 01: 2 10: 3 11: 4
1	RW	0 ROMSIP	**Operating Mode of Generating Address Bus Inversion Bits** 0: Minimize switches on address bus 1: Minimize the number of signals on address bus driven low
0	RW	1b ROMSIP	**Enable Function of Address Bus Inversion** 0: Disable address bus inversion(ABI# always pull-up high in V4 bus) 1: Enable address bus inversion

Offset Address: BFh (D0F2) – Reserved

Offset Address: C0h (D0F2)

GTLPHY Control 4 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HAO_DCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0 ROMSIP	**Clock Skew of GTLPHY** **Bit[6] Bit[3]** 0 0 1.0V GTLPHT clock tree 0 1 0.9V GTLPHT clock tree 1 0 1.2V GTLPHT clock tree
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HAO_DCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0b ROMSIP	**Clock Skew of GTLPHY** See bit [6] for details.
2:0	RW	000b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HAO_DCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C1h (D0F2)

GTLPHY Control 5 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HAO_SCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HAO_SCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HAO_SCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C2h (D0F2)
GTLPHY Control 6 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD0O_DCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0 ROMSIP	**Enable Host Support Dynamic FSB Protocol** 0: Disable 1: Enable
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HD0O_DCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HD0O_DCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C3h (D0F2)
GTLPHY Control 7 **Default Value: 84h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD0O_SCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HD0O_SCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	100b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HD0O_SCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C4h (D0F2)
GTLPHY Control 8 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD1O_DCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HD1O_DCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HD1O_DCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C5h (D0F2)

GTLPHY Control 9 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD1O_SCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HD1O_SCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HD1O_SCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C6h (D0F2)

GTLPHY Control 10 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD2O_DCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HD2O_DCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HD2O_DCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C7h (D0F2)

GTLPHY Control 11 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD2O_SCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HD2O_SCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual Setting on Adjusting Clock Delay of GTL_HD2O_SCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C8h (D0F2)

GTLPHY Control 12 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD3O_DCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on Adjusting Duty Cycle of GTL_HD3O_DCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual setting on adjusting clock delay of GTL_HD3O_DCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: C9h (D0F2)

GTLPHY Control 13 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**GTL_HD3O_SCK Bypasses DCC (Duty Control Corrector)** 0: Not bypass 1: Bypass
6	RW	0	**Reserved**
5:4	RW	00b ROMSIP	**Manual Setting on adjusting duty cycle of GTL_HD3O_SCK** 00: Positive cycle is increased by 40ps 01: Positive cycle is increased by 80ps 10: Positive cycle is reduced by 40ps 11: Positive cycle is reduced by 80ps
3	RW	0	**Reserved**
2:0	RW	000b ROMSIP	**Manual setting on adjusting clock delay of GTL_HD3O_SCK** 000: 60ps 001: 120ps 010: 180ps 011: 240ps 100: 300ps 101: 360ps 110: 420ps 111: 480ps

Offset Address: CA-CFh (D0F2) – Reserved

Offset Address: D0h (D0F2)

GTLPHY Control (HD[15:0]#, HDBI[0]#) **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 1** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0000b.
3:0	RO	0111b	**Auto De-skewing Result of Adjusting Input Delay of Group 0** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0111b.

Offset Address: D1h (D0F2)

GTLPHY Control (HD[15:0]#, HDBI[0]#) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 3** See RxD0[7:4] for details.
3:0	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 2** See RxD0[7:4] for details.

Offset Address: D2h (D0F2)
GTLPHY Control (HD[31:16]#, HDBI[1]#) **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 1** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0000b.
3:0	RO	0111b	**Auto De-skewing Result of Adjusting Input Delay of Group 0** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0111b.

Offset Address: D3h (D0F2)
GTLPHY Control (HD[31:16]#, HDBI[1]#) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 3** See RxD2[7:4] for details.
3:0	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 2** See RxD2[7:4] for details.

Offset Address: D4h (D0F2)
GTLPHY Control (HD[47:32]#, HDBI[2]#) **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 1** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0000b.
3:0	RO	0111b	**Auto De-skewing Result of Adjusting Input Delay of Group 0** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0111b.

Offset Address: D5h (D0F2)
GTLPHY Control (HD[47:32]#, HDBI[2]#) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 3** See RxD4[7:4] for details.
3:0	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 2** See RxD4[7:4] for details.

Offset Address: D6h (D0F2)
GTLPHY Control (HD[63:48]#, HDBI[3]#) **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 1** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0000b.
3:0	RO	0111b	**Auto De-skewing Result of Adjusting Input Delay of Group 0** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0111b.

Offset Address: D7h (D0F2)
GTLPHY Control (HD[63:48]#, HDBI[3]#) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 3** See RxD6[7:4] for details.
3:0	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 2** See RxD6[7:4] for details.

Offset Address: D8h (D0F2)

GTLPHY Control (HAHI[0], HA[16:3]#, HREQ[2:0]#, HABI#) **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 1** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0000b.
3:0	RO	0111b	**Auto De-skewing Result of Adjusting Input Delay of Group 0** Driven through IO buffer from the host bus ((min:typ:max) = (20ps:29ps:39ps) per step, 16 steps as total) When auto de-skew reset assert or auto de-skew not start, the default value is 0111b.

Offset Address: D9h (D0F2)

GTLPHY Control (HAHI[0], HA[16:3]#, HREQ[2:0]#, HABI#) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 3** See RxD8[7:4] for details.
3:0	RO	0	**Auto De-skewing Result of Adjusting Input Delay of Group 2** See RxD8[7:4] for details.

Offset Address: DA-FFh (D0F2) – Reserved

DEVICE 0 FUNCTION 3 (D0F3): DRAM BUS CONTROL

PCI Configuration Space

All registers in D0F3 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 3.
All Function 3, DRAM Controller, registers are implemented in Powell.

Header Registers (00–3Fh)

Offset Address: 01-00h (D0F3)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F3)
Device ID **Default Value: 3409h**

Bit	Attribute	Default	Description
15:0	RO	3409h	**Device ID**

Offset Address: 05-04h (D0F3)
PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F3)
PCI Status — **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RW1C	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus Master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F3)
Revision ID — **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F3)
Class Code — **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F3) – Reserved

Offset Address: 0Dh (D0F3)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F3)
Header Type — **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F3)
Built In Self Test (BIST) — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 10-2Bh (D0F3) – Reserved

Offset Address: 2D-2Ch (D0F3)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F3)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F3) – Reserved

Offset Address: 34h (D0F3)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer**

Offset Address: 35-3Fh (D0F3) – Reserved

DRAM Rank (Row) Ending / Beginning Address (40–4Fh)

Offset Address: 40h (D0F3)
DRAM Rank 0 Ending Address **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**Virtual Rank 0 Ending Address (HA[33:26])**

Offset Address: 41h (D0F3)
DRAM Rank 1 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 1 Ending Address (HA[33:26])**

Offset Address: 42h (D0F3)
DRAM Rank 2 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 2 Ending Address (HA[33:26])**

Offset Address: 43h (D0F3)
DRAM Rank 3 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 3 Ending Address (HA[33:26])**

Offset Address: 44-47h (D0F3) – Reserved

Offset Address: 48h (D0F3)
DRAM Rank 0 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 0 Beginning Address (HA[33:26])**

Offset Address: 49h (D0F3)
DRAM Rank 1 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 1 Beginning Address (HA[33:26])**

Offset Address: 4Ah (D0F3)
DRAM Rank 2 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 2 Beginning Address (HA[33:26])**

Offset Address: 4Bh (D0F3)
DRAM Rank 3 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 3 Beginning Address (HA[33:26])**

Offset Address: 4C-4Fh (D0F3) – Reserved

MA Map / Command Rate (50–53h)

Offset Address: 51-50h (D0F3)
DRAM MA Map Type **Default Value: 2222h**

Bit	Attribute	Default	Description
15:12	RW	2h	**Reserved (Do Not Program)**
11:8	RO	2h	**Reserved (Do Not Program)**
7:5	RW	001b	**Rank 0/1 MA Map Type** Refer to the “Rank MA Map Type” table below.
4	RW	0	**Reserved**
3:1	RW	001b	**Rank 2/3 MA Map Type** Refer to the “Rank MA Map Type” table below.
0	RW	0	**1T Command Rate** This bit should be set when Rx98[5] is 1b. 0: Disable (2T command) 1: 1T command

Table 7. Rank MA Map Type Table

Rank MA Map Type	000	001	010	011	100	101	110	111
Bank Address Bits	2	2	2	2	Rsvd	3	3	3
Row Address Bits	13-12	14-12	15-12	15-13		15-12	15-12	15-13
Column Address Bits	9	10	11	12		10	11	12
DRAM Size (Byte)	128M-64M	512M-128M	2G-256M	4G-1G		2G-256M	4G-512M	8G-2G

Offset Address: 52h (D0F3)
Bank Interleave Address Select **Default Value: 11h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	001b	**BA0 Address Select** Refer to the "DRAM Bank Address" table below for details.
3	RO	0	**Reserved**
2:0	RW	001b	**BA1 Address Select** Refer to the "DRAM Bank Address" table below for details.

Offset Address: 53h (D0F3)
Bank / Rank Interleave Address Select – Channel A **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**BA2 Support** Must be enabled if any 8-bank device exists. 0: Disable 1: Enable
6:4	RW	001b	**BA2 Address Select** Refer to the "DRAM Bank Address" table below for details.
3:2	RW	00b	**Rank Interleave Address Bit 1 (RA1) Select** Refer to the "DRAM Interleave Address" table below for details.
1:0	RW	00b	**Rank Interleave Address Bit 0 (RA0) Select** Refer to the "DRAM Interleave Address" table below for details.

Table 8. DRAM Bank Address Table

	000	001	010	011	100	101	110	111
Rx53[6:4] for BA2	A14	A15	A18	A19	Rsvd	rsvd	rsvd	rsvd
Rx52[2:0] for BA1	A12	A14	A16	A18	A20	rsvd	rsvd	rsvd
Rx52[6:4] for BA0	rsvd	A13	A15	A17	A19	rsvd	rsvd	rsvd

Table 9. Rank Interleave Address Table

	00	01	10	11
Rx53[3:2] for Rank Interleave Address Bit 1 (RA1)	A14	A16	A18	A20
Rx53[1:0] for Rank Interleave Address Bit 0 (RA0)	A15	A17	A19	A21

Notes:
1. Rank Interleave Address Bit 2 is fixed at A6.
2. BA2, BA1, BA0, INLV1, INLV0 should select 5 different address bits for Rx53[7] =1.
3. BA1, BA0, INLV1, INLV0 should select 4 different address bits for Rx53[7] =0.

Physical-to-Virtual Rank Mapping (54–57h)

Offset Address: 54h (D0F3)
Physical-to-Virtual Rank Mapping 1 **Default Value: 89h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Physical Rank 0** 0: Disable 1: Enable
6:4	RW	0	**Virtual Rank Number of Physical Rank 0**
3	RW	1b	**Enable Physical Rank 1** 0: Disable 1: Enable
2:0	RW	001b	**Virtual Rank Number of Physical Rank 1**

Offset Address: 55h (D0F3)
Physical-to-Virtual Rank Mapping 2 **Default Value: ABh**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Physical Rank 2** 0: Disable 1: Enable
6:4	RW	010b	**Virtual Rank Number of Physical Rank 2**
3	RW	1b	**Enable Physical Rank 3** 0: Disable 1: Enable
2:0	RW	011b	**Virtual Rank Number of Physical Rank 3**

Offset Address: 56-57h (D0F3) – Reserved

Virtual Rank Interleave Address Select / Enable (58–5Fh)

Offset Address: 58h (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #0 Interleave Address Select (RINLV0AS[2:0])** This 3-bit field determines the Rank Interleave Address of Rank #0. If RINLV0Asn is 1 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit of Rank 0 is 1, and vice versa.
3	RO	0	**Reserved**
2:0	RW	0	**Rank #0 Interleave Address Enable (RINLV0AEN[2:0])** 0: Disable 1: Enable This 3-bit field determines if the Rank Interleave Address of Rank #0 to be masked (used) or not. If RINLV0AENn is 0 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit will be masked (ignored), and vice versa.

Offset Address: 59h (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #1 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #1 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5Ah (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #2 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #2 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5Bh (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #3 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #3 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5C-5Fh (D0F3) – Reserved

2 Double-Sided DIMM Setting Example:

Following is an example, which shows a possible register setting for a system with 2 double-sided DIMM installed.

(1) Rx53[3:2] = 2 and Rx53[1:0] =2 selects A6, A18, A19 as the Rank Interleave Address for the system.

(2) If the settings on the Rank Interleave Address Selection of Rank 0, 1, 2, 3 (Rx58-5B[6:4]) are
Rx58[6:4] = 001b
Rx59[6:4] = 000b
Rx5A[6:4] = 010b
Rx5B[6:4] = 011b

And if the Rank Interleave Address Enable of Rank 0, 1, 2, 3 (Rx58-5B[2:0]) are
Rx58[2:0] = 011b
Rx59[2:0] = 011b
Rx5A[2:0] = 011b
Rx5B[2:0] = 011b

With the above register settings, Rank Interleave Address 2, A6, is ignored for the system, and the four ranks of the system are decided by A18 and A19 as shown in the following table.

A18	A19	Selected Rank
0	0	Rank#1
0	1	Rank#0
1	0	Rank#2
1	1	Rank#3

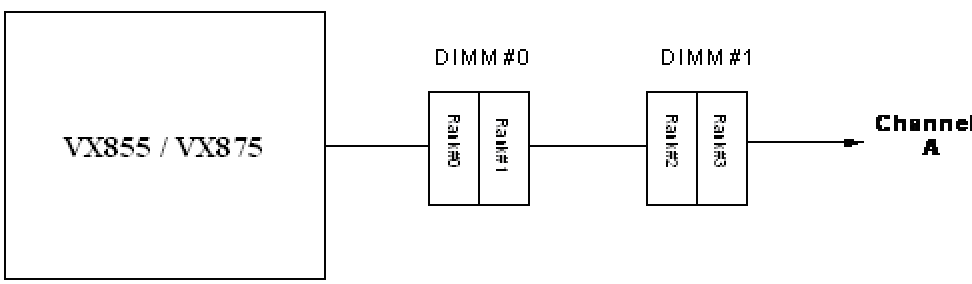


Figure 2. DIMM / Channel Mapping Diagram

DRAM Timing (60–64h)

Offset Address: 60h (D0F3)
DRAM Pipeline Turn-Around Setting — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**0ws Back-to-Back Write to Different DDR Rank** 0: Disable 1: Enable
6	RW	0	**Fast Read-to-Read Turn Around** 0: Disable 1: Enable (DQS post-amble overlap with preamble)
5	RW	0	**Fast Read-to-Write Turn Around** 0: Disable 1: Enable
4	RW	0	**Fast Write-to-Read Turn Around** 0: Disable 1: Enable
3:2	RO	0	**Reserved**
1:0	RW	0	**Reserved**

Offset Address: 61h (D0F3)
DRAM Timing for All Ranks 1 — **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Active-to-Active Period (tRRD)** 00: 2T 01: 3T 10: 4T 11: 5T
5:0	RW	04h	**Refresh-to-Active or Refresh-to-Refresh (tRFC)** 00h: 8T 01h: 9T … 0nh: (8+n)T 3Eh: 70T 3F:h: 71T

Offset Address: 62h (D0F3)
DRAM Timing for All Ranks 2 — **Default Value: 21h**

Bit	Attribute	Default	Description
7:4	RW	0010b	**Active-to-Precharge (tRAS)** 0000: 5T 0001: 6T … 0nh: (5+n)T 1110: 19T 1111: 20T
3	RW	0	**Enable DDR2 8-Bank Device Timing Constraint (tRRD and tRP)**
2:0	RW	001b	**CAS Latency** DDR DDR2 000 1.5 2 (not support DDR2 667/800) 001 2 3 010 2.5 4 011 3 5 1xx reserved 6

Offset Address: 63h (D0F3)
DRAM Timer for All Ranks 3 — **Default Value: 20h**

Bit	Attribute	Default	Description
7:5	RW	001b	**Write Recovery Time (tWR)** 000: 2T 001: 3T 010: 4T 011: 5T 100 : 6T Others: reserved
4	RO	0	**Reserved**
3	RW	0	**Read-to-Precharge Delay (tRTP)** 0: 2T 1: 3T
2	RO	0	**Reserved**
1:0	RW	00b	**Write to Read Command Delay (tWTR)** **DDR** **DDR2** 00 1T 2T 01 2T 3T 10 3T 4T 11 4T 5T

Offset Address: 64h (D0F3)
DRAM Timer for All Ranks 4 — **Default Value: 22h**

Bit	Attribute	Default	Description
7:5	RW	001b	**Active to Read or Write Delay (tRCD)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T Others: reserved
4	RW	0	**CKE Minimum Pulse Width** 0: 3T 1: 4T This function is valid when Dynamic CKE, D0F4 RxA1[6], is set to 1.
3:1	RW	001b	**Precharge Period (tPR)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T Others: reserved
0	RW	0	**Exit Precharge/Active Power Down to Any Command Delay** 0: 1T 1: 2T This function is valid when Dynamic CKE, D0F4 RxA1[6], is set to 1.

DRAM Queue / Arbitration (65–67h)

Offset Address: 65h (D0F3)
DRAM Arbitration Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Timer (In Unit of 4 DCLKs)** DRAM Controller for Channel A (DRAMCA) time slot allocated for AGP device. Active when there are pending memory requests from other requesters.
3:0	RW	0	**Host Timer (In Unit of 4 DCLKs)** DRAMCA time slot allocated for Host. Active when there are pending memory requests from other requesters.

Offset Address: 66h (D0F3)
DRAM Queue / Arbitration — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DRAMCA Queue Size Greater Than 2** 0: No 1: Yes
6	RW	0	**DRAMCA Queue Size Not Equal To 4** 0: No 1: Yes To setup DRAMCA queue size of 2, set Rx66[7:6] to 00b; set Rx66[7:6] to 11b for queue size of 3; set Rx66[7:6] to 10b for queue size of 4.
5:4	RW	00b	**Arbitration Parking Policy** 00: Park at the last bus owner 01: Park at CPU 10: Reserved 11: Park at VGA
3:0	RW	0	**Priority Promotion Timer (In Unit of 4 DCLKs)** A DRAM request is promoted to become a high priority request when it is pending over PTIM*4 DRAM cycles.

Offset Address: 67h (D0F3)
DIMM Command / Address Selection — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	00b	**DIMM 1 Command / Address Selection** 00: SCMD/MA Bus A Others: Reserved
1:0	RW	00b	**DIMM 0 Command / Address Selection** 00: SCMD/MA Bus A Others: Reserved

DRAM Control (68–69h)

Offset Address: 68h (D0F3)
DDR2 Page Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DRAM Expired Page Threshold** Close expired pages with precharge-all command when the number of expired pages exceeds the value.
3:0	RW	0	**Page Register Life Timer (In Unit of 16 DCLKs)** When timer expires, the expired page will be closed.

Offset Address: 69h (D0F3)
DDR2 Page Control 2 **Default Value: 82h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Bank Interleave – Channel A** 00: No interleave 01: 2-bank 10: 4-bank 11: 8-bank
5	RW	0	**Enable Bank Address Scramble** 0: Disable 1: Enable ***When set to 1:*** If Rx53[7] = 1 BA0 = A19 ^ A17 ^ A13; BA1 = A20 ^ A16 ^ A14; BA2 = A18 ^ A15; If Rx53[7] = 0 BA0 = A19 ^ A17 ^A15 ^ A13; BA1 = A20 ^A18 ^ A16 ^ A14; BA2 = 1'b0;
4	RW	0	**Auto-Precharge for TLB Read and CPU Write-Back** 0: Disable 1: Enable
3	RO	0	**Reserved**
2	RW	0	**Promote Priority of Refresh Request** 0: Low 1: High Suggest that set this bit to 1 for better performance.
1	RW	1b	**Keep Page Active When Cross Bank** 0: Disable 1: Enable
0	RW	0	**Multiple Page Mode** 0: Disable 1: Enable

Refresh Control (6A–6Bh)

Offset Address: 6Ah (D0F3)
Refresh Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Refresh Counter (In Unit of 16 DCLKs)** When set to 0, DRAM refresh is disabled

Offset Address: 6Bh (D0F3)
DRAM Miscellaneous Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**DQS Input DLL Adjustment** 0: Disable 1: Enable
6	RW	0	**DQS Output DLL Adjustment** 0: Disable 1: Enable
5	RW	0	**Burst Refresh** This chip only bursts 2 auto refreshes. 0: Disable 1: Enable
4	RW	1b	**DLL Manual Reset** 0: Disable 1: Enable
3	RO	0	**Reserved**
2:0	RW	000b	**SDRAM Operation Mode Select** 000: Normal SDRAM Mode 001: NOP Command Enable 010: All-Banks-Precharge Command Enable 011: MRS to SCMD 100: CBR, CAS-before-RAS refresh, Cycle Enable 101: Reserved 11x: Reserved

DDR SDRAM Control (6C–6Fh)

Offset Address: 6Ch (D0F3)
DRAM Type **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6	RO	0	**Memory Type Detected** 0: DDR 1: DDR2
5	RW	0	**Enable 32-bit Memory Width Mode – Channel A** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	0	**SDRAM Burst Length** For 64-bit mode ranks, SDRAM MRS 0: BL4 1: BL8
2	RW	0	**Channel Select** 0 : Enable channel A & B 1: Enable channel A only
1	RO	0	**Reserved**
0	RW	0	**Reserved**

Offset Address: 6Dh (D0F3)
DQ Channel Select **Default Value: C0h**

Bit	Attribute	Default	Description
7:4	RW	Ch	**Reserved (Do Not Program)**
3:2	RO	0	**Reserved**
1:0	RW	0	**Reserved**

Offset Address: 6Eh (D0F3)
DRAM Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Non-page Mode Support** 0: Disable 1: Enable
3	RW	1b	**Reserved (Do Not Program)**
2:0	RO	0	**Reserved**

Offset Address: 6Fh (D0F3)
Miscellaneous Control **Default Value: 42h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**DRAM-Side-Input-Pointer Non-Return-Zero Mode** 0: Disable 1: Enable Enable to avoid overwrite data
5:2	RW	0	**Reserved**
1	RW	1b	**Compact Refresh Mode (Skip CS for Non-Existing Rank While Refresh)** 0: Disable 1: Enable
0	RW	0	**Reserved**

DRAM Signal Timing Control (70–7Fh)

Offset Address: 70h (D0F3)
DQS Output Delay – Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DQS Output Delay**

Offset Address: 71h (D0F3)
MD Output Delay – Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**MD Output Delay**

Offset Address: 72-73h (D0F3) – Reserved

Offset Address: 74h (D0F3)
DQS Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Reserved**
3	RO	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQS Output – Channel A** Each step increases a phase of 1/8 T.

Offset Address: 75h (D0F3)
DQ Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Reserved**
3	RO	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQ (MD) Output – Channel A** Each step increases a phase of 1/8 T.

Offset Address: 76h (D0F3)

Write Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**1 More Pipeline Stage on Write Data Path** This bit is set to provide safer timing margin. 0: Disable 1:Enable
6	RW	0	**1 More Pipeline Stage on Write Data Path for DDR2-667 and Above** This bit is set to provide safer timing margin. 0: Disable 1:Enable
5	RW	0	**MD/DQS Output Clocks Bypass Delay Component** (i.e. when enabled, Rx70-73 becomes functionless)
4	RO	0	**Reserved**
3:2	RW	00b	**Advance Write Phase Signals to Make Room for the Long Bus Delay** 00: Normal mode 01: Advance 1 cycle 10: Advance 2 cycles 11: Forbidden The 2 bits must be used with bits [1:0].
1:0	RW	0	**Write MD/DQS/CAS Output Timing Range Control** Each step increases the output delay by 1/8 T.

Offset Address: 77h (D0F3)

DQS Input Delay Calibration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Manual DQS Input Delay Setting** 0: Auto 1: Manual
6	RO	0	**Reserved**
5:0	RO/RW	00h	**DDR DQS Input Delay** This is the base delay value of DQS input signal in unsigned binary format. The reading value depends on Rx77[7]. If Rx77[7] = 0 (auto mode), DLL calibration result is returned when read. This bit is RW only when Rx77[7] is 1.

Offset Address: 78h (D0F3)

DQS Input Capture Range Control – Channel A **Default Value: 80h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Reserved (Do Not Program)**
5:0	RW	00h	**DQS Input Capture Range** **Bits [5:4]** 00: 1T prior to 1st DQS rising edge 01: At 1st DQS rising edge 10: 1T after 11: Reserved **Bits [3:1]** Each step increases 1/8T delay **Bit [0]** Add 0.35ns fine tune delay, use Delay Cell Type to generate delay

Offset Address: 79-7Ah (D0F3) – Reserved

Offset Address: 7Bh (D0F3)
Read Data Phase Control — **Default Value: 02h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**MD Input Data Push Timing Control** 000: Start moving data into internal buffer 1T after the 1st DRAM strobe 001: 1.5T 010: 2T 011: 2.5T Bit 6 is always 0.
3	RW	0	**Reserved**
2	RW	0	**Read Data Bus from DIO to Data Path Module 1/2T Earlier**
1	RW	1b	**Extend the Time of DQS Input** 0: Disable (2T) 1: Enable (3T)
0	RW	0	**Reserved**

Offset Address: 7Ch (D0F3)
DLL Phase Detector Count (DLL_PD_CNT) Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1:0	RW	00b	**DLL_PD_CNT Low Pass Filter Setting** 00: 2 steps 01: 3 steps 10: 4 steps 11: 5 steps

Offset Address: 7D-7Fh (D0F3) – Reserved

Shadow RAM Control (80–83h)

Offset Address: 80h (D0F3)
Page-C ROM Shadow Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**C8000-CBFFFh Memory Space Access Control** See the description of bits [7:6].
3:2	RW	00b	**C4000-C7FFFh Memory Space Access Control** See the description of bits [7:6].
1:0	RW	00b	**C0000-C3FFFh Memory Space Access Control** See the description of bits [7:6].

Offset Address: 81h (D0F3)
Page-D ROM Shadow Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**D8000-DBFFFh Memory Space Access Control** See the description of bits [7:6].
3:2	RW	00b	**D4000-D7FFFh Memory Space Access Control** See the description of bits [7:6].
1:0	RW	00b	**D0000-D3FFFh Memory Space Access Control** See the description of bits [7:6].

Offset Address: 82h (D0F3)
Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**E8000-EBFFFh Memory Space Access Control** See the description of bits [7:6].
3:2	RW	00b	**E4000-E7FFFh Memory Space Access Control** See the description of bits [7:6].
1:0	RW	00b	**E0000-E3FFFh Memory Space Access Control** See the description of bits [7:6].

Offset Address: 83h (D0F3)
Page-F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**F0000-FFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
3:2	RW	00b	**Memory Hole** 00: None 01: 512K ~ 640K, MHOLE1 (80000h – 9FFFFh) 10: 15M ~ 16M (1M), MHOLE2 (F00000h – FFFFFFh) 11: 14M ~ 16M (2M), MHOLE 3 (E00000h – FFFFFFh)
1	RW	0	**Disable Data Access on SMRAM (Page A, B) in SM (System Management) Mode** 0: Page A,B CPU Data R/W cycles are forwarded to the memory controller. 1: Page A,B CPU Data R/W cycles are forwarded to the PCI bus Notes: 1. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A,B Code R/W cycles are always forwarded to the memory controller in SM mode.
0	RW	0	**Enable Page A, B DRAM Access In Normal Mode** 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of bit 1, the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller. Check the following table for details.

Table 10. CPU-to-SMRAM Cycle Flow

Rx83[1]	Rx83[0]	CPU MODE	Target of CODE Access Cycle	Target of DATA Access Cycle
x	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

DRAM Above 4G Support (84-8F)

Offset Address: 84h (D0F3)
Low Top Address – Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address [23:20]**
3:0	RO	0	**Reserved**

Offset Address: 85h (D0F3)
Low Top Address – High **Default Value: FFh**

Bit	Attribute	Default	Description
7:0	RW	FFh	**Low Top Address [31:24]**

Offset Address: 86h (D0F3)
SMM and APIC Decoding **Default Value: 03h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Top SM Memory Size** 00: 1M 01: 2M 10: 4M 11: 8M When Rx86[2] = 1, the SM memory is enabled.
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxxh are passed to PCI1 1: Cycles accessing FEC7_FFFFh – FEC0_0000h are passed to PCI1; cycles accessing FECF_FFFFh – FEC8_0000h access cycles are passed to PCI2.
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxxh from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxxh from masters are passed to the Host side for snooping
2	RW	0	**Enable Top SM Memory** 0: Disable 1: Enable
1	RW	1b	**SDIO Support for Using System Memory 4Kbytes** 0: Disable 1: Enable
0	RW	1b	**Enable Compatible SMM** 0: Disable 1: Enable

Offset Address: 87h (D0F3) – Reserved

Offset Address: 89-88h (D0F3)
The Address Next to the Last DRAM Bank Ending Address **Default Value: 0004h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10:0	RO	04h	**The Address Next to the Last Valid DRAM Address**

Offset Address: 8Ah (D0F3)
DQ Driving Strength Auto-Comp Status **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	n	**DQ Pull-up Driving Strength Auto-comp Value**
3:0	RO	n	**DQ Pull-down Driving Strength Auto-comp Value**

Offset Address: 8Bh (D0F3) – Reserved

Offset Address: 8Ch (D0F3)
DQS Output Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**MD/DQS Earlier Output Enable** 0: Disable 1: Enable DQ Output Enable (MDOE) 1/2T earlier DQS Output Enable (DQSOE) 1/2T earlier if bit 0 =0
0	RW	0	**DQS Earlier Output Enable** 0: Disable 1: Enable DQSOE 1/4T earlier if bit 1 =1

Offset Address: 8D-8Fh (D0F3) – Reserved

DRAM Clocking Control (90-9F)

Offset Address: 90h (D0F3)
DRAM Clock Operation Mode and Frequency **Default Value: n0h**

Bit	Attribute	Default	Description
7:5	RW	n	**Reserved**
4:3	RO	n	**Reserved**
2:0	RW	000b	**DRAM Operating Frequency** 000: Reserved 001: Reserved 010: Reserved 011: 200MHz 100: 266MHz 101: 333MHz 110: 400MHz 111: Reserved

Offset Address: 91h (D0F3)
DCLK (MCLK) Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:0	RW	0	**DCLKOA Phase Select** Each step increases 1/8T from DCLK. DCLKOA is the output clock from DRAMCA to populated DIMM.

Offset Address: 92h (D0F3)
CS/CKE Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:0	RW	0	**Sampling Clock Phase Select for CS/CKE – Channel A** Each step increases a phase of 1/8 T from DCLK. Adjusted clock will be used to sample channel B's CS/CKE/ODT signals.

Offset Address: 93h (D0F3)
SCMD/MA Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:0	RW	0	**Sampling Clock Phase Select for SCMD/MA – Channel A** Each step increases a phase of 1/8 T from DCLK. Adjusted clock will be used to sample channel A's SCMD/MA signals.

Offset Address: 94h (D0F3) – Reserved

Offset Address: 95h (D0F3)
By-Rank Self Refresh Related Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Check GFX Vertical Blank When Rank 3 Enters By-Rank Self Refresh** 0: Not check 1: Check
6	RW	0	**Check Self-Refresh Request When Rank 3 Enters By-Rank Self Refresh** 0: Not check 1: Check
5	RW	0	**Check GFX Vertical Blank When Rank 2 Enters By-Rank Self Refresh** 0: Not check 1: Check
4	RW	0	**Check Self-Refresh Request When Rank 2 Enters By-Rank Self Refresh** 0: Not check 1: Check
3	RW	0	**Check GFX Vertical Blank When Rank 1 Enters By-Rank Self Refresh** 0: Not check 1: Check
2	RW	0	**Check Self-Refresh Request When Rank 1 Enters By-Rank Self Refresh** 0: Not check 1: Check
1	RW	0	**Check GFX Vertical Blank When Rank 0 Enters By-Rank Self Refresh** 0: Not check 1: Check
0	RW	0	**Check Self-Refresh Request When Rank 0 Enters By-Rank Self Refresh** 0: Not check 1: Check.

Offset Address: 96h (D0F3)
By-Rank Self Refresh Related Registers 2 **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**Pairwise By-Rank Self Refresh in High Speed** 0: Disable 1: Enable
6:4	RW	001b	**The Number of Idle Auto-Refresh Before A Rank Does By-Rank Self Refresh** 000: Enter self refresh after 0 continuous auto refresh. 001: Enter self refresh after 1 continuous auto refresh. 010: Enter self refresh after 2 continuous auto refreshes. 011: Enter self refresh after 3 continuous auto refreshes. 100: Enter self refresh after 4 continuous auto refreshes. 101: Enter self refresh after 5 continuous auto refreshes. 110: Enter self refresh after 6 continuous auto refreshes. 111: Enter self refresh after 7 continuous auto refreshes.
3	RW	0	**Enable Rank 3 to Do By-Rank Self Refresh** 0: Disable 1: Enable
2	RW	0	**Enable Rank 2 to Do By-Rank Self Refresh** 0: Disable 1: Enable
1	RW	0	**Enable Rank 1 to Do By-Rank Self Refresh** 0: Disable 1: Enable
0	RW	0	**Enable Rank 0 to Do By-Rank Self Refresh** 0: Disable 1: Enable

Offset Address: 97h (D0F3)
By-Rank Self Refresh Related Registers 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Pairwise Exit From By-Rank Self Refresh in High Speed.** This register becomes effective for DDR2 667 and above is supported. 0: Disable 1: Enable
6:3	RO	0	**Reserved**
2:0	RW	0	**Reserved**

Offset Address: 98h (D0F3)
DRAM Channel Pipeline Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Pipelining Stage on Request Page Decoding** This bit is to improve DRAMCA internal timing for DDR2 800 and above, but increase latency. When this bit is set, DRAMCA will provide 1T margin for page decoding. 0: Disable 1: Enable
6	RW	0	**2T Page Close Command**
5	RW	0	**2T Command Scheduling** This bit is set to improve DRAMCA internal timing for DDR2 800 and above when Rx50[0] =1, but may affect performance. 0: Disable 1: Enable
4	RO	0	**Reserved**
3	RW	0	**2T Internal Active and Precharge Command Scheduling** It should be 1b when bit 5 is set.
2	RO	0	**Reserved**
1	RW	0	**Reserved**
0	RW	0	**CKE Pipeline – Channel A** Enable 1T pipe for CKEA output to balance internal timing of CKE and SCMD/MA when Rx6E[3] =0 Rx6E[3] Rx98[0] Pipeline for CKE 1 1 2T 1 0 1T 0 1 1T 0 0 No pipe

Offset Address: 99h (D0F3)
DCLKO (MCLK) Phase Control **Default Value: 7Fh**

Bit	Attribute	Default	Description
7	RW	0	**Write Ready Signal Timing** 0: Write ready signal not register out 1: Write ready signal register out. It should be used for DDR2 667 and above
6:5	RW	11b	**Reserved (Do Not Program)**
4:1	RW	1111b	**Select MCLKO Output (bit-wise)** If bits [4:1] are set to 1111b, all MCLKOA[3:0] will output MCLK. If bits [4:1] are set to 0011b, only MCLKOA[1:0] will output MCLK.
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: 9A-9Bh (D0F3) – Reserved

Offset Address: 9Ch (D0F3)
ODT Lookup Table – Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Rank 3 ODT Signal Selection** 00: ODTA0 01: ODTA1 10: ODTA2 11: ODTA3 Take bits [7:6] =10b for example. When DRAMC forwards R/W command to rank3, rank2 will turn on ODT.
5:4	RW	00b	**Rank 2 ODT Signal Selection** See the description of bits [7:6].
3:2	RW	00b	**Rank 1 ODT Signal Selection** See the description of bits [7:6].
1:0	RW	00b	**Rank 0 ODT Signal Selection** See the description of bits [7:6].

Offset Address: 9Dh (D0F3) – Reserved

Offset Address: 9Eh (D0F3)
SDRAM ODT Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DDR2 SDRAM ODT Control** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	00b	**Add MD Bus Turn-Around Wait State for DDR2 ODT** When MD bus changes from read response to write accept, extra wait state should be appended for ODT. 00: Disable 01: 1T wait state 10: 2T wait state 11: 3T wait state
3:2	RO	0	**Reserved**
1	RW	0	**Differential DQS Input – Channel B** 0: Disable 1: Enable
0	RW	0	**Differential DQS Input – Channel A** 0: Disable 1: Enable

Offset Address: 9Fh (D0F3)
SDRAM ODT Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DDR2 SDRAM ODT Write Cycle Late Extension** Post-amble extends certain cycles according to bits [7:6]. 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension
5:4	RW	00b	**DDR2 SDRAM ODT Read Cycle Late Extension** Post-amble extends certain cycles according to bits [5:4]. 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension
3:2	RO	0	**Reserved**
1:0	RW	00b	**DDR2 SDRAM ODT Early Extension** Pre-amble extends certain cycles according to bits [1:0]. 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension

UMA Registers (A0–AFh)

Offset Address: A1-A0h (D0F3)
CPU Direct Access Frame Buffer Control **Default Value: 8000h**

Bit	Attribute	Default	Description
15	RW	1b	**Internal GFX Enable** 0: Disable 1: Enable
14:12	RW	000b	**System Frame Buffer Size Selection – Channel A** 000: none 001: 8M 010: 16M 011: 32M 100: 64M 101: 128M 110: 256M 111: 512M
11:1	RW	0	**CPU Direct Access Frame Buffer Address [31:21]**
0	RW	0	**CPU Direct Access Frame Buffer Enable** 0: Disable 1: Enable

Offset Address: A2h (D0F3)
Internal GFX Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Internal GFX High Priority Timer (In Unit of 16 DCLKs)**
3:0	RW	0	**Internal GFX Timer (In Unit of 16 DCLKs)**

Offset Address: A3h (D0F3)

GFX MMIO Base Address 1 (M1) Space Size — **Default Value: 02h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	010b	**GFX M1 Space Size Selection** 000: None 001: 8M 010: 16M 011: 32M 100: 64M 101: 128M 110: 256M 111: 512M The base address of M1 is located in D0F0 RxCF-CCh.

Offset Address: A5-A4h (D0F3)

GFX Misc. — **Default Value: 00h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW	0	**Reserved**
12	RO	0	**Reserved**
11:8	RW	0	**Reserved**
7:6	RO	0	**Reserved**
5	RW	0	**Reserved**
4:3	RO	0	**Reserved**
2	RW	0	**Reserved**
1	RO	0	**Reserved**
0	RW	0	**GFX Data Delay to Sync with Clock** 0: Not sync 1: Sync with clock

Offset Address: A6h (D0F3)

Page Register Life Timer 1 in CPU Power Saving States — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable Page Register Life Timer 1 in C4 State** 0: Disable 1: Enable
5	RW	0	**Enable Page Register Life Timer 1 in C3 State** 0: Disable 1: Enable
4	RW	0	**Enable Page Register Life Timer 1 in C2 State** 0: Disable 1: Enable
3:0	RW	0	**Page Register Life Timer 1 (In Unit of 4 DCLKs)** When timer expires, the expired page will be closed.

Offset Address: A7h (D0F3)

GMINT (GFX-Memory Interface) and GFX Related Register — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Guard GFX Snoop Write** 0: Snoop write cycle will treat as read 1: Treat snoop write cycle as normal write
6	RW	0	**All Read Request Snoop** 0: Read requests with G2M (GFX-to-Memory) cycle need snoop host CPU-to-Memory FIFO (CMFIFO) 1: All read request will snoop host CMFIFO
5:4	RO	0	**Reserved**
3	RW	0	**Internal Graphic Enable – for Address Allocation** 0: External GFX 1: Internal GFX allocation
2	RW	0	**Channel-A GFX to DRAM Read Snoop CMFIFO** 0: Not snoop 1: Snoop
1:0	RW	0	**Reserved**

Offset Address: A8-Afh (D0F3) – Reserved

GMINT and AGPCINT Registers (B0–BFh)

Offset Address: B0-B2h (D0F3) – Reserved

Offset Address: B3h (D0F3)
GMINT Misc. **Default Value: 9Eh**

Bit	Attribute	Default	Description
7:5	RW	100b	**Flush Counter Used when RxB3[2] =1 & Write Queue Full** 100b indicates when GMINTA works in read pass write mode, GMINTA will prioritize to pop "4" write requests if write request queue is full.
4:3	RW	11b	**Reserved**
2	RW	1b	**GMINTA Read Pass Write** GMINTA has two 8 level request queues: read queue and write queue. To improve performance, GMINTA will let read request surpass write request. 0: Read write in order (only read queue active) 1: Read pass write
1	RW	1b	**Reserved**
0	RO	0	**Reserved**

Offset Address: B4-BFh (D0F3) – Reserved

Offset Address: C0-CFh (D0F3) – Reserved

DDR2 – I/O Pad Termination and Driving Control (D0–DFh)

Offset Address: D0h (D0F3)
DQ / DQS Termination Strength Manual Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQ/DQS Pull-up Termination Strength Manual Setting**
3:0	RW	0	**DQ/DQS Pull-down Termination Strength Manual Setting**

Offset Address: D1h (D0F3)
DQ / DQS Termination Strength Auto-Comp Status **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	n	**DQ/DQS Pull-up Termination Strength Auto-comp Value**
3:0	RO	n	**DQ/DQS Pull-down Termination Strength Auto-comp Value**

Offset Address: D2h (D0F3)
North Module (NM) Power State **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	000b	**NM Power State** 000: C0, CPU full run 001: C2 010: C4 VRDSLP assert 011: C3, CPU does not snoop DRAM 100: S3 (no use) 101: V1 system in V1 110: C4P PLL gate/reset/off 111: Reserved

Offset Address: D3h (D0F3)

Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RO	0	**Reserved**
1	RW	0	**Control DDR Compensation Auto Mode** 0: Enable Auto Mode 1: Disable Auto Mode If DDR Compensation and DDR Auto Compensation are both enabled, the ODT settings for all DRAM pads are from auto-comp circuit (RxD1); otherwise, if Auto Compensation is disabled, the ODT settings are from manual setting (RxD0).
0	RW	0	**Enable DDR Compensation** 0: Disable 1: Enable Disable DDR Compensation provides a power saving mode; however, the values of RxD1 and RxD2 should be ignored.

Note: The DQ driving bits of RxD2 is the result of the auto-comp circuit; however, there is no “auto-mode” for the DQ/DQB driving control since it depends on the actual number of ranks in the DRAM data channel.

Offset Address: D4h (D0F3)

ODT Pull-up / Pull-down Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PRE Pad ODT for 1st Write Data** 0: Disable 1: Enable When this bit is enabled, PAD ODT will turn on for 1st idle write (the 1st write after long time bus idle).
6	RW	0	**Reserved**
5	RW	0	**Enable DRAM MD Pad ODT – Channel A High 32 Bits** 0: Disable ODT unless RxD4[2] is not equal to 0 1: Enable ODT when reading data
4	RW	0	**Enable DRAM MD Pad ODT – Channel A Low 32 Bits** 0: Disable ODT unless RxD4[1] is not equal to 0 1: Enable ODT when reading data
3	RW	0	**Enable NM Pad ODT – Channel B** 0: Disable ODT unless RxD4[0] is not equal to 0 1: Enable ODT when reading data
2	RW	0	**Turn on DRAM MD Pad ODT of Channel A High 32 Bits** 0: Disable 1: Enable
1	RW	0	**Turn on DRAM MD Pad ODT of Channel A Low 32 Bits** 0: Disable 1: Enable
0	RW	0	**Turn on DDRPHY ODT of Channel B** 0: Disable 1: Enable

MD PADs ODT Control

The MD PADs ODT control will affect the current leakage. Please set RxD4 control registers for different DRAM channel (A or A+B) modes with saving power.

Table 11. MD PADs ODT Control in Different DRAM Mode

DRAM Mode		Group Set *(Please refer to the following Group table)*
Channel A	**Channel B**	
Channel A 64-bit	N/A	{1 & 2}
Channel A 32-bit	N/A	{2}
Channel A 64-bit	Channel B 16-bit	{1 & 2 & 3}
Channel A 32-bit	Channel B 16-bit	{2 & 3}

Table 12. PAD ODT Control Group Setting

Group	MD Byte	Register	MD ODT Control State		
			Turn-off	Static-on	Dynamic-on
1	Channel A upper byte7~4	RxD4[5]	0	x	1
		RxD4[2]	0	1	0
2	Channel A lower byte3~0	RxD4[4]	0	x	1
		RxD4[1]	0	1	0
3	Channel B	RxD4[3]	0	x	1
		RxD4[0]	0	1	0

<u>**Offset Address: D5h (D0F3)**</u>

DQ / DQS Burst Function and ODT Range Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DQ/DQS Burst Function – Channel A** 0: Disable 1: Enable
6	RW	0	**Enable DQ/DQS Burst Function – Channel B** 0: Disable 1: Enable
5	RW	0	**CS/CKE/ODT Burst Function – Channel A** 0: Disable 1: Enable
4	RW	0	**CS/CKE/ODT Burst Function – Channel B** 0: Disable 1: Enable
3:2	RW	00b	**DQ/DQS ODT Range Select – Channel A** 00: 150 ohm / 120 ohm 01: 75 ohm / 60 ohm 1x: 50 ohm / 40 ohm
1:0	RW	00b	**DQ/DQS ODT Range Select – Channel B** 00: 150 ohm / 120 ohm 01: 75 ohm / 60 ohm 1x: 50 ohm / 40 ohm

<u>**Offset Address: D6h (D0F3)**</u>

DCLK / SCMD / CS Driving Select **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**DCLKOA Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
6	RW	0	**DCLKOB Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
5	RW	0	**SCMD/MAA Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
4	RW	0	**SCMD/MAB Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
3	RW	0	**CKE/CSA Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
2	RW	0	**CKE/CSB Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
1:0	RO	0	**Reserved**

Offset Address: D7h (D0F3)
SCMD/MA Burst Function **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SCMD/MAA Burst Function Enable** 0: Disable 1: Enable
6	RW	0	**SCMD/MAB Burst Function Enable** 0: Disable 1: Enable
5:0	RW	0	**Reserved**

Offset Address: D8-Dah (D0F3) – Reserved

Offset Address: DBh (D0F3)
Operation Mode Control – Channel B **Default Value: 80h**

<table>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Description</th></tr>
<tr><td>7</td><td>RW</td><td>1b</td><td>Reserved (Do Not Program)</td></tr>
<tr><td>6</td><td>RW</td><td>0</td><td>Initialization Clock
Choose NM PLL’s 166/133MHz clock as DRAM Controller for Channel B (DRAMCB) clock source in order to proceed initialization or function test.

See the bit 5 for operating mode select.</td></tr>
<tr><td>5</td><td>RW</td><td>0</td><td>Initialization Select
The clocks of DRAMCB and MCLKO0B P/N are always supplied when this bit has been programmed to 1. After initialization is done, this bit must be programmed to 0.

There are 4 different operation modes:
<table>
<tr><th>Bit 6</th><th>Bit 5</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Normal snapshot operation mode</td></tr>
<tr><td>0</td><td>1</td><td>Initialization with GFX’s display clock</td></tr>
<tr><td>1</td><td>0</td><td>DRAMCB snapshot function test mode (RxDD[3] =1)</td></tr>
<tr><td>1</td><td>1</td><td>Initialization with NB’s PLL clock (RxDD[3] =0)</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>4:2</td><td>RW</td><td>0</td><td>Command Type
Command types will be triggered by bit RxDB[1]
<table>
<tr><th>RAS</th><th>CAS</th><th>WE</th><th>Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>NOP</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Ready/completion for Read/Write
This command must be triggered once before/after Read/Write command is issued. This command is only used by NM for preparing/terminating. Read/Write state machine of initialization and won't be really issued on DRAM bus.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Read command
BA[1:0]=RxF9-F8h[14:13], MA[12:0]=RxF9-F8h[12:0], the returned data can be read from D0F7 RxDF-D0 after this command. Bank-Activate command must be triggered before this command can be triggered.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Write command
BA[1:0]=RxF9-F8h[14:13], MA[12:0]=RxF9-F8h[12:0], write data will be D0F7 RxCF-C0. Bank-Activate command must be triggered before this command can be triggered.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Bank-Activate command
BA[1:0]=RxF9-F8h[14:13], MA[12:0]=RxF9-F8h[12:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Single-Bank-Precharge (RxF9-F8h[10]=0)/Precharge-All-Banks (RxF9-F8h[10]=1), BA[1:0]=RxF9-F8h[14:13], MA[12:0]=RxF9-F8h[12:0].</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Auto-Refresh</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MRS(RxF9-F8h[14:13]=00b)/EMRS(1)(RxF9-F8h[14:13]=01b)/ EMRS(2)(RxF9-F8h[14:13]=10b)/EMRS(3)(RxF9-F8h[14:13]=11b), the written content should be pre-programmed in RxF9-F8h[12:0] which will be placed on MA[12:0] when the command is asserted.</td></tr>
</table>
To save more DRAM power consumption, set RxF9-F8h[1] = 1 to enable quarter array self-refresh during EMRS(2). Actually, snapshot mode will work fine even without any DRAM refresh.

To save more DRAM power consumption, set RxF9-F8h[1] = 1 to reduce output driving strength during EMRS.
It may work fine when the frequency is low.</td></tr>
<tr><td>1</td><td>RW</td><td>0</td><td>Command Trigger
Issue a command which is defined by RxDB[3:2] to DRAM bus. Once this bit is writing 0 then 1 will trigger one command to DRAM bus.</td></tr>
<tr><td>0</td><td>RW</td><td>0</td><td>Precharge Power Down
Snapshot DRAM will enter Precharge power down instead of Self Refresh.
It will take less recovery time from pending to access DRAM. This bit can only be turned on/off during initialization.</td></tr>
</table>

Offset Address: DCh (D0F3)

Timing Parameters Control – Channel B **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Read CAS Latency** 00: 2T 01: 3T 10: 4T 11: 5T Normally, RxDC[7:6] = RxDF[7:6]. But if DRAM's DLL has been disabled, it might be set as (RxDF[7:6]-1) or (RxDF[7:6]+1) according to the actual read data timing. Notes: 1. tRCD is always 4T. 2. tRP is always 4T.
5:4	RO	0	**Reserved**
3	RW	0	**Enable Chip's ODT When Read** 0: Disable 1: Enable
2	RW	0	**Enable Chip's ODT When Write** 0: Disable 1: Enable
1	RW	0	**Enable DRAM's ODT When Read** 0: Disable 1: Enable
0	RW	0	**Enable DRAM's ODT When Write** 0: Disable 1: Enable Notes: 1. It is always 1T command. 2. It only supports X16 DRAM chip X 1. 3. It only supports 2 bank address pins, BA1~BA0. 4. It only supports burst length 8.

Offset Address: DDh (D0F3)

PADs Power-Down Control – Channel B **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**ODT PAD Power Down** 0: Disable 1: Enable
6	RW	0	**Column Address Type** 0: MA8~MA0 1: MA9~MA0
5:4	RW	00b	**Power Down Unused MAB PADs** 00: MAB12 and MAB11 are available 01: DRAMCB debug mode. MAB12, MAB11 and CASB[3:0] are not available. 10: MAB12 is not available, but MAB11 is available. 11: MAB12 and MAB11 are not available The corresponding MAB[12:11] pins of DRAM chips used for channel B must be tied to 0 to prevent high impedance.
3	RW	0	**Power Down Data Mask [1:0] PADs** DQM pins must be tied to 0 on boards.
2:0	RW	000b	**Adjust The Timing Window of Capturing 2X Read Data** 000: Rising Clock Edge without extra delay 001: Rising Clock Edge with 0.5 ~ 1ns Delay 010: Rising Clock Edge with 1 ~ 2ns Delay 011: Rising Clock Edge with 1.5 ~ 3ns Delay 100: Falling Clock Edge with 2 ~ 4ns Delay 101: Falling Clock Edge with 2.5 ~ 5ns Delay 110: Falling Clock Edge with 3 ~ 6ns Delay 111: Falling Clock Edge with 3.5 ~ 7ns Delay

Offset Address: DEh (D0F3)

GMINT's Merge Function **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**In Order to Enter S3, DRAMCC Will Enter Self-refresh Mode Even GFX Declares Snapshot Mode** 0: Disable 1: Enable
1	RW	0	**GMINTA Merge Mode** When GFXCTL issues two 2QW requests with address linearly increased, GMINTA will merge these 2QW requests to one 4QW request. 0: Merge 2QW requests 1: Disable 2QW merge
0	RW	0	**Reserved**

Offset Address: DFh (D0F3)

Write Cycle Timing Control – Channel B **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Write CAS Latency** It should be set as (tCL(MRS[6:4]) - 1)T 00: 1T 01: 2T 10: 3T 11: 4T Note: MRS: Mode Register Set, a programming sequence to DRAM DIMM at the beginning of the system boot up. The bits programmed in this register should be corresponding to the MRS[6:4] which defines the CAS latency as: **MRS[6:4] CL[2:0] CAS Latency Bits[7:6]** 111 111 Reserved - 110 110 Reserved - 101 101 5T 11 (4T) 100 100 4T 10 (3T) 011 011 3T 01 (2T) 010 010 2T 00 (1T) 001 001 Reserved - 000 000 Reserved -
5	RW	0	**Tri-state Output Signal Enable for Self-refresh and Precharge Power-down** 0: Disable 1: Enable Tri-state all output signals except CKE during self-refresh, or tri-state all output signals except CKE, ODT and MCLKO during Precharge Power-down. It must be set to 0 in DRAMCB debug mode.
4:3	RW	00b	**Adjust Write DQ Delay** 00: Delay 1 ~ 2 ns from DQS 01: Delay 1.1 ~ 2.2 ns from DQS 10: Delay 1.2 ~ 2.4 ns from DQS 11: Delay 1.3 ~ 2.6 ns from DQS
2	RW	0	**Tri-state Output Signal Enable for Active Power-down** Tri-state all output signals except CKE, ODT and MCLKO during Active Power-down. 0: Disable 1: Enable
1:0	RW	00b	**Adjust MCLKO (DRAM Clock) Delay** 00: -0.2 ~ 0.4 ns 01: -0.1 ~ 0.2 ns 10: 0 ns 11: 0.1 ~ 0.2 ns

DRAM Driving Control (E0–EBh)

Table 13. Physical Pin to Driving Group Mapping Table

Physical Pins	MCLK[A, B]	CKE[A, B]	CS[A, B]	MA[A, B]	DQ[A, B]	DQS[A, B]	DQM[A, B]
Driving Group	MCLK[A, B]	CS[A, B]	CS[A, B]	MA[A, B]	DQ[A, B]	DQS[A, B]	DQ[A, B]

Offset Address: E0h (D0F3)
DRAM Driving – Group DQSA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQSA - PMOS Driving**
3:0	RW	0	**DQSA - NMOS Driving**

Offset Address: E1h (D0F3)
DRAM Driving – Group DQSB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQSB – PMOS Driving**
3:0	RW	0	**DQSB – NMOS Driving**

Offset Address: E2h (D0F3)
DRAM Driving – Group DQA (MD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQA – PMOS Driving**
3:0	RW	0	**DQA – NMOS Driving**

Offset Address: E3h (D0F3)
DRAM Driving – Group DQB (MD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQB – PMOS Driving**
3:0	RW	0	**DQB – NMOS Driving**

Offset Address: E4h (D0F3)
DRAM Driving – Group CSA (CS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**CSA – PMOS Driving**
3:0	RW	0	**CSA – NMOS Driving**

Offset Address: E5h (D0F3)
DRAM Driving – Group CSB (CS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**CSB – PMOS Driving**
3:0	RW	0	**CSB – NMOS Driving**

Offset Address: E6h (D0F3)
DRAM Driving – Group MCLKA **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b	**MCLKA – PMOS Driving**
3:0	RW	1000b	**MCLKA – NMOS Driving**

Offset Address: E7h (D0F3)
DRAM Driving – Group MCLKB **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b	**MCLKB – PMOS Driving**
3:0	RW	1000b	**MCLKB – NMOS Driving**

Offset Address: E8h (D0F3)
DRAM Driving – Group SCMDA/MAA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**MAA – PMOS Driving**
3:0	RW	0	**MAA – NMOS Driving**

Offset Address: E9h (D0F3)
DRAM Driving – Group SCMDB/MAB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**MAB – PMOS Driving**
3:0	RW	0	**MAB – NMOS Driving**

Offset Address: EA-EBh (D0F3) – Reserved

DRAM CKG Control (EC–EFh)

Offset Address: ECh (D0F3)
Channel-A DQS / DQ CKG Output Duty Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 50 ps 10: Falling edge delays 100 ps 11: Falling edge delays 150 ps
5:4	RW	00b	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 50 ps 10: Rising edge delays 100 ps 11: Rising edge delays 150 ps
3:2	RW	00b	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 50 ps 10: Falling edge delays 100 ps 11: Falling edge delays 150 ps
1:0	RW	00b	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 50 ps 10: Rising edge delays 100 ps 11: Rising edge delays 150 ps

Offset Address: EDh (D0F3)
DQS / DQ CKG Output Duty Cycle Control – Channel B **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00b	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00b	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00b	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: EEh (D0F3)
DCLK Output Duty Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Duty Control for DCLKA** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00b	**Duty Control for DCLKA** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00b	**Duty Control for DCLKB** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00b	**Duty Control for DCLKB** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: EFh (D0F3)
DQ CKG Input Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**Delay Control for MDA** 00: 0 ps 01: 50 ps 10: 100 ps 11: 150 ps
3:2	RO	0	**Reserved**
1:0	RW	00b	**Delay Control for MDB** 00: 0 ps 01: 50 ps 10: 100 ps 11: 150 ps

DQ / DQS CKG Output Delay Control (F0–F9h)

Offset Address: F3-F0h (D0F3)
DQ/DQS CKG Output Delay Control - Channel A **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:28	RW	000b	**DQ/DQS Delay Control for Group A7** 000: Default 001: Delay 60 ps 010: Delay 120 ps 011: Delay 180 ps 100: Delay 240 ps 101: Delay 300 ps 110: Delay 360 ps 111: Delay 420 ps
27	RO	0	**Reserved**
26:24	RW	0	**DQ/DQS Delay Control for Group A6** See the description of bits [30:28].
23	RO	0	**Reserved**
22:20	RW	0	**DQ/DQS Delay Control for Group A5** See the description of bits [30:28].
19	RO	0	**Reserved**
18:16	RW	0	**DQ/DQS Delay Control for Group A4** See the description of bits [30:28].
15	RO	0	**Reserved**
14:12	RW	0	**DQ/DQS Delay Control for Group A3** See the description of bits [30:28].
11	RO	0	**Reserved**
10:8	RW	0	**DQ/DQS Delay Control for Group A2** See the description of bits [30:28].
7	RO	0	**Reserved**
6:4	RW	0	**DQ/DQS Delay Control for Group A1** See the description of bits [30:28].
3	RO	0	**Reserved**
2:0	RW	0	**DQ/DQS Delay Control for Group A0** See the description of bits [30:28].

Offset Address: F4-F7h (D0F3) – Reserved

Offset Address: F9-F8h (D0F3)

DRAM Mode Register Setting (MRS) Control – DRAMCB **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:0	RW	0	**DRAMCB MRS Register** The content will be placed on MA and BA when MRS/EMRS(1,2,3)/Bank-Activate/Write/Read commands are triggered. Bits [14:13] - BA[1:0] Bits [12:0] - MA[12:0]

DDR2 – DQ De-Skew Control (FA–FFh)

Offset Address: FAh (D0F3) – Reserved

Offset Address: FBh (D0F3)

Power Management - Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Enable SCMD Top Logic Dynamic Clock** 0: Disable 1:Enable
4	RW	0	**Enable CAS Top Logic Dynamic Clock** 0: Disable 1:Enable
3	RW	0	**Enable MDA Top Logic Dynamic Clock** 0: Disable 1:Enable
2	RW	0	**Enable DQS Top Logic Dynamic Clock** 0: Disable 1:Enable
1	RW	0	**Enable DRAM Page Control Module Dynamic Clock** 0: Disable 1:Enable
0	RW	0	Reserved

Offset Address: FCh (D0F3) – Reserved

Offset Address: FDh (D0F3)

Power Management 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Stop Page Timer's Clock when DRAMCA's Ranks All Enter Self Refresh** 0: Free running 1: Enable dynamic
6	RW	0	**Reserved**
5	RW	0	**Stop MCLKOA When All Ranks Enter Self Refresh** 0: Free running 1: Enable dynamic
4	RW	0	**Reserved**
3	RW	0	**Power Management of Reference Dynamic Clock Enable – Channel A** 0: Free running 1: Enable dynamic
2:1	RW	0	**Reserved**
0	RW	0	**Power Management of Dynamic DQA Clock's Source – Channel A** 0: Free running 1: Enable dynamic

Offset Address: FEh (D0F3)
Power Management 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Precise Power Management of Internal DBX C2MFIFO's Clock** 0: Precise power management 1: Normal power management
5	RW	0	**Enable Auto Refresh Dynamic Clock of Refresh Control Module Stop While DRAM Enters Sleep Mode** 0: Disable 1: Enable
4	RW	0	**Reserved**
3:0	RW	0	**Enable Chip Select A Pin as Power Saving Mode When This Rank Enters Self Refresh** 0: Disable 1: Enable Bit 3 – Chip Select A3 Bit 2 – Chip Select A2 Bit 1 – Chip Select A1 Bit 0 – Chip Select A0

Offset Address: FFh (D0F3)
The Rest of Registers — **Default Value: 01h**

Bit	Attribute	Default	Description
7:2	RW	0	**DQSB Input Delay** The adjustment of DQSB in the read path and each step can delay 30~50p.
1	RW	0	**Reserved**
0	RW	1b	**Enable SCMD** MA Bus floats during suspend state 0: Disable 1: Enable

Device 0 Function 4 (D0F4): Power Management Control

PCI Configuration Space

All registers in D0F4 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 4.

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F4)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F4)

Device ID **Default Value: 4409h**

Bit	Attribute	Default	Description
15:0	RO	4409h	**Device ID**

Offset Address: 05-04h (D0F4)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RO	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F4)

PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target Abort Assertion** This chip does not assert Target Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F4)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F4)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F4) – Reserved

Offset Address: 0Dh (D0F4)

PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master (In Unit of PCI Clocks)**
2:0	RO	0	**Reserved** Bits [2:1] is programmable; however, it is read as 0.

Offset Address: 0Eh (D0F4)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F4)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F4) – Reserved

Offset Address: 2D-2Ch (D0F4)

Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F4)

Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F4) – Reserved

Offset Address: 34h (D0F4)

Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space 0 indicates the end of the list.

Offset Address: 35-3Fh (D0F4) – Reserved

Offset Address: 40-7Fh (D0F4) – Reserved

Power Management Control (80–EFh)

Offset Address: 80-83h (D0F4) – Reserved

Offset Address: 84h (D0F4)
Central Traffic ControllerPower Management 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Level-1 Host Clock (HCLK) Enable** 0: Free-running clock 1: Dynamic clock
6	RW	0	**Level-1 Global PCI Clock (GCLK, Running at 66MHz) Enable** 0: Free-running clock 1: Dynamic clock
5	RW	0	**Reserved**
4	RW	0	**Down-Stream HCLK Enable** 0: Free-running clock 1: Dynamic clock
3	RW	0	**Down-Stream GCLK Enable** 0: Free-running clock 1: Dynamic clock
2	RW	0	**Reserved**
1	RW	0	**Up-Stream HCLK Enable** 0: Free-running clock 1: Dynamic clock
0	RW	0	**Up-Stream GCLK Enable** 0: Free-running clock 1: Dynamic clock

Offset Address: 85h (D0F4)
Central Traffic ControllerPower Management 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Dynamic Configuration Controller Clock Control for the Register Access** 0: Free-running clock 1: Dynamic clock
1	RW	0	**Reserved**
0	RW	0	**Dynamic Configuration Controller Clock Control for the Register Error Report** 0: Free-running clock 1: Dynamic clock

Offset Address: 86-88h (D0F4) – Reserved

Offset Address: 89h (D0F4)
Graphics-Memory Interface (GMINT) Power Management 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic DRAM Clock Control for GMINTA Request Queue** 0: Free-running clock 1: Dynamic clock
6	RW	0	**Dynamic Push Clock Control for GMINTA Data FIFO** 0: Free-running clock 1: Dynamic clock
5	RW	0	**Dynamic Pop Clock Control for GMINTA Data FIFO** 0: Free-running clock 1: Dynamic clock
4	RW	0	**Dynamic GFX Data Read Ready Clock for GMINTA** 0: Free-running clock 1: Dynamic clock
3	RW	0	**Dynamic Snooping C2M Write Data FIFO Clock for GMINTA Request Queue** 0: Free-running clock 1: Dynamic clock
2:0	RW	0	**Reserved**

Offset Address: 8Ah (D0F4) – Reserved

Offset Address: 8Bh (D0F4)
Data Path Module Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Power Management of CPU-to-Memory (C2M) Read Cycle Data Bus of Channel A (M2AI)** 0: The pipeline of M2AI has free-running clocks. 1: The pipeline of M2AI has dynamic clocks.
6	RW	0	**Reserved**
5	RW	0	**Power Management of C2M Write Data FIFO (CMFIFO)** 0: CMFIFO has free-running clocks. 1: CMFIFO has dynamic clocks.
4	RW	0	**Power Management of C2M Read Data FIFO (MCFIFO)** 0: MCFIFO has free-running clocks. 1: MCFIFO has dynamic clocks.
3	RW	0	**Power Management of CPU-to-Central Traffic Controller (C2P) Write Data FIFO (CPWFIFO)** 0: CPWFIFO has free-running clocks. 1: CPWFIFO has dynamic clocks.
2	RW	0	**Power Management of C2P Read Data FIFO (CPRFIFO)** 0: CPRFIFO has free-running clocks. 1: CPRFIFO has dynamic clocks.
1	RW	0	**Power Management of Central Traffic Controller-to-CPU (P2C) Write Data FIFO (PMWFF)** 0: PMWFF has free-running clocks. 1: PMWFF has dynamic clocks.
0	RW	0	**Power Management of P2C Read Data FIFO (PMRFF)** 0: PMRFF has free-running clocks. 1: PMRFF has dynamic clocks.

Offset Address: 8Ch (D0F4) – Reserved

Offset Address: 8Dh (D0F4)
PMU Related Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Snapshot Mode in C3 State** This bit needs to be set 0 by BIOS if this chip supports DRAM Channel A only. 0: Disable 1: Enable
6	RW	0	**Snapshot Mode in C4 State** This bit needs to be set 0 by BIOS if this chip supports DRAM Channel A only. 0: Disable 1: Enable
5	RW	0	**Self Refresh Mode in C3 State** 0: Disable 1: Enable
4	RW	0	**Self Refresh Mode in C4 State** 0: Disable 1: Enable
3	RW	0	**PLL1 Control** 0: Reset PLL1 1: Turn off PLL1
2	RW	0	**PLL2 Control** 0: Reset PLL2 1: Turn off PLL2
1:0	RW	0	**Reserved**

Offset Address: 8Eh (D0F4)

PMU Related Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Suspend State PLL Always on Option** 0: Suspend State will Reset/Turn_off PLLs 1: Suspend State never Reset/Turn_off PLLs
4	RW	0	**Reserved**
3	RW	0	**Force to Exit Snapshot Mode in C0 State** 0: C0 state will exit Snapshot mode 1: C0 state will force to exit Snapshot mode
2:1	RW	0	**Reserved**
0	RW	0	**Allow Software to Enter Snapshot Mode** 0: Not Allow 1: Allow

Offset Address: 8Fh (D0F4)

PMU Related Register 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RO	0	**Snapshot Mode Is Completed** 0: Not completed 1: Completed
1	RW	0	**Exit Condition of C5 State** 0: NM will exit C5 state when SLP# de-asserts. 1: NM will exit C5 state when LVL5 de-asserts.
0	RW	0	**Enter Condition of C5 State** 0: NM will enter C5 state when LVL5 asserts 1: NM will enter C5 state when LVL5 and SLP# from SM both asserts

Offset Address: 90h (D0F4)

Host Power Management Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPURST# Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active during assertion of CPURST#. 0: Disable 1: Enable
6	RW	0	**GTL Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active during the duration of computing auto-compensation values for GTL pads and power-down GTLCOMP after this process has completed. 0: Disable 1: Enable
5	RW	0	**CPU ADS/ PCI Master Snoop Cycles Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active when CPU issues ADS or PCI master issues snooping cycles. 0: Disable 1: Enable
4	RW	0	**ROMSIP Flip-flops Gate Clock Control** 0: Disable 1: Enable
3	RW	0	**Host Data Transmit DIO & GTL Pads Gate Clock Control** Enable to gate clocks for pad of Host Data, only active when transmitting HD#. 0: Disable 1: Enable
2	RW	0	**Host Address / Request Transmit DIO & GTL Pads Gate Clock Control** Enable to gate clocks for pad of Host Address and request, only active when transmitting HA# / HREQ#. 0: Disable 1: Enable
1	RW	0	**Host Address / Request Receive DIO Gate Clock Control** Enable to gate clocks for pad of Host Address and request , only active when receiving HA# / HREQ# 0: Disable 1: Enable
0	RW	0	**1x Host Signal Transmit DIO & GTL Gate Clock Control** Enable to gate clocks for DIO & GTL pads, only active when transmitting 1X host signals. 0: Disable 1: Enable

Offset Address: 91h (D0F4)

Host Power Management Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Set as 1b for the Case When BREQ0# Always Parks on the Host Bus. (e.g. VIA-Centaur CPU, CN Series) to Invoke Another Power – Saving Technique** 0: Disable 1: Enable
6	RW	0	**C2P Flip-flops Gate Clock Control** Enable to gate clocks for flip-flips, only active for C2P cycles. 0: Disable 1: Enable
5	RW	0	**Defer Queue Request Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active when writing requests to Defer Queue. 0: Disable 1: Enable
4	RW	0	**C2M Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active for C2M cycles. 0: Disable 1: Enable
3	RW	0	**Address Strobe Assertion Gate Clock Control** Enable to gate clock for IOQ entries, only active when ADS1 asserts. 0: Disable 1: Enable
2	RW	0	**Enable to Gate Clock for C2P Request QueueEntries, Only Active When Push Signal of PAQ Asserts** 0: Disable 1: Enable
1	RW	0	**Enable to Gate Clock for Post-Write Queue Entries, Only Active When Push Signal of C2M Write Queue Asserts** 0: Disable 1: Enable
0	RW	0	**Triggering Warm Reset Flip-flops Gate Clock Control** Enable to gate clock for flip-flops, only active for triggering warm reset. 0: Disable 1: Enable

Offset Address: 92h (D0F4)

Host Power Management Registers 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Data Dynamic Input Differential Buffer Control** 0: Disable this function 1: Dynamically enable/disable input differential buffer for HD pad.
6	RW	0	**Host Address / Request Dynamic Input Differential Buffer Control** When turned on, it will observe BREQ0# to dynamically enable/disable input differential buffer for HA#, HREQ# pad. If BREQ0# always parks on FSB (e.g. VIA-Centaur CPU, CN series), please also set Rx91[7] = 1b to invoke another power-saving technique. The suggested value is 1b.
5:4	RW	0	**Reserved**
3	RW	0	**Power Down Input Comparators of AGTL+ Pads of HA#/HREQ#/HLOCK#/BNR#/BREQ0# at PMU C2 State** 0: Disable 1: Enable
2	RW	0	**Power Down Input Comparators of All AGTL+ Pads at PMU C3/C4/S1 State** 0: Disable 1: Enable
1:0	RW	0	**Reserved**

Offset Address: 93-9Fh (D0F4) – Reserved

Offset Address: A0h (D0F4)

Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Power Management** 0: Disable 1: Enable
6:0	RW	0	**Reserved**

Offset Address: A1h (D0F4)
DRAM Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DRAM Self-Refresh During Power-Management Mode** 0: Disable 1: Enable
6	RW	0	**Dynamic CKE When DRAM Idle** 0: Disable 1: Enable Before entering STR mode, please turn off this bit.
5	RW	0	**Dynamic Power Down DRAM I/O Pad (i.e. Float)** 0: Disable 1: Enable
4:0	RW	0	**Reserved**

Note: The DRAM power management mode is defined as HALT / SHUTDOWN, STPCLK and Suspend State triggered.

Offset Address: A2h (D0F4)
Dynamic Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Interface Power Management** 0: Disable 1: Enable
6	RW	0	**DRAM Channel A Interface Power Management** 0: Disable 1: Enable
5	RW	0	**Reserved**
4	RW	0	**DBX Interface Power Management** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**GMINT Power Management** 0: Disable 1: Enable
1	RW	0	**NM Configuration Interface Power Management** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: A3h (D0F4)
MA / SCMD Pad Toggle Reduction **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Toggle Reduction on DRAM MA / SCMD Signals** 0: Disable 1: Enable (i.e. do not switch MA / SCMD signal if not accessed)
6:0	RW	0	**Reserved**

Offset Address: A4-A7h (D0F4) – Reserved

Offset Address: A8h (D0F4)
Central Traffic Controller Dynamic Clock Stop **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Central Traffic Controller Dynamic Clock STOP** 0: Disable 1: Enable
4:0	RW	0	**Reserved**

Offset Address: A9-CFh (D0F4) – Reserved

Offset Address: D7-D0h (D0F4)
BIOS Extended Scratch Registers D - Low **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**BIOS Extended Scratch Registers D - Low**

Offset Address: DF-D8h (D0F4)

BIOS Extended Scratch Registers D - High **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**BIOS Extended Scratch Registers D - High**

Offset Address: E7-E0h (D0F4)

BIOS Extended Scratch Registers E - Low **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**BIOS Extended Scratch Registers E - Low**

Offset Address: EF-E8h (D0F4)

BIOS Extended Scratch Registers E - High **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**BIOS Extended Scratch Registers E - High**

Offset Address: F0-FFh (D0F4) – Reserved

DEVICE 0 FUNCTION 5 (D0F5): APIC AND CENTRAL TRAFFIC CONTROL

PCI Configuration Space

All registers in D0F5 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 5.

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F5)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F5)
Device ID **Default Value: 5409h**

Bit	Attribute	Default	Description
15:0	RO	5409h	**Device ID**

Offset Address: 05-04h (D0F5)
PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RO	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F5)
PCI Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target Abort
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F5)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F5)
Class Code **Default Value: 08 0020h**

Bit	Attribute	Default	Description
23:0	RO	080020h	**Class Code**

Offset Address: 0Ch (D0F5)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D0F5)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F5)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F5)
Build In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 10-2Bh (D0F5) – Reserved

Offset Address: 2D-2Ch (D0F5)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F5)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F5) – Reserved

Offset Address: 34h (D0F5)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space 0 indicates the end of the list.

Offset Address: 35-3Fh (D0F5) – Reserved

Offset Address: 40-4Fh (D0F5) – Reserved

Miscellaneous Control (50–5Fh)

Offset Address: 53-50h (D0F5)

Miscellaneous Control — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Reserved**
1	RW	0	**SM DMA Cycle Pass Normal Memory Cycle Function** 0: Enable 1: Disable
0	RW	0	**Disable the Function of Blocking C2G Cycle When System in SnapShot Mode** 0: Enable. Central Traffic Controller will block C2G cycle when system in SnapShot mode 1: Disable. Central Traffic Controller will not block C2G cycle and will not assert SnapShot wak-up mode when system in SnapShot mode.

Offset Address: 54h (D0F5)

PCCA Arbitration Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Priority to SM Request** 0: Disable 1: Enable
6:4	RW	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 55h (D0F5)

PCCA P2C Promote Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 56-57h (D0F5) – Reserved

Offset Address: 58h (D0F5)

Integrated GFX Arbitration Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GADS from Integrated GFX** 0: Disable 1: Enable
6:4	RW	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 59h (D0F5)

IGFX Promote Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 5A-5Dh (D0F5) – Reserved

Offset Address: 5Eh (D0F5)
IPI Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 5Fh (D0F5)
IPI Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Central Traffic - Downstream Control (60–7Fh)

Offset Address: 60h (D0F5)
Extended CFG Address Support **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**CF8 Byte Write Enable** 0: Only supports CF8 write with all byte-enable active 1: Allows CF8 write with partial byte-enable active
3:2	RW	0	**Reserved**
1:0	RW	00b	**Extended CFG Mode** 00: Extended CFG mode is off 01: Reserved 10: Capability header for extended configuration address supported 11: Memory mapped extended CFG address supported (Rx61 should also be programmed)

Offset Address: 61h (D0F5)
Memory Mapped Extended CFG Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Extended Configuration Address [35:28]** 00h: No extended configuration address Other: Extended configuration address [35:28] from host side

Offset Address: 62-63h (D0F5) – Reserved

Offset Address: 64h (D0F5)

Miscellaneous **Default Value: D2h**

Bit	Attribute	Default	Description
7	RW	1b	**Block P2P Request During Arbiter Disable** 0: Non-block 1: Block
6	RW	1b	**Central Traffic Controller Split GFX 1/8QW Request Into DW Access** 0: Disable 1: Enable
5	RW	0b	**Reserved**
4	RW	1b	**Downstream CPU-to-Central Traffic Controller (C2P) Forces Flush of the Upstream Central Traffic Controller-to-CPU (P2C) Write to the Host Side before Return LRDY to the Host Side** 0: Disable 1: Enable Note: C2P Downstream cycles include MEMR, IOR and IOW
3:2	RW	0	**Reserved**
1	RW	1b	**Downstream Write Request Timing** 0: Wait for the write data to issue downstream request 1: Issue downstream request once request from the host is received
0	RW	0	**Traffic Controller Downstream Cycles Are Processed in Order** 0: Disable. Downstream post write transaction can be issued out before the completion of the data phase of the previous read transaction. 1: Enable. Downstream post write transaction won't be issued out until the data phase of the previous read transaction is finished.

Offset Address: 65-7Fh (D0F5) – Reserved

Central Traffic - Upstream Control (80-85h)

Offset Address: 80h (D0F5)

Central Traffic - Upstream Control 1 **Default Value: 10h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:5	RW	0	**Reserved**
4	RO	1b	**Reserved (Do Not Program)**
3	RW	0	**Upstream Request 1T earlier** 0: Normal latency for upstream request 1: Reduced 1T latency for upstream request
2	RW	0	**Reserved**
1	RW	0	**Host Side Upstream Read Data Returning Path** 0: 2-level synchronous FIFO 1: 1-level synchronous FIFO Set 1 will get better performance. Please set based on the designer suggestion.
0	RW	0	**Host Side Upstream Write, Data Return With a 1T Notice** 0: Disable 1: Enable Set 1 will get better performance. Please set based on the designer suggestion.

Offset Address: 81h (D0F5) – Reserved

Offset Address: 82h (D0F5)

Central Traffic - Upstream Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Traffic Controller Blocks Upstream Requests in C3 Mode** 0: Block all upstream requests (except from SM) until de-assertion of Arbiter Disable. 1: Block all upstream requests (except from SM) until receiving STPCLK# de-assert message..
5:0	RW	0	**Reserved**

Offset Address: 83h (D0F5)
Downstream Arbitration Timeout Timer Control — **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**P2PW (PCI-to-PCI Write) Downstream Arbitration Timeout Timer (* 4 LCLK)** 0000: Occupancy timer is off, i.e. the arbitration will be in a fairly RR scheme. 0001: 4 T 0010: 2 x 4 T ….. 1111: 15 x 4 T (* 4 LCLK) Note: LCLK is a clock name which is equal to Host Clock (HCLK)
3:0	RW	0001b	**P2PR (PCI-to-PCI Read) Downstream Arbitration Timeout Timer (* 4 LCLK)** 0000: Occupancy timer is off, i.e. the arbitration will be in a fairly RR scheme. 0001: 4 T 0010: 2 x 4 T ….. 1111: 15 x 4 T (* 4 LCLK)

Offset Address: 84h (D0F5)
Downstream Control – for the VC1 Paths — **Default Value: 05h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0101b	**Downstream Arbitration Timeout Timer for C2P (* 4 LCLK)** 0000: Occupancy timer is off, i.e. the arbitration will be in a fairly RR scheme. 0001: 4 T 0010: 2 x 4 T ….. 1111: 15 x 4 T (* 4 LCLK)

Offset Address: 85h (D0F5)
P2P Related Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Abort P2P Cycle Issued to PCI1, Discard Write, Return FF for Read** 0: Disable 1: Enable
6	RW	0	**CPU to PCI1 Read Cycle Blocks the Following C2P Cycle** 0: Disable 1: Enable
5:0	RW	0	**Reserved**

Offset Address: 86-9Fh (D0F5) – Reserved

Power Management (A0-FFh)

Offset Address: A0-A1h (D0F5) – Reserved

Offset Address: A2h (D0F5)

PMU Downstream Address [15:8] **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	**Downstream Address Bits [15:8]** This register is used for monitoring S3/S4/S5 downstream command. Refers to RxA3[7] for address [7].

Offset Address: A3h (D0F5)

PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Address Bit [7]** This bit is used for monitoring S3/S4/S5 downstream command. Refers to RxA2 for address [15:8].
6:0	RW	0	**Reserved**

Offset Address: A4-FFh (D0F5) – Reserved

Device 0 Function 6 (D0F6): Scratch Registers

PCI Configuration Space

Scratch registers are registers available for the purpose of software programming.

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F6)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F6)
Device ID **Default Value: 6409h**

Bit	Attribute	Default	Description
15:0	RO	6409h	**Device ID**

Offset Address: 05-04h (D0F6)
PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RO	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F6)
PCI Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F6)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**North Module Chip Revision ID**

Offset Address: 0B-09h (D0F6)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F6) – Reserved

Offset Address: 0Dh (D0F6)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master (In Unit of PCI clocks)**
2:0	RO	0	**Reserved** Bits [2:1] is programmable; however, it’s read as 0

Offset Address: 0Eh (D0F6)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F6)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F6) – Reserved

Offset Address: 2D-2Ch (D0F6)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F6)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F6) – Reserved

Offset Address: 34h (D0F6)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-3Fh (D0F6) – Reserved

Scratch Registers (40-FFh)

Offset Address: 47-40h (D0F6)
BIOS Scratch Register 1 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**BIOS Scratch Register 1**

Offset Address: 4F-48h (D0F6)
BIOS Scratch Register 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**BIOS Scratch Register 2**

Offset Address: 50-7Fh (D0F6) – Reserved

Offset Address: 83-80h (D0F6)

Shadow Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: 87-84h (D0F6)

Shadow Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: 8B-88h (D0F6)

Shadow Registers 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: 8F-8Ch (D0F6)

Shadow Registers 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: 93-90h (D0F6)

Shadow Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: 97-94h (D0F6)

Shadow Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: 9B-98h (D0F6)

Shadow Registers 6 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: 9F-9Ch (D0F6)

Shadow Registers 7 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:26	RW	0	**Reserved**
25	RW	0	**Write Control Bit** If the Write Control bit is enabled, the Write Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Write Cycle. 0: Disable 1: Enable
24	RW	0	**Read Control Bit** If the Read Control bit is enabled, the Read Cycle that hit the 2-byte Trapped Address Register defined in bits [23:8] will cause the 1-byte Correct Data Register defined in bits [7:0] to be changed to the value carried by the Read Cycle. 0: Disable 1: Enable
23:19	RW	0	**Device Number**
18:16	RW	0	**Function Number**
15:8	RW	0	**Register Offset**
7:0	RW	0	**Register Data**

Offset Address: A0-FFh (D0F6) – Reserved

DEVICE 0 FUNCTION 7 (D0F7): NORTH-SOUTH MODULE INTERFACE CONTROL

PCI Configuration Space

All registers in D7F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 7.

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F7)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F7)
Device ID **Default Value: 7409h**

Bit	Attribute	Default	Description
15:0	RO	7409h	**Device ID**

Offset Address: 05-04h (D0F7)
PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RO	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F7)
PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip dose not assert Target-Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed, and Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F7)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F7)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F7)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D0F7)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master (In Unit of PCI Clocks)**
2:0	RO	0	**Reserved** Bits [2:1] are programmable; however, it reads as 0.

Offset Address: 0Eh (D0F7)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F7)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F7) – Reserved

Offset Address: 2D-2Ch (D0F7)

Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F7)

Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F7) – Reserved

Offset Address: 34h (D0F7)

Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space 0 indicates the end of the list.

Offset Address: 35-3Fh (D0F7) – Reserved

North-South Module Interface Control <NSMIC> (40–60h)

Offset Address: 40h (D0F7)

Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:1	RW	00b	**Options of Combining Multiple STPGNT Cycles into NSMIC Command** 00: Compatible mode: a NSMIC command per STPGNT cycle 01: Combines 2 STPGNT cycles into a NSMIC command 10: Combines 3 STPGNT cycles into a NSMIC command 11: Combines 4 STPGNT cycles into a NSMIC command
0	RW	0	**Reserved**

Offset Address: 41-60h (D0F7) – Reserved

Offset Address: 61-6Fh (D0F7) – Reserved

Host-PCI Bridge Control (70-FFh)

Offset Address: 70h (D0F7) – Reserved

Offset Address: 71h (D0F7)

CPU to PCI Flow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Compatible TYPE#1 Configuration Cycle AD31** 0: Fixed AD31 1: AD31 will be 1’b0.
0	RW	0	**Reserved**

Offset Address: 72-75h (D0F7) – Reserved

Offset Address: 76h (D0F7)

PCI Arbitration **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6:0	RW	0	**Reserved**

Offset Address: 77-BFh (D0F7) – Reserved

Offset Address: C7-C0h (D0F7)

Write Data for DRAM Channel-B – Low Bytes **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Write Data for Write Command** Channel B initialization or function test mode write data. Only Supports Interleave Mode

Offset Address: CF-C8h (D0F7)

Write Data for DRAM Channel-B – High Bytes **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Write Data for Write Command** Channel B initialization or function test mode write data. Only Supports Interleave Mode

Offset Address: D7-D0h (D0F7)

Read Data for DRAM Channel-B – Low Bytes **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Returned Data for Read Command** Channel B initialization or function test mode read data. Those are Read-Only Registers. DRAM must be programmed to Interleave Mode

Offset Address: DF-D8h (D0F7)

Read Data for DRAM Channel-B – High Bytes **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Returned Data for Read Command** Channel B initialization or function test mode read data. Those are Read-Only Registers. DRAM must be programmed to Interleave Mode

Offset Address: E0-FFh (D0F7) – Reserved

South Module Legacy Control

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented by using discrete logic on original PC/AT motherboards. All the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All the registers reside in I/O space.

System I/O Ports Map

Port	Function
00-1Fh	**Master DMA Controller**
20-3Fh	**Master Interrupt Controller**
40-5Fh	**Timer / Counter**
60-6Fh	**Keyboard Controller**
(60h)	**KBC Data**
(61h)	**Misc Functions & Speaker Control**
(64h)	**KBC Command / Status**
70-77h	**RTC/CMOS/NMI-Disable**
78-7Fh	**-available for system use**
80h	**-reserved- (debug port)**
81-8Fh	**DMA Page Registers**
90-91h	**-available for system use**
92h	**System Control**
93-9Fh	**-available for system use**
A0-BFh	**Slave Interrupt Controller**
C0-DFh	**Slave DMA Controller**
E0-FFh	**-available for system use**
100-CF7h	**-available for system use**
CF8-CFBh	**PCI Configuration Address**
CFC-CFFh	**PCI Configuration Data**
D00-FFFFh	**-available for system use**

I/O Port Address: 61h

Miscellaneous Functions & Speaker Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**SERR# Status** 0: SERR# has not been asserted 1: SERR# was asserted by a PCI agent Note: This bit is set when the PCI bus SERR# signal is asserted. Once set, this bit may be cleared by setting bit-2 of this register. Bit-2 should be cleared to enable recording of the next SERR# (i.e., bit-2 must be set to 0 to enable this bit to be set).
6	RO	0	**IOCHK# Status** 0: IOCHK# has not been asserted 1: IOCHK # was asserted by an ISA agent Note: This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK# (i.e., bit-3 must be set to 0 to enable this bit to be set). IOCHCK# generates NMI to the CPU if NMI is enabled.
5	RO	0	**Timer/Counter 2 Output** This bit reflects the output of Timer/Counter 2 without any synchronization.
4	RO	0	**Refresh Detected** This bit toggles to reflect timer update on every rising edge of the ISA bus REFRESH# signal.
3	RW	0	**IOCHK# Control** 0: Enable (see bit-6 above) 1: Disable (force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6)
2	RW	0	**SERR# Control** 0: Enable (see bit-7 above) 1: Disable (force SERR# inactive and clear any "SERR# Active" condition in bit-7)
1	RW	0	**Speaker Control** 0: Disable 1: Enable Timer/Counter 2 output to drive SPKR pin
0	RW	0	**Timer/Counter 2 Enable** 0: Disable 1: Enable Timer/Counter 2

I/O Port Address: 92h

System Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**A20 Address Line Enable** 0: A20 disabled / forced 0 (real mode) 1: A20 address line enabled
0	RW	0	**High Speed Reset** 0: Normal 1: Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller I/O Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60h.

A “Control” register is also available. It is accessible by writing commands 20h / 60h to the command port (port 64h); the control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for “Output Buffer Full” status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an “Input Port” and an “Output Port” that control pins dedicated to specific functions. These ports are defined as follows:

Bit	**Input Port**
0	Keyboard Data In
1	Mouse Data In

Bit	**Output Port**
0	System Reset (1 = Execute Reset)
1	Gate A20 (1 = A20 Enabled)
2	Mouse Data Out
3	Mouse Clock Out
6	Keyboard Clock Out
7	Keyboard Data Out

Bit	**Test Port**
0	Keyboard Clock In
1	Mouse Clock In

The above definitions are provided for reference only as actual keyboard and mouse control is no longer performed bit by bit using the above ports but controlled directly by keyboard / mouse controller internal logic. Data is sent and received using the command codes listed on the following page.

I/O Port Address: 60h
Keyboard Controller Input / Output Buffer

Bit	Attribute	Default	Description
7:0	RW	-	**When Write:** **Keyboard Controller Input Buffer** Only write to port 60h if port 64h bit-1 = 0 (1=full). **When Read:** **Keyboard Controller Output Buffer** Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Only write to port 60h if port 64h bit-1 = 0 (1=full).

I/O Port Address: 64h (When Read)
Keyboard / Mouse Status — Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	**Parity Error** 0: No parity error (odd parity received) 1: Even parity occurred on last byte received from keyboard / mouse
6	RO	0	**General Receive / Transmit Timeout** 0: No Error 1: Error
5	RO	0	**Mouse Output Buffer Full** 0: Mouse output buffer empty 1: Mouse output buffer holds mouse data
4	RO	0	**Keylock Status** 0: Locked 1: Free
3	RO	0	**Command / Data** 0: Last write was data write 1: Last write was command write
2	RO	0	**System Flag** 0: Power-On default 1: Self test successful
1	RO	0	**Input Buffer Full** 0: Input buffer empty 1: Input buffer full
0	RO	0	**Keyboard Output Buffer Full** 0: Keyboard output buffer empty 1: Keyboard output buffer full

I/O Port Address: 64h (When Write)
Keyboard / Mouse Command

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by this chip are listed in the table below.

Table 14. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) Value: 00h = OK, 01h = clock stuck low, 02h=clock stuck high, 03h = data stuck low, 04h = data stuck high, FFh = general error
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
C0h	Read Input Port (read input data to output buffer)
C1h	Poll Input Port (read Mouse Data In continuously to status bit 5)
C8h	Unblock Mouse Output (use before D1 to change active mode)
C9h	Reblock Mouse Output (protection mechanism for D1)
CAh	Read Mode (output KBC mode info to port 60 output buffer: bit 0 = 0 if ISA, bit 0 = 1 if PS/2)
D0h	Read Output Port (copy output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit 5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit 5 (write following byte to mouse; put value in mouse input buffer so it appears to have action from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read Keyboard Clock In and Mouse Clock In (return in bits 0-1 respectively of response byte)
Exh	Set Mouse Clock Out per command bit 3 Set Mouse Data Out per command bit 2 Set Gate A20 per command bit 1
Fxh	Pulse Mouse Clock Out low for 6 us per command bit 3 Pulse Mouse Data Out low for 6 us per command bit 2 Pulse Gate A20 low for 6 us per command bit 1 Pulse System Reset low for 6 us per command bit 0

All other codes not listed are undefined.

KBC Control Register (R/W via Commands 20h/60h)

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	1b	**PC Compatibility** 0: Disable scan conversion 1: Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes.
5	RW	0	**Mouse Interface** 0: Enable 1: Disable
4	RW	0	**Keyboard Interface** 0: Enable 1: Disable
3	RO	0	**Reserved**
2	RO	0	**System Flag** This bit may be read back as status register bit-2.
1	RW	0	**Mouse Interrupts** 0: Disable 1: Enable. Generate interrupt on IRQ12 when mouse data comes into output buffer.
0	RW	0	**Keyboard Interrupts** 0: Disable 1: Enable. Generate interrupt on IRQ1 when output buffer has been written.

DMA Controller I/O Registers

I/O Ports Address: 00-0Fh
Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 000x 0000	RW	**Channel 0 Base / Current Address**
0000 0000 000x 0001	RW	**Channel 0 Base / Current Count**
0000 0000 000x 0010	RW	**Channel 1 Base / Current Address**
0000 0000 000x 0011	RW	**Channel 1 Base / Current Count**
0000 0000 000x 0100	RW	**Channel 2 Base / Current Address**
0000 0000 000x 0101	RW	**Channel 2 Base / Current Count**
0000 0000 000x 0110	RW	**Channel 3 Base / Current Address**
0000 0000 000x 0111	RW	**Channel 3 Base / Current Count**
0000 0000 000x 1000	RW	**Status / Command**
0000 0000 000x 1001	WO	**Write Request**
0000 0000 000x 1010	WO	**Write Single Mask**
0000 0000 000x 1011	WO	**Write Mode**
0000 0000 000x 1100	WO	**Clear Byte Pointer**
0000 0000 000x 1101	WO	**Master Clear**
0000 0000 000x 1110	WO	**Clear Mask**
0000 0000 000x 1111	RW	**Read/Write All Mask Bits**

I/O Ports Address: C0-DFh
Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1100 000x	RW	**Channel 4 Base / Current Address**
0000 0000 1100 001x	RW	**Channel 4 Base / Current Count**
0000 0000 1100 010x	RW	**Channel 5 Base / Current Address**
0000 0000 1100 011x	RW	**Channel 5 Base / Current Count**
0000 0000 1100 100x	RW	**Channel 6 Base / Current Address**
0000 0000 1100 101x	RW	**Channel 6 Base / Current Count**
0000 0000 1100 110x	RW	**Channel 7 Base / Current Address**
0000 0000 1100 111x	RW	**Channel 7 Base / Current Count**
0000 0000 1101 000x	RW	**Status / Command**
0000 0000 1101 001x	WO	**Write Request**
0000 0000 1101 010x	WO	**Write Single Mask**
0000 0000 1101 011x	WO	**Write Mode**
0000 0000 1101 100x	WO	**Clear Byte Pointer F/F**
0000 0000 1101 101x	WO	**Master Clear**
0000 0000 1101 110x	WO	**Clear Mask**
0000 0000 1101 111x	WO	**Read/Write All Mask Bits**

Note that not all bits of the address are decoded.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: 80-8Fh

DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (address bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1000 0111	RW	**Channel 0 DMA Page (M-0)**
0000 0000 1000 0011	RW	**Channel 1 DMA Page (M-1)**
0000 0000 1000 0001	RW	**Channel 2 DMA Page (M-2)**
0000 0000 1000 0010	RW	**Channel 3 DMA Page (M-3)**
0000 0000 1000 1111	RW	**Channel 4 DMA Page (S-0)**
0000 0000 1000 1011	RW	**Channel 5 DMA Page (S-1)**
0000 0000 1000 1001	RW	**Channel 6 DMA Page (S-2)**
0000 0000 1000 1010	RW	**Channel 7 DMA Page (S-3)**

DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting D17F0 Rx40 bit[1]. If the shadow registers are enabled, DMA control registers' contents could be read back from the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port Address	Attribute	Description
Port 0	RO	**Channel 0 Base Address**
Port 1	RO	**Channel 0 Byte Count**
Port 2	RO	**Channel 1 Base Address**
Port 3	RO	**Channel 1 Byte Count**
Port 4	RO	**Channel 2 Base Address**
Port 5	RO	**Channel 2 Byte Count**
Port 6	RO	**Channel 3 Base Address**
Port 7	RO	**Channel 3 Byte Count**
Port 8	RO	**1st Read Channel 0-3 Command Register**
Port 8	RO	**2nd Read Channel 0-3 Request Register**
Port 8	RO	**3rd Read Channel 0 Mode Register**
Port 8	RO	**4th Read Channel 1 Mode Register**
Port 8	RO	**5th Read Channel 2 Mode Register**
Port 8	RO	**6th Read Channel 3 Mode Register**
Port F	RO	**Channel 0-3 Read All Mask**
Port C4	RO	**Channel 5 Base Address**
Port C6	RO	**Channel 5 Byte Count**
Port C8	RO	**Channel 6 Base Address**
Port CA	RO	**Channel 6 Byte Count**
Port CC	RO	**Channel 7 Base Address**
Port CE	RO	**Channel 7 Byte Count**
Port D0	RO	**1st Read Channel 4-7 Command Register**
Port D0	RO	**2nd Read Channel 4-7 Request Register**
Port D0	RO	**3rd Read Channel 4 Mode Register**
Port D0	RO	**4th Read Channel 5 Mode Register**
Port D0	RO	**5th Read Channel 6 Mode Register**
Port D0	RO	**6th Read Channel 7 Mode Register**
Port DE	RO	**Channel 4-7 Read All Mask**

Interrupt Controller I/O Registers

This chip integrates two Interrupt Controllers, Master and Slave Interrupt Controllers, either one is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: 21-20h
Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7 and occupies two register locations:

I/O Address Bits 15-0	Attribute	Description
0000 0000 001x xxx0	RW	**Master Interrupt Control**
0000 0000 001x xxx1	RW	**Master Interrupt Mask**

Note that not all bits of the address are decoded.

I/O Ports Address: A1-A0h
Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Attribute	Description
0000 0000 101x xxx0	RW	**Slave Interrupt Control**
0000 0000 101x xxx1	RW	**Slave Interrupt Mask**

Note that not all address bits are decoded.

Interrupt Controller I/O Shadow Registers

The following shadow registers are enabled by setting D17F0 Rx40[1]. If the shadow registers are enabled, Interrupt Controller control registers' contents could be read back from the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

I/O Ports Address: 20h
Master Interrupt Control Shadow

Bit	Attribute	Default	Description
7	RO	-	**Reserved**
6	RO	-	**OCW3 bit 2 for Poll Mode (POLL)**
5	RO	-	**OCW3 bit 0 for Read IS Register (RIS)**
4	RO	-	**OCW3 bit 5 for Special Mask Mode (SMM)**
3	RO	-	**OCW2 bit 7 for Rotation (R)**
2	RO	-	**ICW4 bit 4 for Special Fully Nest Mode (SFNM)**
1	RO	-	**ICW4 bit 1 for Automatic End of Interrupt (AEOI)**
0	RO	-	**ICW1 bit 3 for Level Trigger Mode (LTIM)**

Note: OCW: Operation Command Word; ICW: Initialization Command Word

I/O Ports Address: A0h
Slave Interrupt Control Shadow

Bit	Attribute	Default	Description
7	RO	-	**Reserved**
6	RO	-	**OCW3 bit 2 for Poll Mode (POLL)**
5	RO	-	**OCW3 bit 0 for Read IS Register (RIS)**
4	RO	-	**OCW3 bit 5 for Special Mask Mode (SMM)**
3	RO	-	**OCW2 bit 7 for Rotation (R)**
2	RO	-	**ICW4 bit 4 for Special Fully Nest Mode (SFNM)**
1	RO	-	**ICW4 bit 1 for Automatic End of Interrupt (AEOI)**
0	RO	-	**ICW1 bit 3 for Level Trigger Mode (LTIM)**

Note: OCW: Operation Command Word; ICW: Initialization Command Word

I/O Ports Address: 21h
Master Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RO	-	**T7-T3 of Interrupt Vector Address**

I/O Ports Address: A1h
Slave Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RO	-	**T7-T3 of Interrupt Vector Address**

Timer / Counter I/O Registers

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 010x xx00	RW	**Timer / Counter 0 Count**
0000 0000 010x xx01	RW	**Timer / Counter 1 Count**
0000 0000 010x xx10	RW	**Timer / Counter 2 Count**
0000 0000 010x xx11	WO	**Timer / Counter Command Mode**

Note that not all bits of the address are decoded.

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting D17F0 Rx40[1]. If the shadow registers are enabled, Timer / Counter registers are read back from the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port Address	Attribute	Description
Port 40	RO	**Counter 0 Base Count Value (LSB 1st MSB 2nd)**
Port 41	RO	**Counter 1 Base Count Value (LSB 1st MSB 2nd)**
Port 42	RO	**Counter 2 Base Count Value (LSB 1st MSB 2nd)**

CMOS / RTC I/O Registers

I/O Ports Address: 70h
CMOS Address

Bit	Attribute	Default	Description
7	RW	1b	**NMI Disable** 0: Enable NMI Generation. NMI is asserted on encountering SERR# on the PCI bus. 1: Disable NMI Generation
6:0	RW	-	**CMOS Address** (lower 128 bytes of the CMOS memory)

I/O Ports Address: 71h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Data** (128 bytes of the CMOS memory)

Ports 70-71 may be accessed if D17F0 Rx51[3] is set to one to select the internal RTC. If Rx51[3] is set to zero, accesses to ports 70-71 will be directed to an external RTC.

I/O Ports Address: 74h
CMOS Address

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Address** (256 bytes of the CMOS memory)

I/O Ports Address: 75h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Data** (256 bytes of the CMOS memory)

Ports 74-75 may be accessed only if D17F0 Rx4E[3] (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the "CMOS" block. The RTC control registers are located at specific offsets in the CMOS data area (00-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Table 15. CMOS Register Summary

Offset	Description		
	Register Function	Binary Range	Decimal Range
00	Seconds	00-3Bh	00-59
01	Seconds Alarm	00-3Bh	00-59
02	Minutes	00-3Bh	00-59
03	Minutes Alarm	00-3Bh	00-59
04	Hours	am 12hr: 01-0Ch	01-12
		pm 12hr: 81-8Ch	129-140
		24hr: 00-17h	00-23
05	Hours Alarm	am 12hr: 01-0Ch	01-12
		pm 12hr: 81-8Ch	129-140
		24hr: 00-17h	00-23
06	Day of the Week	Sun=1: 01-07h	01-07
07	Day of the Month	01-1Fh	01-31
08	Month	01-0Ch	01-12
09	Year	00-63h	00-99

Offset	Description: Register Function	Bit Description	
0A	Register A	7: UIP Update In Progress 6:4: DV2-0 Divide (010=Enable oscillator & keep time) 3:0: RS3-0 Rate Select for Periodic Interrupt	
0B	Register B	7: SET Inhibit Update Transfers 6: PIE Periodic Interrupt Enable 5: AIE Alarm Interrupt Enable 4: UIE Update Ended Interrupt Enable 3: SQWE No function (read/write bit) 2: DM Data Mode (0= BCD; 1= Binary) 1: 24/12 Hours Byte Format 0: DSE Daylight Savings Enable	
0C	Register C	7: IRQF Interrupt Request Flag 6: PF Periodic Interrupt Flag 5: AF Alarm Interrupt Flag 4: UF Update Ended Flag 3:0 Unused (always read 0)	
0D	Register D	7: VRT Reads 1 if VBAT voltage is OK 6:0 Unused (always read 0)	
0E-7C	Software-Defined Storage Registers		
Offset	**Extended Function**	**Binary Range**	**Decimal Range**
7D	Date Alarm	01-1Fh	01-31
7E	Month Alarm	01-0Ch	01-12
7F	Century Field	13-14h	19-20

Keyboard / Mouse Wakeup Index / Data Registers

The Keyboard / Mouse Wakeup registers are accessed by performing I/O operations to / from an index / data pair of registers in system I/O space at port addresses 2Eh and 2Fh. The registers accessed using this mechanism are used to initialize Keyboard / Mouse Wakeup functions at index values in the range of E0-EFh.

Keyboard / Mouse Wakeup initialization is accomplished in three steps:
Step 1) Enter KBC initialization mode (set D17F0 Rx51[1] = 1)
Step 2) Initialize the chip
a) Write index to port 2Eh
b) Read / write data from / to port 2Fh
c) Repeat a and b for all desired registers
Step 3) Exit KBC initialization mode (set D17F0 Rx51[1] = 0)

I/O Ports Address: 2Eh
Keyboard Wakeup Index

Bit	Attribute	Default	Description
7:0	RW	0	**Index Value** D17F0 PCI configuration space register Rx51[1] must be set to 1 to enable access to the configuration registers.

I/O Ports Address: 2Fh
Keyboard Wakeup Data

Bit	Attribute	Default	Description
7:0	RW	0	**Data Value**

Keyboard / Mouse Wakeup Registers

These registers are accessed via the port 2E / 2F index / data register paired with D17F0 Rx51[1] = 1 using the indicated index values below.

Index: E0h
Keyboard / Mouse Wakeup Enable **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved** Always reads 0.
4	RO	0	**Reserved**
3	RW	1b	**Win98 Keyboard Power Key Wake-up** 0: Disable 1: Enable
2	RW	0	**Password Wake-up** 0: Disable 1: Enable
1	RW	0	**PS/2 Mouse Wake-up** 0: Disable 1: Enable
0	RW	0	**Keyboard Wake-up** 0: Disable 1: Enable

Index: E1h
Keyboard Wakeup Scan Code Set 0 **Default Value: F0h**

Bit	Attribute	Default	Description
7:0	RW	F0h	**Keyboard Wakeup First Reference Scan Code** Write 00 means that keyboard supports any key wake up.

Index: E2h
Keyboard Wakeup Scan Code Set 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Second Reference Scan Code** Write 00 means that PS/2 mouse supports any key wake up.

Index: E3h
Keyboard Wakeup Scan Code Set 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Third Reference Scan Code**

Index: E4h
Keyboard Wakeup Scan Code Set 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Fourth Reference Scan Code**

Index: E5h
Keyboard Wakeup Scan Code Set 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Fifth Reference Scan Code**

Index: E6h
Keyboard Wakeup Scan Code Set 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Sixth Reference Scan Code**

Index: E7h
Keyboard Wakeup Scan Code Set 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Seventh Reference Scan Code**

Index: E8h
Keyboard Wakeup Scan Code Set 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Eighth Reference Scan Code**

Index: E9h
Mouse Wakeup Scan Code Set 1 **Default Value: 09h**

Bit	Attribute	Default	Description
7:0	RW	09h	**Mouse Wakeup Scan Code Set 1**

Index: EAh
Mouse Wakeup Scan Code Set 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mouse Wakeup Scan Code Set 2**

Index: EBh
Mouse Wakeup Scan Code Mask **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mouse Wakeup Scan Code Mask**

Memory Mapped I/O APIC Registers

The IO APIC registers are accessed by an indirect addressing scheme using Index Registers and Data Registers that are mapped into memory space.

Memory Address: FEC00000h
APIC Index **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	0	**I/O APIC Index** 8-bit pointer to the I/O APIC register.

Memory Address: FEC00010h
APIC Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**I/O APIC Data** This is a 32-bit register for the data to be read or written to the I/O APIC indirect register pointed by the Index Register.

Memory Address: FEC00020h
APIC IRQ Pin Assertion **Default Value: nnh**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	WO	nnh	**IRQ Number** Bit[4:0] written to this register contain the IRQ number for this interrupt. The only valid values are 0-23.

Memory Address: FEC00040h
APIC EOI **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	WO	nnh	**Redirection Entry Clear** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the "Remote_IRR" bit for that I/O Redirection Entry will be cleared.

Indexed I/O APIC Registers

For index registers setting, please refer to Memory Address FEC00000h (APIC Index) and FEC00010 (APIC Data).

Index: 00h
I/O APIC Identification — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RW	0	**I/O APIC Identification** Software must program this value before using the I/O APIC.
23:0	RO	0	**Reserved**

Index: 01h
I/O APIC Version — **Default Value: 0017 8003h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RO	17h	**Maximum Redirection Entry** This value is equal to the number of interrupt input pins for the I/O APIC minus one. For this I/O APIC, the value is 17h.
15	RO	1b	**PCI IRQ** This bit is set to 1 to indicate that this version of the I/O APIC implements the IRQ Assertion register and that PCI devices are allowed to write to it to cause interrupt.
14:8	RO	0	**Reserved**
7:0	RO	03h	**APIC Version** The implementation version for this I/O APIC is 03h.

Index: 02h
I/O APIC Arbitration — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RO	0	**I/O APIC Arbitration ID**
23:0	RO	0	**Reserved**

Index: 03h
Boot Configuration — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Delivery Type** 0: Interrupt Delivery Mechanism is via the APIC Serial Bus. 1: Interrupt Delivery Mechanism is a Front-side Bus Message.

There are 24 64-bit I/O Redirection Table entry registers. Each register is a dedicated entry for each interrupt input signal.

Table 16. I/O Redirection Table

Index	Function	Mnemonic
11-10h	I/O APIC Redirection – APIC IRQ0	IOREDTBL0
13-12h	I/O APIC Redirection – APIC IRQ1	IOREDTBL1
15-14h	I/O APIC Redirection – APIC IRQ2	IOREDTBL2
17-16h	I/O APIC Redirection – APIC IRQ3	IOREDTBL3
19-18h	I/O APIC Redirection – APIC IRQ4	IOREDTBL4
1B-1Ah	I/O APIC Redirection – APIC IRQ5	IOREDTBL5
1C-1Dh	I/O APIC Redirection – APIC IRQ6	IOREDTBL6
1E-1Fh	I/O APIC Redirection – APIC IRQ7	IOREDTBL7
21-20h	I/O APIC Redirection – APIC IRQ8	IOREDTBL8
23-22h	I/O APIC Redirection – APIC IRQ9	IOREDTBL9
25-24h	I/O APIC Redirection – APIC IRQ10	IOREDTBL10
27-26h	I/O APIC Redirection – APIC IRQ11	IOREDTBL11
29-28h	I/O APIC Redirection – APIC IRQ12	IOREDTBL12
2B-2Ah	I/O APIC Redirection – APIC IRQ13	IOREDTBL13
2D-2Ch	I/O APIC Redirection – APIC IRQ14	IOREDTBL14
2F-2Eh	I/O APIC Redirection – APIC IRQ15	IOREDTBL15
31-30h	I/O APIC Redirection – APIC IRQ16	IOREDTBL16
33-32h	I/O APIC Redirection – APIC IRQ17	IOREDTBL17
35-34h	I/O APIC Redirection – APIC IRQ18	IOREDTBL18
37-36h	I/O APIC Redirection – APIC IRQ19	IOREDTBL19
39-38h	I/O APIC Redirection – APIC IRQ20	IOREDTBL20
3B-3Ah	I/O APIC Redirection – APIC IRQ21	IOREDTBL21
3D-3Ch	I/O APIC Redirection – APIC IRQ22	IOREDTBL22
3F-3Eh	I/O APIC Redirection – APIC IRQ23	IOREDTBL23

I/O Redirection Entry **Default Value: nnn1 nnnn nnnn nnnnh**

Bit	Attribute	Default	Description
63:56	RW	nnh	**Destination Field** In Physical Mode (bit-11=0), bits [59:56] contain an APIC ID. In Logical Mode (bit-11=1), bits [63:56] of the Destination Field specify the logical destination address. Destination Mode IOREDTBLx[11] — Logical Destination Address 0: Physical Mode — IOREDTBLx[59:56] = APIC ID 1: Logical Mode — IOREDTBLx[63:56] = Set of processors
55:17	RO	0	**Reserved**
16	RW	0	**Interrupt Mask** 0: Not Mask 1: Masked
15	RW	0	**Trigger Mode** Indicates the type of signal on the interrupt pin that triggers an interrupt. 1: Level Sensitive 0: Edge Sensitive
14	RO	0	**Remote Interrupt Request Register (IRR)** This bit is used for level triggered interrupts. Its meaning is undefined for edge triggered interrupts. For level triggered interrupts, this bit is set to 1 when local APIC(s) accept the level interrupt sent by the IOAPIC. 0: EOI message with a matching interrupt vector is received from a local APIC 1: Level sensitive interrupt sent by IOAPIC accepted by local APIC(s)
13	RW	0	**Interrupt Input Pin Polarity** Specifies the polarity of the interrupt signal. 0: High active 1:Low active
12	RO	0	**Delivery Status** Contains the current status of the delivery of this interrupt. 0: Idle (there is currently no activity for this interrupt.) 1: Send Pending (the interrupt has been injected but its delivery is temporarily held either because the APIC bus is busy or because the receiving APIC unit can not currently accept the interrupt.)
11	RW	0	**Destination Mode** Determines the interpretation of the Destination field. 0: Physical Mode 1: Logical Mode
10:8	RW	000b	**Delivery Mode** Specify how the APICs listed in the destination field should act upon reception of this signal. 000: Fixed 001: Lowest Priority 010: SMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	RW	nnh	**Interrupt Vector** Contain the interrupt vector for this interrupt. Vector values range from 10h to FEh.

Indexed I/O UART DMA Control Registers

The base address is located at D17F0 RxB8[15:0] and through D17F0 RxB7[3] to enable or disable access.

Index: 00h
UART Port 1 DMA Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0.
5	RW	0	**COM1 Transmit Using High Performance Way with DMA** 0: Disable 1: Enable
4	RW	0	**COM1 Receive Using High Performance Way with DMA** 0: Disable 1: Enable
3	RW	0	**Generate Interrupt for COM1 Transmit Complete** 0: The interrupt signal of COM1 will not be active even the Index 01h[1] is set. 1: The interrupt signal of COM1 will be active if the Index 01h[1] is set.
2	RW	0	**Generate Interrupt for COM1 Receive Complete** 0: The interrupt signal of COM1 will not be active even the Index 01h[0] is set. 1: The interrupt signal of COM1 will be active if the Index 01h[0] is set.
1	RW	0	**COM1 Use DMA to Transmit Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM1 will not issue any DMA request for transmit data from memory to peripheral. 2) COM1 will ignore DMA acknowledge for its transmit. 3) Index 01h[1] will be cleared. When set as 1, it will be: 1) COM1 will issue DMA request for transmit data from memory to peripheral when COM1 transmit FIFO is available. 2) COM1 will respond to DMA acknowledge for data transmit.
0	RW	0	**COM1 Use DMA to Receive Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM1 will not issue any DMA request for transmit data from peripheral to memory. 2) COM1 will ignore DMA acknowledge for its receive. 3) Index 01h[0] will be cleared. When set as 1, it will be: 1) COM1 will issue DMA request for receive data from peripheral to memory when COM1 receive FIFO is available. 2) COM1 will respond to DMA acknowledge for data receive.

Index: 01h
UART Port 1 DMA Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved** Always reads 0.
1	RW	0	**Status of Interrupt for COM1 Transmit Complete** 0: The DMA for transmit of COM1 has not finished yet. 1: The DMA for transmit of COM1 has finished. Write 1 or disable Index 00h[1] to clear.
0	RW	0	**Status of Interrupt for COM1 Receive Complete** 0: The DMA for receive of COM1 has not finished yet. 1: The DMA for receive of COM1 has finished. Write 1 or disable Index 00h[0] to clear.

Index: 02h
UART Port 2 DMA Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0.
5	RW	0	**COM2 Transmit Using High Performance Way with DMA** 0: Disable 1: Enable
4	RW	0	**COM2 Receive Using High Performance Way with DMA** 0: Disable 1: Enable
3	RW	0	**Generate Interrupt for COM2 Transmit Complete** 0: The interrupt signal of COM2 will not be active even the Index 03h[1] is set. 1: The interrupt signal of COM2 will be active if the Index 03h[1] is set.
2	RW	0	**Generate Interrupt for COM2 Receive Complete** 0: The interrupt signal of COM2 will not be active even the Index 03h[0] is set. 1: The interrupt signal of COM2 will be active if the Index 03h[0] is set.
1	RW	0	**COM2 Use DMA to Transmit Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM2 will not issue any DMA request for transmit data from memory to peripheral. 2) COM2 will ignore DMA acknowledge for its transmit. 3) Index 03h[1] will be cleared. When set as 1, it will be: 1) COM2 will issue DMA request for transmit data from memory to peripheral when COM2 transmit FIFO is available. 2) COM2 will respond to DMA acknowledge for data transmit.
0	RW	0	**COM2 Use DMA to Receive Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM2 will not issue any DMA request for transmit data from peripheral to memory. 2) COM2 will ignore DMA acknowledge for its receive. 3) Index 03h[0] will be cleared. When set as 1, it will be: 1) COM2 will issue DMA request for receive data from peripheral to memory when COM2 receive FIFO is available. 2) COM2 will respond to DMA acknowledge for data receive.

Index: 03h
UART Port 2 DMA Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved** Always reads 0.
1	RW	0	**Status of Interrupt for COM2 Transmit Complete** 0: The DMA for transmit of COM2 has not finished yet. 1: The DMA for transmit of COM2 has finished. Write 1 or disable Index 02h[1] to clear.
0	RW	0	**Status of Interrupt for COM2 Receive Complete** 0: The DMA for receive of COM2 has not finished yet. 1: The DMA for receive of COM2 has finished. Write 1 or disable Index 02h[0] to clear.

When enabling high performance on Tx, it can transfer 16 bytes on one request for DMAC if transmit FIFO is empty, and it can gain much more performance with demand transfer mode and line buffer enabled.
When disabling high performance on Tx, it only transfers 1 byte of single transfer mode and 2 bytes of demand transfer mode on one request for DMAC if transmit FIFO is empty.
When enabling high performance on Rx, it will transfer all data in FIFO when receiver buffer trigger point reached or timeout and it can gain much more performance with demand transfer mode and line buffer enabled.
When disabling high performance on Rx, it will transfer data whenever receive data is not empty.

DEVICE 11 FUNCTION 0 (D11F0): USB DEVICE

This chip can work as a mass storage USB device. Four endpoints are supported, they are: Control endpoint, Bulk In endpoint, Bulk Out endpoint and Interrupt In endpoint.

PCI Configuration Space

All registers in D11F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 11 and function number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D11F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D11F0)
Device ID **Default Value: A409h**

Bit	Attribute	Default	Description
15:0	RO	A409h	**Device ID Code** Fixed at A409h if Rx41[1] = 0.

Offset Address: 05-04h (D11F0)
PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidation Enable** 0: Disable 1: Enable
3	RO	0	**Reserved**
2	RW	0	**Bus Master**
1	RW	0	**Memory Space**
0	RW	0	**I/O Space**

Offset Address: 07-06h (D11F0)
PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8:0	RO	010h	**Fixed at 10h (for PCI PMI)**

Offset Address: 08h (D11F0)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D11F0)
Class Code **Default Value: 02 8000h**

Bit	Attribute	Default	Description
23:0	RO	028000h	**Class Code** 028000h indicates other network controllers.

Offset Address: 0Ch (D11F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D11F0)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Latency Timer**

Offset Address: 0Eh (D11F0)
Header Type Default **Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D11F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 0.

Offset Address: 13-10h (D11F0)
VIACOM MMIO Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RW	0	**Corresponding to AD[31:11]**
10:3	RO	0	**Reserved**
2:1	RO	0	**Memory Mapping** 00: 32-bit space 01: 64-bit space Others: Reserved
0	RO	0	**Reserved**

Offset Address: 14-2Bh (D11F0) – Reserved

Offset Address: 2D-2Ch (D11F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D11F0)

Subsystem ID **Default Value: A409h**

Bit	Attribute	Default	Description
15:0	RO	A409h	**Subsystem ID**

Offset Address: 30-33h (D11F0) – Reserved

Offset Address: 34h (D11F0)

Power Management Capability **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Power Management Capability** Fixed at 80h.

Offset Address: 35-3Bh (D11F0) – Reserved

Offset Address: 3Ch (D11F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**USB Interrupt Routing** The high 4 bits have no effect. 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disabled

Offset Address: 3Dh (D11F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Offset Address: 3E-3Fh (D11F0) – Reserved

USB PHY And MAC Control (40-7Fh)

Offset Address: 40h (D11F0)
Debug Signal Control Register — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:1	RW	000b	**Debug Signal Group Select** 000: Endpoint 0 DMA debug signal 001: Endpoint 1 DMA debug signal 010: Endpoint 2 DMA debug signal 011: Endpoint controller debug signal 100: PHY debug signal 101: HS MAC debug signal 110: FS MAC debug signal 111: Port state debug signal
0	RW	0	**Debug Signal Enable** 0: Disable 1: Enable

Offset Address: 41h (D11F0)
Backdoor Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Backdoor Enable and Value Write Enable** 0: Rx41[3:1], Rx5C-5E and Rx60-65 are read only 1: These registers are writable
3	RW	0	**Subsystem ID and Subsystem Vendor ID Backdoor Enable** 0: Disable 1: Enable When this bit is set, the values read from Rx2F-2C are exactly the ones of Rx63-60.
2:0	RW	0	**Reserved**

Offset Address: 42h (D11F0)
Miscellaneous Control 1 — **Default Value: 24h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:0	RW	24h	**USB 1.1 Full Speed (FS) Timeout Parameter** In FS mode, this register is used to control timeout period with the 80ns unit.

Offset Address: 43h (D11F0)
PHY Signal Monitoring 1 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**15K Pull-up Resistor Enable** This bit enables the connection of 15K pull-up resistor and is valid if bit 5 is set. 0: Disconnect 1: Connect
6	RW	0	**45-Ohm Termination Resistor Enable** This bit enables the connection of 45-ohm termination resistor and is valid if bit 5 is set. 0: Disconnect 1: Connect
5	RW	0	**PHY Resistor Manual Control Enable** This bit enables the control of 45-ohm termination resistor and 15K pull-up resistor via software instead of hardware. 0: Hardware auto mode 1: Manual mode
4	RW	0	**Enable Switch2 Pull-Up** 0: Disconnect switch2 pull-up resistor 1: Connect switch2 pull-up resistor
3:2	RW	00b	**PULL_ON_SW2 Type Select** 00: Connect switch2 pull-on resistor when bus signal changes from 1 to 0 01: When active (from 1 to 0 or 0 to 1) 10: Always disconnect 11: Always connect
1	RW	0	**Reserved**
0	RW	0	**Device Port PHY Signal Monitor Enable** 0: Disable 1: Enable

Offset Address: 44h (D11F0)
PHY Signal Monitoring 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**RxData** 0: RxData = 0 1: RxData = 1
2	RO	0	**Squelch** 0: No squelch 1: Detect squelch
1	RO	0	**TermON** 0: USB bus is term off 1: USB bus is term on
0	RO	0	**PullupResON** 0: USB bus not pulled-on 1: USB bus is pulled-on

Offset Address: 45h (D11F0)
Miscellaneous Control 2 **Default Value: A0h**

Bit	Attribute	Default	Description
7	RW	1b	**USB 2.0 EOP Pattern/PHY Data Buffer Error Check Disable** 0: Enable check 1: Disable check
6	RW	0	**Reserved**
5	RW	1b	**Disable CCA Burst Access** 0: Burst enabled 1: Burst disabled
4	RW	0	**Sync-Fast Option** 0: Disable 1: Enable
3	RW	0	**Sync-Jend Option** 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: 46h (D11F0)
Miscellaneous Control 3 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Clock Auto-Stop Enable** 0: Disable auto-stop 1: Enable auto-stop
6	RW	0	**CRC Received Token Check** 0: Enable check 1: Disable check
5	RW	0	**Hardware Auto-Reset Device Address on USB Reset** 0: Auto reset device address 1: Not reset
4:1	RW	0	**Reserved**
0	RW	0	**USB Transceiver Macrocell (UTM) Auto-Check Enable** 0: Disable 1: Enable

Offset Address: 47h (D11F0)
Miscellaneous Control Register 4 **Default Value: 38h**

Bit	Attribute	Default	Description
7:4	RW	3h	**Pull up Resistor Fine Tune (No Effect)**
3:0	RW	8h	**Termination Resistor Fine Tune**

Offset Address: 48-49h (D11F0) – Reserved

Offset Address: 4Ah (D11F0)
MAC Turn Around Time **Default Value: 09h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	9h	**USB 2.0 MAC Transmit Turn Around Time** High Speed turn around time with the 16ns unit.

Offset Address: 4Bh (D11F0)
High Speed (HS) MAC Receiver Delay Control **Default Value: 61h**

Bit	Attribute	Default	Description
7:4	RW	6h	**Receiver Delay Time After TX Packet (Unit: 16ns)**
3:0	RW	1h	**Receiver Delay Time Between Two Consecutive Rx Packets (Unit: 16ns)**

Offset Address: 4Ch (D11F0)
Function Patch Enable **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**LS Packet Cause FS Packet Timeout Error Patch** 0: Disable 1: Enable
5	RW	1b	**Hardware Attach Process Evaluation Enable** 0: Disable 1: Enable
4	RW	0	**Bulk Endpoint NYET Response Enable** The NYET is a token defined by USB 2.0 spec to indicate device busy. 0: Disable 1: Enable
3	RW	0	**USB 1.1 EOP Issue Patch Disable** 0: Enable patch 1: Disable patch
2	RW	1b	**Force RXACTIVE to Deassert on BABBLE Occur to Prevent System Hang** 0: Disable 1: Enable
1	RW	0	**Disable Patch Unsafe BULK DMA Pause** 0: Enable 1: Disable
0	RW	1b	**CRC16 Even Data Toggle Mismatch Check Enable** 0: Disable 1: Enable

Offset Address: 4Dh (D11F0)
Test Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Enable Eye-Pattern Test Mode** Set this bit to generate continuously toggled pattern to FS test for eye-pattern characterization. 0: Disable 1: Enable
4	RO	0	**UTM Error Auto Check** This bit indicates UTM auto check in loop-back mode error status. 0: No error found 1: Data check error
3	RW	0	**HS Eye Test** 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: 4Eh (D11F0)
USB 2.0 MAC Timeout **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RW	60h	**USB 2.0 Receive Timeout Parameter** The unit is byte time. According to the core spec, the host controller or a device expecting a response to a transmission must not timeout the transaction if the inter-packet delay is within 736 and 816 bit times. The worst round trip delay is 721 bit times.

Offset Address: 4Fh (D11F0)
PHY Control 1 **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RW	00b	**External Current Source Increment** 00: No increment 01: 1% 10: 2 % 11: 4%
5:4	RW	10b	**125mv Squelch Level Fine Tune** 00: 100mv 01: 112.5mv 10: 125mv 11: 137.5mv
3	RW	0	**PLLTEST Output** 0: 48MHz 1: 60MHz
2	RW	0	**HS Transmitter** Used for HS transmitter, no DPLL. 0: Normal 1: Rise / fall time increase 100ps
1:0	RW	00b	**DPLL Input Data Delay Select** 00: 0ps 01: -43~-135ps 10: 43~135ps 11: 86~270ps

Offset Address: 50h (D11F0)
PHY Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reset DPLL for BIST** 0: No work 1: Reset
6	RW	0	**Different Test Pattern for DPLL BIST** 0: Off 1: 1T pulse-shift
5	RW	0	**Different Test Pattern for DPLL BIST** 0: Off 1: 1T duty-offset
4	RW	0	**Different Test Pattern for DPLL BIST** 0: Off 1: 1T phase shift
3	RW	0	**DPLL Receive Data Out (RDOUT[4:0]) Output Enable** 0: Disable 1: Enable
2	RO	0	**DPLL BIST Pattern Match Flag** 0: Error 1: Success
1	RW	0	**FS Tx Test** 0: Disable 1: Enable
0	RO	0	**FS Rx Test** 0: Disable 1: Enable

Offset Address: 51h (D11F0)
PHY Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**DPLL Test Mode Observed Signals (RDOUT[4:0])** Rx51[7:3] are valid only when Rx50[3] is set.
2:1	RW	0	**Reserved**
0	RO	0	**Reserved**

Offset Address: 52h (D11F0)
PHY Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Device Suspend Disable** For test purpose. 0: Normal mode 1: Disable suspend
5:4	RW	0	**Reserved**
3	RW	0	**DPLL Loopback Enable** 0: Disable 1: Enable
2	RW	0	**HS Transmission Test**
1:0	RW	0	**Reserved**

Offset Address: 53h (D11F0)

PHY Control 5 **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**PHY Auto Power-down Disable** If this bit is asserted, and when the port is suspended, the port will auto power-down. 0: Auto power-down 1: Disable auto power-down
6:3	RW	0001b	**Reserved (Do Not Program)**
2	RW	0	**PHY APLL Auto Power Down Enable** 0: Disable 1: Enable
1:0	RW	00b	**DPLL Non-Squelch (NSQ) Offset Set Reg** 00: 0ps 01: -43~-135ps 10: 43~135ps 11: 86~270ps

Offset Address: 54h (D11F0)

PHY Control 6 **Default Value: 17h**

Bit	Attribute	Default	Description
7	RW	0	**Input Data Control (FASTSTART)** 0 Disable 1 Enable
6:5	RW	0	**Reserved**
4	RW	1b	**Fast Lock** 0: Disable 1: Enable
3:2	RW	01b	**DPLL Track Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)
1:0	RW	11b	**DPLL Lock Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)

Offset Address: 55h (D11F0)

New USB 1.1 and USB 2.0 PHY Test Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**HS Test Enable** 0: Disable 1: Enable
4	RW	0	**USB 2.0 Test Packet External Input Mode Enable** 0: Disable 1: Enable
3	RW	0	**USB 2.0 Test Packet Auto Compare Enable** 0: Disable 1: Enable
2:0	RW	000b	**Test Packet Mode** 000: Disable 100: USB 2.0 test packet mode 101: Incremental data of 16 bytes index starting from 0 110: Incremental data of 256 bytes index starting from 0 111: Incremental data of 1024 bytes index starting from 0

Offset Address: 56h (D11F0)

New USB 1.1 and USB 2.0 PHY Test Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**USB2.0 Auto Compare Data Detect Status** 0: No data 1: Data detected
2	RO	0	**USB2.0 Auto Compare Error Status** 0: No error 1: Rx/Tx data compare error
1	RO	0	**USB2.0 Auto Compare Timeout Error Status** 0: No error 1: Timeout error in receiving Rx data
0	RO	0	**USB2.0 Auto Compare EOP Error Status** 0: No error 1: Unable to detect Rx data EOP

Offset Address: 57-5Fh (D11F0) – Reserved

Offset Address: 61-60h (D11F0)
Subsystem ID Back Door **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	**Subsystem ID Back Door** When Rx41[3] is set to 1, the value read from Rx2F-2E is exactly the one of Rx61-60.

Offset Address: 63-62h (D11F0)
Subsystem Vendor ID Backdoor **Default Value: A409h**

Bit	Attribute	Default	Description
15:0	RW	A409h	**Subsystem Vendor ID Back Door** When Rx41[3] is set to 1, the value read from Rx2D-2C is exactly the ones of Rx63-62.

Offset Address: 64-7Fh (D11F0) – Reserved

USB Power Management (80-8Fh)

Offset Address: 80h (D11F0)
USB Device Power Management Capabilities ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**USB Device Power Management Capabilities ID**

Offset Address: 81h (D11F0)
Next Linked Item **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Linked Item**

Offset Address: 83-82h (D11F0)
Power Management Capabilities **Default Value: 7E02h**

Bit	Attribute	Default	Description
15:0	RO	7E02h	**Power Management Capabilities**

Offset Address: 85-84h (D11F0)
Power Management Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME Status** 0: De-active 1: Active
14:9	RO	0	**Reserved**
8	RW	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00: D0 01: D1 10: D2 11: D3 For PHY, D0~D3 states are the same. Power will shut down and be disconnected in D3 state.

Offset Address: 86-FFh (D11F0) – Reserved

VIA USB Device Memory-Mapped I/O Registers (USBD-MMIO)

VIA USB Communication Capability and Shadow Registers (00-0Fh)

Offset Address: 00h (USBD-MMIO)

Capability Register **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Capability Register Length**

Offset Address: 01h (USBD-MMIO)

Interface Version **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Interface Version Number**

Offset Address: 02-0Fh (USBD-MMIO) – Reserved

VIA USB Device Controller Operational Registers (10-1Fh)

Offset Address: 13-10h (USBD-MMIO)

Controller Register **Default Value: 0020 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Device Address Change** On change device address, this bit must be set for status phase decoding. This bit is cleared by hardware when next setup command is received. When this bit is 1, hardware will decode both old address and the newly changed address. Note that when modifying the device address, this bit must also be set.
30:24	RW	0	**Device Address** These bits specify the device address. Default value is 00h. These bits are reset to default value on receiving USB bus reset when D11F0 Rx46[5] is 1. This bit is also programmed by software after address setup procedure completes.
23	RW	0	**Manual Control for PHY Power** 0: Hardware control 1 Manual control
22	RW	0	**PHY Power On** 0: Power off 1: Power on This bit is valid only when bit 23 is 1b.
21	RO	1b	**Self-Powered Device** If the device is in self-powered configuration, set this bit to one for connection determination. 0: Bus-powered 1: Self-powered
20	RW	0	**HS / FS Support** 0: HS supported 1: FS supported This bit disables the device controller high-speed support; default is set to support high-speed.
19	RW	0	**Device Force Resume** This bit forces the suspended device port to issue resume signal to wakeup the host, and the hardware clears this bit automatically after software set this bit. Set this bit must check the suspension status first.
18	RW	0	**Software Ready** 0: Not ready 1: Ready
17	RW	0	**Controller Reset** Write a one to this bit resets device controller. This bit is set to zero by controller when reset process is complete.
16	RW	0	**Run/Stop** Set this bit enables device controller operation, including Host/Device negotiation and endpoint DMA 0: Stop 1: Run
15	RW	0	**PIO Enable** 0: Disable 1: Enable
14	RW	0	**Prevent the System Entering from C1~C4 States** 0: Disable 1: Enable
13:0	RO	0	**Reserved**

Offset Address: 15-14h (USBD-MMIO)
Device Status Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RW1C	0	**Device Port Bus Resume Detected** This bit indicates that the controller has detected bus host resume. 0: No resume detected 1: Host resume detected
6	RW1C	0	**Device Port Bus Suspend Detected** This bit indicates that the controller has detected bus suspend. 0: No suspend detected 1: Bus suspend detected
5	RW1C	0	**Device Reset** This bit is set by the controller if the USB bus reset is detected. 0: No reset 1: Reset
4	RO	0	**Reserved**
3	RW1C	0	**Controller System Error** The controller sets this bit to a one when a serious error occurs during a system access. If this bit is set, the controller also clears Run/Stop bit and sets halted bit. 0: No error 1: System error
2	RO	0	**Reserved**
1	RO	0	**FS Mode Status** This bit indicates if the device is in USB 1.1 FS mode. 0: Not in FS mode 1: FS mode
0	RO	0	**High-Speed Mode Status** This bit indicates if the device is in USB 2.0 High-Speed mode. 0: Not in High-Speed mode 1: High-Speed mode

Offset Address: 17-16h (USBD-MMIO)
Device Port Control / Status Register **Default Value: 0200h**

Bit	Attribute	Default	Description
15:13	RW	000b	**Port Test Control – R/W** 000: Test mode not enabled 001: Test J_STATE 010: Test K_STATE 011: SE0_NAK 100: Test Packet 101: Test FORCE_ENABLE 110: Test Chirp J 111: Test Chirp K
12:10	RO	0	**Reserved**
9:8	RO	10b	**Bus Line Status** These bits correspond to USB bus signals [D+: D-] with bit [9:8].
7:2	RO	0	**Reserved**
1	RW1C	0	**Connection Change** This bit is set if bit 0 state changes. This bit is valid if bit 2 is set. 0: No change 1: Status changed
0	RO	0	**Current Connection Status** This bit indicates current connection status and is valid only when bit 2 is set. 0: No connect 1: Connected

Offset Address: 19-18h (USBD-MMIO)
Device Interrupt Status Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3	RO	0	**Descriptor Error Interrupt Enable** 0: Disable 1: Enable
2	RW1C	0	**Bus Activities Interrupt** The controller sets this bit when any USB bus activities interrupt is generated. The bus activities include bus reset, bus suspend, and bus resume. 0: No bus activities events 1: Bus activities events occur
1	RO	0	**Babble Interrupt** The controller set this bit to a one when packet babble received. 0: No babble 1: Babble received
0	RO	0	**Complete Interrupt** The controller sets this bit on transfer completion. Software can clear the interrupts from all endpoints to clear this bit. 0: No interrupt 1: Transfer completed

Offset Address: 1B-1Ah (USBD-MMIO)
Device Interrupt Enable Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3	RW	0	**Descriptor Error Interrupt Enable**
2	RW	0	**Bus Activities Interrupt Enable** When this bit is set, controller will generate interrupt if any bus activities occur. 0: Disable 1: Enable
1	RW	0	**Babble Interrupt Enable** When this bit is set, controller will generate interrupt if packet babble error occurs. 0: Disable 1: Enable
0	RW	0	**Complete Interrupt Enable** When this bit is set, controller will generate interrupt on transfer completion. 0: Disable 1: Enable

Offset Address: 1D-1Ch (USBD-MMIO)
Force Interrupt Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW	0	**Force Bus Active Interrupt to be Asserted** 0: Disable 1: Enable
7	RW	0	**Force End Point 3 Interrupt of Complete (IOC)** 0: Disable 1: Enable
6	RW	0	**Force End Point 2 Descriptor Error** 0: Disable 1: Enable
5	RW	0	**Force End Point 2 Interrupt of Complete (IOC)** 0: Disable 1: Enable
4	RW	0	**Force End Point 1 Descriptor Error** 0: Disable 1: Enable
3	RW	0	**Force End Point 1 Babble Interrupt to be Asserted** 0: Disable 1: Enable
2	RW	0	**Force End Point 1 Interrupt of Complete (IOC)** 0: Disable 1: Enable
1	RW	0	**Force End Point 0 Babble** 0: Disable 1: Enable
0	RW	0	**Force End Point 0 Interrupt of Complete (IOC)** 0: Disable 1: Enable

Offset Address: 1E-1Fh (D11F0) – Reserved

VIA USB Device Endpoint Controller Operational Registers (20-2Fh)

Offset Address: 23-20h (USBD-MMIO)
Endpoint 0 Status and Control Register **Default Value: 0040 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Endpoint Number** This field stores this endpoint's ID number. Note that this field of the control endpoint is fixed to zero, and only least two bits are writable since only four endpoints are implemented in this design.
27	RW	0	**DMA Reset** Set this bit to reset DMA to initial idle state. Once the reset is finished by hardware, this bit will clear to 0 automatically.
26:16	RW	040h	**Endpoint Max Packet Size (Bytes)** This field specifies the maximum packet size of this endpoint. This value must not exceed: 8: Interrupt endpoint and the attribute is RO 64: Control endpoint 512: Bulk endpoint
15	RW1C	0	**Endpoint Received an Error Descriptor Interrupt** Hardware set this bit when it gets an error descriptor, also controller will generate interrupt.
14	RW1C	0	**Endpoint Received Packet Babble Interrupt** Controller sets this bit when it receives packet babble if schedule has its IOC bit set. If interrupt enabled, controller will also generate interrupt. 0: No interrupt 1: Interrupt event
13	RW1C	0	**Endpoint Transfer Completion Interrupt** Controller sets this bit when it completes transfer if schedule has its IOC bit set. If interrupt enabled, controller will also generate interrupt. 0: No interrupt 1: Interrupt event
12	RO	0	**Endpoint DMA Engine Active Status** This bit is set by endpoint controller if it starts DMA engine including USB bus and PCI bus traffics and is cleared if DMA process completes. When this bit is set, software must not modify the pointed related data buffer.
11	RO	0	**DMA Need Reset** 0: Control data DMA don't need reset 1: Control data DMA need reset When meet complete interrupt, check this bit, if it is 1, issue a DMA reset for this endpoint. Other endpoint always 0
10	RO	0	**Reserved**
9:8	RO	0	**Index of the Next Descriptor would Deal (NEXTDES)**
7:6	RO	0	**Index of the Last Descriptor would Deal (ENDDES)**
5:4	RO	0	**Index of Current Descriptor (CURDES)**
3	RW	0	**Endpoint Stalled** This bit stalls this endpoint. If set this bit, the DMA engine may halt at once and will return STALL handshake to USB bus query. The endpoint controller also sets this bit if DMA engine encounters serious error.
2	RW	0	**Endpoint Light Reset** If this bit is set, this endpoint will be reset to initial condition except the endpoint number and maximum packet size. Software should wait this bit goes to zero before any further operations. 0: Not reset 1: Endpoint light reset
1	RW	0	**Endpoint DMA Engine Enable** Set this bit activates endpoint DMA engine. Software may disable DMA engine by clear this bit to remove schedule. Software must check DMA active status goes to zero before remove or modify the schedule. 0: Disable 1: Enable
0	RW	0	**Endpoint Run/Stop** When set to a one, the endpoint controller starts executing the specified descriptor. If set to zero, the controller will not respond to any USB host packets. If serious error occurs, controller also clears this bit. 0: Stop 1: Run

Offset Address: 27-24h (USBD-MMIO)
Bulk Out Endpoint Control and Status **Default Value: 1200 0100h**

Bit	Attribute	Default	Description
31:0	RW	1200 0100h	**Bulk Out Endpoint Control and Status** Maximum packet size is 512 bytes. The rest definitions are same as control endpoint.

Offset Address: 2B-28h (USBD-MMIO)
Bulk In Endpoint Control and Status **Default Value: 2200 0100h**

Bit	Attribute	Default	Description
31:0	RW	2200 0100h	**Bulk In Endpoint Control and Status** Maximum packet size is 512 bytes. The rest definitions are same as control endpoint.

Offset Address: 2F-2Ch (USBD-MMIO)
Interrupt Endpoint Control and Status **Default Value: 3008 0000h**

Bit	Attribute	Default	Description
31:0	RW	3008 0000h	**Interrupt Endpoint Control and Status** Maximum packet size is 8 bytes. The rest definitions are same as control endpoint.

VIA USB Device Endpoint Transfer Descriptor Registers (30-11Fh)

Offset Address: 37-30h (USBD-MMIO)
Interrupt Buffer **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Interrupt Buffer**

Offset Address: 38-3Fh (USBD-MMIO) – Reserved

Offset Address: 43-40h (USBD-MMIO)
Control Endpoint Transfer Descriptor - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Data Toggle Initial Value** Initial data toggle of this transfer. 0: Data0 1: Data1
30:23	RO	0	**Reserved**
22:16	RW	0	**Total Bytes to Transfer** Maximum is 64 bytes.
15	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when data phase transfer or setup command transfer is complete or on short packet/babble packet is received.
14:13	RO	0	**Reserved**
12	RW1C	0	**Receive Setup Command Data of Valid 8 Bytes** Controller asserts this bit when a new 8 bytes setup packet is received, and shows the data in the next two double words.
11	RW	0	**Transfer Direction I/O** Transfer direction is from the view of host. 0: Host out 1: Host in
10:4	RO	0	**Reserved**
3	RW	0	**Enable Endpoint of DMA Engine First** 0: Inactive 1: Active
2	RW	0	**Short Packet Detect** If bit 15 is set, interrupt will be generated. 0: Not detected 1: Detected In D11F0 this chip acts as USB device and therefore functions as a receiver side during Host Out. This bit should be check when receive complete interrupt on Host Out.
1	RW	0	**Babble Detected** If bit 15 is set, interrupt will be generated. 0: Not detected 1: Detected In D11F0 this chip acts as USB device and therefore functions as a receiver side during Host Out. This bit should be check when receive complete interrupt on Host Out.

0	RW	0	**Transaction Error** Babble condition is also included. No interrupts will be generated. 0: No error 1: Transaction error This bit should be checked when the transfer is complete.

Offset Address: 47-44h (USBD-MMIO)
Control Endpoint Transfer Descriptor - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointers points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx48[0] filed to produce starting buffer address for this transaction.

Offset Address: 4B-48h (USBD-MMIO)
Control Endpoint Transfer Descriptor - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointers points to the physical memory address which stores all the data to transfer.
11:1	RO	0	**Reserved**
0	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list. Valid values are in the range of 0 to 1.

Offset Address: 4F-4Ch (USBD-MMIO)
Control Endpoint Transfer Descriptor - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Command Byte 3**
23:16	RO	0	**Command Byte 2**
15:8	RO	0	**Command Byte 1**
7:0	RO	0	**Command Byte 0**

Offset Address: 53-50h (USBD-MMIO)
Control Endpoint Transfer Descriptor - 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Command Byte 7**
23:16	RO	0	**Command Byte 6**
15:8	RO	0	**Command Byte 5**
7:0	RO	0	**Command Byte 4**

Offset Address: 54h (USBD-MMIO)
Interrupt In Endpoint Transfer Descriptor **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Total Bytes to Transfer** Maximum is 8 bytes.
3	RW	0	**Data Toggle Initial Value** Initial data toggle of this packet. 0: Data 0 1: Data 1
2	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when this transaction is completed.
1	RW	0	**Transaction Active Status** 0: Inactive 1: Active
0	RW	0	**Transaction Error Status** Timeout and PID errors are also included. No interrupts will be generated. 0: No error 1: Transaction error

Offset Address: 55-57h (USBD-MMIO) – Reserved

Offset Address: 58h (USBD-MMIO)

Fake Attach Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Fake Attach Enable** 0: Disable 1: Enable
0	RO	0	**Fake Attach Detect** 0: PHY clock is not OK in FAKE mode or it's not in FAKE mode 1: PHY clock is OK in Fake Attach mode

Offset Address: 59h (USBD-MMIO) – Reserved

Offset Address: 5Ah (USBD-MMIO)

Dynamic Clock Enable - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**HS_MAC_RX_CLK60M Clock Enable** 0: No effect 1: Enable
6	RW	0	**HS_MAC_TX_CLK60M clock Enable** 0: No effect 1: Enable
5	RW	0	**ENDP0_FIFO_CLK Clock Enable** 0: No effect 1: Enable
4	RW	0	**ENDP3_CTRL_CLK Clock Enable** 0: No effect 1: Enable
3	RW	0	**ENDP2_CTRL_CLK Clock Enable** 0: No effect 1: Enable
2	RW	0	**ENDP1_CTRL_CLK Clock Enable** 0: No effect 1: Enable
1	RW	0	**ENDP0_CTRL_CLK Clock Enable** 0: No effect 1: Enable
0	RW	0	**DEV_CLK60M Clock Enable** 0: No effect 1: Enable

Offset Address: 5Bh (USBD-MMIO)

Dynamic Clock Enable -2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**UTM_CHK_CLK60M Clock Enable** 0: No effect 1: Enable
2	RW	0	**UD_PCLK66_EP3 and UD_PCLK66_SR3 Clock Enable** 0: No effect 1: Enable
1	RW	0	**UD_PCLK66_EP2 and UD_PCLK66_SR2 Clock Enable** 0: No effect 1: Enable
0	RW	0	**UD_PCLK66_EP1 and UD_PCLK66_SR1 Clock Enable** 0: No effect 1: Enable

Offset Address: 5C-5Fh (USBD-MMIO) – Reserved

Offset Address: 63-60h (USBD-MMIO)
Bulk OUT Endpoint Transfer Descriptor (Host Out) 1 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer**
15:9	RW	0	**Scratch Register** R/W for software use
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In/Out transfer. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** 0: Disable 1: Enable The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is only valid for Bulk Out, not Bulk In.
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble/short packet is received.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** 0: Inactive 1: Active
2	RW	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. 0: Not detected 1: Detected This bit should be checked when receive complete interrupt on HOST OUT. RO is for BULK IN Descriptor.
1	RW	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. 0: Not detected 1: Detected This bit should be checked when receive complete interrupt on HOST OUT. RO is for BULK IN Descriptor.
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. 0: No error 1: Transaction error This bit should be checked when receive complete interrupt on HOST OUT

Offset Address: 67-64h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor (Host Out) 1 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointers points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: 6B-68h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor (Host Out) 1 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointers points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: 6F-6Ch (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor (Host Out) 1 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: 77-70h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor 2 – 1&2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk Out Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions.

Offset Address: 7F-78h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor 2 – 3&4 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk Out Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions.

Offset Address: 87-80h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor 3 – 1&2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk Out Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions.

Offset Address: 8F-88h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor 3 – 3&4 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk Out Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions.

Offset Address: 97-90h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor 4 – 1&2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk Out Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions.

Offset Address: 9F-98h (USBD-MMIO)
Bulk Out Endpoint Transfer Descriptor 4 – 3&4 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk Out Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions.

Offset Address: A7-A0h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor (Host In) 1 – 1&2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: AF-A8h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor (Host In) 1 – 3&4 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: B7-B0h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: BF-B8h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: C7-C0h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor 3 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: CF-C8h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor 3 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: D7-D0h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor 4 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: DF-D8h (USBD-MMIO)
Bulk In Endpoint Transfer Descriptor 4 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Bulk In Endpoint Transfer Descriptor** The definition is the same as Bulk Out endpoint I. Please refer to the Rx60-6F bit descriptions. The attribute of bit[2:1] is RO.

Offset Address: E3-E0h (USBD-MMIO)
Control PIO Descriptor **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Control PIO Descriptor** The definition is the same as Bulk In endpoint I. Please refer to the Rx60-6F bit descriptions. The Shadow register of control descriptor, and valid only when USBD-MMIO Rx10[15] PIO Enable is 1.

Offset Address: E7-E4h (USBD-MMIO)
Bulk Out PIO Descriptor **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Bulk Out PIO Descriptor** The definition is the same as Bulk Out endpoint I. The Shadow register of the first Bulk Out descriptor, and valid only when USBD-MMIO Rx10[15] PIO Enable is 1.

Offset Address: EB-E8h (USBD-MMIO)

Bulk In PIO Descriptor **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Bulk In PIO Descriptor** The definition is the same as Bulk In endpoint I. The Shadow register of the first Bulk In descriptor, and valid only when USBD-MMIO Rx10[15] PIO Enable is 1.

Offset Address: EC-FFh (USBD-MMIO) – Reserved

Offset Address: 107-100h (USBD-MMIO)

MAC Address 1 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**MAC Address 1**

Offset Address: 10F-108h (USBD-MMIO)

MAC Address 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**MAC Address 2**

Offset Address: 117-110h (USBD-MMIO)

USB Serial Number 1 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**USB Serial Number 1**

Offset Address: 11F-118h (USBD-MMIO)

USB Serial Number 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**USB Serial Number 2**

DEVICE 12 FUNCTION 0 (D12F0): SDIO HOST CONTROLLER

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D12F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D12F0)
Device ID **Default Value: 95D0h**

Bit	Attribute	Default	Description
15:0	RO	95D0h	**Device ID**

Offset Address: 05-04h (D12F0)
PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9	RO	0	**Fast Back to Back** Hardwired to 0. (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0. (Not supported)
7	RO	0	**Address Stepping** Hardwired to 0. (Not supported)
6	RO	0	**Parity Error Response** Hardwired to 0. (Not supported)
5	RO	0	**VGA Palette Snooping** Hardwired to 0. (Not implemented)
4	RW	0	**Memory Write and Invalidate** 0: Memory write instead 1: Master can generate the command This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
3	RO	0	**Respond to Special Cycle** Hardwired to 0. (Not supported)
2	RW	0	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	0	**I/O Space Access** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 07-06h (D12F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Detect Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR#)** This bit is set whenever the device asserts SERR#. 0: No error 1: Error occurs
13	RO	0	**Received Master Abort** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Signaled Target Abort** 0: No abort signaled 1: Transaction aborted by this chip.
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error Detected** This bit is only set by bus masters. 0: No parity error detected 1: Error detected in data phase
7	RO	0	**Fast Back-to-Back Capability** 0: Device can't accept fast back-to-back transactions 1: Device can accept fast back-to-back transactions
6:5	RO	0	**Reserved**
4	RO	1b	**Capability List** 0: No new capabilities linked list 1: Available implement the pointer for a new capabilities linked at offset 34h
3	RO	0	**Interrupt Status** This read-only bit reflects the state of the interrupt in the device/function. This bit is only valid when Rx04[10] is 0. 0: No interrupt 1: Interrupt asserted
2:0	RO	0	**Reserved**

Note: More detailed information on PCI Command & Status registers please refer to the PCI Local Bus Specification Revision 3.0 Chapter 6.2

Offset Address: 08h (D12F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D12F0)

Class Code **Default Value: 08 0501h**

Bit	Attribute	Default	Description
23:0	RO	080501h	**Class Code** 080501h means SDIO host controller.

Offset Address: 0C-0Dh (D12F0) – Reserved

Offset Address: 0Eh (D12F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device.

Offset Address: 0Fh (D12F0) – Reserved

Offset Address: 13-10h (D12F0)
SDIO Slot 1 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Base Address [31:8]**
7:1	RO	0	**Reserved** Fixed at 0
0	RO	0	**Space Indicator** 0: Memory space 1: IO Space

Offset Address: 17-14h (D12F0)
SDIO Slot 2 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Base Address [31:8]**
7:1	RO	0	**Reserved** Fixed at 0
0	RO	0	**Space Indicator** 0: Memory space 1: IO Space

Offset Address: 1B-18h (D12F0)
SDIO Slot 3 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Base Address [31:8]**
7:1	RO	0	**Reserved** Fixed at 0
0	RO	0	**Space Indicator** 0: Memory space 1: IO Space

Offset Address: 1C-2Bh (D12F0) – Reserved

Offset Address: 2D-2Ch (D12F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D12F0)
Subsystem ID **Default Value: 95D0h**

Bit	Attribute	Default	Description
15:0	RO	95D0h	**Subsystem ID**

Offset Address: 30-33h (D12F0) – Reserved

Offset Address: 34h (D12F0)
Capabilities Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capabilities Pointer** Point to the power management capability

Offset Address: 35-3Bh (D12F0) – Reserved

Offset Address: 3Ch (D12F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (D12F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#)

Offset Address: 3E-3Fh (D12F0) – Reserved

SDIO PCI Device Specific Registers (40-FFh)

Offset Address: 40h (D12F0)
Slot Information **Default Value: 20h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RO	010b	**Number of Slots** 000: One slot 001: Two slots 010: Three slots Others: Reserved
3:0	RO	0	**Reserved**

Offset Address: 41-43h (D12F0) – Reserved

Offset Address: 44h (D12F0)
Back Door Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Subsystem ID / Subsystem Vender ID Back Door Enable** Specify whether Rx2C~2D and 2E~2F are RO or RW 0: Read Only 1: Read / Write

Offset Address: 45-7Fh (D12F0) – Reserved

Offset Address: 81-80h (D12F0)
PCI Power Management Capabilities ID **Default Value: 0001h**

Bit	Attribute	Default	Description
15:8	RO	0	**Point to the Next Capability Structure**
7:0	RO	01h	**PCI Power Management Capability**

Offset Address: 83-82h (D12F0)

PCI Power Management Capabilities **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:11	RO	1Fh	**PME Can Be Generated from D3 and D0 State**
10	RO	1b	**D2 State Support** 0: Not supported 1: Supported
9	RO	1b	**D1 State Support** 0: Not supported 1: Supported
8:6	RO	111b	**Report D3 Max Suspend Current** 111b indicates 375mA required.
5	RO	0	**Device-Specific Initialization** 0: Not required 1: Required
4	RO	0	**Reserved**
3	RO	0	**Hardwired to 0**
2:0	RO	010b	**PCI Power Management Capability** 010b indicates PCI power management 1.1 support.

Offset Address: 87-84h (D12F0)

Power Management Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Hardwired to 0**
21:16	RO	0	**Reserved**
15	RW1C	0	**PME Status** This bit is set when the SDIO Host Controller would assert the PME# independent of the state of bit 8. This bit is in resume well.
14:9	RO	0	**Reserved**
8	RWS	0	**Enable PME** Enable PME wake up if bit 15 is set. This bit is in resume well. 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** This field is used both to determinate the current power state and to set a new power state. 00: D0 01: D1 10: D2 11: D3 If software attempts to write an unsupported optional state to this field, the write operation will complete normally on the bus; however, the data is discarded and no state change occurs.

Offset Address: 8B-88h (D12F0)

SDIO Host Capabilities **Default Value: 0560 0181h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26	RW	1b	**Voltage Support 1.8V** 0: Not supported 1: Supported
25	RO	0	**Reserved**
24	RW	1b	**Voltage Support 3.3V** 0: Not supported 1: Supported
23	RW	0b	**Suspend / Resume Support** 0: Not supported 1: Supported
22	RW	1b	**DMA Support** 0: Not supported 1: Supported
21	RW	1b	**High Speed Support** 0: Not supported 1: Supported
20:18	RO	0	**Reserved**
17:16	RW	00b	**Max Block Length** 00: 512 bytes 01: 1024 bytes (not supported) 10: 2048 bytes (not supported) 11: Reserved
15:9	RO	0	**Reserved**
8	RW	1b	**Base Clock Frequency For SD Clock** 0: 33MHz 1: 48MHz
7	RW	1b	**Timeout Clock Unit** 0: KHz (Not supported) 1: MHz
6:1	RO	0	**Reserved**

0	RW	1b	**Timeout Clock Frequency** 0: 33MHz 1: 48MHz Must ensure the setting is the same as that of bit 8.

Offset Address: 8Ch (D12F0)
SDIO Host Capabilities 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Slot 2 Receiving Logic Clock Enable** 0: Disable 1: Enable
6	RW	0	**Slot 1 Receiving Logic Clock Enable** 0: Disable 1: Enable
5:2	RW	0	**Reserved**
1	RW	0	**Slot 2 Data Output Clock Trigger Edge under High Speed** 0: Rising edge trigger 1: Falling edge trigger
0	RW	0	**Slot 1 Data Output Clock Trigger Edge under High Speed** 0: Rising edge trigger 1: Falling edge trigger

Offset Address: 8Dh (D12F0)
SDIO Host Capabilities 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**Slot 3 Receiver Delay Clock Select** 0: 2-clock period 1: 3-clock period
2	RO	0	**Slot 2 Receiver Delay Clock Select** 0: 2-clock period 1: 3-clock period
1	RO	0	**Slot 1 Receiver Delay Clock Select** This bit is used to control how to generate read wait signal and stop clock. 0: 2-clock period 1: 3-clock period
0	RO	0	**Receiving Logic Control** 0: Using receiving logic 1: Bypass receiving logic

Offset Address: 8Eh (D12F0)
SDIO Host Capabilities 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PAD TNI Enable** 0: Don't bypass PAD TNI 1: Bypass PAD TNI & by pass SDWP gating
6:5	RW	00b	**Slot 3 Host CLK Delay Latency** 00: Bypass mode 01: Delay 1.6ns 10: Delay 3.2ns 11: Delay 4.8ns
4:3	RW	00b	**Slot 2 Host CLK Delay Latency** 00: Bypass mode 01: Delay 1.6ns 10: Delay 3.2ns 11: Delay 4.8ns
2:1	RW	00b	**Slot 1 Host CLK Delay Latency** 00: Bypass mode 01: Delay 1.6ns 10: Delay 3.2ns 11: Delay 4.8ns
0	RW	0	**Debug Port Select** 0: Host controller 1: DMA buffer

Offset Address: 8Fh (D12F0)
SDIO Host Capabilities 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Slot 3 Receiving Logic Clock Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Slot 3 Data Output Clock Trigger Edge under High Speed** 0: Rising edge trigger 1: Falling edge trigger

Offset Address: 93-90h (D12F0)

SDIO Host Debug Signals 1 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**SDIO Host Debug Signals 1**

Offset Address: 97-94h (D12F0)

SDIO Host Debug Signals 2 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**SDIO Host Debug Signals 2**

Offset Address: 98h (D12F0)

SDIO Host Capabilities 5 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1:0	RW	0	**De-bouncing Time Select** 00h: 0.5 sec 01h: 1 sec 02h: 2 sec 03h: bypass debounce

Offset Address: 99h (D12F0)

SDIO Host Capabilities 6 — **Default Value: FAh**

Bit	Attribute	Default	Description
7	RW	1b	**Dynamic Clock for PCI Configuration Clock** 0: Disable 1: Enable
6	RW	1b	**Dynamic Clock for DMA Transfer Path of Slot 1** 0: Disable 1: Enable
5	RW	1b	**Dynamic Clock for DMA Transfer Path of Slot 2** 0: Disable 1: Enable
4	RW	1b	**Dynamic Clock for SDIO Host Controller Slot 1** 0: Disable 1: Enable
3	RW	1b	**Dynamic Clock for SDIO Host Controller Slot 2** 0: Disable 1: Enable
2:0	RW	010b	**Number of Slot which SDIO Host Supports** 000: One slot 001: Two slots 010: Three slots Others: Reserved

Offset Address: 9Ah (D12F0)

SDIO Host Capabilities 7 — **Default Value: 03h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	1b	**Dynamic Clock for DMA Transfer Path of Slot 3** 0: Disable 1: Enable
0	RW	1b	**Dynamic Clock for SDIO Host Controller Slot 3** 0: Disable 1: Enable

Offset Address: 9B-FFh (D12F0) – Reserved

MMIO Space (00-FFh)

SDIO Host Standard Registers (00-FFh)

This section describes memory mapped I/O registers. Please refer to SD Host Controller Standard Specification 1.0 for details.

Offset Address: 03-00h (SDIO-MMIO)

DMA System Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**DMA System Address**

Offset Address: 05-04h (SDIO-MMIO)

Data Block Size **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RW	000b	**Host DMA Buffer Boundary** 000: 4K Bytes (Detects A11 carry out) 001: 8K Bytes (Detects A12 carry out) 010: 16K Bytes (Detects A13 carry out) 011: 32K Bytes (Detects A14 carry out) 100: 64K Bytes (Detects A15 carry out) 101: 128K Bytes (Detects A16 carry out) 110: 256K Bytes (Detects A17 carry out) 111: 512K Bytes (Detects A18 carry out)
11:0	RW	000h	**Transfer Block Size** These bits specify the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. 0000h: No data transfer 0001h: 1 Byte 0002h: 2 Bytes 0003h: 3 Bytes 0004h: 4 Bytes …… 01FFh: 511 Bytes 0200h: 512 Bytes …… 0800h: 2048 Bytes

Offset Address: 07-06h (SDIO-MMIO)

Block Count **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0000h	**Block Count for Current Transfer** This bit is enabled when Block Count Enable in the Transfer Mode Register (Rx0C[1]) is set to 1 and is valid only for multiple black transfers. 0000h: Stop Count 0001h: 1 block 0002h: 2 blocks …… FFFFh: 65535 blocks

Offset Address: 0B-08h (SDIO-MMIO)

Command Argument **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Command Argument**

Offset Address: 0D-0Ch (SDIO-MMIO)
Data Transfer Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RW	0	**Multi / Single Block Select** 0: Single Block 1: Multiple Block
4	RW	0	**Data Transfer Direction Select** 0: Write (Host to Card) 1: Read (Card to Host)
3	RO	0	**Reserved**
2	RW	0	**Auto CMD12 Enable** 0: Disable 1: Enable
1	RW	0	**Block Count Enable** 0: Disable 1: Enable
0	RW	0	**DMA Enable** This bit can be enabled only when DMA is supported (SDIO-MMIO Rx40[22]=1) 0: Disable 1: Enable

Table 17. Determination of Transfer Type

Rx0C[5] (Multi/Single Block Select)	Rx0C[1] (Block Count Enable)	Rx07-06 (Block Count)	Function
0	Don't care	Don't care	Single Transfer
1	0	Don't care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

Offset Address: 0F-0Eh (SDIO-MMIO)
Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13:8	RW	0	**Command Index**
7:6	RW	00b	**Command Type** 00: Normal (Other commands) 01: Suspend (CMD52 for writing "Bus Suspend" in CCCR) 10: Resume (CMD52 for writing "Function Select" in CCCR) 11: Abort (CMD12, CMD52 for writing "I/O Abort" in CCCR) Note: CCCR (Card Common Control Register)
5	RW	0	**Data Present Select** 0: No data present 1: Data present
4	RW	0	**Command Index Check Enable** 0: Disable 1: Enable
3	RW	0	**Command CRC (Cyclic Redundancy Check) Check Enable** 0: Disable 1: Enable
2	RO	0	**Reserved**
1:0	RW	00b	**Response Type Select** 00: No Response 01: Response length 136 10: Response length 48 11: Response length 48 check Busy after response

Offset Address: 17-10h (SDIO-MMIO)
Command Response 1 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Command Response**

Offset Address: 1F-18h (SDIO-MMIO)
Command Response 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Command Response**

Offset Address: 23-20h (SDIO-MMIO)
Buffer Data Port **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Buffer Data** The host controller buffer can be accessed through this 32-bit data port register.

Offset Address: 27-24h (SDIO-MMIO)
Present State **Default Value: 01F2 0000h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**CMD Line (SDIO[1:0]CMD#) Signal Level** 0: Low level 1: High level
23:20	RO	Fh	**DAT Line (SDIO[1:0]D[3:0]) Signal Level** For each bit: 0: Low level 1: High level
19	RO	0	**Write Protect Signal Level** 0: Write protected (SDIO[1:0]WPD# = 0) 1: Write enabled (SDIO[1:0]WPD# = 1)
18	RO	0	**Card Detect Signal Level** 0: No card present (SDIO[1:0]CD# = 1) 1: Card present (SDIO[1:0]CD# = 0)
17	RO	1b	**Card State Stable** 0: Reset or de-bouncing 1: No card or inserted
16	RO	0	**Card Inserted** 0: Reset or de-bouncing or no card 1: Card inserted
15:12	RO	0	**Reserved**
11	RO	0	**Buffer Read Enable** This status is used for non-DMA read transfers. 0: Read disable 1: Read enable
10	RO	0	**Buffer Write Enable** This status is used for non-DMA write transfers. 0: Write disable 1: Write enable
9	RO	0	**Read Transfer Active** 0: No valid data 1: Transferring data
8	RO	0	**Write Transfer Active** 0: No valid data 1: Transferring data
7:3	RO	0	**Reserved**
2	RO	0	**DAT Line Active** This bit indicates whether one of the data lines on SD Bus is in use. 0: DAT line inactive 1: DAT line active
1	RO	0	**Command Inhibit (DAT)** 0: Can issue command using the DAT line 1: Cannot issue command using the DAT line
0	RO	0	**Command Inhibit (CMD)** 0: Can issue command using only the CMD line 1: Cannot issue command

Offset Address: 28h (SDIO-MMIO)
Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**High Speed Enable** 0: Normal speed mode 1: High speed mode
1	RW	0	**Data Transfer Width** 0: 1-bit mode 1: 4-bit mode
0	RW	0	**LED Control** 0: LED off 1: LED on

Offset Address: 29h (SDIO-MMIO)

Power Control **Default Value: 0Eh**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:1	RW	111b	**SD Bus Voltage Select** 000-100: Reserved 101: 1.8V 110: 3.0V (not supported) 111: 3.3V
0	RW	0	**SD Bus Power** 0: Power off 1: Power on (This bit is RW only when the card is in the slot.)

Offset Address: 2Ah (SDIO-MMIO)

Block Gap Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Interrupt at Block Gap** 0: Disable 1: Enable
2	RW	0	**Read Wait Control** 0: Disable 1: Enable
1	RW	0	**Continue Request** 0: No effect 1: Restart
0	RW	0	**Stop at Block Gap Request** 0: Transfer 1: Stop

Offset Address: 2Bh (SDIO-MMIO)

Wakeup Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Wakeup Event Enable on SD Card Removal** 0: Disable 1: Enable
1	RW	0	**Wakeup Event Enable on SD Card Insertion** 0: Disable 1: Enable
0	RW	0	**Wakeup Event Enable on Card Interrupt** 0: Disable 1: Enable

Offset Address: 2D-2Ch (SDIO-MMIO)

Clock Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RW	00h	**SDCLK (SDIO[1:0]CLK) Frequency Select** 00h: Base clock (10MHz-63MHz) 01h: Base clock divided by 2 02h: Base clock divided by 4 04h: Base clock divided by 8 08h: Base clock divided by 16 10h: Base clock divided by 32 20h: Base clock divided by 64 40h: Base clock divided by 128 80h: Base clock divided by 256 Others: Reserved
7:3	RO	0	**Reserved**
2	RW	0	**SD Clock Enable** 0: Disable 1: Enable (This bit is RW only when the card is in the slot.)
1	RO	0	**Internal Clock Stable** 0: Not ready 1: Ready
0	RW	0	**Internal Clock Enable** 0: Stop 1: Oscillate

Offset Address: 2Eh (SDIO-MMIO)

Timeout Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Data Timeout Counter Value** 0000: TMCLK x 2^{13} 0001: TMCLK x 2^{14} ………. 1110: TMCLK x 2^{27} 1111: Reserved

Offset Address: 2Fh (SDIO-MMIO)

Software Reset **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Software Reset for DAT (SDIO[1:0]D[3:0]) Line** 0: Work 1: Reset
1	RW	0	**Software Reset for CMD (SDIO[1:0]CMD#) Line** 0: Work 1: Reset
0	RW	0	**Software Reset for All** 0: Work 1: Reset

Offset Address: 31-30h (SDIO-MMIO)

Normal Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Error Interrupt** 0: No Error 1: Error
14:9	RO	0	**Reserved**
8	RO	0	**Card Interrupt** 0: No card interrupt 1: Generate card interrupt
7	RW1C	0	**Card Removal** 0: Card state stable or de-bouncing 1: Card removed
6	RW1C	0	**Card Insertion** 0: Card state stable or de-bouncing 1: Card inserted
5	RW1C	0	**Buffer Read Ready** 0: Not ready to read buffer 1: Ready to read buffer
4	RW1C	0	**Buffer Write Ready** 0: Not ready to write buffer 1: Ready to write buffer
3	RW1C	0	**DMA Interrupt** 0: No DMA interrupt 1: DMA interrupt is generated
2	RW1C	0	**Block Gap Event** 0: No block gap event 1: Transaction stopped at block gap
1	RW1C	0	**Transfer Complete** 0: No transfer complete 1: Data transfer complete
0	RW1C	0	**Command Complete** 0: No command complete 1: Command complete

Offset Address: 33-32h (SDIO-MMIO)
Error Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW1C	0	**Vendor Specific Error Status**
11:9	RO	0	**Reserved**
8	RW1C	0	**Auto CMD12 Error** 0: No error 1: Error
7	RW1C	0	**Current Limit Error** 0: No error. The host controller is supplying power. 1: Power failure. The host controller is not supplying power to SD card.
6	RW1C	0	**Data End Bit Error** 0: No error 1: Error
5	RW1C	0	**Data CRC Error** 0: No error 1: Error
4	RW1C	0	**Data Timeout Error** 0: No error 1: Time out
3	RW1C	0	**Command Index Error** 0: No error 1: Error
2	RW1C	0	**Command End Bit Error** 0: No error 1: End bit error generated
1	RW1C	0	**Command CRC Error** 0: No error 1: CRC error generated
0	RW1C	0	**Command Timeout Error** 0: No error 1: Time out

Offset Address: 35-34h (SDIO-MMIO)
Normal Interrupt Status Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Fixed at 0**
14:9	RO	0	**Reserved**
8	RW	0	**Card Interrupt Status Enable** 0: Mask 1: Enable
7	RW	0	**Card Removal Status Enable** 0: Mask 1: Enable
6	RW	0	**Card Insertion Status Enable** 0: Mask 1: Enable
5	RW	0	**Buffer Read Ready Status Enable** 0: Mask 1: Enable
4	RW	0	**Buffer Write Ready Status Enable** 0: Mask 1: Enable
3	RW	0	**DMA Interrupt Status Enable** 0: Mask 1: Enable
2	RW	0	**Block Gap Event Status Enable** 0: Mask 1: Enable
1	RW	0	**Transfer Complete Status Enable** 0: Mask 1: Enable
0	RW	0	**Command Complete Status Enable** 0: Mask 1: Enable

Offset Address: 37-36h (SDIO-MMIO)
Error Interrupt Status Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**Vendor Specific Error Status Enable** 0: Mask 1: Enable
11:9	RO	0	**Reserved**
8	RW	0	**Auto CMD12 Error Status Enable** 0: Mask 1: Enable
7	RW	0	**Current Limit Error Status Enable** 0: Mask 1: Enable
6	RW	0	**Data End Bit Error Status Enable** 0: Mask 1: Enable
5	RW	0	**Data CRC Error Status Enable** 0: Mask 1: Enable
4	RW	0	**Data Timeout Error Status Enable** 0: Mask 1: Enable
3	RW	0	**Command Index Error Status Enable** 0: Mask 1: Enable
2	RW	0	**Command End Bit Error Status Enable** 0: Mask 1: Enable
1	RW	0	**Command CRC Error Status Enable** 0: Mask 1: Enable
0	RW	0	**Command Timeout Error Status Enable** 0: Mask 1: Enable

Offset Address: 39-38h (SDIO-MMIO)
Normal Interrupt Signal Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Fixed at 0**
14:9	RO	0	**Reserved**
8	RW	0	**Card Interrupt Signal Enable** 0: Mask 1: Enable
7	RW	0	**Card Removal Signal Enable** 0: Mask 1: Enable
6	RW	0	**Card Insertion Signal Enable** 0: Mask 1: Enable
5	RW	0	**Buffer Read Ready Signal Enable** 0: Mask 1: Enable
4	RW	0	**Buffer Write Ready Signal Enable** 0: Mask 1: Enable
3	RW	0	**DMA Interrupt Signal Enable** 0: Mask 1: Enable
2	RW	0	**Block Gap Event Signal Enable** 0: Mask 1: Enable
1	RW	0	**Transfer Complete Signal Enable** 0: Mask 1: Enable
0	RW	0	**Command Complete Signal Enable** 0: Mask 1: Enable

Offset Address: 3B-3Ah (SDIO-MMIO)
Error Interrupt Signal Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**Vendor Specific Error Signal Enable** 0: Mask 1: Enable
11:9	RO	0	**Reserved**
8	RW	0	**Auto CMD12 Error Signal Enable** 0: Mask 1: Enable
7	RW	0	**Current Limit Error Signal Enable** 0: Mask 1: Enable
6	RW	0	**Data End Bit Error Signal Enable** 0: Mask 1: Enable
5	RW	0	**Data CRC Error Signal Enable** 0: Mask 1: Enable
4	RW	0	**Data Timeout Error Signal Enable** 0: Mask 1: Enable
3	RW	0	**Command Index Error Signal Enable** 0: Mask 1: Enable
2	RW	0	**Command End Bit Error Signal Enable** 0: Mask 1: Enable
1	RW	0	**Command CRC Error Signal Enable** 0: Mask 1: Enable
0	RW	0	**Command Timeout Error Signal Enable** 0: Mask 1: Enable

Offset Address: 3D-3Ch (SDIO-MMIO)
Auto CMD12 Error Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RO	0	**Command Not Issued by Auto CMD12 Error** 0: No error 1: Command not issued
6:5	RO	0	**Reserved**
4	RO	0	**Auto CMD12 Index Error** 0: No error 1: Error
3	RO	0	**Auto CMD12 End Bit Error** 0: No error 1: End bit error generated
2	RO	0	**Auto CMD12 CRC Error** 0: No error 1: CRC error generated
1	RO	0	**Auto CMD12 Timeout Error** 0: No error 1: Timeout
0	RO	0	**Auto CMD12 Not Executed** 0: Executed 1: Not executed

Offset Address: 3E-3Fh (SDIO-MMIO) – Reserved

Offset Address: 47-40h (SDIO-MMIO)
Capabilities Register **Default Value: 0000 0000 0560 30B0h**

Bit	Attribute	Default	Description
63:32	RO	0	**Reserved**
31:27	RO	0	**Reserved** Reserved for voltage support.
26	RO	1b	**Voltage Support 1.8V** 0: Not supported 1: Supported
25	RO	0	**Voltage Support 3.0V** 0: Not supported 1: Supported
24	RO	1b	**Voltage Support 3.3V** 0: Not supported 1: Supported
23	RO	0	**Suspend / Resume Support** 0: Not supported 1: Supported
22	RO	1b	**DMA Support** 0: Not supported 1: Supported
21	RO	1b	**High Speed Support** 0: Not supported 1: Supported
20:18	RO	0	**Reserved**
17:16	RO	00b	**Max Block Length** 00: 512 bytes 01: 1024 bytes 10: 2048 bytes 11: Reserved
15:14	RO	0	**Reserved**
13:8	RO	30h	**Base Clock Frequency for SD Clock** 0: Get information via another method Not 0: 1MHz to 63MHz
7	RO	1b	**Timeout Clock Unit** 0: KHz 1: MHz
6	RO	0	**Reserved**
5:0	RO	30h	**Timeout Clock Frequency** These bits indicate the base clock frequency for Data Timeout Error. 0: Get information via another method Not 0: 1KHz to 63KHz or 1MHz to 63MHz

Offset Address: 4F-48h (SDIO-MMIO)
Maximum Current Capabilities **Default Value: 0000 0000 00F0 01F0h**

Bit	Attribute	Default	Description
63:24	RO	0	**Reserved**
23:16	RO	F0h	**Maximum Current for 1.8V** 0: Get information via another method 1: 4 mA 2: 8 mA 3: 12 mA ……… 255: 1020 mA
15:8	RO	01h	**Maximum Current for 3.0V** 0: Get information via another method 1: 4 mA 2: 8 mA 3: 12 mA ……… 255: 1020 mA
7:0	RO	F0h	**Maximum Current for 3.3V** 0: Get information via another method 1: 4 mA 2: 8 mA 3: 12 mA ……… 255: 1020 mA

Offset Address: 50-FBh (SDIO-MMIO) – Reserved

Offset Address: FD-FCh (SDIO-MMIO)
Slot Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RO	0	**Interrupt Signal for Each Slot** Bit [n] is for Slot [n] (n = 0 ~ 7).

Offset Address: FF-FEh (SDIO-MMIO)

Host Controller Version **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Vendor Version Number**
7:0	RO	0	**Specification Version Number** 00h: SD Host Specification Version 1.0 Others: Reserved

DEVICE 13 FUNCTION 0 (D13F0): SECURE DIGITAL AND EXTREME DIGITAL-PICTURE CARD CONTROLLER

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D13F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D13F0)

Device ID **Default Value: 9530h**

Bit	Attribute	Default	Description
15:0	RO	9530h	**Device ID**

Offset Address: 05-04h (D13F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9:3	RO	0	**Reserved**
2	RW	0	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	0	**I/O Space** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 07-06h (D13F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**Signaled System Error (SERR# Asserted)** 0: No error 1: Error occurs
13	RW1C	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** 0: No abort signaled 1: Transaction aborted by this chip.
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01. 00: Fast 01: Medium 10: Slow 11: Reserved
8:5	RO	0	**Reserved**

4	RO	1b	**Capability List** 0: No new capability linked list 1: Available. Implement the pointer for a new capability linked at Rx34.
3	RO	0	**Interrupt Status** 0: No interrupt 1: Interrupt occurs
2:0	RO	0	**Reserved**

Offset Address: 08h (D13F0)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D13F0)
Class Code **Default Value: 05 0100h**

Bit	Attribute	Default	Description
23:0	RO	050100h	**Class Code**

Offset Address: 0Ch (D13F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D13F0)
Latency Timer **Default Value: 16h**

Bit	Attribute	Default	Description
7:0	RW	16h	**Latency Timer**

Offset Address: 0Eh (D13F0)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device.

Offset Address: 0Fh (D13F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 0.

Offset Address: 13-10h (D13F0)
Card Reader (CR) MMIO Register Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RW	0	**Card Reader MMIO Register Base Address [31:11]**
10:0	RO	0	**Card Reader MMIO Register Base Address [10:0]**

Offset Address: 17-14h (D13F0)
Card Reader (CR) IO Register Base Address **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:3	RW	0	**Card Reader I/O Register Base Address [31:3]**
2:0	RO	001b	**Card Reader I/O Register Base Address [2:0]**

Offset Address: 18-2Bh (D13F0) – Reserved

Offset Address: 2D-2Ch (D13F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D13F0)
Subsystem ID **Default Value: 9530h**

Bit	Attribute	Default	Description
15:0	RO	9530h	**Subsystem ID**

Offset Address: 30-33h (D13F0) – Reserved

Offset Address: 34h (D13F0)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability List Pointer** Points to next capability structure

Offset Address: 35-3Bh (D13F0) – Reserved

Offset Address: 3Ch (D13F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**Interrupt Line Selection** 0000: Disable 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: Disable 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: Disable 1110: IRQ14 1111: IRQ15

Offset Address: 3Dh (D13F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Offset Address: 3E-3Fh (D13F0) – Reserved

PCI Card Reader - Specific Configuration Registers (40-FFh)

Offset Address: 40h (D13F0)
Card Reader Working Mode Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	0	**SDC Bus Width Capability** 0: Do not support 8-bit MMC 1: Supports 8-bit MMC
0	RW	0	**Scatter-Gather Mode Select** 0: PIO mode 1: Scatter-Gather DMA mode

Offset Address: 41-7Fh (D13F0) – Reserved

Offset Address: 80h (D13F0)
Power Management Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Power Management Capability ID**

Offset Address: 81h (D13F0)
Next Item Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer: Null** 0 indicates there is no next item.

Offset Address: 83-82h (D13F0)
Power Management Capability **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:11	RO	1Fh	**PME# Support** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. xxxx1: PME# can be asserted from D0 xxx1x: PME# can be asserted from D1 xx1xx: PME# can be asserted from D2 x1xxx: PME# can be asserted from D3 hot 1xxxx: PME# can be asserted from D3 cold
10	RO	1b	**D2 Support** 0: Not supported 1: Supported
9	RO	1b	**D1 Support** 0: Not supported 1: Supported
8:6	RO	111b	**Aux Current (Maximum Current Required)** 111: 375 mA
5	RO	0	**Device Specific Initialization <DSI>** 1 indicates that beyond the standard PCI configuration header, the function requires a device specific initialization sequence following transition to the D0 uninitialized state, which is before the generic class device driver is able to use it. Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this.
4	RO	0	**Reserved**
3	RO	0	**PME# Clock** 0: No PCI clock is required for the function to generate PME#. 1: The function relies on the presence of the PCI clock for PME# operation.
2:0	RO	010b	**Version** 010: Complies with Revision 1.1 of the PCI Power Management Interface Specification.

Offset Address: 85-84h (D13F0)

Power Management Capability Control / Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME# Status**
14:9	RO	0	**Reserved**
8	RW	0	**PME# Assertion** 0: Disable PME# assertion 1: Enable PME# assertion
7:2	RO	0	**Reserved**
1:0	RW	00b	**Device Status Control** 00: D0 01: D1 10: D2 11: D3 hot

Offset Address: 86-FBh (D13F0) – Reserved

Offset Address: FCh (D13F0)

Backdoor Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Subsystem ID Write Enable** 0: Disable 1: Enable
2	RW	0	**Subsystem Vender ID Write Enable** 0: Disable 1: Enable
1:0	RW	0	**Reserved**

Offset Address: FD-FFh (D13F0) – Reserved

MMIO Space

Card Reader MMIO Base Address Register: Rx13-10h
Card Reader IO Base Address Register: Rx17-14h

Table 18. PCI CardReader-Specific MMIO Registers

Offset Range	Function
000h~~0FFh	xDC
200h~~2FFh	SDC
400h~~4FFh	Data DMA
500h~~5FFh	CICH DMA
600h~~6FFh	PCI Control

xDC MMIO Registers (00-FFh)

Offset Address: 03-00h (xDC-MMIO)
XD Configuration 1 — **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	FFFFh	**Read Data 16-Bit Port** This port is used for single read or status data read while block data transfers through DMA engine.

Offset Address: 07-04h (xDC-MMIO)
XD Configuration 2 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Turn Off Data Phase** 0: Enable 1: Disable
6	RW	0	**Enable Data Read** 0: Disable 1: Enable When enabled, it indicates that the data is transferred from Flash Memory to the controller.
5	RW	0	**Enable Single Read / Write** 0: Disable 1: Enable When enabled, it initiates single read / write sequence.
4	RW	0	**Enable End with Command** 0: Disable 1: Enable This is used for command sequence similar to "command 1 + address + command 2". While in different hardware mode, command 1 / 2 refer to different command port register.
3:1	RW	000b	**Command Phase Byte Number** Total byte number of command: Sequence like (command 1 + address + command 2), (command 1 + address) or (command 1) does not include data phase byte number.
0	RW	0	**New Command** Set 1 will trigger command sequence and this bit will be cleared after initiating command sequence header. (command 1 + address + command 2) or (command 1 + address) or (command 1)

Offset Address: 0B-08h (xDC-MMIO)
XD Configuration 3 — **Default Value: 0000 00FFh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	FFh	**xD Card Command Port 0** In command sequence, write command 1 to this port.

Offset Address: 0F-0Ch (xDC-MMIO)
XD Configuration 4 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 2**
7:0	RW	FFh	**xD Card Command Port 1** In command sequence, write address to this port.

Offset Address: 13-10h (xDC-MMIO)
XD Configuration 5 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 4** In command sequence, write row address of device to this port.
7:0	RW	FFh	**xD Card Command Port 3** In command sequence, write row address of device to this port.

Offset Address: 17-14h (xDC-MMIO)
XD Configuration 6 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 6** In command sequence, write command data to this port according to command phase byte number register set.
7:0	RW	FFh	**xD Card Command Port 5** In command sequence, write row address or command data to this port according to command phase byte number register set.

Offset Address: 1B-18h (xDC-MMIO)
XD Configuration 7 **Default Value: 0000 00FFh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	FFh	**xD Card Command Port 7** In HW_ADDR_MAP (Hardware Address Mapping) mode, the command data is written to this port according to command phase byte number register set.

Offset Address: 1F-1Ch (xDC-MMIO)
XD Configuration 8 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 9** ***In HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 9 replaces command port 6 (xDC-MMIO Rx15) for the second block address. ***In non-HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 9 replaces command for port 5 (xDC-MMIO Rx14) for the second block address.
7:0	RW	FFh	**xD Card Command Port 8** ***In HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 8 replaces command port 5 (xDC-MMIO Rx14) for the second block address. ***In non-HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 8 replaces command port 4 (xDC-MMIO Rx11) for the second block address.

Offset Address: 23-20h (xDC-MMIO)
XD Configuration 9 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: 27-24h (xDC-MMIO)
XD Configuration 10 **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:3	RW	0	**Reserved**
2	RW	0	**Enable Second Block Address** 0: Disable 1: Enable ***In HW_ADDR_MAP mode:*** Replace command port 5 / 6 (xDC-MMIO Rx14 / Rx15) with command port 8 / 9 (xDC-MMIO Rx1C / Rx1D) for the second block address. ***In non-HW_ADDR_MAP mode:*** Replace command port 4 / 5 (xDC-MMIO Rx11 / Rx14) with command port 8 / 9 (xDC-MMIO Rx1C / Rx1D) for the second block address.
1	RW	0	**Enable Redundant Area Read Cycle** 0: Disable 1: Enable Store the data from flash into internal FIFO (xDC-MMIO RxC0-FF) This register is used when doing redundant data read only from xD card.
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: 2B-28h (xDC-MMIO)
XD Configuration 11 **Default Value: 0000 00D1h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RO	1b	**Write Protect Detect Status** Input signal XD_WPD# status
6:5	RO	10b	**Reserved (Do Not Program)**
4	RO	1b	**xDC Card Line Status** 0: xD card inserted 1: xD card not inserted
3	RO	0	**Timer-Out Indicator** 0: No time-out 1: Time-out happens
2	RO	0	**New Command Status** 0: The command sequence is finished. The controller is in data phase or idle phase. 1: The command sequence is being initiated to flash I/O bus.
1	RO	0	**All Command Status** 0: The whole transfer in flash I/O bus is finished. 1: The command and data is being transferred in flash I/O bus.
0	RO	1b	**Ready / Busy Status** 0: The selected flash is busy 1: The selected flash is ready

Offset Address: 2F-2Ch (xDC-MMIO)
XD Configuration 12 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW1C	0	**Reserved**
6	RO	0	**Reserved**
5	RW1C	0	**Reserved**
4	RW1C	0	**xDC Card Insertion / Extraction Interrupt** 0: Interrupt is not caused by card insertion. 1: Interrupt is caused by device of xDC card insertion or extraction.
3	RW1C	0	**From Busy to Ready Status** 0: No status change 1: Status change occurs and the flash is from busy to ready now.
2:0	RO	0	**Reserved**

Offset Address: 33-30h (XDC-MMIO)
XD Configuration 13 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	0	**XDC DMA Counter 0** Set the low 8 bits of data transfer count.
7:0	RW	0	**XDC DMA Counter 1** Set the high 8 bits of data transfer count.

Offset Address: 37-34h (xDC-MMIO)
XD Configuration 14 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	0	**Reserved**

Offset Address: 3B-38h (xDC-MMIO)
XD Configuration 15 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: 3F-3Ch (xDC-MMIO)
XD Configuration 16 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Reserved**

Offset Address: 43-40h (xDC-MMIO)
XD Configuration 17 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Reserved**

Offset Address: 47-44h (xDC-MMIO)
XD Configuration 18 — **Default Value: 0000 00FFh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	FFh	**Enable xD Card** ***In indirect map mode:*** 0001x000: xD Card chip 0~7 disable 0000x000: xD Card chip 0 enable 0000x001: xD Card chip 1 enable 0000x010: xD Card chip 2 enable 0000x011: xD Card chip 3 enable 0000x100: xD Card chip 4 enable 0000x101: xD Card chip 5 enable 0000x110: xD Card chip 6 enable 0000x111: xD Card chip 7 enable Others: Reserved ***In direct map mode:*** Bit n is used to control chip enable. For each bit: 0: Enable 1: Disable

Offset Address: 4B-48h (xDC-MMIO)
XD Configuration 19 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Enable Clock Stop** Set 1 will drive output signal xD Card Controller Host Clock Stop high when xDC in idle phase (finish current transfer phase or command phase).
6	RW	0	**Disable Hardware to Generate Page Ok** 0: Check page write correct and output DMA Transfer Complete signal. 1: Disable check page write correct
5	RW	0	**Enable Chip Enable (XD_CE#) Direct Map** 0: Disable direct map 1: Enable direct map
4	RW	0	**Write Protect** 0: Drive output signal XD_WP low (valid) 1: Drive output signal XD_WP high (invalid)
3:0	RW	0	**Reserved**

Offset Address: 4F-4Ch (xDC-MMIO)
XD Configuration 20 **Default Value: 0000 0080h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	1b	**Interrupt Mask Control** 0: Enable all none-mask interrupt 1: Mask all interrupt
6:5	RW	0	**Reserved**
4	RW	0	**xD Card Change Interrupt Mask** 0: Enable xD card status change interrupt 1: Mask xD card status change interrupt
3	RW	0	**From Busy to Ready Status Mask** 0: Enable this interrupt 1: Disable this interrupt
2	RW	0	**Redundant Uncorrectable Error Mask** This bit controls whether the interrupt will be generated when uncorrectable errors occur. 0: Enable this interrupt 1: Disable this interrupt
1	RW	0	**Redundant 1-Bit Error Mask** This bit controls whether the interrupt will be generated when uncorrectable errors occur. 0: Enable this interrupt 1: Disable this interrupt
0	RW	0	**Redundant Code Error Mask** This bit controls whether the interrupt will be generated when ECC code errors occur. 0: Enable this interrupt 1: Disable this interrupt

Offset Address: 53-50h (xDC-MMIO)
XD Configuration 21 **Default Value: 1212 1212h**

Bit	Attribute	Default	Description
31:28	RW	1h	**Read Pulse Time (Unit: ns)** Based on xDC clock, pulse width cycle numbers of XDC Read Pulse Time (XDC_RE tRP).
27:24	RW	2h	**Read Cycle Time (Unit: ns)** Based on xDC clock, read cycle numbers of XDC Read Cycle Time (XDC_REtRC).
23:20	RW	1h	**Write Pulse Time (Unit: ns)** Based on xDC clock, pulse width cycle numbers of XDC Write Pulse Time (XDC_WE tWP).
19:16	RW	2h	**Write Cycle Time (Unit: ns)** Based on xDC clock, write cycle numbers of XDC Write Cycle Time (XDC_WE tWC).
15:0	RW	1212h	**Reserved (Do Not Program)**

Offset Address: 57-54h (xDC-MMIO)
XD Configuration 22 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Reserved**
6	RW	0	**Enable Hardware Address Mapping** 0: Disable this function and programmer should write correct address to the command port registers 1: Enable hardware physical address mapping, which will enable block address / page address mapping according to different kinds of chip.
5	RW	0	**Timer Run Mask** 0: Enable timer run signal output 1: Disable timer run signal output
4	RW	0	**Timer Time Out Mask** 0: Enable timer time out interrupt 1: Disable timer time out interrupt
3	RW	0	**Enable Three Cycles** 0: For xDC 512 bytes/page structure erase operation, address phase is 3 cycles 1: For xDC 512 bytes/page structure erase operation , address phase is 2 cycles
2	RW	0	**Enable ECC Test Mode** 0: Disable 1: Enable. Will write redundant area data in the place of ECC code.
1:0	RW	00b	**Bank Select (for 1-Bit Error Location)** Set these two bits to select the appropriate bank, and then read ECC data from ECC register to locate the error bit. 00: Bank 12 selected 01: Bank 34 selected 10: Bank 56 selected 11: Bank 78 selected

Offset Address: 5B-58h (xDC-MMIO)
XD Configuration 23 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:13	RW	0	**Reserved**
12	RW	0	**Enable Dummy High** 0: Insert FFh data before valid data if data source can not pre-fetch enough data. 1: Insert FFh data after valid data if data source can not pre-fetch enough data.
11:0	RW	0	**Dummy 12-Bit Counter** Dummy data counter

Offset Address: 5F-5Ch (xDC-MMIO)
XD Configuration 24 **Default Value: 0000 001Fh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:5	RW	000b	**Page Size Select** 000: 16 pages per block 001: 32 pages per block 010: 64 pages per block 011: 128 pages per block 100: 256 pages per block 101: 512 pages per block 110 / 111: Reserved
4:0	RW	1Fh	**Reserved (Do Not Program)**

Offset Address: 63-60h (xDC-MMIO)
XD Configuration 25 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Support xD Card ECC Format** 1: Support XDC mode
6:4	RW	0	**Reserved**
3	RW	0	**Fixed Command Hold** 0: Disable 1: Enable
2	RW	0	**XDC Write Strobe Negative Edge Clock** 0: Disable 1: Enable
1	RW	0	**XDC Read Strobe Sync Delay One Clock** 0: Disable 1: Enable
0	RW	0	**XDC Read Strobe Negative Edge Clock** 0: Disable 1: Enable

Offset Address: 67-64h (xDC-MMIO)
XD Configuration 26 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Enable Bank 8 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
30	RW	0	**Enable Bank 8 Uncorrectable Error Mask** 0: Disable 1: Enable
29	RW	0	**Enable Bank 8 1-Bit Error Mask** 0: Disable 1: Enable
28	RW	0	**Enable Bank 8 Code Error Mask** 0: Disable 1: Enable
27	RW	0	**Enable Bank 7 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
26	RW	0	**Enable Bank 7 Uncorrectable Error Mask** 0: Disable 1: Enable
25	RW	0	**Enable Bank 7 1-Bit Error Mask** 0: Disable 1: Enable
24	RW	0	**Enable Bank 7 Code Error Mask** 0: Disable 1: Enable
23	RW	0	**Enable Bank 6 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
22	RW	0	**Enable Bank 6 Uncorrectable Error Mask** 0: Disable 1: Enable
21	RW	0	**Enable Bank 6 1-Bit Error Mask** 0: Disable 1: Enable
20	RW	0	**Enable Bank 6 Code Error Mask** 0: Disable 1: Enable
19	RW	0	**Enable Bank 5 Bits[3:0] = 0 Mask** 0: Disable 1: Enable
18	RW	0	**Enable Bank 5 Uncorrectable Error Mask** 0: Disable 1: Enable
17	RW	0	**Enable Bank 5 1-Bit Error Mask** 0: Disable 1: Enable
16	RW	0	**Enable Bank 5 Code Error Mask** 0: Disable 1: Enable
15	RW	0	**Enable Bank 4 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
14	RW	0	**Enable Bank 4 Uncorrectable Error Mask** 0: Disable 1: Enable
13	RW	0	**Enable Bank 4 1-Bit Error Mask** 0: Disable 1: Enable
12	RW	0	**Enable Bank 4 Code Error Mask** 0: Disable 1: Enable
11	RW	0	**Enable Bank 3 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
10	RW	0	**Enable Bank 3 Uncorrectable Error Mask** 0: Disable 1: Enable
9	RW	0	**Enable Bank 3 1-Bit Error Mask** 0: Disable 1: Enable
8	RW	0	**Enable Bank 3 Code Error Mask** 0: Disable 1: Enable
7	RW	0	**Enable Bank 2 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
6	RW	0	**Enable Bank 2 Uncorrectable Error Mask** 0: Disable 1: Enable
5	RW	0	**Enable Bank 2 1-Bit Error Mask** 0: Disable 1: Enable
4	RW	0	**Enable Bank 2 Code Error Mask** 0: Disable 1: Enable
3	RW	0	**Enable Bank 1 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
2	RW	0	**Enable Bank 1 Uncorrectable Error Mask** 0: Disable 1: Enable
1	RW	0	**Enable Bank 1 1-Bit Error Mask** 0: Disable 1: Enable
0	RW	0	**Enable Bank 1 Code Error Mask** 0: Disable 1: Enable

Offset Address: 6B-68h (xDC-MMIO)
XD Configuration 27 — **Default Value: 0000 0FFFh**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:9	RO	111b	**Odd Bank (Bank 1, 3, 5, 7) Column Parity Bits [2:0] Status** Bit value represents the ECC code.
8:0	RO	1FFh	**Odd Bank (Bank 1, 3, 5, 7) Line Parity Status** Bit value represents the ECC code.

Offset Address: 6F-6Ch (xDC-MMIO)
XD Configuration 28 — **Default Value: 0000 0EFFh**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:9	RO	111b	**Even Bank (Bank 2, 4, 6, 8) Column Parity Bits [2:0] Status** Bit value represents the ECC code.
8:0	RO	0FFh	**Even Bank (Bank 2, 4, 6, 8) Line Parity Status** Bit value represents the ECC code.

Offset Address: 73-70h (xDC-MMIO)
XD Configuration 29 — **Default Value: 0000 073Fh**

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10:8	RO	111b	**Redundant Area Column Parity Bits [2:0] Status**
7:6	RO	0	**Reserved**
5:0	RO	3Fh	**Redundant Area Line Parity Bits [5:0] Status**

Offset Address: 77-74h (xDC-MMIO)
XD Configuration 30 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**xD Card Controller At Idle Phase** 0: Not idle 1: Idle

Offset Address: 7B-78h (xDC-MMIO)
XD Configuration 31 — **Default Value: 00FF FFFFh**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RO	FFFFFFh	**Page Address [23:0]**

Offset Address: 7F-7Ch (xDC-MMIO)
XD Configuration 32 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW1C	0	**Redundant Uncorrectable Error Status** 0: Error bit is less than 2 bits or no error 1: Error bit are 2 bits or more than 2 bits
1	RW1C	0	**Redundant 1-Bit Error Status** 0: No error 1: Error status occurs
0	RW1C	0	**Redundant Code Error Status** 0: No error 1: Error status occurs

Offset Address: 83-80h (xDC-MMIO)

XD Configuration 33 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW1C	0	**Bank 8 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
30	RW1C	0	**Bank 8 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
29	RW1C	0	**Bank 8 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
28	RW1C	0	**Bank 8 Code Error Status** 0: Not ECC code error 1: ECC code error
27	RW1C	0	**Bank 7 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
26	RW1C	0	**Bank 7 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
25	RW1C	0	**Bank 7 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
24	RW1C	0	**Bank 7 Code Error Status** 0: Not ECC code error 1: ECC code error
23	RW1C	0	**Bank 6 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
22	RW1C	0	**Bank 6 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
21	RW1C	0	**Bank 6 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
20	RW1C	0	**Bank 6 Code Error Status** 0: Not ECC code error 1: ECC code error
19	RW1C	0	**Bank 5 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
18	RW1C	0	**Bank 5 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
17	RW1C	0	**Bank 5 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
16	RW1C	0	**Bank 5 Code Error Status** 0: Not ECC code error 1: ECC code error
15	RW1C	0	**Bank 4 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
14	RW1C	0	**Bank 4 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
13	RW1C	0	**Bank 4 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
12	RW1C	0	**Bank 4 Code Error Status** 0: Not ECC code error 1: ECC code error
11	RW1C	0	**Bank 3 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0

10	RW1C	0	**Bank 3 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
9	RW1C	0	**Bank 3 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
8	RW1C	0	**Bank 3 Code Error Status** 0: Not ECC code error 1: ECC code error
7	RW1C	0	**Bank 2 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
6	RW1C	0	**Bank 2 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
5	RW1C	0	**Bank 2 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
4	RW1C	0	**Bank 2 Code Error Status** 0: Not ECC code error 1: ECC code error
3	RW1C	0	**Bank 1 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
2	RW1C	0	**Bank 1 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
1	RW1C	0	**Bank 1 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
0	RW1C	0	**Bank 1 Code Error Status** 0: Not ECC code error 1: ECC code error

Offset Address: 84-BFh (xDC-MMIO) – Reserved

Offset Address: C0-FFh (xDC-MMIO) – Reserved

Refer to xDC-MMIO Rx24[1] for details.

SDC MMIO Registers (00-FFh)

Offset Address: 00h (SDC-MMIO)

Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Command Type** Refer to the *Command Type Field Encoding* table below for valid encoding and descriptions.
3	RW1C	0	**Response FIFO Reset** Writing 1 to this bit will clear the contents of response register Rx10-1Fh. The response will be loaded to the corresponding registers according to response type whether response FIFO is reset or not.
2	RW	0	**Read or Write Operation** 0: Specifies that the data transfer direction of the current command is from card to system memory. 1: Specifies that the data transfer direction of the current command is from system memory to card
1	RW	0	**Reserved**
0	RW1C	0	**Command Start / Busy** This bit is set to initiate a command. The bit is reset once the last bit of the command argument is transmitted. Rx00[7:4], Rx00[2], Rx01, Rx02[3:0] and Rx07-04 must be configured before this bit is set.

Table 19. Command Type Field Encodings

Command Type[3:0]	Action Applied to SD Memory	Action Applied to SDIO
0000b	Non-data-write, non-data-read, non-data-stop, non-io-abort commands.	Non-data-write, non-data-read, non-data-stop, non-io-abort commands.
0001b	Single block write. Use when doing a WRITE_BLOCK (CMD24) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (seep.41 of SD spec) and is also programmed into **Block Length Register (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.	Single block IO write. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 0 (byte mode). The block size is defined in Byte/Block Count. A 0x0 value in Byte/Block Count is considered to be 256 Bytes (see p.18 of SDIO spec). The block size is also programmed Into **Block Length Register (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.
0010b	Single block read. Use when doing a READ_SINGLE_BLOCK (CMD17) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is also programmed into **Block Length Registe (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.	Single block IO read. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 0 (byte mode). The block size is defined in Byte/Block Count. A 0x0 value in Byte/Block Count is considered to be 256 Bytes (see p.18 of SDIO spec). The block size is also programmed Into **Block Length Register (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.
0011b	Multiple block write requiring STOP command to end transfer. Use when doing a WRITE_MULTIPLE_BLOCK (CMD25) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a STOP_TRANSMISSION (CMD12) command.	Multiple block IO write requiring writing to CCCR to end transfer. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/ W Flag = 1 (direction is write) and Block Mode = 1 (block mode) and Byte/Block Count = 0x0 (infinite block count) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to FN0 Block Size Registers (2 of them) inside CCCR (see p.26 of SDIO spec). For Functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The Block size is also programmed into **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a IO_RW_DIRECT (CMD52) command to write to the abort register in CCCR (bits [2:0] of register 6) (see p.23 of SDIO spec).

0100b	Multiple block read requiring STOP command to end transfer. Use when doing a READ_MULTIPLE_BLOCK (CMD18) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is programmed into **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a STOP_TRANSMISSION (CMD12) command.	Multiple block IO read requiring writing to CCCR to end transfer. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 1 (block mode) and Byte/Block Count = 0x0 (infinite block count) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a IO_RW_DIRECT (CMD52) command to write to the abort register in CCCR (bits [2:0] of register 6) (see p.23 of SDIO spec).
0101b	Not applicable.	Multiple block IO write with fixed number of blocks. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 1 (block mode) and Byte/Block Count set to the desired number of blocks to transfer (must Be non-zero) (see p.18 of SDIO spec). For function 0, block size is Programmed by using the IO_RW_DIRECT (CMD52) command To write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into the **Block Length Register (Rx0D-0C)** field. Based on the Byte/Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. Using either 1-bit or 4-bit wire will not affect this number because in the 4-bit wire case, 1 block of data is split into 4 sub-blocks (each 1/4 of the orig-inal block size) on each data wire. The start and stop bits still define the boundary of a block. The transfer will be terminated when the correct number of blocks have been transmitted. No abort action is required.
0110b	Not applicable.	Multiple block IO read with fixed number of blocks. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 1 (block mode) and Byte/Block Count set to the desired number of blocks to transfer (must Be non-zero) (see p.18 of SDIO spec). For function 0, block size is Programmed by using the IO_RW_DIRECT (CMD52) command To write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into the **Block Length Register (Rx0D-0C)** field. Based on the Byte/Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. Using either 1-bit or 4-bit wire will not affect this number because in the 4-bit wire case, 1 block of data is split into 4 sub-blocks (each 1/4 of the orig-inal block size) on each data wire. The start and stop bits still define the boundary of a block. The transfer will be terminated when the correct number of blocks have been transmitted. No abort action is required.
0111b	Terminate transfer of a multiple block write or read. Use when doing a STOP_TRANSMISSION (CMD12) command (see p.41 of SD spec).	Not applicable.
1000b	Not applicable.	Terminate transfer of a multiple block IO write or read without a fixed desired number of block count. Use when issuing a IO_RW_DIRECT (CMD52) command to write to the abort register In CCCR (bits [2:0] of register 6) to stop the transfer (see p.23 of SDIO spec).
1001b to 1111b	Reserved.	Reserved.

Offset Address: 01h (SDC-MMIO)
Command Index **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Command Index** Bits [13:8] will be the contents of bits [45:40] in SD command token.

Offset Address: 02h (SDC-MMIO)
Response Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RO	0	**Response Ready** This bit is set by the SD block once the command-response sequence is finished and reset once response FIFO is read.
3:0	RW	0000b	**Response Type** 0000: No response 0001: R1 response (48 bits) 0010: R2 response (136 bits) 0011: R3 response (48 bits) 0100: R4 response (48 bits) 0101: R5 response (48 bits) 0110: R6 response (48 bits) 1001: R1b response (48 bits) All other values are reserved.

Offset Address: 03h (SDC -MMIO) – Reserved

Offset Address: 07-04h (SDC-MMIO)
Command Argument **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Command Argument**

Offset Address: 08h (SDC-MMIO)
Bus Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**SD Host Power Down Clock Stop** Set this bit in order to save power if there is no cycle. It must be cleared before transferring any data or command. In fact, it is a software programmable clock gating.
3:2	RW	0	**Reserved**
1	RW	0	**Bus Width** 0: 1-bit mode 1: 4-bit mode Before changing the value of this bit, set card bus width with corresponding command first.
0	RW	0	**Reserved**

Offset Address: 09-0Bh (SDC-MMIO) – Reserved

Offset Address: 0D-0Ch (SDC-MMIO)
Block Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SD Host Interrupt** 0: Disable 1: Enable
14	RW	0	**Reserved**
13	RW	0	**Select GPI Pin to Detect Card** GPI pin means CR_CD# in top design. Set this bit always. 0: Disable 1: Enable
12	RW	0	**Active Polarity of Card Detection Pin** 0: Indicates the card insertion is active low. Low means the existence of memory card. 1: Indicates the card insertion is active high
11	RW	0	**Enable Transaction Abort When Multiple Blocks R/W Command CRC Error Occurs** 0: Disable 1: Enable
10:0	RW	0	**Block Length** The block length = Bits [10:0] + 1 For example: Block length = 512B, set bits [10:0] = 511.

Offset Address: 0F-0Eh (SDC-MMIO)
Block Count **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Block Count** Block Count = Bits [15:0] When Rx0F-0Eh is set to FFFFh, this field is ignored in multiple blocks R/W command. Data are transferred infinitely until the controller is programmed to generate CMD12 to terminate data transfer.

Offset Address: 1F-10h (SDC-MMIO)
Response Register **Default Value: 0h**

Bit	Attribute	Default	Description
127:0	RO	0	**Bits [5:0]: Index or reserved bit according to response type.** **Bits [15:8], [23:16]…: Response Content (except start bit, transmission bit, index or reserved bits, CRC, end bit).** ***For response type R1, R1b, R3, R6:*** Response data bits [7:1] (CRC or reserved) and bit 0 (end bit) will not be updated into the response register. ***For response type R2:*** Response data bit 135 (start bit), bit 134 (transmission bit), bits [133:128] (reserved bits), bits [127:8] (CID beside internal CRC) will be updated into the response register.

Offset Address: 21-20h (SDC-MMIO)
Current Block Count **Default Value: FFFFh**

Bit	Attribute	Default	Description
15:0	RO	FFFFh	**Current Block Count** The number of blocks that has not been transmitted in multiple blocks R/W command. When the command is done, this field value must be 0000h.

Offset Address: 22h (SDC-MMIO)
Current Bus State **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Current SD Bus State (Data Line State/CMD Line State)**

Offset Address: 23h (SDC -MMIO) – Reserved

Offset Address: 24h (SDC-MMIO)

Interrupt Mask 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Card Insertion or Removal Interrupt Enable** Interrupt is generated by CR_CD# pin. 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	0	**Enable Interrupt for Block Data Transfer Done** Generate an interrupt at the completion of each block of data transfer. 0: Disable 1: Enable
4	RW	0	**Enable Interrupt for Multiple Blocks Transfer Done** Generate an interrupt at the completion of all successful data transfer no matter it is single block or multiple blocks data transfer. 0: Disable 1: Enable
3:0	RW	0	**Reserved**

Offset Address: 25h (SDC-MMIO)

Interrupt Mask 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Write Data CRC Error Interrupt Enable** 0: Disable 1: Enable
6	RW	0	**Read Data CRC Error Interrupt Enable** 0: Disable 1: Enable
5	RW	0	**Response CRC Error Interrupt Enable** 0: Disable 1: Enable
4	RW	0	**Data Access Timeout Interrupt Enable** 0: Disable 1: Enable
3	RW	0	**Enable Interrupt for Multiple Blocks R/W Auto Stop Command-Response Transfer Done** 0: Disable 1: Enable
2	RW	0	**Enable Interrupt for Command-Response Response Access Timeout** 0: Disable 1: Enable
1	RW	0	**Command-Response Transfer Done Interrupt Enable (or Command Only if the Command Does Not Require A Response)** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 26-27h (SDC -MMIO) – Reserved

Offset Address: 28h (SDC-MMIO)

SD Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Card Detect Interrupt by GPI Pin** Card insertion or removal interrupt, using CR_CD# as card detection pin. 0: No interrupt 1: Card insertion or removal interrupt is detected
6	RW1C	0	**Reserved**
5	RW1C	0	**Block Data Transfer Done Interrupt Status** 0: No interrupt 1: Completion of one block data transfer
4	RW1C	0	**Multiple Blocks Transfer Done Interrupt Status** All data are transferred whether it is single block or multiple blocks data. 0: No interrupt 1: Block transfer complete interrupt
3	RO	0	**SD Slot Status (GPI)** Card insertion and removal share the same interrupt, so software use this bit to determine whether it is insertion or removal. The value is valid only if Rx0C[13] is set; otherwise it always is 0. 0: No card in the slot 1: SD card in the slot
2	RO	0	**Reserved**
1	RO	0	**SD Card Write Protect Status** 0: Write protected 1: Write freely
0	RW1C	0	**Reserved**

Offset Address: 29h (SDC-MMIO)

SD Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Write Data CRC Error Interrupt Status** 0: No error (Normal) 1: Error detected
6	RW1C	0	**Read Data CRC Error Interrupt Status** 0: No error 1: Error detected
5	RW1C	0	**Response CRC Error Interrupt Status** 0: No error 1: Error detected
4	RW1C	0	**Data Access Timeout Interrupt Status (NAC)** 0: Normal 1: Timeout
3	RW1C	0	**Multiple Block R/W Auto Stop Command-Response Transfer Done Interrupt Status** During multiple blocks read and write cycles, when SDC-MMIO Rx21-20 is 0, controller will generate CMD12 automatically. When receiving response of CMD12, this bit is set. 0: No interrupt 1: Interrupt occurs
2	RW1C	0	**Command-Response Response Access Timeout Interrupt (NCR) Status** 0: Normal 1: Timeout. There is no response during the given time.
1	RW1C	0	**Command-Response Transfer Done Interrupt Status (or Command Only if the Command Does Not Require A Response).** 0: No interrupt 1: Interrupt occurred
0	RO	0	**Reserved**

Offset Address: 2Ah (SDC-MMIO)

SD Status 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SD Host Automatic Clock Freezing Enable** 0: Disable. Card always transfers data without stopping clock. 1: Enable. When DMA cannot transfer data, controller can stop the clock of card in order to block the card data. It is highly recommended to set this bit always.
6	RO	0	**Clock Freezing Status** 0: Normal clocking 1: Clock frozen (potential overrun / underrun)
5	RO	0	**SD Data Response Busy Status** 0: SD card has finished programming and is idle. 1: SD card is busy in programming after write block.
4:3	RO	0	**Reserved**
2:0	RO	0	**SD Mode : Write Data CRC Status** These 3 bits contains the CRC status data of write operation. These 3 bits reflect the value which card sends to the host. 010: Transmission is ok. 101: Error occurs. **SPI Mode: Write Data Response**

Offset Address: 2Bh (SDC -MMIO) – Reserved

Offset Address: 2Ch (SDC-MMIO)

Response Timeout **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	**Number of Clocks Before A Response Timeout**

Offset Address: 2D-33h (SDC-MMIO) – Reserved

Offset Address: 34h (SDC-MMIO)
Extended Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Speed Bus Mode Selection** Set this bit when the controller works under clock frequency 33MHz or 48MHz. 0: Normal speed mode 1: High speed mode
6	RW	0	**Auto Stop Token Generation When Multiple Blocks Write Command Completes** For SPI mode only. 0: No stop token generated after multiple block Write command complete 1: Generate stop token automatically after multiple block Write command complete
5	RW	0	**Issue Bad Data (CRC = 0)** 0: Not issue 1: Issue data with wrong CRC
4	RW	0	**Issue Bad Command (CRC = 0)** 0: Not issue 1: Issue command with wrong CRC
3	RW1C	0	**Reload Block Count** This bit only takes effect during multiple blocks write. If this bit is set, controller will generate the same multiple blocks write transfer directly after finishing current multiple blocks transfer. When the new transfer starts, this bit is cleared.
2	RW	0	**MMC 8-Bit Bus Width Selection** 0: Normal mode 1: 8-bit mode Before setting this bit, set Rx08[1]=1 first. Otherwise SD bus will meet error. Rx08[1] and this bit can not be set at the same time.
1	RW	0	**Command Argument Shift 9 Bits During R/W Command**
0	RW	0	**Auto Stop Command Generation When Multiple Blocks R/W Command Completes** For SD mode only. It is highly recommended to set this bit. 0: No CMD12 after multiple blocks data transfer. 1: Generate stop command CMD12 automatically after finishing multiple blocks data transfer.

Offset Address: 35-FFh (SDC-MMIO) – Reserved

Data DMA Control Registers (00-FFh)

Offset Address: 03-00h (Data DMA-MMIO)
Data DMA Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Data DMA Base Address** ***When Write:*** Base Address for Data DMA. ***When Read:*** Current memory address will be read or write if DMA is busy or Base Address for Data DMA if DMA is idle. When DMA hang and the transfer direction is from device to memory, read from this register can be refer to judge how many data in bytes are valid in memory When DMA hang and the transfer direction if from memory to device, read from this register is no meaning for the DMA has a FIFO and shift register

Offset Address: 07-04h (Data DMA-MMIO)
Data DMA Terminate Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Data DMA Terminate Count** ***When Write*:** This register indicates the data length wanted in the next DMA transaction. ***When Read*:** The data count left to transfer if DMA is busy or terminate count if DMA is idle

Offset Address: 0B-08h (Data DMA-MMIO)
Data DMA Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RW	0	**Data DMA Soft Reset** Write 1 to reset data DNA. It's a soft reset bit that changes to 0 automatically.
23:17	RO	0	**Reserved**
16	RW	0	**Enable IRQ after Transfer Finished** 0: Disable 1: Enable
15:11	RO	0	**Reserved**
10	RW	0	**Mode Select for DMA Data Empty / Full** 0: Nature mode. The empty and full from Data DMA will reflect the actual state of internal FIFO; thus, when DMA is idle, full will be 0 and empty will be 1. 1: Hold mode. The empty and full from Data DMA will reflect the actual state of internal FIFO when DMA is busy. But when DMA is idle, full will be 0 and empty will be 1 if bit 8 is 1; full will be 1 and empty will be 0 if bit 8 is 0.
9	RW	0	**Controller Data Bus Width** 0: 8 bits 1: 16 bits
8	RW	0	**Transaction Direction** 0: From Card to Memory 1: From Memory to Card
7:0	RO	0	**Reserved**

Offset Address: 0F-0Ch (Data DMA-MMIO)
Data DMA Status 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16	RW1C	0	**IRQ Status** IRQ will assert when this bit is set and IRQ is enabled.
15:0	RO	0	**Reserved**

Offset Address: 13-10h (Data DMA-MMIO)
Data DMA Status 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**DMA Busy Status** 0: DMA is idle. 1: Start DMA transfer and DMA is busy. Set this bit will trigger data transfer, and it can reset automatically after data transfer.

Offset Address: 14-FFh (Data DMA-MMIO) – Reserved

CICH DMA Control Registers (00-FFh)

Offset Address: 03-00h (CICH DMA-MMIO)
Scatter-Gather Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Scatter-Gather Descriptor Base Address** The starting address of the first descriptor in the Scatter-Gather descriptor list.
1:0	RO	0	**Reserved**

Offset Address: 07-04h (CICH DMA-MMIO)

Control Register — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RO	0	**Current Descriptor Address** After Rx08[0] is triggered, this register will keep updating to reflect descriptor execution process. This register always contains the current descriptor starting address.
1:0	RO	0	**Reserved**

Offset Address: 0B-08h (CICH DMA-MMIO)

Engine Control — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3	RW	0	**Stop Current Descriptor List Execution** 0: Disable 1: Enable The driver might cancel current descriptor list execution. When this bit asserts, the descriptor engine will stop after current descriptor execution finishes. This bit will de-assert automatically.
2	RW	0	**Reset Engine** 0: Disable 1: Enable After exception handling, software can set this bit to reset the SG DMA, Descriptor Register File and the Descriptor Interpreter. This will terminate execution of the current descriptor list. This bit will de-assert automatically after several clocks when reset complete.
1	RW	0	**Resume Descriptor Execution** 0: Disable 1: Enable After exception handling, software can set this bit to resume the descriptor execution from the next descriptor in current list. This bit will de-assert automatically after one clock cycle.
0	RW	0	**Start Descriptor Execution** 0: Disable 1: Enable Software can set this bit to start executing a new descriptor list. The starting address of the list is specified by CICH DMA-MMIO Rx00[31:2]. This bit will de-assert automatically after one clock cycle.

Offset Address: 0F-0Ch (CICH DMA-MMIO)

Status Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Reserved**
21:20	RO	00b	**Descriptor Engine Status** 00: Idle. Engine is not executing any descriptor. 01: Busy. Engine is fetching or executing descriptor. 10: Wait. Engine is waiting for controller interrupt. 11: Stall. Exception happens, engine stalls.
19	RO	0	**xDC Interrupt Request** This bit reflects the interrupt request status of xDC. 0: xDC is not requesting to interrupt CPU. 1: xDC is requesting to interrupt CPU.
18	RO	0	**SDC Interrupt Request** This bit reflects the interrupt request status of SDC. 0: SDC is not requesting to interrupt CPU. 1: SDC is requesting to interrupt CPU.
17	RO	0	**Reserved**
16	RO	0	**DMA Interrupt Request** This bit reflects the interrupt request status of normal DMA engine. 0: Normal DMA engine is not requesting to interrupt CPU. 1: Normal DMA engine is requesting to interrupt CPU.
15:10	RO	0	**Reserved**
9	RW1C	0	**Slot Execution Done**
8	RW1C	0	**Current Descriptor List Execution Stopped** This bit will assert after current descriptor finishes when the software tries to stop current descriptor list execution by programming CICH DMA-MMIO Rx08[3]. 0: Normal execution 1: Execution stopped
7	RW1C	0	**Interrupt Clear Failed** This bit will assert when the descriptor engine try to clear the interrupt status but the interrupt signal keeps asserting. 0: Interrupt cleared successfully. 1: Failed to clear interrupt.
6	RW1C	0	**Interrupt Status Error** This bit will assert when the status register bit hits the exception pattern. 0: No exception detected from card controller 1: Exception detected from card controller
5	RO	0	**Reserved**
4	RW1C	0	**Descriptor List Execution Complete** After the last descriptor in the list execution finishes, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: Descriptor list execution is not complete. 1: Descriptor list execution is complete.
3	RW1C	0	**Descriptor Execution Complete** After current descriptor execution finishes, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: Descriptor execution is not complete. 1: Descriptor execution is complete.
2	RW1C	0	**Descriptor Format Errors Interrupt** When there is any error exists within the descriptor itself, this bit will assert and interrupt CPU if interrupt generation is enabled. For example: Reserved encoding used by the software. 0: No error detected 1: Error detected
1	RW1C	0	**Controller Exceptions Interrupt** When the card host controllers or the normal DMA engine assert interrupt request signal caused by exception conditions, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: No exception condition reported by controller 1: Exception condition reported by controller
0	RW1C	0	**Interrupt of Waiting for Controller Interrupt Time Out** When the CRDE (CardReader Description Engine) is waiting for the controller to issue interrupt request signal, if no interrupt is detected after timer expires, this register bit will assert and interrupt CPU if interrupt generation is enabled. 0: Not time out 1: Time-out happens

Offset Address: 13-10h (CICH DMA-MMIO)

Engine Setting — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17:16	RW	00b	**Wait for Controller Interrupt Time-Out Counter** 00: Never time out 01: Time out after 1 us 10: Time out after 1 ms 11: Time out after 1024 ms
15:11	RO	0	**Reserved**
10	RW	0	**Enable Interrupt On Complete** 0: Disable 1: Enable
9	RW	0	**Enable Slot Execution Done Interrupt** 0: Disable 1: Enable
8	RW	0	**Enable Current Descriptor List Execution Stopped Interrupt** 0: Disable 1: Enable
7	RW	0	**Enable Interrupt Clear Failed Interrupt** 0: Disable 1: Enable
6	RW	0	**Enable Interrupt Status Error Interrupt** 0: Disable 1: Enable
5	RW	0	**Enable Wrong Interrupt Source Interrupt** 0: Disable 1: Enable
4	RW	0	**Enable Descriptor List Execution Complete Interrupt** 0: Disable 1: Enable
3	RW	0	**Enable Descriptor Execution Complete Interrupt** 0: Disable 1: Enable
2	RW	0	**Enable Descriptor Format Errors Interrupt** 0: Disable 1: Enable
1	RW	0	**Enable Controller Exceptions Interrupt** 0: Disable 1: Enable
0	RW	0	**Enable Interrupt of Waiting for Controller Interrupt Time Out** 0: Disable 1: Enable

Offset Address: 14-FFh (CICH DMA-MMIO) – Reserved

PCI Control Registers (00-FFh)

Offset Address: 00-01h (PCI Control-MMIO) – Reserved

Offset Address: 02h (PCI Control-MMIO)

Clock Gating Control — **Default Value: 11h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Power On / Off Select** The signal outputs from pad to control the power supplied for device. 0: Power off 1: Power on
4	RW	1b	**Pad Power Select** Select the pad power according to the device supply voltage. 0: 1.8V 1: 3.3V
3:2	RW	0	**Reserved**
1	RW	0	**Enable Clock Gating** 0: Disable 1: Enable
0	RW	1b	**Soft Reset** 0: Soft reset all the controller and it will be de-asserted automatically 1: Soft reset is de-asserted

Offset Address: 03h (PCI Control-MMIO)
xDC Clock Control **Default Value: 06h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	110b	**Clock Select** 000: 12M 001: 24M 010: 48M 011: Reserved 100: 8M 101: 16M 110: 33M 111: Reserved

Offset Address: 04h (PCI Control-MMIO) – Reserved

Offset Address: 05h (PCI Control-MMIO)
SDC Clock Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	011b	**Clock Select** 000: 12M 001: 24M 010: 48M 011: 375K 100: 8M 101: 16M 110: 33M 111: Reserved

Offset Address: 06h (PCI Control-MMIO) – Reserved

Offset Address: 07h (PCI Control-MMIO)
DMA Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	000b	**Clock Select** 000: xDC 010: SDC 1xx: Reserved

Offset Address: 08h (PCI Control-MMIO)
Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Enable CICH Interrupt** 0: Disable 1: Enable
4	RW	0	**Enable DMA Interrupt** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**Enable SDC Interrupt** 0: Disable 1: Enable
1	RW	0	**Reserved**
0	RW	0	**Enable xDC Interrupt** 0: Disable 1: Enable

Offset Address: 09h (PCI Control-MMIO)

Interrupt Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**CICH Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
4	RO	0	**DMA Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
3	RO	0	**Reserved**
2	RO	0	**SDC Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
1	RO	0	**Reserved**
0	RO	0	**xDC Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred

Offset Address: 0Ah (PCI Control-MMIO)

Time Out Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	000b	**Time-Out Control** 000: No time-out 001: 32 us time-out 010: 256 us time-out 011: 1024 us time-out 100: 256 ms time-out 101: 512 ms time-out 110: 1024 ms time-out 111: Reserved

Offset Address: 0B-FFh (PCI Control-MMIO) – Reserved

DEVICE 15 FUNCTION 0 (D15F0): EIDE CONTROLLER

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D15F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D15F0)
Device ID **Default Value: C409h**

Bit	Attribute	Default	Description
15:0	RO	C409h	**Device ID** If Rx0A = 04h (RAID), Device ID = 0581h If Rx0A = 01h (IDE), Device ID = C409h Note: The value of this field will change dependent on Sub Class Code (Rx0Ah).

Offset Address: 05-04h (D15F0)
PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9	RW	0	**Reserved**
8:7	RO	0	**Reserved**
6	RO	0	**Parity Error Response**
5	RO	0	**VGA Palette Snooping (Reserved)**
4	RO	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle**
2	RW	0	**Bus Master**
1	RO	0	**Memory Space Access**
0	RW	0	**I/O Space Access** When the "I/O Space" bit is disabled, the device will not respond to I/O addresses. 0: Not respond to I/O address 1: Respond to I/O address

Offset Address: 07-06h (D15F0)
PCI Status **Default Value: 0290h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error**
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 01: Medium
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed, Rx04[6] should be set first to enable this function.
7	RO	1b	**Fast Back-to-Back Capability**
6	RO	0	**Reserved**
5	RO	0	**66 MHz Capable**
4	RO	1b	**Power Management Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D15F0)
Revision ID — **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 09h (D15F0)
Programming Interface — **Default Value: 00h**

If Rx0A = 04h, this register will be read as configuration RAID.

Bit	Attribute	Default	Description
7:0	RO	0	**Programming Interface** 0: RAID controller

Offset Address: 09h (D15F0)
Programming Interface — **Default Value: 8Ah**

If Rx0A = 01h, this register will be read as configuration IDE.

Bit	Attribute	Default	Description
7	RO	1b	**Master IDE Device**
6:4	RO	0	**Fixed at 0.**
3	RO	1b	**Programmable Indicator - Secondary**
2	RW	0	**Channel Operating Mode – Secondary** 0: Compatible mode 1: Native mode
1	RO	1b	**Programmable Indicator – Primary**
0	RW	0	**Channel Operating Mode – Primary** 0: Compatible mode 1: Native mode

Offset Address: 0Ah (D15F0)
Sub Class Code — **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Sub Class** 01h: IDE controller 04h: RAID controller

Offset Address: 0Bh (D15F0)
Base Class Code — **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Base Class** 01h indicates this is a mass storage controller

Offset Address: 0Ch (D15F0)
Cache Line Size — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Cache Line Size** Fixed at 0.

Offset Address: 0Dh (D15F0)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Latency Timer**
3:0	RO	0	**Fixed at 0.**

Offset Address: 0Eh (D15F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Multiple Function Device**
6:0	RO	0	**Fixed at 0.**

Offset Address: 0Fh (D15F0) – Reserved

Offset Address: 13-10h (D15F0)

PATA (Primary Channel) Data / Command Base Address **Default Value: 0000 0000h**

Specify an 8-byte I/O address space.
Configuration IDE Class (if Rx0A = 01h) and Compatible Mode (if Rx09[0] = 0)

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved** (Must set to 0)
15:0	RO	0	**Port Address**

Offset Address: 13-10h (D15F0)

PATA (Primary Channel) Data / Command Base Address **Default Value: 0000 03E1h**

Configuration IDE Class (if Rx0A = 01h) and Native Mode (if Rx09[0] = 1) or Configuration RAID Class (if Rx0A = 04h)

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved** (Must set to 0)
15:3	RW	003Eh	**Port Address [15:3]**
2:0	RO	001b	**Port Address [2:0]** Fixed at 001b.

Offset Address: 17-14h (D15F0)

PATA (Primary Channel) Control / Status Base Address **Default Value: 0000 0000h**

Specify a 4-byte I/O address space of which only the third byte is active.
Configuration IDE Class (if Rx0A = 01h) and Compatible Mode (if Rx09[0] = 0)

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved** (Must set to 0)
15:0	RO	0	**Port Address**

Offset Address: 17-14h (D15F0)

PATA (Primary Channel) Control / Status Base Address **Default Value: 0000 0FD1h**

Configuration IDE Class (if Rx0A = 01h) and Native Mode (if Rx09[0] = 1) or Configuration RAID Class (if Rx0A = 04h) [don't program it]

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved** (Must set to 0)
15:2	RW	00FDh	**Port Address [15:2]**
1:0	RO	01b	**Port Address [1:0]** Fixed at 01b.

Offset Address: 18-1Fh (D15F0) – Reserved

Offset Address: 23-20h (D15F0)

PATA Bus Master Mode Base Address **Default Value: 0000 CC01h**

Specify a 16-byte I/O address space for EIDE bus master controllers.

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	CC01h	**Port Address** Fixed at 0001b and bits [3:0] are RO.

Offset Address: 24-2Bh (D15F0) - Reserved

Offset Address: 2D-2Ch (D15F0)

Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D15F0)

Subsystem ID **Default Value: C409h**

Bit	Attribute	Default	Description
15:0	RO	C409h	**Subsystem ID**

Offset Address: 30-33h (D15F0) - Reserved

Offset Address: 34h (D15F0)

Capabilities Pointer **Default Value: B0h**

Bit	Attribute	Default	Description
7:0	RO	B0h	**Power Management Capabilities Pointer**

Offset Address: 35-3Bh (D15F0) - Reserved

Offset Address: 3Ch (D15F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Writeable when Rx45[4] is 0, but do not program it.**
3:0	RW	0	**IDE Interrupt Routing** If bits [7:4] are set to Fh, interrupt is routed to IRQ0. Otherwise, bits [3:0] are decoded to IRQ0~IRQ15. Writeable when Rx45[4] is 0

Offset Address: 3Dh (D15F0)

Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Interrupt Routing Mode (use INTA#)** 00: Legacy Mode Interrupt Routing Others: Native Mode Interrupt Routing When in native mode, default is 01h (INTA# used).

Offset Address: 3E-3Fh (D15F0) - Reserved

EIDE Registers (40-AFh)

Offset Address: 40h (D15F0)
EIDE Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Chip ID**
3:2	RO	0	**Reserved**
1	RW	0	**EIDE (Primary Channel) Enable** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 41-44h (D15F0) - Reserved

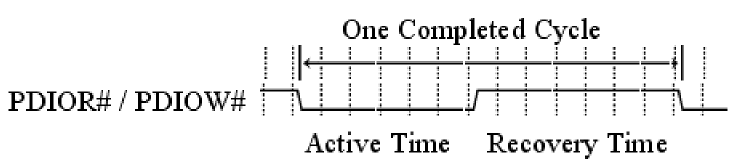
Offset Address: 45h (D15F0)
EIDE Control **Default Value: 82h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6	RW	0	**Reserved**
5	RO	0	**Reserved**
4	RW	0	**Interrupt Line Register (Rx3C) Write Protect** 0: Enable write to Rx3C 1: Disable write to Rx3C
3:2	RO	0	**Reserved**
1	RW	1b	**Flush Primary Channel Read DMA Data After Interrupt** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 46-49h (D15F0) - Reserved

Offset Address: 4B-4Ah (D15F0)
EIDE (Primary Channel) PIO Data Port & Multi-Word DMA Timing Control **Default Value: A8A8h**

The following waveform defines the Active Pulse Width and Recovery Time for the EIDE PDIOR# and PDIOW# signals when accessing the data ports (1f0h):



The actual pulse width is the encoded value in the field plus one in unit of PCI clocks. For example, if the value of the field is 1010b (10 decimal), the active pulse width or recovery time is 11 PCI clocks.

Bit	Attribute	Default	Description
15:12	RW	1010b	**IDE Drive 0 Active Pulse Width (Master)**
11:8	RW	1000b	**IDE Drive 0 Recovery Time (Master)**
7:4	RW	1010b	**IDE Drive 1 Active Pulse Width (Slave)**
3:0	RW	1000b	**IDE Drive 1 Recovery Time (Slave)**

Offset Address: 4Ch (D15F0)

Address Setup Time **Default Value: F0h**

The following fields define the Address Setup Time. The Address Setup Time is measured from the point when address signals are stable to the point when PDIOR# and PDIOW# are asserted. The IDE specification requires the setup time to not exceed 1T. However, this chip provides flexibility for devices that could not meet the 1T requirement.

Bit	Attribute	Default	Description
7:6	RW	11b	**IDE Drive 0 Address Setup Time (Master)** 00: 1T 01: 2T 10: 3T 11: 4T
5:4	RW	11b	**IDE Drive 1 Address Setup Time (Slave)** 00: 1T 01: 2T 10: 3T 11: 4T
3:0	RO	0	**Reserved**

Note: Address Setup Time = (Program Value + 1) * 30 ns, 1T = 30ns.

Offset Address: 4D-4Eh (D15F0) – Reserved

Offset Address: 4Fh (D15F0)

EIDE (Primary Channel) Non-Data Port Access Timing **Default Value: B6h**

IDE Non-Data Port (1f1h ~ 1f7h) access timing control: pulse width = (Program Value + 1) * 30ns.

Bit	Attribute	Default	Description
7:4	RW	Bh	**DIOR# / DIOW# Active Pulse Width**
3:0	RW	6h	**DIOR# / DIOW# Recovery Time**

Offset Address: 50-51h (D15F0) - Reserved

Offset Address: 52h (D15F0)

EIDE (Primary Channel) Slave Ultra DMA Mode Control **Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	**Way to Enable Ultra DMA Mode for Slave Device** 0: Enabled by the Set Feature (EFh) command 1: Ultra DMA On/Off is decided by the setting of Rx52[6]
6	RW	0	**Ultra DMA Mode Enable** 0: Disable 1: Enable
5	RO	0	**Current Transfer Mode** 0: Multi-words DMA Mode or PIO Mode 1: Ultra DMA Mode
4	RW	0	**Cable Type Reporting** This bit should be set by software like the System BIOS. 0: 40-pin cable is used 1: 80-pin cable is used
3:0	RW	7h	**Ultra DMA Write Strobe Timing Control** 0: (Program value + 2) * 7.5ns 1: (Program value + 2) * 10ns (for Ultra DMA 100) 2-15: (Program value + 2) * 7.5ns

Offset Address: 53h (D15F0)
EIDE (Primary Channel) Master Ultra DMA Mode Control **Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	**Way to Enable Ultra DMA Mode for Master Device** 0: Enabled by the Set Feature (EFh) command 1: Ultra DMA On/Off is decided by the setting of Rx52[6]
6	RW	0	**Ultra DMA Mode Enable** 0: Disable 1: Enable
5	RO	0	**Current Transfer Mode** 0: Multi-words DMA Mode or PIO Mode 1: Ultra DMA Mode
4	RW	0	**Cable Type Reporting** This bit should be set by software like the System BIOS. 0: 40-pin cable is used 1: 80-pin cable is used
3:0	RW	7h	**Ultra DMA Write Strobe Timing Control** 0: (Program value + 2) * 7.5ns 1: (Program value + 2) * 10ns (for Ultra DMA 100) 2-15: (Program value + 2) * 7.5ns

Offset Address: 54-AFh (D15F0) – Reserved

Legacy / Back Door Registers (B0-BFh)

Offset Address: B1-B0h (D15F0)
Power Management Capability ID **Default Value: 0001h**

Bit	Attribute	Default	Description
15:8	RO	0	**Fixed at 0**
7:0	RO	01h	**Capability ID** A PCI power management capability pointer.

Offset Address: B3-B2h (D15F0)
Power Management Interface Revision **Default Value: 0002h**

Bit	Attribute	Default	Description
15:3	RO	0	**Fixed at 0**
2:0	RO	010b	**Power Management Interface Revision** Indicates that this function compiles with Revision 1.1 of PCI Power Management Interface Spec.

Offset Address: B5-B4h (D15F0)
Power Management Capability Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Fixed at 0**
1:0	RW	00b	**Power Management Capability Status** 00: D0 11: D3 Hot Others: Reserved

Offset Address: B6-B8h (D15F0) – Reserved

Offset Address: B9h (D15F0)
Interrupt Back Door **Default Value: 01h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	001b	**Native Mode Interrupt Pin Setting** 001: Assert interrupt through INTA#. 010: Assert interrupt through INTB# 011: Assert interrupt through INTC# 100: Assert interrupt through INTD# Others: Reserved The value must be set to 001b so PCI spec can be complied.

Offset Address: BB-BAh (D15F0)
Device ID (IDE) Back Door **Default Value: C409h**

Bit	Attribute	Default	Description
15:0	RW	C409h	**Device ID (Rx2-3 IDE) Back Door**

Offset Address: BD-BCh (D15F0)
Subsystem Vendor ID Back Door **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	**Subsystem Vendor ID (Rx2C-2D) Back Door**

Offset Address: BF-BEh (D15F0)
Subsystem ID Back Door **Default Value: C409h**

Bit	Attribute	Default	Description
15:0	RW	C409h	**Subsystem ID (Rx2E-2F) Back Door**

EIDE Registers (C0-FFh)

Offset Address: C0h (D15F0) – Reserved

Offset Address: C1h (D15F0)
EIDE Configuration **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**EIDE Primary PIO Read Prefetch Enable** 0: Disable 1: Enable
6	RW	0	**EIDE Primary PIO Post Write Enable** 0: Disable 1: Enable
5:4	RO	0	**Reserved**
3	RW	0	**Reserved**
2:0	RW	010b	**Reserved (Do Not Program)**

Offset Address: C2h (D15F0)
Reserved Registers **Default Value: 09h**

Bit	Attribute	Default	Description
7:0	RW	09h	**Reserved (Do Not Program)**

Offset Address: C3h (D15F0)

EIDE FIFO Threshold — **Default Value: 01h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:2	RO	0	**Reserved**
1:0	RW	01b	**EIDE (Primary Channel) FIFO** This field determines the FIFO threshold before the primary channel FIFO is flushed. 00: FIFO is flushed when reaching 1/4 full. 01: FIFO is flushed when reaching 1/2 full. 10: FIFO is flushed when reaching 3/4 full. 11: FIFO is flushed when completely filled up (Can not be used when UDMA is read) Check RxF2 for additional FIFO threshold control.

Notes:
If RxF2[4] = 1, bits [1:0] select the threshold for Device-to-Memory data transfer.
If RxF2[4] = 0, bits [1:0] select the threshold for both Device-to-Memory and Memory-to-Device data transfer.

Offset Address: C4h (D15F0)

EIDE Configuration 1 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**EIDE PIO Read Pre-Fetch Byte Counter** 0: Disable. Pre-fetch will continue when FIFO has vacancy. 1: Enable. The pre-fetch byte count is determined by RxE1-E0[11:0] for EIDE PIO Read.
3	RW	0	**Bus Master IDE Status Register Read Retry** Determines whether a read to the bus master IDE status register is retried when DMA operation is not complete. 0: Disable. Reads will return status even if DMA operation is not complete 1: Enable. Reads of the status register are automatically retried while DMA operation is not complete.
2	RW	0	**Packet Command Pre-fetch** Determines whether pre-fetching is enabled for packet commands. Packet commands are commands for ATAPI, which is used for devices such as CD-ROM drives. 0: Disable 1: Enable
1	RW	0	**Reserved**
0	RW	0	**Ultra DMA Host Transfer Termination** 0: Enable. The Ultra DMA host must wait until at least the first transfer is completed before it can terminate a transaction. 1: Disable

Offset Address: C5h (D15F0) – Reserved

Offset Address: C6h (D15F0)

EIDE Configuration 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RW	0	**Reserved**

Offset Address: C7-D3h (D15F0) - Reserved

Offset Address: D4h (D15F0)

EIDE Configuration 3 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	**IRQ14 Usage when IDE Channel is Disabled** 0: Release IRQ14 for system usage when IDE Channel is disable (i.e. Rx40[1] is cleared) 1: IRQ14 is reserved.
6	RW	0	**Reserved**
5	RW	0	**Clear Native Mode Interrupt on Falling Edge of Gated Interrupt** 0: Disable 1: Enable. The interrupt will be automatically cleared on the falling edge of the gated interrupt.
4	RW	0	**Reserved**
3	RW	1b	**Prefetch Line Count** This bit determines how many memory lines are prefetched for IDE transactions. 0: Prefetch 1 line 1: Prefetch 2 lines (16 DoubleWords).
2	RW	1b	**Change Drive Clears All FIFO & Internal States** 0: Disable 1: When command switch from one drive to another drive on the same channel, the controller will terminate the outstanding transactions involving the previous drive.
1:0	RW	0	**Reserved**

Offset Address: D5h (D15F0)

EIDE Clock Gating **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Clock Gating for 33MHz** 0: Enable 1: Disable
3	RW	0	**FIFO 133/100 MHz Dynamic Clock Gating** 0: Enable 1: Disable
2	RW	0	**Reserved**
1	RW	0	**EIDE 133/100 MHz Dynamic Clock Gating** 0: Enable 1: Disable
0	RW	0	**EIDE 66 MHz Dynamic Clock Gating** 0: Enable 1: Disable

Offset Address: D6-DFh (D15F0) - Reserved

Offset Address: E1-E0h (D15F0)

EIDE Sector Size (for Pre-fetch Control) **Default Value: 0200h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11:0	RW	200h	**Prefetch Sector Size (In Unit of Byte)**

Offset Address: E2-EFh (D15F0) - Reserved

Offset Address: F0h (D15F0)

EIDE (Primary Channel) Status **Default Value: 02h**

Bit	Attribute	Default	Description
7	RO	0	**Interrupt Status** 0: No interrupt 1: Interrupted
6	RO	0	**PIO Prefetch Status** 0: No PIO prefetch 1: IDE controller is doing PIO prefetch
5	RO	0	**PIO Post Write Status** 0: No PIO Post write 1: IDE controller is doing PIO Post write
4	RO	0	**DMA Read Operation Status** 0: No DMA read operation 1: IDE controller is doing DMA read operation
3	RO	0	**DMA Write Operation Status** 0: No DMA write operation 1: IDE controller is doing DMA write operation
2	RO	0	**Bus Master Operation Complete** 0: Complete 1: Not complete
1	RO	1b	**FIFO Empty Status** 0: Not empty 1: Empty
0	RO	0	**External DMA Request** 0: No external DMA request 1: There is an external DMA request

Offset Address: F1h (D15F0)

Primary Channel (IDE) Interrupt Gating **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	1b	**Interrupt Gating** 0: Disable 1: Enable (IRQ output gated until FIFO is completed flushed.)

Offset Address: F2h (D15F0)

EIDE FIFO Threshold Control **Default Value: 24h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	1b	**Enable Reset IO Base Address** 0: Disable 1: Enable
4	RW	0	**Two FIFO Thresholds** 0: Disable (Use one threshold, defined in RxC3[1:0], for both direction of data transfer between Device and Memory) 1: Enable (Memory-to-Device and Device-to-Memory use RxF2[3:2] and RxC3[1:0] settings, respectively as threshold settings)
3:2	RW	01b	**Memory-to-Device FIFO Threshold** 00: 1/4 01: 1/2 10: 3/4 11: Full
1:0	RO	0	**Reserved**

Offset Address: F3-FFh (D15F0) – Reserved

Bus Master IDE I/O Space

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details. D15F0 Rx23-20h is the base address of Bus Master IDE I/O Registers.

Bus Master Controller (00-0Fh)

Offset Address: 00h (IDE-IO)
Primary Channel Bus Master IDE Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Channel Bus Master IDE Command**

Offset Address: 01h (IDE-IO) - Reserved

Offset Address: 02h (IDE-IO)
Primary Channel Bus Master Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	**Primary Channel Bus Master Status**

Offset Address: 03h (IDE-IO) - Reserved

Offset Address: 07-04h (IDE-IO)
Primary Channel Bus Master IDE Descriptor Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Primary Channel Bus Master IDE Descriptor Table Pointer**

Offset Address: 08h (IDE-IO)
Secondary Channel Bus Master IDE Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Channel Bus Master IDE Command**

Offset Address: 09h (IDE-IO) - Reserved

Offset Address: 0Ah (IDE-IO)
Secondary Channel Bus Master Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	**Secondary Channel Bus Master Status**

Offset Address: 0Bh (IDE-IO) - Reserved

Offset Address: 0F-0Ch (IDE-IO)
Secondary Channel Bus Master IDE Descriptor Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Secondary Channel Bus Master IDE Descriptor Table Pointer**

DEVICE 16 FUNCTION 0-2 (D16F0-F2): USB 1.1 UHCI PORTS 0-5

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Device 16 Function 0-2 PCI configuration space of the chip. The USB I/O registers are defined in UHCI specification v1.1. The registers are identical in the Device 16 Functions 0-2 where each function controls different USB ports (function 0 for ports 0-1, function 1 for ports 2-3, and function 2 for ports 4-5).

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D16F0-F2)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D16F0-F2)

Device ID **Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RO	3038h	**Device ID**

Offset Address: 05-04h (D16F0-F2)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable 1: Disable
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidate**
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles).
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RW	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D16F0-F2)
PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01. 00: Fast 01: Medium 10: Slow 11: Reserved
8:4	RO	01h	**Fixed at 01h (for PCI PMI)**
3	RW1C	0	**Interrupt Status**
2:0	RO	0	**Fixed at 0 (for PCI PMI)**

Offset Address: 08h (D16F0-F2)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D16F0-F2)
Class Code **Default Value: 0C 0300h**

Bit	Attribute	Default	Description
23:0	RO	0C0300h	**Class Code** 0C0300h indicates the USB1.1 Host Controller.

Offset Address: 0Ch (D16F0-F2)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D16F0-F2)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Latency Timer**

Offset Address: 0Eh (D16F0-F2)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h indicates a multi-function device.

Offset Address: 0Fh (D16F0-F2)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 0.

Offset Address: 10-1Fh (D16F0-F2) – Reserved

Offset Address: 23-20h (D16F0-F2)

USB I/O Register Base Address — **Default Value: 0000 FCE1h**

Bit	Attribute	Default	Description
31:16	RW	0	**Reserved**
15:5	RW	7E7h	**USB I/O Register Base Address [15:5]** Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5].
4:0	RO	01h	**32-Byte Aligned IO Space**

Offset Address: 24-2Bh (D16F0-F2) – Reserved

Offset Address: 2D-2Ch (D16F0-F2)

Subsystem Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW1	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D16F0-F2)

Subsystem ID — **Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RW1	3038h	**Subsystem ID**

Offset Address: 30-33h (D16F0-F2) – Reserved

Offset Address: 34h (D16F0-F2)

Capability Pointer — **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability Pointer** This register contains the offset address from the start of the configuration space. Fixed at 80h.

Offset Address: 35-3Bh (D16F0-F2) – Reserved

Offset Address: 3Ch (D16F0-F2)

Interrupt Line — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**USB Interrupt Routing** 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disabled

Offset Address: 3Dh (D16F0-F2)

Interrupt Pin (D16F0) **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Interrupt Pin (D16F1) **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Interrupt Pin** Fixed at 02h (INTB#).

Interrupt Pin (D16F2) **Default Value: 03h**

Bit	Attribute	Default	Description
7:0	RO	03h	**Interrupt Pin** Fixed at 03h (INTC#).

Offset Address: 3E-3Fh (D16F0-F2) – Reserved

USB 1.1-Specific Configuration Registers (40-FFh)

Offset Address: 40h (D16F0-F2)

Control Register 1 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**Babble Option** This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. 0: Automatically disable babbled port when EOF babble occurs. 1: Do not disable babbled port.
5	RW	0	**Reserved**
4	RW	0	**Frame Interval Select** 0: 1ms frame time 1: 0.1ms frame time
3	RW	0	**USB Data Length Option** 0: Supports Transfer Descriptor length up to 1280 bytes 1: Supports Transfer Descriptor length up to 1023 bytes
2	RW	0	**Improve FIFO Latency** 0: Improve latency if packet size < 64 bytes. 1: Disable improvement.
1	RW	0	**DMA Option** 0: Enhanced performance (8 DW burst access with better FIFO latency). 1: Normal performance (16 DW burst access with normal FIFO latency).
0	RW	0	**Reserved**

Offset Address: 41h (D16F0-F2)

Control Register 2 — **Default Value: 12h**

Bit	Attribute	Default	Description
7	RW	0	**USB 1.1 Improvement for EOP** This bit controls whether USB Specification 1.1 or 1.0 is followed when a stuffing error occurs before an EOP (End-Of-Packet). A stuffing error results when the receiver sees seven consecutive ones in a packet. Under USB specification 1.1, when this occurs in the interval just before an EOP, the receiver will accept the packet. Under USB specification 1.0, the packet is ignored. 0: USB Spec 1.1 Compliant (packet accepted) 1: USB Spec 1.0 Compliant (packet ignored)
6:5	RW	0	**Reserved**
4	RW	1b	**Reserved (Do Not Program)**
3	RW	0	**Reserved**
2	RW	0	**I/ O Port 60/64 Trap Option** Under the UHCI spec, port 60 / 64 is trapped only when its corresponding enable bits are set. When this bit is set, trap can be set without checking the enable bits. 0: Set trap 60/64 status bits without checking enable bits. 1: Set trap 60/64 status bits only when trap 60/64 enable bits are set.
1	RW	1b	**A20Gate Pass Through Option** This bit controls whether the A20Gate pass-through sequence (as defined in UHCI) is followed. The A20Gate sequence consists of 4 commands. When this bit is 0, the 4-command sequence is followed. When this bit is 1, the last command (write FFh to port 64) is skipped. 0: A20GATE Pass-through command sequence as defined in UHCI. 1: Last command skipped.
0	RO	0	**Reserved**

Offset Address: 42h (D16F0-F2)

Control Register 3 — **Default Value: 03h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Hold Data Transmission till FIFO Reaches Transmission Threshold** 0: Enable 1: Disable
1:0	RW	11b	**Reserved (Do Not Program)**

Offset Address: 43h (D16F0-F2)

Control Register 4 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Continue Transmitting Erroneous Data When FIFO Underrun** 0: Enable 1: Disable
2	RW	0	**Issue CRC Error Instead of Stuffing Error on FIFO Underrun** 0: Enable 1: Disable
1:0	RW	0	**Reserved**

Offset Address: 44-47h (D16F0-F2) – Reserved

Offset Address: 48h (D16F0-F2)
Control Register 5 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6:3	RW	0	**Reserved**
2	RW	0	**Issue Bad CRC5 in SOF After FIFO Underrun** 0: Enable 1: Disable
1	RW	0	**Lengthen PreSOF Time** The preSOF time point determines whether there is enough time in the remaining frame period to perform a 64-byte transaction. It prevents a packet that may not fit in the remaining frame period from being initiated. This bit controls whether the preSOF time point is moved back so that the preSOF time is lengthened. 0: Disable 1: Enable (PreSOF time lengthened)
0	RW	0	**Issue Non-Zero Bad CRC Code on FIFO Underrun** A FIFO underrun occurs when there is no data in the FIFO to supply data transmission. When this occurs, the controller invalidates the data by sending an incorrect CRC code to the device. This bit controls the type of incorrect CRC sent. 0: Non zero CRC (recommended) 1: All zero CRC This option isn't really needed now as non-zero CRC always works.

Offset Address: 49h (D16F0-F2)
Control Register 6 **Default Value: 0Bh**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Bypass 32KHz RTC Clock, Use Internal 1.5MHz Clock for USB 1.1 LS Controller Instead** 0: Disable (Use 32KHz RTC clock) 1: Enable (Use 1.5MHz Clock for USB 1.1 LS Controller)
4	RW	0	**Reset USBC Internal 12MHz Clock for UHCI Divider from 48MHz Clock** When this bit transfers from 0 to 1, 12MHz Clock for UHCI divider is reset.
3:2	RW	10b	**Reserved (Do Not Program)**
1	RW	1b	**EHCI Supports PME Assertion in D3 Cold State** 0: Not Supported 1: Supported
0	RW	1b	**UHCI Supports PME Assertion in D3 Cold State** 0: Not Supported 1: Supported

Offset Address: 4Ah (D16F0-F2)
Control Register 7 **Default Value: A0h**

Bit	Attribute	Default	Description
7:3	RW	14h	**USB 1.1 Bus Timeout Parameter** ***For FS mode:*** Timeout Parameter cycle of 12MHz is taken as the judgment of USB1.1 Bus timeout. ***For LS mode:*** Timeout Parameter cycle of 1.5MHz is taken as the judgment of USB1.1 Bus timeout.
2	RW	0	**Reserved**
1	RW	0	**Enable Stop Bus Master Cycle If HALT Bit Is Asserted** 0: Disable 1: Enable
0	RW	0	**Use External 60 MHz Clock** Set this bit to use external 60 MHz input clock. 0: Disable 1: Enable

Offset Address: 4Bh (D16F0-F2)

Control Register 8 **Default Value: 8Bh**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6	RW	0	**Enable 66MHz New UHCI Dynamic Scheme (UHCI_PCLK66_PD_EN)** 0: Disable 1: Enable
5	RW	0	**Enable 33MHz New UHCI Dynamic Scheme (UHCI_PCLK33_PD_EN)** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	1b	**Reserved (Do Not Program)**
2	RW	0	**Reserved**
1	RW	1b	**Reserved (Do Not Program)**
0	RW	1b	**Enable Clock Auto Stop** 0: Disable (No Stop) 1: Enable (Auto Stop)

Offset Address: 4Ch (D16F0-F2)

Control Register 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Reserved**

Offset Address: 4D-5Fh (D16F0-F2) – Reserved

Offset Address: 60h (D16F0-F2)

Serial Bus Release Number **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Serial Bus Release Number** Fixed at 10h.

Offset Address: 61-7Fh (D16F0-F2) – Reserved

Offset Address: 83-80h (D16F0-F2)

Power Management Capability **Default Value: FFC2 0001h**

Bit	Attribute	Default	Description
31:0	RO	FFC2 0001h	**Power Management Capability** If Rx49[0] = 1, this register is fixed at FFC2 0001h. If Rx49[0] = 0, this register is fixed at 7E0A 0001h. Please refer to the “PCI Bus Power Management Interface Specification Revision 1.1 Chapter 3.2” for details.

Offset Address: 84h (D16F0-F2)

Power Management Capability Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power Management Capability Status** 00: D0 01: Reserved 10: Reserved 11: D3 Hot

Offset Address: 85-BFh (D16F0-F2) – Reserved

Offset Address: C1-C0h (D16F0-F2)
Legacy Support (for UHCI v1.1 Compliant) **Default Value: 2000h**

Bit	Attribute	Default	Description
15	RW1C	0	**End of A20Gate Pass Through Status (A20PTS)** 1 indicates A20Gate pass through sequence has ended.
14	RO	0	**Reserved** Fixed to 0.
13	RW	1b	**USB PIRQ Enable (USBPIRQDEN)** 0: Disable 1: Enable
12	RO	0	**USB IRQ Status (USBIRQS)** 1 indicates USB IRQ is active.
11	RW1C	0	**Trap By 64h Write Status (TBY64W)** 1 indicates a write to port 64h occurred.
10	RW1C	0	**Trap By 64h Read Status (TBY64R)** 1 indicates a read to port 64h occurred.
9	RW1C	0	**Trap By 60h Write Status (TBY60W)** 1 indicates a write to port 60h occurred.
8	RW1C	0	**Trap By 60h Read Status (TBY60R)** 1 indicates a read to port 60h occurred.
7	RW	0	**SMI At End Of Pass Through Enable (SMIEPTE)** 0: Disable 1: Enable
6	RO	0	**Pass Through Status (PSS)** 1 indicates A20Gate pass through sequence is currently in progress.
5	RW	0	**A20Gate Pass Through Enable (A20PTEN)** 0: Disable 1: Enable
4	RW	0	**Trap/SMI ON IRQ Enable (USBSMIEN)** 0: Disable 1: Enable
3	RW	0	**Trap/SMI On 64h Write Enable (64WEN)** 0: Disable 1: Enable
2	RW	0	**Trap/SMI On 64h Read Enable (64REN)** 0: Disable 1: Enable
1	RW	0	**Trap/SMI On 60h Write Enable (60WEN)** 0: Disable 1: Enable
0	RW	0	**Trap/SMI On 60h Read Enable (60REN)** 0: Disable 1: Enable

Note: This register provides control and status capability for the legacy keyboard and mouse functions. Please refer to UHCI Spec. for further details.

Offset Address: C2-FFh (D16F0-F2) – Reserved

USB 1.1 I/O Space

USB 1.1 I/O Registers (00-13h)

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset Address: 01-00h (USB 1.1-IO)
USB Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RW	0	**Max Packet**
6	RW	0	**Configure Flag (CF)**
5	RW	0	**Software Debug (SWDBG)**
4	RW	0	**Force Global Resume (FGR)**
3	RW	0	**Enter Global Suspend Mode (EGSM)**
2	RW	0	**Global Reset (GRESET)**
1	RW	0	**Host Controller Reset (HCRESET)**
0	RW	0	**Run / Stop (RS)**

I/O Offset Address: 03-02h (USB 1.1-IO)
USB Status **Default Value: 0020h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	1b	**Host Controller Halted**
4	RW1C	0	**Host Controller Process Error**
3	RW1C	0	**Host System Error**
2	RW1C	0	**Resume Detect**
1	RW1C	0	**USB Error Interrupt**
0	RW1C	0	**USB Interrupt (USBINT)**

I/O Offset Address: 05-04h (USB 1.1-IO)
USB Interrupt Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3	RW	0	**Short Packet Interrupt Enable**
2	RW	0	**Interrupt On Complete (IOC) Enable**
1	RW	0	**Resume Interrupt Enable**
0	RW	0	**Timeout / CRC Interrupt Enable**

I/O Offset Address: 07-06h (USB 1.1-IO)
Frame Number **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10:0	RW	0	**Frame List Current Index / Frame Number**

I/O Offset Address: 0B-08h (USB 1.1-IO)
Frame List Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Frame List Base Address**
11:0	RO	0	**Reserved**

I/O Offset Address: 0Ch (USB 1.1-IO)
Start of Frame Modify **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:0	RW	40h	**Start of Frame Timing Value**

I/O Offset Address: 0D-0Fh (USB 1.1-IO) – Reserved

I/O Offset Address: 11-10h (USB 1.1-IO)
Port 0 Status / Control **Default Value: 0080h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved.**
12	RW	0	**Suspend**
11:10	RO	0	**Reserved**
9	RW	0	**Port Reset**
8	RO	0	**Low Speed Device Attached**
7	RO	1b	**Reserved (Do Not Program)**
6	RW	0	**Resume Detect**
5:4	RO	0	**Line Status**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 13-12h (USB 1.1-IO)

Port 1 Status / Control **Default Value: 0080h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Suspend**
11:10	RO	0	**Reserved**
9	RW	0	**Port Reset**
8	RO	0	**Low Speed Device Attached**
7	RO	1b	**Reserved (Do Not Program)**
6	RW	0	**Resume Detect**
5:4	RO	0	**Line Status**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

DEVICE 16 FUNCTION 4 (D16F4): USB 2.0 EHCI

This Universal Serial Bus host controller interface is fully compatible with EHCI specification v1.0. There are two sets of software accessible registers: PCI configuration registers and USB memory mapped I/O registers. The PCI configuration registers are located in the Device 16 Function 4 PCI configuration space of the chip. The USB memory mapped I/O registers are defined in EHCI specification v1.0.
The EHCI memory mapped I/O base address is located in Rx13-10.

PCI Configuration Space

All registers in D16F4 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 16 and function number 4.

Header Registers (00-3Fh)

Offset Address: 01-00h (D16F4)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D16F4)
Device ID **Default Value: 3104h**

Bit	Attribute	Default	Description
15:0	RO	3104h	**Device ID Code**

Offset Address: 05-04h (D16F4)
PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** Fixed at 0b (Not supported).
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidate**
3	RO	0	**Reserved** Special cycle monitoring. Fixed at 0b (Not supported).
2	RW	0	**Bus Master**
1	RW	0	**Memory Space**
0	RW	0	**I/O Space**

Offset Address: 07-06h (D16F4)
PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8:4	RO	01h	**Fixed at 01h (for PCI PMI)**
3	RW1C	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D16F4)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D16F4)
Class Code **Default Value: 0C 0320h**

Bit	Attribute	Default	Description
23:0	RO	0C0320h	**Class Code for USB2.0 EHCI Host Controller**

Offset Address: 0Ch (D16F4)
Cache Line Size **Default Value:00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D16F4)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Latency Timer**

Offset Address: 0Eh (D16F4)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D16F4)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 00h.

Offset Address: 13-10h (D16F4)
EHCI Memory Mapped I/O Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**EHCI Memory Mapped I/O Registers Base Address** Memory Address for the base of the USB 2.0 EHCI I/O Register block is corresponding to AD[31:8].
7:3	RO	0	**Reserved**
2:1	RO	00b	**Memory Mapping** Reads 00b for 32-bit addressing if Rx40[2] is 0. If Rx40[2] is set, these 2 bits are read as 10b for 64-bit addressing.
0	RO	0	**Reserved**

Offset Address: 17-14h (D16F4)
EHCI Memory Mapped I/O Base Address (High 32-bit) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO/RW	0	**EHCI Memory Mapped I/O Registers High 32-bit Base Address** If Rx40[2] is 0b, this register is RO as 0h. If Rx40[2] is 1b, this register is RW as high 32-bit Memory Base Address for the USB 2.0 EHCI Memory Mapped I/O Register block, corresponding to AD[63:32].

Offset Address: 18-2Bh (D16F4) – Reserved

Offset Address: 2D-2Ch (D16F4)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW1	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D16F4)
Subsystem ID **Default Value: 3104h**

Bit	Attribute	Default	Description
15:0	RW1	3104h	**Subsystem ID**

Offset Address: 30-33h (D16F4) – Reserved

Offset Address: 34h (D16F4)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability Pointer** This register contains the offset address from the start of the configuration space. Fixed at 80h.

Offset Address: 35-3Bh (D16F4) – Reserved

Offset Address: 3Ch (D16F4)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**USB Interrupt Routing** 0000: Disable 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disable

Offset Address: 3Dh (D16F4)
Interrupt Pin **Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	**Interrupt Pin** Fixed at 04h (INTD#).

Offset Address: 3E-3Fh (D16F4) – Reserved

USB 2.0-Specific Configuration Registers (40-FFh)

Offset Address: 40h (D16F4)

Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Babble Option** This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled. 0: Automatically disable babbled port when EOF babble occurs 1: Do not disable babbled port
5	RW	0	**Reserved**
4	RW	0	**Micro-Frame Interval Select** 0: 125 us micro-frame time 1: 31.25 us micro-frame time
3	RW	0	**Reserved**
2	RW	0	**DAC Enable** This is a PCI 64-bit DAC cycle enable bit. If this bit is enabled, USB2.0 controller could respond both DAC memory cycle and normal 32-bit PCI cycle. After setting this bit to 1b, Rx14[31:0] could be written as high 32-bit PCI memory base address and Rx10[2:1] is read as 10b. 0: Disable DAC cycle 1: Enable DAC cycle
1	RW	0	**DMA Option** Also used to control FIFO over/under run criteria. 0: 16 DW burst access 1: 8 DW burst access
0	RW	0	**Reserved**

Offset Address: 41h (D16F4) – Reserved

Offset Address: 42h (D16F4)

Control Register 2 **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Enable Check PRESOF for ITD OUT Transaction During Fetching Data from DRAM** If SB data bandwidth is slow down much more, ITD controller could not fetch enough data to be transmitted at current micro-Frame. So this transaction will cross the SOF, mostly for Multiple ITD transactions. Enable this bit, ITD controller will check PRESOF even at data fetching period. 0: Disable 1: Enable
5:3	RW	0	**Reserved**
2:0	RW	011b	**Reserved (Do Not Program)**

Offset Address: 43h (D16F4)

Control Register 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable 66MHz Dynamic Scheme** 0: Disable 1: Enable
6	RW	0	**Enable 33MHz Dynamic Scheme** 0: Disable 1: Enable
5:0	RW	0	**Reserved**

Offset Address: 44-47h (D16F4) – Reserved

Offset Address: 48h (D16F4)

Control Register 4 **Default Value: BEh**

Bit	Attribute	Default	Description
7	RW	1b	**USB 2.0 EOP Pattern (FEh) Error Check** 0: Disable 1: Enable
6	RW	0	**Extra Handshake Error Checking in Isochronous Transaction** 0: Disable 1: Enable
5	RW	1b	**DMA Burst Access** 0: Burst Enable 1: Burst Disable
4	RW	1b	**USB 2.0 Reference Bus Idle Status** When this bit is set to 1, the hardware refers to the bus idle status from PHY to check the start and the end of an incoming packet. 0: Disable 1: Enable
3	RW	1b	**Reserved (Do Not Program)**
2	RW	1b	**Reserved (Do Not Program)**
1	RW	1b	**USB 2.0 CRC16 Check Enable for Toggle Mismatch** 0: Disable 1: Enable
0	RW	0	**HS (High Speed) Port Align to Micro-Frame Boundary** 0: Align 1: Not Align

Offset Address: 49h (D16F4)

Control Register 5 **Default Value: 68h**

Bit	Attribute	Default	Description
7	RW	0	**MAC Allows More Delay between Transactions** The delay parameter could be specified in Rx4A. Unit is period of 60MHz clock. 0: Disable 1: Enable
6	RW	1b	**MAC Provides Timeout to Device When Receiver Detects Error** The delay parameter could be specified in Rx51. Unit is period of 33MHz PCI clock. 0: Disable 1: Enable
5	RW	1b	**EHCI Clock Auto Stop** 0: Disable (No stop) 1: Enable (Auto stop)
4	RW	0	**Auto Power Down Receiver Squelch Detector** 0: Auto power down 1: Always power up
3	RW	1b	**Enable New USB C4P State** 0: Disable 1: Enable
2	RW	0	**USB Analog PLL Control When Entering C4P State** 0: Not turn off 48MHz PLL 1: PMU will control to turn off PHY PLL in USBC (USB Controller)
1:0	RW	00b	**USB HS NULL-SOF (Null Start Of Frame) Valid Time Selection (for C4P Support). Rx64[2] and these 2 bits are combined to select NULL-SOF valid time** **{Rx64[2], Rx49[1:0]}:** 000: 2 micro frames 001: 4 micro frames 010: Invalid value 011: Invalid value 100: 8 micro frames 101: 16 micro frames 110: 24 micro frames 111: 32 micro frames

Offset Address: 4Ah (D16F4)

MAC Inter-Transaction Delay Parameter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**MAC Inter-Transaction Delay Parameter** Unit is period of 60MHz clock.

Offset Address: 4Bh (D16F4)
MAC Turn Around Time Parameter **Default Value: 09h**

Bit	Attribute	Default	Description
7	RW	0	**SOF (Start of Frame) Disconnects Detection Period** 0: SOF disconnects detection with the narrow window. 1: SOF disconnects detection with the larger window, 2 more periods of 60MHz clock.
6:5	RW	00b	**EHCI Sleep Time Select** 00: 1 us 01: 10 us 10: 10 us 11: 80 us
4	RW	0	**Disable Sending UTM_SOF (Start of Frame of USB Transceiver Macrolcell) When RUN Bit is Cleared** 0: Sending UTM_SOF when RUN bit (USB 2.0-MMIO Rx10[0]) is cleared 1: Do not send UTM_SOF when RUN bit is cleared
3:0	RW	9h	**USB 2.0 MAC Transmit Turn Around Time Parameter** Unit is period of 60MHz clock.

Offset Address: 4Ch (D16F4)
PHY Control 1 **Default Value: 12h**

Bit	Attribute	Default	Description
7	RW	0	**Resume ACK Control** 0: 20ms resume, then send ACK to C4P state resume request 1: Quickly send ACK to C4P state resume request
6	RW	0	**Reserved**
5	RW	0	**USB1.0 UTM (USB Transceiver Macrocell) Tx Speed Up** 0: Disable 1: Enable
4	RW	1b	**USB2.0 EHCI Debug Port Support Enable** 0: Disable 1: Enable
3	RW	0	**USB2.0 Receiver Fast Sync Pattern Detect** 0: Detect sync pattern only after receiving 1010b or 0101b data sequence 1: Always detect sync pattern
2	RW	0	**Enable USB2.0 Receiver Sync Pattern Detect with ‘J’_End** 0: Disable 1: Enable
1:0	RW	10b	**Squelch Detector Fine Tune** 125mv squelch level fine tune (USB2.0 PHY control signal) 00: 100mv 01: 112.5mv 10: 125mv 11: 137.5mv

Offset Address: 4Dh (D16F4)
PHY Control 2 **Default Value: 84h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6:3	RW	0	**Reserved**
2:0	RW	100b	**Reserved (Do Not Program)**

Offset Address: 4Eh (D16F4)
USB CP4 Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Reserved**

Offset Address: 4Fh (D16F4)
USB CP4 Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Enable Clear RUN Bit when EHCI_IDLE, if S/W Clears RUN Bit** 0: Enable clear RUN bit (USB 2.0-MMIO Rx10[0]) at any time, if S/W clear this bit 1: Enable clear RUN bit only when EHCI is idle, if S/W clear this bit
3:0	RW	0	**Reserved**

Offset Address: 50h (D16F4)

Test Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**USB 2.0 Doorbell Bit Function Patch** 0: Keep original setting 1: Fetch one more QH before de-asserting Doorbell bit
6:5	RW	0	**Reserved**
4:2	RO	0	**Reserved**
1	RW	0	**Reserved**
0	RO	0	**Reserved**

Offset Address: 51h (D16F4)

USB 2.0 MAC Timeout Parameter **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RW	60h	**USB 2.0 Receiver Timeout Parameter** The unit is byte time. According to the core spec, the host controller or a device expecting a response to a transmission must not timeout the transaction if the inter-packet delays in 736 and 816 bit times. The worst round trip delay is 721 bit times.

Offset Address: 52h (D16F4)

Control Register 6 **Default Value: 10h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	1b	**Reset NULLSOF and NULLSOF Counter When Exiting C4P State** 0: Disable 1: Enable
3	RW	0	**Send Out Interrupt of IOC and RollOver When USB is in C4P State** 0: Disable 1: Enable
2	RW	0	**Enable USB Responding to PMU C4P State Request by Entering / Exiting D3 State** 0: Enable 1: Disable (without entering / exiting D3 state)
1	RW	0	**Enable New PLL Power Down Scheme** When there is no high-speed device connection, power down PLL 0: Disable 1: Enable
0	RW	0	**USB Physical Circuitry Power Down Condition** 0: When the port is disabled or suspended. 1: When the port is disabled or suspended, or when there is no TX (transmit) activity.

Offset Address: 53h (D16F4)
C4P Control Register **Default Value: F0h**

Bit	Attribute	Default	Description
7	RW	1b	**C4P State Request Control** 0: USBC (USB controller) feedback to C4P request does not consider RUN bit (USB 2.0-MMIO Rx10[0]) and connect status 1: When RUN bit = 0, or when no device is connected, USBC feedback to C4P request is from PMU quickly.
6	RW	1b	**PLLOK Selection Control** 0: Use logic control PLLOK 1: Use circuit control PLLOK
5	RW	1b	**PORT6 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT6 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT6 is enabled
4	RW	1b	**PORT5 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT5 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT5 is enabled
3	RW	0	**PORT4 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT4 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT4 is enabled
2	RW	0	**PORT3 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT3 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT3 is enabled
1	RW	0	**PORT2 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT2 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT2 is enabled
0	RW	0	**PORT1 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT1 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT1 is enabled

Offset Address: 54h (D16F4)
PHY Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DPLL Non-Squelch (NSQ) Offset Setting** 00: 0ps 10: 43~135ps 01: -43~-135ps 11: 86~270ps
5	RO	0	**Reserved**
4	RO	0	**DPLL BIST Pattern Matching Flag**
3	RW	0	**Reset DPLL for BIST** 0: Disable 1: Enable
2	RW	0	**DPLL BIST Setting for Different Test Pattern 2** 0: Off 1: 1T phase-shift
1	RW	0	**DPLL BIST Setting for Different Test Pattern 1** 0: Off 1: 1T duty-offset
0	RW	0	**DPLL BIST Setting for Different Test Pattern 0** 0: Off 1: 1T pulse-shift

Offset Address: 55h (D16F4)
PHY Control 4 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**Disconnection Level Fine Tune – For Port 3** 00: 525mv 10:575mv 01: 550mv 11:600mv
5:4	RW	10b	**Disconnection Level Fine Tune – For Port 2** 00: 525mv 10:575mv 01: 550mv 11:600mv
3:2	RW	10b	**Disconnection Level Fine Tune – For Port 1** 00: 525mv 10:575mv 01: 550mv 11:600mv
1:0	RW	10b	**Disconnection Level Fine Tune – For Port 0** 00: 525mv 10:575mv 01: 550mv 11:600mv

Offset Address: 56h (D16F4)
PHY Control 5 — **Default Value: 0Ah**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	10b	**Disconnection Level Fine Tune – For Port 4** 00: 525mv 10:575mv 01: 550mv 11:600mv
1:0	RW	10b	**Disconnection Level Fine Tune – For Port 5** 00: 525mv 10:575mv 01: 550mv 11:600mv

Offset Address: 57h (D16F4)
PHY Control 6 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**High-Speed Tx Test Mode Register F** 0: Normal 1: Enter EPHY self-test mode
4	RW	0	**High-Speed Tx Test Mode Register E** 0: Normal 1: Enter EPHY self-test mode
3	RW	0	**High-Speed Tx Test Mode Register D** 0: Normal 1: Enter EPHY self-test mode
2	RW	0	**High-Speed Tx Test Mode Register C** 0: Normal 1: Enter EPHY self-test mode
1	RW	0	**High-Speed Tx Test Mode Register B** 0: Normal 1: Enter EPHY self-test mode
0	RW	0	**High-Speed Tx Test Mode Register A** 0: Normal 1: Enter EPHY self-test mode

Offset Address: 58h (D16F4)
PHY Control 7 — **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	1b	**Detect High-Speed Disconnect During SOF Period** 0: Disable 1: Enable
1:0	RW	0	**Reserved**

Offset Address: 59h (D16F4)
PHY Control 8 — **Default Value: 0Bh**

Bit	Attribute	Default	Description
7	RW	0	**Disable PHY Auto Power-Down Feature** When set this bit, if port is suspended or is not owned by EHCI, the port will auto power-down. 0: Auto power-down 1: Disable Auto power-down
6	RW	0	**Transit POwner (Port Owner) Control** This bit controls port route logic to be programmable if port connection is not present, default is to transit POwner only at falling edge of connect status. 0: Falling edge 1: Level
5:4	RW	0	**Reserved**
3	RW	1b	**DPLL Fast Lock Enable** 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	1b	**Disable PHY Receiver Including Squelch Detector Power up Time Improvement** 0: Enable improvement 1: Disable improvement
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: 5B-5Ah (D16F4)

High-Speed Port Pad Termination Resistor Fine Tune 1 **Default Value: 8888h**

Bit	Attribute	Default	Description
15:12	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 0.** CTRL_A[3:1]: 100: 45ohm (default) 010: 48ohm 001: 52ohm. CTRL_A[0] : 0: 0% 1: -33%
11:8	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 1** Refer to the information provided in bits [15:12].
7:4	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 2** Refer to the information provided in bits [15:12].
3:0	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 3** Refer to the information provided in bits [15:12].

Offset Address: 5Ch (D16F4)

PHY Control 9 **Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	**DPLL Zero Phase Start Select** 0: ZPS takes 8-bit times to start 1: ZPS takes 4-bit times to start
6	RW	0	**High Speed Transmitter** Used for high speed transmitter, no DPLL. 0: Normal 1: Rise / fall time increase 100ps
5:4	RW	00b	**DPLL Input Data Delay Select** 00: 0ps 01: -43~-135ps 10: 43~135ps 11: 86~270ps
3:2	RW	01b	**DPLL Track Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)
1:0	RW	11b	**DPLL Lock Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)

Offset Address: 5Dh (D16F4)

High-Speed Port Pad Termination Resistor Fine Tune 2 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 4** Refer to the information provided in Rx5B-5A[15:12].
3:0	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 5** Refer to the information provided in Rx5B-5A [15:12].

Offset Address: 5Eh (D16F4)

PHY Control 10 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Internal Current Source Increment** 00: No increment 01: 1% 10: 2 % 11: 4%
5	RW	0	**USB Port 5 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
4	RW	0	**USB Port 4 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
3	RW	0	**USB Port 3 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
2	RW	0	**USB Port 2 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
1	RW	0	**USB Port 1 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
0	RW	0	**USB Port 0 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.

Offset Address: 5Fh (D16F4)
PHY Control 11 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**USB Port 5 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
4	RO	0	**USB Port 4 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
3	RO	0	**USB Port 3 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
2	RO	0	**USB Port 2 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
1	RO	0	**USB Port 1 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
0	RO	0	**USB Port 0 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.

Offset Address: 60h (D16F4)
Serial Bus Release Number **Default Value: 20h**

Bit	Attribute	Default	Description
7:0	RO	20h	**Serial Bus Release Number** Fixed at 20h for USB2.0.

Offset Address: 61h (D16F4)
Frame Length Adjustment **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	20h	**Frame Length Adjustment** This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. Please refer to “EHCI Specification for USB” Section 2.1.5.

Offset Address: 63-62h (D16F4)
Port Wake Capability **Default Value: 0001h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6:1	RW	0	**Port Wake Up Capability Mask** Bits [6:1] in the mask correspond to a physical port implemented on the current EHCI controller. Please refer to “EHCI Specification for USB” Section 2.1.6. 0: A zero in a bit position indicates that a device connected below the port can NOT be enabled as a wake-up device and the port may be NOT enabled for disconnect/connect or over-current events as wake-up events. 1: A one in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/connect or over-current events as wake-up events.
0	RO	1b	**Port Wake Capability Register Implementation** This bit indicates whether this Port Wake Capability register is implemented. Please refer to “EHCI Specification for USB” Section 2.1.6. 0: Port Wake Capability register is NOT implemented 1: Port Wake Capability register is implemented

Offset Address: 64h (D16F4)

USB CP4 Control 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Self-Wakeup microFrame Selection** 00: Generate Self-Wakeup signal every microFrame (125us) 01: Generate Self-Wakeup signal every 2 microFrames (250us) 10: Generate Self-Wakeup signal every 3 microFrames (375us) 11: Generate Self-Wakeup signal every 4 microFrames (500us)
5:4	RW	00b	**Self-Wakeup Time Selection** 00: Generate Self-Wakeup signal as close as HS SOF boundary 01: Generate Self-Wakeup signal as close as 1/4 HS SOF boundary 10: Generate Self-Wakeup signal as close as 2/4 HS SOF boundary 11: Generate Self-Wakeup signal as close as 3/4 HS SOF boundary
3	RW	0	**Enable Self-Wakeup Function during C4P State** 0: Disable Self-Wakeup function during C4P state 1: Eable Self-Wakeup function during C4P state
2	RW	0	**USB HS NULL-SOF (Null Start Of Frame) Valid Time Selection Extend bit2 (for C4P Support). Rx64[2] and Rx49[1:0] are combined to select NULL-SOF valid time {Rx64[2], Rx49[1:0]}:** 000: 2 micro frames 001: 4 micro frames 010: Invalid value 011: Invalid value 100: 8 micro frames 101: 16 micro frames 110: 24 micro frames 111: 32 micro frames
1	RW	0	**Enable USB2.0 HS ISO Device C4 Inhibition Mechanism** 0: System is NOT inhibited into C4 state if valid transactions with USB2.0 HS ISO devices 1: System is inhibited into C4 state if valid transactions with USB2.0 HS ISO devices.
0	RW	0	**Enable USB1.1 ISO Device C4 Inhibition Mechanism** 0: System is NOT inhibited into C4 state if valid transactions with USB1.1 ISO devices 1: System is inhibited into C4 state if valid transactions with USB1.1 ISO devices.

Offset Address: 65-67h (D16F4) – Reserved

Offset Address: 6B-68h (D16F4)

USB Legacy Support Extended Capability — **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RW	0	**USB Host Controller OS-owned Semaphore**
23:17	RO	0	**Reserved**
16	RW	0	**USB Host Controller BIOS-owned Semaphore**
15:8	RO	0	**Next EHCI Extended Capability Pointer**
7:0	RO	01h	**Capability ID** 01h identifies the capability as Legacy Support. Please also refer to EHCI Spec. Section 2.1.7 for more details.

Offset Address: 6F-6Ch (D16F4)
USB Legacy Support Control / Status — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW1C	0	**SMI on BAR**
30	RW1C	0	**SMI on PCI Command**
29	RW1C	0	**SMI on OS Ownership Change**
28:22	RO	0	**Reserved**
21	RO	0	**SMI on Ssync Advance**
20	RO	0	**SMI on Host System Error**
19	RO	0	**SMI on Frame List Rollover**
18	RO	0	**SMI on Port Change Detect**
17	RO	0	**SMI on USB Error**
16	RO	0	**SMI on USB Complete**
15	RW	0	**SMI on BAR Enable**
14	RW	0	**SMI on PCI Command Enable**
13	RW	0	**SMI on OS Ownership Enable**
12:6	RO	0	**Reserved**
5	RW	0	**SMI on Async Advance Enable**
4	RW	0	**SMI on Host System Error Enable**
3	RW	0	**SMI on Frame List Rollover Enable**
2	RW	0	**SMI on Port Change Enable**
1	RW	0	**SMI on USB Error Enable**
0	RW	0	**USB SMI Enable**

Offset Address: 70-7Fh (D16F4) – Reserved

Offset Address: 80h (D16F4)
Power Management Capability ID — **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Power Management Capability ID**

Offset Address: 81h (D16F4)
Next Item Pointer 1 — **Default Value: 88h**

Bit	Attribute	Default	Description
7:0	RO	88h	**Next Item Pointer 1** If Rx4C[4] = 1, this register is fixed at 88h. If Rx4C[4] = 0, this register is fixed at 00h.

Offset Address: 83-82h (D16F4)
Power Management Capability — **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:0	RO	FFC2h	**Power Management Capability** If D16F0-F2 Rx49[1]= 1, this register is fixed at FFC2h. If D16F0-F2 Rx49[1]= 0, this register is fixed at 7E0Ah. Please refer to the "PCI Bus Power Management Interface Specification Revision 1.1 Chapter 3.2" for details.

Offset Address: 85-84h (D16F4)
Power Management Capability Control / Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME Status** 0: Not active 1: Active
14:9	RO	0	**Reserved**
8	RW	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00: D0 01: D1 10: D2 11: D3 Hot

Offset Address: 86-87h (D16F4) – Reserved

Offset Address: 88h (D16F4)
Debug Port Capability ID **Default Value: 0Ah**

Bit	Attribute	Default	Description
7:0	RO	0Ah	**Debug Port Capability ID** If Rx4C[4] = 1, this register is fixed at 0Ah. If Rx4C[4] = 0, this register is fixed at 00h.

Offset Address: 89h (D16F4)
Next Item Pointer 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer 2**

Offset Address: 8B-8Ah (D16F4)
Debug Port Base Offset **Default Value: 20A0h**

Bit	Attribute	Default	Description
15:0	RO	20A0h	**Debug Port Base Offset** If Rx4C[4] = 1, this register is fixed at 20A0h If Rx4C[4] = 0, this register is fixed at 0000h

Offset Address: 8C-FFh (D16F4) – Reserved

EHCI USB 2.0 Memory Mapped I/O Registers (00-B3h)

These registers are compliant with the EHCI v1.0 standard. Refer to the EHCI v1.0 specification for further details.

EHCI Capabilities (00-0Bh)

Offset Address: 00h (USB 2.0-MMIO)
Capability Register Length **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Capability Register Length**

Offset Address: 01h (USB 2.0-MMIO)– Reserved

Offset Address: 03-02h (USB 2.0-MMIO)
Interface Version Number **Default Value: 0100h**

Bit	Attribute	Default	Description
15:0	RO	0100h	**Interface Version Number**

Offset Address: 07-04h (USB 2.0-MMIO)
Structure Parameters **Default Value: 0000 3206h**

Bit	Attribute	Default	Description
31:0	RO	0000 3206h	**Structure Parameters** If D16F4 Rx4C[4] = 1, fixed at 0010 3206h. If D16F4 Rx4C[4] = 0, fixed at 0000 3206h.

Offset Address: 0B-08h (USB 2.0-MMIO)
Capability Parameters **Default Value: 0000 6872h**

Bit	Attribute	Default	Description
31:0	RO	0000 6872h	**Capability Parameters**

Offset Address: 0C-0Fh (USB 2.0-MMIO) – Reserved

Host Controller Operations (10-9Fh)

Offset Address: 13-10h (USB 2.0-MMIO)
USB Command **Default Value: 0008 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RW	08h	**Interrupt Threshold Control**
15:8	RO	0	**Reserved**
7	RW	0	**Light Host Controller Reset**
6	RW	0	**Interrupt on Async Advance Doorbell**
5	RW	0	**Asynchronous Schedule Enable**
4	RW	0	**Periodic Schedule Enable**
3:2	RW	0	**Frame List Size**
1	RW	0	**Host Controller Reset**
0	RW	0	**Run / Stop**

I/O Offset Address: 17-14h (USB 2.0-MMIO)
USB Status **Default Value: 0000 1000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15	RO	0	**Asynchronous Schedule Status**
14	RO	0	**Periodic Schedule Status**
13	RO	0	**Reclamation**
12	RO	1b	**Host Controller Halted**
11:6	RO	0	**Reserved**
5	RW1C	0	**Interrupt on Async Advance**
4	RW1C	0	**Host System Error**
3	RW1C	0	**Frame List Rollover**
2	RW1C	0	**Port Change Detect**
1	RW1C	0	**USB Error Interrupt**
0	RW1C	0	**USB Interrupt**

I/O Offset Address: 1B-18h (USB 2.0-MMIO)
USB Interrupt Enable **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:6	RO	0	**Reserved**
5:0	RW	0	**USB Interrupt Enable** 0: Disable 1: Enable

I/O Offset Address: 1F-1Ch (USB 2.0-MMIO)
USB Frame Index **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	RO	0	**Reserved**
12:0	RW	0	**USB Frame Index**

I/O Offset Address: 23-20h (USB 2.0-MMIO)
4G Segment Selector **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**4G Segment Selector**

I/O Offset Address: 27-24h (USB 2.0-MMIO)
Frame List Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Frame List Base Address**
11:0	RO	0	**Reserved**

I/O Offset Address: 2B-28h (USB 2.0-MMIO)
Next Asynchronous List Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:5	RW	0	**Next Asynchronous List Address**
4:0	RO	0	**Reserved**

I/O Offset Address: 2C-4Fh (USB 2.0-MMIO) - Reserved

I/O Offset Address: 53-50h (USB 2.0-MMIO)
Configured Flag **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Configured Flag**

I/O Offset Address: 57-54h (USB 2.0-MMIO)
Port 0 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 5B-58h (USB 2.0-MMIO)

Port 1 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 5F-5Ch (USB 2.0-MMIO)

Port 2 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 63-60h (USB 2.0-MMIO)

Port 3 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 67-64h (USB 2.0-MMIO)

Port 4 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 6B-68h (USB 2.0-MMIO)

Port 5 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

Offset Address: 6C-9Fh (USB 2.0-MMIO) – Reserved

Debug Port Controller Operational Registers (A0-B3h)

Offset Address: A3-A0h (USB 2.0-MMIO)

Debug Port Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**Force the Ownership of the Debug Port to the EHCI Controller (Owner)** 0: Disable 1: Enable
29	RO	0	**Reserved**
28	RW	0	**Enable Debug Port (Enabled)** 0: Disable 1: Enable
27:17	RO	0	**Reserved**
16	RW1C	0	**Transaction Request Complete (Done)** 0: Not complete 1: Complete
15:11	RO	0	**Reserved**
10	RW	0	**Port In Use (In Use)** 0: Port available. 1: Port in use
9:7	RO	000b	**Exception Error Type (Exception)** 000: None 001: Transaction error or babble: indicates the USB2 transaction had an error (CRC, bad PID, timeout, packet babble, etc.) 010: HW error. Request was attempted (or in progress) when port was suspended or reset. Others: Reserved
6	RO	0	**Error Status (Error / Good#)** 0: No error occurred 1: Error occurred
5	RW	0	**Start a Request (Go)** 0: Not start a request 1: Notify hardware to perform a request
4	RW	0	**Current Request Type (Write / Read#)** 0: Current request for read 1: Current request for write
3:0	RW	0	**Data Length**

Offset Address: A7-A4h (USB 2.0-MMIO)
Debug Port USB PIDs (Packet Identifier) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RO	0	**Received PID**
15:8	RW	0	**Send PID**
7:0	RW	0	**Token PID**

Offset Address: AF-A8h (USB 2.0-MMIO)
Debug Port Data Buffer **Default Value: FFFF FFFF FFFF FFFFh**

Bit	Attribute	Default	Description
63:0	RW	FFFF FFFF FFFF FFFFh	**Debug Port Data Buffer**

Offset Address: B3-B0h (USB 2.0-MMIO)
Debug Port Device Address **Default Value: 0000 7F01h**

Bit	Attribute	Default	Description
31:15	RO	0	**Reserved**
14:8	RW	7Fh	**USB Address**
7:4	RO	0	**Reserved**
3:0	RW	1h	**USB Endpoint**

DEVICE 17 FUNCTION 0 (D17F0): BUS CONTROL AND POWER MANAGEMENT

PCI Configuration Space

All registers are located in D17F0 Configuration Space. These registers are accessed through PCI configuration mechanism #1 via I/O address 0CF8h / 0CFCh.

The base address of UART IO space is in D17F0:

- UART1 I/O base address is located in D17F0 RxB4 while UART2 I/O base address is located in D17F0 RxB5.

Header Registers (00-3Fh)

Offset Address: 01-00h (D17F0)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D17F0)
Device ID — **Default Value: 8409h**

Bit	Attribute	Default	Description
15:0	RO	8409h	**Device ID**

Offset Address: 05-04h (D17F0)
PCI Command — **Default Value: 0003h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	**Reserved**
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	0	**PCI Master Function**
1	RW	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RW	1b	**I/O Space Access** Hardwired to 1 (Responds to I/O space access)

Offset Address: 07-06h (D17F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus Master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6:0	RO	10h	**Reserved (Do Not Program)**

Offset Address: 08h (D17F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D17F0)

Class Code **Default Value: 06 0100h**

Bit	Attribute	Default	Description
23:0	RO	060100h	**Class Code**

Offset Address: 0C-0Dh (D17F0) – Reserved

Offset Address: 0Eh (D17F0)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h means multi-function device.

Offset Address: 0Fh (D17F0)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 00h.

Offset Address: 10-2Bh (D17F0) – Reserved

Offset Address: 2D-2Ch (D17F0)

Subsystem Vendor ID — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D17F0)

Subsystem ID — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Subsystem ID**

Offset Address: 30-3Fh (D17F0) – Reserved

ISA Bus Control (40-49h)

Offset Address: 40h (D17F0)

ISA Bus Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Extra / Normal ISA Command Delay** 0: Normal 1: External
6	RW	0	**I/O Recovery Time** 0: Disable 1: Enable
5	RW	0	**Reserved**
4	RW	0	**ROM Write** 0: Disable 1: Enable
3	RW	0	**Double DMA Clock** 0: Disable 1: Enable
2	RW	0	**4D0 / 4D1 Support** 0: Disable 1: Enable
1	RW	0	**MEGA Cells (DMAC, INTC and TMRC) Shadow Register Read** 0: Disable 1: Enable
0	RW	0	**BCLK (Bus Clock) = PCLK (PCI Bus Clock) / 2** 0: Disable 1: Enable

Offset Address: 41h (D17F0)

ROM Decode Control — **Default Value: 80h**

Setting these bits to 1 enables the indicated address range to be included in the LPC BIOS ROM address decoding.

Bit	Attribute	Default	Description
7	RW	1b	**000E0000h-000EFFFFh**
6	RW	0	**FFF00000h-FFF7FFFFh** **FFB00000h-FFB7FFFFh**
5	RW	0	**FFE80000h-FFEFFFFFh** **FFA80000h-FFAFFFFFh**
4	RW	0	**FFE00000h-FFE7FFFFh** **FFA00000h-FFA7FFFFh**
3	RW	0	**FFD80000h-FFDFFFFFh** **FF980000h-FF9FFFFFh**
2	RW	0	**FFD00000h-FFD7FFFFh** **FF900000h-FF97FFFFh**
1	RW	0	**FFC80000h-FFCFFFFFh** **FF880000h-FF8FFFFFh**
0	RW	0	**FFC00000h-FFC7FFFFh** **FF800000h-FF87FFFFh**

Offset Address: 42h (D17F0)

Line Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DMA Line Buffer** 0: Disable 1: Enable. Setting this bit to 1 indicates Master DMA waits until the line buffer is full (8 DW) before transmitting data (bit-6 must also be enabled to ensure that there are no coherency issues).
6	RW	0	**Gate INTR Assertion Until Line Buffer Flush Is Complete** 0: Disable 1: Enable. INTR assertion is gated until the line buffer is flushed. This bit should be enabled if bit 7 is enabled.
5	RW	0	**IRQ Flush Line Buffer When No DMA is Granted** 0: Disable 1: Enable This bit is to enable line buffer flushing when interrupt request is received. However, the line buffer flushing is performed only when no DMA is granted.
4	RW	0	**Uninterruptible Burst Read** 0: Disable 1: Enable. The PCI bus is not granted to DMA until burst read transactions from the host are completed.
3	RW	0	**Gate Serial IRQ Inputs Until Line Buffer Flush Is Complete** 0: Disable 1: Enable
2	RW	0	**IRQ Flush Line Buffer Even When DMA Is Granted** Line buffer is flushed even if DMA is granted with bit 5 =1 0: Disable 1: Enable
1:0	RW	0	**Reserved**

Offset Address: 43h (D17F0)

Delay Transaction Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:5	RO	0	**Reserved**
4	RW	0	**Reserved**
3	RW	1b	**Delayed Transactions (PCI Spec Rev 2.1)** This bit controls whether delayed transactions (delayed read / write and posted write) are enabled. 0: Disable 1: Enable
2	RW	0	**Delayed Transaction – Posted Write Only** 0: Disable 1: Enable
1	RW	0	**Write Delay Transaction Timeout Timer** When enabled, if a delayed transaction (write cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable
0	RW	0	**Read Delay Transaction Timeout Timer** When enabled, if a delayed transaction (read cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable

Offset Address: 44h (D17F0)

PCI PnP Interrupt Routing − INTE#, INTF# **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTF# Routing** Refer to Table 20 PnP IRQ Routing Table
3:0	RW	0	**PCI INTE# Routing** Refer to Table 20 PnP IRQ Routing Table

Offset Address: 45h (D17F0)

PCI PnP Interrupt Routing − INTG#, INTH# **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTH# Routing** Refer to Table 20 PnP IRQ Routing Table
3:0	RW	0	**PCI INTG# Routing** Refer to Table 20 PnP IRQ Routing Table

Offset Address: 46h (D17F0)
PCI INT[H:E]# UART Multiplex Select Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**UART Multiplex with DVP or VCP Pad** 0: Multiplex with VCP pad when UART enabled 1: Multiplex with DVP pad when UART enabled Must set bit 6 or RxB0[0] to enable this function. If UART is disabled, neither DVP nor VCP pad is used.
6	RW	0	**UART Function Multiplex with DVP or VCP Pad** 0: Disable 1: Enable
5	RW	0	**Control the Destination of IO Port 0x80** Reference Rx5B[6]
4	RW	0	**PCI INT Sharing Control** 0: INTH# shared with INTD# INTG# shared with INTC# INTF# shared with INTB# INTE# shared with INTA# 1: INTH# routing according to Rx45[7:4] INTG# routing according to Rx45[3:0] INTF# routing according to Rx44[7:4] INTE# routing according to Rx44[3:0] If Rx55[3]=1 and external general interrupt selects INTE#, INTF#, INTG# or INTH#, this bit must be programmed to 1.
3	RW	0	**PCI INTH# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
2	RW	0	**PCI INTG# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
1	RW	0	**PCI INTF# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
0	RW	0	**PCI INTE# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert

Note: For routing control of PCI INTA# ~ INTD#, see Device 17 Function 0 Rx54-57 and PnP IRQ Routing Table (Refer to Table 20).

Offset Address: 47h (D17F0)
PATA PAD Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	00b	**IDE Pad Multiplex Select** 00: The pads multiplex is determined by strapping value (registers default value). 01: IDE pads are dedicated to IDE. Others: Reserved
1	RW	1b	**Pull Up PATA IORDY** 0: Disable 1: Enable
0	RW	1b	**Pull Down PATA DMA Request** 0: Disable 1: Enable

Offset Address: 48h (D17F0)
APIC FSB Data Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FSB Fixed at Low DW** 0: Disable. Address bit-2 (A2) is not masked/ 1: Enable. Force A2 from APIC FSB to low. Address bit A2 controls whether data is in the lower (0) or upper (1) doubleword of a quadword sent to the CPU. When this bit is enabled, A2 is masked which means it is always 0 to select the lower doubleword.
6:0	RO	0	**Reserved**

Offset Address: 49h (D17F0)
SM Peripheral Device Control — **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**SERR from Host Directed to PMU (SMI, SCI)** 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	1b	**Gated IRQ before SM Buffer Clean** Controls whether interrupt requests are gated until data is written to memory. 0: Disable 1: Enable
4	RW	0	**PCIM Address Stepping** 0: Disable 1: Enable
3	RW	0	**PCIM Wait State** 0: Disable 1: Enable
2	RW	0	**WSC Mask Off INTR** Controls whether INTR is masked until write snoop is complete. 0: Disable 1: Enable
1:0	RW	0	**Reserved**

LPC Firmware Memory Control (4A-4Bh)

Offset Address: 4Ah (D17F0)
LPC Firmware Memory Control 1 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**LPC Firmware Memory Base Address [23:17]**
0	RW	0	**LPC Firmware Memory Programmable IDSEL** 0: Disable 1: Enable When this bit is enabled, the memory cycles in the address range, specified by Rx4A-4Bh, will be transferred into LPC firmware memory cycles no matter what the setting of Rx59 is.

Offset Address: 4Bh (D17F0)
LPC Firmware Memory Control 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	000b	**LPC Firmware Memory Base Address Mask** Set bit 6 to 1 to mask A19 decoding. Set bit 5 to 1 to mask A18 decoding. Set bit 4 to 1 to mask A17 decoding.
3:0	RW	0	**LPC Firmware Memory IDSEL Value**

Miscellaneous Control (4C-4Fh)

Offset Address: 4Ch (D17F0)
IDE Interrupt Select — **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00b	**I/O Recovery Time Select** When Rx40[6] is enabled, this field determines the I/O recovery time. 00: 1 bus clock 01:2 bus clock 10: 4 bus clock 11:8 bus clock
5:4	RW	0	**Reserved**
3:2	RW	01b	**Reserved (Do Not Program)**
1:0	RW	00b	**IDE Primary Channel IRQ Routing** 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11

Offset Address: 4Dh (D17F0)

Miscellaneous Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LPC Firmware Memory 16 Bytes Burst Read** 0: Disable 1: Enable
6	RW	0	**LPC Firmware Memory 4 Bytes Burst Read / Write Access** 0: Disable 1: Enable
5	RW1	0	**Firmware Memory Burst Detection** Write 1 to start to detect the Firmware memory burst ability 0: Complete 1: Incomplete If the LPC Firmware memory supports 16-byte burst, bit 7 will be set to 1 after burst detection complete. If the LPC Firmware memory support 4-byte burst, the bit 6 will be set 1 after burst detection complete.
4	RW	0	**LPC Firmware Memory IDSEL Value** 0: IDSEL is from Rx75[7:4] 1: IDSEL is from AD28-AD31 This control bit is valid when Rx4D[1] is set to 1.
3	RW	0	**Enable Fixed Path of External Interrupt Delivery Only in APIC IRQ0 When the Interrupt Controller Has Not Been Masked Yet** 0: Disable 1: Enable
2	RW	0	**Serial IRQs Always be Shared in APIC Mode** 0: Disable 1: Enable
1	RW	0	**LPC Firmware Memory Cycle Configuration** 0: Only cycles which are targeting the specified programmable ROM space are converted into LPC firmware memory cycles (LPC ROM range and IDSEL value is determined by registers in Rx75-76h and Rx7C-7Fh) 1: All memory cycles are converted into LPC firmware memory cycles (IDSEL value is decided by bit 4) This register bit is used to select the memory ranges that are treated as LPC Firmware Memory space when Rx59[7] is set to 0.
0	RW	0	**LPC TPM Function** 0: Disable 1: Enable

Offset Address: 4Eh (D17F0)

Internal RTC Test Mode and Extra Feature Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**RTC High Bank Rx3F-38 R/W Protect** 0: Disable (allow R/W) 1: Enable (Protect)
6	RW	0	**RTC Low Bank Rx3F-38 R/W Protect** 0: Disable (allow R/W) 1: Enable (Protect)
5	RW	0	**Reserved**
4	RO	0	**RTC Last Write Status** 0: Last write was to port 70 1: Last write was to port 74
3	RW	0	**Enable RTC Port 74/75** The RTC is normally accessed though ports 70/74. This bit controls whether two extra ports (74/75) can be used to access the RTC. 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: 4Fh (D17F0)

PCI Reset Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Software PCI Reset** 0: Disable 1: Enable Write 1 to generate PCI reset. Software reset can also be initiated through I/O port CF9 as follows: Write 1 to I/O port CF9 bit-2 for software reset: if CF9 bit 1 is 0, INIT will be asserted; if CF9 bit 1 is 1 (default), PCIRST will be asserted.

Function Control (50-51h)

Offset Address: 50h (D17F0)

Function Control 1 Default Value:00h

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**USB Device Mode Enable** 0: Enable 1: Disable
5	RW	0	**Device 16 Function 1 (USB 1.1 UHCI Port 2-3)** 0: Enable 1: Disable
4	RW	0	**Device 16 Function 0 (USB 1.1 UHCI Port 0-1)** 0: Enable 1: Disable
3	RW	0	**Device 15 Function 0 (EIDE)** 0: Enable 1: Disable
2	RW	0	**Device 16 Function 2 (USB 1.1 UHCI Port 4-5)** 0: Enable 1: Disable
1	RW	0	**Device 16 Function 4 (USB 2.0 EHCI Port 0-5)** 0: Enable 1: Disable
0	RW	0	**Reserved**

Offset Address: 51h (D17F0)

Function Control 2 Default Value: 0Dh

Bit	Attribute	Default	Description
7	RW	0	**SDC (SD Controller) Disable** 0: Enable 1: Disable
6	RW	0	**Reserved**
5	RO	0	**Reserved**
4	RW	0	**SDIO Disable** 0: Enable 1: Disable
3	RW	1b	**Internal RTC** 0: Disable 1: Enable
2	RW	1b	**Internal PS2 Mouse** 0: Disable 1: Enable
1	RW	0	**Internal Keyboard Controller Configuration** 0: Disable 1: Enable
0	RW	1b	**Internal Keyboard Controller** 0: Disable 1: Enable

Serial IRQ, LPC and PC / PCI DMA Control (52-53h)

Offset Address: 52h (D17F0)

Serial IRQ, PCI / DMA Control and LPC Control Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**LPC Short Wait Abort** 0: Disable 1: Enable. In a short wait, the cycle is aborted after 8Ts.
5	RW	0	**LPC Frame Wait State** 0: Disable 1: Enable
4	RW	0	**Serial IRQ Stop to Start Frame Wait State** 0: Disable. One idle state is inserted between Stop and Start. 1: Enable. Stop is followed immediately by Start.
3	RW	0	**Serial IRQ** 0: Disable 1: Enable. (IRQ asserted via SERIRQ)
2	RW	0	**Serial IRQ Quiet Mode** 0: Continuous Mode 1: Quiet Mode
1:0	RW	00b	**Serial IRQ Start-Frame Width** 00: 4 PCI clocks 01: 6 PCI clocks 10: 8 PCI clocks 11: 10 PCI clocks

Offset Address: 53h (D17F0)

PC / PCI DMA Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PC/PCI DMA Control** 0: Disable PC/PCI DMA. (The signal balls are used for GPIO) 1: Enable PC/PCI DMA
6	RW	0	**DMA Channel 7 for PC/PCI DMA** 0: Disable 1: Enable
5	RW	0	**DMA Channel 6 for PC/PCI DMA** 0: Disable 1: Enable
4	RW	0	**DMA Channel 5 for PC/PCI DMA** 0: Disable 1: Enable
3	RW	0	**DMA Channel 3 for PC/PCI DMA** 0: Disable 1: Enable
2	RW	0	**DMA Channel 2 for PC/PCI DMA** 0: Disable 1: Enable
1	RW	0	**DMA Channel 1 for PC/PCI DMA** 0: Disable 1: Enable
0	RW	0	**DMA Channel 0 for PC/PCI DMA** 0: Disable 1: Enable

Plug and Play Control – PCI (54-57h)

Offset Address: 54h (D17F0)

PCI Bus and CPU Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved** The following bits all default to "Low Active Level " triggered (0)
4	RW	0	**Enable PCI Debug Mode** If enabled, reuse SDIO/CR/SPI Pads as PCI bus signal. 0: Disable 1: Enable
3	RW	0	**PCI INTA# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
2	RW	0	**PCI INTB# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
1	RW	0	**PCI INTC# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
0	RW	0	**PCI INTD# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert

Note: PCI INTA-D# normally connect to PCI interrupt pins INTA-D# (see signal descriptions for more information).

Offset Address: 55h (D17F0)

PCI PnP Interrupt Routing 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTA# Routing** Refer to Table 20 PnP IRQ Routing Table
3	RW	0	**Enable External General Interrupt from GPIO14** 0: Disable 1: Enable
2:0	RW	000b	**External General Interrupt Routing Selection.** 000: Routing to INTA# 001: Routing to INTB# 010: Routing to INTC# 011: Routing to INTD# 100: Routing to INTE# 101: Routing to INTF# 110: Routing to INTG# 111: Routing to INTH#

Offset Address: 56h (D17F0)
PCI PnP Interrupt Routing 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTC# Routing** Refer to Table 20 PnP IRQ Routing Table
3:0	RW	0	**PCI INTB# Routing** Refer to Table 20 PnP IRQ Routing Table

Offset Address: 57h (D17F0)
PCI PnP Interrupt Routing 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTD# Routing** Refer to Table 20 PnP IRQ Routing Table
3:0	RO	0	**Reserved** Always reads 0.

Table 20. PnP IRQ Routing Table

INTA#~INTH# Routing Register	PIC Mode
0000	Reserved
0001	IRQ1
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

APIC Mode	INTA~INTH
PIRQ16	INTA
PIRQ17	INTB
PIRQ18	INTC
PIRQ19	INTD
PIRQ20	INTE
PIRQ21	INTF
PIRQ22	INTG
PIRQ23	INTH

When enable internal APIC, PCI devices and internal function, IRQ routing are shown as below:

Table 21. Internal APIC, PCI Devices IRQ Routing Table

HPET IRQ	IRQ16
HPET IRQ	IRQ17
HPET IRQ	IRQ18
HPET IRQ	IRQ19
UHCI Port 0-1 IRQ and Card Boot IRQ	IRQ20
EIDE IRQ and UHCI Port 4-5 IRQ	IRQ21
UHCI Port 2-3 IRQ and SDIO IRQ	IRQ22
Card Reader IRQ and EHCI Port 0-5	IRQ23

Table 22. HPET IRQ Routing Table

Mode	Timer 0	Timer 1	Timer 2
Legacy Mode	IRQ0(PIC) / IRQ2(APIC)	IRQ8(PIC) / IRQ8(APIC)	Not Support(PIC) / IRQ11, IRQ16-19 for APIC only
Non-legacy Mode	IRQ16-19 for APIC only	IRQ16-19 for APIC only	IRQ11, IRQ16-19 for APIC only

GPIO and Miscellaneous Control (58-5Bh)

Offset Address: 58h (D17F0)

South Module Miscellaneous Control 1 **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Internal APIC** 0: Disable 1: Enable
5	RW	1b	**South Module Interrupt Cycles Sync. with 33 MHz Clock** 0: Disable (8 MHz) 1: Enable
4	RW	0	**South Module PCI Cycle Decode** 0: Subtractive 1: Positive
3	RW	0	**RTC High Bank Access** 0: Disable 1: Enable
2	RW	0	**RTC Rx32 Write Protect** 0: Disable (not protected) 1: Enable (write protected)
1	RW	0	**RTC Rx0D Write Protect** 0: Disable (not protected) 1: Enable (write protected)
0	RW	0	**RTC Rx32 Map to Century Byte** Controls whether RTC Rx32 is mapped to the century byte. 0: Disable 1: Enable

Offset Address: 59h (D17F0)

South Module Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LPC/SPI Memory Space** 0: All memory cycles are forwarded to LPC/SPI 1: Memory cycles with address in the ranges specified by the ROM Memory Address Range registers are forwarded to LPC/SPI.
6	RW	0	**Reserved**
5	RW	0	**LPC RTC** 0: Disable 1: Enable
4	RW	0	**LPC Keyboard** 0: Disable (ISA Keyboard) 1: Enable (LPC Keyboard)
3	RW	0	**Port 62h / 66h (MCCS#) to LPC** 0: Disable 1: Enable
2	RW	0	**Port 62h / 66h (MCCS#) Decode** 0: Disable 1: Enable
1	RW	0	**Mask A20M# Active** 0: Disable (A20M# acts normally) 1: Enable (A20M# signal de-asserted)
0	RW	0	**NMI on PCI Parity Error** 0: Disable 1: Enable (to generate NMI, Port 61[3] and Port 70[7] must also be set)

Note: To trigger NMI assertion correctly, both IO port 61 bit3 and IO port70 bit7 must be set to 0 since data parity error report is combined with IOCHK.

Offset Address: 5Ah (D17F0)

DMA Bandwidth Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DMA Channel 7 Bandwidth** 0: Normal 1: Improved
6	RW	0	**DMA Channel 6 Bandwidth** 0: Normal 1: Improved
5	RW	0	**DMA Channel 5 Bandwidth** 0: Normal 1: Improved
4	RW	0	**DMA Single Transfer Mode Bandwidth** 0: Normal 1: Improved
3	RW	0	**DMA Channel 3 Bandwidth** 0: Normal 1: Improved
2	RW	0	**DMA Channel 2 Bandwidth** 0: Normal 1: Improved
1	RW	0	**DMA Channel 1 Bandwidth** 0: Normal 1: Improved
0	RW	0	**DMA Channel 0 Bandwidth** 0: Normal 1: Improved

Note: The above bits determine if DMA bandwidth is improved for the specified channel. If enabled, bandwidth improvement is accomplished by reducing the transaction latency between the DMA Controller and the LPC Bus Controller.

Offset Address: 5Bh (D17F0)
Miscellaneous Control **Default Value: 41h**

Bit	Attribute	Default	Description
7	RW	0	**LPC Firmware Memory Read TRDY 1 Wait State** 0: Disable 1: Enable
6	RW	1b	**Control the Destination of IO Port 0x80** Work with Rx46[5] Rx5B[6], Rx46[5] 0X: IO Port 0x80 goes to ISA bus. 10: IO Port 0x80 goes to LPC bus. 11: IO Port 0x80 goes to SPI bus.
5	RW	0	**PCI/DMA Memory Cycles Output to PCI Bus** 0: Disable 1: Enable
4	RW	0	**APIC Clock Gating Enable** 0: Disable 1: Enable
3	RW	0	**Bypass APIC De-Assert Message** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	1b	**Dynamic Clock Stop** 0: Disable 1: Enable

Programmable Chip Select (PCS) Control (5C-66h)

Offset Address: 5D-5Ch (D17F0)
PCS 0 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 0 I/O Port Address**

Offset Address: 5F-5Eh (D17F0)
PCS 1 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 1 I/O Port Address**

Offset Address: 61-60h (D17F0)
PCS 2 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 2 I/O Port Address**

Offset Address: 63-62h (D17F0)
PCS 3 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 3 I/O Port Address**

Offset Address: 65-64h (D17F0)

PCS I/O Port Address Mask — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0000b	**PCS 3 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
11:8	RW	0000b	**PCS 2 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
7:4	RW	0000b	**PCS 1 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
3:0	RW	0000b	**PCS 0 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.

Offset Address: 66h (D17F0)

PCS Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**PCS 3** 0: Disable 1: Enable
2	RW	0	**PCS 2** 0: Disable 1: Enable
1	RW	0	**PCS 1** 0: Disable 1: Enable
0	RW	0	**PCS 0** 0: Disable 1: Enable

Offset Address: 67h (D17F0)

Output and PCS Control — **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**PCS 3 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
6	RW	0	**PCS 2 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
5	RW	0	**PCS 1 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
4	RW	0	**PCS 0 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
3	RW1C	0	**SPI External Interrupt Status** 0: Interrupt pending 1: No interrupt
2	RW	1b	**FERR# Voltage** 0: 2.5V 1: 1.5V
1:0	RW	00b	**IDE Pad Driving Select** 00: 12 mA 01: 13.3 mA 10: 14 mA 11: 15.2 mA

Note: PCS IO cycle can be claimed in two ways:
Positive decoding: Set Rx58[4] and the corresponding bits in Rx6C[1:0] and Rx6F[5] to 1, and program the PCS address range.
Subtractive decoding: Program the PCS address range.

High Precision Event Timers (HPET) (68-6Bh)

Offset Address: 68h (D17F0)

HPET Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Precision Event Timers** 0: Disable 1: Enable
6:4	RW	0	**Reserved**
3	RW	0	**PCS 3 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
2	RW	0	**PCS 2 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
1	RW	0	**PCS 1 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
0	RW	0	**PCS 0 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable

Offset Address: 6B-69h (D17F0)

HPET Address — **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:2	RW	0	**HPET Memory Base Address [31:10]**
1:0	RW	0	**Reserved**

ISA Decoding Control (6C-73h)

Offset Address: 6Ch (D17F0)

ISA Positive Decoding Control 1 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**On-Board I/O (Ports 00-FFh) Positive Decoding** 0: Disable 1: Enable
6	RW	0	**Microsoft Sound System I/O Port Positive Decoding** 0: Disable 1: Enable (bits [5:4] determine the decode range)
5:4	RW	00b	**Microsoft Sound System I/O Decode Range** 00: 0530h-0537h 01: 0604h-060Bh 10: 0E80h-0E87h 11: 0F40h-0F47h
3	RW	0	**APIC Positive Decoding** 0: Disable 1: Enable
2	RW	0	**ROM Positive Decoding** 0: Disable 1: Enable
1	RW	0	**PCS1# Positive Decoding** 0: Disable 1: Enable
0	RW	0	**PCS0# Positive Decoding** 0: Disable 1: Enable

Offset Address: 6Dh (D17F0)

ISA Positive Decoding Control 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FDC Positive Decoding** 0: Disable 1: Enable
6	RW	0	**LPT Positive Decoding** 0: Disable 1: Enable
5:4	RW	00b	**LPT Decode Range** 00: 3BCh-3BFh, 7BCh-7BEh 01: 378h-37Fh, 778h-77Ah 10: 278h-27Fh, 678h-67Ah 11: Reserved
3	RW	0	**Game Port Positive Decoding** 0: Disable 1: Enable
2	RW	0	**MIDI Positive Decoding** 0: Disable 1: Enable
1:0	RW	00b	**MIDI Decode Range** 00: 300h-303h 01: 310h-313h 10: 320h-323h 11: 330h-333h

Offset Address: 6Eh (D17F0)

ISA Positive Decoding Control 3 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**COM Port B Positive Decoding** 0: Disable 1: Enable
6:4	RW	000b	**COM Port B Decode Range** 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3EFh (COM3)
3	RW	0	**COM Port A Positive Decoding** 0: Disable 1: Enable
2:0	RW	000b	**COM Port A Decode Range** 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3Efh (COM3)

Offset Address: 6Fh (D17F0)

ISA Positive Decoding Control 4 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SPI Positive Decoding** 0: Disable 1: Enable
6	RW	0	**LPC TPM Positive Decoding** 0: Disable 1: Enable
5	RW	0	**PCS2# and PCS3# Positive Decoding** 0: Disable 1: Enable
4	RW	0	**I/O Port 0CF9h Positive Decoding** 0: Disable 1: Enable
3	RW	0	**Floppy Disk Controller (FDC) Decoding Range** 0: Primary 1: Secondary
2	RW	0	**Sound Blaster Positive Decoding** 0: Disable 1: Enable
1:0	RW	00b	**Sound Blaster Decode Range** 00: 220-22F, 230-233h 01: 240-24F, 250-253h 10: 260-26F, 270-273h, 11: 280-28F, 290-293h

Offset Address: 71-70h (D17F0)

Subsystem Vendor ID Backdoor Registers — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Subsystem Vendor ID (Rx2D-2C) Back Door**

Offset Address: 73-72h (D17F0)
Subsystem ID Backdoor Registers — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Subsystem Vendor ID (Rx2F-2E) Back Door**

PCI I/O Cycle Control (74-7Fh)

Offset Address: 74h (D17F0) – Reserved

Offset Address: 75h (D17F0)
LPC ROM Memory Address Range — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Firmware Memory IDSEL for All Memory Range** Used when Rx4D[1] is 1 and Rx4D[4] is 0.
3	RW	0	**Select LPC ROM Memory Address Range 1 {FF700000h-FF7FFFFFh, FF300000h-FF3FFFFFh}** 0: Not select 1: Select
2	RW	0	**Select LPC ROM Memory Address Range 2 {FF600000h-FF6FFFFFh, FF200000h-FF2FFFFFh}** 0: Not select 1: Select
1	RW	0	**Select LPC ROM Memory Address Range 3 {FF500000h-FF5FFFFFh, FF100000h-FF1FFFFFh}** 0: Not select 1: Select
0	RW	0	**Select LPC ROM Memory Address Range 4 {FF400000h-FF4FFFFFh, FF000000h-FF0FFFFFh}** 0: Not select 1: Select

Offset Address: 76h (D17F0)
Firmware Memory IDSEL 1 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF500000h-FF5FFFFFh, FF100000h-FF1FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF400000h-FF4FFFFFh, FF000000h-FF0FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 77h (D17F0)
Firmware Memory IDSEL 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF700000h-FF7FFFFFh, FF300000h-FF3FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF600000h-FF6FFFFFh, FF200000h-FF2FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 78-7Bh (D17F0) – Reserved

Offset Address: 7Ch (D17F0)

Firmware Memory IDSEL 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFC80000h-FFCFFFFFh, FF880000h-FF8FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFC00000h-FFC7FFFFh, FF800000h-FF87FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Dh (D17F0)

Firmware Memory IDSEL 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFD80000h-FFDFFFFFh, FF980000h-FF9FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFD00000h-FFD7FFFFh, FF900000h-FF97FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Eh (D17F0)

Firmware Memory IDSEL 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFE80000h-FFEFFFFFh, FFA80000h-FFAFFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFE00000h-FFE7FFFFh, FFA00000h-FFA7FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Fh (D17F0)

Firmware Memory IDSEL 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges { FFB80000h-FFBFFFFFh, 000E0000h-000FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFF00000h-FFF7FFFFh, FFB00000h-FFB7FFFFh }** 0000: IDSEL0 … 1111: IDSEL15

Power Management-Specific Configuration Registers (80-AFh)

Offset Address: 80h (D17F0)

PM General Configuration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Enable GPIO12 as SLPBTN#** 0: Disable 1: Enable
5	RW	0	**Power Button De-bounce** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	0	**Enable Microsoft Sound Monitor in Audio Access** This access means an I/O cycle to the sound port as specified in D17F0 Rx6C[5:4]. 0: Disable 1: Enable
2	RW	0	**Enable Game Port Monitor in Audio Access** This access means an I/O cycle to the game port: 200h-207h. 0: Disable 1: Enable
1	RW	0	**Enable Sound Blaster Monitor in Audio Access** This access means an I/O cycle to the sound blaster port as specified in D17F0 Rx6F[1:0] or 388h-38Bh. 0: Disable 1: Enable
0	RW	0	**Enable MIDI Monitor in Audio Access** This access means an I/O cycle to the midi port as specified in D17F0 Rx6D[1:0]. 0: Disable 1: Enable

Offset Address: 81h (D17F0)

PM General Configuration 2 **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**Enable ACPI I/O** 0: Disable access to ACPI I/O block 1: Allow access to Power Management I/O register block (see Rx89-88h to set the base address for this register block). Please refer to section “Power Management I/O Space” for register descriptions.
6:4	RW	0	**Reserved** Always reads 0.
3	RW	0	**ACPI Timer with 32-Bit Width Control** 0: ACPI timer counts with 24-bit width. 1: ACPI timer counts with 32-bit width.
2	RW	1b	**Enable RTC Control Signal Gated with PSON (SUSC#) in Soft-Off Mode** 0: Disable 1: Enable This is to prevent CMOS and Power-Well register data from being corrupted during system on/off when the RTC control signal (PWRGD) may not be stable.
1	RW	0	**Throttle Timer Base Clock Period (for STPCLK#)** This bit controls the timer tick base for the throttle timer. 0: 30 usec (480 usec cycle time when using a 4-bit timer) 1: 1 msec (16 msec cycle time when using a 4-bit timer) The timer tick base can be further lowered to 7.5 usec (120 usec cycle time when using a 4-bit timer) by setting Rx8D[4] = 1. When Rx8D[4] = 1, the setting of this bit is ignored.
0	RW	0	**Reserved**

Offset Address: 82h (D17F0)
ACPI Interrupt Select **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**ATX / AT Power Indicator** 0: ATX 1: AT
6	RO	1b	**PSON (SUSC#) Current State** 0: PSON Gating Active 1: PSON Gating Complete During system on/off, this status bit reports whether PSON gating state has been completed. 0 means that gating is active now; 1 means that gating is complete. Software should not access any CMOS or Power-Well registers until this bit becomes 1 if Rx81[2] = 1.
5	RW	0	**Reserved** Always reads 0.
4	RO	0	**SUSC# AC-Power-On Default** This bit reflects the value of RTC Index 0D bit 7. If 0, the system is configured to "default on" when power is connected.
3:0	RW	0000b	**ACPI IRQ Select** This field determines the routing of the ACPI IRQ. 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: IRQ15

Offset Address: 83h (D17F0)
Internal Timer Read Test **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Internal Timer Read Test**

Offset Address: 85-84h (D17F0)

IRQn as Primary Interrupt **Default Value: 0000h**

If an IRQ is enabled as a Primary IRQ, its assertion can be used as a wakeup event in system power management. This register is used in conjunction with:

- PMIO Rx28[7] – Primary Resume Status
- PMIO Rx2A[7] – Primary Resume Enable

If a device's IRQ is enabled as a Primary Interrupt, once the device asserts the IRQ, the PMIO Rx28[7] status bit will be set to 1 to report the occurrence of the Primary IRQ. If PMIO Rx2A[7] is set to 1 to enable the Resume-on-Primary-IRQ function, the IRQ becomes a wakeup event.

Bit	Attribute	Default	Description
15	RW	0	**IRQ15 as Primary Interrupt Channel** 0: Disable 1: Enable
14	RW	0	**IRQ14 as Primary Interrupt Channel** 0: Disable 1: Enable
13	RW	0	**IRQ13 as Primary Interrupt Channel** 0: Disable 1: Enable
12	RW	0	**IRQ12 as Primary Interrupt Channel** 0: Disable 1: Enable
11	RW	0	**IRQ11 as Primary Interrupt Channel** 0: Disable 1: Enable
10	RW	0	**IRQ10 as Primary Interrupt Channel** 0: Disable 1: Enable
9	RW	0	**IRQ9 as Primary Interrupt Channel** 0: Disable 1: Enable
8	RW	0	**IRQ8 as Primary Interrupt Channel** 0: Disable 1: Enable
7	RW	0	**IRQ7 as Primary Interrupt Channel** 0: Disable 1: Enable
6	RW	0	**IRQ6 as Primary Interrupt Channel** 0: Disable 1: Enable
5	RW	0	**IRQ5 as Primary Interrupt Channel** 0: Disable 1: Enable
4	RW	0	**IRQ4 as Primary Interrupt Channel** 0: Disable 1: Enable
3	RW	0	**IRQ3 as Primary Interrupt Channel** 0: Disable 1: Enable
2	RW	0	**Reserved** Always reads 0.
1	RW	0	**IRQ1 as Primary Interrupt Channel** 0: Disable 1: Enable
0	RW	0	**IRQ0 as Primary Interrupt Channel** 0: Disable 1: Enable

Offset Address: 87-86h (D17F0)

IRQn as Secondary Interrupt **Default Value: 0000h**

This register is used in conjunction with:

- PMIO Rx28[1] – Secondary Event Timer Timeout Status
- PMIO Rx2A[1] – SMI on Secondary Event Timer Timeout

Secondary IRQ is different from Primary IRQ in systems that resume due to a Secondary IRQ event can return to the suspend state after the secondary event timer times out. For this to work, PMIO Rx2A[1] needs to be set to one to enable SMI-on-Secondary-Event-Timer-Timeout (when PMIO Rx28[1] = 1). The timer's count value can be set via Rx90[27:26].

Bit	Attribute	Default	Description
15	RW	0	**IRQ15 as Secondary Interrupt Channel** 0: Disable 1:Enable
14	RW	0	**IRQ14 as Secondary Interrupt Channel** 0: Disable 1:Enable
13	RW	0	**IRQ13 as Secondary Interrupt Channel** 0: Disable 1:Enable
12	RW	0	**IRQ12 as Secondary Interrupt Channel** 0: Disable 1:Enable
11	RW	0	**IRQ11 as Secondary Interrupt Channel** 0: Disable 1:Enable
10	RW	0	**IRQ10 as Secondary Interrupt Channel** 0: Disable 1:Enable
9	RW	0	**IRQ9 as Secondary Interrupt Channel** 0: Disable 1:Enable
8	RW	0	**IRQ8 as Secondary Interrupt Channel** 0: Disable 1:Enable
7	RW	0	**IRQ7 as Secondary Interrupt Channel** 0: Disable 1:Enable
6	RW	0	**IRQ6 as Secondary Interrupt Channel** 0: Disable 1:Enable
5	RW	0	**IRQ5 as Secondary Interrupt Channel** 0: Disable 1:Enable
4	RW	0	**IRQ4 as Secondary Interrupt Channel** 0: Disable 1:Enable
3	RW	0	**IRQ3 as Secondary Interrupt Channel** 0: Disable 1:Enable
2	RW	0	**Reserved.** Always reads 0
1	RW	0	**IRQ1 as Secondary Interrupt Channel** 0: Disable 1:Enable
0	RW	0	**IRQ0 as Secondary Interrupt Channel** 0: Disable 1:Enable

Offset Address: 89-88h (D17F0)

Power Management I/O Base **Default Value: 0001h**

Bit	Attribute	Default	Description
15:7	RW	0	**ACPI IO Base [15:7]**
6:0	RO	01h	**Hardwired to 01h**

Offset Address: 8Ah (D17F0)

Auto-Switching Processor Power State **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Slow C4 Recovery Mode in Short C4 Setting** 0: Normal entry and recovery latencies 1: Slow recovery latencies When enabled with short C4 setting fast, slow recovery latencies of C3/C4 state are performed. In detail, please refer to C3/C4 latency configuration tables.
6:5	RW	0	**Reserved**
4	RW	0	**C2 to C3 / C4 Auto Mode** 0: Not automatically switch from C2 to C3 or C4 state 1: In C2 state, if no bus master activity after a period of time, it will return to C3 or C4 state. This bit is used in conjunction with bit 3. If bit 3 is 0, this bit must be 0.
3	RW	0	**C3/C4 to C2 Auto Mode** 0: When bus master request is treated as a break event, the processor power state will switch from C3/C4 to C0. 1: When bus master request asserted, the processor power state will switch from C3/C4 to C2 and automatically enable the bus arbiter, so that snooping and memory access could be processed correctly.
2	RW	0	**Bus Master Status Report Disable** 0: PMIO Rx00[4] is set when there is bus master activity. 1: PMIO Rx00[4] is not set by bus master activity. Must set this bit when bit 3 is set. PMIO Rx00[4] will be set by LPC DMA or LPC masters even if this bit is set.
1	RW	0	**C4 to C3 Auto Mode** 0: Disable 1: Enable ***If disabled:*** When entering C4 state, even if bus master request occurs before VRDSLP assertion, the processor will enter C4 state. ***If enabled:*** When entering C4 state, if bus master request occurs before VRDSLP assertion, the C4 state transition will be aborted and the processor will stay in C3 state.
0	RW	0	**Bus Master Request Delay C3/C4 Mode** 0: Disable 1: Enable ***If disabled:*** When entering C3/C4 state, if bus master request occurs before SLP# assertion, the processor will enter C3/C4 without waiting. ***If enabled:*** When entering C3/C4 state, if bus master request occurs before SLP# assertion, the processor will stay in C2 state and then enter C3/C4 state when bus master request is finished.

Offset Address: 8Bh (D17F0) – Reserved

Offset Address: 8Ch (D17F0)

Host Power Management Control **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Thermal Duty Cycle** This field determines STPCLK# duty cycle when the THRM# signal is asserted. The duty cycle of STPCLK#, if not activated by the assertion of THRM#, is controlled by PMIO Rx10[3:0]. The duty cycle indicates the percentage of host bus activation (the lower the percentage, the lower the performance and the higher the power savings). If the Throttling Timer Width (Rx8D[6:5]) is set to 3-bit width, bit 0 of this field should be set to 0 (and the performance increment is in unit of 12.5%). If the Throttling Timer Width is set to 2-bit width, bits [1:0] of this field should be set to 0 (and the performance increment is in unit of 25%). **Throttling Timer Width**
3	RW	0	**THRM# Enable** 0: Disable 1: Enable
2	RW	1b	**Processor Break Events** 0: Disable 1: Enable Allows processor break events, such as FERR#, to wake up processor from C1/C2/C3/C4 to C0.
1	RW	1b	**Disable Bus Arbiter C3/C4 Auto Gating** 0: Bus arbiter is auto-disabled when processor state is switched to C3/C4 state. 1: Disable the bus arbiter auto-disabled mode. The arbiter is disabled through IO Port 22h.
0	RW	1b	**Reserved (Do Not Program)**

Throttling Timer Width (Bit 7:4):

	4-Bit	3-Bit	2-Bit
0000	-	-	-
0001	6.25%	-	-
0010	12.50%	12.50%	-
0011	18.75%	-	-
0100	25.00%	25.00%	25.00%
0101	31.25%	-	-
0110	37.50%	37.50%	-
0111	43.75%	-	-
1000	50.00%	50.00%	50.00%
1001	56.25%	-	-
1010	62.50%	62.50%	-
1011	68.75%	-	-
1100	75.00%	75.00%	75.00%
1101	81.25%	-	-
1110	87.50%	87.50%	-
1111	93.75%	-	-

Offset Address: 8Dh (D17F0)

Throttle / Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Throttle Timer Reset** Write 1 to reset the throttle timer.
6:5	RW	00b	**Throttle Timer Counter Width** 0x: 4-Bit 10: 3-Bit 11: 2-Bit (See also Rx8C[7:4] and PMIO Rx10[3:0].) This field determines the counter width of the throttle timer, which in conjunction with the throttle timer tick determines the cycle time of STPCLK#. For example, if a 2-bit timer and a 7.5 usec timer tick are selected, the STPCLK# cycle time would be 30 usec (2**2 x 7.5). If a 4-bit timer and a 7.5 usec timer tick is selected, the cycle time would be 120 usec (2**4 x 7.5).
4	RW	0	**Use Fast Clock (7.5us) as Throttle Timer Tick** 0: Timer tick is selected by Rx81[1]. 1: Timer tick is 7.5usec (setting of Rx81[1] is ignored).
3	RW	0	**SMI# Low Level Output** 0: Disable 1: Enable; during an SMI event, SMI# is held low until SMI event status is cleared
2	RW	0	**Internal Clock Stops for PCI Idle** This bit controls whether the internal PCI clock stops when CLKRUN# is high. 0: PCI clock does not stop 1: PCI clock stops
1	RW	0	**Internal Clock Stops During C3/C4** This bit controls whether the internal PCI clock stops during C3/C4 state. 0: PCI clock does not stop 1: PCI clock stops
0	RW	0	**Internal Clock Stops During Suspend** This bit controls whether the internal PCI clock stops during suspend state. 0: PCI clock does not stop 1: PCI clock stops

Offset Address: 8E-8Fh (D17F0) – Reserved

Offset Address: 93-90h (D17F0)
Power Management Timer Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	00b	**Power Conserve Mode Timer Period** 00: 1/16 second 01: 1/8 second 10: 1 second 11: 1 minute
29	RW1C	0	**Power Conserve Mode Status** This bit reads 1 when in Conserve Mode
28	RW	0	**Power Conserve Mode** This bit controls whether conserve mode (through throttling) is enabled. 0: Disable 1: Enable When this bit is set, the system can enter conserve mode when primary activity is not detected within a given time period (determined by bits [31:30]). Primary activity is defined in PMIO Rx33-30.
27:26	RW	00b	**Secondary Event Timer Count Value** 00: 2 milliseconds 01: 64 milliseconds 10: ½ second 11: by EOI + 0.25 milliseconds
25	RW1C	0	**Secondary Event Occurred Status** This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.
24	RW	0	**Secondary Event Timer Enable** 0: Disable 1: Enable
23:16	RW	0	**GP1 Timer Count Value** (base defined by bits [5:4]) Write to load count value; read to get current count.
15:8	RW	0	**GP0 Timer Count Value** (base defined by bits [1:0]) Write to load count value; read to get current count.
7	RW	0	**GP1 Timer Enable** 0: Disable 1: Enable When this bit is set, the GP1 timer loads the value defined in bits [23:16] and starts counting down. The GP1 timer will be reloaded at the occurrence of peripheral events that are enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit PMIO Rx28[3] is set to one. Additionally, if the GP1 Timer Timeout Enable bit PMIO Rx2A[3] is set, an SMI is generated.
6	RW	0	**GP1 Timer Automatic Reload** 0: GP1 timer stops at 0. 1: Reload GP1 timer automatically after counting down to 0.
5:4	RW	00b	**GP1 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute
3	RW	0	**GP0 Timer Start** 0: Disable 1: Enable When this bit is set, the GP0 timer loads the value defined by bits [15:8] and starts counting down. The GP0 timer is reloaded at the occurrence of peripheral events that are enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit PMIO Rx28[2] is set to one. Additionally, if the GP0 Timer Timeout Enable bit PMIO Rx2A[2] is set, an SMI is generated.
2	RW	0	**GP0 Timer Automatic Reload** 0: GP0 Timer stops at 0 1: Reload GP0 timer automatically after counting down to 0.
1:0	RW	00b	**GP0 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute

Offset Address: 94h (D17F0)
Miscellaneous Configuration 1 (Power Well) **Default Value: 88h**

Bit	Attribute	Default	Description
7	RW	1b	**SMBus Clock Select** 0: From divider of 14.318 Mhz 1: From RTC clock If set, SMBus always uses RTC clock. If not set, SMBus uses RTC clock in suspend mode and uses 128K when RxD2[2] is set.
6	RW	0	**Check Power Button Enable When PWRBTN# Asserted to Resume from STR / STD** 0: Not check 1: Check Power Button Enable is controlled through register ACPI I/O Space Rx03[0].
5	RW	0	**Reset North Module PLL During S1 State** 0: Disable 1: Enable Setting this bit to 0 will let North Module PLL stop during S1.
4	RW	0	**KBC D2 Command Interrupt Gating** 0: Disable 1: Enable
3	RW	1b	**Pull up Pad of Card Reader / SDIO Power Switch** 0: Disable 1: Enable
2	RW	0	**Multi-Function Signal Select: GPO[9:8] vs. SUS[C:B]#** 0: SUS[C:B]# 1: GPO[9:8]
1:0	RW	00b	**GPO7 Output Select** This field controls the GPO7 output signal for Pulse Width Modulation. 00: Fixed output port (output value is defined by PMIO Rx4C[7]). 01: GPO7 output is 1 Hz slow clock rate. 10: GPO7 output is 4 Hz slow clock rate. 11: GPO7 output is 16 Hz slow clock rate.

Offset Address: 95h (D17F0)
Miscellaneous Configuration 2 (Power Well) **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**SUS[A:C]# to CPUSTP# and CPUSTP# to NM PLL Resume Delay Select** This bit controls the following two minimum delays of the resume process: De-assertion of SUS[A:C]# to the de-assertion of CPUSTP#. De-assertion of CPUSTP# to NM PLL start. 0: (A) 16 msec, (B) 1 msec 1: (A) 1 msec, (B) 125 usec
6	RW	1b	**Start NM PLL Before PWRGD when Resume from STD** 0: Disable 1: Enable
5	RW	0	**Keyboard / Mouse Port Swap** This bit determines whether the keyboard and mouse ports can be swapped. 0: Disable 1: Enable
4	RW	0	**PWRGD Reset**
3	RW	0	**Multi-Function Signal Select: SMBDT2, SMBCK2 vs. GPIO0, GPIO1** 0: SMBDT2, SMBCK2 1: GPIO0, GPIO1
2	RW	0	**AOL 2 SMB Slave (through SMB Port 2)** This bit controls whether external SMB masters can access internal SMB registers (for Alert-On-LAN). 0: Enable 1: Disable
1	RW	0	**Multi-Function Signal Select: GPO7 vs. SUSA#** 0: SUSA# 1: GPO7
0	RW	0	**USB Wakeup for POS / STR / STD** This bit controls whether USB device wakeup is enabled when PMIO Rx20[14]=1. It allows system wakeup from POS / STR / STD state when OS (or BIOS) turns on USB device remote wakeup feature and the system software enables USB wakeup register (PMIO Rx22[14]=1) also. 0: Disable 1: Enable

Offset Address: 96h (D17F0)
Miscellaneous Configuration 3 (Battery Well) **Default Value: 0Fh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0.
5	RW	0	**Reserved**
4	RW	0	**Enable SMB GPOUT6 and GPOUT7 as PWRGD and PWRBTN#** 0: Disable 1: Enable Enable ASF function. Used by Alert-on-LAN to reset the system.
3:0	RW	Fh	**CPU Frequency Strapping Value** Output through NMI, INTR, IGNNE#, and A20M# during RESET#. The value written to this field is reflected through NMI, INTR, IGNNE#, and A20M# during RESET# to determine the multiplier of the CPU's internal frequency. If the CPU hangs due to inappropriate settings written here, the GP3 timer (second timeout) can be used to initiate a system reboot (PMIO Rx42[2] set to 1). Refer to the BIOS Porting Guide for additional details.

Offset Address: 97h (D17F0)
Miscellaneous Configuration 3 (Power Well) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Wait for PWRGD Low Before Wake-up during S3/S4 State** 0: Not wait 1: Wait
6	RW	0	**Multi-Function Signal Select: MSDT, MSCK vs. GPIO2, GPIO3** 0: MSDT, MSCK 1: GPIO2, GPIO3 Note: MSCK is not supported as a GPIO I/O pad when the keyboard interrupt is sent through SERIRQ pin.
5	RW	0	**Multi-Function Signal Select: GPI2 vs. SDIO0PWOFF and GPI3 vs. SDIO0PWSEL** 0: SDIO0PWOFF / SDIO0PWSEL 1: GPI2 / GPI3
4:3	RO	00b	**Reserved**
2	RW	0	**Disable SMBALT and PWRBTN Pull-up** 0: Enable 1: Disable (not pull up)
1	RW	0	**Multi-Function Signal Select: GPI12 vs. SDIO1PWSEL and GPI13 vs. SDIO1PWOFF** 0: SDIO1PWSEL / SDIO1PWOFF 1: GPI12 / GPI13
0	RW	0	**Multi-Function Signal Select: KBDT / KBC_CPURST#, KBCK / A20GATE vs. GPIO4, GPIO5** 0: KBDT / KBC_CPURST#, KBCK / A20GATE 1: GPIO4, GPIO5

Offset Address: 98h (D17F0)
GP2 / GP3 Timer Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**GP3 Timer Start** 0: Disable 1: Enable When this bit is set, the GP3 timer loads the value specified by Rx9A and starts counting down. The GP3 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP3 timer counts down to zero, then the GP3 Timer Timeout Status bit PMIO Rx28[13] is set to one, a SMI will be asserted if the GP3 Timer Timeout Enable bit PMIO Rx2A[13] is set.
6	RW	0	**GP3 Timer Automatic Reload** 0: GP3 timer stops at 0. 1: Reload GP3 timer automatically after counting down to 0.
5:4	RW	01b	**GP3 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute
3	RW	0	**GP2 Timer Start** 0: Disable 1: Enable When this bit is set, the GP2 timer loads the value specified by Rx99 and starts counting down. The GP2 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx 38). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit PMIO Rx28[12] is set to one, a SMI will be asserted if the GP2 Timer Timeout Enable bit PMIO Rx2A[12] is set.
2	RW	0	**GP2 Timer Automatic Reload** 0: GP2 timer stops at 0. 1: Reload GP2 timer automatically after counting down to 0.

1:0	RW	00b	**GP2 Timer Tick Select** 00: Disable 01: 1 ms 10: 1 second 11: 1 minute

Offset Address: 99h (D17F0)

GP2 Timer Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI2 Timer Counter** Write will set GP2 Timer Load Value. Read will get GP2 Timer Current Count.

Offset Address: 9Ah (D17F0)

GP3 Timer Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI3 Timer Counter** Write will set GP3 Timer Load Value. Read will get GP3 Timer Current Count.

Offset Address: 9Bh (D17F0)

Boot Option Bit Mask (ASF) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Lock Sleep Button** To lock sleep button means SLPBTN# is always de-asserted. 0: Disable 1: Enable
5	RW	0	**Lock Keyboard Controller Access** 0: Enable 1: Disable
4	RW	0	**PAD TP6 Function Select** 0: Output suspend power internal 32K clock 1: Input for bypass RTC function
3	RW	0	**USB Device Mode Wakeup for POS / STR / STD / Soft Off** This bit controls whether USB device mode wakeup is enabled. This allows wakeup from STR, STD, Soft Off and POS. 0: Disable 1: Enable
2	RW	0	**Lock Reset Button** To lock reset button means Reset button is always de-asserted. 0: Disable 1: Enable
1	RW	0	**Lock Power Button** To lock reset button means PWRBTN# button is always de-asserted. 0: Disable 1: Enable
0	RW	0	**Multi-Function Signal Select: CR_PWSEL vs. GPO11, CR_PWOFF vs.GPO12** 0: CR_PWSEL, CR_PWOFF 1: GPO11, GPO12

Offset Address: 9Ch (D17F0)

ASF Byte Write Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Command Decode Table** 00h: Reserved 01h: Generate ASF wakeup event and SCI or SMI event. PMIO Rx3A[0]: SCI enable, PMIO Rx3B[0]: SMI enable. 02h: Unconditional Power Down 03h: System Reset 04h: Power Cycle Reset 05h: Reserved 06h: Watch Dog Timer Reload 07h: Reserved

Offset Address: 9Dh (D17F0)

ASF Data Message1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**ASF Data Message 1**

Offset Address: 9Eh (D17F0)

ASF Data Message 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**ASF Data Message 2**

Offset Address: 9Fh (D17F0)

CR / SDIO Voltage Change Function **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**KB/MS PAD Pull-up Select** 0: Not pull-up 1: Pull-up
6	RW	0	**SMB Bus Collision Monitor Enable** 0: Disable 1: Enable
5	RW	0	**Reserved**
4:3	RW	00b	**CR/SDIO Pads Power up Delay Select** 00: 30 ms 01: 10 ms 10: 50 ms 11: 100 ms
2	RW	0	**Select SDIO or CR to Serve SD/MMC Card** 0: SDIO 1:CR
1	RW	0	**Reserved**
0	RW	0	**Mask INTR Before 8259 Initialization Disable** 0: Mask INTR before 8259 initialization 1: Unmask INTR

Offset Address: A0-AFh (D17F0) – Reserved

UART Miscellaneous Control Registers (B0-BFh)

Offset Address: B0h (D17F0)

UART Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**UART2 MIDI Mode Enable** 0: Disable 1: Enable
6	RW	0	**UART1 MIDI Mode Enable** 0: Disable 1: Enable
5	RW	0	**UART 2** 0: Disable 1: Enable
4	RW	0	**UART 1** 0: Disable 1: Enable
3	RW	1b	**APIC C4P State Mode Control** 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: B1h (D17F0) – Reserved

Offset Address: B2h (D17F0)

UART IRQ Routing **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**UART2 IRQ Routing** Refer to Table 20 PnP IRQ Routing Table
3:0	RW	0	**UART1 IRQ Routing** Refer to Table 20 PnP IRQ Routing Table

Offset Address: B3h (D17F0) – Reserved

Offset Address: B4h (D17F0)

UART 1 I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**UART 1 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**UART 1 I/O Base Address [9:3]**

Offset Address: B5h (D17F0)

UART 2 I/O base address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**UART 2 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**UART 2 I/O Base Address [9:3]**

Offset Address: B6h (D17F0) – Reserved

Offset Address: B7h (D17F0)

COM Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:5	RW	0	**Reserved**
4	RW	0	**Enable UART DMA I/O Cycle Positive Decoding** 0: Disable 1: Enable
3	RW	0	**Enable UART DMA Function** 0: Disable 1: Enable
2	RW	0	**COM2 Speed-up Mode Enable** 0: Disable 1: Enable
1	RW	0	**COM1 Speed-up Mode Enable** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: B8h (D17F0)

UART DMA I/O Base Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**UART DMA Control Registers Base Address [7:2]**
1:0	RO	0	**Reserved**

Offset Address: B9h (D17F0)

UART DMA I/O Base Address - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**UART DMA Control Registers Base Address [15:8]**

Offset Address: BAh (D17F0)

COM1 DMA Channel Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	000b	**COM1 Receive DMA Channel Select** 000: No channel selected 100: DMA Channel 0 101: DMA Channel 1 110: DMA Channel 2 111: DMA Channel 3 Others: Reserved
3	RW	0	**Reserved**
2:0	RW	000b	**COM1 Transmit DMA Channel Select** 000: No channel selected 100: DMA channel 0 101: DMA channel 1 110: DMA channel 2 111: DMA channel 3 Others: Reserved

Offset Address: BBh (D17F0)

COM2 DMA Channel Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	000b	**COM2 Receive DMA Channel Select** 000: No channel selected 100: DMA channel 0 101: DMA channel 1 110: DMA channel 2 111: DMA channel 3 Others: Reserved
3	RW	0	**Reserved**
2:0	RW	000b	**COM2 Transmit DMA Channel Select** 000: No channel selected 100: DMA channel 0 is selected for COM2 transmit. 101: DMA channel 1 is selected for COM2 transmit. 110: DMA channel 2 is selected for COM2 transmit. 111: DMA channel 3 is selected for COM2 transmit. Others: Reserved

Offset Address: BE-BCh (D17F0)

SPI MMIO Space Base Address **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:4	RW	0	**SPI MMIO Space Base Address [31:12]**
3:0	RO	0	**Reserved**

Offset Address: BFh (D17F0) – Reserved

Power Management-Specific Configuration Registers (C0-CFh)

Offset Address: C3-C0h (D17F0)

Power Management Capability **Default Value: 0002 0001h**

Bit	Attribute	Default	Description
31:16	RO	0002h	**Power Management Capability** 0002h indicates that: This function does not support D2 or D1 power state. This function does not require PCI clock to generate PME#. This function complies with PCI Power Management Interface Specification Revision 1.1.
15:8	RO	0	**Next Pointer** 0 indicates that there are no additional items in the Capabilities List.
7:0	RO	01h	**Capability ID**

Offset Address: C7-C4h (D17F0)

Power Management Capability **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Capability Data**
23:16	RO	0	**PM CSR (Certificate Signing Request) P2P Support Extensions**
15:2	RO	0	**PM Control / Status (D0/D3 Only) High**
1:0	RW	00b	**PM Control / Status (D0/D3 Only) Low** 00: D0 11: D3

Offset Address: C8-CFh (D17F0) – Reserved

System Management Bus-Specific Configuration Registers (D0-E7h)

Offset Address: D1-D0h (D17F0)

SMBus I/O Base **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**SMBus I/O Base [15:4] (16-byte I/O space)**
3:0	RO	1h	**Hardwire to 01h**

Offset Address: D2h (D17F0)

SMBus Host Configuration **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**SMBus Alert IRQ SCI / SMI Select** 0: SMI 1: SCI
2	RW	0	**SMBus Clock from 128K Source** Divider from 14.318Mhz
1	RW	0	**Enable SMBus IRQ** 0: Disable 1: Enable
0	RW	0	**Enable SMBus Host Controller** 0: Disable 1: Enable

Offset Address: D3h (D17F0)

SMBus Host Slave Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Host Slave Command**

Offset Address: D4h (D17F0)

SMBus Slave Address for Port 1 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Slave Address [7:1] for Port 1**
0	RW	0	**Read / Write for Shadow Port 1** 0: Read 1: Write

Offset Address: D5h (D17F0)

SMBus Slave Address for Port 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Slave Address [7:1] for Port 2**
0	RW	0	**Read / Write for Shadow Port 2** 0: Read 1: Write

Offset Address: D6h (D17F0)

SMBus Revision ID — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**SMBus Revision ID**

Offset Address: D7-DFh (D17F0) – Reserved

Offset Address: E0h (D17F0)

GPI Trigger Level for SCI / SMI Generation — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI Input Trigger Mode for SCI/SMI Generation** Bit [7:2]: GPIO [13:10, 1:0] Bit 1: GPI3 Bit 0: GPI2 0: Falling edge 1: Rising edge

Offset Address: E1h (D17F0)

GPI SCI / SMI Select — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI SCI / SMI Select** Bit [7:2]: GPIO [13:10, 1:0] Bit 1: GPI3 Bit 0: GPI2 0: SCI 1: SMI

Offset Address: E2h (D17F0)

Internal NM PLL Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Inhibit C4 State During USB Isochronous Transaction** 0: Disable 1: Enable
6:0	RW	0	**Reserved**

Offset Address: E3h (D17F0)

Pull-up Option **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**SPI Bus Master as Break Event** 0: Disable 1: Enable
6	RW	0	**VR Change Timer Select** 0: 7.5 us 1: 45us
5	RW	0	**Enable SDIO Device 2 Break Event** 0: Disable 1: Enable
4	RW	0	**Enable SDIO Device 1 Break Event** 0: Disable 1: Enable
3	RW	0	**Enable Card Boot Break Event** 0: Disable 1: Enable
2	RW	0	**Multi-Function Signals: SSPICLK vs. GPIO8 Select** 0: SSPICLK 1: GPIO8
1	RW	1b	**Enable IO Pads (INTR, IGNNE#, A20M#, SMI#, INIT#, FERR#, NMI#) to Use CPU Power Rail** 0: Disable 1: Enable
0	RW	1b	**Enable IO Pads (THRMTRIP#, NAP#, DPSLP#, STPCLK#, SLP#) to Use CPU Power Rail** 0: Disable 1: Enable

Offset Address: E4h (D17F0)

Multi-Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Short C3/C4 Mode** When this bit is enabled, fast entry and recovery latencies of C3/C4 state are performed. In detail, please refer to C3/C4 latency configuration tables. 0: Normal entry and recovery latencies 1: Fast entry and recovery latencies
6	RW	0	**Multi-Function Signal Select: SYSIDLE vs. GPO10** 0: SYSIDLE 1: GPO10
5	RW	0	**Multi-Function Signal Select: CSTATE1, C4PSTOP# vs. GPO5, GPO6** 0: CSTATE1, C4PSTOP# 1: GPO5, GPO6
4	RW	0	**Multi-Function Signal Select: SPKR vs. GPO0** 0: SPKR 1: GPO0
3	RW	0	**Multi-Function Signal Select: SSPISDI, SSPISS# vs. GPI10, GPI11** 0: SSPISDI, SSPISS# 1: GPI10, GPI11
2	RW	0	**Multi-Function Signal Select: SSPISDO vs. GPO4** 0: SSPISDO 1: GPO4
1	RW	0	**Multi-Function Signal Select: SPI vs. GPIO** 0: MSPIDI, MSPICLK, MSPIDO, MSPISS1#, MSPISS0# 1: GPI0, GPIO6, GPO1, GPO2, GPO3
0	RW	0	**Multi-Function Signal Select: THRMTRIP# vs. GPIO7** 0: THRMTRIP# 1: GPIO7

Table 23. C3 Latency Configuration Table

<table>
<tr><th>RxEC[2]</th><th>RxE4[7]</th><th>STOP GRANT to SLP# 1->0</th><th>SLP# 1->0 to CPUSTP# 1->0</th><th>Break Event to CPUSTP# 0->1</th><th>CPUSTP# 0->1 to SLP# 0->1</th><th>SLP# 0->1 to STPCLK# 0->1</th></tr>
<tr><td>0</td><td>0</td><td>7.5~15 us</td><td>8~11.25 us</td><td>7.5~15 us</td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1 to SLP# 0->1</th></tr><tr><td>00</td><td>7~8 us</td></tr><tr><td>01</td><td>14.5~15.5 us</td></tr><tr><td>10</td><td>22~23 us</td></tr><tr><td>11</td><td>29.5~30.5 us</td></tr></table></td><td>7.5 us</td></tr>
<tr><td>0</td><td>1</td><td>0.83~1.66 us</td><td>1~1.25 us</td><td>0.83~1.66 us</td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1 to SLP# 0->1</th></tr><tr><td>00</td><td>0.83 us</td></tr><tr><td>01</td><td>7.5~16 us</td></tr><tr><td>10</td><td>15~23.5 us</td></tr><tr><td>11</td><td>22.5~31 us</td></tr></table></td><td>0.83 us</td></tr>
<tr><td>1</td><td>x</td><td>0.56~1.12 us</td><td>0.84 us</td><td>0.56~1.12 us</td><td>0.56 us</td><td>0.56 us</td></tr>
</table>

Table 24. C4 Latency Configuration Table

<table>
<tr><th>RxEC[2]</th><th>RxE4[7]</th><th>STOP GRANT to SLP# 1->0</th><th>SLP# 1->0 to CPUSTP# 1->0</th><th>CPUSTP# 1->0 to VRDSLP 0->1</th><th>Break Event to VRDSLP 1->0</th><th>VRDSLP 1->0 to CPUSTP# 0->1</th><th>CPUSTP# 0->1 to SLP# 0->1</th><th>SLP# 0->1 to STPCLK# 0->1</th></tr>
<tr><td>0</td><td>0</td><td>7.5~15 us</td><td>8~11.25 us</td><td>3.75~7.5 us</td><td>0~7.5 us</td><td><table><tr><th>RxE5[7] & RxE3[6]</th><th>VRDSLP 1->0 to CPUSTP# 0->1</th></tr><tr><td>0x</td><td>90~132 us</td></tr><tr><td>10</td><td>31~39 us
or 7.5 us</td></tr><tr><td>11</td><td>30~70 us</td></tr></table></td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1 to SLP# 0->1</th></tr><tr><td>00</td><td>7~8 us</td></tr><tr><td>01</td><td>14.5~15.5 us</td></tr><tr><td>10</td><td>22~23 us</td></tr><tr><td>11</td><td>29.5~30.5 us</td></tr></table></td><td>7.5 us</td></tr>
<tr><td>0</td><td>1</td><td>0.83~1.66 us</td><td>1~1.25 us</td><td>0.63~0.83 us</td><td>0~0.83 us</td><td><table><tr><th>Rx8A[7]</th><th>RxE5[7] & RxE3[6]</th><th>VRDSLP 1->0 to CPUSTP# 0->1</th></tr><tr><td>0</td><td>0x</td><td>11.5~13.5 us</td></tr><tr><td></td><td>10</td><td>3.3~4.5 us
or 0.84 us</td></tr><tr><td></td><td>11</td><td>3.5~7.5 us</td></tr><tr><td>1</td><td>0x</td><td>35~45us</td></tr><tr><td></td><td>10</td><td>Not suggested</td></tr><tr><td></td><td>11</td><td>20~25 us</td></tr></table></td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1 to SLP# 0->1</th></tr><tr><td>00</td><td>0.83 us</td></tr><tr><td>01</td><td>7.5~16 us</td></tr><tr><td>10</td><td>15~23.5 us</td></tr><tr><td>11</td><td>22.5~31 us</td></tr></table></td><td>0.83 us</td></tr>
<tr><td>1</td><td>x</td><td>0.56~1.12 us</td><td>0.84 us</td><td>0.28~0.56 us</td><td>0~0.56 us</td><td>0.56 us</td><td>0.56 us</td><td>0.56 us</td></tr>
</table>

Offset Address: E5h (D17F0)

Multi-Function Select 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**C4 VR Recovery Latency Selection Bit** VRDSLP de-assertion to DPSLP de-assertion latency. In detail, please refer to C3/C4 latency configuration tables. RxE5[7] / RxE3[6] — VR Change Timer Select 00 — 90~100 us 01 — 90~100 us 10 — 7.5~15 us 11 — 30~45 us RxE4[7] and RxEC[2] must set to 0.
6	RW	0	**NM Bus Master as Source of Bus Master Status** 0: Disable 1: Enable
5	RW	0	**Enable North Bridge Interrupt to Wake up Cx State** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	0	**CPU Frequency Change** 0: DPSLP# 1: Disable (output high) 0: VRDSLP 1: Disable (output high)
2	RW	0	**PCS1 Chip Select Output via PDIOW#** 0: Disable 1: Enable When enabled, if any C2P cycle hits PCS1 I/O port address range (D17F0 Rx5E-5F), the chip select of PCS1 is asserted and output via PDIOW#.
1	RW	0	**PCS0 Chip Select Output via PDIOR#** 0: Disable 1: Enable When enabled, if any C2P cycle hits PCS0 I/O port address range (D17F0 Rx5C-5D), the chip select of PCS0 is asserted and output via PDIOR#
0	RW	0	**Enable SDIO Device 3 Break Event** 0: Disable 1: Enable

Offset Address: E6h (D17F0)

Cx State Break Event Enable 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Parallel IDE Bus Master as Break Event** 0: Disable 1: Enable
6	RW	0	**USB Device Mode Bus Master as Break Event** 0: Disable 1: Enable
5	RW	0	**PCI Bus Master as Break Event**
4	RW	0	**Card Reader as Break Event** 0: Disable 1: Enable
3	RW	0	**NM Bus Master as Break Event** 0: Disable 1: Enable
2	RW	0	**EHCI Bus Master as Break Event** 0: Disable 1: Enable
1	RW	0	**UHCI Bus Master as Break Event** 0: Disable 1: Enable
0	RW	0	**HDAC / PCI DMA Bus Master as Break Event** 0: Disable 1: Enable

Offset Address: E7h (D17F0)
Cx State Break Event Enable 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable APIC Cycle Reflect to ALL Bus Master Activity Effective Signal** 0: Disable 1: Enable
6	RW	0	**HD Audio Record FIFO Status Reflect Control** Enable HD audio record FIFO not empty signal reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. 0: Disable 1: Enable
5	RW	0	**Enable HD Audio Play Run Bit to Inhibit C4P** When HD audio play run bit is open, C4P can be inhibited. 0: Disable 1: Enable
4	RW	0	**Enable HD Audio Record Run Bit to Inhibit C4P** When HD audio record run bit is open, C4P can be inhibited 0: Disable 1: Enable
3	RW	0	**HD Audio CORB / RIRB RW Pointer Compare Reflect to DMA Control** Enable HD audio CORB / RIRB write / read pointer compare signal reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx00[4]). 0: Disable 1: Enable
2	RW	0	**HD Audio CORB / RIRB Run Bit Reflect to DMA Control** Enable HD audio CORB / RIRB run bit reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx0[4]). 0: Disable 1: Enable
1	RW	0	**HD Audio Record Run Bit Reflect to DMA Control** Enable HD audio record run bit reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx00[4]). 0: Disable 1: Enable
0	RW	0	**HD Audio Play Run Bit Reflect to DMA Control** Enable HD audio play run bit reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx00[4]). 0: Disable 1: Enable

Watchdog Timer Registers (E8-FFh)

Offset Address: EB-E8h (D17F0)
Watchdog Timer Memory Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Watchdog Timer Memory Base [31:8]**
7:0	RO	0	**Hardwire to 0**

Offset Address: ECh (D17F0)
Watchdog Timer Control & C3 Latency Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**V1 Interrupt Routing** This field determines the routing of V1 interrupt. **PIC mode:** 0000: Disabled 0001: IRQ1 0010: IRQ2 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: IRQ15 **APIC mode:** 0000: Disabled 0001: IRQ16 0010: IRQ17 0011: IRQ18 0100: IRQ19 0101: IRQ20 0110: IRQ21 0111: IRQ22 1000: IRQ23
3	RW	0	**Extend Delay from SLP# De-assert to STPCLK# De-assert** In detail, please refer to C3/C4 latency configuration tables. 0: Disable 1: Enable
2	RW	0	**Enable Fast C3 Mode** 0: Depends on RxE4[7] setting 1: Enable fast C3 mode Enable C4 is not allowed. In detail, please refer to C3/C4 latency configuration tables.
1	RW	0	**Enable Watch Dog Timer** If set, this bit can be reset only by PCIRST#. 0: Disable 1: Enable
0	RW	0	**Watchdog Timer Memory** 0: Disable 1: Enable

Offset Address: ED-FBh (D17F0) – Reserved

Offset Address: FCh (D17F0)
Processor Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:3	RW	0	**Reserved**
2:1	RW	0	**DPSLP# to SLP# Latency Adjustment** ***When RxE4[7] =0:*** 00: 7.5 us 01: 15 us 10: 22.5 us 11: 30 us ***When RxE4[7]=1:*** 00: 0.83 us 01: 1.5~7.5 us 10: 7.5~15 us 11: 10~22.5 us
0	RW	0	**Reserved**

Offset Address: FD-FFh (D17F0) – Reserved

SPI MMIO Space Registers (SPI MMIO 000-FFFh)

The base address of SPI MMIO space registers is located in D17F0 RxBE-BCh.

Control Registers (SPI-MMIO 000-009h)

Offset Address: 000h (SPI-MMIO)

SPI Bus0 Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**SPI Bus0 Enable** 0: Disable 1: Enable

Offset Address: 003-001h (SPI-MMIO)

SPI Bus0 Memory Map Base Address **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:0	RW	0	**SPI Bus0 Memory Map Base Address**

Offset Address: 004h (SPI-MMIO)

SPI Bus1 Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**SPI Bus1 Enable** 0: Disable 1: Enable

Offset Address: 007-005h (SPI-MMIO)

SPI Bus1 Memory Map Base Address **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:0	RW	0	**SPI Bus1 Memory Map Base Address**

Offset Address: 008h (SPI-MMIO)

SPI Bus Misc. Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**SPI External Device Interrupt Enable** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 009h (SPI-MMIO)

SPI Bus Interrupt Routing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**SPI IRQ Routing** 0000: IRQ0 0001: IRQ1 … … 1111: IRQ15

Offset Address: 00A-FFFh (SPI-MMIO) – Reserved

Power Management IO Space

ACPI IO Space Registers (PMIO 00-0Bh)

Offset Address: 01-00h (PMIO)

Power Management Status **Default Value: 0000h**

The bits in this register are set by hardware and can be reset by software by writing a one to the desired bit position.

Bit	Attribute	Default	Description
15	RW1C	0	**Wakeup Status** This bit is set when the system is in the suspend state (S1 … S5) and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3/C4 to C0 for the processor).
14	RW1C	0	**Reserved**
13:12	RO	0	**Reserved**
11	RW1C	0	**Power Status** 0: Core power on 1: Abnormal power off
10	RW1C	0	**RTC Alarm Status** This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).
9	RW1C	0	**Sleep Button Status** This bit is set when the sleep button is pressed (SLPBTN# signal asserted low).
8	RW1C	0	**Power Button Status** This bit is set when the PWRBTN# signal is asserted low. If the PWRBTN# signal is held low for more than four seconds, this bit is cleared, the Power Button Status bit is set, and the system will change into the soft off state.
7:6	RO	0	**Reserved**
5	RW1C	0	**Global Status** This bit is set by hardware when the BIOS Release bit (Rx2C[1]) is set (typically by an SMI routine to release control of the SCI / SMI lock). When this bit is cleared by software (by writing a one to this bit position), the BIOS Release bit is also cleared at the same time by hardware.
4	RW1C	0	**Bus Master Status** This bit is set when a bus master request is asserted. All PCI master, ISA master and ISA DMA devices are included.
3:1	RO	0	**Reserved**
0	RW1C	0	**ACPI Timer Carry Status** The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

Offset Address: 03-02h (PMIO)

Power Management Enable **Default Value: 0100h**

The bits defined in this register correspond to the same location of Rx01-00h, Power Management Status Register.

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RW	0	**Reserved**
13:11	RO	0	**Reserved**
10	RW	0	**RTC Alarm Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the RTC Status bit is set. 0: Disable 1: Enable
9	RW	0	**Sleep Button Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Sleep Button Status bit is set. 0: Disable 1: Enable
8	RW	1b	**Power Button** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Power Button Status bit is set. 0: Disable 1: Enable
7:6	RO	0	**Reserved**
5	RW	0	**Global Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Global Status bit (Rx00[5]) is set. 0: Disable 1: Enable
4:1	RO	0	**Reserved**
0	RW	0	**ACPI Timer Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Timer Status bit is set. 0: Disable 1: Enable

Offset Address: 05-04h (PMIO)

Power Management Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	WO	0	**Soft Resume** This bit is used to allow a system using an AT power supply to operate as if an ATX power supply were being used. Refer to the BIOS Porting Guide for implementation details. 0: Disable 1: Enable
14	RO	0	**Reserved**
13	WO	0	**Sleep Enable** Reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the Sleep Type, bits [12:10].
12:10	RW	000b	**Sleep Type** 000: Normal On 001: Suspend to RAM (STR) 010: Suspend to Disk (STD, also called Soft Off). The VCC power plane is turned off while the VSUS33 and VBAT planes remain on. 011: Reserved 100: Power On Suspend without Reset 101: Power On Suspend with CPU/PCI Reset 11x: Reserved In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.
9	RO	0	**Reserved**
8	RW	0	**Suspend-to-Disk Command Generates System Reset Only** 0: Disable. STD command will trigger normal STD power off sequence. 1: Enable. STD command triggers a system reset but not STD power off.
7:3	RO	0	**Reserved**
2	WO	0	**Global Release** This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS Status bit (Rx28[5]). This bit is cleared by hardware when the BIOS Status bit is cleared by software. Note that setting on this bit will cause an SMI to be generated if the BIOS Enable bit (Rx2A[5]) is set.
1	RW	0	**Bus Master Reload** This bit controls whether bus master request (Rx00[4]) resumes the processor from C3/C4 to C0 state. 0: Bus master requests are ignored by power management logic. 1: Bus master requests resume the processor from the C3/C4 state to the C0 state.
0	RW	0	**SCI / SMI Select** This bit controls either SCI or SMI is generated for power management events triggered by the Power Button, Sleep Button and RTC (when PMIO Rx00 bits 8, 9, or 10 equal one). 0: SMI 1: SCI Note that certain power management events can be programmed to select either SCI or SMI interrupt independently of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at PMIO Rx22 and 24). Also, Timer Status & Global Status always generates SCI and BIOS Status always generates SMI.

Offset Address: 06-07h (PMIO) – Reserved

Offset Address: 0B-08h (PMIO)

ACPI Timer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Extended Timer Value** This field reads back 0 if the 24-bit timer option is selected (D17F0 Rx81[3]).
23:0	RO	0	**Timer Value** This field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during system reset, and then continues counting until the 14.31818 MHz input clock of the chip is stopped. If the clock is restarted without a reset, the counter will continue counting from where it was stopped.

Offset Address: 0C-0Fh (PMIO) – Reserved

Processor Power Management Registers (PMIO 10-18h)

Offset Address: 13-10h (PMIO)

Processor Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:6	RW	0	**Reserved**
5	RW	0	**Reserved**
4	RW	0	**Throttling Enable** Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. Its duty cycle is determined by bits [3:0] of this register.
3:0	RW	0	**Throttling Duty Cycle**

Offset Address: 14h (PMIO)

Processor Level 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 2 (LVL2)**

Offset Address: 15h (PMIO)

Processor Level 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 3 (LVL3)**

Offset Address: 16h (PMIO)

Processor Level 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 4 (LVL4)**

Offset Address: 17h (PMIO)

Processor Level 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 5 (LVL5)**

Offset Address: 18-1Fh (PMIO) – Reserved

General Purpose Power Management Registers (PMIO 20-53h)

Offset Address: 21-20h (PMIO)

General Purpose Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**North Module SERR# Status**
14	RW1C	0	**USB Wake-Up in Suspend** For suspend states: POS / STR / STD.
13	RW1C	0	**HDAC Wake-Up Status** It can be set only in suspend mode.
12	RW1C	0	**Battery Low Status** Set when the BATLOW# input is asserted low.
11	RW1C	0	**LID# Status** Set when the edge changes as selected by Rx2C[7] on the LID# input is detected.
10	RW1C	0	**Thermal Detect Status** Set when the edge changes as selected by Rx2C[6] on the THRM# input is detected.
9	RW1C	0	**Mouse Controller PME Status**
8	RW1C	0	**RING# Status** Set when the RING# input is asserted low.
7	RW1C	0	**GP3 Timer Time Out Status**
6	RW1C	0	**INTRUDER# Status** Set when the INTRUDER# pin is asserted low.
5	RW1C	0	**PME# Status** Set when the PME# pin is asserted low.
4	RW1C	0	**EXTSMI# Status** Set when the EXTSMI# pin is asserted low.
3	RW1C	0	**V1 Interrupt Status**
2	RW1C	0	**Internal KBC (Keyboard Controller) PME Status** Set when the internal KBC PME signal is asserted.
1	RW1C	0	**GPI1 Status** Set when the GPI1 pin is asserted low.
0	RW1C	0	**GPI0 Status** Set when the GPI0 pin is asserted low.

Note that the above bits correspond to the respective bits at the same location of the General Purpose SCI Enable and General Purpose SMI Enable registers at offset address 22h and 24h: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one. The above bits are set by hardware only and can only be cleared by writing a one.

Offset Address: 23-22h (PMIO)
General Purpose SCI / RESUME Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SCI on North Module SERR Event** 0: Disable 1: Enable
14	RW	0	**Enable SCI on USB Wake-up Event** 0: Disable 1: Enable
13	RW	0	**Enable SCI on HDAC Wake-up Event** 0: Disable 1: Enable
12	RW	0	**Enable SCI on BATLOW# Event** 0: Disable 1: Enable
11	RW	0	**Enable SCI on LID# Event** 0: Disable 1: Enable
10	RW	0	**Enable SCI on THRM# Event** 0: Disable 1: Enable
9	RW	0	**Enable SCI on Mouse PME** 0: Disable 1: Enable
8	RW	0	**Enable SCI on RING# Event** 0: Disable 1: Enable
7	RW	0	**Enable SCI on GP3 Timer Timeout** 0: Disable 1: Enable
6	RW	0	**Enable SCI on INTRUDER# Event** 0: Disable 1: Enable
5	RW	0	**Enable SCI on PME# Assertion** 0: Disable 1: Enable
4	RW	0	**Enable SCI on EXTSMI# Assertion** 0: Disable 1: Enable
3	RW	0	**Enable SCI on V1 Mode Interrupt** 0: Disable 1: Enable
2	RW	0	**Enable SCI on Internal KBC PME** 0: Disable 1: Enable
1	RW	0	**Enable SCI on GPI1 Assertion** 0: Disable 1: Enable
0	RW	0	**Enable SCI on GPI0 Assertion** 0: Disable 1: Enable

Offset Address: 25-24h (PMIO)

General Purpose SMI / Resume Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SMI on North Module SERR Event** 0: Disable 1: Enable
14	RW	0	**Enable SMI on USB Wake-up Event** 0: Disable 1: Enable
13	RW	0	**Enable SMI on HDAC Wake-up Event** 0: Disable 1: Enable
12	RW	0	**Enable SMI on BATLOW# Event** 0: Disable 1: Enable
11	RW	0	**Enable SMI on LID# Event** 0: Disable 1: Enable
10	RW	0	**Enable SMI on THRM# Event** 0: Disable 1: Enable
9	RW	0	**Enable SMI on Mouse PME** 0: Disable 1: Enable
8	RW	0	**Enable SMI on RING# Event** 0: Disable 1: Enable
7	RW	0	**Reserved**
6	RW	0	**Enable SMI on INTRUDER# Event** 0: Disable 1: Enable
5	RW	0	**Enable SMI on PME# Assertion** 0: Disable 1: Enable
4	RW	0	**Enable SMI on EXTSMI# Assertion** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**Enable SMI on Internal KBC PME** 0: Disable 1: Enable
1	RW	0	**Enable SMI on GPI1** 0: Disable 1: Enable
0	RW	0	**Enable SMI on GPI0** 0: Disable 1: Enable

Offset Address: 26h (PMIO)

Processor Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**PCISTP# Assertion while CLKRUN# is De-asserted** 0: Assert PCISTP# 1: Not assert PCISTP# (no stop on PCICLK)
3	RW	0	**PCI CLKRUN# Control** 0: CLKRUN# is always asserted 1: CLKRUN# will be de-activated after the PCI bus is idle for 26 clocks
2	RW	0	**Host Clock Stop (CPUSTP#) Control** This bit controls whether CPUSTP# is asserted in C3/C4 and S1 states. Normally CPUSTP# is not asserted in C3/C4 and S1 states, only STPCLK# is asserted. 0: CPUSTP# will not be asserted in C3/C4 and S1 states (only STPCLK# is asserted) 1: CPUSTP# will be asserted in C3/C4 and S1 states
1	RW	0	**SLP# Assertion in Processor Level 3 Read** This bit controls whether SLP# is asserted in C3 state. 0: SLP# is not asserted in C3 state 1: SLP# is asserted in C3 state
0	RW	0	**Lower CPU Voltage (Activate VRDSLP) During C3 / S1** This bit controls whether the CPU voltage is lowered in C3/S1 state. The CPU voltage is lowered using the VRDSLP signal to the voltage regulator. To activate this control bit, bits 1 and 2 of this register must be set to 1. 0: Disable (normal voltage during C3/S1) 1: Enable (lower voltage during C3/S1) Notes: 1. To enter C4 state in C3 command read, register bits [2:0] must be set. 2. Reading LVL4 (PMIO Rx16) has the same effect as reading LVL3 with bits [2:0] are set to1. 3. VRDSLP will be activated either in C3 with this control bit set or LVL4 is read.

Offset Address: 27h (PMIO) – Reserved

Offset Address: 29-28h (PMIO)

Global Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**GPIO Range 1 Access Status** This bit is set when GPIO range 1 is accessed.
14	RW1C	0	**GPIO Range 0 Access Status** This bit is set when GPIO range 0 is accessed.
13	RW1C	0	**GP3 Timer Timeout Status** This bit is set when GP3 timer times out.
12	RW1C	0	**GP2 Timer Timeout Status** This bit is set when GP2 timer times out.
11	RW1C	0	**SERIRQ SMI Status** This bit is set when serial interrupt IRQ2 is asserted.
10	RW1C	0	**PMIO Rx5[5] (Sleep Enable) Write Status** This bit reports whether PMIO Rx5[5] has been write-accessed. If PMIO Rx2B[3] is set to enable SMI, an SMI in generated when this bit is 1.
9	RW1C	0	**THRMTRIP# Activity Status** This bit is set when THRMTRIP# is asserted.
8	RW1C	0	**CLKRUN# Resume Status** This bit is set when PCI bus peripherals asserting CLKRUN#.
7	RW1C	0	**Primary IRQ/INIT/NMI/SMI Resume Status** This bit is set at the occurrence of primary IRQs as defined in Rx85-84 of PCI configuration space.
6	RW1C	0	**Software SMI Status** This bit is set when the SMI Command port (Rx2F) is write-accessed.
5	RW1C	0	**BIOS Status** This bit is set when the Global Release bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one) the Global Release bit is reset at the same time by hardware.
4	RW1C	0	**Legacy USB Status** This bit is set when a legacy USB event occurs. This is normally used for USB keyboards.
3	RW1C	0	**GP1 Timer Timeout Status** This bit is set when the GP1 timer times out.
2	RW1C	0	**GP0 Timer Timeout Status** This bit is set when the GP0 timer times out.
1	RW1C	0	**Secondary Event Timer Timeout Status** This bit is set when the secondary event timer times out.
0	RO	0	**Primary Activity Status** This bit can be cleared by writing 1 to clear Rx30-33.

Notes:
1. SMI can be generated when any of the above bits is set if the corresponding control bit is enabled (see the Rx2A Global Enable register bit descriptions).
2. The above status bits are set by hardware and can only be cleared by writing a one to the desired bit position.
3. The above status bits, when set, will trigger assertion of SMI.

Offset Address: 2B-2Ah (PMIO)

Global Enable **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW	0	**SMI Enable on GPIO Range 1 Access** 0: Disable 1: Enable
14	RW	0	**SMI Enable on GPIO Range 0 Access** 0: Disable 1: Enable
13	RW	0	**SMI Enable on GP3 Timer Timeout** 0: Disable 1: Enable
12	RW	0	**SMI Enable on GP2 Timer Timeout** 0: Disable 1: Enable
11	RW	0	**SMI Enable on SERIRQ SMI** 0: Disable 1: Enable
10	RW	0	**SMI Enable on Rx05[5] Write** 0: Disable 1: Enable
9	RW	1b	**THRMTRIP# Activity Power Off Enable** 0: Disable 1: Enable
8	RW	0	**CLKRUN# Resume Enable** This bit may be set to trigger an SMI assertion when the CLKRUN# Resume Status bit is set.
7	RW	0	**Primary IRQ/INIT/NMI/SMI Resume Enable in POS State** This bit may be set to trigger an SMI assertion when the Primary IRQ / INIT / NMI / SMI Resume Status bit is set.
6	RW	0	**SMI Enable on Software SMI** This bit may be set to trigger an SMI assertion when the Software SMI Status bit is set.
5	RW	0	**SMI Enable on BIOS** This bit may be set to trigger an SMI assertion when the BIOS Status bit is set.
4	RW	0	**SMI Enable on Legacy USB** This bit may be set to trigger an SMI assertion when the Legacy USB Status bit is set.
3	RW	0	**SMI Enable on GP1 Timer Timeout** This bit may be set to trigger an SMI assertion when the GP1 Timer Timeout Status bit is set.
2	RW	0	**SMI Enable on GP0 Timer Timeout** This bit may be set to trigger an SMI assertion when the GP0 Timer Timeout Status bit is set.
1	RW	0	**SMI Enable on Secondary Event Timeout** This bit may be set to trigger an SMI assertion when the Secondary Event Timer Timeout Status bit is set.
0	RW	0	**SMI Enable on Primary Activity** This bit may be set to trigger an SMI assertion when the Primary Activity Status bit is set.

Offset Address: 2D-2Ch (PMIO)

Global Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13:11	RW	0	**Reserved**
10	RW	0	**IDE Bus Power-Off** 0: Disable 1: Enable
9	RO	0	**Reserved**
8	RW1C	0	**SMI Active Status** 0: SMI inactive 1: SMI active If the SMI Lock bit is set, this bit must be written 1 to clear it before the next SMI can be generated.
7	RW	0	**LID# Triggering Polarity** 0: Rising edge 1: Falling edge
6	RW	0	**THRM# Triggering Polarity** 0: Rising edge 1: Falling edge
5	RW	0	**Disable Battery Low Resume** 0: Enable resume 1: Disable resume from suspend when BATLOW# is asserted.
4	RO	0	**Reserved** Always reads 0.
3	RO	0	**Reserved** Always reads 0.
2	RW	0	**Power Button Triggering Polarity** 0: Rising edge 1: Falling edge Set to zero to avoid the situation where the Power Button Status bit is set to wake up the system then reset again by 4's-Override status to switch the system into the soft-off state.
1	RW	0	**BIOS Release** This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the Global Status bit. This bit is cleared by hardware when the Global Status bit cleared by software. Note that if the Global Enable bit is set (Power Management Enable register Rx2[5]), setting this bit causes an SCI or SMI to be generated (since setting on this bit causes the Global Status bit to be set).
0	RW	0	**SMI Enable** 0: Disable all SMI generation 1: Enable SMI generation

Offset Address: 2Eh (PMIO) – Reserved

Offset Address: 2Fh (PMIO)

Software SMI Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMI Command** Writing to this port triggers SMI assertion.

Offset Address: 33-30h (PMIO)

Primary Activity Detect Status **Default Value: 0000 0000h**

The Primary Activity Detect Status bits have one-to-one correspondence to the Primary Activity Detect Enable bits in Rx37-34. If the corresponding bit is set in the Enable register, setting of a bit in the Status register will cause the Primary Activity Status (Rx28[0]) bit to be set. Bit in this register default to be 0, is set by hardware only and it could only be cleared by writing 1 to the desired bit.

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW1C	0	**Audio Status** Set if Audio is accessed.
9	RW1C	0	**Keyboard Controller Access Status** Set if the KBC is accessed via I/O port 60h.
8	RW1C	0	**VGA Access Status** Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.
7	RW1C	0	**LPT Port Status** Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).
6	RW1C	0	**Serial Port B Access Status** Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2EFh (COM2 and COM4 respectively).
5	RW1C	0	**Serial Port A Access Status** Set if the serial port is accessed via I/O ports 3F8-3FFh or 3E8-3EFh (COM1 and COM3, respectively).
4	RW1C	0	**Floppy Access Status** Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.
3	RW1C	0	**IDE Access Status** Set if the EIDE controller is accessed via I/O ports 170-177h or 376h.
2	RW1C	0	**Reserved**
1	RW1C	0	**Primary Interrupt Activity Status** Set on the occurrence of a primary interrupt (enabled via the register at D17F0 PCI configuration Rx84h.).
0	RW1C	0	**PCI Master Access Status** Set on the occurrence of PCI master activity.

Notes:

1. Setting of Primary Activity Status may be done to enable a "Primary Activity Event": an SMI will be generated if the Primary Activity Enable bit (Rx2A[0]) is set and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit (Rx38[0]) is set.
2. Bits [9:2] above also correspond to bits of GP Timer Reload Enable register Rx38: If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

Offset Address: 37-34h (PMIO)

Primary Activity Detect Enable **Default Value: 0000 0000h**

The Primary Activity Detect Enable bits have one-to-one correspondence to the Primary Activity Detect Status bits in Rx33-30. Setting of any of Status bits also sets the Primary Activity Status (Rx28[0]) bit which causes the GP0 timer to be reloaded (if the Primary Activity GP0 Enable bit is set) or generates an SMI (if Primary Activity Enable is set).

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW	0	**SMI on Audio Status** 0: Do not set Rx28[0] if Rx30[10] is set. 1: Set Rx28[0] if Rx30[10] is set.
9	RW	0	**SMI on Keyboard Controller Status** 0: Do not set Rx28[0] if Rx30[9] is set. 1: Set Rx28[0] if Rx30[9] is set.
8	RW	0	**SMI on VGA Status** 0: Do not set Rx28[0] if Rx30[8] is set. 1: Set Rx28[0] if Rx30[8] is set.
7	RW	0	**SMI on LPT Status** 0: Do not set Rx28[0] if Rx30[7] is set. 1: Set Rx28[0] if Rx30[7] is set.
6	RW	0	**SMI on Serial Port B Status** 0: Do not set Rx28[0] if Rx30[6] is set. 1: Set Rx28[0] if Rx30[6] is set.
5	RW	0	**SMI on Serial Port A Status** 0: Do not set Rx28[0] if Rx30[5] is set. 1: Set Rx28[0] if Rx30[5] is set.
4	RW	0	**SMI on Floppy Status** 0: Do not set Rx28[0] if Rx30[4] is set. 1: Set Rx28[0] if Rx30[4] is set.
3	RW	0	**SMI on IDE Status** 0: Do not set Rx28[0] if Rx30[3] is set. 1: Set Rx28[0] if Rx30[3] is set.
2	RW	0	**Reserved**
1	RW	0	**SMI on Primary IRQ Status** 0: Do not set Rx28[0] if Rx30[1] is set. 1: Set Rx28[0] if Rx30[1] is set.
0	RW	0	**SMI on PCI Master Status** 0: Do not set Rx28[0] if Rx30[0] is set. 1: Set Rx28[0] if Rx30[0] is set.

Offset Address: 38h (PMIO)

GP Timer Reload Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**GP1 Timer Reload on KBC Access** 0: Normal GP1 Timer Operation 1: Setting of Rx30[9] causes the GP1 timer to reload.
6	RW	0	**GP1 Timer Reload on Serial Port Access** 0: Normal GP1 Timer Operation 1: Setting of Rx30[5] or Rx30[6] causes the GP1 timer to reload.
5	RW	0	**Reserved**
4	RW	0	**GP1 Timer Reload on VGA Access** 0: Normal GP1 Timer Operation 1: Setting of Rx30[8] causes the GP1 timer to reload.
3	RW	0	**GP1 Timer Reload on Drive Access** 0: Normal GP1 Timer Operation 1: Setting of Rx30[4:2] causes the GP1 timer to reload.
2	RW	0	**GP3 Timer Reload on GPIO Range 1 Access** 0: Normal GP3 Timer Operation 1: Setting of Rx28[15] causes the GP3 timer to reload.
1	RW	0	**GP2 Timer Reload on GPIO Range 0 Access** 0: Normal GP2 Timer Operation 1: Setting of Rx28[14] causes the GP2 timer to reload.
0	RW	0	**GP0 Timer Reload on Primary Activity** 0: Normal GP0 Timer Operation 1: Setting of Rx28[0] causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (Rx37-34) with status recorded in the Primary Activity Detect Status register (Rx33-30).

Offset Address: 39h (PMIO)

General Purpose Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved** Always reads 0.
0	RW1C	0	**ASF Wake-up Status**

Offset Address: 3Ah (PMIO)

General Purpose SCI Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved** Always reads 0.
0	RW	0	**SCI Enable on ASF Wake** 0: Disable 1: Enable

Offset Address: 3Bh (PMIO)

General Purpose SMI Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved** Always reads 0.
0	RW	0	**SMI Enable on ASF Wake** 0: Disable 1: Enable

Offset Address: 3C-3Fh (PMIO) – Reserved

Offset Address: 40h (PMIO)

Extend SMI/IO Trap Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW1C	0	**BIOS Write Access Status**
3	RW1C	0	**GP3 Timer Second Timeout With No Cycles** 0: No cycles occurred in between GP3 timer 2nd timeout and reset assertion. 1: One or more cycles occurred in between GP3 timer 2nd timeout and reset assertion.
2	RW1C	0	**GP3 Timer Second Timeout Status** Set to 1 when GP3 timer has two consecutive timeouts.
1	RW1C	0	**GPIO Range 3 Access Status** This bit is set when GPIO range 3 is accessed.
0	RW1C	0	**GPIO Range 2 Access Status** This bit is set when GPIO range 2 is accessed.

Offset Address: 41h (PMIO) – Reserved

Offset Address: 42h (PMIO)

Extend SMI/IO Trap Enable **Default Value: 04h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**SMI on BIOS Write Access** This bit controls whether SMI is asserted when BIOS Write Access Status Rx40[4] is set. 0: Disable 1: Enable (can be reset only through PCI Reset)
3	RW	0	**Override GP3 Timer Second Timeout Reboot** 0: No override. GP3 timer second timeout resets the system only when bit 2 is set and AZSDOUT is strapped to enable auto reboot. 1: Enable GP3 timer second timeout reset anyway (override bit 2 and strapping)
2	RW	1b	**GP3 Timer Second Timeout Reboot** This bit controls whether the system is rebooted when the GP3 timer times out twice (Rx40[2] = 1). 0: Disable 1: Enable
1	RW	0	**SMI on GPIO Range 3 Access** This bit controls whether SMI is generated when Rx40[1] = 1. 0: Disable 1: Enable
0	RW	0	**SMI on GPIO Range 2 Access** This bit controls whether SMI is generated when Rx40[0] = 1. 0: Disable 1: Enable

Offset Address: 43h (PMIO) – Reserved

Offset Address: 45-44h (PMIO)

EXTSMI and Miscellaneous Input Value **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RO	0	**Latest PCS (PCS0-PCS3) IOR/IOW Status** 0: IOR 1: IOW
11	RO	0	**FM SMI or Serial SMI Status**
10	RO	0	**Reserved**
9	RO	0	**SMBus IRQ Status**
8	RO	0	**SMBus Resume Status**
7:0	RO	0	**Reserved**

Offset Address: 46-47h (PMIO) – Reserved

Offset Address: 4B-48h (PMIO)

General Purpose Input **Default Value: 10FA03F2h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28:0	RO	10FA 03F2h	**General Purpose Input** Bit 0: GPI0 Bit 1: GPI1 Bit 2: GPI2 Bit 3: GPI3 Bit 4: GPI4 Bit 5: GPI5 Bit 6: GPI6 Bit 7: GPI7 Bit 8: GPI8 Bit 9: GPI9 Bit 10: GPIO0 Bit 11: GPIO1 Bit 12: GPIO2 Bit 13: GPIO3 Bit 14: GPIO4 Bit 15: GPIO5 Bit 16: GPIO6 Bit 17: GPIO7 Bit 18: GPIO8 Bit 19: GPIO9 Bit 20: GPIO10 Bit 21: GPIO11 Bit 22: GPIO12 Bit 23: GPIO13 Bit 24: GPI10 Bit 25: GPI11 Bit 26: GPI12 Bit 27: GPI13 Bit 28: GPIO14

Offset Address: 4F-4Ch (PMIO)

General Purpose Output **Default Value: FFFF FFFFh**

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output, the output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

Bit	Attribute	Default	Description
31:28	RW	Fh	**Reserved**
27:0	RW	FFF FFFFh	**General Purpose Output** Bit 0: GPO0 Bit 1: GPO1 Bit 2: GPO2 Bit 3: GPO3 Bit 4: GPO4 Bit 5: GPO5 Bit 6: GPO6 Bit 7: GPO7 Bit 8: GPO8 Bit 9: GPO9 Bit 10: GPO10 Bit 11: GPIO0 Bit 12: GPIO1 Bit 13: GPIO2 Bit 14: GPIO3 Bit 15: GPIO4 Bit 16: GPIO5 Bit 17: GPIO6 Bit 18: GPIO7 Bit 19: GPIO8 Bit 20: GPIO9 Bit 21: GPIO10 Bit 22: GPIO11 Bit 23: GPIO12 Bit 24: GPIO13 Bit 25: GPO11 Bit 26: GPO12 Bit 27: GPIO14

Offset Address: 50h (PMIO)

GPI Change Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	**Pin Change Status** Bit 0: GPI2 Bit 1: GPI3 Bit 2: GPIO0 Bit 3: GPIO1 Bit 4: GPIO10 Bit 5: GPIO11 Bit 6: GPIO12 Bit 7: GPIO13 0: No change 1: Change occurs

Offset Address: 51h (PMIO) – Reserved

Offset Address: 52h (PMIO)
GPI Change SCI/SMI Enable — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Pin Change SCI / SM** Bit 0: GPI2 Bit 1: GPI3 Bit 2: GPIO0 Bit 3: GPIO1 Bit 4: GPIO10 Bit 5: GPIO11 Bit 6: GPIO12 Bit 7: GPIO13 0: Disable SMI / SCI on pin input change 1: Enable SMI / SCI on pin input change

Offset Address: 53h (PMIO) – Reserved

IO Trap Registers (PMIO 54-6Fh)

Offset Address: 57-54h (PMIO)
I/O Trap PCI Data — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**PCI Data During I/O Trap SMI**

Offset Address: 59-58h (PMIO)
I/O Trap PCI I/O Address — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**PCI Address During I/O Trap SMI**

Offset Address: 5Ah (PMIO)
I/O Trap PCI Command / Byte Enable — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**PCI Command Type During I/O Trap SMI**
3:0	RO	0	**PCI Byte Enable During I/O Trap SMI**

Offset Address: 5B-5Ch (PMIO) – Reserved

Offset Address: 5Dh (PMIO)
Scratch Register — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Register**

Offset Address: 5E-5Fh (PMIO) – Reserved

Offset Address: 60h (PMIO)
C4P State Event Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable to Support PLL Off State during C4 State** If this bit is set to 1, the bus master monitor timer is enabled. 0: Disable 1: Enable
6	RW	0	**Enable to Support PLL Off during C3 State** If this bit is set to 1, the bus master monitor timer is enabled. 0: Disable 1: Enable
5:4	RW	00b	**Bus Master Idle Timer Tick** 00: 0.125KHz (the max timeout = 2 sec) 01: 0.5KHz (the max timeout = 512 ms) 10: 1KHz (the max timeout = 256 ms) 11: 32KHz (the max timeout = 7 ms)
3	RW	0	**Enable RTC Interrupt to Wake Up C4P State** 0: Disable 1: Enable
2	RW	0	**C4PSTP# Output to the Clock Generator** 0: Disable 1: Enable
1	RW	0	**Enable Keyboard Interrupt to Wake up C4P State** 0: Disable 1: Enable
0	RW	0	**Enable Mouse Interrupt to Wake up C4P State** 0: Disable 1: Enable

Offset Address: 61h (PMIO)
C4P State Bus Master Idle Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Current Count Value of the Bus Master Idle Timer** If this timer is not time out, a C4P state is inhibitive.

Offset Address: 62h (PMIO)
C4P State Bus Master Idle Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Initial Value of the Bus Master Idle Timer** Refer to Rx60[5:4] for details of the time unit.

Offset Address: 63h (PMIO)
C4P State H2R Timer Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Initial Value of Resume Timeout Using 4KHz Clock**

Offset Address: 64h (PMIO)
C4P State Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**PMIO Rx24[4:0] Write Protection Bit** 0: PMIO Rx24[4:0] can be written 1: PMIO Rx24[4:0] can not be written
3:0	RW	0	**Reserved**

Offset Address: 65h (PMIO)

C4P State USB and NM Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**APIC Interrupt Wake Up System from C4P State** 0: Disable 1: Enable
6	RW	0	**Enable PIC Wakeup Event in C4P** 0: Disable 1: Enable
5	RW	0	**Turn Off USB PHY 120MHz PLL** 0: Disable 1: Enable
4	RW	0	**USB Wakeup Event for C4P State** 0: Disable 1: Enable
3	RW	0	**Enable USB Controller Master Reset Bus Master Idle Timer** 0: Ignore USB controller master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
2	RW	0	**Enable USB C4P Function As A Device** 0: Disable 1: Enable
1	RW	0	**PMU Request to USB to Enter C4P State And Wait for USB D3 Mode Acknowledge Signal** 0: Disable 1: Enable
0	RW	0	**Enable USB PHY 120MHz PLL Gating** 0: Disable 1: Enable

Offset Address: 66h (PMIO)

C4P State NM and HDAC Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable HDAC Master Reset Bus Master Idle Timer** 0: Ignore HDAC master reset bus master idle time. 1: Enable bus master idle timer reset signal.
6	RW	0	**HD Wakeup Event for C4P State** 0: Disable 1: Enable
5	RW	0	**NM PLL Gating** 0: Disable 1: Enable
4	RW	0	**Turn Off NM PLL** 0: Disable 1: Enable
3	RW	0	**NM Wakeup Event for C4P State** 0: Disable 1: Enable
2	RW	0	**Enable NM Master Reset Bus Master Idle Timer** 0: Ignore NM master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
1	RW	0	**Option Register to Select Signal from P6IF or PCIS to Indicate STPGNT Special Cycle** 0: PCIS signal 1: P6IF signal
0	RW	0	**PMU Request to USB to Enter C4P State And Wait for NM D3 Mode Acknowledge Signal** 0: Disable 1: Enable

Offset Address: 67h (PMIO)

C4P State IDE Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable C4P State Back to C2** 0: Disable 1: Enable
6	RW	0	**Enable SPI Master Reset Bus Master Idle Timer** 0: Ignore SPI master reset bus master idle timer. 1: Enable SPI bus master idle timer reset signal.
5	RW	0	**Enable C4P State Wakeup for Resume Timeout** 0: Disable 1: Enable
4	RW	0	**Enable UART Wakeup Event in C4P State** 0: Disable 1: Enable
3:2	RW	0	**Reserved**
1	RW	0	**Enable IDE Master Reset Bus Master Idle Timer** 0: Ignore IDE master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
0	RW	0	**Enable IDE Wakeup Event in C4P State** 0: Disable 1: Enable

Offset Address: 68h (PMIO)
C4P State Other Devices Related Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**Enable PCI Master Reset Bus Master Idle Timer** 0: Disable 1: Enable
6	RW1C	0	**PWRGD Status** This bit records PWRGD signal state change: 1: The PWRGD signal state has been toggled since last clear to 0 or power up. It indicates that the last system reset is due to core power lost. 0: The PWRGD signal state remains unchanged since last clear to 0. It indicates that no core power lost since then.
5	RW	0	**Enable PCI REQ# as a C4 PME Event** 0: Disable 1: Enable Note: If PCICLK keeps running (disable CLKRUN# or PCISTP#) during C4P state, this bit must be set to make PCI REQ# be a C4 PME event.
4	RW	0	**Enable USB Device Mode Bus Master Reset Bus Master Idle Timer** 0: Disable 1: Enable
3	RW	0	**Enable CR (Card Reader) Master Reset Bus Mater Idle Timer** 0: Disable 1: Enable
2	RW	0	**Enable Card Reader Wakeup Event in C4P State** 0: Disable 1: Enable
1	RW	0	**Enable SDIO Master Reset Bus Mater Idle Timer** 0: Ignore SDIO master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
0	RW	0	**Enable SDIO Wakeup Event for C4P in State** 0: Disable 1: Enable

Offset Address: 69h (PMIO)
Clock Generator Resume Timer Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Initial Value of Clock Generator Resume Timer**

Offset Address: 6Ah (PMIO)
V1 State Idle Timer Reset Enable 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable SDIO DMA Request to Reset V1 Timer** 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	0	**Enable UART Interrupt to Reset V1 Timer** 0: Disable 1: Enable
4	RW	0	**Enable LPC/UART DMA Request to Reset V1 Timer** 0: Disable 1: Enable
3	RW	0	**Enable HDAC DMA Request to Reset V1 Timer** 0: Disable 1: Enable
2	RW	0	**Enable CR DMA Request to Reset V1 Timer** 0: Disable 1: Enable
1	RW	0	**Enable USB Activity to Reset V1 Timer** 0: Disable 1: Enable
0	RW	0	**Enable IDE DMA Request to Reset V1 Timer** 0: Disable 1: Enable

Offset Address: 6Bh (PMIO)

V1 State Idle Timer Reset Enable 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Reserved**
4	RW	0	**Enable Serial Interrupt to Reset V1 Timer** 0: Disable 1: Enable
3	RW	0	**Enable Mouse Interrupt to Reset V1 Timer** 0: Disable 1: Enable
2	RW	0	**Enable Keyboard Interrupt to Reset V1 Timer** 0: Disable 1: Enable
1	RW	0	**Enable SPI Interrupt to Reset V1 Timer** 0: Disable 1: Enable
0	RW	0	**Enable SPI DMA Request to Reset V1 Timer** 0: Disable 1: Enable

Offset Address: 6Ch (PMIO)

V1 State Related Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable CR Card Detect Interrupt Wakeup in V1 Mode** 0: Disable 1: Enable
6	RW	0	**Enable SPI External Interrupt Wakeup in V1 Mode** 0: Disable 1: Enable
5	RW	0	**Enable Embedded Controller (EC) as KB/MS Interrupt Wakeup in V1 Mode** 0: Disable 1: Enable
4	RW	0	**Enable Serial Interrupt Wakeup in V1 Mode** 0: Disable 1: Enable
3:1	RW	0	**Reserved**
0	RW	0	**Enable V1 Mode** 0: Disable 1: Enable

Offset Address: 6Dh (PMIO)

V1 State Related Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Enable CR/SDIO Card Insertion/Removal to Reflect on Bit 0** 0: Disable 1: Enable
4	RW	0	**Enable UHCI Interrupt to Reflect on Bit 0** 0: Disable 1: Enable
3	RW	0	**Enable UART Interrupt to Reflect on Bit 0** 0: Disable 1: Enable
2	RW	0	**Enable LPC DMA/Bus Master Request to Reflect on Bit 0** 0: Disable 1: Enable
1	RW	0	**Enable KB/MS Interrupt to Reflect on Bit 0** 0: Disable 1: Enable
0	RW1C	0	**V1 Inhibition Status** 0: Inactive. V1 state can be entered 1: Active. V1 state can not be entered If this bit is set, this bit must be written 1 to clear it before the next V1 SCI.

Offset Address: 6Eh (PMIO) – Reserved

Offset Address: 6Fh (PMIO)
Suspend Power Domain **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Enable SUSA# to NM PLL Stop** 0: SUSA# outputs normal SUSA# function. 1: SUSA# to stop NM PLL. This enable register is only valid when Rx95[1] is set to 0. When Rx95[1] is set, SUSA# outputs GPO7.

Power Management Memory Mapped IO Space

Watchdog Timer Memory Base (PM-MMIO 00-07h)

The memory base address of these registers is defined in RxEB-E8h of the D17F0 PCI configuration registers.

Offset Address: 03-00h (PM-MMIO)
Watchdog Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	WO	0	**Watchdog Trigger** Setting this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to the Watchdog Count Register. This bit is always read as zero. Setting this bit has no effect if the watchdog is disabled or stopped.
6:4	RO	0	**Reserved**
3	RO	0	**Disable Watchdog** This bit reflects the state of the watchdog timer hardware. 0: Enable 1: Disable
2	RW	0	**Watchdog Action** This bit determines the action to be taken when the watchdog timer expires. 0: System reset 1: System power off The bit is only valid when the watchdog is enabled.
1	RW1C	0	**Watchdog Fired** When set, the watchdog timer expires and causes the current restart. The bit is cleared by writing a 1 to bit 1 in the Watchdog Control register. Writing a 0 has no effect. The bit is cleared by a power cycle or by the operating system and it must remain cleared for any restart that is not caused by the watchdog timer firing. The bit is only valid when the watchdog is enabled.
0	RW	0	**Watchdog Enable** This bit is used to control or indicate whether the watchdog is in the Enabled\Running and Enabled\Stopped states. 1: Watchdog is in the Enabled\Running state 0: Watchdog is in the Enabled\Stopped state If the watchdog is in the Enabled\Stopped state and a 1 is written to bit 0, the watchdog moves to the running state but a count interval is not started until a 1 is written to bit 7. If the watchdog is in the Enabled\Running state, writing a 1 to bit 0 has no effect. The bit is only valid when the watchdog is enabled.

Offset Address: 07-04h (PM-MMIO)
Watchdog Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RO	0	**Reserved**
9:0	WO	0	**Count Register** This defines the countdown time for the counter. A value of zero is reserved. Reading this register results in the current counter value. Writing to the register has no effect until a one is written to the watchdog trigger bit of the Watchdog Control/Status Register. These bits are only valid when the watchdog is enabled.

System Management IO Space

System Management Bus I/O Space Registers (SMIO 00-0Fh)

The base address for these registers is defined in RxD1-D0 of the D17F0 PCI configuration registers. The System Management Bus I/O space is enabled for access if D17F0 RxD2[0] = 1.

Offset Address: 00h (SMIO)

SMBus Host Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**SMB Host PEC Error** 0: SMBus Host PEC calculation is correct. 1: SMBus Host PEC calculation is error.
6	RW1C	0	**SMB Semaphore** This bit is used as a semaphore among various independent software threads that may need to use the Host SMBus logic and it has no effect on hardware. After reset, this bit reads 0. Write 1 to this bit causes the next read to return 0, all reads after that return 1. Write 0 to this bit has no effect. Software can therefore write 1 to request control and if readback is 0 then it will own usage of the host controller.
5	RO	0	**Reserved**
4	RW1C	0	**Failed Bus Transaction** 0: SMBus interrupt is not caused by failed bus transaction 1: SMBus interrupt is caused by failed bus transaction. This bit may be set when the Rx02[1] is set and can be cleared by write 1 to this bit position.
3	RW1C	0	**Bus Collision** 0: SMBus interrupt is not caused by transaction collision. 1: SMBus interrupt is caused by transaction collision.
2	RW1C	0	**Device Error** 0: SMBus interrupt is not caused by SMBus transaction error 1: SMBus interrupt is caused by SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout).
1	RW1C	0	**SMBus Interrupt** 0: SMBus interrupt is not caused by host command completion 1: SMBus interrupt is caused by host command completion.
0	RO	0	**Host Busy** 0: SMBus controller host interface is not processing a command 1: SMBus host controller is busy in processing a command. None of the other SMBus registers should be accessed if this bit is set.

Offset Address: 01h (SMIO)

SMBus Slave Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**SMB GPIO Slave PEC Error** 0: SMBus GPIO slave PEC calculation is correct. 1: SMBus GPIO slave PEC calculation is incorrect.
6	RW1C	0	**SMB Host Slave PEC Error** 0: SMBus Host Slave PEC calculation is correct. 1: SMBus Host Slave PEC calculation is incorrect.
5	RW1C	0	**Alert Status** 0: SMBus interrupt is not caused by SMBALRT# signal. 1: SMBus interrupt is caused by SMBALRT# signal. This bit will be set only if the Alert Enable bit in Rx08[3] is set.
4	RW1C	0	**Shadow 2 Status** 0: SMBus interrupt is not caused by address match to SMBus Slave Address Port 2 1: SMBus interrupt / resume event is caused by slave cycle address match to SMBus Shadow Address Port 2.
3	RW1C	0	**Shadow 1 Status** 0: SMBus interrupt is not caused by address match to SMBus Slave Address Port 1 1: SMBus interrupt / resume event is caused by slave cycle address match to SMBus Shadow Address Port 1.
2	RW1C	0	**Slave Status** 0: SMBus interrupt is not caused by slave event match. 1: SMBus interrupt / resume event is caused by slave cycle event match of the SMBus Slave Command Register at RxD3 (command match) and the SMBus Slave Event Register at Rx0A (data event match).
1	RO	0	**Reserved**
0	RO	0	**Slave Busy** 0: SMBus controller slave interface is not processing data 1: SMBus controller slave interface is busy receiving data. None of the other SMBus registers should be accessed if this bit is set.

Offset Address: 02h (SMIO)

SMBus Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PEC Enable** 0: Disable 1: Enable SMBus Host to support PEC calculation.
6	RW	0	**Start** 0: Write 0 has no effect 1: Start Execution of Command Write 1 to this bit causes the SMBus controller host interface to initiate execution of the command in the SMBus Command Protocol field (bits [5:2]). All necessary registers should be programmed prior to writing 1 to this bit. The Host Busy bit at Rx00[0] can be used to identify when the SMBus controller has completed command execution.
5:2	RW	0000b	**SMBus Command Protocol** Selects the command type that the SMBus host controller will execute. Reads or Writes are determined by Rx04[0]. **Protocol** 0000: Quick 0001: Byte 0010: Byte Data 0011: Word Data 0100: Process Call 0101: Block 0110: I2C with 10-bit Address 0111: Reserved 10xx: Reserved 1100: I2C Process Call 1101: I2C Block 1110: I2C with 7-bit Address 1111: Universal
1	RW	0	**Kill Transaction in Progress** 0: Normal host controller operation 1: Stop host transaction currently in progress. Setting this bit also sets the status bit Rx00[4] and asserts the interrupt selected by the SMB Interrupt Select bit at RxD2[3].
0	RW	0	**Interrupt Enable** 0: Disable interrupt generation 1: Enable generation of interrupts on completion of the current host transaction

Offset Address: 03h (SMIO)

SMBus Host Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Host Command** This field contains the data transmitted in the command field of the SMBus host transaction.

Offset Address: 04h (SMIO)

SMBus Host Address **Default Value: 00h**

The contents of this register are transmitted in the address field of the SMBus host transaction.

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Address** This field contains the 7-bit address of the targeted slave device.
0	RW	0	**SMBus Read or Write** 0: Execute a WRITE command 1: Execute a READ command

Offset Address: 05h (SMIO)

SMBus Host Data 0 **Default Value: 00h**

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 byte is stored here.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Data 0** For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

Offset Address: 06h (SMIO)

SMBus Host Data 1 **Default Value: 00h**

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 byte is stored here.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Data 1** This register should be programmed with the value to be transmitted in the Data 1 field of an SMBus host interface transaction

Offset Address: 07h (SMIO)

SMBus Block Data **Default Value: 00h**

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the Rx02 and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during a SMBus transaction always starts at index address 0.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Block Data Byte**

Offset Address: 08h (SMIO)

SMBus Slave Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SMBus GPIO Slave PEC Enable** 0: Disable 1: Enable SMBus GPIO Slave to support PEC calculation.
6	RW	0	**SMBus Host Slave PEC Enable** 0: Disable 1: Enable SMBus Host Slave to support PEC calculation.
5	RW	0	**PEC Abort** 0: Disable 1: Enable SMBus to abort PEC calculation error.
4	RW	0	**SMBus GPIO Slave Enable** 0: Disable 1: Enable the generation of a resume event when an external SMBus master generates a transaction with an address that matches the GPIO Slave Address register (SMIO Rx0F).
3	RW	0	**SMBus Alert Enable** 0: Disable 1: Enable generation of an interrupt or resume event on the assertion of the SMBALRT# signal
2	RW	0	**SMBus Shadow Port 2 Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (PCI configuration register: F0RxD5).
1	RW	0	**SMBus Shadow Port 1 Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (PCI configuration register: F0RxD4).
0	RW	0	**SMBus Slave Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (PCI configuration register: F0RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (Rx0A).

Offset Address: 09h (SMIO)

SMBus Shadow Command **Default Value: 00h**

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

Bit	Attribute	Default	Description
7:0	RO	0	**Shadow Command** This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

Offset Address: 0B-0Ah (SMIO)

SMBus Slave Event **Default Value: 0000h**

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

Bit	Attribute	Default	Description
15:0	RW	0	**SMBus Slave Event** This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (Rx0C). When a bit in this register is set and the corresponding bit in Rx0C is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

Offset Address: 0D-0Ch (SMIO)

SMBus Slave Data **Default Value: 0000h**

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

Bit	Attribute	Default	Description
15:0	RO	0	**SMBus Slave Data** This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

Offset Address: 0Eh (SMIO) – Reserved

Offset Address: 0Fh (SMIO)

SMBus GPIO Slave Address **Default Value: 00h**

This register is used to store data values of SMBus GPIO Slave address.

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus GPIO Slave Address** Specifies the address used to match against incoming SMBus addresses for GPIO slave.
0	RO	0	**Reserved**

HPET MMIO SPACE

These registers are offsets from the "HPET Memory Base Address" in the MMIO space, which are located in D17F0 Rx6B-69.

Offset Address: 07-00h (HPET-MMIO)
General Capabilities and ID **Default Value: 0429 B17F 1106 8201h**

Bit	Attribute	Default	Description
63:32	RO	0429 B17Fh	**Main Counter Tick Period** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). A value of 0 in this field is not permitted. The value in this field must be less than or equal to 05F5 E100h (10^8 femtoseconds = 100 nanoseconds). The resolution must be in femtoseconds (rather than picoseconds) in order to achieve a resolution of 50 ppm.
31:16	RO	1106h	**VIA Technologies ID Code**
15	RO	1b	LegacyReplacement Route Capable If this bit is a 1, it indicates that the hardware supports the LegacyReplacement Interrupt Route option.
14	RO	0	**Reserved**
13	RO	0	**Counter Size** 0: Indicates that the main counter is 32 bits wide (and cannot operate in 64-bit mode). 1: Indicates that the main counter is 64 bits wide (although this does not preclude it from being operated in a 32-bit mode).
12:8	RO	02h	**Number of Timers** This indicates the number of timers in this block. The number in this field indicates the last timer (i.e. if there are three timers, the value will be 02h, four timers will be 03h, five timers will be 04h, etc.).
7:0	RO	01h	**Revision ID** This indicates which revision of the function is implemented. The value must not be 01h.

Offset Address: 08-0Fh (HPET-MMIO) – Reserved

Offset Address: 17-10h (HPET-MMIO)
General Configuration **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:2	RO	0	**Reserved**
1	RW	0	**LegacyReplacement Route** 0: Does not support LegacyReplacement Route 1: Supports LegacyReplacement Route If bit 0 and the this bit are both set, the interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in Non-APIC or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in Non-APIC or IRQ8 in the I/O APIC Timer 2 will be routed as per the routing in the timer 2 configure registers. If the LegacyReplacement Route bit is set, the individual routing bits for timers 0 and 1 will have no impact. If the LegacyReplacement Route bit is not set, the individual routing bits for each of the timers are used.
0	RW	0	**Overall Enable** 0: Halt main counter and disable all timer interrupts 1: Allow main counter to run and allow timer interrupts if enabled. This bit must be set to enable for any of the timers to generate interrupts. If this bit is 0, the main counter will halt (will not increment) and no interrupts will be caused by any of these timers.

Offset Address: 18-1Fh (HPET-MMIO) – Reserved

Offset Address: 27-20h (HPET-MMIO)
General Interrupt Status **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:3	RO	0	**Reserved**
2	RW1C	0	**Timer 2 Interrupt Active** Same functionality as Timer 0.
1	RW1C	0	**Timer 1 Interrupt Active** Same functionality as Timer 0.
0	RW1C	0	**Timer 0 Interrupt Active** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. ***Level-triggered Mode*:** This bit default is set to 0. This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. For example, if the bit is already set, a write of 0 will not clear the bit. ***Edge-triggered Mode*:** This bit should be ignored by software. Software should always write 0 to this bit.

Offset Address: 28-EFh (HPET-MMIO) – Reserved

Offset Address: F3-F0h (HPET-MMIO)
Main Counter Value **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Main Counter Value** Bits [31:0] of the counter.

Offset Address: F4-FFh (HPET-MMIO) – Reserved

Timer n Configuration & Capability **Default Value: 0000 FFFF 0000 001Ch**
Offset Address: 107-100h (HPET-MMIO) – Timer 0
Offset Address: 127-120h (HPET-MMIO) – Timer 1
Offset Address: 147-140h (HPET-MMIO) – Timer 2

N is the timer number from 0 to 2, offset address:= (20h*n) + 100h.

Bit	Attribute	Default	Description
63:32	RW	0000 FFFFh	**Timer n Interrupt Routing Capability** This 32-bit field indicates to which interrupts in the I/O (x) APIC this timer's interrupt can be routed. This is used in conjunction with bits [13:9] field. Each bit in this field corresponds to a particular interrupt. For example, if this timer's interrupt can be mapped to interrupts 16, 18, 20, 22, or 24, bits 16, 18, 20, 22 and 24 in this field will be set to 1. All other bits will be 0.
31:14	RW	0	**Reserved**
13:9	RW	0	**Timer n Interrupt Route** This 5-bit read/write field indicates the routing for the interrupt to the I/O APIC. A maximum value of 32 interrupts is supported. Default is 00h. Software writes to this field to select which interrupt in the I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, the value read back will not match what is written. The software must only write valid values. Note: If the LegacyReplacement Route bit is set, Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers.
8	RW	0	**Timer n 32-Bit Mode** Software can set this read/write bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if the software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of doing an atomic 64-bit read to the timer. If the timer is not 64 bits wide, this bit will always be read as 0 and writes will have no effect.
7	RW	0	**Reserved**
6	RW	0	**Timer n Value Set** Software uses this read/write bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set a periodic timer's accumulator. Software does not have to write this bit back to 0 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode.

5	RO	0	**Timer n Size** This read-only field indicates the size of the timer. 0: 32 bits 1: 64 bits
4	RO	1b	**Timer n Periodic Interrupt Capable** If this read-only bit is 1, the hardware will support a periodic mode for this timer's interrupt.
3	RW	1b	**Timer n Type** If bit 4 is 0, this bit will always return 0 when read and writes will have no impact. If bit 4 is 1, then this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. Writing a 1 to this bit enables the timer to generate a periodic interrupt. Writing a 0 to this bit enables the timer to generate a non-periodic interrupt.
2	RW	1b	**Timer n Interrupt Enable** This read/write bit must be set to enable timer n to cause an interrupt when the timer event fires. 0: Disable 1: Enable Note: If this bit is 0, the timer will still operate and generate appropriate status bits, but will not cause an interrupt.
1	RW	0	**Timer n Interrupt Type** 0: The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1: The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active.
0	RW	0	**Reserved**

Offset Address: 110-13Fh (HPET-MMIO) – Reserved

Timer n Comparator Value

Default Value: 0000 0000 FFFF FFFFh

Offset Address: 10F-108h (HPET-MMIO) – Timer 0
Offset Address: 12F-128h (HPET-MMIO) – Timer 1
Offset Address: 14F-148h (HPET-MMIO) – Timer 2

N is the timer number from 0 to 2, offset address:= (20h*n) + 100h.

Bit	Attribute	Default	Description
63:32	RW	0	**Reserved**
31:0	RW	FFFF FFFFh	**Timer n Comparator** Bits [31:0] of the Comparator Value.

SPI Host Controller

SPI Bus 0 MMIO Register Space

MMIO Register (00-87h)

The SPI Bus 0 MMIO base register is located in D17F0 MMIO Rx003-001, whose base register is derived from D17F0 RxBE-BC.

Offset Address: 01-00h (SPI0-MMIO)
SPI Status (SPIS) **Default Value: 0002h**

Bit	Attribute	Default	Description
15	RO/RW	0	**SPI Configuration Lock-Down** 0: No lock-down 1: SPI static configuration information from Rx50 to Rx6F cannot be overwritten. Once set to 1, this bit can only be cleared through hardware reset.
14:4	RO	0	**Reserved**
3	RW1C	0	**Blocked Access Status** 0: Not blocked 1: Blocked Hardware sets this bit to 1 when an access is blocked from running on the SPI interface due to one of the protection policies, or when any of the programmed cycle register is written while a programmed access is already in progress. This bit is set for both programmed accesses and direct memory reads that get blocked. This bit remains asserted until cleared by software writing a 1 or hardware reset.
2	RW1C	0	**SPI Bus 0 Cycle Done Status** 0: Not done 1: SPI controller completes the SPI cycle after software sets bit Rx02[1] This bit remains asserted until cleared by software writing a 1 or hardware reset. Software must make sure this bit is cleared prior to a new programmed access. This bit must be set to “0” after the Status Register Polling sequence completes. It is cleared before and during that sequence.
1	RO	1b	**SPI Bus0 Internal FIFO Empty Flag** 0: FIFO is not empty 1: FIFO is empty
0	RO	0	**SPI Cycle Progress** 0: Cycle not in progress 1: Cycle in progress Hardware sets this bit when software sets Rx02[1]. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must program the next command only when this bit is 0.

Offset Address: 03-02h (SPI0-MMIO)

SPI Control (SPIC) **Default Value: 4004h**

Bit	Attribute	Default	Description
15	RW	0	**SPI SMI# Enable** 0: Disable 1: Enable The SPI asserts the SMI# request whenever Rx00[2] Cycle Done Status bit is set.
14	RW	1b	**Data Cycle** 0: No data is delivered for this cycle. The Data Byte Count (DBC) and data fields are ignored. 1: There are data corresponding to this transaction.
13:12	RW	00b	**Bus 0 Port Select[1:0]** Bus 0 can connect three devices, these two bits select to which device the cycle will go. 00: Select device 0 (CS0). When SPI Strapping Pin = 1, this port connects to SPI ROM. When SPI Strapping Pin = 0, this port connects to SPI device. 01: Select device 1 (CS1). Connects to SPI device. 10: Select device 2 (CS2). Connects to SPI device 11: Reserved
11:8	RW	0	**Data Byte Count** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid setting can be any value from 0 to 15. The number of bytes transferred is the value of this field plus 1.
7	RW	0	**Data Atomic Cycle Sequence** 0: No data atomic cycle sequence 1: When set to 1 along with the SPI Cycle Go (bit 1) assertion, the chip will execute a sequence of data on the SPI interface. SPI will not transfer address again.
6:4	RW	0	**Cycle Opcode Pointer** The field selects one of the programmed opcodes in the Opcode Menu and uses it as the SPI command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	RW	0	**Sequence Prefix Opcode Pointer** 0: Points to the opcode in the ***least*** significant byte of the Prefix Opcodes register 1: Points to the opcode in the ***maximum*** significant byte of the Prefix Opcodes register This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. By making this programmable, this chip supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	RW	1b	**Atomic Cycle Sequence** 0: No atomic cycle sequence 1: When set to 1 along with bit 1 assertion, the chip will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles.
1	RW	0	**SPI Cycle Go** 0: SPI cycle not started 1: Set this bit to 1 to start the SPI cycle defined by the other bits in this register. Rx00[0] SPI Cycle in Progress gets set through this action. This bit always returns 0 on reads. Writes to this bit will be ignored if Cycle In Progress bit is set. Other bits in this register can be programmed for the same transaction when writing this bit to 1.
0	RW	0	**SPI Fast Read Enable** 0: Disable 1: Enable

Offset Address: 07-04h (SPI0-MMIO)

SPI Address (SPIA) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**SPI Cycle Address [23:0]** This field is shifted out as the SPI Address (Msb first).

Offset Address: 0F-08h (SPI0-MMIO)
SPI Data 0 Register (SPID0) **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**SPI Cycle Data[0]** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. The register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

Offset Address: 17-10h (SPI0-MMIO)
SPI Data 1 Register (SPID1) **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**SPI Cycle Data[1]** (Same as SPID0)

Notes for SPI Cycle Data:
SCD Memory Address
SPI Data[0]: SPIBAR + 08h (Size:64bits)
SPI Data[1]: SPIBAR + 10h (Size:64bits)
SPI Data[2..7]: SPIBAR + (18h~47h) Reserved

SCD Shift Order
The SCD[N] register does not begin shift until SPID[N-1] has completely shifted in/out. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-…-8-23-22-…-16-31…-24-39..32…-etc. Bit 56 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address.

Default
1. For SPI Data [7:1]: Default values are 0.
2. For SPI Data 0: This register is initialized to 0 by the reset assertion. However, the least significant byte of this register is loaded with the first Status Register read of the Atomic Cycle Sequence that the hardware automatically runs out of reset. Therefore, bit 0 of this register can be read later to determine if the platform encountered the boundary case in which the SPI flash was busy with an internal instruction when the platform reset deasserted.

Offset Address: 18-4Fh (SPI0-MMIO) – Reserved

Offset Address: 53-50h (SPI0-MMIO)
BIOS Base Address (BBAR) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:8	RW	0	**Bottom of System Flash** This field determines the bottom of the System BIOS. The chip will not run programmed commands nor memory reads whose address field is less than this value. This field corresponds to bit [23:8] of the 3-Bytes address; bit [7:0] are assumed to be 00h for this vector when comparing to a potential SPI address. Software must always program 1s into the upper, don't-care bits of this field based on the flash size. Hardware does not know the size of the flash array and relies upon the correct programming by software. The default value of 0000h results in all cycles allowed. In the event that this value is programmed below some of the BIOS Memory segments, this protection policy takes precedence.
7:0	RO	0	**Reserved**

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 55-54h (SPI0-MMIO)

Prefix Opcode Configuration (PREOP) **Default Value: 0004h**

Bit	Attribute	Default	Description
15:8	RW	0	**Prefix Opcode 1** Software programs an SPI Opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	RW	04h	**Prefix Opcode 0** Software programs an SPI Opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 57-56h (SPI0-MMIO)

Opcode Type Configuration (OPTYPE) **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RW	00b	**Opcode Type7** (Refer to the description in bits [1:0])
13:12	RW	00b	**Opcode Type6** (Refer to the description in bits [1:0])
11:10	RW	00b	**Opcode Type5** (Refer to the description in bits [1:0])
9:8	RW	00b	**Opcode Type4** (Refer to the description in bits [1:0])
7:6	RW	00b	**Opcode Type3** (Refer to the description in bits [1:0])
5:4	RW	00b	**Opcode Type2** (Refer to the description in bits [1:0])
3:2	RW	00b	**Opcode Type1** (Refer to the description in bits [1:0])
1:0	RW	00b	**Opcode Type0** This field specifies information about the corresponding Opcode 0. This information allows the hardware to: 1) Decide whether to use the address field and 2) Provide BIOS and Shared Flash protection capabilities. The encodings of the two bits are: 00: No address associated with this opcode; read cycle type 01: No address associated with this opcode; write cycle type 10: Address required; read cycle type 11: Address required; write cycle type

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 5F-58h (SPI0-MMIO)

Opcode Menu Configuration (OPMENU) **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:56	RW	0	**Opcode 7** (See the description in bits [7:0].)
55:48	RW	0	**Opcode 6** (See the description in bits [7:0].)
47:40	RW	0	**Opcode 5** (See the description in bits [7:0].)
39:32	RW	0	**Opcode 4** (See the description in bits [7:0].)
31:24	RW	0	**Opcode 3** (See the description in bits [7:0].)
23:16	RW	0	**Opcode 2** (See the description in bits [7:0].)
15:8	RW	0	**Opcode 1** (See the description in bits [7:0].)
7:0	RW	0	**Opcode 0** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 63-60h (SPI0-MMIO)

Protected BIOS Range[0] (PBR0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Write Protection Enable** 0: Disable. The base and limit field are ignored when this bit is cleared. 1: Enable. The base and limit fields in this register are valid.
30:24	RO	0	**Reserved**
23:12	RW	0	**Protected Range Limit** This field corresponds to SPI address bits [23:12] and specifies the upper limit of the protected range. Any address greater than the value programmed in this field is unaffected by this protected range.
11:0	RW	0	**Protected Range Base** This filed corresponds to SPI address [23:12] and specifies the lower base of the protected range. Address bits [11:0] are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 67-64h (SPI0-MMIO)

Protected BIOS Range[1] (PBR1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Write Protection Enable** 0: Disable. The base and limit field are ignored when this bit is cleared. 1: Enable. The base and limit fields in this register are valid.
30:24	RO	0	**Reserved**
23:12	RW	0	**Protected Range Limit** This field corresponds to SPI address bits [23:12] and specifies the upper limit of the protected range. Any address greater than the value programmed in this field is unaffected by this protected range.
11:0	RW	0	**Protected Range Base** This filed corresponds to SPI address [23:12] and specifies the lower base of the protected range. Address bits [11:0] are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Offset Address: 6B-68h (SPI0-MMIO)

Protected BIOS Range[2] (PBR2) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Write Protection Enable** 0: Disable. The base and limit field are ignored when this bit is cleared. 1: Enable. The base and limit fields in this register are valid.
30:24	RO	0	**Reserved**
23:12	RW	0	**Protected Range Limit** This field corresponds to SPI address bits [23:12] and specifies the upper limit of the protected range. Any address greater than the value programmed in this field is unaffected by this protected range.
11:0	RW	0	**Protected Range Base** This filed corresponds to SPI address [23:12] and specifies the lower base of the protected range. Address bits [11:0] are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Offset Address: 6Ch (SPI0-MMIO)

SPI Bus 0 Clock Divider **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RW	02h	**SPI Bus 0 Master Mode Clock Divider Value** 00h indicates 33 MHz. 01h indicates 33/2*1 MHz. 02h indicates 33/2*2 MHz. n = value (Rx6C) The exact frequency: 33/2n MHz For PIO Mode, supports up to 33 MHz, For DMA Mode, supports up to 33/2 MHz

Offset Address: 6Dh (SPI0-MMIO)

SPI Bus 0 Miscellaneous Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**SPI Bus 0 Working Node Select** 0: PIO mode 1: DMA mode
5	RO	0	**Reserved**
4	RW	0	**SPI Bus 0 cycle done Interrupt Enable** 0: Disable (SPI will not send interrupt) 1: Enable (SPI will send interrupt when bus0 cycle is done)
3	RW	0	**SPI Bus 0 Dynamic Clock On** 0: Free clock 1: Dynamic clock (when SPI controller doesn't receive request from Host, there is no clock in SPI controller)
2:1	RO	0	**Reserved**
0	RW	0	**PIO Mode Command Post Write Enable** 0: Disable 1: Enable (when Host sends write cycle to SPI controller in PIO mode ,if this bit set to 1,SPI controller will assert write done signal to Host before data transmit done in SPI bus0)

Offset Address: 6Eh (SPI0-MMIO)

SPI Bus 0 Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Latch Master Input Data at Negative Edge of CLK** 0: Disable 1: Enable Note: In PIO mode, when Rx6C is 33MHz, set this bit to 1b.
1:0	RW	00b	**SPI Bus 0 Clock Latency Select When SPI Samples Data** 00: Bypass mode 01: Delay line mode 1 10: Delay line mode 2 11: Delay line mode 3 Note: In DMA mode, when Rx6C is 33/2MHz, set this bit to 11b.

Offset Address: 6Fh (SPI0-MMIO) – Reserved

Offset Address: 70h (SPI0-MMIO)

SPI Bus 0 Interrupt Control **Default Value: FFh**

Bit	Attribute	Default	Description
7	RW	1b	**Bus 0 DMA Write Buffer Block B (High Half) Full Interrupt Enable** 0: Disable 1: Enable
6	RW	1b	**Bus 0 DMA Write Buffer Block A (Low Half) Full Interrupt Enable** 0: Disable 1: Enable
5	RW	1b	**Bus 0 DMA Read Buffer Block B (High Half) Empty Interrupt Enable** 0: Disable 1: Enable
4	RW	1b	**Bu s0 DMA Read Buffer Block A (Low Half) Empty Interrupt Enable** 0: Disable 1: Enable
3	RW	1b	**Bus 0 DMA Read Buffer Under Run Interrupt Enable** 0: Disable 1: Enable
2	RW	1b	**Bus 0 DMA Write Buffer Over Run Interrupt Enable** 0: Disable 1: Enable
1	RW	1b	**Bus 0 Data FIFO Under Run Interrupt Enable** 0: Disable 1: Enable
0	RW	1b	**Bus 0 Data FIFO Over Run Interrupt Enable** 0: Disable 1: Enable

Offset Address: 72-71h (SPI0-MMIO)
SPI Bus 0 Cycle Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Bus 0 Length Check Enable** 0: Disable. SPI will continue transfer/receive data till Rx02[1] is set to 0. The value of Rx72-71[12:0] is "don't care" to SPI controller. 1: Enable. In receive mode, SPI controller will receive data with data length = Rx72-71[12:4]. In transmit mode, SPI controller will send data with data length = Rx71[3:0]. Valid only when Rx02[1] is set to 1.
14:13	RW	0	**Bus 0 Cycle Type** 00: SPI receive data from device 01: SPI transmit data to device 10: SPI transmit data first, then receive data from device (this type needs bit [15]=1) 11: Reserved
12:4	RW	0	**Bus 0 Read Length** Data length which SPI receives from the device. Valid when bit 15 = 1. The real length = This register value + 1. Supports up to 512 bytes.
3:0	RW	0	**Bus 0 Write Length** Data length which SPI transmit to device. Valid when bit 15 = 1. The real length = This register value + 1. Supports up to 16 bytes.

Offset Address: 73h (SPI0-MMIO)
SPI Bus 0 Interrupt Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Bus 0 DMA Write Buffer Block B (High Half)** 0: Not full 1: Full When DMA Write Buffer has been fully written, it means from Rx7B-78 to (Rx7B-78 + Rx7F-7E) has been written, and this status is set to 1.
6	RW1C	0	**Bus 0 DMA Write Buffer Block A (Low Half)** 0: Not full 1: Full When DMA Write Buffer has been half written, it means from Rx7B-78 to (Rx7B-78 + Rx7F-7E/2) has been written, and this status is set to 1.
5	RW1C	0	**Bus 0 DMA Read Buffer Block B (High Half)** 0: Not empty 1: Empty When DMA Read Buffer has been fully read, it means from Rx77-74 to (Rx77-74 + Rx7D-7C) has been read, and this status is set to 1.
4	RW1C	0	**Bus 0 DMA Read Buffer Block A (Low Half)** 0: Not empty 1: Empty When DMA Read Buffer has been half read, from Rx77-74 to (Rx77-74 + Rx7D-7C/2) has been read, and this status is set to 1.
3	RW1C	0	**Bus 0 DMA Read Buffer Underrun Status** 0: Not underrun 1: Underrun
2	RW1C	0	**Bus 0 DMA Write Buffer Overrun Status** 0: Not overrun 1: Overrun
1	RW1C	0	**Bus 0 Data FIFO Underrun Status** 0: Not underrun 1: Underrun
0	RW1C	0	**Bus 0 Data FIFO Overrun Status** 0: Not overrun 1: Overrun

Offset Address: 77-74h (SPI0-MMIO)
SPI Bus 0 DMA Read Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Bus 0 DMA Read Buffer Base Address[31:2]** 4-byte alignment.
1:0	RO	0	**Reserved**

Offset Address: 7B-78h (SPI0-MMIO)
SPI Bus 0 DMA Write Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Bus 0 DMA Write Buffer Base Address [31:2]** 4-byte alignment.
1:0	RO	0	**Reserved**

Offset Address: 7D-7Ch (SPI0-MMIO)
SPI Bus 0 DMA Read Buffer Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Bus 0 DMA Read Buffer Length** 4-byte alignment.

Offset Address: 7F-7Eh (SPI0-MMIO)
SPI Bus 0 DMA Write Buffer Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Bus 0 DMA Write Buffer Length** 4-byte alignment.

Offset Address: 83-80h (SPI0-MMIO)
SPI Bus 0 DMA Read Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Bus 0 DMA Read Pointer** Indicates the address that SPI controller will read data from DMA read buffer.

Offset Address: 87-84h (SPI0-MMIO)
SPI Bus 0 DMA Write Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Bus 0 DMA Write Pointer** Indicates the address that SPI controller will write data to DMA write buffer.

SPI Bus 1 MMIO Register Space

MMIO Register (00-1Bh)

The SPI Bus 1 MMIO base register is located in D17F0 MMIO Rx007-005, whose base register is derived from D17F0 RxBE-BCh.
SPI Memory-Mapped Base Address (SPIBAR) = D17F0 RxBEh~RxBCh [23:0] << 8

Offset Address: 00h (SPI1-MMIO)
SPI Bus 1 Clock Divider **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RW	02h	**SPI Bus 1 Master Mode Clock Divider Value** 00h indicates 33 MHz. 01h indicates 33/2*1 MHz. 02h indicates 33/2*2 MHz. n = value (Rx6C) The exact frequency: 33/2n MHz For DMA Mode, supports up to 33/2 MHz

Offset Address: 01h (SPI1-MMIO)
SPI Bus 1 Miscellaneous Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**SPI Bus 1 Working Mode Select** 0: Master mode 1: Slave mode
5	RO	0	**Reserved**
4	RW	0	**SPI Bus 1 cycle done Interrupt Enable** 0: Disable (SPI will not send interrupt) 1: Enable (SPI will send interrupt when bus1 cycle is done)
3	RW	0	**SPI Bus 1 Dynamic Clock On** 0: Free clock 1: Dynamic clock (when SPI controller doesn't receive request from Host, there is no clock in SPI controller)
2:0	RO	0	**Reserved**

Offset Address: 02h (SPI1-MMIO)
SPI Bus 1 Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Latch Master Input Data at the Negative Edge of CLK** 0: Disable 1: Enable
1:0	RW	00b	**SPI Bus 1 Clock Latency Select When SPI Samples Data** 00: Bypass mode 01: Delay line mode 1 10: Delay line mode 2 11: Delay line mode 3 Note: When Rx00 is 33/2MHz, set this bit to 11b.

Offset Address: 03h (SPI1-MMIO)
SPI Bus 1 Interrupt Control **Default Value: FFh**

Bit	Attribute	Default	Description
7	RW	1b	**Bus 1 DMA Write Buffer Block B (High Half) Full Interrupt Enable** 0: Disable 1: Enable
6	RW	1b	**Bus 1 DMA Write Buffer Block A (Low Half) Full Interrupt Enable** 0: Disable 1: Enable
5	RW	1b	**Bu s1 DMA Read Buffer Block B (High Half) Empty Interrupt Enable** 0: Disable 1: Enable
4	RW	1b	**Bus 1 DMA Read Buffer Block A (Low Half) Empty Interrupt Enable** 0: Disable 1: Enable
3	RW	1b	**Bus 1 DMA Read Buffer Under Run Interrupt Enable** 0: Disable 1: Enable
2	RW	1b	**Bus 1 DMA Write Buffer Over Run Interrupt Enable** 0: Disable 1: Enable
1	RW	1b	**Bus 1 Data FIFO Under Run Interrupt Enable** 0: Disable 1: Enable
0	RW	1b	**Bus 1 Data FIFO Over Run Interrupt Enable** 0: Disable 1: Enable

Offset Address: 05-04h (SPI1-MMIO)

SPI Bus 1 Cycle Control 1 **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Bus 1 Length Check Enable** 0: Disable. SPI will continue transfer/receive data till Rx06[0] is set to 0. The value of Rx05-04[12:0] is “don’t care” to SPI controller. 1: Enable. In receive mode, SPI controller will receive data with data length= Rx05-04[12:4]. In transmit mode, SPI controller will send data with data length= Rx05-04[3:0]. Valid only when Rx06[0] is set to 1.
14:13	RW	0	**Bus 1 Cycle Type** 00: SPI receive data from device 01: SPI send data to device 10: SPI send data first, then receive data from device (this type needs bit [15]=1) 11: Reserved
12:4	RW	0	**Bus 1 Read Length** The data length which SPI receives from the device. Valid when bit 15 = 1. The real length = This register value + 1. Support up to 512 bytes.
3:0	RW	0	**Bus 1 Write Length** The data length which SPI transmit to device. Valid when bit 15 = 1. The real length = This register value + 1. Support up to 16 bytes.

Offset Address: 06h (SPI1-MMIO)

SPI Bus 1 Cycle Control 2 **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RO	1b	**SPI Bus1 Internal FIFO Empty Flag** 0: FIFO is not empty 1: FIFO is empty
1	RW1C	0	**SPI Bus 1 Cycle Done Status** 0: Not done 1: Completes the SPI Cycle after software sets the Rx06[0] bit. This bit remains asserted until cleared by software writing a 1 or hardware reset.
0	RW	0	**Bus 1 Cycle GO** 0: SPI cycle does not started 1: Set this bit to 1 to start the SPI cycle Software must make sure that this bit is 0 before setting this bit to 1 to start a SPI cycle.

Offset Address: 07h (SPI1-MMIO)

SPI Bus 1 Interrupt Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Bus 1 DMA Write Buffer Block B (High Half)** 0: Not full 1: Full When DMA Write Buffer has been fully written, it means from Rx0F-0C to (Rx0F-0C + Rx11-10) has been written, and this status is set to 1.
6	RW1C	0	**Bus 1 DMA Write Buffer Block A (Low Half)** 0: Not full 1: Full When DMA Write Buffer has been half written, it means from Rx0F-0C to (Rx0F-0C + Rx11-10/2) has been written, and this status is set to 1.
5	RW1C	0	**Bus 1 DMA Read Buffer Block B (High Half)** 0: Not empty 1: Empty When DMA Read Buffer has been fully read, it means from Rx0B-08 to (Rx0B-08 + Rx11-10) has been read, and this status is set to 1.
4	RW1C	0	**Bus 1 DMA Read Buffer Block A (Low Half)** 0: Not empty 1: Empty When DMA Read Buffer has been half read, it means from Rx0B-08 to (Rx0B-08 + Rx11-10/2) has been read, and this status is set to 1.
3	RW1C	0	**Bus 1 DMA Read Buffer Underrun Status** 0: Not under run 1: Under run

2	RW1C	0	**Bus 1 DMA Write Buffer Overrun Status** 0: Not overrun 1: Overrun
1	RW1C	0	**Bus 1 Data FIFO Underrun Status** 0: Not under run 1: Under run
0	RW1C	0	**Bus 1 Data FIFO Overrun Status** 0: Not overrun 1: Overrun

Offset Address: 0B-08h (SPI1-MMIO)
SPI Bus 1 DMA Read Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Bus 1 DMA Read Buffer Base Address[31:2]** 4-byte alignment
1:0	RO	0	**Reserved**

Offset Address: 0F-0Ch (SPI1-MMIO)
SPI Bus 1 DMA Write Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Bus 1 DMA Write Buffer Base Address[31:2]** 4-byte alignment
1:0	RO	0	**Reserved**

Offset Address: 11-10h (SPI1-MMIO)
SPI Bus 1 DMA Read Buffer Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Bus 1 DMA Read Buffer Length** 4-byte alignment.

Offset Address: 13-12h (SPI1-MMIO)
SPI Bus 1 DMA Write Buffer Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Bus 1 DMA Write Buffer Length** 4-byte alignment.

Offset Address: 17-14h (SPI1-MMIO)
SPI Bus 1 DMA Read Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Bus 1 DMA Read Pointer** Indicates the address that SPI controller will read data from DMA read buffer.

Offset Address: 1B-18h (SPI1-MMIO)
SPI Bus 1 DMA Write Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Bus 1 DMA Write Pointer** Indicates the address that SPI controller will write data to DMA write buffer.

UART Host Controller

UART Host Controller I/O Space Registers

These register addresses are offsets from the "UART1 I/O Address Base" in the I/O address space, which are located in D17F0 RxB4; or offsets from the "UART2 I/O Address Base", which are located in D17F0 RxB5.

UART Host Control (01-06h)

Offset Address: 01h (UART-IO)
Interrupt Enable Register (IER) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Modem Status Interrupt Enable** The UART will interrupt when modem status changes. 0: Disable 1: Enable
2	RW	0	**Receiver Line Status Interrupt Enable** The UART will interrupt when the receiver line status changes. 0: Disable 1: Enable
1	RW	0	**Transmitter Holding Register Empty Interrupt Enable** If this bit is set, interrupt will be generated when the transmitter buffer is empty. 0: Disable 1: Enable
0	RW	0	**Received Data Available Interrupt Enable** If this bit is set, interrupt will be generated when the receiving register/FIFO contains data to be read by the CPU. 0: Disable 1: Enable

Offset Address: 02h (UART-IO)
Interrupt Identification Register (IIR) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**FIFO Buffer Status** 00: No FIFO 01: FIFO enable but unusable 10: Reserved 11: FIFO enable
5:3	RO	0	**Reserved**
2:1	RO	00b	**Interrupt Occurred Status** 00: Modem status interrupt 01: Transmitter holdings register empty interrupt 10: Received data available interrupt 11: Receiver line status interrupt If an interrupt has occurred, its status will be shown by bits 1 and 2. These interrupts work on a priority status. The Line Status Interrupt has the highest priority, followed by the Data Available Interrupt, then the Transmit Register Empty Interrupt and finally the Modem Status Interrupt which has the lowest priority.
0	RO	0	**Interrupt Pending Status** This bit shows whether an interrupt has occurred or not. 0: Interrupt pending 1: No interrupt pending

Offset Address: 02h (UART-IO)
FIFO Control Register (FCR) **Default Value: C1h**

Bit	Attribute	Default	Description
7:6	WO	11b	**Interrupt Trigger Level Control** 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes
5:3	RO	0	**Reserved**
2	WO	0	**Clear Transmit FIFO** See functionality as Clear Receive FIFO.
1	WO	0	**Clear Receive FIFO** Bits 1 and 2 control the clearing of the transmit or receive FIFOs. Bit 1 is responsible for the receive buffer while bit 2 is responsible for the transmit buffer. Setting these bits to 1 will only clear the contents of the FIFO and will not affect the shift register. These two bits are self resetting, thus it is not necessary to set the bits to '0' when finished. 0: Disable 1: Enable
0	WO	1b	**Enable FIFOs** Bit 0 enables the operation of the receive and transmit FIFOs. Writing a '0' to this bit will disable the operation of transmit and receive FIFOs, thus all data stored in these FIFO buffers will be lost. 0: Disable 1: Enable

Offset Address: 03h (UART-IO)
Line Control Register (LCR) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DLAB or Transceiver Buffer Control** 0: Access to receiver buffer, transmitter buffer and interrupt enable register 1: Divisor Latch Access Bit Bit 7 is DLAB (Divisor Latch Access Bit). When this bit is set, we can access Transceiver Buffer and IER to set the Divisor Latch Access Bit by which we can get commonly used baud rate. When this bit is not set, the function of IER and Receiver Buffer or Transmitter Holding Buffer is used when respectively read or write.
6	RW	0	**Set Break Enable** 0: Disable 1: Enable Bit 6 sets break enable. When active, the TD line goes into "Spacing" state, which causes a break in the receiving UART.
5:3	RW	000b	**Parity Selection** 000: No parity 001: Odd parity 011: Even parity 101: Space parity (sticky) 111: Mark parity (sticky)
2	RW	0	**Stop Bit Length** 0: One stop bit 1: Two stop bits for words of length 6,7 or 8 bits or 1.5 stop bits for word lengths of 5 bits. Note that the receiver only checks the first stop bit.
1:0	RW	00b	**Word Length** 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

Offset Address: 04h (UART-IO)

Modem Control Register (MCR) **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**LoopBack Mode** In this mode any data which is placed in the transmitter registers for output is received by the receiver circuitry on the same chip and is available at the receiver buffer. This can be used to test the UART operation. 0: Disable 1: Enable
3:2	RW	0	**Reserved**
1	RW	0	**Force Request to Send** This bit is set to make the request to send line active. 0: Disable 1: Enable
0	RW	0	**Force Data Terminal Ready** This bit is set to make the Data Terminal Ready line active. 0: Disable 1: Enable

Offset Address: 05h (UART-IO)

Line Status Register (LSR) **Default Value: 60h**

Bit	Attribute	Default	Description
7	RO	0	**Error in Received FIFO** This bit is high when at least one break, parity or framing error has occurred on a byte which is contained in the FIFO. 0: No error occurs 1: Error occurs
6	RO	1b	**Empty Data Holding Registers** When this bit is set, both the transmitter holding register and the shift register are empty. This indicates that no serial conversions are taking place so there should be no activity on the transmit data line. 0: Not empty 1: Empty
5	RO	1b	**Empty Transmitter Holding Register** When this bit is set, the transmitter holding register is empty, thus another byte can be sent to the data port, but a serial conversion using the shift register may be taking place. 0: Not empty 1: Empty
4	RO	0	**Break Interrupt** The break interrupt occurs when the received data line is held in a logic state '0' (Space) for more than the time it takes to send a full word. That includes the time for the start bit, data bits, parity bits and stop bits. 0: No break interrupt 1: Break interrupt occurs
3	RO	0	**Framing Error** A framing error is set when the last bit is not a stop bit. 0: No frame error 1: Frame error occurs
2	RO	0	**Parity Error** A parity error is set when the parity error has occurred. 0: No parity error 1: Parity error occurs
1	RO	0	**Overrun Error** An overrun error is set when the overrun has occurred. An overrun error normally occurs when your program can't read from the port fast enough. If you did not get an incoming byte out of the register fast enough, and another byte just happened to be received, the last byte will be lost and a overrun error will result. 0: No overrun error 1: Overrun error occurs
0	RO	0	**Data Ready** Data Ready is set when a byte has been received by the UART and is at the receiver buffer ready to be read. 0: Data not ready 1: Data ready

Offset Address: 06h (UART-IO)
Modem Status Register (MSR) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Carrier Detect** This bit shows the current state of the data lines DCD. 0: Inactive 1: Active
6	RO	0	**Ring Indicator** This bit shows the current state of the data lines RI. 0: Inactive 1: Active
5	RO	0	**Data Set Ready** This bit shows the current state of the data lines DSR. 0: Inactive 1: Active
4	RO	0	**Clear To Send** This bit shows the current state of the data lines CTS. 0: Inactive 1: Active
3	RO	0	**Delta Data Carrier Detect** See delta functionality as bit 0. 0: Inactive 1: Active
2	RO	0	**Trailing Edge Ring Indicator** 0: Inactive 1: Active The assertion of bit 2 indicates that there was a transformation from low to high state on the Ring Indicator line.
1	RO	0	**Delta Data Set Ready** See delta functionality as bit 0. 0: Inactive 1: Active
0	RO	0	**Delta Clear to Send** 0: Inactive 1: Active Bit 0 of the modem status register shows delta clear to send, delta meaning a change in, thus delta clear to send means that there was a change in the clear to send line, since the last read of this register.

UART DMA Controller I/O Space Registers

These registers are offsets from the "UART DMA IO base address" in the I/O address space, which are located in D17F0 RxB8 and RxB9.

UART DMA Control (00-03h)

Offset Address: 00h (UART-DMA-IO)
UART Port1 (COM1) DMA Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0
5	RW	0	**Enable COM1 Transmit Using High Performance Way with DMA** 0: Disable 1: Enable
4	RW	0	**Enable COM1 Receive Using High Performance Way with DMA** 0: Disable 1: Enable
3	RW	0	**Generate Interrupt for COM1 Transmit Complete** 0: The interrupt signal of COM1 will not be active even the Rx01[1] is set. 1: The interrupt signal of COM1 will be active if the Rx01[1] is set.
2	RW	0	**Generate Interrupt for COM1 Receive Complete** 0: The interrupt signal of COM 1 will not be active even the Rx01[0] is set 1: The interrupt signal of COM 1 will be active if the Rx01[0] is set
1	RW	0	**COM1 Use DMA to Transmit Data** ***When reset as 0, it will be:*** 1) COM1 will not issue any DMA request for transmit data from memory to peripheral. 2) COM1 will ignore DMA acknowledge for its transmit. 3) Rx01[1] will be cleared. ***When set as 1, it will be:*** 1) COM1 will issue DMA request for transmit data from memory to peripheral when COM1 transmit FIFO is available. 2) COM1 will response for DMA acknowledge for data transmit.
0	RW	0	**COM1 Use DMA to Receive Data** ***When reset as 0, it will be:*** 1) COM1 will not issue any DMA request for transmit data from peripheral to memory. 2) COM1 will ignore DMA acknowledge for its receive. 3) Rx01[0] will be cleared. ***When set as 1,it will be:*** 1) COM1 will issue DMA request for receive data from peripheral to memory when COM1 receive FIFO is available. 2) COM1 will response to DMA acknowledge for data receive.

Offset Address: 01h (UART-DMA-IO)
UART Port1 (COM1) DMA Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved** Always reads 0
1	RW1C	0	**Status of Interrupt for COM1 Transmit Complete** 0: The DMA for COM1 transmit has not finished. 1: The DMA for COM1 transmit has finished. Write 1 or disable R00[1] to clear.
0	RW1C	0	**Status of Interrupt for COM1 Receive Complete** 0: The DMA for COM1 receive has not finished. 1: The DMA for COM1 receive has finished. Write 1 or disable Rx00[0] to clear.

Offset Address: 02h (UART-DMA-IO)

UART Port2 (COM2) DMA Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0
5	RW	0	**Enable COM2 Transmit Using High Performance Way with DMA** 0: Disable 1: Enable
4	RW	0	**Enable COM2 Receive Using High Performance Way with DMA** 0: Disable 1: Enable
3	RW	0	**Generate Interrupt for COM2 Transmit Complete** 0: The interrupt signal of COM2 will not be active even the Rx03[1] is set. 1: The interrupt signal of COM2 will be active if the Rx03[1] is set.
2	RW	0	**Generate Interrupt for COM2 Receive Complete** 0: The interrupt signal of COM2 will not be active even the Rx03[0] is set 1: The interrupt signal of COM2 will be active if the Rx03[0] is set
1	RW	0	**COM2 Use DMA to Transmit Data** ***<u>When reset as 0, it will be:</u>*** 1) COM2 will not issue any DMA request for transmit data from memory to peripheral. 2) COM2 will ignore DMA acknowledge for its transmit. 3) Rx03[1] will be cleared. ***<u>When set as 1, it will be:</u>*** 1) COM2 will issue DMA request for transmit data from memory to peripheral when COM2 transmit FIFO is available. 2) COM2 will response to DMA acknowledge for data transmit.
0	RW	0	**COM2 Use DMAC to Receive Data** ***<u>When reset as 0, it will be:</u>*** 1) COM2 will not issue any DMA request for transmit data from peripheral to memory. 2) COM2 will ignore DMA acknowledge for its receive. 3) Rx03[0] will be cleared. ***<u>When set as 1, it will be:</u>*** 1) COM2 will issue DMA request for receive data from peripheral to memory when COM2 receive FIFO is available. 2) COM2 will response to DMA acknowledge for data receive.

Offset Address: 03h (UART-DMA-IO)

UART Port2 (COM2) DMA Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved** Always reads 0
1	RW1C	0	**Status of Interrupt for COM2 Transmit Complete** 0: The DMA for COM2 transmit has not finished. 1: The DMA for COM2 transmit has finished. Write 1 or disable Rx02[1] to clear.
0	RW1C	0	**Status of Interrupt for COM2 Receive Complete** 0: The DMA for COM2 receive has not finished. 1: The DMA for COM2 receive has finished. Write 1 or disable Rx02[0] to clear.

DEVICE 17 FUNCTION 7 (D17F7): SOUTH-NORTH MODULE INTERFACE CONTROL

PCI Configuration Space

This configuration is provided to facilitate the configuration of the North Module Interface logic of the South Module ("SM") without requiring new enumeration code. This function is represented as Device 17, Function 7.

Header Registers (00-3Fh)

Offset Address: 01-00h (D17F7)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D17F7)
Device ID — **Default Value: A353h**

Bit	Attribute	Default	Description
15:0	RO	A353h	**Device ID**

Offset Address: 05-04h (D17F7)
PCI Command — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RW	0	**SERR# Enable** 0: Disable 1: Enable
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0. (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0. (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0. (Not supported)
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RO	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D17F7)

PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RW1C	0	**Signaled System Error (SERR# Asserted)**
13	RW1C	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion**
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Set When Set or Observed SERR# and Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Reserved
6	RO	0	**Reserved**
5	RO	0	**66 MHz Capable**
4	RO	0	**Capability List** 0: No new capability linked list 1: Available. Implement the pointer for a new capability linked at Rx34.
3:0	RO	0	**Reserved**

Offset Address: 08h (D17F7)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D17F7)

PCI Header Registers **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D17F7) – Reserved

Offset Address: 0Dh (D17F7)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice Bits [7:3] for CPU as A Master (In Unit of PCI Clocks)** Bits [7:3] is programmable; however it is always read as 0 if RxE0[5] = 1.
2:0	RO	0	**Reserved**

Offset Address: 0Eh (D17F7)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device. It adheres to the PCI-PCI Bridge Configuration.

Offset Address: 0Fh (D17F7)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST**
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D17F7) – Reserved

Offset Address: 2D-2Ch (D17F7)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D17F7)
Subsystem ID **Default Value: 7323h**

Bit	Attribute	Default	Description
15:0	RO	7323h	**Subsystem ID**

Offset Address: 30-33h (D17F7) – Reserved

Offset Address: 34h (D17F7)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer** Byte offset into configuration space to capability list 0 indicates the end of the list.

Offset Address: 35-3Fh (D17F7) – Reserved

South -North Module Interface Control (40-5F)

Offset Address: 40-4Eh (D17F7) – Reserved

Offset Address: 4Fh (D17F7)
South-North Module Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Device Number and Function Number of Internal Configuration Cycle Output to External PCI Bus** 0: Disable 1: Enable This bit is only used when bit 6 is 1b.
6	RW	0	**Enable P2P Bridge Header for External PCI Bus** 0: Disable 1: Enable Rx4F[6] needs to be set to 0, then IDSEL is exported for most SM devices. Except following configurations: 1. For D17F7, it is internal configuration to PCCA, and does not appear on CI bus 2. For D20F0, it is HD audio configuration. It is not through PCI bus, but it has dedicated interface.
5:4	RW	0	**Reserved**
3	RW	0	**Improve P2CR (PCI Master to DRAM Read Cycle) Performance** 0: Disable 1:Enable
2	RW	0	**Hide C2P (CPU to PCI) Cycle for Internal Devices on PCI Bus** When bit 6 is set to 1, only cycles which act with external PCI devices will appear on PCI Bus. 0: Cycles of internal PCI devices show on PCI bus then to internal device. 1: Cycles of internal PCI devices go to internal devices directly.
1	RW	0	**Support Extended Configuration Space Up to 4096 Bytes** 0: Disable 1: Enable
0	RW	0	**C2P Cycle Wait till P2C Write Flushed (Except C2P Post-Write)** 0: Disable. CPU to PCI Peripheral Device Read is not blocked. 1: Enable. CPU to PCI Peripheral Device Read waits for PCI1 P2C write FIFO empty.

Offset Address: 50h (D17F7)
Bus Priority of SM Peripheral Device 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Card Reader Priority** 0: Low Priority 1: High Priority
6	RW	0	**SDIO Priority** 0: Low Priority 1: High Priority
5	RW	0	**Reserved**
4	RW	0	**USB Priority** 0: Low Priority 1: High Priority
3	RW	0	**HDAC Priority** 0: Low Priority 1: High Priority
2	RW	0	**IDE Priority** 0: Low Priority 1: High Priority
1	RW	0	**LPC / UART Priority** 0: Low Priority 1: High Priority
0	RW	0	**PCI1 Priority** 0: Low Priority 1: High Priority

Offset Address: 51h (D17F7)
P2P Bridge Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Subtract Decode for P2P Cycle** 0: Disable 1: Enable
6:3	RW	0	**Reserved**
2	RW	0	**Enable PCI Master Function** 0: Enable PCI master function by D19F0 Rx04[2] 1: Enable PCI master function even when D19F0 Rx04[2] is disabled.
1	RW	0	**Reserved**
0	RW	0	**Support Subtract Decode in PCI to PCI Bridge Class Code** 0: Class code will be 060400 as positive decode P2P Bridge 1: Class code will be 060401 as subtractive decode P2P Bridge (The setting of this register should be sync with the setting of Rx51[7])

Offset Address: 52h (D17F7)
CCA Arbitration Occupy Timer Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**SM Internal Device Occupy Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants
3:0	RW	0001b	**HDAC Occupy Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants

Offset Address: 53h (D17F7)
CCA Arbitration Promote Timer Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**SM Internal Device Promote Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants
3:0	RW	0001b	**HDAC Promote Timer** 0000: Disable timer, granted as long as request asserted 0001 : Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants

Offset Address: 54h (D17F7)
CCA REQ Timing Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Synchronize** SPI **REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
5	RW	0	**Synchronize Card Reader REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
4	RW	0	**Synchronize SDIO REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
3	RW	0	**Synchronize IDE REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
2	RW	0	**Reserved**
1	RW	0	**Synchronize USB REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
0	RW	0	**Synchronize LPC / ISA REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using

Offset Address: 55h (D17F7)
RIOPU for PAD **Default Value: 0Fh**

Bit	Attribute	Default	Description
7:3	RW	00001b	**Reserved (Do Not Program)**
2	RW	1b	**IRQ14, PDIOR#, PDIOW# Signal Pad Internal Pull-Up** 0: Disable 1: Enable
1	RW	1b	**REQ[1:0]#, GNT[1:0]#, INTA# Signal Pad Internal Pull-Up** 0: Disable 1: Enable
0	RW	1b	**FRAME#, TRDY#, IRDY#, STOP#, DEVSEL# Signal Pad Internal Pull-Up** 0: Disable 1: Enable

Offset Address: 56h (D17F7)
Strapping Pin Value **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**DebugLink Mode Enable Status** 1: DebugLink mode is enabled 0: DebugLink mode is disabled. xD mode is enabled. Default sets from the strapping signal TDO during system initialization. The DebugLink mode is for internal debugging purpose only.
6	RO	0	**Boot ROM Interface Select** 0: SPI / LPC ROM Default sets from the strapping signal MSPISS2# during system initialization.
5:4	RO	00b	**IDE Controller** 00: IDE Others: Reserved Default sets from the strapping signals MSPISS1# and MSPISS0# during system initialization.
3	RO	0	**Reserved**
2	RO	0	**LPC FWH Command** 0: Disable 1: Enable Default sets from the strapping signal AZSYNC during system initialization.
1	RO	0	**System Auto Reboot** 0: Enable 1: Disable Default sets from the strapping signal AZSDOUT during system initialization.
0	RO	0	**SPI / LPC ROM Select** 0: LPC ROM 1: SPI ROM Default sets from the strapping signal AZBITCLK during system initialization.

Offset Address: 57-5Fh (D17F7) – Reserved

DRAM Configuration (60h)

Offset Address: 60h (D17F7)
DRAM Ending for Bank 7 **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**DRAM Bank 7 Ending Address High (Host Address Bits[31:24])**

Shadow RAM Control (61-6Fh)

Offset Address: 61h (D17F7)

Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**C8000-CBFFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
3:2	RW	00b	**C4000-C7FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
1:0	RW	00b	**C0000-C3FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)

Offset Address: 62h (D17F7)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**D8000-DBFFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
3:2	RW	00b	**D4000-D7FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
1:0	RW	00b	**D0000-D3FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)

Offset Address: 63h (D17F7)

Page-E / F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**E0000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**F0000-FFFFFh Memory Space Access Control** See bits [7:6] descriptions.
3:2	RW	00b	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)
1:0	RW	0	**Reserved**

Offset Address: 64h (D17F7)

Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**E8000-EBFFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
3:2	RW	00b	**E4000-E7FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
1:0	RW	00b	**E0000-E3FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)

Offset Address: 65-6Fh (D17F7) – Reserved

Conventional PCI Bus Control (70-7Fh)

Offset Address: 70h (D17F7)
CPU to PCI Flow Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU to PCI Post-Write** 0: Disable 1: Enable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed).
6	RW	0	**PCI Delay Transaction for Master Read when Timer Time-Out** 0: Disable 1: Enable To enable this function, RxE3[0] must be set to 1. When this bit is set, the PCI controller will assert STOP# when a PCI master read occupies the PCI bus longer than the PCI Master Timer period. PCI Master Timer is set up through Rx75[2:0]. If D17F7 RxE3[0] is not set concurrently, STOP# will NOT be asserted even after the timer times out in the following conditions: GNTPK is on There is only one PCI master request
5:4	RW	00b	**PCI Master to DRAM Prefetch Control** 00: Always prefetch 10: Prefetch only for enhancing command x1: Disable prefetch
3	RW	0	**PCI Delay Transaction for Master Read** 0: Disable 1: Assert STOP# for PCI master read cycle and start delay transaction.
2	RW	0	**Reserved**
1	RW	0	**Delay Transaction** 0: Disable 1: Enable
0	RW	0	**Cache Line Size** 0: 4QW 1: 8QW

Offset Address: 71h (D17F7)
CPU to PCI Flow Control 2 **Default Value: 48h**

Bit	Attribute	Default	Description
7	RW1C	0	**Retry Status** 0: No retry occurred 1: Retry occurred
6	RW	1b	**Action When Retry Timeout** 0: Continuous retry (record status only) 1: Flush buffer (write) or return 0FFFFFFFFh (read)
5:4	RW	00b	**Retry Count (before back off CPU)** 00: Retry 2 times, back off CPU 01: Retry 16 times, back off CPU 10: Retry 4 times, back off CPU 11: Retry 64 times, back off CPU
3	RW	1b	**PCI Burst Timeout Enable** 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	0	**Compatible TYPE#1 Configuration Cycle AD31** 0: Fix AD31 1: Support type#1 configuration cycle
0	RW	0	**Reserved**

Offset Address: 72h (D17F7)
PCI P2C Read Caching and Prefetch Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**No Arbitration on PCI Bus during PCI-DMA Period** 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	0	**Conservative Read Caching** 0: Disable 1: Enable If this bit is set to 1, the previous prefetched data will be flushed when PCI master changes or starting address is not consecutive.
4	RW	0	**Reserved**
3	RW	0	**P2CR Pre-fetched Data Flushing Condition** 0: Pre-fetched data will only be flushed when C2P cycle occurs or when interrupt comes. 1: Besides the above conditions, the pre-fetched data will also be flushed when the next FRAME# comes with different REQ/GNT or address.
2	RW	0	**P2CR Pre-fetched Data Control** 0: Pre-fetched data is invalidated when FRAME# is de-asserted without STOP. 1: Pre-fetched data is invalidated based on the setting of bit 3.
1:0	RW	00b	**P2CR FIFO Prefetch Depth** 00: Prefetch if outstanding read <= 1 line 01: Prefetch if outstanding read <= 2 line 10: Prefetch if outstanding read <= 3 line 11: Prefetch if outstanding read <= 5 line

Offset Address: 73h (D17F7)
PCI Master Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**PCI Master 1-Wait State Write** 0: Disable 1: Enable
5	RW	0	**PCI Master 1-Wait State Read** 0: Disable 1: Enable
4	RW	0	**APIC Cycle Block P2C Write Cycle** 0: Enable 1: Disable
3	RW	0	**P2CR Caching Flush by NM Special Cycle** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**PCI Master Broken Timer Enable** 0: Disable 1: Enable. Force into arbitration when there is no FRAME# 16 PCICLK after GNT.

Offset Address: 74h (D17F7)
South-North Module Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic CCA Clock Stop** 0: Enable 1: Disable
6	RW	0	**Dynamic PCI1 Clock Stop (including VKCKG)** 0: Enable 1: Disable
5	RW	0	**Reserved**
4	RW	0	**Lock Cycle Issued by CPU Flush P2C Cycles Before C2P**
3	RW	0	**Lock Cycle Issued by CPU Block P2C Cycles**
2:0	RW	0	**Reserved**

Offset Address: 75h (D17F7)

PCI Arbitration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Arbitration Mode** 0: REQ-based (arbitrate at the end of REQ#) 1: Frame-based (arbitrate as FRAME# asserts)
6:4	RW	0	**PCI Bus Time Slice Bits [2:0] for CPU as A Master (In Unit of PCI Clocks)**
3	RW	0	**PCI Master Time-out / New Grant Mechanism Control** 0: Enable PCI Master time-out / disable new grant mechanism 1: Disable PCI Master time-out / enable new grant mechanism
2:0	RW	000b	**PCI Master Bus Timeout** 000: Disable 001: 1x16 PCLKs 010: 2x16 PCLKs 011: 3x16 PCLKs 111: 7 x 16 PCLKs

Offset Address: 76h (D17F7)

PCI Arbitration 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IO Port 22 Enable (SM)** 0: CPU access to IO address 22 is passed onto the PCI bus 1: CPU access to IO address 22 is processed internally IO
6	RW	0	**PCI Bus Parking at the Last PCI Master** 0: Disable 1: Enable
5:4	RW	00b	**Master Priority Rotation Control** 00: Disable 01: Grant to CPU after every PCI master grant 10: Grant to CPU after every 2 PCI master grants 11: Grant to CPU after every 3 PCI master grants
3:2	RW	00b	**Selected REQ# as REQ4 for PCI1** 01: REQ0 10: REQ1 Others: reserved
1	RW	0	**Reserved**
0	RW	0	**Enable REQ4 for PCI1 as High Priority Master** 0: Disable 1: Enable

Offset Address: 77h (D17F7)

South Module Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**CPU to PCI Peripheral Device Read Blocked by PCI1 FIFO Empty** 0: CPU to PCI peripheral device read blocked by PCI master to memory write 1: CPU to PCI peripheral device read blocked by PCI1 FIFO empty CPU to PCI peripheral device read is blocked by PCI master to memory write when Rx4F[0] = 1. Note: This bit needs to work with Rx4F[0] assertion.
5	RW	0	**Reserved**
4:3	RW	00b	**Read FIFO Timer** 00: No timeout 01: Timeout after 1 ms 10: Timeout after 4 ms 11: Timeout after 16 ms
2:0	RW	0	**Reserved**

Offset Address: 78h (D17F7)

PCI PAD Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Data Pad (AD, PAR) Driving Control** 0: Disable 1: Enable
6	RW	0	**Data Pad (AD, PAR) Slew Rate Control** 0: Disable 1: Enable
5	RW	0	**Strobe Pad (GNT) Driving Control** 0: Disable 1: Enable
4	RW	0	**Strobe Pad (GNT) Slew Rate Control** 0: Disable 1: Enable
3:2	RW	0	**Data in Delay**
1	RW	0	**Reserved**
0	RO	0	**Bridge is V2X Capable** Note: V2X means the frequency of PCICLK is 66MHz.

Offset Address: 79h (D17F7)

PCI V2X Data / Strobe Out Delay Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Data Out Change Based Clock** 0: Data out changed by internal clock 1: Data out changed by external PCICLK
6:4	RW	000b	**Data Out Delay** 000: No delay 001: Delay 0.7 ns 010: Delay 1.3 ns 011: Delay 2.0 ns 100: Delay 3.1 ns 101: Delay 3.8 ns 110: Delay 4.4 ns 111: Delay 5.1 ns
3	RW	0	**Strobe Out Source Clock** 0: Strobe out from internal clock 1: Strobe out from external PCICLK
2:0	RW	000b	**Strobe Out Delay** 000: No delay 001: Delay 0.7 ns 010: Delay 1.3 ns 011: Delay 2.0 ns 100: Delay 3.1 ns 101: Delay 3.8 ns 110: Delay 4.4 ns 111: Delay 5.1 ns

Offset Address: 7Ah (D17F7)

PCI V2X Device Capability — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PREQ's Device Is Capable of V2X** Internal devices pass to PCI bus in V2X mode. 0: Not support V2X mode 1: Support V2X mode Note: PREQ means the request from CCA.
6	RW	0	**REQ6's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
5	RW	0	**REQ5's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
4	RW	0	**REQ4's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
3	RW	0	**REQ3's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
2	RW	0	**REQ2's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
1	RW	0	**REQ1's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
0	RW	0	**REQ0's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode

Offset Address: 7Bh (D17F7)

REQ Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**PREQ Status** PREQ is for internal devices. 0: Inactive 1: Active
6	RO	0	**REQ6 Status** 0: Inactive 1: Active
5	RO	0	**REQ5 Status** 0: Inactive 1: Active
4	RO	0	**REQ4 Status** 0: Inactive 1: Active
3	RO	0	**REQ3 Status** 0: Inactive 1: Active
2	RO	0	**REQ2 Status** 0: Inactive 1: Active
1	RO	0	**REQ1 Status** 0: Inactive 1: Active
0	RO	0	**REQ0 Status** 0: Inactive 1: Active

Offset Address: 7Ch (D17F7)

MSI Related Control **Default Value: 02h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	1b	**APIC FSB Is Directly Up Through CCA (not on PCI)** 0: Disable 1: Enable To enable this function, both Rx74[2] and Rx7C[1] must be set to 1.
0	RW	0	**Reserved**

Offset Address: 7D-7Fh (D17F7) – Reserved

CCA Related Control (80-CFh)

Offset Address: 80h (D17F7)
CCA New Feature Option — **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**PCI1 Upstream Read Cycle Does Not Pass Write** 0: PCI1 upstream read passes write 1: PCI1 upstream read does not pass write
1	RW	0	**HDAC Upstream Read Cycle Does Not Pass Write** 0: HDAC upstream read cycle passes write 1: HDAC upstream read cycle does not pass write
0	RW	0	**APIC Cycle Blocks Upstream Write** 0: APIC cycle does not block HDAC upstream write cycle 1: APIC cycle blocks HDAC upstream write cycle

Offset Address: 81h (D17F7)
Bus Priority of SM Peripheral Device 2 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**SPI Priority** 0: Low priority 1: High priority

Offset Address: 82h (D17F7)
CCA Test Mode Address Selection — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:2	RW	0	**CCA Interface Monitor Action Selection** 1h: Monitor the action of the interface between CCA and legacy devices 2h: Monitor the action of the interface between CCA and IDE 3h: Monitor the action of the interface between CCA and CR 4h: Monitor the action of the interface between CCA and UHCI 5h: Monitor the action of the interface between CCA and SDIO3 6h: Monitor the action of the interface between CCA and SDIO1 7h: Reserved 8h: Monitor the action of the interface between CCA and SDIO2 9h: Monitor the action of the interface between CCA and EHCI Ah: Monitor the action of the interface between CCA and Card Boot (CB) Bh: Monitor the action of the interface between CCA and USBD Ch: Monitor the action of the interface between CCA and SPI Dh-Fh: Reserved
1	RW	0	**CCA Debug Mode Signals Selection** 0: Select group 0 CCA debug signals 1: Select group 1 CCA debug signals
0	RW	0	**Reserved**

Offset Address: 83h (D17F7) – Reserved

Offset Address: 84h (D17F7)

Read Passes Write Control **Default Value: 00h**

Read Passes Write: If this function is disabled, a read cannot be performed before a preceding write has been completed; if this function is enabled, the internal controller is allowed to perform a read before a preceding write.

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**SPI Slave Mode Read Passes Write** 0: Disable 1: Enable
5	RW	0	**Card Reader Read Passes Write** 0: Disable 1: Enable
4	RW	0	**SDIO Read Passes Write** 0: Disable 1: Enable
3	RW	0	**LPC Read Passes Write** 0: Disable 1: Enable
2	RW	0	**IDE Read Passes Write** 0: Disable 1: Enable
1	RW	0	**USB Read Passes Write** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 85-CFh (D17F7) – Reserved

HDAC Control (D0-DFh)

Offset Address: D0h (D17F7) – Reserved

Offset Address: D1h (D17F7)

HDAC and P2P Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Enable the Capability / Status Write of the P2P Bridge Configuration Capability** 0: Disable 1: Enable
2	RW	0	**Disable HDAC** 0: Enable HDAC 1: Disable HDAC
1:0	RW	0	**Reserved**

Offset Address: D2-DFh (D17F7) – Reserved

Dynamic Clock Control (E0-E3h)

Offset Address: E0h (D17F7)

Dynamic Clock Control 1 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**CCA New Dynamic Clock Scheme Enable** 0: Old dynamic clock scheme 1: New dynamic clock scheme
6	RW	1b	**CCA Dynamic Clock On** 0: CCA uses dynamic clock 1: CCA uses free running clock
5	RW	0	**Enable D19F0 Rx0D Latency Timer** Always reads as 0. 0: Disable 1: Enable
4:0	RW	0	**Reserved**

Offset Address: E1h (D17F7) – Reserved

Offset Address: E2h (D17F7)
Dynamic Clock Control 3 **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	1b	**Downstream Interface Clock Control** 0: Dynamic clock scheme 1: Free run
3	RW	1b	**PCI1 Clock Control** 0: Dynamic clock scheme 1: Free run
2	RW	1b	**Downstream HDAC Clock Control** 0: Dynamic clock scheme 1: Free run
1	RW	1b	**Downstream SM Internal PCI Device Clock Control** 0: Dynamic clock scheme 1: Free run
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: E3h (D17F7)
PCI1 Internal 33/66MHz Dynamic Clock Control **Default Value: 6Eh**

Bit	Attribute	Default	Description
7	RW	0	**Improve P2CR Performance** 0: Allocate one cacheline of FIFO for P2CR prefetch. 1: Allocate two cachelines of FIFO for P2CR prefetch. Set 1 when only one PCI master has requested (no pending PCI REQ); otherwise, allocate one cacheline of FIFO for prefetch.
6	RW	1b	**Improve the PCI1 Dynamic Clock** 0: Clock enable until FIFO release. 1: Clock enable until cycle is done. Set this bit for better power saving.
5	RW	1b	**PCI1 33/66MHz Dynamic Clock Control** 0: PCI clock (33/66MHz) is kept ON as long as GRANT# is asserted to PCI device. 1: PCI clock (33/66 MHz) will be gated OFF whenever PCI1 is idle (with or without GRANT# asserted).
4	RW	0	**P2CR Data Timout Enable** Back off PCI Master while not getting TRDY and PCI time out (PCI timer is at Bit [3:1]). 0: Disable 1: Enable
3:1	RW	111b	**P2CR Data Timer (PCI Master TRDY Timeout)** 000: Disable 001: 1*8 PCICLKs 010: 2*8 PCICLKs 011: 3*8 PCICLKs 100: 4*8 PCICLKs 101: 5*8 PCICLKs 110: 6*8 PCICLKs 111: 7*8 PCICLKs
0	RW	0	**Enable P2C Read Backoff Even when Only One PCI Master** It can't retry when only one PCI master and Rx76[6] = 1. (This bit works with Rx70[6] =1.) 0: Not retry when only one PCI Master and bus times out. 1: Retry when bus times out, even though there is only one PCI Master.

DRAM Above 4G Support (E4-FFh)

Offset Address: E4h (D17F7)
Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address [23:20]**
3:0	RW	0	**DRAM Granularity (Powell)** Bits [3:0] / Total DRAM Less than / Granularity 0h / 4G / 16M 1h / 8G / 32M 2h / 16G / 64M 3h / 32G / 128M 4h / 64G / 256M RANK Ending Address Formula: ENDxA[35:24] = RENDxA << Bits [3:0]; (x = 0,1,2,3,4,5,6,7)

Offset Address: E5h (D17F7)
Low Top Address - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Low Top Address [31:24]**

Offset Address: E6h (D17F7)
System Management Mode (SMM) and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxx are passed to PCI1. 1: Cycles accessing to FEC7_FFFF - FEC0_0000 are passed to PCI1. Cycles accessing to FECF_FFFF - FEC8_0000 are passed to PCI2.
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxx from masters are passed to PCI1. (PCIC will not claim). 1: Cycles accessing FEEx_xxxx from masters are passed to the Host side for snooping.
2	RW	0	**Top SMM Enable** 0: Disable 1: Enable
1	RW	0	**High SMM Enable** 0: Disable 1: Enable
0	RW	1b	**Compatible SMM Enable** 0: Disable 1: Enable

Offset Address: E7-FBh (D17F7) – Reserved

Offset Address: FCh (D17F7)
PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Enable CCA Read Clock When The State Machine of MTXCTL Is Not Idle.** 0: Disable 1: Enable
5:0	RW	0	**Reserved**

Offset Address: FD-FFh (D17F7) – Reserved

DEVICE 19 FUNCTION 0 (D19F0): PCI TO PCI BRIDGE

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D19F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D19F0)
Device ID **Default Value: B353h**

Bit	Attribute	Default	Description
15:0	RO	B353h	**Device ID**

Offset Address: 05-04h (D19F0)
PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable error report
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	**Reserved**
3	RO	0	**Respond to Special Cycle** Hardwired to 0.
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RW	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D19F0)
PCI Status — **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RW1C	0	**Detected SERR#** 0: No SERR# error 1: SERR# error occurred
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion**
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-Back as a Target** Reserved
6:0	RO	10h	**Reserved**

Offset Address: 08h (D19F0)
Revision ID — **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D19F0)
Class Code — **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D19F0) – Reserved

Offset Address: 0Dh (D19F0)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer, Reserved** Guarantee time slice for CPU master

Offset Address: 0Eh (D19F0)
Header Type — **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type** 01h indicates the register layout will follow PCI-to-PCI bridge specification.

Offset Address: 0Fh (D19F0)
Built In Self Test (BIST) — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST** Hardwired to 0. (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-17h (D19F0) – Reserved

Offset Address: 18h (D19F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D19F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D19F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D19F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer**

Offset Address: 1Ch (D19F0)
IO Base Address **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**IO Base Address**
3:0	RO	0	**Reserved**

Offset Address: 1Dh (D19F0)
IO Limit Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**IO Limit Address**
3:0	RO	0	**IO Addressing Capability**

Offset Address: 1Eh (D19F0)
Secondary Status Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Fast Back-to-Back Cycle** 0: Not Fast Back-to-Back Cycle 1: Fast Back-to-Back Cycle
6	RO	0	**Reserved**
5	RO	0	**66MHz Capability** 0: 33MHz Capability 1: 66MHz Capability
4:0	RO	0	**Reserved**

Offset Address: 1Fh (D19F0)
Secondary Status Register 2 — **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
6	RW1C	0	**Detected SERR#** 0: No SERR# error 1: SERR# error occurred
5	RO	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
4	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
3	RO	0	**Target-Abort Assertion**
2:1	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 01: Slow 11: Reserved
0	RW1C	0	**Master Data Parity Error** Reserved

Offset Address: 23-20h (D19F0)
Memory Limit and Base — **Default Value: 0000 FFF0h**

Bit	Attribute	Default	Description
31:20	RW	0	**Memory Limit [31:20]**
19:16	RO	0	**Reserved**
15:4	RW	FFFh	**Memory Base [31:20]**
3:0	RO	0	**Reserved**

Offset Address: 27-24h (D19F0)
Prefetchable Memory Limit and Base — **Default Value: 0001 FFF1h**

Bit	Attribute	Default	Description
31:20	RW	0	**Prefetchable Memory Limit [31:20]**
19:16	RO	1h	**Reserved**
15:4	RW	FFFh	**Prefetchable Memory Base [31:20]**
3:0	RO	1h	**Reserved**

Offset Address: 2F-28h (D19F0)
Prefetchable Upper Limit and Base — **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:36	RW	0	**Prefetchable Upper Limit 32 Bits [31:4] (Not Supported)**
35:32	RW	0	**Prefetchable Upper Limit 32 Bits [3:0]**
31:4	RW	0	**Prefetchable Upper Base 32 Bits [31:4] (Not Supported)**
3:0	RW	0	**Prefetchable Upper Base 32 Bits [3:0]**

Offset Address: 33-30h (D19F0)
Upper IO Base and Limit — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Upper IO Limit [15:0]**
15:0	RO	0	**Upper IO Base [15:0]**

Offset Address: 34h (D19F0)
Capability Pointer — **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**Capability Pointer**

Offset Address: 35-3Dh (D19F0) – Reserved

Offset Address: 3F-3Eh (D19F0)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11	RW	0	**Discard Timer SERR# Enable** 0: Disable 1: Enable
10	RW1C	0	**Discard Timer Status** This bit is not set in this chip design. 0: Disable 1: Enable
9	RW	0	**Secondary Discard Timer**
8	RW	0	**Primary Discard Timer**
7	RO	0	**Fast Back-to-Back Enable** 0: Disable 1: Enable
6	RW	0	**Secondary Bus Reset** 0: Disable 1: Enable
5	RW	0	**Master Abort Mode** 0: Disable 1: Enable
4	RW	0	**VGA 16-Bit Decode** 0: Disable 1: Enable
3	RW	0	**VGA Enable** 0: Disable 1: Enable
2	RW	0	**ISA Enable** 0: Disable 1: Enable
1	RW	0	**SERR# Enable** 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Disable 1: Enable

PCI Device-Specific Registers (40-FFh)

Offset Address: 40h (D19F0)

External PCI Device Enable Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Hide AD25 on External PCI Bus when Assert** 0: Disable 1: Enable
5	RW	0	**Hide AD24 on External PCI Bus when Assert** 0: Disable 1: Enable
4	RW	0	**Hide AD23 on External PCI Bus when Assert** 0: Disable 1: Enable
3	RW	0	**Hide AD22 on External PCI Bus when Assert** 0: Disable 1: Enable
2	RW	0	**Hide AD21 on External PCI Bus when Assert** 0: Disable 1: Enable
1	RW	0	**Hide AD20 on External PCI Bus when Assert** 0: Disable 1: Enable
0	RW	0	**Hide AD19 on External PCI Bus when Assert** 0: Disable 1: Enable

Offset Address: 41-6Fh (D19F0) – Reserved

Offset Address: 73-70h (D19F0)

Capability ID and Pointer — **Default Value: 0000 000Dh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RO	0	**Capability Next Pointer**
7:0	RO	0Dh	**Capability ID** 0Dh is the capability ID for "Subsystem ID / Subsystem Vendor ID"

Offset Address: 77-74h (D19F0)

Subsystem ID and Subsystem Vendor ID — **Default Value: 9323 1106h**

Bit	Attribute	Default	Description
31:16	RO	9323h	**Subsystem ID**
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 78-FFh (D19F0) – Reserved

DEVICE 20 FUNCTION 0 (D20F0): HIGH DEFINITION AUDIO CONTROLLER (HDAC)

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D20F0)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D20F0)
Device ID — **Default Value: 3288h**

Bit	Attribute	Default	Description
15:0	RO	3288h	**Device ID**

Offset Address: 05-04h (D20F0)
PCI Command — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9	RO	0	**Fast Back to Back**
8	RO	0	**SERR# Enable**
7	RO	0	**Address Stepping**
6	RO	0	**Parity Error Response**
5	RO	0	**VGA Palette Snooping**
4	RO	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle**
2	RW	0	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Does not respond to memory space access 1: Responds to memory space access
0	RO	0	**I/O Space Access**

Offset Address: 07-06h (D20F0)
PCI Status — **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error**
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master Abort**
12	RO	0	**Received Target Abort**
11	RO	0	**Signaled Target Abort**
10:9	RO	0	**DEVSEL# Timing**
8	RO	0	**Master Data Parity Error**
7	RO	0	**Fast Back-to-Back Capability**
6:5	RO	0	**Reserved**
4	RO	1b	**Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D20F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D20F0)

Class Code **Default Value: 04 0300h**

Bit	Attribute	Default	Description
23:0	RO	040300h	**Class Code**

Offset Address: 0Ch (D20F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D20F0)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D20F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device.

Offset Address: 0Fh (D20F0)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D20F0)

HDAC Lower Base Address **Default Value: 0000 0004h**

Bit	Attribute	Default	Description
31:14	RW	0	**Lower Base Address** 16 KB are required by hardwiring [13:4] to 0.
13:4	RO	0	**Hardwired to 0**
3	RO	0	**Not Prefetchable**
2:1	RO	10b	**Reserved (Do Not Program)**
0	RO	0	**Reserved**

Offset Address: 17-14h (D20F0)

HDAC Upper Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**HDAC Upper Base Address**

Offset Address: 18-2Bh (D20F0) – Reserved

Offset Address: 2D-2Ch (D20F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D20F0)
Subsystem ID **Default Value: 3288h**

Bit	Attribute	Default	Description
15:0	RO	3288h	**Subsystem ID**

Offset Address: 33-30h (D20F0)
Expansion ROM **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Expansion ROM**

Offset Address: 34h (D20F0)
Capability Pointer **Default Value: 50h**

Bit	Attribute	Default	Description
7:0	RO	50h	**Capability Pointer** Points to the power management capability.

Offset Address: 35-3Bh (D20F0) – Reserved

Offset Address: 3Ch (D20F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (D20F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTB#).

Offset Address: 3Eh (D20F0)
Minimum Grant Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Minimum Grant Period** Used to specify how long a burst period is needed.

Offset Address: 3Fh (D20F0)
Maximum Latency **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Latency**

HDAC Device-Specific Configuration (40-FFh)

Offset Address: 40h (D20F0)

Back Door Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Subsystem ID / Subsystem Vender ID Back Door Enable** Specifies whether Rx2C~2F are RO or RW. 0: Read Only 1: Read / Write

Offset Address: 41h (D20F0)

HDAC Control **Default Value: 30h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Reserved**
5	RW	1b	**Reserved (Do Not Program)**
4	RW	1b	**Reserved (Do Not Program)**
3:1	RW	0	**Reserved**
0	RW	0	**HDAC Dynamic Stop** 0: Free running 1:Enable dynamic stop clock

Offset Address: 42-43h (D20F0) – Reserved

Offset Address: 44h (D20F0)

Traffic Class Select **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	000b	**HDAC Traffic Class Assignment** 000b indicates TC0.

Offset Address: 45-4Fh (D20F0) – Reserved

Offset Address: 51-50h (D20F0)

PCI Power Management Capabilities ID **Default Value: 6001h**

Bit	Attribute	Default	Description
15:8	RO	60h	**Next Capability Pointer** Point to the MSI (Message Signaled Interrupt) capability structure
7:0	RO	01h	**PCI Power Management Capability** 01h indicates the linked list item as being the PCI Power Management register.

Offset Address: 53-52h (D20F0)

PCI Power Management Capabilities **Default Value: C842h**

Bit	Attribute	Default	Description
15:11	RO	19h	**PME# Can Be Generated from D3 ~ D0 State** Indicates the power states in which the function may assert PME#. Bit-15: PME# can be asserted from D3 cold Bit-14: PME# can be asserted from D3 hot Bit-13: PME# can be asserted from D2 Bit-12: PME# can be asserted from D1 Bit-11: PME# can be asserted from D0
10	RO	0	**D2 State Supported** 0: Not supported 1: Supported
9	RO	0	**D1 State Supported** 0: Not supported 1: Supported
8:6	RO	001b	**Report D3 Max Suspend Current** Reports the 3.3V auxiliary current requirements for the PCI function. 000: 0 mA 001: 55 mA 010: 100 mA 011: 160 mA 100: 220 mA 101: 270 mA 110: 320 mA 111: 375 mA
5	RO	0	**Device-Specific Initialization Requirement** 0: Not required 1: Required
4	RO	0	**Reserved**
3	RO	0	**Hardwired to 0**
2:0	RO	010b	**PCI Power Support** 010b indicates that this function complies with the PCI Power Management Interface specification version 1.1.

Offset Address: 57-54h (B0D20F0)

Power Management Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Hardwired to 0**
21:16	RO	0	**Reserved**
15	RW1C	0	**PME Status** This bit is set when the HDAC would assert the PME# independent of the state of the bit 8. This bit is in resume well.
14:9	RO	0	**Reserved**
8	RWS	0	**PME Enable** Enable PME wake up if bit 15 is set. This bit is in resume well.
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** This field is used both to determinate the current power state and to set a new power state. 00: D0 01: D1 10: D2 11: D3 If software attempts to write a value of 10b or 01b into this field, the write operation will complete normally; however, no state change will occur.

Offset Address: 58-5Fh (D20F0) – Reserved

Offset Address: 61-60h (D20F0)

MSI Capability ID **Default Value: 7005h**

Bit	Attribute	Default	Description
15:8	RO	70h	**Next Capability Pointer** Point to the PCI Express capability structure
7:0	RO	05h	**MSI Capability**

Offset Address: 63-62h (D20F0)
MSI Message Control — **Default Value: 0080h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RO	1b	**64-Bit Address Capability** 0: 32-bit 1: 64-bit
6:4	RO	0	**Multiple Message Enable** Normally these are RW bits, but software will always read 000b to indicate only 1 message is supported.
3:1	RO	0	**Multiple Message Capable** 0 indicates the number of requested vector is 1.
0	RW	0	**MSI Enable** 0: Assert INTx instead of MSI. 1: MSI will be generated instead of INTx assertion.

Offset Address: 67-64h (D20F0)
MSI Message Lower Address — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Message Lower Address**
1:0	RO	0	**Reserved**

Offset Address: 6B-68h (D20F0)
MSI Message Upper Address — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Message Upper Address**

Offset Address: 6D-6Ch (D20F0)
MSI Data — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Data Used for MSI Message**

Offset Address: 6E-6Fh (D20F0) – Reserved

Offset Address: 71-70h (D20F0)
PCI Express Capability ID — **Default Value: 0010h**

Bit	Attribute	Default	Description
15:8	RO	0	**Capability Link** This is the last capability structure of the list.
7:0	RO	10h	**PCI Express Capability**

Offset Address: 73-72h (D20F0)
PCI Express Capability **Default Value: 0091h**

Bit	Attribute	Default	Description
15:8	RO	0	**Hardwired to 0**
7:0	RO	91h	**Capability Version #1** ***Bits [7:4]:*** **Device / Port Type** 0000: PCI Express Endpoint device 0001: Legacy PCI Express Endpoint device 0100: Root Port of PCI Express Root Complex 0101: Upstream Port of PCI Express Switch 0110: Downstream Port of PCI Express Switch 0111: PCI Express -_to-_PCI/PCI-X Bridge 1000: PCI/PCI-X to PCI Express Bridge 1001: Root Complex Integrated Endpoint Device 1010: Root Complex Event Collector ***Bits [3:0]:*** **Capability Version**

Offset Address: 77-74h (D20F0)
Device Capabilities **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Device Capabilities** Hardwired to 0.

Offset Address: 79-78h (D20F0)
Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	0	**Hardwired to 0**
11	RO	0	**Snoop**
10:0	RO	0	**Hardwired to 0**

Offset Address: 7B-7Ah (D20F0)
Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transaction Pending** 0: All non-posted requests have been executed. 1: Some non-posted requests are still pending.
4	RO	1b	**AUX Power Detected** Hardwired to 1b.
3:0	RO	0	**Hardwired to 0**

Offset Address: 7C-FFh (D20F0) – Reserved

HDAC PCI Extended Configuration Space

HDAC PCI Extended Configuration (100-260h)

Offset Address: 103-100h (D20F0)
Virtual Channel Enhanced Capability — **Default Value: 1301 0002h**

Bit	Attribute	Default	Description
31:20	RO	130h	**Next Capability Pointer** Hardwired to 130h.
19:16	RO	1h	**Capability Structure Revision** This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Hardwired to 1h to indicate PCIe version 1.1.
15:0	RO	0002h	**Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. Hardwired to 0002h to indicate the virtual channel capability.

Offset Address: 107-104h (D20F0)
Port VC Capability 1 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:3	RO	0	**Hardwired to 0**
2:0	RO	0	**Hardwired to 0** Indicates that one extended VC is supported by the controller.

Offset Address: 10B-108h (D20F0)
Port VC Capability 2 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Hardwired to 0** Indicates that a VC arbitration table is not present.
23:8	RO	0	**Reserved**
7:0	RO	0	**Hardwired to 0**

Offset Address: 10D-10Ch (D20F0)
Port VC Control — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Port VC Control** Reserved.

Offset Address: 10F-10Eh (D20F0)
Port VC Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**Hardwired to 0** Indicates that VC arbitration table is not present.

Offset Address: 113-110h (D20F0)
VC0 Resource Capability — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Hardwired to 0** This field is not valid for endpoint devices.

Offset Address: 117-114h (D20F0)
VC0 Resource Control **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC0 Enable** Hardwired to 1 for VC0.
30:27	RO	0	**Reserved**
26:24	RO	0	**VC0 ID** Hardwired to 0 since this field is assigned to VC0.
23:20	RO	0	**Reserved**
19:16	RO	0	**Hardwired to 0**
15:8	RO	0	**Reserved**
7:1	RW	7Fh	**TC/VC0 Map** Bits [7:1] are implemented as RW bits.
0	RO	1b	**TC/VC0 Map** Hardwired to 1b since TC0 is always mapped to VC0.

Offset Address: 118-119h (D20F0) – Reserved

Offset Address: 11B-11Ah (D20F0)
VC0 Resource Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1	RO	0	**Hardwired to 0** This bit is not applied to integrated device.
0	RO	0	**Hardwired to 0** This bit is not valid for endpoint devices.

Offset Address: 11C-12Fh (D20F0) – Reserved

Offset Address: 133-130h (D20F0)
Root Complex Link Declaration Enhanced Capability Header Register **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:16	RO	0001h	**Next Capability** Hardwired to 0001h.
15:0	RO	0005h	**PCI Express Extended Capability ID** Hardwired to 0005h.

Offset Address: 137-134h (D20F0)
Element Self Description **Default Value: 0401 0100h**

Bit	Attribute	Default	Description
31:24	RO	04h	**Port Number** 04h indicates HDAC controller is assigned as port #5.
23:16	RO	01h	**Component ID**
15:8	RO	01h	**Number of Link Entries** Hardwired to 01h.
7:4	RO	0	**Reserved**
3:0	RO	0	**Element Type** The HDAC controller is an integrated root complex device, and this field reports a value of 0h.

Offset Address: 138-13Fh (D20F0) – Reserved

Offset Address: 143-140h (D20F0)

Link Description **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Target Port Number** Hardwired to 00h.
23:16	RO	01h	**Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Indicates that the link points to RCRB.
0	RO	1b	**Link Valid**

Offset Address: 144-147h (D20F0) – Reserved

Offset Address: 14B-148h (D20F0)

Link Lower Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Link Lower Address** (RCRBH Memory Address)
11:0	RO	0	**Reserved** Always reads 0.

Offset Address: 14F-14Ch (D20F0)

Link Upper Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved** Always reads 0.
3:0	RO	0	**Link Upper Address**. (RCRBH Memory Address)

Offset Address: 150-260h (D20F0) – Reserved

High Definition Audio Controller Memory Mapped I/O Space (HDAC-MMIO)

This section describes the memory mapped HDAC registers. Please refer to High Definition Audio Specification 1.0 for details.

Global Capabilities and Control (00-1Bh)

Offset Address: 01-00h (HDAC-MMIO)

Global Capabilities – GCAP **Default Value: 4401h**

Bit	Attribute	Default	Description
15:12	RO	4h	**Number of Output Streams Supported** 0h: No output streams supported. 1h: 1 output streams supported. 2h: 2 output streams supported. Fh: 15 output streams supported.
11:8	RO	4h	**Number of Input Streams Supported** 0h: No input streams supported. 1h: 1 input streams supported. 2h: 2 input streams supported. Fh: 15 input streams supported.
7:3	RO	0	**Number of Bidirectional Streams Supported** 0h: No bidirectional stream supported. 1h: 1 bidirectional stream supported. 2h: 2 bidirectional streams supported. 1Eh: 30 bidirectional streams supported.
2	RO	0	**Reserved**
1	RO	0	**Number of Serial Data Out Signals** 0: 1 SDOUT line is supported. 1: 2 SDOUTs are supported.
0	RO	1b	**64-Bit Address Supported** 0: Only 32-bit addressing is available. 1: 64-bit addressing is supported.

Offset Address: 03-02h (HDAC-MMIO)

Version Number **Default Value: 0100h**

Bit	Attribute	Default	Description
15:8	RO	01h	**Major Version**
7:0	RO	0	**Minor Version**

The version number “0100h” indicates this chip complies with High Definition Audio Specification Rev 1.0.

Offset Address: 07-04h (HDAC-MMIO)

Payload Capability **Default Value: 001D 003Ch**

Bit	Attribute	Default	Description
31:16	RO	001Dh	**Input Payload Capability** 001Dh indicates 29-word payload (464 bits). Note: This does not include bandwidth used for command and control.
15:0	RO	003Ch	**Output Payload Capability** 003Ch indicates 60-word payload (960 bits). It indicates the total output payload available on the link is 60 word (960 bits).

Offset Address: 0B-08h (HDAC-MMIO)
Global Control – GCTL **Default Value: 0000 000nh**

Bit	Attribute	Default	Description
31:9	RO	0	**Reserved**
8	RW	0	**Accept Unsolicited Response Enable** 0: Unsolicited responses from codec are not accepted. 1: Unsolicited responses from codec are accepted by the controller.
7:2	RO	0	**Reserved**
1	RW	0	**Flush Control** Writing a 1 to this bit initiates a flush.
0	RWS	HwInit	**Controller Reset** For read: 0: In reset state. 1: Controller is ready for operations. For write: 0: Reset the controller. 1: Write 1 causes the controller exit its reset state and de-assert link AZRST#.

Offset Address: 0D-0Ch (HDAC-MMIO)
Wake Enable – WAKEEN **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1:0	RW	0	**AZSDIN Wake Enable Flags** 0: Not allow the associated AZSDIN signal to generate a wake or processor interrupt. 1: Allow the associated AZSDIN signal to generate a wake or processor interrupt. The bit[i] corresponds to AZSDIN[i] signal.

Offset Address: 0F-0Eh (HDAC-MMIO)
AZSDIN State Change Status – STATESTS **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1:0	RW1CS	0	**AZSDIN State Change Status Flags** 0: No state change 1: The associated AZSDIN signal received a "State Change" event. The bit[i] corresponds to AZSDIN[i] signal.

Offset Address: 11-10h (HDAC-MMIO)
Global Status – GSTS **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1	RW1C	0	**Flush Status** 0: No flush cycle completed 1: Flush cycle completed This bit is set to 1 by the hardware to indicate that the flush cycle initiated by the Rx08[1] has completed. Software must write 1 to clear this bit before the next time Rx08[1] is set.
0	RO	0	**Reserved**

Offset Address: 12-17h (HDAC-MMIO) – Reserved

Offset Address: 1B-18h (HDAC-MMIO)
Stream Payload Capability **Default Value: 001D 003Ch**

Bit	Attribute	Default	Description
31:16	RO	001Dh	**Input Stream Payload Capability** 001Dh indicates 29-word payload (464 bits).
15:0	RO	003Ch	**Output Stream Payload Capability** 003Ch indicates 60-word payload (960 bits).

Offset Address: 1C-1Fh (HDAC-MMIO) – Reserved

Interrupt Control (20-27h)

Offset Address: 23-20h (HDAC-MMIO)
Interrupt Control – INTCTL **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Global Interrupt Enable** 0: Disable 1: Enable device interrupt generation
30	RW	0	**Controller Interrupt Enable** 0: Disable 1: Enable controller's general interrupt. When set to 1, the controller generates an interrupt when the corresponding status bit is set due to a response interrupt, a response buffer overrun, and wake events.
29:8	RO	0	**Reserved**
7:4	RW	0	**Stream Interrupt Enable – for Output Stream [3:0]** 0: Disable 1: Enable
3:0	RW	0	**Stream Interrupt Enable – for Input Stream [3:0]** 0: Disable 1: Enable

Offset Address: 27-24h (HDAC-MMIO)
Interrupt Status – INTSTS **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Global Interrupt Status** This bit is set when one of the interrupt status bits is set. 0: No interrupt occurred 1: Some interrupt(s) occurred
30	RW1C	0	**Controller Interrupt Status** 0: No interrupt occurred 1: Some interrupt(s) occurred A 1 indicates that an interrupt condition occurred due to a response interrupt, a response overrun, or a codec state change request. The exact cause can be determined by interrogating the RIRB status register and the state change status register.
29:8	RO	0	**Reserved**
7:4	RW1C	0	**Stream Interrupt Status – for Output Stream [3:0]** 0: No interrupt occurred 1: Interrupt occurred
3:0	RW1C	0	**Stream Interrupt Status – for Input Stream [3:0]** 0: No interrupt occurred 1: Interrupt occurred

Offset Address: 28-2Fh (HDAC-MMIO) – Reserved

Synchronization Control (30-3Bh)

Offset Address: 33-30h (HDAC-MMIO)
Wall Clock Counter **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Wall Clock Counter** 32 bits counter that is incremented at the link bitclk rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds.

Offset Address: 34-37h (HDAC-MMIO) – Reserved

Offset Address: 3B-38h (HDAC-MMIO)

Stream Synchronization – SSYNC **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:4	RW	0	**Stream Synchronization Bits – for Output Stream [3:0]** 0: Do not block data. 1: Stop in sending data to the link.
3:0	RW	0	**Stream Synchronization Bits – for Input Stream [3:0]** 0: Do not block data. 1: Stop in receiving data from the link.

Offset Address: 3C-3Fh (HDAC-MMIO) – Reserved

HDAC CORB (Command Output Ring Buffer) Control (40-4Eh)

Offset Address: 43-40h (HDAC-MMIO)

CORB Lower Base Address – CORBLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	**CORB Lower Base Address** Lower address of the Command Output Ring Buffer.
6:0	RO	0	**Reserved** Hardwired to 0 for alignment to 128-byte boundary.

Offset Address: 47-44h (HDAC-MMIO)

CORB Upper Base Address – CORBUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**CORB Upper Base Address** Upper 32 bits of address of the Command Output Ring Buffer.

Offset Address: 49-48h (HDAC-MMIO)

CORB Write Pointer **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	0	**CORB Write Pointer** Software writes the last valid CORB entry offset into this field in DW granularity. The DMA engine fetches commands from the CORB until the read point matches the write pointer. The field may be written while the DMA engine is running.

Offset Address: 4B-4Ah (HDAC-MMIO)

CORB Read Pointer **Default Value: 0000h**

Bit	Attribute	Default	Description
15	WO	0	**CORB Read Pointer Reset** Writes a 1 to reset the CORB Read Pointer to 0. DMA engine must be stopped prior to resetting the read pointer or DMA transfer may be corrupted. This bit is always read 0.
14:8	RO	0	**Reserved**
7:0	RO	0	**CORB Read Pointer** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB read pointer offset in DW granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports up to 256 CORB entries (256*4B = 1KB) in the cyclic buffer.

Offset Address: 4Ch (HDAC-MMIO)
CORB Control – CORBCTL **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Enable CORB DMA Engine** 0: DMA stop 1: DMA run (when read pointer lags write pointer). Software must read the value back.
0	RW	0	**CORB Memory Error Interrupt Enable** 0: Disable 1: Enable. The controller will generate an interrupt when Rx4D[0] is set to 1.

Offset Address: 4Dh (HDAC-MMIO)
CORB Status – CORBSTS **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW1C	0	**CORB Memory Error Indication** 0: No error. 1: Error detected. The controller has detected an error in the pathway between the controller and memory. An interrupt is asserted if Rx4C[0] is set to 1.

Offset Address: 4Eh (HDAC-MMIO)
CORB Size – CORBSIZE **Default Value: 42h**

Bit	Attribute	Default	Description
7:4	RO	4h	**CORB Size Capability** 4h indicates 256 entries (1 KB).
3:2	RO	0	**Reserved**
1:0	RO	10b	**CORB Size** 00: 2 entries (8 bytes) 01: 16 entries (64 bytes) 10: 256 entries (1 KB) 11: Reserved

Offset Address: 4Fh (HDAC-MMIO) – Reserved

HDAC RIRB (Response Input Ring Buffer) Control (50-5Eh)

Offset Address: 53-50h (HDAC-MMIO)
RIRB Lower Base Address – RIRBLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	**RIRB Lower Base Address** Lower address of the Response Input Ring Buffer.
6:0	RO	0	**Reserved** Hardwired to 0 for alignment to 128-byte boundary.

Offset Address: 57-54h (HDAC-MMIO)
RIRB Upper Base Address – RIRBUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**RIRB Upper Base Address** Upper 32 bits of address of the Response Input Output Ring Buffer.

Offset Address: 59-58h (HDAC-MMIO)

RIRB Write Pointer – RIRBWP **Default Value: 0000h**

Bit	Attribute	Default	Description
15	WO	0	**RIRB Write Pointer Reset** Writes 1 to reset the RIRB Write Pointer to 0. The DMA engine must be stopped prior to resetting the write pointer or DMA transfer may be corrupted. This bit is always read as 0.
14:8	RO	0	**Reserved**
7:0	RO	0	**RIRB Write Pointer** This register indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB write pointer offset in 2 DW units. Up to 256 RIRB entries in the cyclic buffer is supported.

Offset Address: 5B-5Ah (HDAC-MMIO)

Response Interrupt Count – RINTCNT **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	00h	**Response Interrupt Count – N Response** 00h: 256 responses 01h to FFh: 1 to 255 responses The DMA engine should be stopped when changing this field or else an interrupt may be lost.

Offset Address: 5Ch (HDAC-MMIO)

RIRB Control – RIRBCTL **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Response Overrun Interrupt Control** 0: Disable 1: Enable
1	RW	0	**Enable RIRB DMA Engine** 0: DMA stop 1: DMA run (when response queue is not empty).
0	RW	0	**Response Interrupt Control** 0: Disable 1: Enable. Generate an interrupt after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx input after a frame which returned a response. The N counter is reset when the interrupt is generated.

Offset Address: 5Dh (HDAC-MMIO)

RIRB Status – RIRBSTS **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW1C	0	**Response Overrun Interrupt Status** Hardware sets this bit to 1 when an overrun occurs in the RIRB. An interrupt may be generated if the response overrun interrupt control bit is set. 0: No overrun 1: Overrun occurred
1	RO	0	**Reserved**
0	RW1C	0	**Response Interrupt** Hardware sets this bit to 1 when an interrupt has been generated after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx inputs. 0: No response interrupt 1: Response interrupt occurred

Offset Address: 5Eh (HDAC-MMIO)

RIRB Size – RIRBSIZE **Default Value: 42h**

Bit	Attribute	Default	Description
7:4	RO	0100b	**RIRB Size Capability** 0100b indicates 256 entries (2 KB).
3:2	RO	0	**Reserved**
1:0	RO	10b	**RIRB Size** 00: 2 entries (16 bytes) 01: 16 entries (128 bytes) 10: 256 entries (2 KB) 11: Reserved

Offset Address: 5Fh (HDAC-MMIO) – Reserved

HDAC Immediate Command Control (60-69h)

Offset Address: 63-60h (HDAC-MMIO)
Immediate Command Input / Output Interface **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	**Immediate Command Write** The written value will be sent out over the link in the next available frame. Reads always return 0's. Software must ensure that the ICB bit (bit-0) in the Immediate Command Status register is cleared before writing a value into this register or undefined behavior will result.

Offset Address: 67-64h (HDAC-MMIO)
Immediate Response Input Interface **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Immediate Response Read** Reads return the last response came over the link.

Offset Address: 69-68h (HDAC-MMIO)
Immediate Command Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:4	RO	0	**Immediate Response Result Address** This is the address of the codec which sent the response currently been latched in the Immediate Response Input register.
3	RO	0	**Immediate Response Result Unsolicited** This bit indicates whether the response latched in the Immediate Response Input register is solicited or unsolicited. 0: A solicited response latched 1: An unsolicited response latched
2	RO	0	**Immediate Command Version** This bit is corresponding to Rx40[4]. 0: Bits [7:4] and bit 3 are reserved. 1: Both bits [7:4] and bit 3 are implemented.
1	RW1C	0	**Immediate Result Valid** This bit is set to 1 by hardware when a new response has been received. 0: No new response 1: A new response arrived
0	RO	0	**Immediate Command Busy** 0: Ready for accepting an immediate command. 1: Not ready. Software must wait until this bit becomes 0 before writing a value in Rx63-60. Before codec initialization finishes, this bit is 1.

Offset Address: 6A-6Fh (HDAC-MMIO) – Reserved

DMA Position Base Address (70-77h)

Offset Address: 73-70h (HDAC-MMIO)
DMA Position Lower Base Address – DPLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	**DMA Position Lower Base Address**
6:1	RO	0	**DMA Position Lower Base Unimplemented Bits** Hardwired to 0.
0	RW	0	**DMA Position Buffer Enable** 0: Disable 1: Enable

Offset Address: 77-74h (HDAC-MMIO)
DMA Position Upper Base Address – DPUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**DMA Position Upper Base Address** Upper 32 bits of address of the DMA Position Buffer Base Address.

Offset Address: 78-7Fh (HDAC-MMIO) – Reserved

HDAC Stream Descriptors (80-17Fh)

HDAC Stream Descriptor Control **Default Value: 00 0000h**

Offset Address: 82-80h (HDAC-MMIO) – Input Stream 0
Offset Address: A2-A0h (HDAC-MMIO) – Input Stream 1
Offset Address: C2-C0h (HDAC-MMIO) – Input Stream 2
Offset Address: E2-E0h (HDAC-MMIO) – Input Stream 3
Offset Address: 102-100h (HDAC-MMIO) – Output Stream 0
Offset Address: 122-120h (HDAC-MMIO) – Output Stream 1
Offset Address: 142-140h (HDAC-MMIO) – Output Stream 2
Offset Address: 162-160h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
23:20	RW	0h	**Stream ID** A tag corresponds to the transferred data on the link. 0h: Unused 1h to 0Fh: Stream 1 to 15
19	RO	0	**Bidirectional Direction Control** Hardwired to 0. Bidirectional engine is not supported.
18	RW	0	**Traffic Priority** Hardwired to 0. The traffic will be handled on a best effort basis. 0: Handles on a “best effort” basis 1: Handles as preferred traffic
17:16	RO	00b	**Stripe Control** Hardwired to 0 indicating that the controller supports 1 SDO line. 00: 1 SDO 01: 2 SDOs 10: 4 SDOs 11: Reserved (Read Only for input streams)
15:5	RO	0	**Reserved**
4	RW	0	**Descriptor Error Interrupt Enable** Controls whether an interrupt is generated when the descriptor error status bit is set. 0: Disable 1: Enable
3	RW	0	**FIFO Error Interrupt Enable** Controls whether an interrupt is generated when FIFO error (underrun/overrun) occurs. 0: Disable 1: Enable
2	RW	0	**Interrupt On Completion Enable** Controls whether an interrupt occurs when a buffer completion with the IOC bit set in its descriptor. 0: Disable 1: Enable.
1	RW	0	**Stream Run** 0: DMA disable. The DMA engine associated with this input stream will be disabled. If the corresponding Rx38 (SSYNC) bit is 0, input stream data will be taken from the link and moved to the FIFO and an overrun may occurs. 1: DMA enable. The DMA engine associated with this input stream is enabled to transfer data in the FIFO to main memory.
0	RW	0	**Stream Reset** For read: 0: Ready (not in reset state) 1: In reset state For write: 0: Exit reset 1: Reset the steam Write a 1 causes the corresponding stream to be reset. The stream descriptor registers (except this bit), FIFOs, and cadence generator for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to being operation, it will report 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The run bit must be cleared before SRST is asserted.

HDAC Stream Descriptor Status **Default Value: 00h**

Offset Address: 83h (HDAC-MMIO) – Input Stream 0
Offset Address: A3h (HDAC-MMIO) – Input Stream 1
Offset Address: C3h (HDAC-MMIO) – Input Stream 2
Offset Address: E3h (HDAC-MMIO) – Input Stream 3
Offset Address: 103h (HDAC-MMIO) – Output Stream 0
Offset Address: 123h (HDAC-MMIO) – Output Stream 1
Offset Address: 143h (HDAC-MMIO) – Output Stream 2
Offset Address: 163h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**FIFO Ready** ***For an output stream:*** 0: Not enough data for transferring. 1: The output DMA FIFO contains enough data to maintain the output stream on the link. This bit default to 0 on reset because the FIFO is cleared on a reset. ***For an input stream:*** This bit is not meaningful for an input stream. Therefore, it is always read 0 for input stream.
4	RW1C	0	**Descriptor Error** 0: No error 1: Error occurred during the fetch of a descriptor - something bad happened. This could be a result of a master abort, a parity error, or ECC error on the bus, or any other error which renders the current buffer descriptor or BDL list useless.
3	RW1C	0	**FIFO Error** For an input stream, it indicates a FIFO overrun occurred while run bit is set. For an output stream, it indicates a FIFO underrrun occurred while there are still buffers to send. 0: No error 1: Error occurred
2	RW1C	0	**Buffer Completion Interrupt Status** 0: Not completed 1: Buffer operation completed This bit is set to 1 by the controller after the last sample of a buffer has been processed and the interrupt on completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit.
1:0	RO	0	**Reserved**

HDAC Stream Descriptor Link Position in Buffer **Default Value: 0000 0000h**

Offset Address: 87-84h (HDAC-MMIO) – Input Stream 0
Offset Address: A7-A4h (HDAC-MMIO) – Input Stream 1
Offset Address: C7-C4h (HDAC-MMIO) – Input Stream 2
Offset Address: E7-E4h (HDAC-MMIO) – Input Stream 3
Offset Address: 107-104h (HDAC-MMIO) – Output Stream 0
Offset Address: 127-124h (HDAC-MMIO) – Output Stream 1
Offset Address: 147-144h (HDAC-MMIO) –Output Stream 2
Offset Address: 167-164h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RO	0	**Link Position in Buffer** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the cyclic buffer length register and then wrap to 0.

HDAC Stream Descriptor Cyclic Buffer Length **Default Value: 0000 0000h**

Offset Address: 8B-88h (HDAC-MMIO) – Input Stream 0
Offset Address: AB-A8h (HDAC-MMIO) – Input Stream 1
Offset Address: CB-C8h (HDAC-MMIO) – Input Stream 2
Offset Address: EB-E8h (HDAC-MMIO) – Input Stream 3
Offset Address: 10B-108h (HDAC-MMIO) – Output Stream 0
Offset Address: 12B-128h (HDAC-MMIO) – Output Stream 1
Offset Address: 14B-148h (HDAC-MMIO) – Output Stream 2
Offset Address: 16B-168h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RW	0	**Cyclic Buffer Length** Indicates the number of bytes in the cyclic buffer. Link position in buffer will be reset when it reaches this value.

HDAC Stream Descriptor Last Valid Index (HDAC-MMIO) **Default Value: 0000h**

Offset Address: 8D-8Ch (HDAC-MMIO) – Input Stream 0
Offset Address: AD-ACh (HDAC-MMIO) – Input Stream 1
Offset Address: CD-CCh (HDAC-MMIO) – Input Stream 2
Offset Address: ED-ECh (HDAC-MMIO) – Input Stream 3
Offset Address: 10D-10Ch (HDAC-MMIO) – Output Stream 0
Offset Address: 12D-12Ch (HDAC-MMIO) – Output Stream 1
Offset Address: 14D-14Ch (HDAC-MMIO) – Output Stream 2
Offset Address: 16D-16Ch (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	0	**Last Valid Index** The value written to this register indicates the index for the last valid buffer descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list on continue processing. This register must be at least 1.

Offset Address: 8E-8Fh (HDAC-MMIO) – Reserved

HDAC Input Stream Descriptor FIFO Size **Default Value: 0060h**

Offset Address: 91-90h (HDAC-MMIO) – Input Stream 0
Offset Address: B1-B0h (HDAC-MMIO) –Input Stream 1
Offset Address: D1-D0h (HDAC-MMIO) – Input Stream 2
Offset Address: F1-F0h (HDAC-MMIO) – Input Stream 3

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RO	60h	**FIFO Size** The max number of bytes that can be fetched by the controller at one time.

HDAC Output Stream Descriptor FIFO Size **Default Value: 00C0h**

Offset Address: 111-110h (HDAC-MMIO) – Output Stream 0
Offset Address: 131-130h (HDAC-MMIO) – Output Stream 1
Offset Address: 151-150h (HDAC-MMIO) – Output Stream 2
Offset Address: 171-170h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8:0	RO	0C0h	**FIFO Size** The max number of bytes that can be fetched by the controller at one time. Note: Bit 8 can *only* be modified together with [7:0].

HDAC Stream Descriptor Format **Default Value: 0000h**

Offset Address: 93-92h (HDAC-MMIO) – Input Stream 0
Offset Address: B3-B2h (HDAC-MMIO) – Input Stream 1
Offset Address: D3-D2h (HDAC-MMIO) – Input Stream 2
Offset Address: F3-F2h (HDAC-MMIO) – Input Stream 3
Offset Address: 113-112h (HDAC-MMIO) – Output Stream 0
Offset Address: 133-132h (HDAC-MMIO) – Output Stream 1
Offset Address: 153-152h (HDAC-MMIO) – Output Stream 2
Offset Address: 173-172h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RW	0	**Sample Base Rate** 0: 48 KHz 1: 44.1 KHz
13:11	RW	000b	**Sample Base Rate Multiple** 000: x1 001: x2 010: x3 011: x4 Others: Reserved
10:8	RW	000b	**Sample Base Rate Divisor** 000 to 111: the actual sample rate divisor is DIV + 1 000: divide by 1 (48 KHz, 44.1 KHz) 001: divide by 2 (24 KHz, 22.05 KHz) 010: divide by 3 (16 KHz, 32 KHz) …
7	RO	0	**Reserved**
6:4	RW	000b	**Bits per Sample** 000: 8 bits, packed in memory in 8-bit containers on 16-bit boundary. 001: 16 bits, packed in memory in 8-bit containers on 16-bit boundary. 010: 20 bits, packed in memory in 8-bit containers on 16-bit boundary. 011: 24 bits, packed in memory in 8-bit containers on 16-bit boundary. 100: 32 bits, packed in memory in 8-bit containers on 16-bit boundary. Others: Reserved.
3:0	RW	0	**Number of Channels** 0000 to 1111: 1 to 16 channels

Offset Address: 94-97h (HDAC-MMIO) – Reserved

HDAC Stream Descriptor BDL Pointer Lower Base Address **Default Value: 0000 0000h**

Offset Address: 9B-98h (HDAC-MMIO) – Input Stream 0
Offset Address: BB-B8h (HDAC-MMIO) – Input Stream 1
Offset Address: DB-D8h (HDAC-MMIO) – Input Stream 2
Offset Address: FB-F8h (HDAC-MMIO) – Input Stream 3
Offset Address: 11B-118h (HDAC-MMIO) – Output Stream 0
Offset Address: 13B-138h (HDAC-MMIO) – Output Stream 1
Offset Address: 15B-158h (HDAC-MMIO) – Output Stream 2
Offset Address: 17B-178h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:7	RW	0	**Buffer Descriptor List Lower Base Address**
6:0	RO	0	**Unimplemented Bits** Hardwired to 0 for alignment to 128-byte boundary.

Stream Descriptor BDL Pointer Upper Base Address **Default Value: 0000 0000h**

Offset Address: 9F-9Ch (HDAC-MMIO) –Input Stream 0
Offset Address: BF-BCh (HDAC-MMIO) – Input Stream 1
Offset Address: DF-DCh (HDAC-MMIO) – Input Stream 2
Offset Address: FF-FCh (HDAC-MMIO) – Input Stream 3
Offset Address: 11F-11Ch (HDAC-MMIO) – Output Stream 0
Offset Address: 13F-13Ch (HDAC-MMIO) – Output Stream 1
Offset Address: 15F-15Ch (HDAC-MMIO) – Output Stream 2
Offset Address: 17F-17Ch (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RW	0	**Buffer Descriptor List Upper Base Address**

Offset Address: AE-177h (HDAC-MMIO) – Reserved

Offset Address: 180-202Fh (HDAC-MMIO) - Reserved

Alias Registers (2030-2167h)

Offset Address: 2033-2030h (HDAC-MMIO)
Wall Clock Counter Alias – WALCLKA **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Wall Clock Counter Alias**

Offset Address: 2034-2083h (HDAC-MMIO) - Reserved

HDAC Stream Descriptor Link Position in Buffer Alias **Default Value: 0000 0000h**

Offset Address: 2087-2084h (HDAC-MMIO) – Input Stream 0
Offset Address: 20A7-20A4h (HDAC-MMIO) – Input Stream 1
Offset Address: 20C7-20C4h (HDAC-MMIO) – Input Stream 2
Offset Address: 20E7-20E4h (HDAC-MMIO) – Input Stream 3
Offset Address: 2107-2104h (HDAC-MMIO) – Output Stream 0
Offset Address: 2127-2124h (HDAC-MMIO) – Output Stream 1
Offset Address: 2147-2144h (HDAC-MMIO) – Output Stream 2
Offset Address: 2167-2164h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RO	0	**Link Position in Buffer Alias** An alias of the link position in buffer register for each stream descriptor.

Offset Address: 2088-2163h (HDAC-MMIO) – Reserved