FEATURES

- 100% PC/AT Compatible.

- Up to 25 MHz Performance.

- ISA Bus Control Logic.

  - Synchronous or Asynchronous System Control Operation.
  - Programmable Command Delays.
  - Numerical Co-processor Support.
  - Programmable Wait States for Local and Off-board Cycles.
  - Fast Gate A20 and Fast Reset.
  - IOCHRDY Timeout.

- Memory Control Logic

  - Enhanced Page Mode/2-Way Word and Multi-Page Interleave.
  - Supports up to 64M bytes of On-Board Memory.
  - Shadow RAM Feature for System, Video, LAN BIOS.
  - Can use 4M, 1M and 256K DRAMs or a mix.
  - Staggered RAS Refresh.

- Programmable Memory Options

  - User Selectable 8 or 16 bit ROM with Selectable wait states.
  - Selectable Hit (0-3) and Miss (1-4) wait states for DRAM access.
  - Mapping of Logical Banks to Physical Banks.
  - 512 X 512 Split.
  - Disable (On Board) Memory to 0K in 128K Resolution.
  - Memory Backfill.
  - EMS LIM 4.0 Mapping Registers
    - Up to 4 Sets of 4 Registers
    - Each Set Maps 64K Boundry
    - Each Register Maps 16K anywhere above 1M Memory

- Testability Features.

- Advanced, Low Power CMOS Technology for Laptops.

- 160 Pin Flatpack.
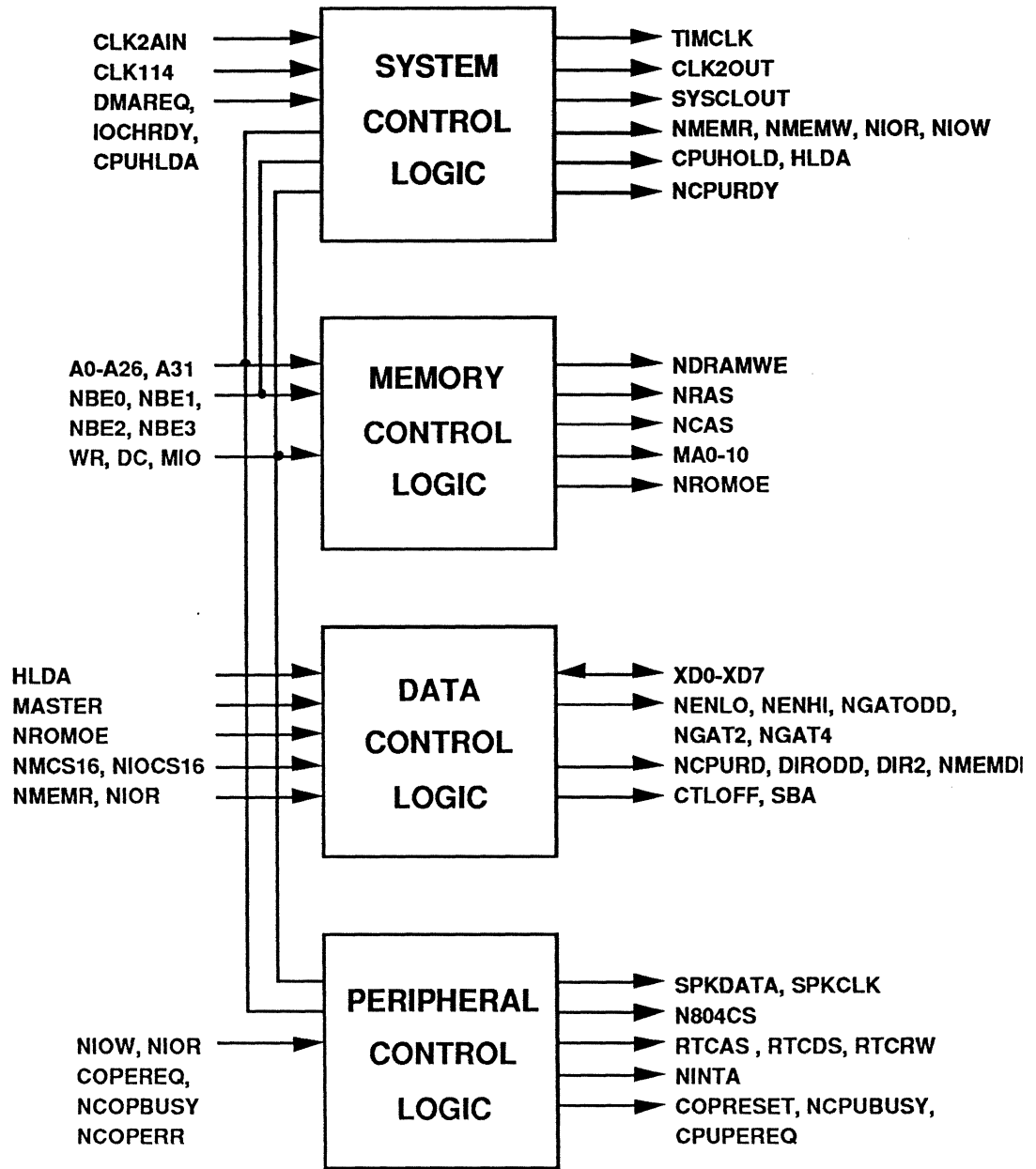
BLOCK DIAGRAM SL9352

Fig. 1 Functional Block Diagram

I. DESCRIPTION

VIA's System and Memory Controller SL9352, has the logic for the System Control, Memory Control, Data Control and chip select for some of the peripherals used in an AT system. The device is fully configurable via software. No external hardware jumpers are needed to utilize its features. Default values are provided to boot any system configuration. On reset, BIOS routines are used to program the device, transparent to the user, to utilize its special features.

Four configuration registers in the System Control Logic control the AT bus and peripheral bus operations. Synchronous and asynchronous bus operations are supported. In synchronous mode, bus clock is derived from the processor's CLK2. In asynchronous mode, it is derived from an independent external bus clock pin.

Support for page mode and non-page mode operation with non-interleave or word/multi-page interleave, along with programmable memory timing, allow the system designer to get maximum performance for the chosen DRAMs. High drive for RAS, CAS, memory address, and write lines are provided to connect SL9352 directly to a large DRAM memory array without external buffering. In addition, CAS for all the banks in non-interleave and 2-way interleave are provided to reduce external gates.

Shadowing features are supported in 16K granularity from 640K to 1M. Remap options allow shadowing of eight different combinations of top of memory, Local ROM, and Video ROM to 640K to 1M region.

VIA's System and Memory Controller, SL9352, can be used with two of VIA's SL9020 Data Controllers, or with discrete latches and buffers. Data direction and enable signals for the data controller are provided for both modes of operation.

SL9352 provides decoding for Real Time Clock and Keyboard Controller, thus avoiding external decoding gates. In addition, Port B logic, PS/2 Compatible Port 92 for fast reset, and A20GATE provide the necessary logic support for a one-chip solution.
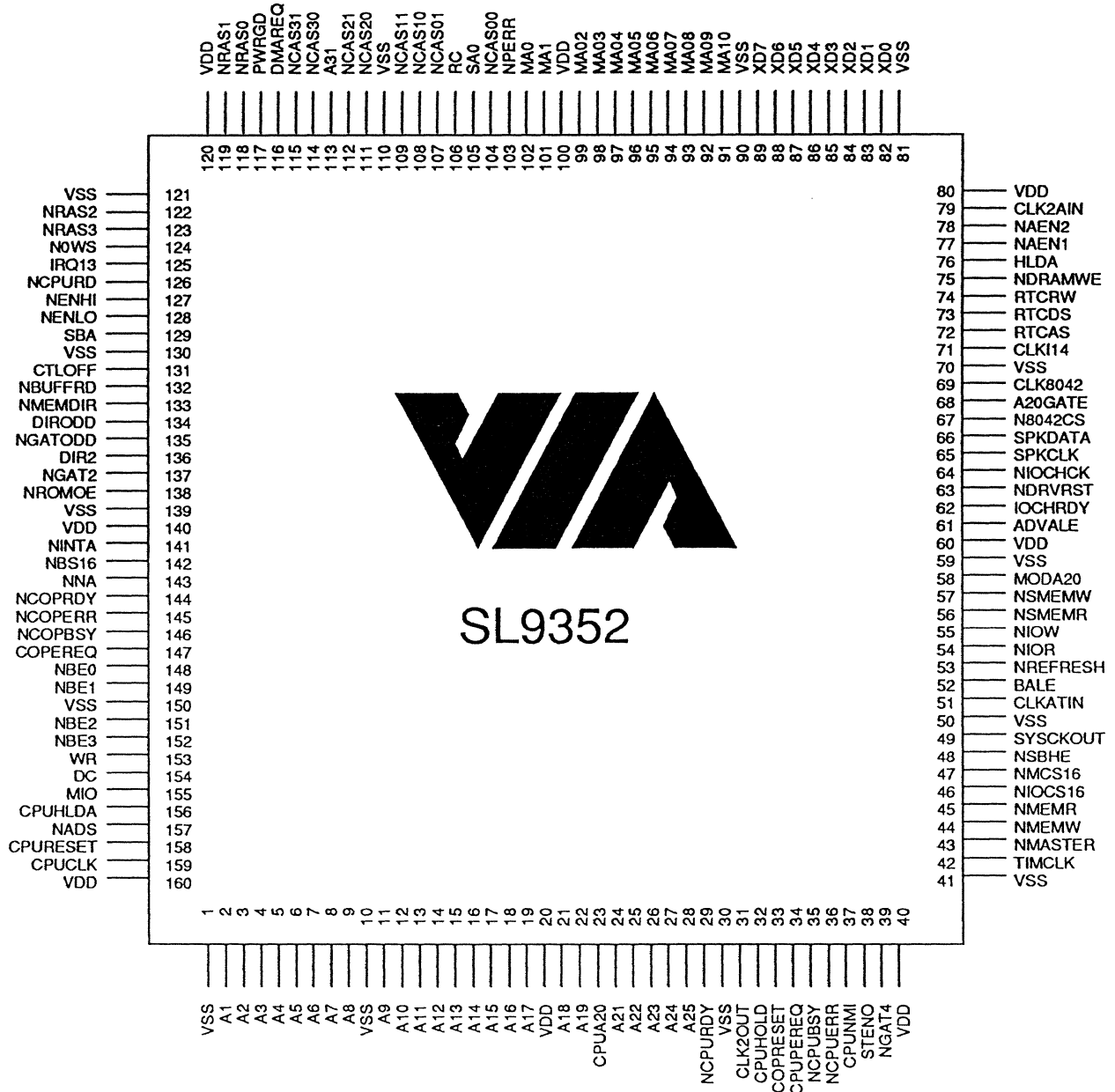
Figure 1 shows the Functional Block Diagram of SL9352. It is logically divided into 4 blocks:

1. System Control Logic
2. Memory Control Logic
3. Data Control Logic
4. Peripheral Control Logic

The following sections cover detailed operational descriptions of these four internal blocks.

Top pins (120–81):
VDD, NRAS1, NRAS0, PWRGD, DMAREQ, NCAS31, NCAS30, A31, NCAS21, NCAS20, VSS, NCAS11, NCAS10, NCAS01, RC, SA0, NCAS00, NPERR, MA0, MA1, VDD, MA02, MA03, MA04, MA05, MA06, MA07, MA08, MA09, MA10, VSS, XD7, XD6, XD5, XD4, XD3, XD2, XD1, XD0, VSS

Left pin	#		#	Right pin
VSS	121		80	VDD
NRAS2	122		79	CLK2AIN
NRAS3	123		78	NAEN2
NOWS	124		77	NAEN1
IRQ13	125		76	HLDA
NCPURD	126		75	NDRAMWE
NENHI	127		74	RTCRW
NENLO	128		73	RTCDS
SBA	129		72	RTCAS
VSS	130		71	CLKI14
CTLOFF	131		70	VSS
NBUFFRD	132		69	CLK8042
NMEMDIR	133		68	A20GATE
DIRODD	134		67	N8042CS
NGATODD	135		66	SPKDATA
DIR2	136		65	SPKCLK
NGAT2	137		64	NIOCHCK
NROMOE	138		63	NDRVRST
VSS	139		62	IOCHRDY
VDD	140		61	ADVALE
NINTA	141		60	VDD
NBS16	142		59	VSS
NNA	143		58	MODA20
NCOPRDY	144		57	NSMEMW
NCOPERR	145		56	NSMEMR
NCOPBSY	146		55	NIOW
COPEREQ	147		54	NIOR
NBE0	148		53	NREFRESH
NBE1	149		52	BALE
VSS	150		51	CLKATIN
NBE2	151		50	VSS
NBE3	152		49	SYSCKOUT
WR	153		48	NSBHE
DC	154		47	NMCS16
MIO	155		46	NIOCS16
CPUHLDA	156		45	NMEMR
NADS	157		44	NMEMW
CPURESET	158		43	NMASTER
CPUCLK	159		42	TIMCLK
VDD	160		41	VSS

SL9352

Bottom pins (1–40):
VSS, A1, A2, A3, A4, A5, A6, A7, A8, VSS, A9, A10, A11, A12, A13, A14, A15, A16, A17, VDD, A18, A19, CPUA20, A21, A22, A23, A24, A25, NCPURDY, VSS, CLK2OUT, CPUHOLD, COPRESET, CPUPEREQ, NCPUBSY, NCPUERR, CPUNMI, STENO, NGAT4, VDD

II. PIN DESCRIPTION SL9352

SYMBOL	TYPE	DESCRIPTION
		CLOCK AND RESET SIGNALS
CLKI14	I	Clock In 14.31818 MHz. 14 MHz input from oscillator.
CLK2AIN	I	Input Clock used to generate CLK2 and clock internal state machine. It is twice the frequency of the CPU clock.
CLKATIN	I	Asynchronous AT Clock Input. CLKATIN IS twice the BUSCLK frequency, generated from the oscillator.
CLK2OUT	O	Clock 2 Output to CPU.
CLK8042	O	CLK8042 is CLKI14 divided by two. It is the keyboard controller clock.
COPRESET	O	Reset 387 is an active HIGH output. It is generated in response to any one of the following signals: PWRGD, RC, and PS/2 Fast Reset. It is also asserted when I/O port 00F1 is written to. The signal is active for 96 CPUCLK cycles.
CPURESET	O	Reset Signal to the CPU is an active HIGH output. It is generated in response to any one of the following signals: PWRGD, RC and PS/2 fast reset.
NDRVRST	O	Device Reset is an active LOW output. It is used to reset the SL9025 Address Controller and Keyboard Controller.
PWRGD	I	Power Good is an active HIGH input from the power supply. A reset switch can be connected to this.
SYSCKOUT	O	System Clock Out is a free running system clock generated by dividing CPUCLK by 2. In synchronous mode this is synchronized with NADS. In asynchronous mode, this is generated from CLKATIN.
TIMCLK	O	1.19 MHz Timer Clock.
		CPU INTERFACE SIGNALS
A2-25	I/O	These are inputs for CPU, DMA, and AT bus MASTER accesses and outputs during refresh cycle. A2 to A11 has the refresh address (all with MSB). A12 to A25 are LOW during refresh.
A31	I/O	This is in input mode for CPU accesses. During HLDA output is LOW on this address line.

SYMBOL	TYPE	DESCRIPTION
		CPU INTERFACE SIGNALS Cont'd
A20GATE	I	Internal Adress 20 is forced LOW when A20GATE is LOW and is same as generated by CPU when A20GATE is HIGH.
ADVALE	O	Advanced Address Latch Enable from the memory control logic. It latches local bus address for the system bus.
CPUA20	I/O	CPU Address Bus, bit 20. Output for ATbus MASTER accesses.
CPUCLK	O	Clock synchronized with 386DX internal clock. It is CLK2 divided by two.
CPUNMI	O	CPU Non-Maskable Interrupt, generated from PERR or IOCHCK. Output to 80386.
CPUPEREQ	O	CPU Processor Extension Request. When active (HIGH) it indicates to CPU that NPX is ready for data transfer to/from its data FIFO. When FIFO is empty, this signal is negated. CPUPEREQ connects directly to the PEREQ pin on the CPU.
DC	I	CPU Status Signal. Differentiates between Data and Control instructions.
MIO	I	Memory Input/Output signal from the CPU. When HIGH, it indicates a memory cycle, when LOW, it indicates an I/O cycle.
MODA20	I/O	CPU Address 20 gated with A20GATE.
NADS	I	Address Strobe is an active LOW input generated by the CPU. When asserted it indicates the start of a new cycle.
NNA	O	CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle.
WR	I	CPU output control signal Write.
		MEMORY INTERFACE SIGNALS
MA0-MA10	O	RAM Address Bus Output. Directly drives DRAM address inputs.
NCAS00	O	Memory column address strobe. Asserted when CPU, DMA or MASTER is accessing Bank 0, byte 0.

PIN DESCRIPTION SL9352 (Cont'd)

SYMBOL	TYPE	DESCRIPTION
		MEMORY INTERFACE SIGNALS Cont'd
NCAS01	O	Memory Column Address Strobe for Bank 0, byte 1.
NCAS10	O	CAS for Bank 0, byte 2.
NCAS11	O	CAS for Bank 0, byte 3.
NCAS20	O	CAS for Bank 1, byte 0.
NCAS21	O	CAS for Bank 1, byte 1.
NCAS30	O	CAS for Bank 1, byte 2.
NCAS31	O	CAS for Bank 1, byte 3.
NCOPBSY	I	Numerical Coprocessor (NPX) Busy is an active LOW input indicating that NPX is currently executing a command. It is used to generate busy signal to the CPU, NCPUBUSY.
NDRAMWE	O	Active Low Memory Write signal. Used to drive DRAM write input.
NMEMDIR	O	Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is also used to drive SL9020 NMEMDIR input when using the SL9020.
NPERR	I	Parity Error from the SL9020 Data Controller.
NRAS0-3	O	Row Address Strobes for Banks 0,1,2 and 3 for the on-board memory. Generated during CPU, DMA or MASTER cycle for memory access. Used to directly drive DRAM RAS inputs.
NROMOE	I/O	Bi-directional pin which enables ROM output during ROM read cycles. During power-up, this is an input, and if pulled LOW an 8 bit ROM is assumed. Connects directly to ROMOE pin.
		COPROCESSOR INTERFACE SIGNALS
COPEREQ	I	NPX Peripheral Request is an active HIGH input from NPX. When asserted it causes CPUPEREQ to assert, indicating to the CPU that NPX is ready to transfer data to/from its data FIFO. When all data is written to or read from the data FIFO, PEREQ is negated.

SYMBOL	TYPE	DESCRIPTION
COPROCESSOR INTERFACE SIGNALS Cont'd		
IRQ13	O	Interrupt Request 13 is an active HIGH output which indicates an interrupt from the numeric coprocessor. It connects to the SL9030 pin IRQ13.
NCOPERR	I	NPX Error is an active LOW input from 80X87. When asserted it indicates that a non-maskable exception has occurred during the current command cycle. It is used to generate NCPUERR.
NCOPRDY	I	Coprocessor Ready is an active LOW input from the NPX to terminate an NPX bus cycle.
NCPUBSY	O	CPU Busy is an active LOW output to the CPU indicating that the NPX is busy executing a command. It connects to the CPU pin BUSY.
NCPUERR	O	CPU Error is an active LOW output from the NPX to the CPU indicating that an unmasked error condition exists. NCPUERR connects to the ERROR input pin on the CPU.
STENO	O	Status Enable is an active HIGH output. This pin serves as a chip select for the 80387. When inactive, it forces the NPX outputs NBUSY, PEREQ, NERROR and NRDY into floating state.
BUS CONTROL AND INTERFACE SIGNALS		
A1	I/O	Input for DMA and AT bus MASTER. Output for CPU and Refresh cycles. CPU access byte enable 1 and 0 are combined to generate A1. During refresh cycles, refresh counter LSB is output on this.
ADVALE	O	Advanced Address Latch Enable from the memory control logic. It latches local bus address for the system bus.
BALE	O	Buffered Address Latch Enable. Directly drives AT slot signal BALE.
CTLOFF	O	Control Output Flag. Rising edge clocks data from SD[7:0] to D [7:0] latches during Bus-conversion cycles. Connects directly to the SL9020 pin CTLOFF.
DIR2	O	Controls data transfer direction between D16-D31 and SD0-SD15.

SYMBOL	TYPE	DESCRIPTION
		BUS CONTROL AND INTERFACE SIGNALS Cont'd
DIRODD	O	Direction ODD. Controls data transfer direction between SD[7:0] and SD[15:8] in the SL9020 Data Controller. NGAT1 must be asserted. It is used during data conversion (8 bit SLOT Read/Writes) cycles.
IOCHRDY	I/O	I/O Channel Ready is an active HIGH input from the AT bus. When LOW it indicates a not ready condition and inserts wait states in AT bus or peripheral bus cycles. It is used to generate NCPURDY. It is an output during NPX reset cycle.
NAEN1,2	I	DMA Enable 1,2 are active LOW inputs from the SL9030. When NAEN1 is asserted LOW it indicates an 8-bit DMA cycle. When NAEN2 is asserted LOW it indicates a 16-bit DMA cycle. When both are HIGH it indicates that a non-DMA device owns the system's bus controls. They should not be LOW at the same time. They are used to generate direction control signals NSBHE, SBA, NENHI and NENLO.
NBE0	I	Active LOW Byte Enable 0 from CPU.
NBE1	I	Active LOW Byte Enable 1 from CPU.
NBE2	I	Active LOW Byte Enable 2 from CPU.
NBE3	I	Active LOW Byte Enable 3 from CPU.
NBUFFRD	O	Direction control for buffer between SD Bus and XD Bus.
NBS16	O	CPU control input signal, Bus size 16. Activates 16-bit data bus operation; data is transferred on the lower 16 bits of the data bus.
NCPURD	O	CPU Read is an active LOW output to the SL9020 Data Controller that sets the direction of data between D0-D15 and SD0-SD15. When asserted, the direction is from SD to D.
NCPURDY	O	Ready to CPU to terminate the cycle. Ready for local RAM, ROM (16 or 8 bit) accesses, on-chip I/O and AT bus accesses are generated in SL9352. External Coprocessor ready is input to 9352 and is OR'd with internal ready.
NENHI	O	Enable HIGH byte to the SL9020 Data Controller, is asserted LOW to enable HIGH byte data transfer between D8-D15 and SD8-SD15.

SYMBOL	TYPE	DESCRIPTION
BUS CONTROL AND INTERFACE SIGNALS Cont'd		
NENLO	O	Enable LOW byte to the SL9020 Data Controller, is asserted LOW to enable LOW byte data transfers between D0-D7 and SD0-SD7.
NGAT2	O	Active LOW buffer enable control to transfer between D16-D23 and SD0-SD7.
NGAT4	O	Active LOW buffer enable control to transfer between D24-D31 and SD8-SD15.
NGATODD	O	This is asserted LOW to enable the data buffer between HIGH byte and LOW byte of SD Bus. It is used in bus conversion cycles to assemble 8 bit bytes into 16 bit words in the SL9020 Data Controller.
NIOCHCK	I	I/O channel check. Active LOW signal from AT bus to assert CPUNMI.
NIOR	I/O	Input/Output Read is an active LOW bi-directional signal. It is an output when CPU is reading peripheral or AT bus ports. It is an input for DMA and AT bus Master.
NIOW	I/O	Input/Output Write is an active LOW bi-directional signal. It is an output when CPU is writing to peripheral or AT bus ports. It is an input for DMA and AT bus Master.
NMASTER	I	External Master is an active LOW input from the AT bus. When asserted, indicates that an external master device is currently active.
NMCS16	I	Memory Chip Select 16 is an active LOW input from the AT bus. When asserted indicates a 16 bit memory cycle. When HIGH it implies an 8-bit memory transfer. It is used to control NGATODD.
NMEMR	I/O	Memory Read is an active LOW bi-directional signal. It is an output when CPU is reading peripheral or AT bus memory, and during refresh cycle. It is an input for DMA and AT bus Master.
NMEMW	I/O	Memory Write is an active LOW bi-directional signal. It is an output when CPU is writing peripheral or ATbus memory. It is an input for DMA and AT bus Master.

PIN DESCRIPTION SL9352 (Cont'd)

SYMBOL	TYPE	DESCRIPTION
BUS CONTROL AND INTERFACE SIGNALS Cont'd		
N0WS	I	Zero Wait State is an active LOW input from the AT System bus. It causes termination of a bus cycle.
NSBHE	I/O	Byte HIGH Enable is an active LOW bi-directional pin for the AT bus. It indicates the transfer of data on the HIGH byte of the data bus. It is also asserted for 16-bit bus cycles. It is an output for CPU and DMA cycles and an input for an external master cycle.
NSMEMR	O	System Memory Read is active for a read access to lower 1 Meg memory. All other times it is tri-stated.
NSMEMW	O	System Memory Write is active for a write access to lower 1 Meg memory. All other times it is tri-stated.
SA0	I/O	System Bus Address 0-bit. It is a bi-directional pin. It is an output for CPU, Refresh and an input for DMA and AT bus Master.
SBA	O	Select Data Buffer Data. This signal drives the SL9020 Data Controller. When HIGH it selects latched SD Bus LOW byte data during bus conversions cycles. When LOW, unlatched SD Bus LOW byte data will pass onto D Bus.
HOLD INTERFACE SIGNALS		
CPUHLDA	I	CPU Hold Acknowledge. It is active HIGH when bus is granted in response to hold request (HOLD). It is used to generate HLDA.
CPUHOLD	O	Hold is asserted HIGH whenever another bus master device like DMA or an external master wants to become a bus master. The signal goes to the CPU.
DMAREQ	I	DMA Request is asserted HIGH to request a bus from CPU. It initiates hold request (HOLD) to the CPU for a DMA cycle to begin. Normally, SL9030 IPC's CPUHRQ is connected to this.
HLDA	O	Hold Acknowledge is an active HIGH output to the SL9030 Integrated Peripheral Controller. When asserted it indicates that CPU has released its control on the local bus in favor of another bus master device (DMA external master). It is generated by resynchronizing CPUHLDA with CPUCLK.

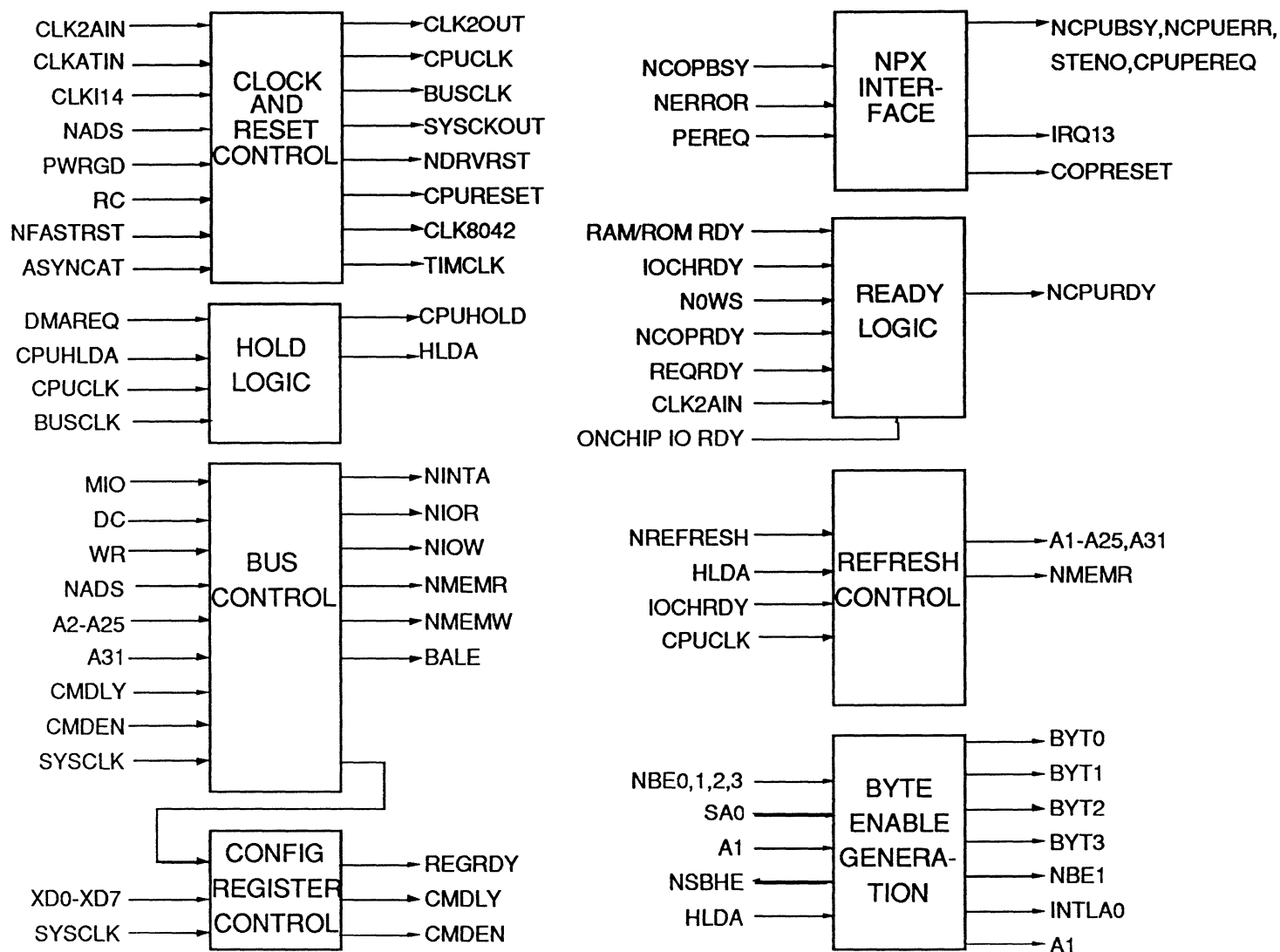| SYMBOL	TYPE	DESCRIPTION
		HOLD INTERFACE SIGNALS Cont'd
NREFRESH	I	On-board RAM refresh signal.
		PERIPHERAL INTERFACE SIGNALS
N8042CS	O	Active LOW keyboard controller chip select.
NINTA	O	Interrupt Acknowledge is an active LOW output for the interrupt controller. It is also used to direct data from the XD bus to SD bus during an interrupt acknowledge cycle.
NIOCS16	I	Peripheral I/O Chip select 16 is an active LOW input. It is asserted from AT bus by a 16-bit I/O device to indicate a 16-bit bus cycle. When HIGH it implies an 8-bit I/O transfer. It is used to control NGATODD.
RC	I	External CPU Reset is an active LOW input. When asserted it resets the CPU by generating CPURST. It is connected to the Keyboard Controller.
RTCAS	O	Active HIGH Real Time Clock Address Strobe.
RTCDS	O	Active LOW Real Time Clock Address Strobe.
RTCRW	O	Active LOW Real Time Clock Write Enable.
SPKCLK	O	Speaker clock.
SPKDATA	O	Active HIGH speaker data output. This is used to gate the timer tone signal to the speaker.
XD0-XD7	I	Peripheral data bus to read/write SL9352 registers.
		POWER AND GROUND SIGNALS
VDD	-	+5V. Power.
VSS	-	0V. Ground.

Fig. 2 System Control Logic Block Diagram

III. SYSTEM CONTROL LOGIC

Figure 2 shows the block diagram of system control logic. System control is divided into nine sections:

a. Clock and Reset Control
b. Hold Logic
c. Bus Control Logic
d. Coprocessor Interface
e. Ready Logic
f. Refresh Counter Logic
g. Byte Enable Generation
h. Bus Size 16 Logic
i. PS/2 Compatible Port 92

a. Clock and Reset Control

The clock inputs to the chip are:

1. CLK2AIN
2. CLKI14.

The processor clock, CLK2, CPUCLK, and system clock SYSCKOUT are derived from CLK2IN. In asynchronous mode SYSCKOUT is derived from CLKATIN. Asynchronous clock selection for the system clock is performed using the control bit ASYNCAT in register 18h. CLKI14 is the 14MHz clock used to derive the 8042 clock and TIMCLK.

SL9352 generates CPU reset (CPURST), Coprocessor reset (RST387) and system bus reset (NDRVRST) from PWRGD, RC and PS/2 compatible port 92 fast reset. External reset through a switch can be provided by pulling PWRGD line low. RC is the keyboard controller output that generates software reset. CPURST will go active from 3 to 11 CPUCLK's after RC is asserted. It will go inactive either 16 CPUCLK's later or 16 CPUCLK's after RC is negated. An equivalent high speed reset can be generated through port 92 bit 0. As with RC and fast reset, CPURST will go active within 3 to 11 CPUCLK's of detecting the shutdown command and be negated 16 CPUCLK's later. CPURST is always asserted and negated at the beginning of Phase 1.

b. Hold Logic

The hold request to CPU and hold acknowledge to external devices (e.g. SL9030) are synchronized with CPUCLK and BUSCLK. External devices requesting the bus should assert DMAREQ and use HLDA as the hold acknowledge.

c. Bus Control Logic

SL9352 contains logic to generate bus command and control signals in four basic modes. The most commonly used is CPU mode. This is active whenever there is no HLDA. The three other modes, DMA mode, MASTER mode and REFRESH mode, can be active only when HLDA is high.

During CPU mode the commands NMEMR, NMEMW, NIOR, NIOW are in output mode. One of these is asserted for an ATbus or peripheral bus access. The command delay can be programmed separately for read and write accesses through register 1Bh.

c. Bus Control Logic, cont'd

The bus activity and direction of the SL9352 pins depend on the mode. DMA is master when NAEN1 or NAEN2 (but not both) is asserted during HLDA. If NREFRESH is asserted during HLDA, it is in refresh mode. AT bus Master is master when NMASTER is asserted during HLDA. The following table lists the various signals and their direction for the modes mentioned above:

SIGNAL	MODE			
	CPU	DMA	AT Bus MASTER	REFRESH
NMEMR	O	I	I	O
NMEMW	O	I	I	I
NIOR	O	I	I	I
NIOW	O	I	I	I
SA0	O	I	I	I
NSBHE	O	O	I	O
A2 - A25	I	I	I	O
A31	I	O	O	O
CPUA20	I	I	O	I
LA20	O	O	I	O

O = Output   I = Input

Table 1 Signal Direction Descriptions

d. Coprocessor Interface

SL9352 generates reset for coprocessor 387 and is asserted whenever CPURST is asserted. It can also be activated through an I/O write to address 0F1h. It is active for 96 CPUCLK cycles. IOCHRDY will be asserted when RST387 is active. It will be negated 95 CPUCLK's after RST387 is negated.

From reset until the first CPU cycle, coprocessor error NERROR is routed to the CPU as NCPUERR. If coprocessor error is detected during coprocessor busy period, STENO is negated and interrupt request 13 is asserted. It also latches CPUBUSY. CPUBUSY is asserted to prevent the processor from accessing the co-processor until the error handling routine is completed. The interrupt handler clears the latched BUSY condition, by performing a dummy write to I/O port 0F0h. STENO and IRQ13 are also negated by writing to port 0F0h.

e. Ready Logic

SL9352 generates ready for DRAM, on-chip I/O and bus accesses. Wait states for DRAM accesses can be programmed separately for HIT and MISS cycles through register 08h. For the same number of wait states the pipeline mode ready will be one CPUCLK later compared to non-pipeline mode ready. On-chip I/O accesses have 1 wait state. The bus access wait states can be programmed separately for 16 bit and 8 bit devices. They can also be programmed separately for memory and I/O devices using registers 19h and 1Ah. IOCHRDY can be used to extend the cycle. Wait states are introduced until IOCHRDY is de-asserted. N0WS overides IOCHRDY and programmed wait states and the current cycle is terminated as soon as it is detected internally and synchronized to CPU CLK2. These three ready sources are combined with NCOPRDY (coprocessor ready) to generate the ready to the CPU.

f. Refresh Logic

SL9352 contains logic for refresh counter and refresh RAS generation. Refresh cycle starts when NREFRESH is asserted low and HLDA is active. Staggered refresh is enabled by setting the two stagger RAS control bits in register 12h. During refresh NRAS0-3 are asserted low, NCAS00 and NCAS31 are held high, and the current bus state is ignored. Refresh counter is incremented at the end of the refresh cycle. Refresh address is output on A1 to A11. NMEMR is asserted during the refresh cycle.

g. Byte Enable Generation

Four byte enable controls for asserting CAS are generated using the four byte enables from the CPU, A1, SA0 and NSBHE. In CPU mode the four byte enables from the CPU are selected. During DMA and MASTER address input A1 decides the word, and SA0 and NSBHE decide the low or high byte within a word. During DMA mode, NSBHE is generated internally by SL9352, based on 8 bit or 16 bit DMA.

h. Bus Size 16 Logic

SL9352 asserts active low bus size 16 to 80386DX CPU for all ROM, on-chip I/O and bus accesses. For 8 bit ROM, BS16 is asserted in addition to data conversion cycle.

i. PS/2 Compatible Port 92

PS/2 compatible port 92 to issue fast reset and fast A20GATE are provided in SL9352. On reset, fast reset logic is disabled. It can be enabled through bit 1 of register 13h.

SL9352's Memory Control Logic section provides the control interface between CPU, DMA, MASTER and local DRAM for non-interleave and interleave modes of operation in page mode and non page mode. In page mode either single page and multiple pages can be active simultaneously.

In page non-interleave mode there is only one page active. The page size is 2K bytes for 256K, 4K bytes for 1M and 8K bytes for 4M memories. It is doubled for 2-way word interleave and quadrupled for 4-way word interleave. For multiple page interleave there can be a maximum of four different pages: one page for each bank with four banks. Page size of each of these pages is same as in page non-interleave mode.

IV. MEMORY CONTROL LOGIC

Figure 3 shows the block diagram of the Memory Control Logic. It is logically divided into six sections:

   a. Address Decode
   b. HIT/MISS Detection
   c. RAS/CAS Logic
   d. Memory Address Generation
   e. Next Address and Ready Logic
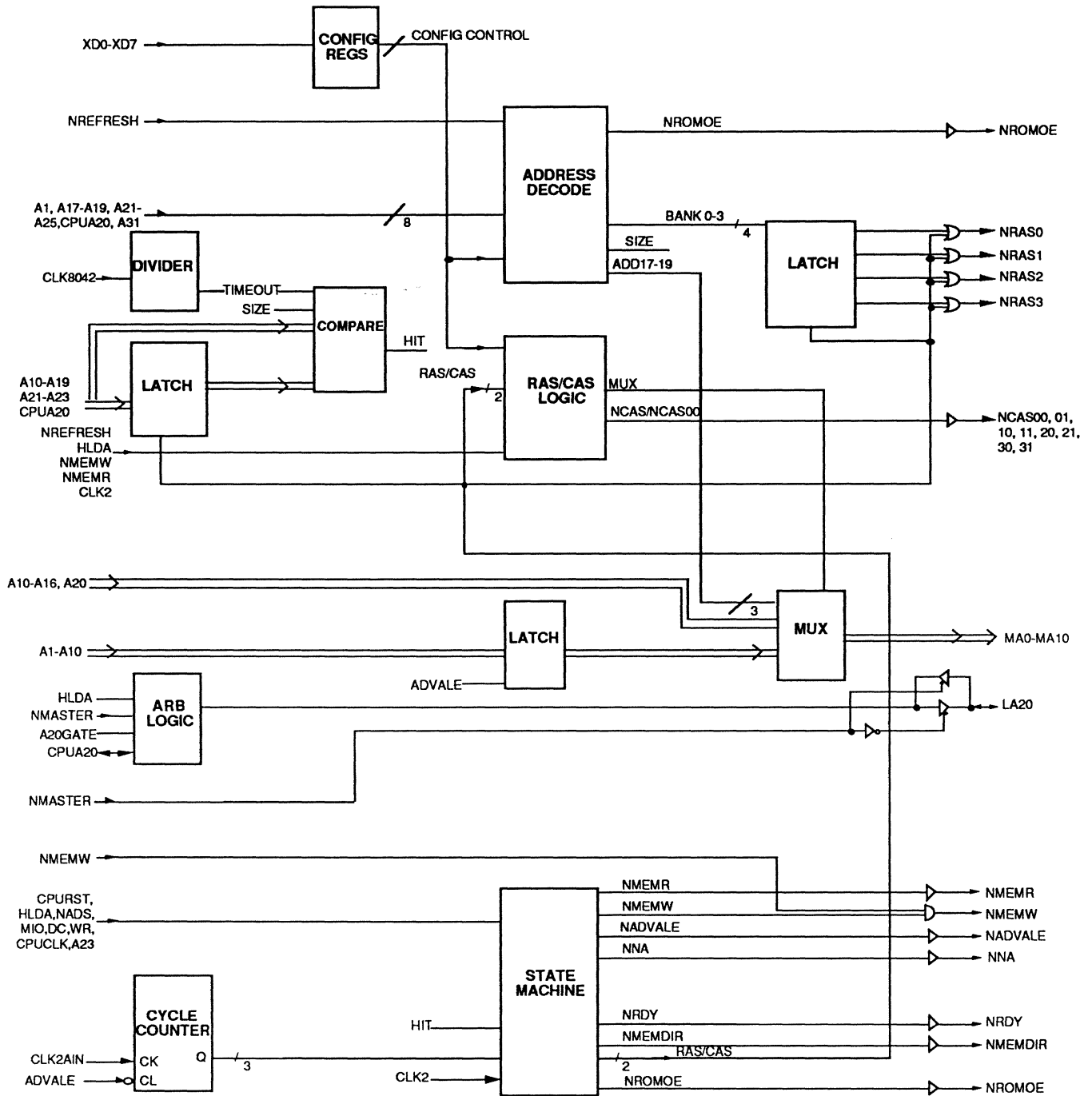   f. ROM Data Conversion Logic

Fig. 3 Memory Control Logic Block Diagram

a. Address Decode

In addition to shadow and remap decoding, SL9352 provides all necessary circuitry to decode on-board RAM, ROM, and on-chip I/O. Sixteen memory type and select combinations can be chosen to support one to four banks using 256K, 1M, 4M or a mix of these using regular and static column DRAMs. The controller can be configured for 640K bytes to 64M bytes. The memory address range for different bank select codes for page mode (non-interleave and multi-page interleave) and non-page mode are shown in Table 2. The bank selection code is written to register 11h.

For page word interleave, the selection code and size are the same as shown in Table 2 except that the address range of the bank depends on address A2 for 2-way interleave and addresses A2 and A3 for 4-way interleave.

D3	D2	D1	D0	BANK 0	BANK 1	BANK 2	BANK 3	MEMORY
0	0	0	0	0-640K/SHDW				1M
0	0	0	1	0-640K/SHDW	1M-2M			2M
0	0	1	0	0-640K/SHDW	1M-2M	2M-3M		3M
0	0	1	1	0-640K/SHDW	1M-2M	2M-3M	3M-4M	4M
0	1	0	0	0-640K/SHDW	1M-5M			5M
0	1	0	1	RESERVED				
0	1	1	0	0-640K/SHDW	1M-2M	2M-6M		6M
0	1	1	1	0-640K/SHDW	1M-2M	2M-6M	6M-10M	10M
1	0	0	0	0-640K/1M-16M/SHDW				16M
1	0	0	1	0-640K/1M-16M/SHDW	16M-32M			32M
1	0	1	0	0-640K/1M-16M/SHDW	16M-32M	32M-48M		48M
1	0	1	1	0-640K/1M-16M	16M-32M	32M-48M	48M-64M	64M
1	1	0	0	0-640K/1M-4M/SHDW				4M
1	1	0	1	0-640K/1M-4M/SHDW	4M-8M			8M
1	1	1	0	0-640K/1M-4M/SHDW	4M-8M	8M-12M		12M
1	1	1	1	0-640K/1M-4M/SHDW	4M-8M	8M-12M	12M-16M	16M

Table 2 Bank Select Codes and Memory Address Range

`SHDW' corresponds to the 384K memory available from 640K to 1M. This area corresponds to the shadow address range or remap range. Shadow address range is decoded based on the bits set in registers 00h to 07h and the remap decoding is based on the remap register (09h) setting. Remap RAM address is always above the maximum DRAM memory specified in Table 2 for the selected memory select code. The programmer should make sure two or more address ranges do not overlap to the same physical area.

On reset, ROM is decoded from FE0000h to FFFFFFh and from 0F0000 to 0FFFFF. The second area can be disabled by resetting bits 0 and 1 in ROM control register 0Ch. Local ROM can be decoded from 0C0000 to 0EFFFF in 16k granularity by setting the control bits in ROM control register 0Ah and 0Bh. For the selected address range NROMOE is asserted active low.

b. Hit/Miss Detection

SL9352 supports both page non-interleave and page interleave modes of operation. In page mode, there is only one page active and the page size is 2K bytes for 256K, 4K bytes for 1M and 8K bytes for 4M memories. The page size is doubled for 2-way word interleave and quadrupled for 4-way word interleave. For multi-page interleave, there can be a maximum of four different pages, one page for each bank with four banks. Page size of each of these pages is the same as in page non-interleave mode.

After reset and after every HLDA cycle the first access to memory is treated as a MISS cycle asserting RAS and CAS as programmed in registers 0Dh, 0Eh, 0Fh, and 13h for MISS cycles. The page number is stored internally in a page register, and at the end of the cycle RAS is left low and CAS returned high. During all subsequent accesses, the access page number is compared with the stored page number and a HIT detected if they are same. If a mismatch (MISS) is detected, RAS is negated and asserted again after the programmed number of clocks for RAS precharge. The new page number is stored for subsequent cycle comparisons. For word page interleave on a MISS all banks' RAS's are negated and asserted together. For multiple page interleave only the bank for which there is a MISS will have its RAS negated. Thus, in multi-page interleave different banks can have different active pages. In non-page mode each access is treated as a MISS cycle.

c. RAS/CAS Logic

On-board memory timing is programmable as a multiple of CLK2. This gives unlimited flexibility in matching DRAM specifications to the CPU speed for optimal performance and cost. Four configuration registers are used for programming RAS and CAS precharge, and RAS to column address delay. These values can be different for HIT and MISS cycles and for read and write cycles. CAS is negated for every cycle and asserted after the specified number of CLK2's. RAS is negated for a MISS cycle and asserted after the specified number of CLK2's. The RAS and CAS access times are provided by programming the number of wait states correctly. The programmed values affect only CPU accesses. DMA, REFRESH and MASTER timings are fixed as shown in the timing diagrams. During refresh cycles, support for 1 or 2 CLK2 staggered refreshing is provided. During staggered refreshing, bank 0 RAS is asserted first and bank 3 RAS asserted last.

RAS timeout logic may be optionally enabled by setting bit 5 in register 10h to ensure that the RAS active time limit is not violated during page mode operation. If RAS remains active for a period greater than the selected period, RAS is negated during the next CPU access. The cycle is treated as a MISS cycle even if the access is to the same page.

d. Memory Address Generation

SL9352 provides the necessary circuitry to multiplex the access address as row address and column address. The physical address generated for row and column depends on the memory size and mode of operation. Table 3 gives the address generation process. Row address hold time (RAS to column address) can be programmed through register 0Dh.

MODE	MEMORY		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10
NON-INTERLEAVE	256K	ROW	11	12	13	14	15	16	17	18	19		
		COL	10	2	3	4	5	6	7	8	9		
	1M	ROW	21	12	13	14	15	16	17	18	19	20	
		COL	11	2	3	4	5	6	7	8	9	10	
	4M	ROW	21	22	13	14	15	16	17	18	19	20	23
		COL	11	2	3	4	5	6	7	8	9	10	12
2-WAY INTERLEAVE	256K	ROW	20	12	13	14	15	16	17	18	19		
		COL	10	11	3	4	5	6	7	8	9		
	1M	ROW	21	22	13	14	15	16	17	18	19	20	
		COL	11	12	3	4	5	6	7	8	9	10	
	4M	ROW	21	22	23	14	15	16	17	18	19	20	24
		COL	11	12	3	4	5	6	7	8	9	10	13
4-WAY INTERLEAVE	256K	ROW	20	21	13	14	15	16	17	18	19		
		COL	10	11	12	4	5	6	7	8	9		
	1M	ROW	21	22	23	14	15	16	17	18	19	20	
		COL	11	12	13	4	5	6	7	8	9	10	
	4M	ROW	21	22	23	24	15	16	17	18	19	20	25
		COL	11	12	13	4	5	6	7	8	9	10	14

TABLE 3 Address Generation

e. Next Address and Ready Logic

SL9352 provides logic for pipeline mode and non-pipeline mode CPU operation. Setting bit 3 in register 12h disables pipeline operation. In pipeline mode the next address to CPU is asserted for on-board DRAM accesses before ready is asserted. For the same number of wait states the ready for non-pipeline operation will be one CPUCLK earlier than in pipeline operation. The number of wait states for HIT and MISS can be programmed separately. In addition, the wait state for write cycles can be one less than the read. Next address is not asserted for ROM on-chip I/O and bus accesses.

f. ROM Data Conversion Logic

With SL9352, the system designer has the flexibility to choose 8 bit or 16 bit ROM. If NROMOE is pulled low on reset then 8 bit ROM is assumed and SL9352 does the necessary data conversion cycles for ROM accesses. During word access to ROM the low byte is accessed first (SA0 = 0) and latched. SA0 is then toggled to 1 and high byte is accessed. Ready to CPU is issued after the specified number of wait states for the second access. The first access also assumes the same number of wait states.
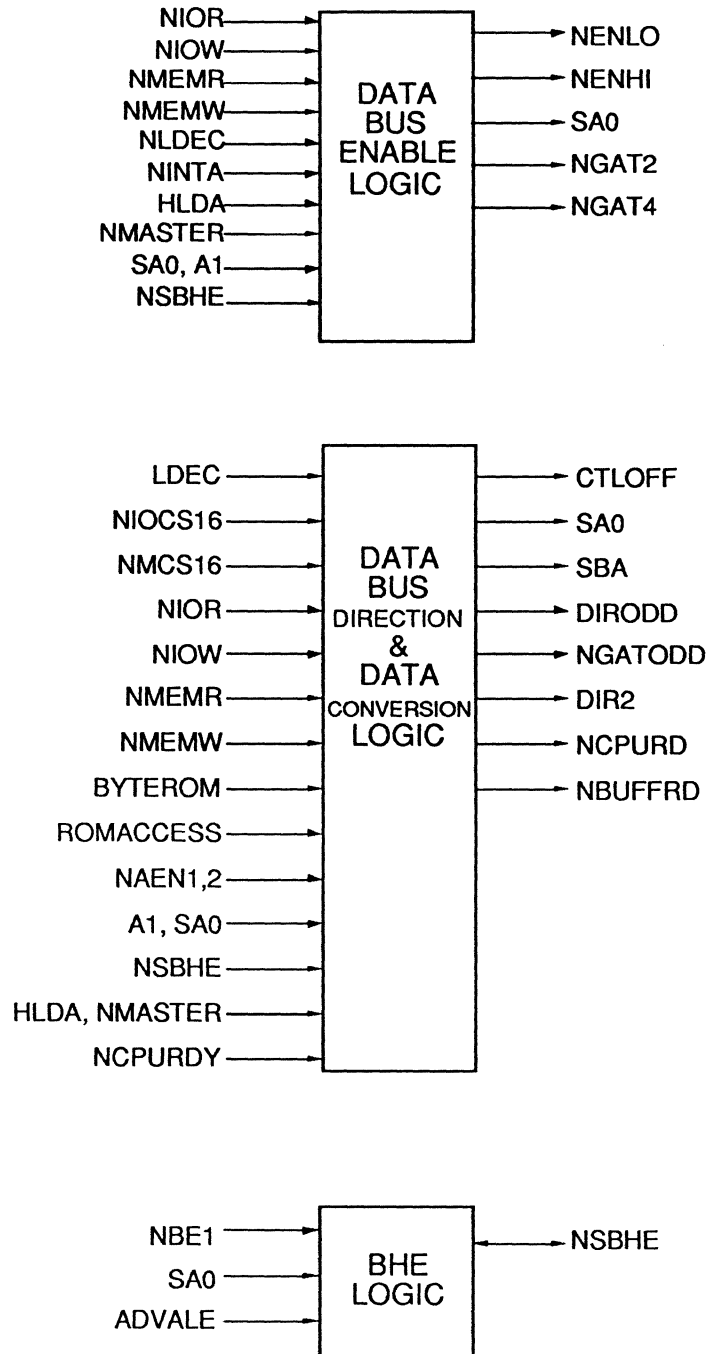
DATA BUS ENABLE LOGIC

Inputs:
- NIOR
- NIOW
- NMEMR
- NMEMW
- NLDEC
- NINTA
- HLDA
- NMASTER
- SA0, A1
- NSBHE

Outputs:
- NENLO
- NENHI
- SA0
- NGAT2
- NGAT4

DATA BUS DIRECTION & DATA CONVERSION LOGIC

Inputs:
- LDEC
- NIOCS16
- NMCS16
- NIOR
- NIOW
- NMEMR
- NMEMW
- BYTEROM
- ROMACCESS
- NAEN1,2
- A1, SA0
- NSBHE
- HLDA, NMASTER
- NCPURDY

Outputs:
- CTLOFF
- SA0
- SBA
- DIRODD
- NGATODD
- DIR2
- NCPURD
- NBUFFRD

BHE LOGIC

Inputs:
- NBE1
- SA0
- ADVALE

Output:
- NSBHE

Fig. 4 Data Control Logic Block Diagram

V. DATA CONTROL LOGIC

Figure 4 shows the block diagram of the Data Control Logic. The three major blocks are:

a. Bus Enable Logic
b. Bus Direction and Data Conversion Logic
c. High Byte Enable Logic

a. Bus Enable Logic

SL9352 provides logic support for use of an external SL9020 Data Controller, or TTL buffers and latches. SL9352 generates necessary buffer enable controls for these two modes of operation. System control register 19h, bit 0 must be set if the SL9020 Data Controller is used. The following five enable controls are used to enable the buffers between D and SD bus. NENLO and NENHI enable the low word, low and high byte respectively. NGATODD enables the swap buffer between SD0-SD7 and SD8-SD15. NGAT2 and NGAT4 are for enabling high word, low and high byte respectively. For all CPU accesses to AT bus and peripheral bus, bus size 16 is asserted to indicate a 16 bit device. Therefore, only NENLO, NENHI and NGATODD will be asserted during CPU mode access to the bus. NGAT2 and NGAT4 are asserted during DMA and AT bus MASTER for transfer to on-board 32 bit memory.

b. Bus Direction and Data Conversion Logic

The following signals control direction of AT bus and peripheral bus data buffers: NCPURD for low and high bytes of low word, DIRODD for the SD0-SD7 to SD8-SD15 swap buffer, DIR2 for low and high bytes of high word, and NBUFRD for XD0-XD7 to SD0-SD7 buffer. NMEMDIR is used with SL9020 to direct data to and from memory data bus when local memory is on MD bus. The following table lists directions of the data bus signals:

Signal	Direction	
NCPURD	0	SD to D
	1	D to SD
DIRODD	0	SD8-SD15 to SD0-SD7
	1	SD0-SD7 to SD8-SD15
DIR2	0	SD to D
	1	D to SD
NBUFRD	0	XD0-XD7 to SD0-SD7
	1	SD0-SD7 to XD0-XD7
NMEMDIR	0	MD to D
	1	D to MD

Table 4 Signal Directions

In addition to these enable and direction controls, SL9352 provides a clock and select signal for data conversion during word access to a byte port. CTLOFF is used to clock the low byte data, and SBA is used to select the latched data.

c. High Byte Enable Logic

NSBHE is ATbus byte high enable signal and is an input during MASTER mode and output at all other times. During CPU mode this is asserted whenever CPU accesses high byte of either word. During 8 bit DMA it is of opposite polarity to SA0 and during 16 bit DMA it is low.

VI. PERIPHERAL CONTROL LOGIC

Figure 5 shows the block diagram of Peripheral Control Logic. It provides logic for the following:

  a. Peripheral Address Decoding
  b. Port B Logic

a. Peripheral Address Decoding

SL9352 provides address decoding logic to support the Real Time Clock and Keyboard Controller. RTCAS, RTCRW and RTCDS are generated for write access to 70h, 71h, and read access to 70h respectively. Keyboard controller chip select goes active for port 60h read and write accesses. The number of wait states for these accesses depends on the programmed number of wait states for bus accesses. These devices are to be located on XD bus.

b. Port B Logic

SL9352 also provides the port B (address 61h) logic for CPUNMI, and speaker data.
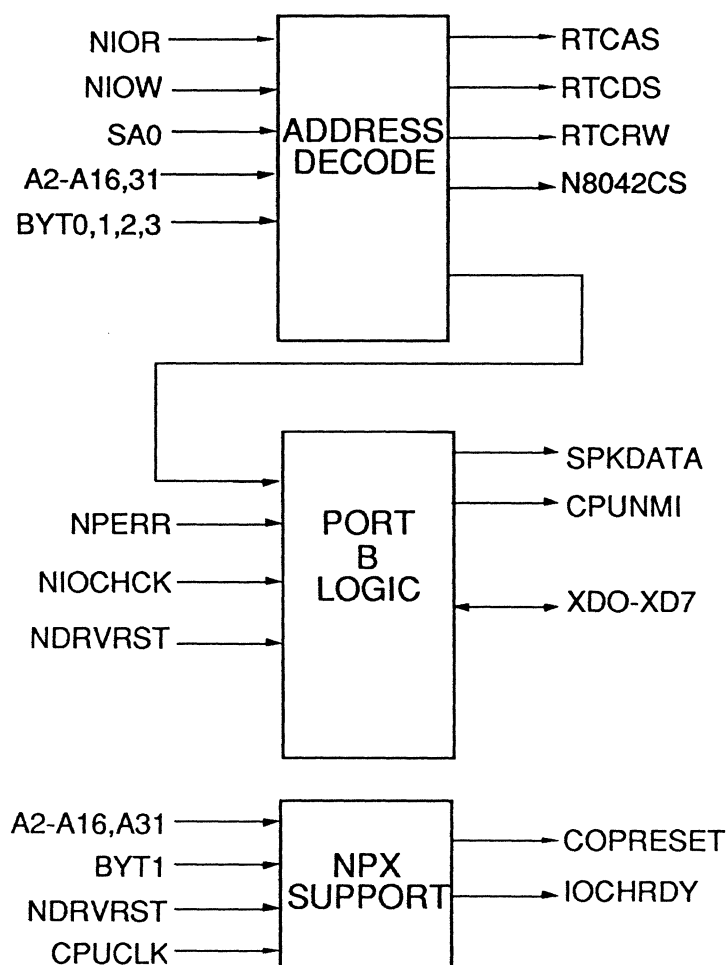
Fig. 5 Peripheral Control Logic Block Diagram

VII. CONFIGURATION REGISTERS

SL9352 provides 28 configuration registers for all programmable functions in the chip. All these registers are accessed through an index/data addressing scheme. Only one I/O address is used to access both index and data registers. The address defaults to 0122h after reset and can be remapped to any other unused I/O address (must be on byte 2 boundary) between 0000h and FFFFh by loading the new I/O address into the relocation registers. The addresses from these registers are transferred to a pipeline register, for comparing, with a write to configuration register 3 (using the unrelocated address i.e., 0122h) with bit 0 = 1. After this the temporary relocation registers are also in the new address space until the reset, when it defaults to 0122h.

The data registers are selected by writing their addresses in the index register. An internal pointer is used to determine whether the on-chip I/O write is for the index or data registers. After reset, the pointer points to the index register. Any write to the index register or data register will toggle the pointer. Only data registers can be read back and any read to the data registers will leave the pointer pointing to the index register.

The following table lists all the configuration registers by their index address, name and description:

INDEX ADDRESS	NAME	REGISTER
0	SDWREG0	Shadow control 0
1	SDWREG1	Shadow control 1
2	SDWREG2	Shadow control 2
3	SDWREG3	Shadow control 3
4	SDWREG4	Shadow control 4
5	SDWREG5	Shadow control 5
6	SDWREG6	Shadow control 6
7	SDWREG7	Shadow control 7
8	RAMWAIT	RAM wait state select
9	REMAP	Remap
A	ROMCTL1	Local ROM control register 1
B	ROMCTL2	Local ROM control register 2
C	ROMCTL2	Local ROM control register 3
D	RASTIM	RAS timing register
E	CASTIM1	CAS timing register 1
F	CASTIM2	CAS timing register 2
10	DISMEM	Disable to 0K
11	MEMTYPE	Memory type and size select
12	CONFIG1	Configuration register 1
13	CONFIG2	Configuration register 2
14	CONFIG3	Configuration register 3
15	IOMAPLOW	Relocation register low
16	IOMAPHI	Relocation register high
17	Reserved	
18	SYSCTL	System control register
19	WAIT16	System bus 16 bit device wait state select
1A	WAIT8	System bus 8 bit device wait state select
1B	CMDDLY	System bus command delay
1C	Reserved	
1D	Reserved	
1E	Reserved	
1F	RASMAP	RAS map register

Table 5 Configuration Registers

PACKAGE INFORMATION

160 Pin Flat Pack

ORDERING INFORMATION

Device Type:
SL9352

Package Type:
FP-Plastic Flat Pack

Temperature Range:
C- Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

SL9352 XX X
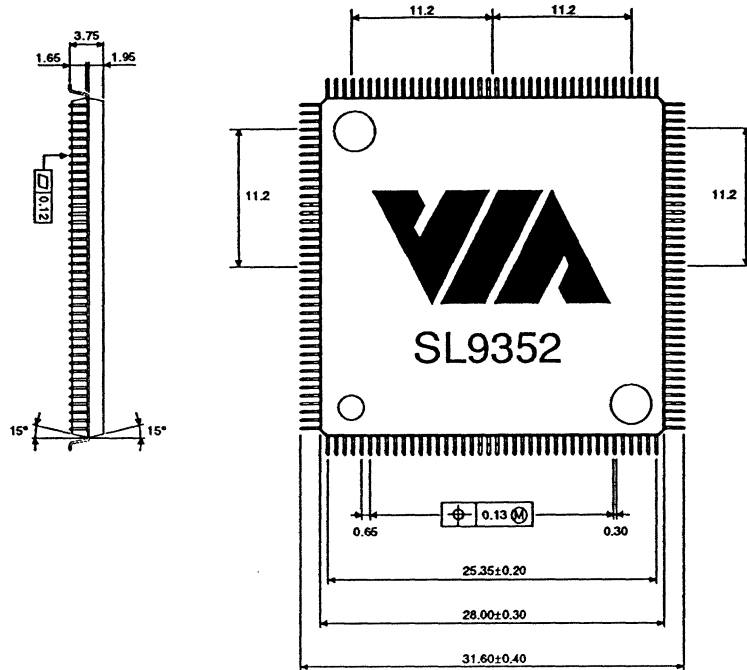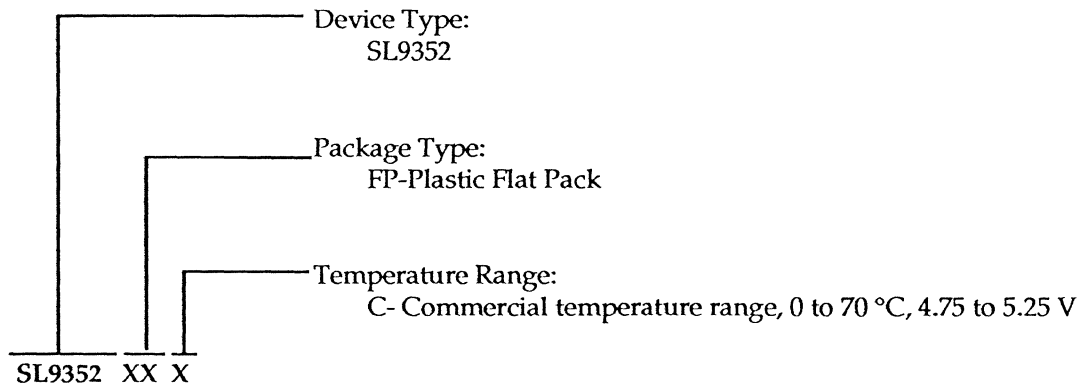
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